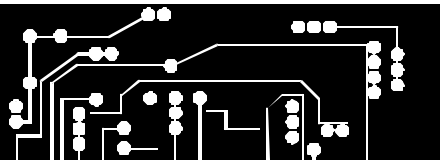
PowerPC Embedded Processors
Application Note



Performance Comparisons of the IBM PowerPC750L vs IBM PowerPC750CXe

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Abstract- This application note describes the effects of certain characteristics on the processor performance when comparing the features of the IBM™ PowerPC™ 750 PID-8p (PPC750L™) Microprocessor and the IBM PowerPC PPC750CXe™ Microprocessor (PPC750CXe). To illustrate performance differences, comparisons of PPC750CXe with PPC750L using various external cache sizes are explained.

Overview

The IBM PowerPC PPC750CXe is an implementation of the PowerPC750 that includes an internal 256KB L2 cache. On chip cache can be accessed at full processor speed as compared to off chip cache that is accessed at 50% processor speed. This is a major performance advantage for many applications. The PowerPC PPC750CXe also operates at significantly higher core speeds than the PPC 750L. The advantages of on chip cache and higher core speeds along with other differences in features will be discussed as follows.

The PPC750CXe with a smaller internal cache at processor speed performs very competitivel with the PPC750L with several external cache sizes at half the processor speed.

The PPC750CXe has a wider L1 cache data bus reload path width.

The higher core speed of the PPC750CXe allow for higher performance levels than the PPC 750L.

Higher maximum system bus speed is also available on the PPC750CXe.

The PPC750CXe has an additional FPU reservation station.

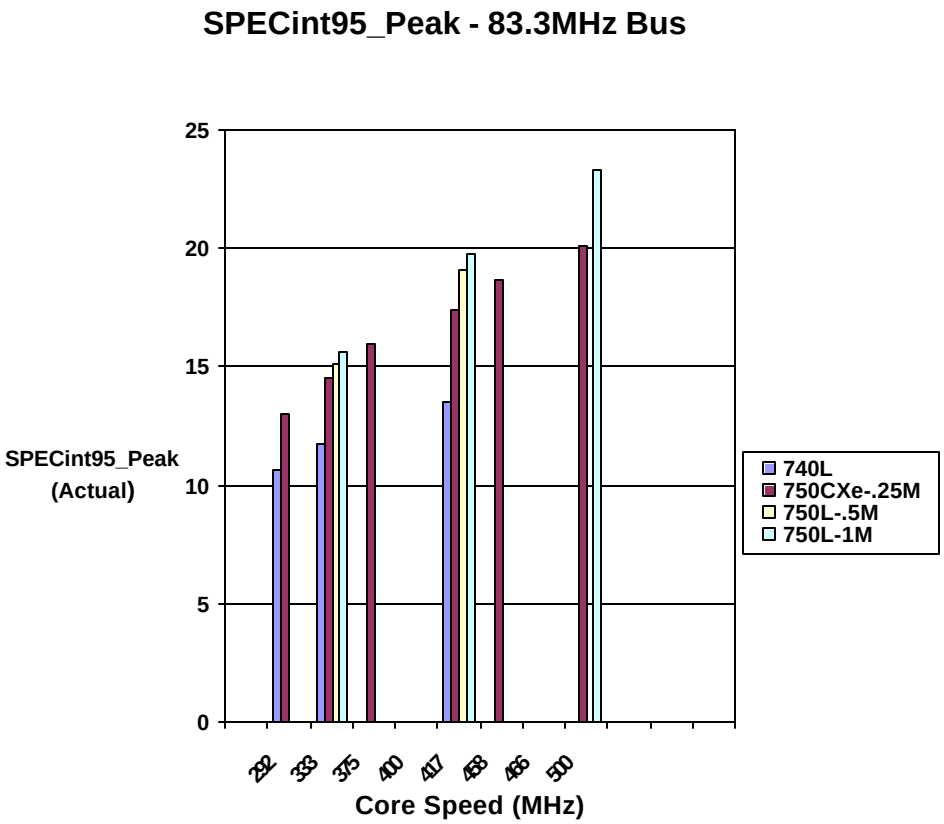
On the PPC750CXe the floating reciprocal estimate single instruction provides an estimate to a higher precision.

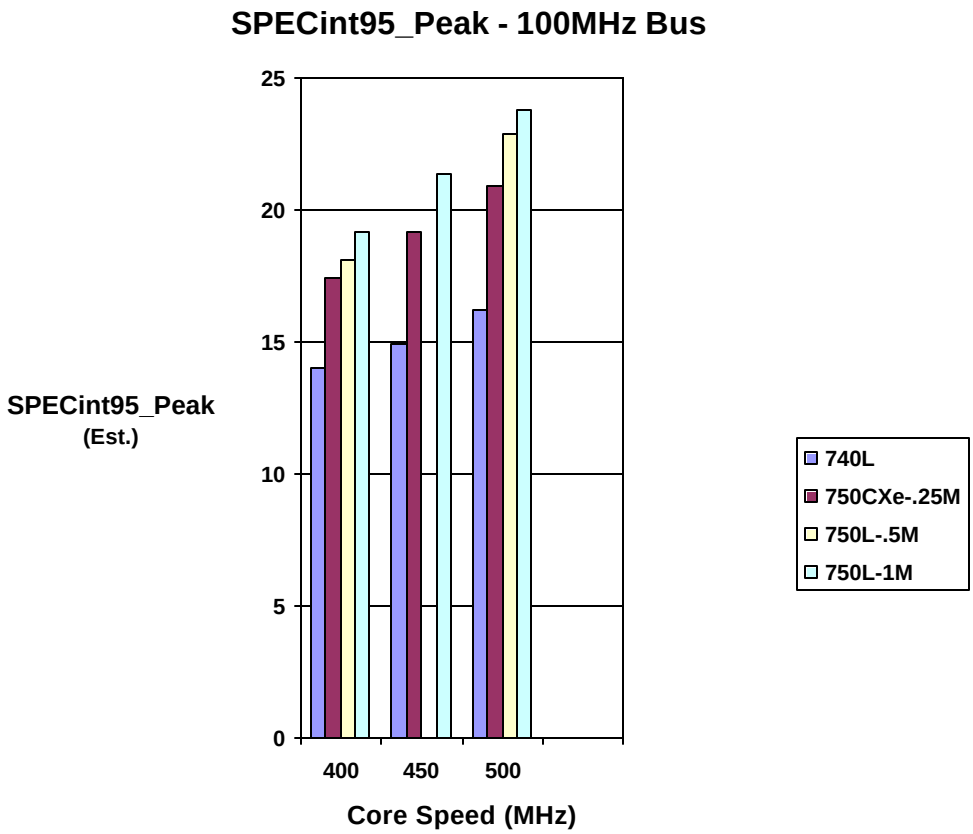
The floating point reciprocal square root estimate instruction provides and estimate to a higher precision.

The PPC750CXe has lower power dissipation at the same frequency.

1. Internal Cache

The performance advantage of the PPC750CXe that is derived from having the L2 cache accessible at the same speed as the processor is clearly evident in the chart below. Its performance is compared to that of the PPC750L with various cache sizes. In the following charts, the 740 represents the 750 with no external L2 cache.

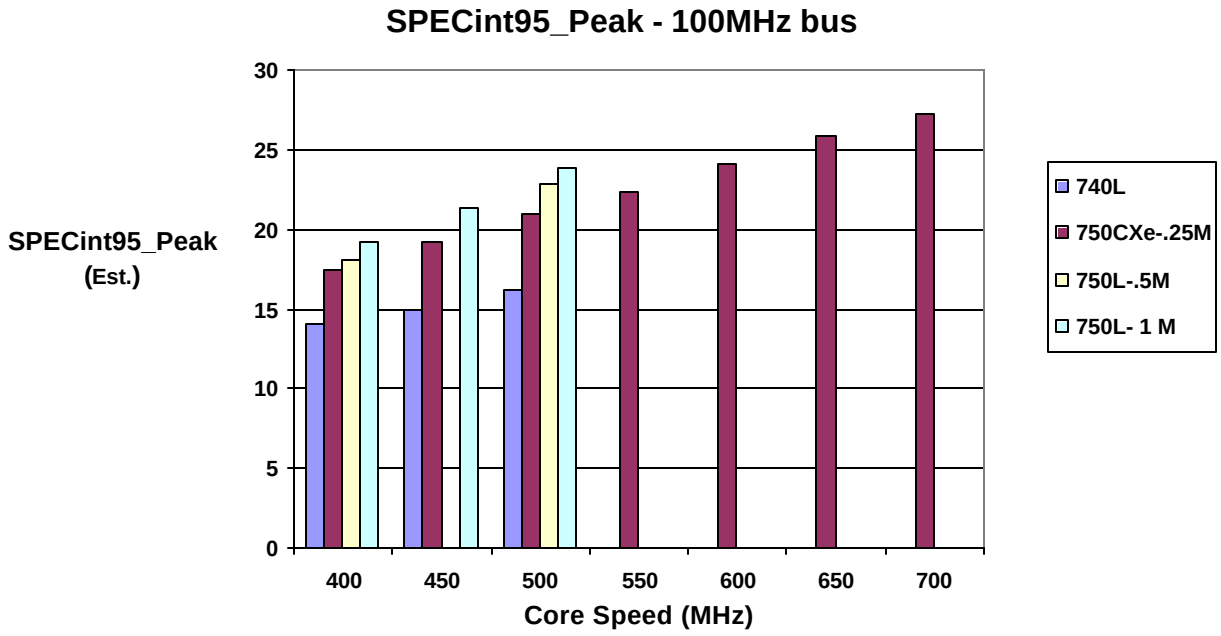




The chart data shows that the PPC750CXe running at 400MHz with a 0.25 MB internal L2 cache performs similarly to the PPC750L with significantly larger external L2 caches. As the core speed increases the differential in performance between the PPC750CXe and the PPC750L with larger caches at the same speed reflect that the PPC750L has a slight performance advantage. This aspect is compensated for in the PPC750CXe in that it can run at higher core and bus speeds. These characteristics are discussed in the next sections.

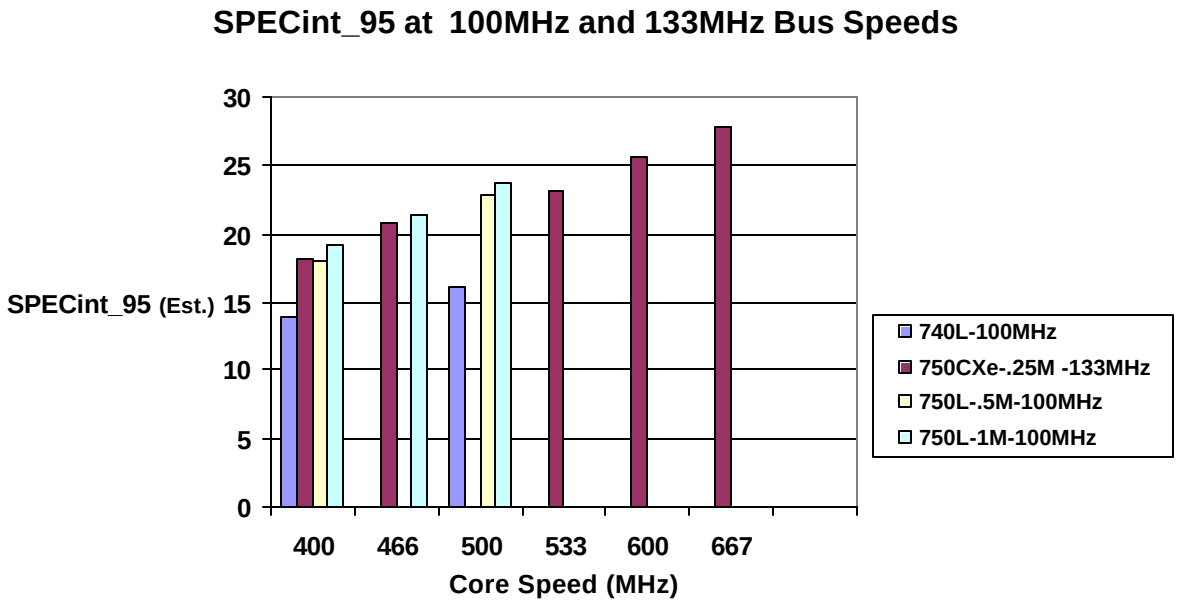
2. Core Speed

The PPC750CXe processor can run at speeds up to 700MHz. This larger range of speed increases the performance as expected. The following chart describes performance characteristic of the PPC750L with various cache sizes in comparison to the PPC750CXe running with higher core speeds.



3. Bus Speed

The maximum bus speed of the PPC750CXe is 133MHz while the maximum bus speed for the PPC750L is 100MHz. This next chart compares the performance of the PPC750CXe running with a 133MHz bus speed in relation to the PPC750L running with a 100MHz bus speed.



At 400MHz the PPC750CXe with its 1/4M cache and the 133MHz bus slightly outperforms the PPC750L with a larger 1/2M cache and 100MHz bus speed. The faster core speeds combined with the faster bus allow the PPC750CXe to advance into a range of performance that is well beyond that of the PPC750L.

Additional Features

The addition of another FPU reservation station in the PPC750CXe results in a higher throughput for applications that extensively use the floating point functionality.

Higher precision in the floating reciprocal square root estimate instruction and the floating reciprocal estimate single instruction allows for fewer iterations and enhances performance in applications that require these features. The PPC750CXe also has lower power dissipation than the PPC750L.

The following table summarizes some of the discussed features of the PPC750L and PPC750CXe.

Performance Features	**PPC750L**	**PPC750CXe**
L1 data bus reload path width	64 Bits	256 Bits
L2 cache size	L2 cache controller for external cache (256KB,512KB,1MB)	Internal 256 KB
FPU reservation stations	1	2
Fres precision	8 bits	12 bits
Frsqrte precision	5 bits	12 bits
Silicon Technology	0.22u copper	0.18u copper
Core Speed Range	300-500 MHz	366-700MHz
Maximum Bus Speed	100 MHz	133 MHz
Power Dissipation (typical) at 500Mhz, 1.89 V 65C	6.0 W	4.3 W
L2 Cache Speed	Off-chip cache is accessed over external bus that is generally up to ½ the speed of the processor.	Internal cache is accessed at same speed as processor.
ECC error detection		Uses ECC to correct and detect single bit errors. 8 bit ECC foe every 64 bit double word in memory.

In conclusion these enhancements and their combined effects on the performance show the strength of the PPC750CXe in comparison to the PPC750L.

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