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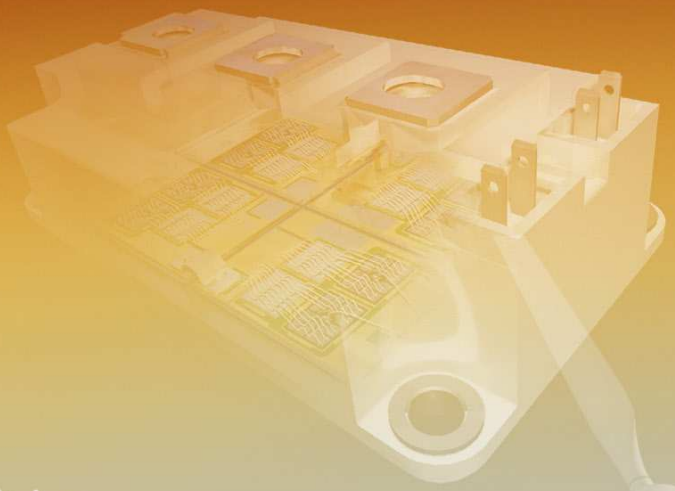
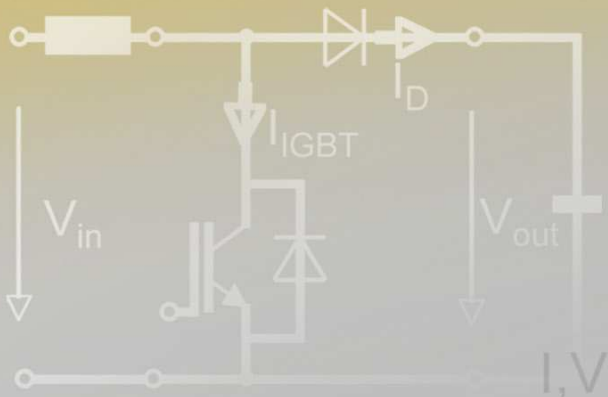
Application Manual Power Semiconductors





Application Manual
Power Semiconductors

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Preface

Since the first Application Manual for IGBT and MOSFET power modules was published, these components have found their way into a whole host of new applications, mainly driven by the growing need for the efficient use of fossil fuels, the reduction of environmental impact and the resultant increased use of regenerative sources of energy. General development trends (space requirements, costs, and energy efficiency) and the advancement into new fields of application (e.g. decentralised applications under harsh conditions) bring about new, stricter requirements which devices featuring state-of-the-art power semiconductors have to live up to. For this reason, this manual looks more closely than its predecessor at aspects pertaining to power semiconductor application and also deals with rectifier diodes and thyristors, which were last detailed in a SEMIKRON manual over 30 years ago.

This manual is aimed primarily at users and is intended to consolidate experience which up till now has been contained in numerous separate articles and papers. For reasons of clarity and where deemed necessary, theoretical background is gone into briefly in order to provide a better understanding of the subject matter. A deeper theoretical insight is provided in various highly-recommendable textbooks, some of which have been cited in the bibliography to this manual.

SEMIKRON's wealth of experience and expertise has gone into this advanced application manual which deals with power modules based on IGBT, MOSFET and adapted diodes, as well as rectifier diodes and thyristors in module or discrete component form from the point of view of the user. Taking the properties of these components as a basis, the manual provides tips on how to use and interpret data sheets, as well as application notes on areas such as cooling, power layout, driver technology, protection, parallel and series connection, and the use of transistor modules in soft switching applications.

This manual includes contributions from the 1998 "Application Manual for IGBT and MOSFET Power Modules" written by Prof. Dr.-Ing. Josef Lutz and Prof. Dr.-Ing. habil. Jürgen Petzoldt, whose authorship is not specifically cited in the text here. The same applies to excerpts taken from the SEMIKRON Power Semiconductor Manual by Dr.-Ing. Hans-Peter Hempel. We would like to thank everyone for granting their consent to use the relevant excerpts.

We would also like to take this opportunity to express our gratitude to Rainer Weiß and Dr. Uwe Scheuermann for their expertise and selfless help and support. Thanks also go to Dr.-Ing. Thomas Stockmeier, Peter Beckedahl and Thomas Grasshoff for proofing and editing the texts, and Elke Schöne and Gerlinde Stark for their editorial assistance.

We very much hope that the readers of this manual find it useful and informative. Your feedback and criticism is always welcome. If this manual facilitates component selection and design-in tasks on your part, our expectations will have been met.

Nuremberg, Dresden, Ilmenau; November 2010

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1 Power Semiconductors: Basic Operating Principles

1.1 Basics for the operation of power semiconductors

With the exception of a few special applications, power semiconductors are used predominantly in switching applications. This results in a number of basic principles and operating modes that apply to all power electronics circuitries. In the development and use of power semiconductors the most important goal is to achieve minimum power losses.

A switch used in an inductive circuit can turn on actively, i.e. at any given time. For an infinitely short switching time no power losses occur, since the bias voltage may drop directly over the line inductance. If the circuit is live, turn-off is not possible without conversion of energy, since the energy stored in L has to be converted. For this reason, switch turn-off without any energy conversion is only possible if $i_S = 0$. This is also called passive turn-off, since the switching moment is dependent on the current flow in the circuit. A switch that is running under these switching conditions is called a ZCS (**Z**ero **C**urrent **S**witch).

Only for $v_S = 0$ can turn-on of a switch under an impressed voltage applied directly at the switch terminals be ideal, i.e. non-dissipative. This is called passive turn-on, since the voltage waveform at the switch and, thus, the zero crossing of the switch voltage is determined by the outer circuit. Active turn-off, in contrast, is possible at any time. Switches that operate under these switching conditions are called ZVS (**Z**ero **V**oltage **S**witches).

Figure 1.1.1 shows current and voltage waveforms at the switches during the basic switching processes described above. The use of real power semiconductors as switches will result in the following conditions. Before active turn-on, the current-transferring semiconductor is under positive voltage. To enable the voltage to drop, the current - triggered by the controller - has to increase by a certain rate determined by the turn-on characteristics of the power semiconductor. Both the turn-on characteristic and the effective series inductance limit the current rise and voltage distribution within the circuit between power semiconductor and inductor. As the inductance increases, the turn-on power losses of the given power semiconductor are diminished to a minimum threshold value.

During passive turn-off of a live power semiconductor carrying current in positive direction, current drops to zero due to the voltage polarity of the outer circuit. Current is conducted back as reverse current by the charge carriers still stored in the semiconductor; this happens until the semiconductor has recovered its blocking capability to take up the negative circuit voltage (reverse recovery).

Active turn-off of a live power semiconductor will initially produce a voltage rise in positive direction triggered by the controller (turn-off characteristic). Then, an effective parallel capacitance at the switch terminals can take over the current flow given by the turn-off characteristic of the power semiconductor. For the given power semiconductor, the energy loss caused by the turn-off procedure drops as the capacitance increases (turn-off load reduction).

A passively switched power semiconductor is under negative voltage before turn-on. If this voltage changes polarity due to processes in the outer circuit, the power semiconductor will take up current in positive direction, which, in the case of a substantial increase in current, will lead to turn-on overvoltage (forward recovery).

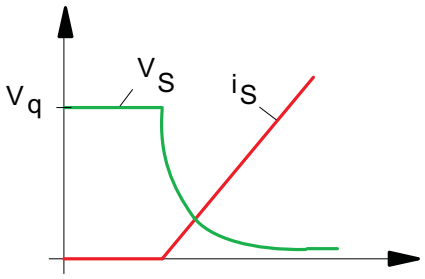
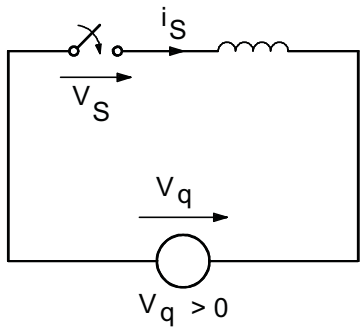
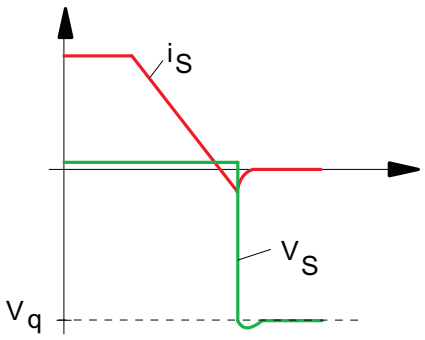
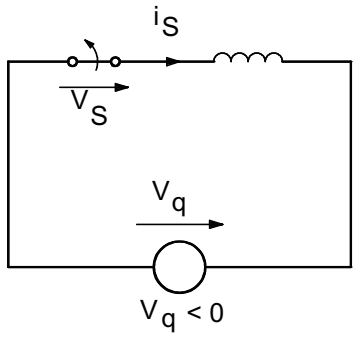
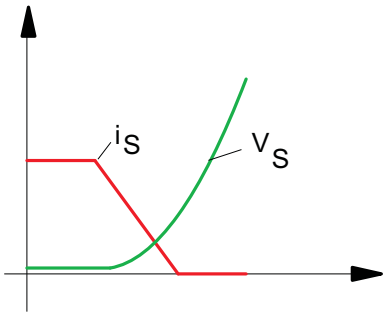
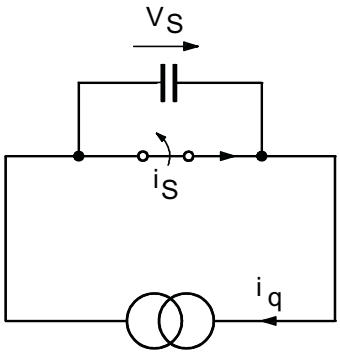
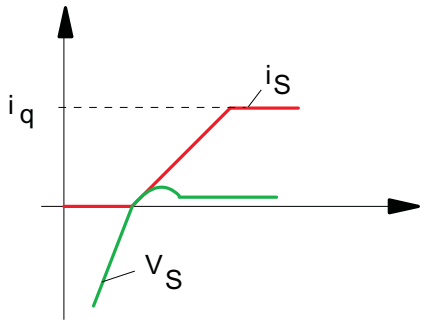
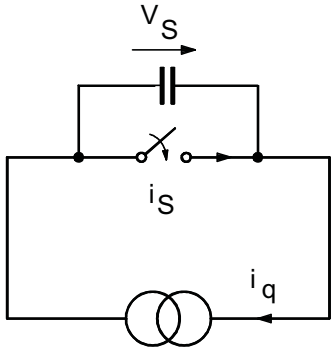
Switching Process	Waveform	Equivalent Circuit
active ON $\frac{di_S}{dt} > 0$; $\frac{dV_S}{dt} < 0$		
passive OFF $\frac{di_S}{dt} < 0$; $\frac{dV_S}{dt} < 0$		
active OFF $\frac{di_S}{dt} < 0$; $\frac{dV_S}{dt} > 0$		
passive ON $\frac{di_S}{dt} > 0$; $\frac{dV_S}{dt} > 0$		

Figure 1.1.1 Basic switching processes

The basic operating principle behind power semiconductors is clearly defined in the aforementioned active and passive switching processes during cyclic switching of individual switches (turn-on and turn-off of connecting lines between energy-transfer circuits) and inductive or capacitive commutation (alternating switching of two switches each, alternating current-carrying and voltage-carrying). Figure 1.1.2 shows a summary of the relationships between current and voltage during the different possible switching procedures.

Hard switching (HS, Figure 1.1.2 and Figure 1.2.3)

Hard turn-on is characterized by an almost total v_K commutation voltage drop across the current-carrying switch S_1 for the entire current commutation time, causing considerable power loss peaks within the power semiconductor. At this point, inductance L_K in the commutation circuit is at its minimum value, i.e. the semiconductor that is turned on determines the current increase. Current commutation is ended by passive turn-off of switch S_2. Commutation and total switching time are almost identical.

In case of hard turn-off, the voltage across S_1 increases up to a value exceeding commutation voltage v_K while current i_{S1} continues to flow. Only then does current commutation begin as a result of passive turn-on of S_2. The capacitance C_K in the commutation circuit is very low, meaning that the voltage increase is determined mainly by the properties of the power semiconductor. The total switching and commutation time are therefore virtually identical, and very high power loss peaks occur in the switch.

Soft switching (ZCS, ZVS, Figure 1.1.2, Figure 1.2.4 and Figure 1.2.5)

In the case of soft turn-on of a zero-current switch (ZCS; S_1 actively on), the switch voltage will drop to the forward voltage drop value relatively quickly, provided L_K has been dimensioned sufficiently, meaning that there are no or only very low dynamic power losses in the switches during current commutation. Current increase is determined by the commutation inductance L_K. Current commutation ends when switch S_2 is passively turned off. This means that the commutation time t_K is higher than the switching times of the individual switches.

Active turn-off of S_1 will initialize soft turn-off of a zero-voltage switch. The decreasing switch current commutates to the capacitors C_K, which are positioned parallel to the switch, and initialises the voltage commutation process. The size of C_K determines the voltage increase in conjunction with the commutation current. Dynamic power losses are reduced by the delayed voltage increase at the switch.

Resonant switching (ZCRS, ZVRS, Figure 1.1.2, Figure 1.2.6 and Figure 1.2.7)

Resonant switching refers to the situation where a zero-current switch is turned on at the moment when current i_L drops virtually to zero. The switching losses are thus even lower than in the case of soft switching of a zero-current switch. Since the switch cannot actively determine the time of zero-current crossing, overall system controllability is somewhat restricted.

Resonant turn-off of a zero-voltage switch, in contrast, occurs when the commutation voltage drops virtually to zero during the turn-off process. Once again, switching losses are lower than for soft turn-off of the zero-voltage switch; here, too, there is less controllability.

Neutral switching (NS, Figure 1.1.2 and Figure 1.2.8)

Neutral switching refers to the situation where both switch voltage and switch current are zero at the moment of switching. This is commonly the case when diodes are used.

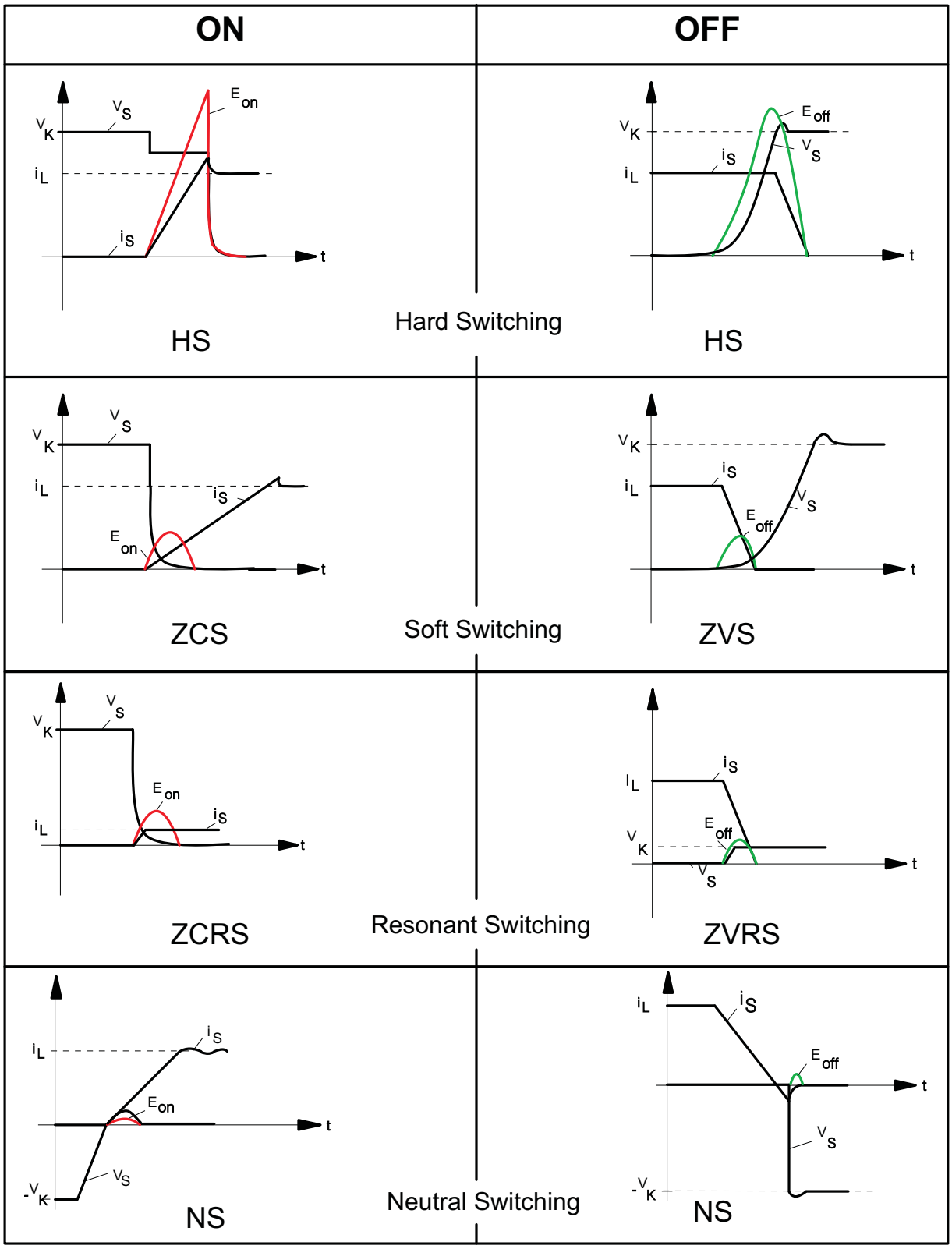


Figure 1.1.2 Types of switching processes (v_K = driving commutation voltage, i_L = load current to be commutated)

1.2 Power electronic switches

A power electronic switch integrates a combination of power electronic components and a driver circuit for the actively switchable power semiconductors. The internal functional correlations and interactions within this integrated system determine several characteristics of the switch.

Figure 1.2.1 shows a power electronic switch system including interfaces to external electric circuitry (normally high voltage) and the control unit (information processing, auxiliary power supply). Optical or inductive transmitters are normally used to ensure the necessary potential separation. The combination possibilities for power semiconductors with different switch current direction and voltage direction are shown in Figure 1.2.2.

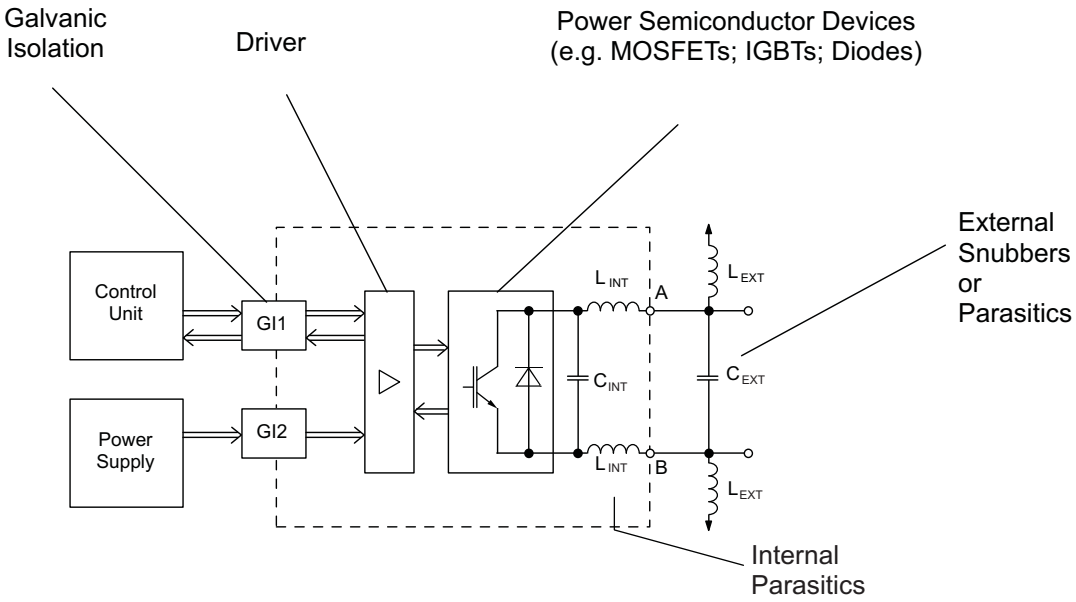


Figure 1.2.1 Power electronic switch system

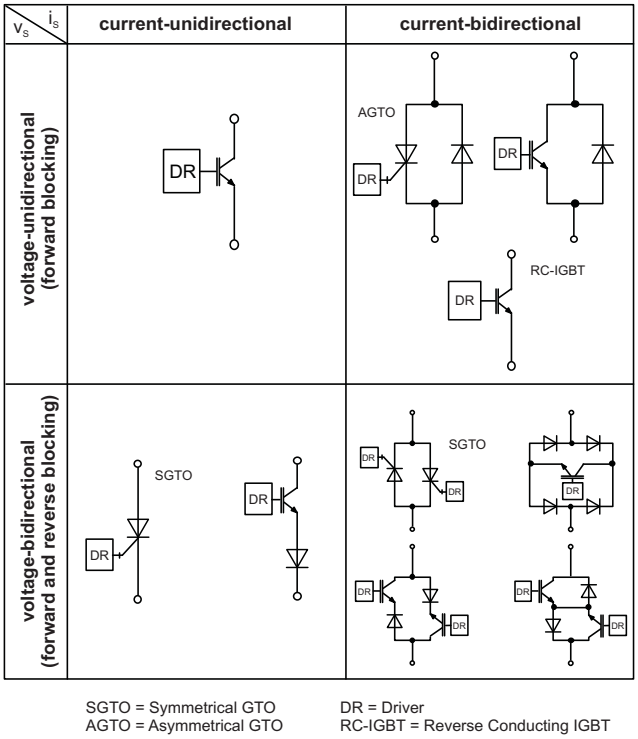


Figure 1.2.2 Possible combinations of power semiconductors in power electronic switches

On the one hand, the parameters of a complete switch result from the semiconductor switching behaviour, which has to be adapted to the operating mode of the entire switch by way of semiconductor chip design. On the other hand, the driver circuit is responsible for the main switch parameters and performs the key protection and diagnosis functions.

Basic types of power electronic switches

Owing to the operational principles of power semiconductors, which are clearly responsible for the dominant characteristics of the circuits in which they operate, power electronic switches may be split up into the following basic types. The main voltage and current directions clearly result from the requirements in the actual circuit, in particular from the injected currents and voltages in the commutation circuits.

Hard switch (HS)

Except for the theoretical case of pure ohmic load, a single switch with hard turn-on and turn-off switching behaviour can be used solely in a commutation circuit with minimum passive energy storage components ($C_{K,min}$; $L_{K,min}$) in combination with a neutral-switching power semiconductor. Compared to the neutral switch which has no control possibility, a hard switch may be equipped with two control possibilities, namely individually adjustable turn-on and turn-off points. This results in the possibility of operating the entire circuit using pulse width modulation (PWM). These topologies dominate in power converter circuits in industrial applications.

Figure 1.2.3 shows the possible circuit configurations (in IGBT technology) and commutation circuits. Examples of typical circuits are the three-phase voltage source inverter (VSI) or the current source inverter (CSI). In symmetrical switch arrangements, only one alternating current-carrying switch will operate actively with two control possibilities, while the other one switches neutrally.

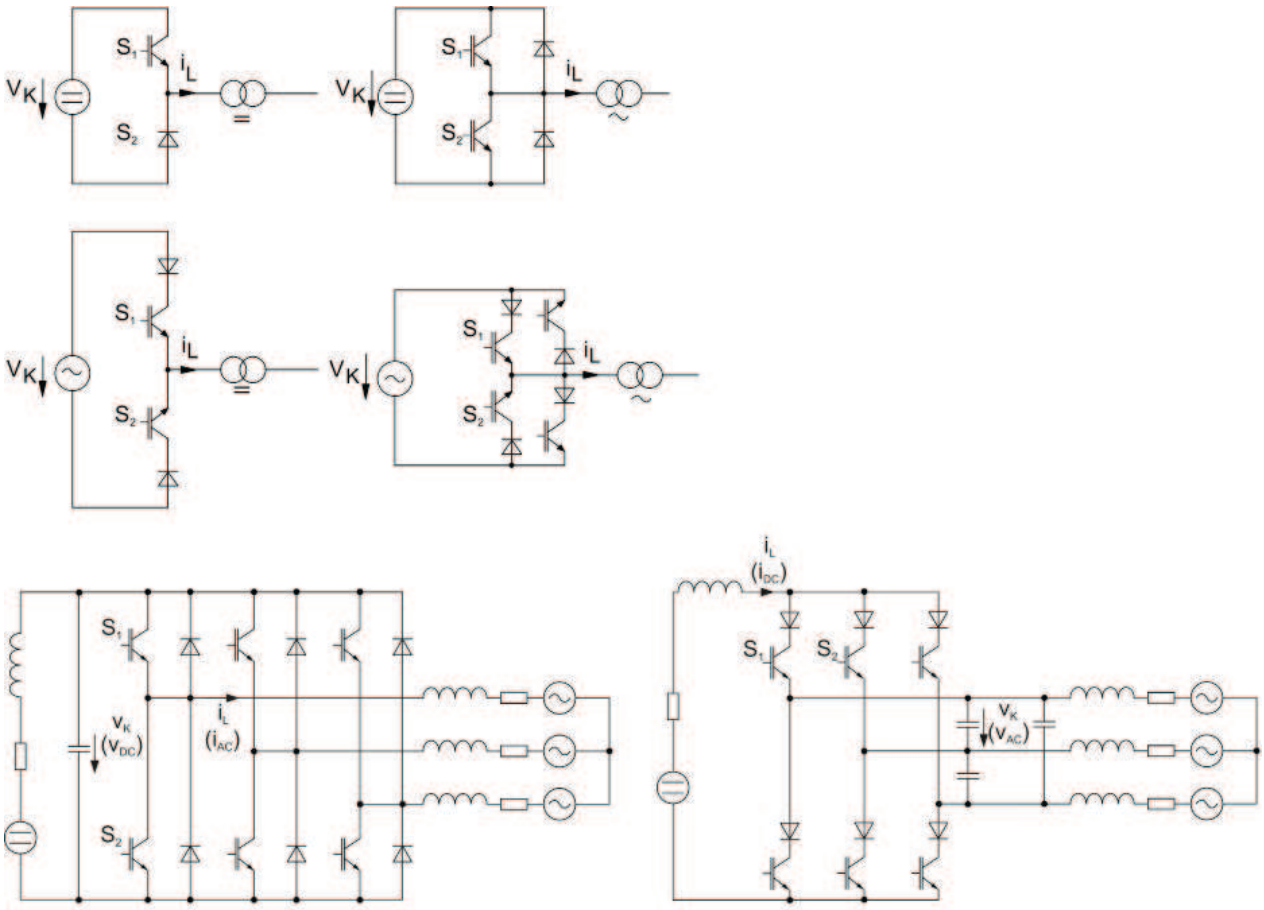
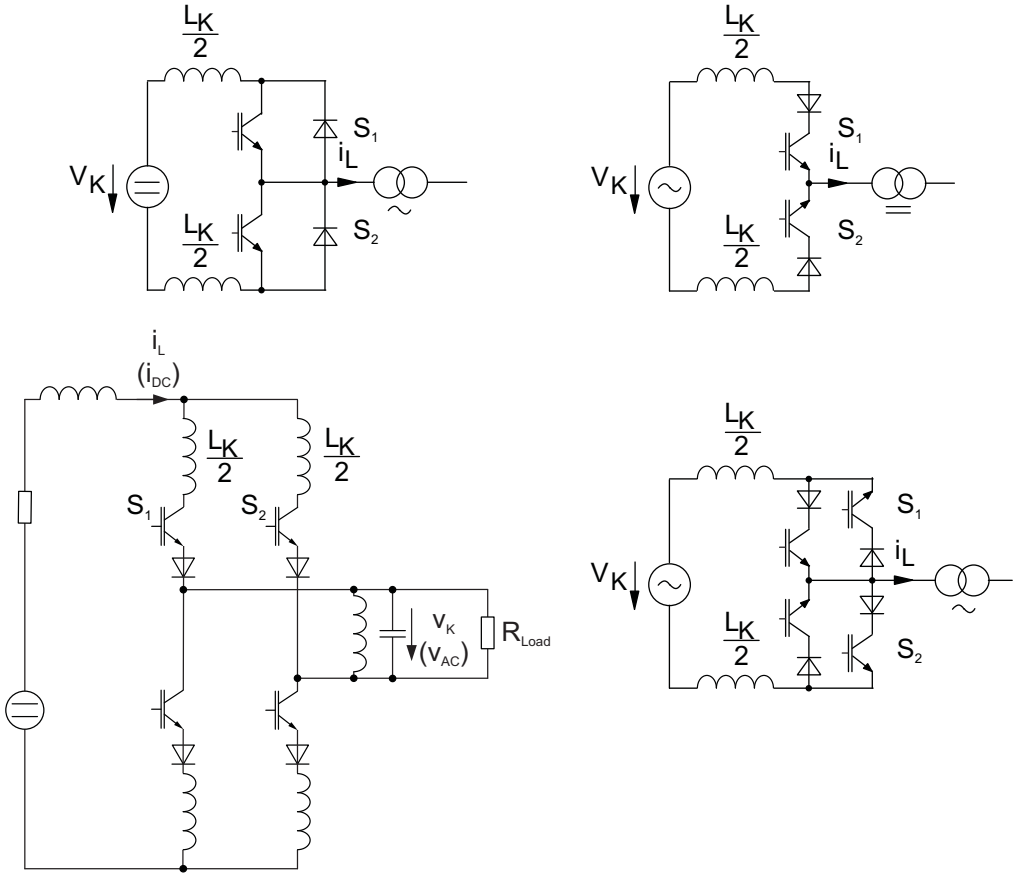


Figure 1.2.3 HS commutation circuits and examples of typical circuits

Zero current switch (ZCS)

In zero-current switches, the power semiconductors are always turned on actively and turned off passively (for i_S=0). Accepting the loss of one control possibility compared to a HS, active switching may be performed with far lower power losses thanks to sufficient series inductance L_K. This makes it possible to achieve higher switching frequencies than for hard switching.

The single remaining switch control possibility calls for the use of the control process "pulse shift modulation" (PSM). In concrete circuits applications with zero-current switches, this control process is also known as "phase-angle control". Figure 1.2.4 shows the possible switch configurations of a ZCS in IGBT technology operating in an equivalent commutation circuit; these switch configurations can also be used in circuits with cyclic switching and no commutation. An example of a typical circuit is a impressed-current parallel resonant converter. The resistance R_{Load} symbolises load connection in series with the resonant circuit. A further group of circuit topologies that work exclusively on the basis of zero-current switches are line-commutated thyristor rectifier circuits.



Parallel Resonant Converter

Figure 1.2.4 ZCS commutation circuits and example of a typical circuit

Zero Voltage Switch (ZVS)

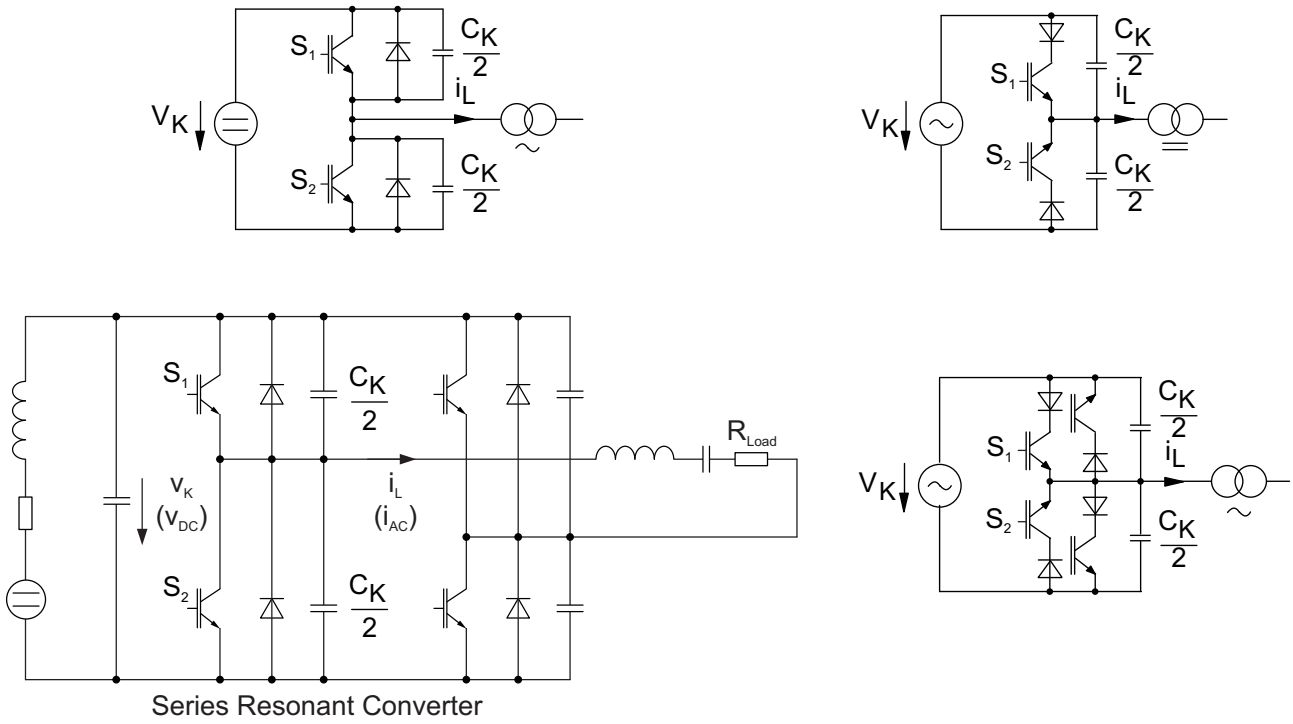


Figure 1.2.5 ZVS commutation circuits and example of a typical circuit

Zero-voltage switches are designed such that they may be turned off actively and turned on passively when the switch voltage drops to zero (v_S=0). Active turn-off will produce very low losses if a sufficiently high parallel capacitance is selected. Compared to hard switching, a decrease in power losses is obtained by dispensing with one control possibility. The lower switching losses, however, allow for higher switching frequencies than is the case in hard switching.

The single remaining switch control possibility calls for the use of the control process "pulse shift modulation" (PSM). In concrete circuits applications with zero-voltage switches, this control process is also known as "phase-angle control". Figure 1.2.5 shows the possible switch configurations of a ZVS in IGBT technology operating in an equivalent commutation circuit; these switch configurations can also be used in circuits with cyclic switching and no commutation. An example of a typical circuit is a voltage-impressed parallel resonant converter. The resistance R_{Load} symbolises load connection in series with the resonant circuit.

Zero Current Resonant Switch (ZCRS)

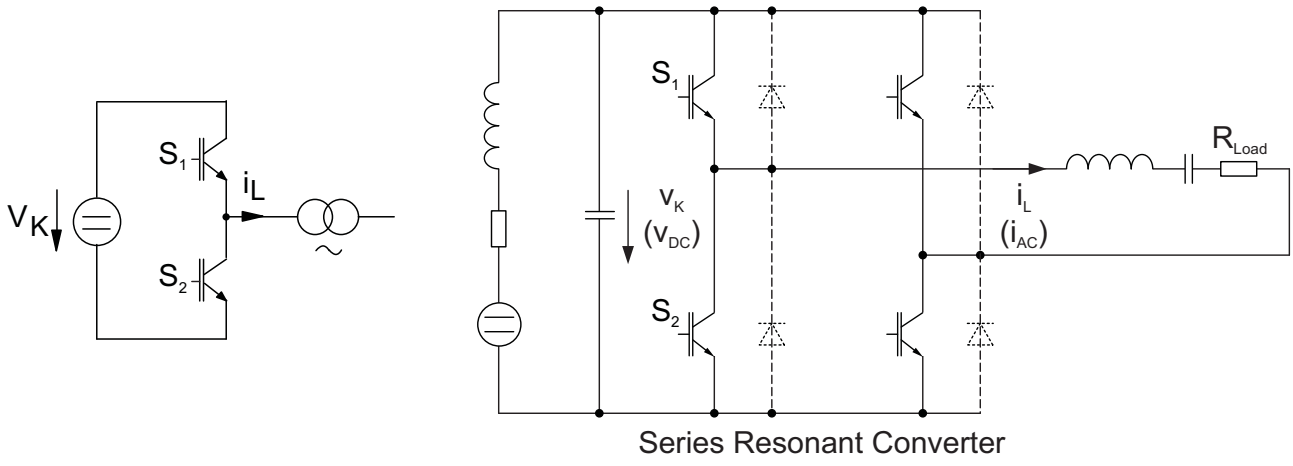


Figure 1.2.6 ZCRS commutation circuit and example of a typical circuit

A zero-current resonant switch is controlled such that active turn-on begins at the very moment at which the current i_L displays zero crossing. Thus, actual current commutation does not take place. Consequently, even if there is a minimum commutation inductance L_K, the turn-on losses are lower than in zero-current switches and are caused by the necessary change in charge of the junction capacitances of the given power semiconductors. At the same time, the further power loss reduction compared to ZCS means another loss of controllability, since the turn-on moment is not controllable, but is triggered by the zero-current crossing given by the outer circuitry. In circuits with ZCRS, only indirect control of the energy flow is possible and is done by conducting and blocking the switches across several periods of alternating current. This is referred to as pulse density modulation (PDM) or even pulse group modulation.

Figure 1.2.6 shows a commutation circuit with ZCRS, as well as a sample circuit in IGBT technology. For ideal switching at zero crossing of alternating current, the switches would not need antiparallel switch diodes for the second current direction. In practice, however, these are included owing to non-ideal behaviour. The resistance R_{Load} symbolises load connection in series with the resonant circuit.

Zero Voltage Resonant Switch (ZVRS)

This basic type of switch is to be considered a borderline case of the ZVS. If a ZVS actively turns off exactly at the point of zero-crossing of the applied alternating commutation voltage V_K, the increasing switch voltage will trigger the current commutation process (between the switches). Even for a very low capacitance C_K in the commutation circuit, the switching losses are lower than for the ZVS, in combination with the loss of a further control possibility, because the turn-off moments are no longer independently adjustable but are triggered by the zero voltage crossing given by the outer circuitry. Similar to the case for ZCRS, in circuits with ZVRS, only indirect control of the energy flow is possible and is done by conducting and blocking the switches across several periods of alternating current. This is referred to as pulse density modulation (PDM) or even pulse group modulation.

Figure 1.2.7 shows a commutation circuit with ZVRS, as well as a sample circuit in IGBT technology. For ideal switching at zero crossing of the alternating voltage, the switches would not need antiparallel switch diodes for the second current direction. In practice, however, these are included owing to non-ideal behaviour. The resistance R_{Load} symbolises load connection parallel to the resonant circuit.

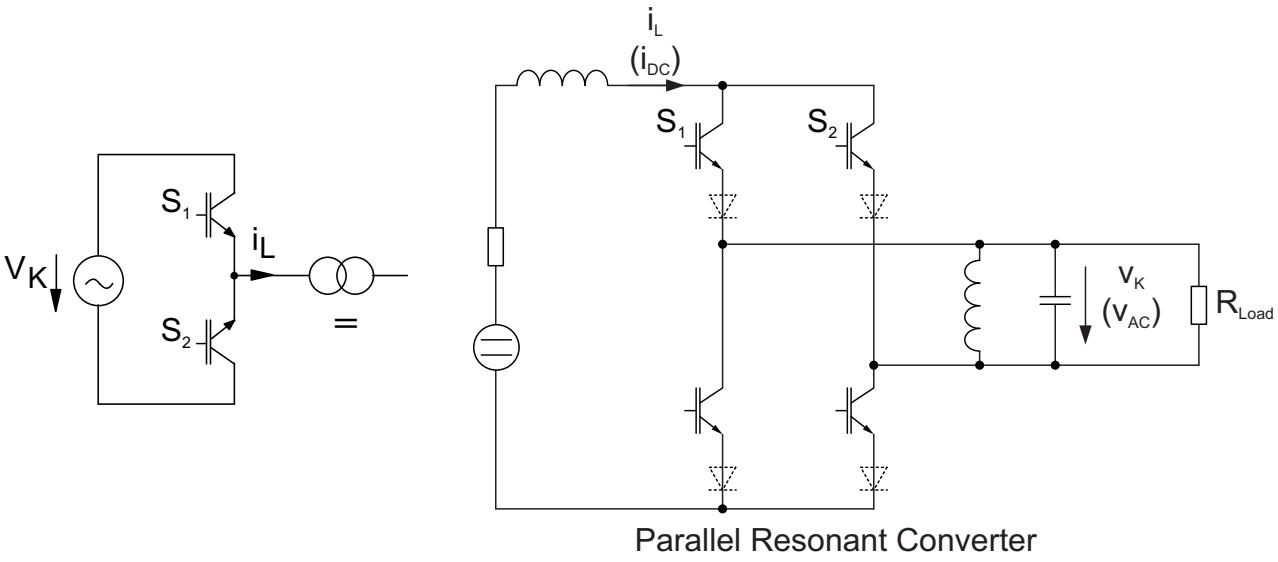


Figure 1.2.7 ZVRS commutation circuit and example of a typical circuit

Neutral Switch (NS)

A commutation process is started or ended by neutral turn-on or turn-off of a neutral switch. Here, both voltage and current across the switch are zero at the moment of switching. Owing to its natural switching behaviour, a diode displays these properties. Neutral switches can also be implemented by integrating actively switching power semiconductors (e.g. IGBT) provided this is given "diode properties" by way of suitable intelligent control.

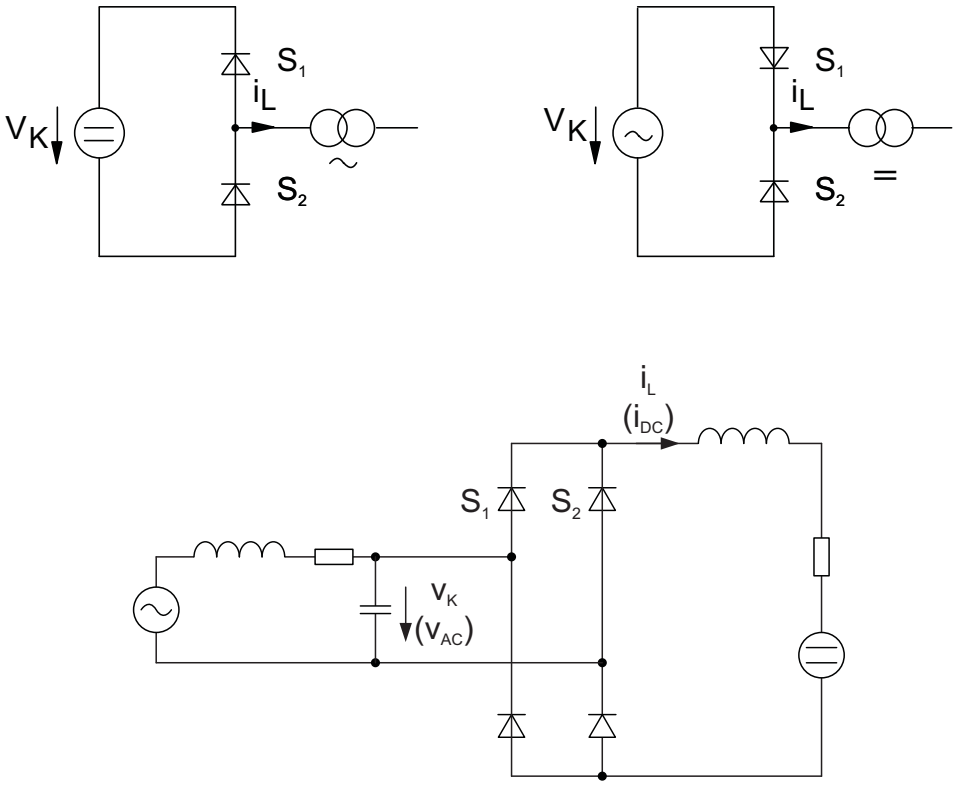


Figure 1.2.8 NS commutation circuits and example of a typical circuit

Figure 1.2.8 shows commutation circuits with neutral switches, as well as a diode rectifier topology as an example of a typical circuit for neutral switches. Table 1.2.1 shows a summary of all basic types of power electronic switches incl. the aforementioned turn-on and turn-off processes. The blank fields are modifications of the basic types which are required in almost all applications. If the resonant conditions in a circuit working with soft or resonant switches are not met at certain operating points, the switches have to be able to cope with hard switching - something that is not normally within their original features (modified ZVS = MZVS; modified ZCS = MZCS) - in order to ensure that the entire system continues to work. Normally, the switches are operated in this deviating mode for a very short time only. In the case of hard active turn-off of a ZVS or hard active turn-on of a ZCS, the switches are operated as ZVHS or ZCHS, respectively.

OFF \ ON	**hard**	**soft L_K in series**	**resonant $i_L = 0$**	**neutral $V_s = 0$**
hard	HS	MZCS		ZVHS
soft C_K in parallel	MZVS			ZVS
resonant $V_K = 0$				ZVRS
neutral $i_S = 0$	ZCHS	ZCS	ZCRS	NS

Table 1.2.1 Basic types of power electronic switches

2 Basics

2.1 Application fields and current performance limits for power semiconductors

The development of power semiconductors saw the onset of lasting success for power electronics across all fields of electrical engineering. Given the ever increasing call for resource conservation (e.g. energy saving agenda), the use of renewable energies (e.g.wind power and photovoltaics) and the need for alternatives to fossil fuels (e.g. electric and hybrid drives for vehicles), this success is gaining more and more momentum today.

This development is also largely driven by the interactions between system costs and market penetration, as well as the energy consumption required for production and the energy saving potential of products in operation. In addition to the general aim to expand the performance profile, the development aims "low materials consumption/ low costs" and "high efficiency" are gaining more and more importance.

Figure 2.1.1 shows maximum current and voltage values for controllable power semiconductors on the market today. Today, the use of parallel and series connections for power semiconductors, as well as power converters equipped with semiconductors, means that virtually any amount of electric power can be transformed, converted into another form of energy or "generated" from another type of energy.

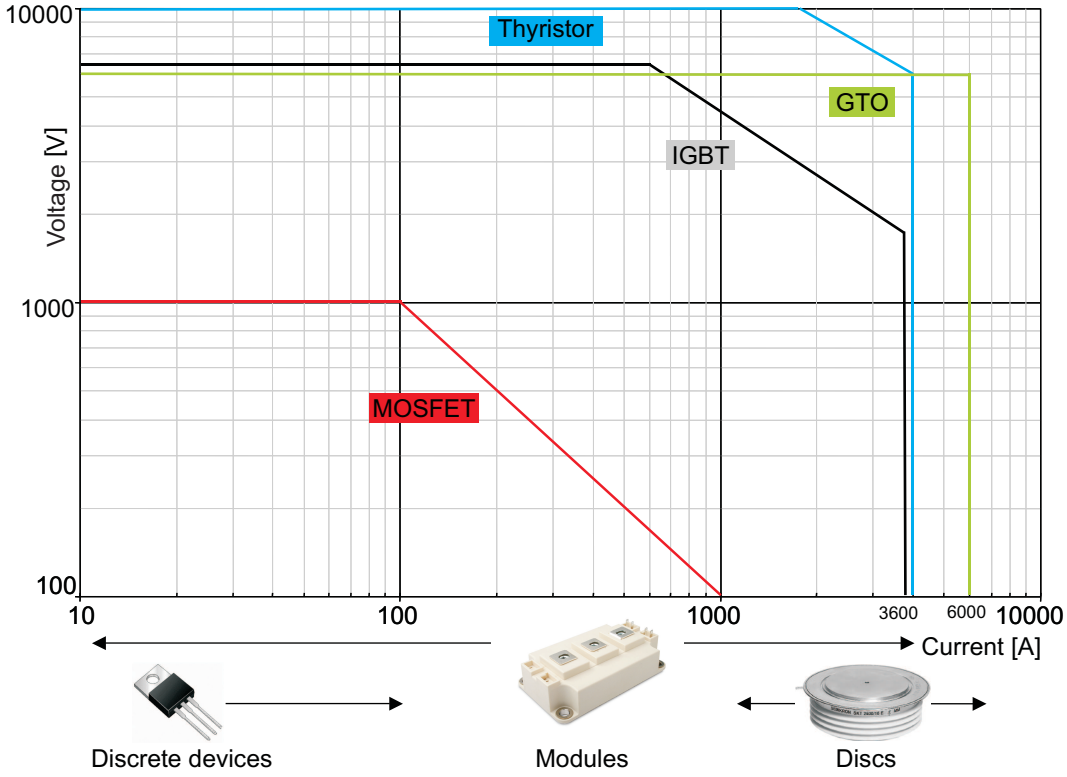


Figure 2.1.1 Present current and voltage limits for controllable power semiconductors

Figure 2.1.2a) shows common switching frequency ranges for various power semiconductors. Figure 2.1.2b) illustrates the current key application fields and limits.

IGBT (**I**nsulated **G**ate **B**ipolar **T**ransistors) have become especially important for the "mass markets" of mains-powered systems and equipment with a medium or high switching performance in the range of some kW and several MW, this is particularly true for potential-free power modules.

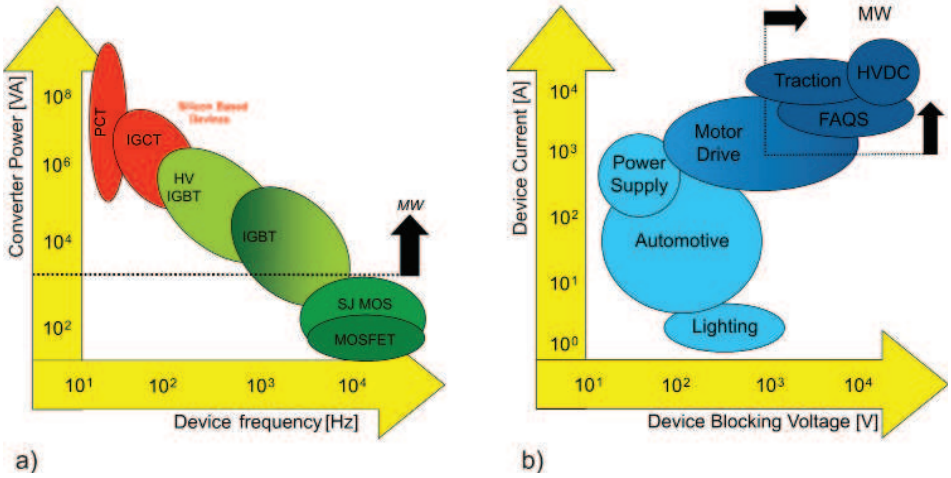


Figure 2.1.2 a) Switching frequency ranges for various power semiconductors;
b) Current application areas and limits [1]

Since the mid-eighties, these are other actively switchable power semiconductors such as power MOSFET (**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor), GTO (**G**ate **T**urn **O**ff-) thyristors and IGCT (**I**ntegrated **G**ate **C**ommutated **T**hyristor) have almost completely pushed back conventional thyristors to line-commutated applications. Compared to other switchable power semiconductors, such as conventional GTO-thyristors, **IGBT** and **MOSFET** have a number of application advantages, such as active turn-off even in the event of a short circuit, operation without snubbers, simple control, short switching times and, consequently, relatively low switching losses. The production of MOSFET and IGBT using technologies from the field of microelectronics is comparatively simple and low-priced.

Today, most applications for currents of some 10 A use power semiconductors with silicon chips integrated in **potential-free power modules**. In 1975, it was SEMIKRON who launched them commercially for the first time. These modules often contain several silicon chips of identical or different components (e.g. IGBT and freewheeling diode, or thyristor and line rectifier diode), and more components (e.g. temperature and current sensors) or control and protective circuits ("intelligent power modules"/IPM), if required.

Despite the disadvantage of one-side cooling only, for up to high power ranges, potential-free power modules are gaining more ground than disk cells, even though the latter are able to dissipate about 30% more of the heat losses thanks to double-sided cooling and are better suited to series connections from a mechanical point of view. The reason that modules are more popular than disk cells is that, apart from easy assembly, they boast "integrated", well-proven electrical isolation between chip and heat sink, almost any combination of different components in one module and relatively low costs thanks to batch production.

Today, important areas of application for **power MOSFET** are power supply systems, low-voltage switch applications in automotive electronics and applications featuring very high switching frequencies (50…500 kHz), where standardised power modules are of rather low importance.

The following chapters will detail the layout, function, characteristics and applications of line rectifier diodes and thyristors, power MOSFET and IGBT, and fast diodes required as freewheeling diodes, and outline development trends in these areas. Based on the requirements described at the beginning of this chapter, the general aims and directions for the further development of power semiconductors can be summarised as follows:

The key **aims for further development** are as follows:
- Increasing the switching performance (current, voltage)
- Reducing losses in the semiconductors as well as in control and protective circuits
- Expanding the operating temperature range
- Improved service life, ruggedness and reliability
- Reducing the amount of control and protection required; improving component behaviour in the event of error / failure
- Cost reduction

The **development directions** can be broken down as follows:

Semiconductor materials
- New semiconductor materials (e.g. wide bandgap materials)

Chip technology
- Higher permissible chip temperatures or current densities (reduction of chip area)
- Finer structures (reduction of chip area)
- New structures (improvement of chip characteristics)
- Integration of functions on the chip (e.g. gate resistance, temperature measurement, monolithic system integration)
- New monolithic components by combining functions (RC-IGBT, ESBT)
- Improved stability of chip characteristics under different climatic conditions

Packaging
- Increase in thermal and power cycling capability
- Improvement of heat dissipation (isolation substrate, base plate, heat sink)
- Wider scope of application as regards climate conditions thanks to improvements in casing and potting materials or new packaging concepts
- Optimisation of internal connections and connection layouts regarding parasitic elements
- User-friendly package optimisation to simplify device construction
- Reduction of packaging costs and improvement of environmental compatibility in production, operation and recycling

Degree of integration
- Increasing the complexity of power modules to reduce system costs
- Integration of driver, monitoring and protective functions
- System integration

Figure 2.1.3 shows different power module integration levels

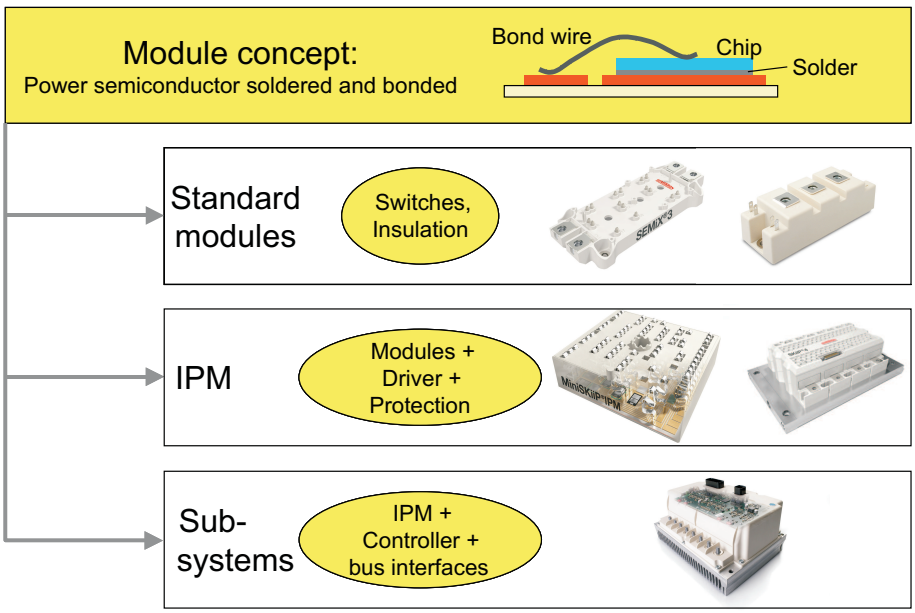


Figure 2.1.3 Power module integration levels

More complex technologies, smaller semiconductor structures and precise process control are inevitably driving the properties of modern power semiconductors towards the physical limits of silicon. For this reason, research into alternative semiconductor materials, which began as early as the 1950s, was pushed in recent years and has since resulted in the first mass products.

Today, the "**wide bandgap materials**" silicon carbide (SiC) and gallium nitride (GaN) are the main focus of this research. Compared to silicon, they display a far higher energetic gap between valence and conduction band, resulting in comparatively lower forward on-state losses and switching losses, higher permissible chip temperatures, and better heat conductivity than silicon.

Table 2.1.1 contains quantitative data on the key material parameters [2], Figure 2.1.4 shows the impact they have on material properties.

Parameters			**Si**	**4H-SiC**	**GaN**
Bandgap energy	E_g	eV	1.12	3.26	3.39
Intrinsic density	n_i	cm^{-3}	$1.4*10^{-10}$	$8.2*10^{-9}$	$1.9*10^{-10}$
Breakdown field intensity	E_c	MV/cm	0.23	2.2	3.3
Electron mobility	μ_n	cm^2/Vs	1,400	950	1,500
Drift velocity	ν_{sat}	cm/s	10^7	$2.7*10^7$	$2.5*10^7$
Dielectric constant	ε_r	-	11.8	9.7	9.0
Heat conductivity	λ	W/cmK	1.5	3.8	1.3

Table 2.1.1 Wide band-gap semiconductor materials versus silicon: a comparison of material properties

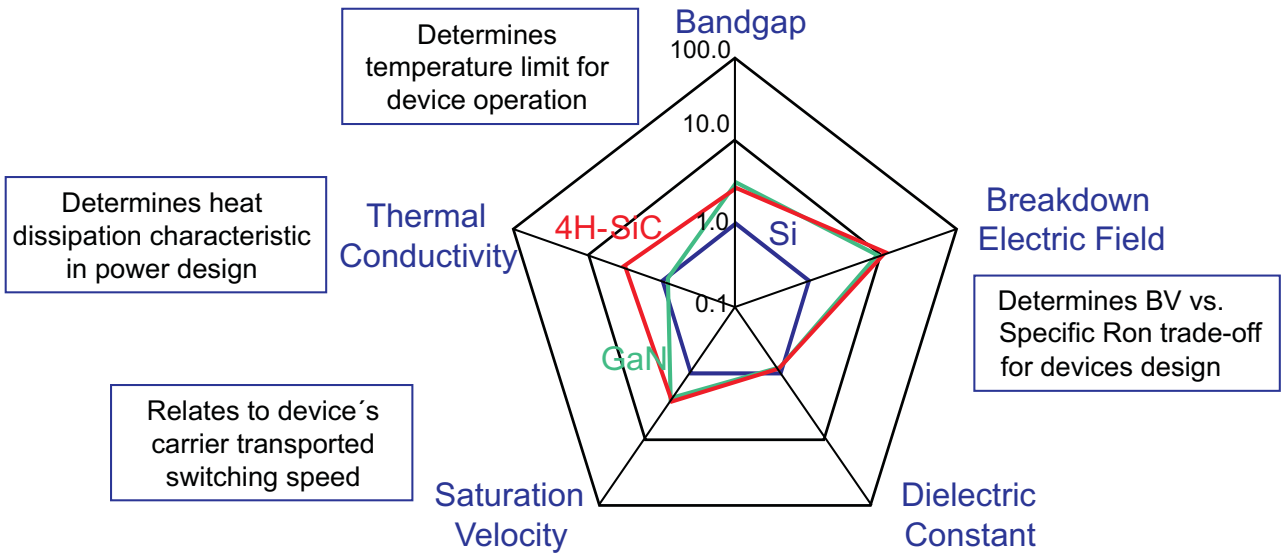


Figure 2.1.4 Impact of different physical parameters of semiconductor materials [3]

Today, the key to more widespread use of SiC, however, is to enable the cost-efficient production of suitable monocrystalline chips that are sufficiently high in quality to eliminate crystal degradation (micropipes), and that are available in optimum wafer sizes for the power electronics industry. While Si is currently produced on 8“ wafers virtually defect-free for € 0.10/cm², the defect density for SiC wafers with a diameter of 4“ is one order of magnitude higher, multiplying costs in comparison to Si. GaN, which displays slightly poorer properties than SiC, has been used mainly in optoelectronic components so far. The carrier material employed today is sapphire. Since this material

is non-conductive, GaN components must have planar structures. The most common type of diode on the market today is the SiC Schottky diode.

Owing to the advanced development stage of Si power semiconductors, there is no technical need to introduce other semiconductor materials for MOSFET and IGBT in the voltage range < 1000 V. In this voltage range, wide bandgap semiconductor materials are more likely to be competitive in junction-gate driven power semiconductors such as JFET (junction gate field-effect transistors), bipolar transistors and thyristors, whereas MOS-driven transistors clearly outplay silicon components when higher voltages are applied.

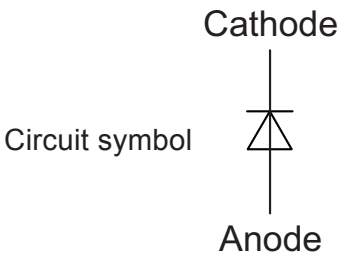
Owing to high material costs, power semiconductors made of "wide bandgap materials" are used first and foremost in applications where a particularly high efficiency ratio or minimum absolute losses are required, as well as in applications whose requirements – e.g. temperature, voltage or frequency – cannot be met with Si power semiconductors.

In order to to fully benefit from the main advantages that power semiconductors made of SiC or GaN have over conventional components, such as
- low conduction and switching losses
- higher blocking voltages
- higher possible power densities
- higher permissible operating temperatures
- shorter switching times, higher switching frequencies,

it is vital for packaging to be further developed and improved on accordingly.

2.2 Line rectifiers

2.2.1 Rectifier diodes



2.2.1.1 General terms

Forward direction

Direction of current flow where the rectifier diode has the lower resistance.

Reverse direction

Direction of current flow where the rectifier diode has the higher resistance.

Anode terminal

Terminal into which the forward current (on-state current) flows.

Cathode terminal

Terminal out of which the forward current (on-state current) flows.

On-state current (forward current)

Current flowing in forward direction.

On-state voltage (forward voltage)

Voltage applied between the terminals as a result of the forward current.

Reverse current

Current flowing in reverse direction as a result of blocking voltage (reverse voltage). If the off-state current is displayed using a plotter, an oscilloscope or a similar measuring instrument with a screen, DC voltage should be used for measurements if possible. If measurements are taken using AC voltage, it is important to note that the capacitance of the pn-junction causes a split in the characteristic curve. Depending on the rising or falling voltage, there will be a positive or negative displacement current which splits the characteristic into two branches. The point in the peak of the measurement voltage is not distorted by capacitive influences and shows the true reverse current (Figure 2.2.1).

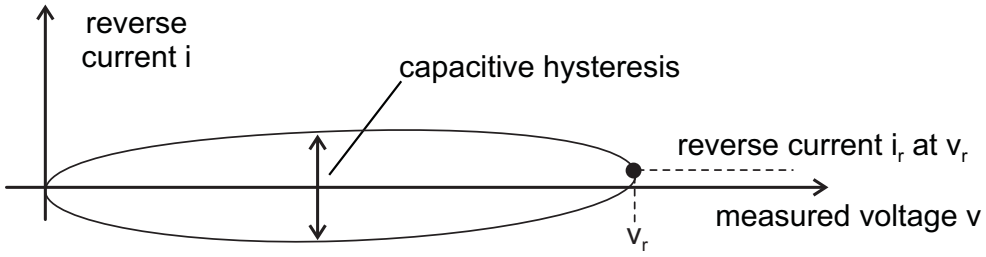


Figure 2.2.1 Blocking characteristic with capacitive splitting as a result of AC measurements.

Blocking voltage (reverse voltage)

Voltage applied between the terminals in reverse direction

2.2.1.2 Structure and functional principle

Rectifier diodes are components with two terminals and are used to rectify alternating currents. They have an asymmetrical current-voltage characteristic (Figure 2.2.2).

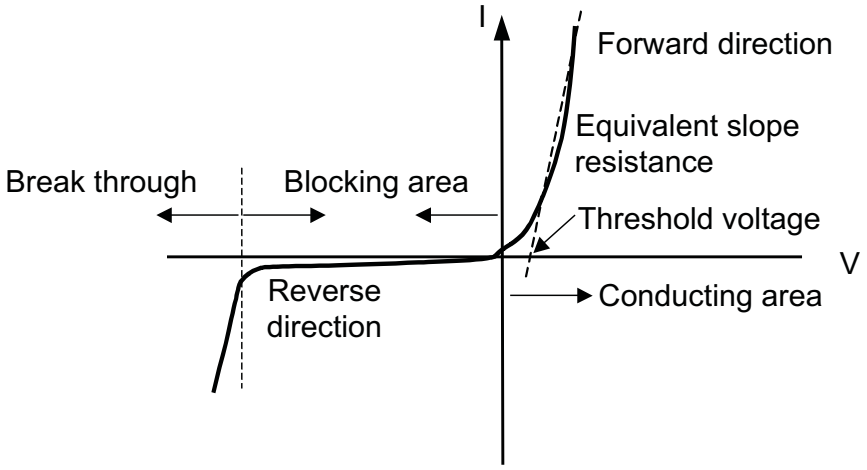


Figure 2.2.2 Current-voltage characteristic of a rectifier diode with voltage directions, current/voltage areas and equivalent resistance line

Today, the semiconductor diodes used to rectify line voltages are produced mainly on the basis of monocrystalline silicon. A distinction is made between diodes whose rectifying effect is caused by the transition of mobile charge carriers from an n-doped to a p-doped area in the semiconductor (**pn-diodes**) and **Schottky diodes**, where a metal-semiconductor junction produces the rectifying effect.

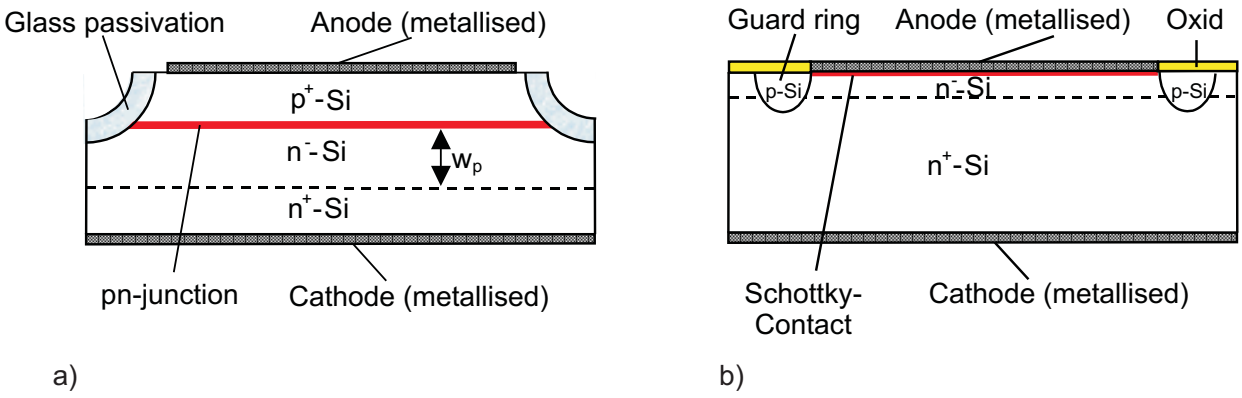


Figure 2.2.3 Schematic layout of a pn-diode (a) and a Schottky diode (b);
The glassivation and the guard ring with oxide cover provide protection from environmental impacts and stabilize reverse currents.

pn-diodes (pin-diodes)

A pn-diode consists of a heavily p-doped p^+-layer with many free-moving holes, a heavily n-doped n^+-layer with many free-moving electrons and a weakly n-doped n^--layer (also called i-layer, i meaning intrinsic) in between, whose width w_p and doping determine the maximum blocking voltage. The electrons and holes present in the vicinity of the pn-junction recombine with each other, which is why they are no longer available for current transmission. Thus, an insulating thin layer with no free-moving charge carriers is created. This is called the space charge region, since a potential difference between p-doped and n-doped silicon is built up here as a result of the non-mobile charges of ionised doping atoms. This happens without external voltage being applied.

If a negative voltage is applied to the p-silicon and a positive voltage to the n-silicon, free electrons in the n-silicon are sucked toward the cathode, and the holes in the p-silicon toward the anode. Owing to this effect, the insulating space charge region is widened and the electric field intensity in the vicinity of the pn-junction increases. The diode is poled in reverse direction and there is (almost) no current flow. Even if a diode is poled in reverse direction, a small current will flow. This is called the leakage current. This current results from the fact that free charge carrier pairs are generated in the space charge region as a result of thermal energy or irradiation. These charge carrier pairs are separated in the field of the space charge region and drained toward the terminals.

If a positive voltage is applied to the p-silicon and a negative voltage to the n-silicon, the free electrons in the n-silicon and the holes in the p-silicon are pushed into the space charge region. The space charge region is flooded by mobile charge carriers and disappears. A current flows and more charge carriers are supplied from the outer circuit. The diode is poled in forward direction (Figure 2.2.2).

Schottky diodes

In Schottky diodes, the metal-semiconductor contact (Schottky contact) carries out the tasks of the pn-junction. The biggest difference between pn-diodes and Schottky diodes is that in pn-diodes both electrons and holes assist in current transmission (the pn-diode is a bipolar component), whereas only one type of charge carrier is responsible for current transmission in Schottky diodes (unipolar component). This has a particularly strong affect on the dynamic behaviour (also see chapter 2.2.1.4 and 2.3.1.1).

2.2.1.3 Static behaviour

On-state behaviour

When forward voltage is applied, the current will increase steeply as soon as the **threshold voltage** for silicon this is approx. 0.7 V) has been reached (Figure 2.2.2). Only at very high currents which are far above the permissible continuous current will this on-state curve level out slightly. For low and medium currents, the temperature coefficient of the on-state voltage is negative, which means that, at constant current, the higher the temperature, the lower the on-state voltage. With very high currents this behaviour is reversed. When the on-state current flows, on-state losses are created (= on-state current * on-state voltage), heating up the diode. This heat build-up limits the forward current, since excessive heat may damage the diode.

Blocking behaviour

If voltage is applied to a diode in reverse direction, the reverse current will initially rise until it reaches a level - at just a few volts - which will barely increase further as the voltage is increased. The reverse current is highly temperature-dependent and rises proportionate to temperature, an effect that is particularly strong in the case of Schottky diodes. Under normal operating conditions, however, the losses that occur (= blocking voltage * reverse current) are so small that they can be neglected when calculating the overall losses (exception: Schottky diodes). If the voltage applied in reverse direction is increased until it reaches the breakdown region (Figure 2.2.2), the reverse current will rise more or less steeply. Two mechanisms may cause this rise: the Zener effect and the avalanche effect.

Zener effect

In diodes with a very highly doped n^- middle region, the field intensity in the space charge region may become so high that electrons are snatched away from the silicon atom bonds, thus creating free charge carrier pairs (Zener effect). This causes the reverse current to rise very steeply. The Zener voltage which is present when this rise occurs drops as the temperature increases. The Zener effect appears only in combination with extremely high field intensities in the space charge region. Such field intensities are only observed in diodes with a relatively low breakdown voltage. The limit is 5.7 V. In the case of higher breakdown voltages, this effect is known as the avalanche effect.

Avalanche effect

Within the space charge region, free charge carriers (electrons or holes) are generated as a result of thermal or optical energy. In the avalanche effect, these charge carriers are accelerated by the electric field intensity prevailing in the space charge region to such an extent that, due to their kinetic energy, they may create more charge carrier pairs by bumping into valence electrons (ionisation by collision). The number of free charge carriers increases like an avalanche, which is also true for the reverse current. The avalanche voltage which is present when this effect appears has a positive temperature coefficient, i.e. it increases proportionate to the temperature. All breakdown voltages greater than 5.7 V are caused by the avalanche effect. Avalanche diodes are often wrongly called Zener diodes. Operating a diode in avalanche breakdown is only permitted if explicitly specified in the datasheet.

2.2.1.4 Dynamic behaviour

Turn-on behaviour

When the diode switches to conductive state, the voltage will initially increase to the maximum turn-on voltage V_{FRM}. Only when the n^--region has been completely flooded by charge carriers will the on-state voltage drop to its static value V_F (Figure 2.2.4). Forward recovery time t_{fr} is in the range of 100 ns. The steeper the current rise and the thicker the low-doped n^--region in the diode, the higher V_{FRM} will be. The turn-on peak voltage may be 300 V and above.

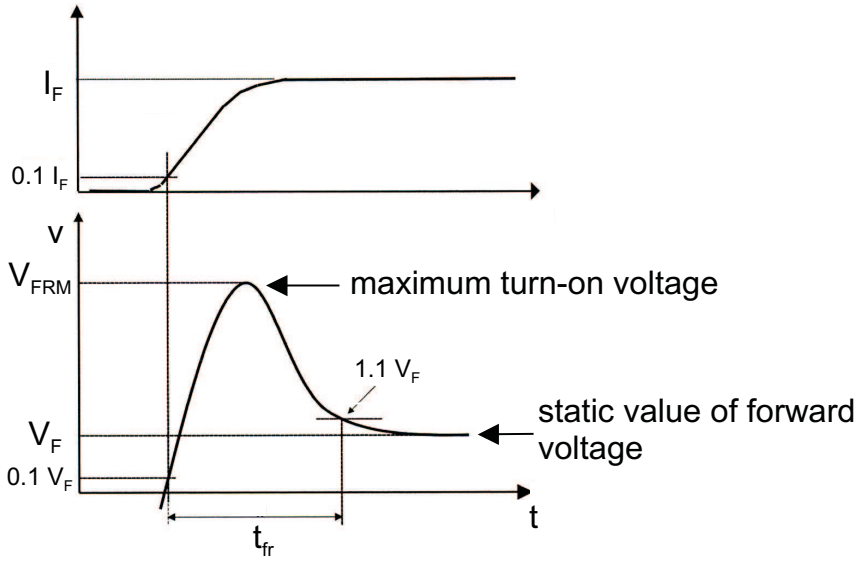


Figure 2.2.4 Diode turn-on behaviour

Turn-off behaviour

pn-diodes

In conductive state, the entire volume of the diode is flooded with electrons and holes. If voltage polarity is then reversed, the diode will also conduct in reverse direction, meaning that no blocking voltage can be built up. Owing to the reverse current and the recombination of electrons and holes, excess charge is depleted in the diode. As soon as all excess charge carriers are depleted to zero at the pn-junction, the diode can take up blocking voltage again, the peak reverse recovery current I_{RRM} is reached, and from this point on the reverse current will decline again (Figure 2.2.5).

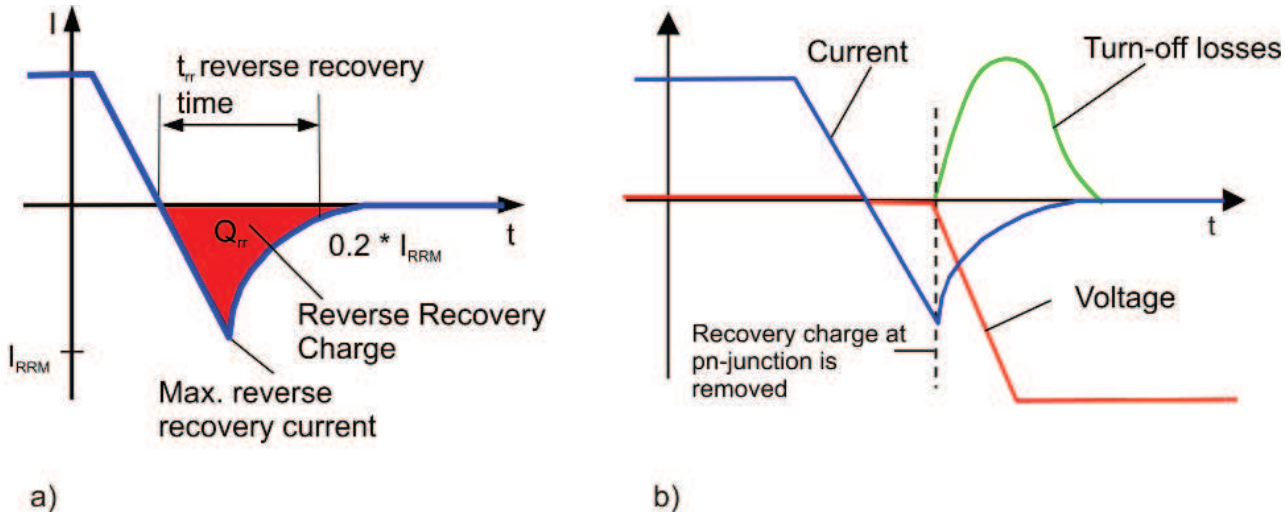


Figure 2.2.5 Turn-off behaviour of a pn-diode: definitions (a) and current curve, voltage and switching losses (b)

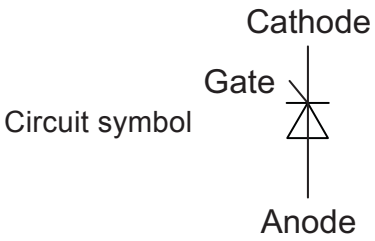
The red triangle Q_{rr} is the charge stored in the diode. When the peak reverse recovery current I_{RRM} has passed, voltage is present at the diode and a current flows through it. This results in switching losses, which may reach considerable levels when higher frequencies are applied and must be taken into account in the total losses. Reverse recovery time t_{rr}, storage charge Q_{rr} and peak reverse recovery current I_{RRM} increase strongly at higher temperatures. Diodes with a short reverse recovery time t_{rr}, small storage charge Q_{rr} and low peak reverse recovery current I_{RRM} are called fast diodes (see chapter 2.3). Fast diodes are obtained by reducing the carrier life, for example.

Schottky diodes

Schottky diodes are unipolar components; only one type of charge carrier is responsible for current transmission. While the on-state current is flowing, no excess charge which could appear as storage charge when the diode is turned off (reversed polarity) is built up. This means that Schottky diodes have no reverse current I_{RRM}, apart from a very low current for recharging the junction capacitance. A reverse recovery time is not defined.

Owing to their minimal switching losses, Schottky diodes are highly suitable for use in high-frequency applications. Their blocking voltages, however, are limited due to the reverse currents which rise steeply when the temperature rises and the unipolar on-state character. Silicon-based Schottky diodes are currently available with a blocking voltage of up to around 200 V; those made of gallium arsenide (GaAs) are suitable for up to 300 V, while Schottky diodes made of silicon carbide (SiC) are available for up to 1200 V. The suitability of SiC for high-blocking Schottky diodes is down to the material's breakdown field intensity, which is nine times higher than silicon.

2.2.2 Thyristors



2.2.2.1 General terms

Forward direction, switching direction

The direction of current flow through the main terminals in which the thyristor can assume two stable operating states, i.e. off-state and on-state.

Reverse direction

The direction opposite to switching direction.

On-state

Operating state at a certain operating point or operating point range where the DC resistance is small (compared to the resistance in off-state).

Off-state

Operating state where the DC resistance is high (compared to the resistance in on-state).

Anode terminal

Main terminal where the forward current enters the thyristor.

Cathode terminal

Main terminal where the forward current leaves the thyristor.

Gate

Terminal through which only gate current flows. The device intended for control is connected to the gate and the cathode terminal. For this purpose, larger thyristors are equipped with a second cathode terminal.

Forward current

The current flowing in forward direction through the main terminals.

Reverse current

The current flowing in reverse direction through the main terminals.

On-state current

The current flowing through the main terminals in on-state.

Off-state current

The current flowing through the main terminals in off-state. If the off-state current is displayed using a plotter, an oscilloscope or a similar measuring instrument with a screen, DC voltage should be used for measurements if possible. If measurements are taken using AC voltage, it is important to note that the capacitance of the pn-junction causes a split in the characteristic curve. Depending on the rising or falling voltage, there will be a positive or negative displacement current which splits the characteristic into two branches. The point in the peak of the measurement voltage is not distorted by capacitive influences and shows the true reverse current (see Figure 2.2.1).

Forward voltage

Voltage applied at the main terminals in forward direction.

Reverse voltage

Voltage applied at the main terminals in reverse direction.

On-state voltage

Voltage applied at the main terminals in on-state.

Reverse voltage

Voltage applied at the main terminals in off-state.

Breakover voltage

Blocking voltage in forward direction, where the thyristor suddenly transits into on-state without gate current flowing.

Gate current

The current flowing through the gate. This is called positive when it flows into the gate.

Gate voltage

Voltage between gate and cathode terminal. This is known as positive if the gate has the higher potential.

2.2.2.2 Structure and functional principle

A thyristor is a semiconductor component with a minimum of 3 pn-junctions which can be switched from off-state to on-state. Often, "thyristor" specifically designates the reverse-blocking triode thyristor which cannot be switched in reverse direction but blocks. In addition to the two terminals that a diode provides, a thyristor has a gate which serves to switch the thyristor to the on-state (Figure 2.2.6).

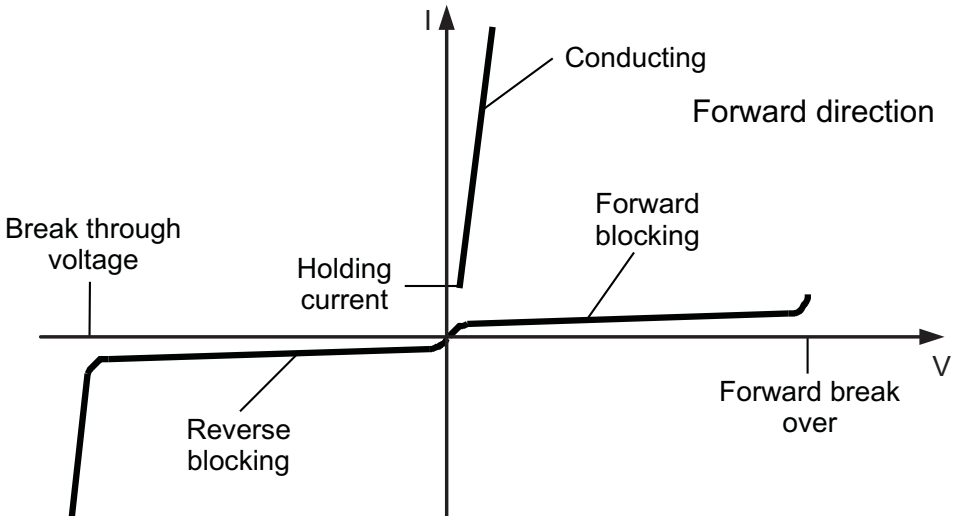


Figure 2.2.6 Current-voltage characteristic of a thyristor with voltage directions and operating states.

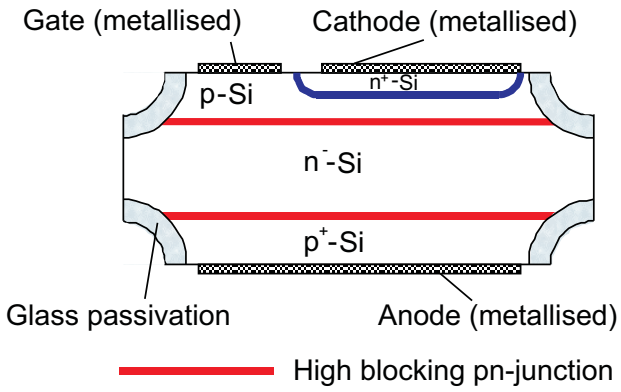


Figure 2.2.7 Diagram of a thyristor (glassivation acts as protection from environmental impacts and stabilizes reverse currents).

A thyristor consists of four alternate n-doped and p-doped regions (Figure 2.2.7). Together with the adjacent p-doped regions, the middle n^--region forms the high-blocking pn-junctions in forward and reverse direction. Passiviation (here: glassivation) must be performed for both pn-junctions. In order to be able to understand how a thyristor works, you can first imagine the thyristor divided into an NPN transistor and a PNP transistor (Figure 2.2.8)

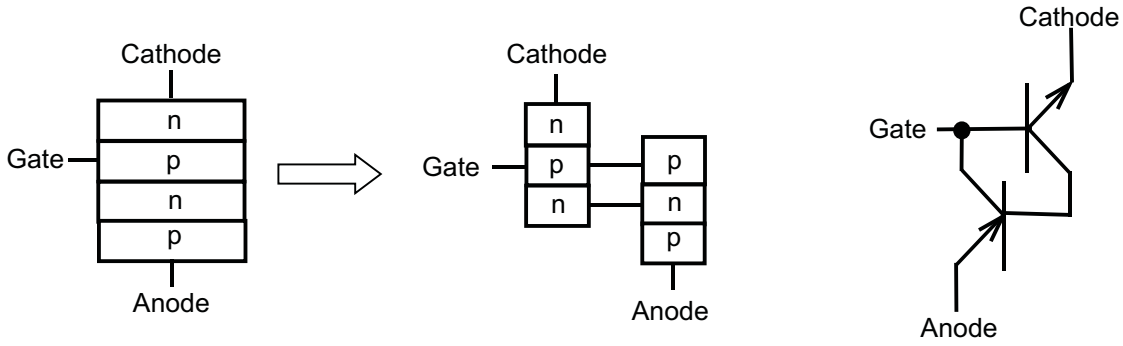


Figure 2.2.8 Splitting a thyristor into two coupled NPN and PNP transistors

If the cathode is negatively polarized with respect to the anode, a current will flow from the gate to the cathode; as a result, the cathode, which is the emitter of the NPN transistor, will inject electrons. The gate current is amplified by the NPN transistor. Some of these electrons will reach the low-doped region which simultaneously acts as collector of the NPN transistor and basis of PNP transistor. In the PNP transistor, this current is further amplified and conducted to the basis of the NPN transistor. This coupling of the transistor parts is crucial for the functioning of the thyristor.

The current amplification in the transistor is current-dependent. As soon as the current in the gate region becomes so high that the sum of current gains (in basis circuit) results in $\alpha_{npn} + \alpha_{pnp} \geq 1$, the current is amplified beyond all measure and the thyristor is triggered, meaning it turns into an on-state. A short current pulse to the gate (e.g. lasting 10 µs) is sufficient to trigger the thyristor. If the main current has exceeded the latching current I_L at the end of the trigger pulse, the thyristor will stay in on-state. Only if the main current falls below the holding current I_H will the thyristor switch back to forward off-state (blocking state) (see chapter 2.2.2.3). Every current flowing through the pn-junction from the gate to the cathode acts as trigger current if it is high enough:
- External trigger current from gate to cathode
- Off-state current by exceeding the maximum blocking voltage (breakover voltage) ("break-over triggering")
- Current generated in the space charge region by light incidence (light triggering)
- Excessive temperature (thermally generated off-state current)
- Capacitive displacement current owing to steeply rising anode voltage (dv/dt).

2.2.2.3 Static behaviour

On-state behaviour

The on-state behaviour of thyristors corresponds to that of diodes. When forward voltage is applied, current will increase steeply as soon as the threshold voltage has been reached (Figure 2.2.6). Only at very high currents which are far above the permissible continuous current will this on-state curve level out slightly. For low and medium currents, the temperature coefficient of the on-state voltage is negative, which means that, at constant current, the higher the temperature, the lower the on-state voltage. With very high currents this behaviour is reversed.
When the on-state current flows, on-state losses are created (= on-state current * on-state voltage), heating up the thyristor. This heat build-up limits the forward current, since excessive heat might damage the thyristor.

Blocking behaviour

If **voltage is applied to a thyristor in reverse direction**, the off-state current will initially rise until it reaches a level - at just a few volts - which will barely increase further as the voltage is increased. The off-state current is highly temperature-dependent and increases in proportion to the temperature. If the voltage applied in reverse direction is increased until it reaches the breakdown region (Figure 2.2.6), the off-state current will rise steeply as a result of the avalanche effect (see chapter 2.2.1.3).

If **voltage is applied to a thyristor in forward direction**, it initially behaves as it would if voltage were applied in reverse direction. If breakover voltage is reached, the thyristor will suddenly transit into on-state and stay in this condition until this value falls below the latching current. Forward off-state voltage is also temperature-dependent. This dependence can vary greatly from one thyristor to another. At high temperatures, the forward off-state current is often higher than in reverse direction. The reason for this is usually the off-state current gain from the NPN transistor for which this off-state current is a base current. High forward off-state currents do not limit the functionality and reliability of thyristors; they do not constitute a quality impairing characteristic. Under normal operating conditions, the losses that occur (= blocking voltage * off-state current) are so small that they can be neglected when calculating the overall losses.

2.2.2.4 Dynamic behaviour

Turn-on behaviour

Firing by way of an external trigger current from gate to cathode

Thyristor firing starts locally at the point where the highest trigger current density is present. The triggered area spreads relatively slowly (depending on the conditions, at a rate of between 30 µm and 100 µm per µs), meaning that for a thyristor diameter of 100 mm, it will take some 1,000 microseconds for the entire thyristor surface to become conductive (Figure 2.2.9).

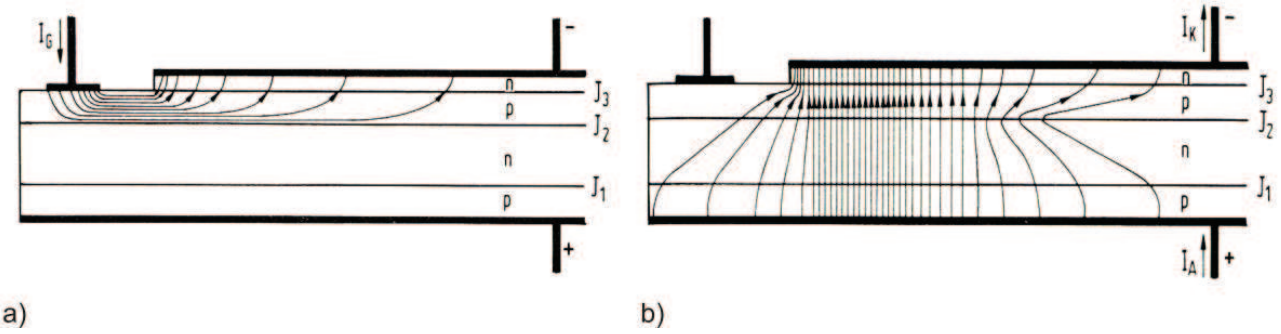


Figure 2.2.9 Current distribution in the thyristor after gate current turn-on (a) and immediately after firing (b)

After the thyristor has been fired, the forward voltage will drop very slowly to the static value V_F. This results in a power loss peak which grows in proportion to the current rise slope (Figure 2.2.10).

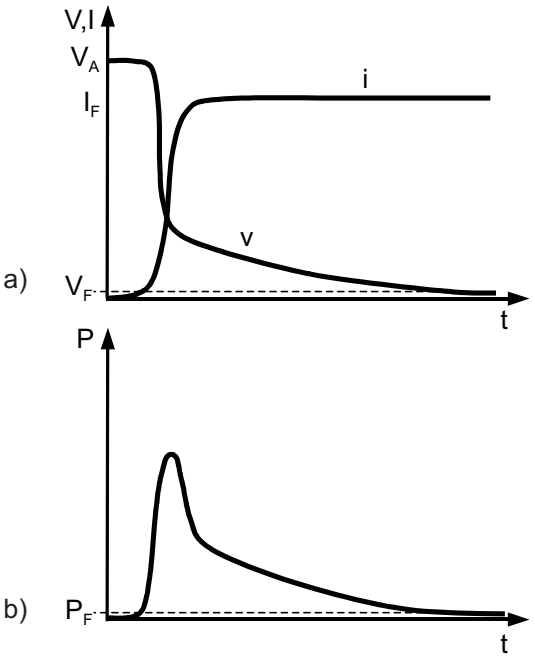
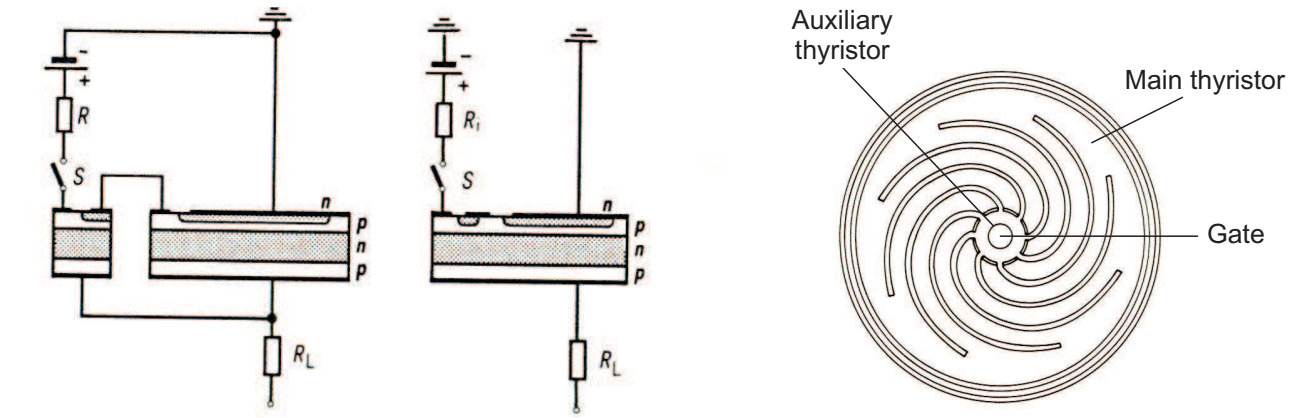


Figure 2.2.10 Current and voltage curves (a) and losses (b) during thyristor turn-on.

Since the area fired initially is very small, the turn-on losses caused by the gradual decline of the on-state voltage to its static value V_F are concentrated on a small area. This causes the silicon to heat up locally. In order to avoid damage to the thyristor, the rate of current rise must be limited to the maximum permissible **critical rate of current rise** $(di/dt)_{cr}$.

For larger thyristors, the critical rate of current rise $(di/dt)_{cr}$ is increased by integrating an auxiliary thyristor (pilot thyristor). Here, a smaller thyristor whose cathode is connected to the gate of the main thyristor serves to amplify the trigger current for the main thyristor (Figure 2.2.11). The trigger energy for the main thyristor is taken from the main circuit. This is called internal turn-on amplification or **amplifying gate-thyristor**.



Hybrid auxiliary thyristor | Integrated auxiliary thyristor | Finger like auxiliary thyristor

Figure 2.2.11 Trigger energy amplification using an auxiliary thyristor (amplifying gate).

The ratio of $(di/dt)_{cr}$ is further improved by the finger-shaped amplifying gate which extends the edge length between auxiliary and main thyristor. A shortcoming of this, however, is that the active emitter area is reduced, as is the current carrying capacity.

Thyristor firing using capacitive displacement current (dv/dt firing)

Every pn-junction is a voltage-dependent capacitance. This capacitance will be biggest if no voltage is applied, and will drop as the blocking voltage applied is increased. Changes in voltage (high dv/dt) cause a capacitive displacement current to flow through the pn-junction. If this current is high enough, it can, like any other current through the p-base–emitter-junction, induce thyristor firing.

Triggering by exceeding the breakover voltage ("overhead firing")

If the breakover voltage is exceeded (Figure 2.2.12), the off-state current will become so high that it will fire the thyristor. Since the off-state current rises in proportion to the temperature and the necessary trigger current decreases in proportion to the temperature, the breakover voltage will decline in proportion to the increase in temperature.

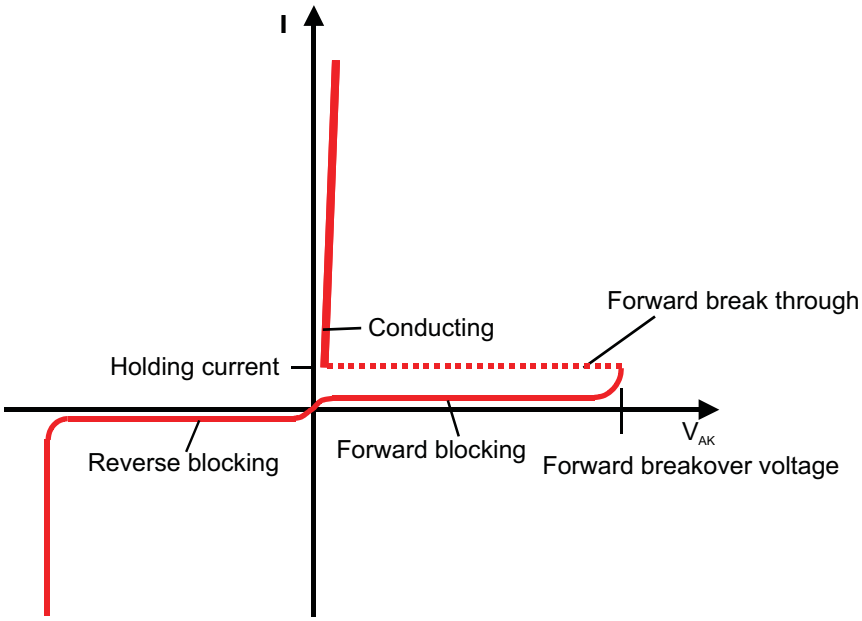


Figure 2.2.12 Triggering a thyristor by exceeding the breakover voltage

Triggering by light or excessive temperature

Light incidence creates charge carrier pairs which are separated in the space charge region and flow through the pn-junction to the cathode. They therefore act like a trigger current. The same is true for thermally generated charge carrier pairs.

Turn-off behaviour

As is the case for line rectifier diodes (see chapter 2.2.1.4), the volume of a thyristor semiconductor is also flooded by charge carriers when a forward current flows. The majority of these charge carriers have to be depleted when the voltage is reversed for the thyristor to be able to pick up voltage in reverse direction. That said, residual charge carriers will still be present in the semiconductor volume and these may cause thyristor firing if voltage is applied in forward direction.

The **circuit commutated turn-off time t_q** refers to the time that elapses from the moment of zero-current-crossing until the moment that blocking voltage can be re-applied without the thyristor re-firing (Figure 2.2.13). The typical t_q for thyristors is about 100 to 500 µs. **Fast thyristors (frequency thyristors)** are thyristors where the circuit commutated turn-off time has been shortened to between 10 and 100 µs by reducing the carrier life. More details on the dependency of the circuit commutated turn-off time on the parameters can be found in chapter 3.2.5.2. The characteristics are explained in chapter 3 "Datasheet parameters".

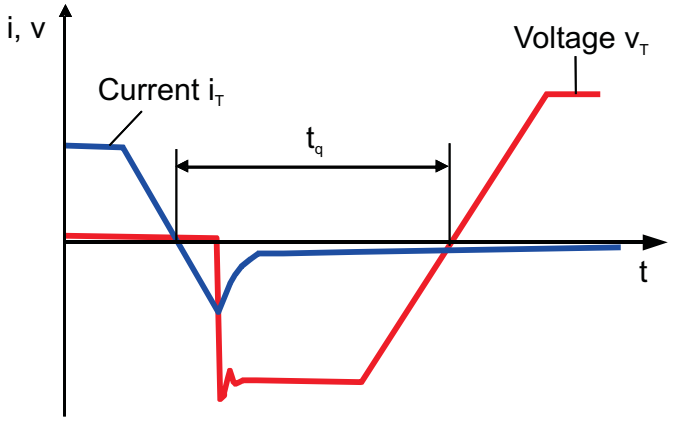


Figure 2.2.13 Current i_T and voltage v_T curves of a thyristor during turn-off and circuit commutated recovery time t_q

2.3 Freewheeling and snubber diodes

2.3.1 Structure and functional principle

Modern fast switching devices require fast diodes as freewheeling diodes in the power circuit. In the predominant applications which use inductive loads, the freewheeling diode is commutated from conductive to blocking state with every turn-on operation of the switch. Here, storage charges are to be depleted gently in order to avoid induced voltage spikes and high-frequency oscillations. For this reason, these diodes are also referred to as soft-recovery diodes. They are also instrumental to switch performance. When designing these devices, a compromise between conflicting requirements has to be found. Two main types of fast diodes exist: the Schottky diode, and pin-diodes in epitaxial or diffused design.

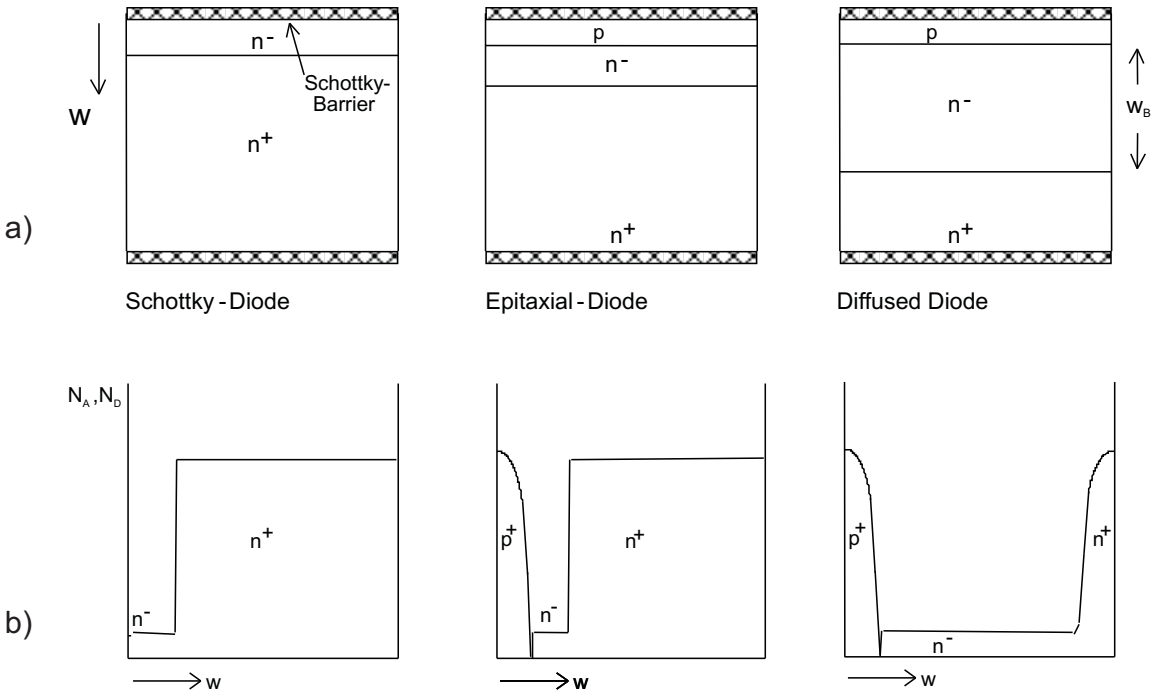


Figure 2.3.1 Schottky, pin-epitaxial and pin-diffused diode
a) basic structure
b) doping profile diagram

2.3.1.1 Schottky diodes

In Schottky-diodes, the metal-semiconductor junction serves as a blocking junction. In on-state, only the small potential barrier between metal and semiconductor material must be overcome (around 0.3 V for silicon). There is no diffusion voltage at the pn-junction as is the case in pin-diodes (approx. 0.7 V for Si); this ensures a lower on-state voltage than occurs in any pin-diode, provided the n^--region is thin. With n-doped material, only electrons participate in the current flow (unipolar). When diodes are operated close to the blocking voltage range, the off-state current will considerably increase. This must be taken into account for power loss ratings, otherwise thermal stability cannot be ensured.

When switching from conductive to blocking state, ideally only the low capacitance of the space charge region has to be charged. For this reason, the component storage charge is some powers of ten lower than the pin-diode, thus causing very low switching losses. As a result, the Schottky diode comes very close to being an ideal diode. The Schottky diode is particularly well suitable for use at very high frequencies and as a snubber diode with an extremely low on-state voltage.

For silicon, these advantages are limited to voltages < 100 V. When higher blocking voltages are to be applied, the n^--region must be extended and the on-state voltage will increase considerably. In this voltage range, materials with a higher permissible electric field intensity such as GaAs (<= 600 V) or SiC (<=1700 V) are used. They have similar on-state characteristics to pin-diodes, but the advantages they offer as regards switching properties are retained. The costs for the base material and the manufacture of diodes made of the materials mentioned last are so high, however, that it only makes sense to use them in applications that require a particularly high efficiency, switching frequencies or temperatures.

2.3.1.2 PIN diodes

Epitaxial diodes

The advantages of pin-diodes become effective from 100 V upwards. In diodes produced today, the middle region is not "i" (intrinsic), but n^--type, with a much lower doping level than in the outer regions. In epitaxial PIN diodes (Figure 2.3.1 mid) an n^--region is first separated from the highly doped n^+-substrate (epitaxy). Then the p-region is diffused. In this manner, very small base widths w_B in the region of just a few µm can be obtained. By integrating recombination centres (mostly gold), ultra-fast diodes can be achieved. Owing to the small base width w_B, the on-state voltage will remain low despite the recombination centres. That said, it will still always be greater than the diffusion voltage of the pn-junction (0.6 to 0.8 V). The main field of application for epitaxial (epi)-diodes are applications with off-state voltages of between 100 V and 600 V; some manufacturers even produce epi-diodes for 1200 V.

Controlled axial lifetime (CAL) diodes

From 1000 V upwards, the n^--region is being enlarged to such an extent that a diffused PIN diode (Figure 2.3.1 to the right) can be obtained. The p- and n^+-regions are diffused into the n^--wafer. Recombination centres are also used. Recombination centre profiles similar to those shown in Figure 2.3.2 can be generated by implanting protons or He^{++}-ions into silicon. Implantation requires particle accelerators performing up to 10 MeV.

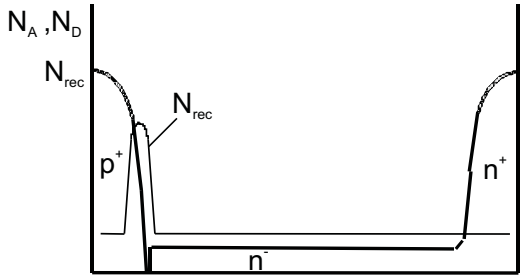


Figure 2.3.2 Narrow region with a high concentration of recombination centres at the pn-junction, generated by light ion irradiation

The arrangement of the high recombination centre density at the pn-junction (Figure 2.3.2) is an optimum set-up [4], [5]. In [6] it is demonstrated that the closer the arrangement of recombination centres at the pn-junction, the better the relation between peak reverse recovery current and forward on-state voltage will be. In on-state condition, charge carrier distribution will be inverted, with a higher charge carrier density at the n^--n^+-junction. As shown in Figure 2.3.3, the peak of radiation-induced recombination centres is even placed in the p-region close to the pn-junction in a CAL diode, since this will result in lower off-state currents. He^{++} implantation is combined with an adjustment to the basic charge carrier lifetime, preferably achieved by electron beam radiation.

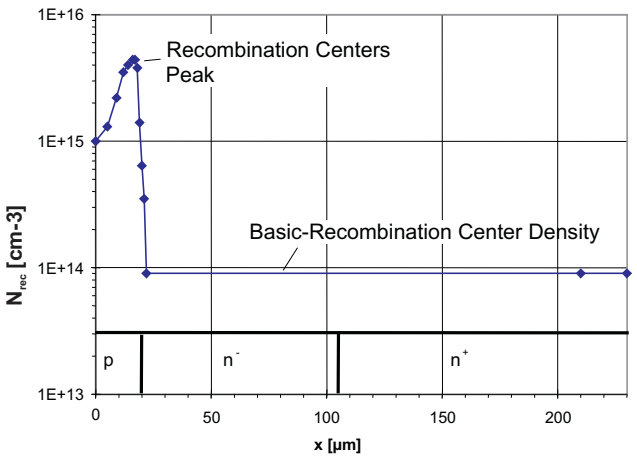


Figure 2.3.3 Recombination centre profile in the CAL diode (diagram)

The height of the recombination centre peak can be adjusted by varying the dose of He^{++}-implantation: The higher the peak, the smaller the peak reverse recovery current. The lion's share of the CAL diode storage charge occurs in the tail current. The tail current itself can be controlled by the basic recombination centre density. A reduction in basic charge carrier lifetime will reduce tail current duration; however, this is to the detriment of the diode on-state voltage. The two parameters "basic charge carrier lifetime" and "He^{++} implantation dose" enable the recovery behaviour be controlled to a large extent. In this way, the diode will display soft-recovery behaviour under any operating conditions, especially when low currents are applied. CAL diodes manufactured in this way boast excellent dynamic ruggedness. CAL diodes dimensioned for 1200 V and 1700 V have been tested under lab conditions at dI/dts up to 15 kA/cm²µs and did not result in diode destruction.

A comparatively narrow base width w_B can be chosen for CAL diodes regarding the PT (punch through) dimensioning described in chapter 2.3.2.2. This provides a comparatively low on-state voltage or results in a better compromise between switching characteristics and on-state voltage. The base width w_B also has a considerable impact on the turn-on behaviour of the diode. The forward recovery voltage V_{FR} rises in proportion to the increase w_B. In contrast to conventional diodes, 1700 V-CAL diodes were shown to result in a more than a 50% reduction in V_{FR} [7].

Freewheeling diodes for IGCT with high reverse voltage ratings, as well as snubber diodes [8] are manufactured in line with the CAL concept, since dynamic ruggedness is one of the most important requirements. Optimised dimensioning in the direction of PT dimensioning now becomes possible, resulting in improved cosmic ray stability. This also allows for a more favourable trade-off between diode on-state voltage and switching characteristics. In snubber diodes, this enables a minimum V_{FR} to be reached. In addition, a lower reverse current can be obtained than is the case for the conventional gold-diffusion process.

Emitter concept

In a common PIN diode, the pn-junction is flooded by more charge carriers than the n^--n^+-junction (Figure 2.3.11). The idea behind the emitter concept is to invert this charge carrier distribution: the n^--n^+-junction is to be flooded by more charge carriers than the pn^--junction. This is achieved by reducing the injection quantity at the p-emitter.

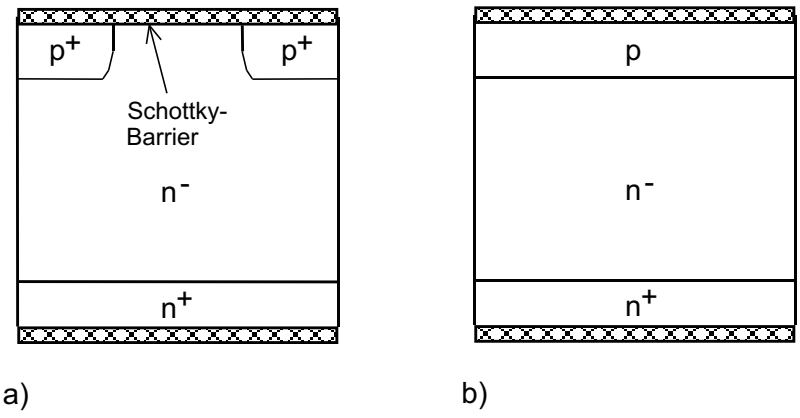


Figure 2.3.4 p-emitter to improve soft recovery behaviour:
a) Emitter structures, e.g. merged PIN/Schottky diode
b) Fully reduced p-doping

A number of emitter structures whose functions basically result in this effect have been proposed. One example is the "Merged PIN/Schottky diode", which consists of a series of p^+-regions and Schottky regions [9] (Figure 2.3.4a). A number of similar structures also exist, including structures with diffused p-regions and n-regions.

The advantages of Schottky regions or similar regions, however, are restricted to voltages below 600 V. For blocking voltages of 1000 V and above, the ohmic voltage drop outweighs this effect. What is left is the reduction of the area of injecting sub-areas at the p-region. The same effect as with emitter structures can be achieved with a uniformly low-doped p-region (Figure 2.3.4b).

2.3.2 Static behaviour

The statements made about the static behaviour of line rectifier diodes in chapter 2.2.1.3 essentially apply to fast diodes, too.

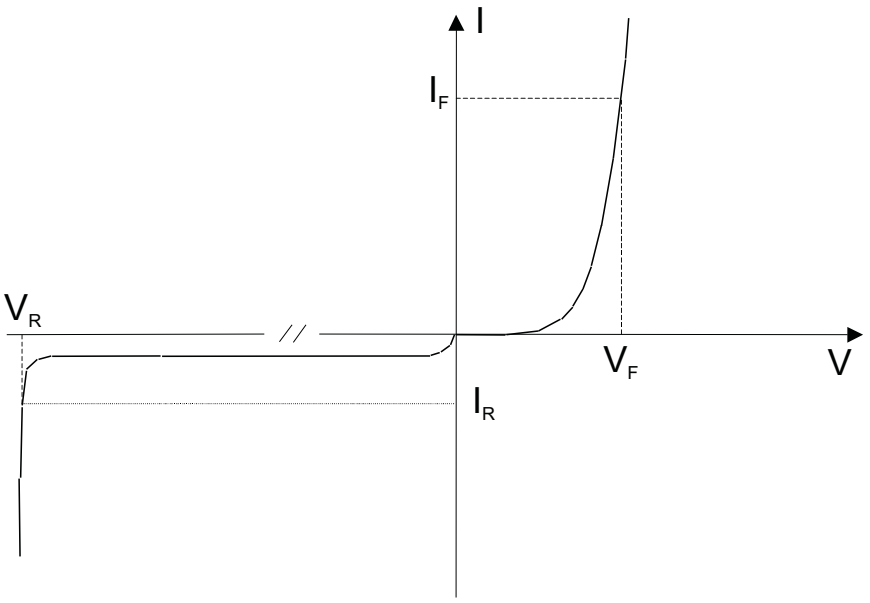


Figure 2.3.5 Definition of reverse and forward diode voltage

2.3.2.1 On-state behaviour

The maximum forward voltage V_F indicates that, at a specified current, the forward voltage drop across the diode must not exceed the specified limit value. This specification is made for room temperature and a higher temperature, typically the maximum recommended operating temperature. In forward direction, the current must overcome the diffusion voltage of the pn-junction and the resistance of the adjacent n^--region. The voltage drop is composed of

$$V_F = V_{diff} + V_{ohm}$$

The diffusion voltage at the pn-junction depends on the amount of doping of both sides of the pn-junction and it is typically in the range of 0.6...0.8 V. The ohmic share depends on the base width w_B (proportionate to the blocking voltage) and the charge carrier density. For fast diodes with a blocking voltage of 600 V and above, the ohmic part dominates. The charge carrier lifetime of freewheeling diodes has to be kept so short that the on-state voltage will depend exponentially on the base width w_B and the charge carrier lifetime τ [10]:

$$V_{ohm} = \frac{3 \cdot \pi kT}{8q} \cdot e^{\frac{w_B}{2\sqrt{D_A \cdot \tau}}}$$

with the ambipolar diffusion constant

$$D_A = 2\frac{\mu_n \mu_p}{\mu_n + \mu_p}\frac{kT}{q}$$

k: Boltzmann constant; 1.38066 _ 10^{-23} I/K
q: electronic charge; 1.60218 _ 10^{-19}
T: absolute temperature [K]

Here, μ_n and μ_p represent electron and hole mobility, provided the n^--region is flooded with free electrons and holes [11]. Due to this exponential correlation, it is important to select the smallest possible w_B.

The diffusion voltage has a negative temperature coefficient, while the ohmic voltage part has a positive temperature coefficient. Depending on which part is dominant, there will be an intersection of the on-state characteristic "Hot" and "Cold" at different current levels, typically within the rated current range or up to 3-4 times the rated current.

2.3.2.2 Blocking behaviour

The reverse voltage V_R indicates that, at a specified value, the reverse current must not exceed the limit for I_R. Specifications in the databooks are made for an operating temperature of 25°C. In case of lower temperatures, the blocking capability will decrease, for example by about 1.5 V/K for a 1200 V diode. For components which are operated at temperatures below room temperature, this has to be taken into account in the circuit layout. At higher temperatures, the blocking voltage will increase accordingly. At the same time, the reverse current will also rise, doubling roughly every 10 K. For this reason, a reverse current is also specified for a high temperature (125°C or 150°C). For gold-diffused components, the reverse current increase may be very strong, possibly causing problems due to thermal instability in systems operated at high temperatures.

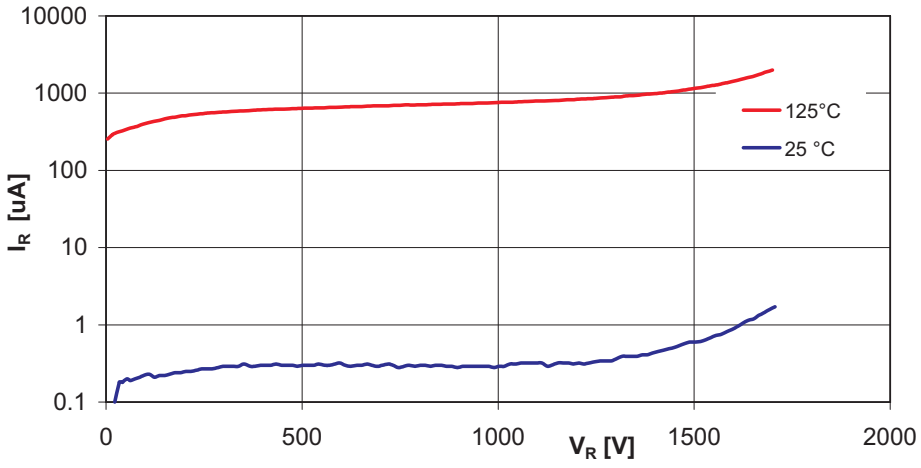
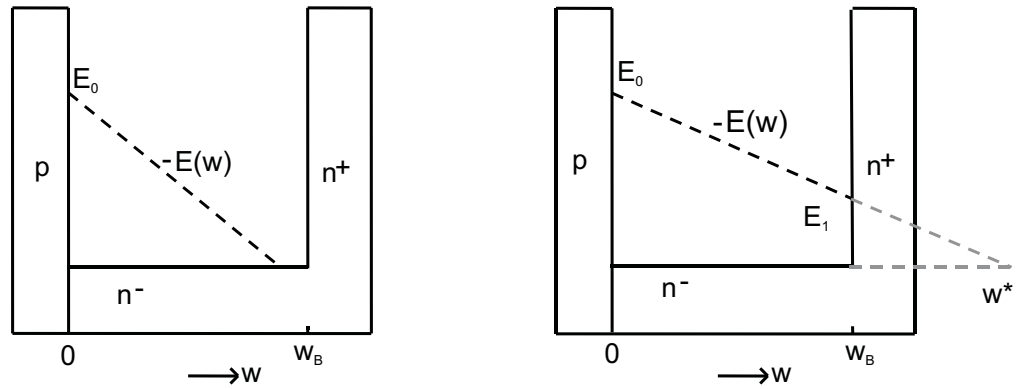


Figure 2.3.6 Example of the reverse current of a 1700 V CAL diode, parameter T_j

The base width w_B not only affects the on-state voltage, but also has a crucial impact on the blocking voltage. Two cases can be distinguished between (Figure 2.3.7): if w_B has been dimensioned such that the space charge zone cannot protrude into the n^+-region (triangular field shape), this is called Non-Punch-Through (NPT) dimensioning in line with the terminology used for IGBT [12]. If w_B has been dimensioned such that the space charge region protrudes into the n^+-region, the field shape will be trapezoidal and the diode is called a Punch-Through (PT) diode. This, however, is not actual punch-through, where the space charge region would reach the area of the other doping type. This designation has nonetheless become widely accepted.



non-punch-through (NPT)-Diode a)

punch-through (PT)-Diode b)

Figure 2.3.7 Diode dimensioning for triangular (a) and trapezoidal (b) field shape for $0 \le w \le w_B$

For an ideal NPT diode, w_B is selected such that, at maximum reverse voltage, the end of the triangular field is located at this point. For optimum doping, the minimum width would then be

$$w_{B(NPT)} = 2^{\frac{2}{3}} C^{\frac{1}{6}} V_{BD}^{\frac{7}{6}}$$

where $C = 1.8 \cdot 10^{-35}\ cm^6 V^{-7}$

The minimum doping needed for PT diodes can be calculated in the same way. In the extreme case, the field would be rectangular, $E_1 = E_0$ (Figure 2.3.7). This results in

$$w_{B(PT,Minimum)} = C^{\frac{1}{6}} \cdot V_{BD}^{\frac{7}{6}}$$

Compared to w_B for the NPT diode, the following applies:

$$w_{B(PT,Minimum)} = 2^{\frac{2}{3}} w_{B(NPT)} \cong 0{,}63 \cdot w_{B(NPT)}$$

Although this extreme case cannot be achieved, available technology allows us to come close to this, i.e.:

$$w_{B(PT)} \cong 0{,}66 \cdot w_{B(NPT)}$$

For the charge carrier lifetimes presently in use, the difference in forward voltage for PT dimensioning and NPT dimensioning is approximately 0.8 V. For this reason, PT dimensioning is to be given preference if possible.

2.3.3 Dynamic behaviour

2.3.3.1 Turn-on behaviour

When the diode is turned on, it has to overcome the resistance of the low-doped base. The turn-on peak voltage thus increases proportionate to w_B. The turn-on peak voltage becomes especially critical if a significant base width w_B has to be chosen due to a high blocking voltage of more than 1200 V. For this reason, optimum turn-on behaviour is once again achieved with PT diodes.

Freewheeling diodes always contain recombination centres to reduce charge carrier lifetime. Recombination centres (e.g. gold) causing an increase in base resistance are to be avoided for diodes with a high blocking voltage. Recombination centres generated by platinum diffusion, electron beam radiation or light ions will only slightly increase the turn-on overvoltage in comparison to diodes without recombination centres.

When the diode turns into the conductive state, the voltage will initially increase to the repetitive peak forward voltage V_{FRM} before dropping to the forward voltage level again (Figure 2.2.4). When the current is actively switched at a very high di/dt ratio, V_{FRM} may reach between 200 V and 300 V for an unsuitable 1700 V-diode, a level which is more than 100 times the value of V_F. Turning the diode on from a blocked state will result in a far higher V_{FRM} than turning it on from a neutral state. A low V_{FRM} is one of the most important requirements of snubber diodes, since the snubber circuit becomes effective only after diode turn-on.

The repetitive peak forward voltage is also of importance for freewheeling diodes in IGBT which are designed for a blocking voltage > 1200 V. When the IGBT is turned off, a voltage spike is generated across the parasitic inductances which still superimposes the V_{FRM} of the freewheeling diode. The sum of both components may cause critical voltage peaks. However, this measurement is not trivial, since the inductive component and V_{FRM} cannot be told apart in application-oriented chopper circuits. Measurements can be taken on an open construction directly from the diode bonding wires. Turn-on behaviour of a diode is rarely important for the total power losses, since turn-on losses only amount to a small percentage of the turn-off and forward on-state losses and are therefore negligible.

2.3.3.2 Turn-off behaviour

When turning from the conductive into the blocking state, the internal diode storage charge has to be discharged. This causes a current to flow in reverse direction in the diode. The waveform of this current characterises the reverse recovery behaviour.

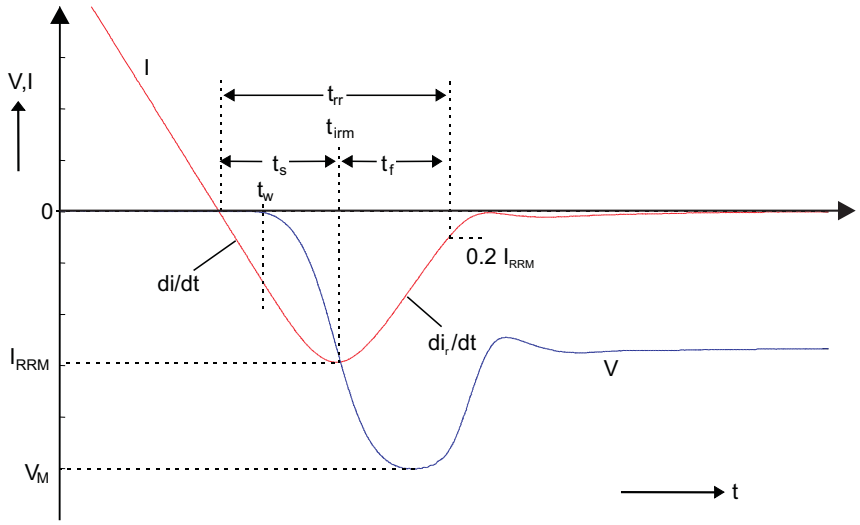


Figure 2.3.8 Current and voltage characteristic of the reverse recovery process of a soft-recovery diode in a circuit as shown in Figure 2.3.15 and definition of the characteristics of the recovery behaviour

Commutation velocity di/dt (Figure 2.3.8) is determined either by the switching speed of an active switch (IGBT) or by the commutation inductance. At t_0 the current reaches its zero crossing. At t_w the diode starts to pick up voltage. At this instant, the pn-junction in the diode becomes free of charge carriers. This constitutes a turning point in the current flow. At t_{irm} the reverse current reaches its maximum. After t_{irm} has elapsed, the current declines to the reverse current. The current characteristic depends solely on the diode. A steep decline in current is referred to as snappy recovery behaviour. A slow decline in current is referred to as soft recovery behaviour. Di_r/dt determines the overvoltage present in the diode, which is why soft recovery behaviour is aimed at. Reverse recovery time t_{rr} is defined as the period between t_0 and the moment where the current has fallen to 20% of the maximum I_{RRM}.

Soft recovery behaviour and switching overvoltage

As shown in Figure 2.3.8, differentiating between t_f and t_s for t_{rr} helps to define a "soft factor" as a quantitative characteristic for recovery behaviour:

Soft factor $$s = \frac{t_f}{t_s}$$

The soft factor should be greater than 1 in order to minimise switching overvoltages. This definition, however, is imprecise. For, according to it, the current characteristic shown in Figure 2.3.9a would be regarded as snappy, whereas the current characteristic as in Figure 2.3.9b would be considered soft. Despite s > 1, there is a steep edge in a part of the reverse current flow. A definition that refers to the maximum di_f/dt during the fall time t_f would be better. For a soft recovery diode, di_f/dt is within the range of di/dt for t_s.

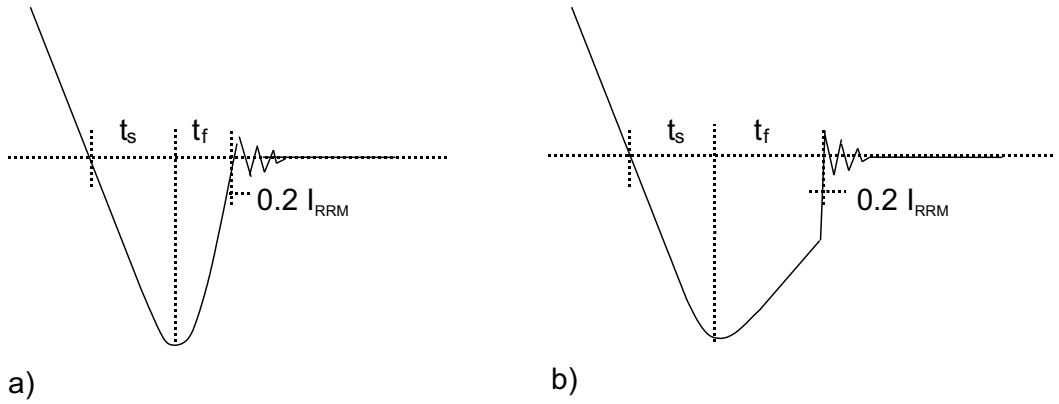


Figure 2.3.9 Current characteristic for two different possibilities of snappy reverse recovery behaviour

Specifying the recovery behaviour at the nominal operating point only is likewise not sufficiently meaningful. It varies as a function of different circuit parameters.

- Current: Measurements have to be taken at a current flow of less than 10% and at 200% of the specified current. This approach gives proper consideration to the fact that small currents are particularly critical for the reverse recovery behaviour.
- Temperature: High temperatures are often more problematic for the recovery behaviour. For certain fast diodes, however, the recovery behaviour will deteriorate at room temperature or below.
- Voltage applied: Higher voltage results in poorer reverse recovery behaviour.
- Rate of rise for di/dt: The dependency of di/dt varies greatly in diodes made by different manufacturers. One type of diode will become "softer" when the di/dt increases, while another will become "snappier".

The best way to charaterise soft recovery behaviour is to measure the turn-off overvoltage under different operating conditions (I_F, T_j, V_{CC}, di/dt). In a typical application, where the chopper is in a semiconductor module, the parasitic inductance L_{sges} is in the range of some 10 nH. This reduces the overvoltage generated. Due to a lack of ideal switches, the voltage applied to the IGBT will drop to a certain degree during the reverse recovery phase. The voltage measured becomes

$$-V(t) = -V - L_{\sigma ges} \cdot \frac{di_R}{dt} + V_{CE}(t)$$

where $V_{CE}(t)$ is the voltage across the IGBT at the given moment in time. In a 100 A soft recovery diodes with moderate rates of rise of up to 1500 A/µs and minimum parasitic inductances, V(t) will very often be smaller than V_{CC} at any time and no voltage spikes will occur.

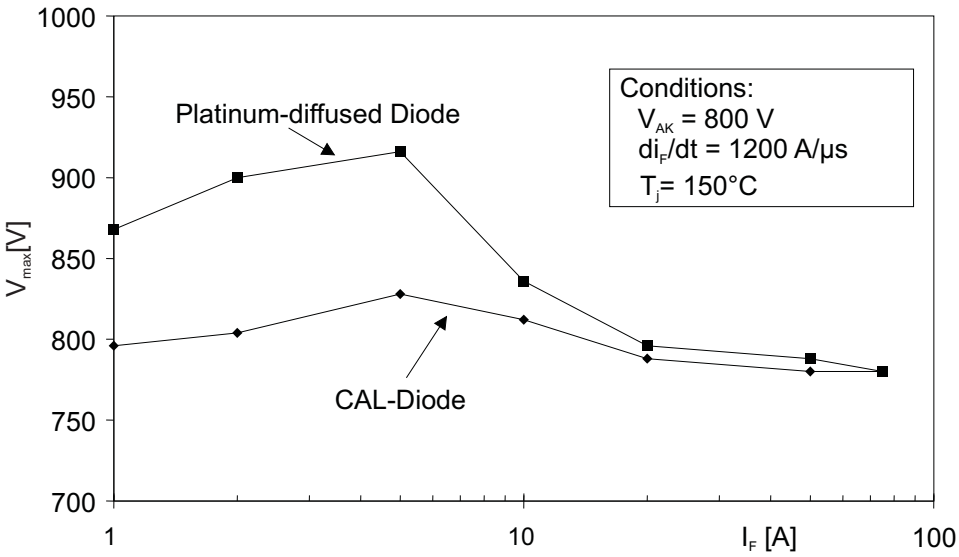


Figure 2.3.10 Peak voltage during commutation in dependence of the forward current as a parameter for diode switching behaviour

Figure 2.3.10 compares the overvoltage of a CAL diode to that of a platinum-diffused diode with soft-recovery behaviour owing to reduced p-emitter efficiency. At rated current (75 A), the platinum-diffused diode is just as soft as the CAL diode. For lower currents, however, overvoltages caused by snappy switching behaviour will be present in the diode. The maximum overvoltages at 10% rated current will be as over 100 V. The IGBT used will switch even lower currents more slowly, and the overvoltage will decrease. By way of contrast, CAL diodes don't display significant overvoltages under any condition. Considered from the point of view of semiconductor physics, Figure 2.3.11 shows the concentration of charge carriers in the cross section of the semiconductor material during turn-off in a snappy diode and Figure 2.3.12 depicts the same for a soft recovery diode.

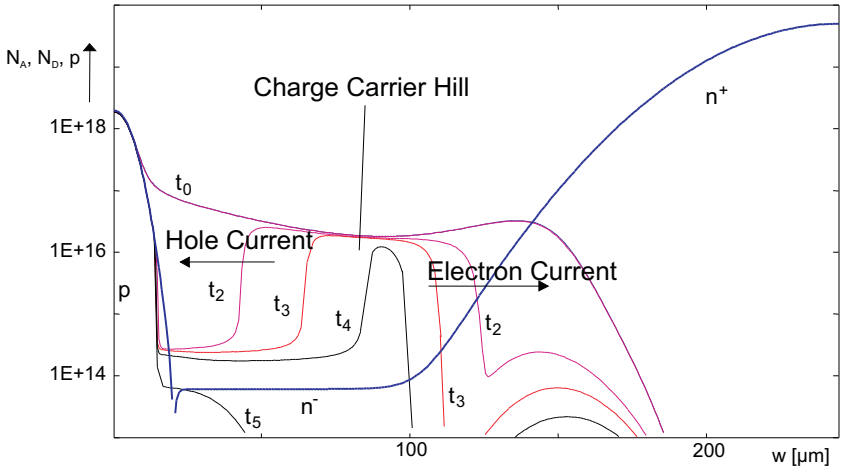


Figure 2.3.11 Diffusion profile and simulation of the decline in charge carriers (hole density) in a snappy diode

Under on-state load, the n^--region of the diode is flooded by > 10^{16} cm^{-3} of electrons and holes; the concentration of electrons (n) and holes (p) may be assumed to be equal. During the switching operation, a charge carrier hill is formed between t_2 and t_4 in the n^--region; at the same time n ≈ p. Charge carriers are reduced toward the cathode as a result of the electron flow and toward the anode owing to the hole flow, which appears as reverse current in the outer circuit. In the case of the snappy diode (see Figure 2.3.11), the charge carrier hill will have been consumed shortly after t_4 has elapsed. Between t_4 and t_5, the diode will suddenly turn from its state with charge carrier hill to a state without charge carrier hill; the reverse current will snap off.

The process in a soft-recovery diode is shown in Figure 2.3.12. Throughout the entire process, a charge carrier hill which feeds the reverse current is retained . At t_5, the diode will already have picked up the voltage applied. The dynamic behaviour described results in a tail current, as shown in the measurement in Figure 2.3.17.

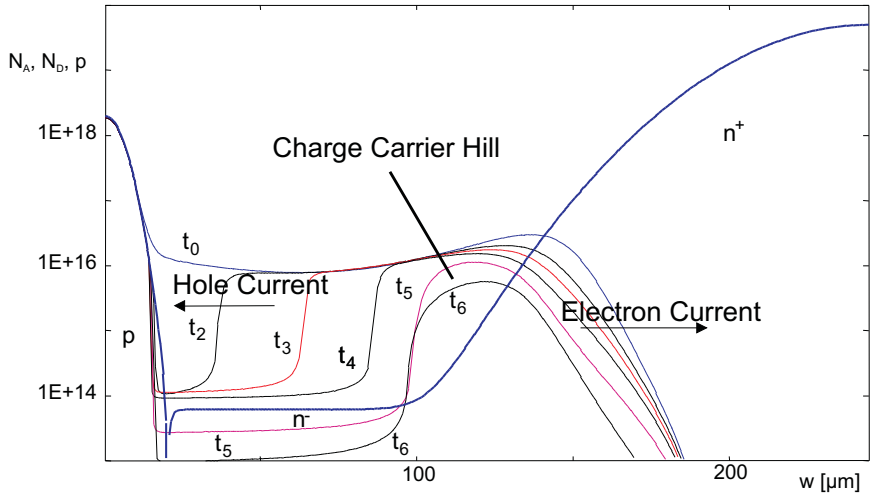


Figure 2.3.12 Diffusion profile and simulated decline in charge carriers (hole density) in a soft recovery diode

Whether soft recovery behaviour will be achieved depends on how successfully this charge carrier reduction is managed. The following measures will result in softer recovery behaviour:

- The width w_B in the n^--region is enlarged, NPT dimensioning is used, and a region is also integrated into the diode which cannot be reached by the field at nominal voltage. This, however, will result in a stark increase in on-state voltage or in the V_F/Q_{RR} relation.
- In order to restrict the increase in w_B somewhat, a two-stage n^--region can be used [13] with increased doping close to the n-n^+-junction. Figure 2.3.11 and Figure 2.3.12 demonstrate how a similar effect is achieved by a flat gradient at the n^--n^+-junction. This measure alone, however, will not be enough to achieve soft recovery behaviour.
- Charge carrier distribution is inverted by a low-efficiency p-emitter (see "Emitter concept").
- An axial charge carrier lifetime profile according to the CAL concept, providing for a low charge carrier life at the pn-junction, and a longer charge carrier life at the n^--n^+-junction.

To ensure soft recovery behaviour under any conditions, several of these measures normally have to be taken at the same time. That said, the achievements made in this respect must always be assessed with a view to the extent to which a higher on-state voltage or a higher Q_{RR} is accepted.

Minimum turn-on time

In order to reach the "soft" switching characteristics described above, the charge carriers must be granted sufficient time to reach the state of quasi-static charge carrier distribution. This is not the case for very short conduction times.

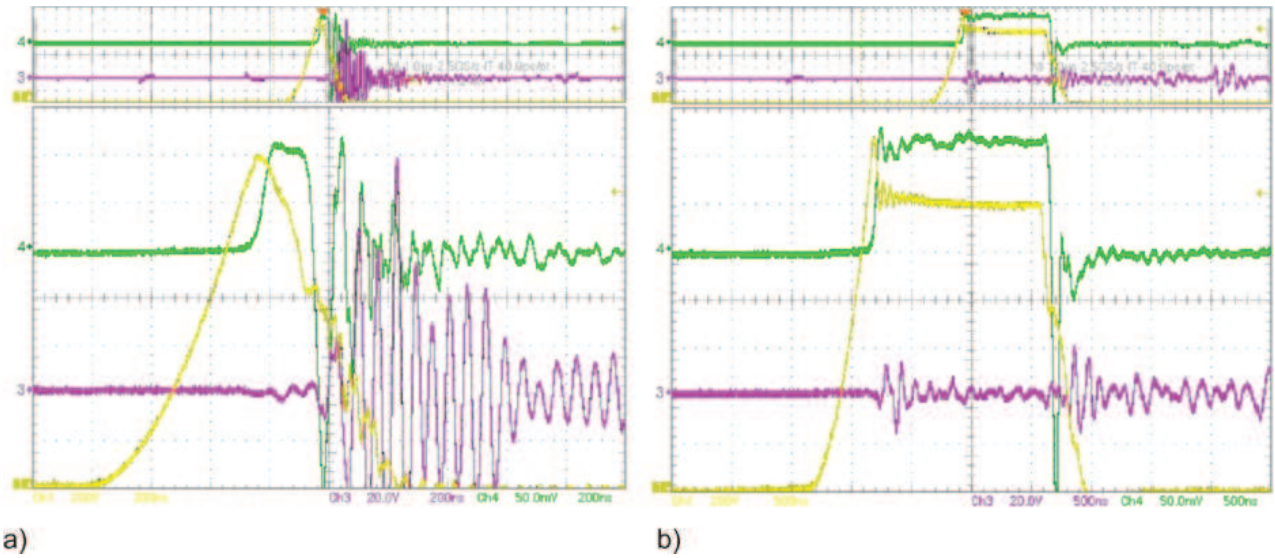


Figure 2.3.13 a) Turn-off at high interference level (pink) at V_{CC}=1200 V (V_{AK} -yellow) and I_F=400 A (green) at t_p=0.8 µs (200 ns/Div); b) Turn-off at "normal" interference level (pink) at t_p=2 µs (500 ns/Div)

Figure 2.3.13 shows switching operations during very short diode turn-on times with inductive load. The fact has been taken into account that the real turn-on time of the diode is reduced by about 1 µs, since the driver short-pulse suppression and $t_{d(off)}$ of the IGBT are subtracted from $t_{p(off)}$-IGBT. For a very short turn-on time, oscillations with a high amplitude can be detected in the the current curve (green). The interference level (pink) is only a relative measurement, taken with a conductor loop above the module. These high-frequency oscillations may influence signals and logic devices and impair safe and reliable operation. For this reason, we recommend suppressing switching signals for less than 3 µs for 1200 V IGBT and < 5 µs for 1700 V.

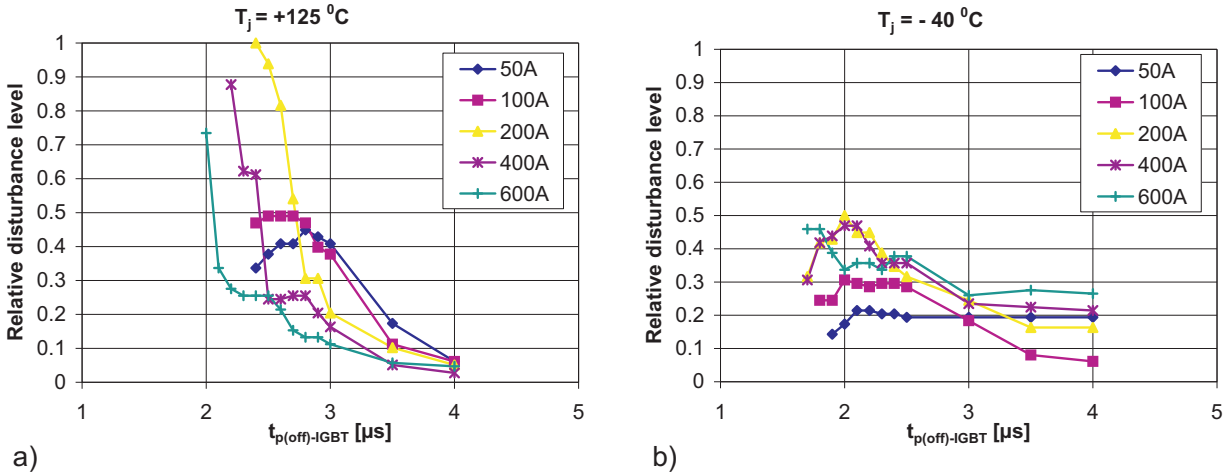


Figure 2.3.14 Relative interference level related to the maximum value at 200 A and 125°C for IGBT turn-off signals of different durations as a function of current and temperature (a) T_j=125°C, b) T_j=-40°C)

Owing to the lower mobility of charge carriers, this effect is particularly strong at high temperatures. At -40°C, the interference levels read were only around 50% of the values measured at 125°C. The highest interference level readings were taken at half the rated current (200 A) (Figure 2.3.14). For lower currents and turn-off signals of under 2 µs, the delay and switching times were so high that the diode was no longer capable of fully turning on.

Switching losses

The easiest way to charaterise turn-on and turn-off behaviour is to use a step-down converter circuit as shown in Figure 2.3.15.

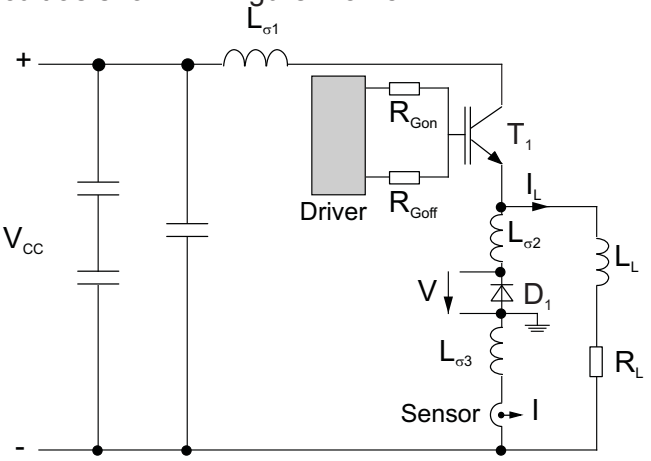


Figure 2.3.15 Reverse recovery test circuit

The IGBT T_1 is turned on and off twice by means of a double pulse. The rate of rise of commutation current di/dt is set by the gate series resistor R_{Gon}. V_{CC} is the DC link voltage. Parasitic inductances $L_{s1...3}$ are generated in the connections between capacitors, IGBT and diode. Figure 2.3.16 shows the IGBT control signals ("driver") and the current flow in the IGBT and diode during double-pulse operation. By turning off the IGBT, the load current in the inductance L_L will be taken up by the freewheeling diode. As soon as the IGBT is turned on next time, the diode will be commutated, and at that very moment its recovery behaviour will be charaterised. In addition, the IGBT takes over the reverse current of the freewheeling diode during turn-on. This process is depicted at a higher time resolution in Figure 2.3.17 for a soft recovery diode.

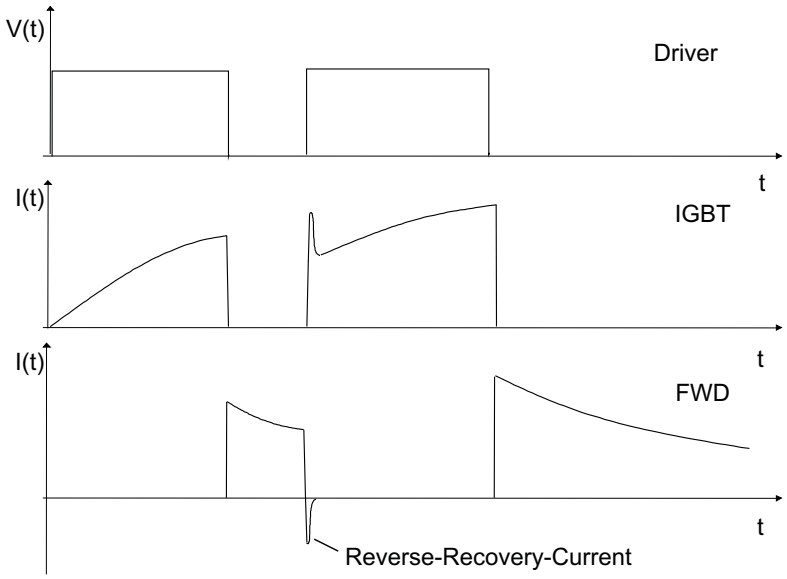


Figure 2.3.16 Driver control signal, IGBT and freewheeling diode current flow in a circuit during double-pulse operation

When the IGBT conducts the peak reverse current, the IGBT voltage is still on DC-link voltage level (Figure 2.3.17a). This is the moment of maximum turn-on losses in the IGBT. The diode reverse recovery characteristic may be divided into two phases: The phase of increase up to the reverse peak current and the subsequent drop in reverse current with di_r/dt.

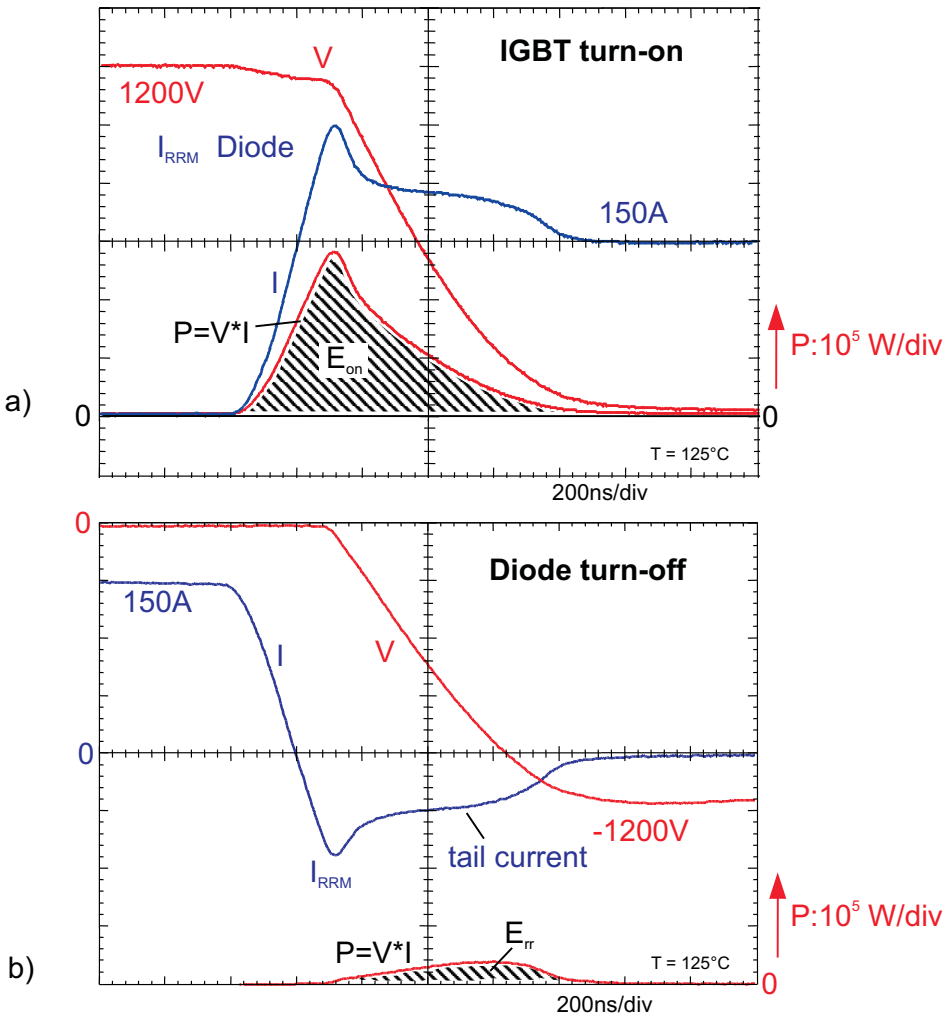


Figure 2.3.17 Current, voltage and power losses during turn-on of a 150 A / 1700 V IGBT (a) and diode turn-off (b) during recovery behaviour measurements

The second part is the tail phase where the reverse current slowly declines to zero. A t_{rr} can no longer be reasonably defined. The tail phase causes the greatest losses in the diode, since voltage is already applied to the diode. A snappy diode without tail current generates less switching losses in the diode but also high overvoltages during turn-off. The tail phase is less harmful to the IGBT, since the applied voltage has already decreased at this time.

Diode switching losses in Figure 2.3.17b are represented in the same scale as for the IGBT in Figure 2.3.17a. In application, they are low compared to the switching losses in the IGBT. For the overall power losses of both IGBT and diode, it is important to keep the peak reverse current low and to have the main part of the storage charge discharged during the tail phase. The trend towards increasingly faster switching - thus reducing the switching losses in the IGBT - results in ever increasing stresses on the diode. Depending on the type of application, it may be useful with regard to the total losses to switch more slowly than recommended in the datasheet ratings.

Switching losses largely depend on 4 parameters:

- The rate of rise of commutation current di/dt or the gate resistance of the switching IGBT (Figure 2.3.18 a): switching losses tend to fall in proportion to the increase in resistance; with a very small gate resistance, the existing stray inductance will limit di/dt. The range shown corresponds to a gate series resistor of 0.5 Ω up to 8.2 Ω.
- The blocking voltage (DC link voltage V_{CC}; Figure 2.3.18 b), which builds up in the component after turn-off. The dependency can be approximately calculated using an exponent of 0.6:

$$E_{rr}(V_{CC}) = E_{rr}(V_{ref})\left(\frac{V_{CC}}{V_{ref}}\right)^{0,6}$$

- Forward current I_F (Figure 2.3.19 a): The higher the current, the greater the losses. However, this dependency is not linear and can be approximated using an exponent between 0.5 and 0.6:

$$E_{rr}(I_F) = E_{rr}(I_{ref}) \left(\frac{I_F}{I_{ref}} \right)^{0,6}$$

- Junction temperature T_j (Figure 2.3.19 a): Switching losses initially rise linear to the temperature. Only above 125°C does the increase become slightly disproportionate. Using a temperature coefficient of 0.0055…0.0065, the switching losses can be calculated as a function of the temperature.

$$E_{rr}(T_j) = E_{rr}(T_{ref}) \cdot (1 + TC_{Err} \cdot (T_j - T_{ref}))$$

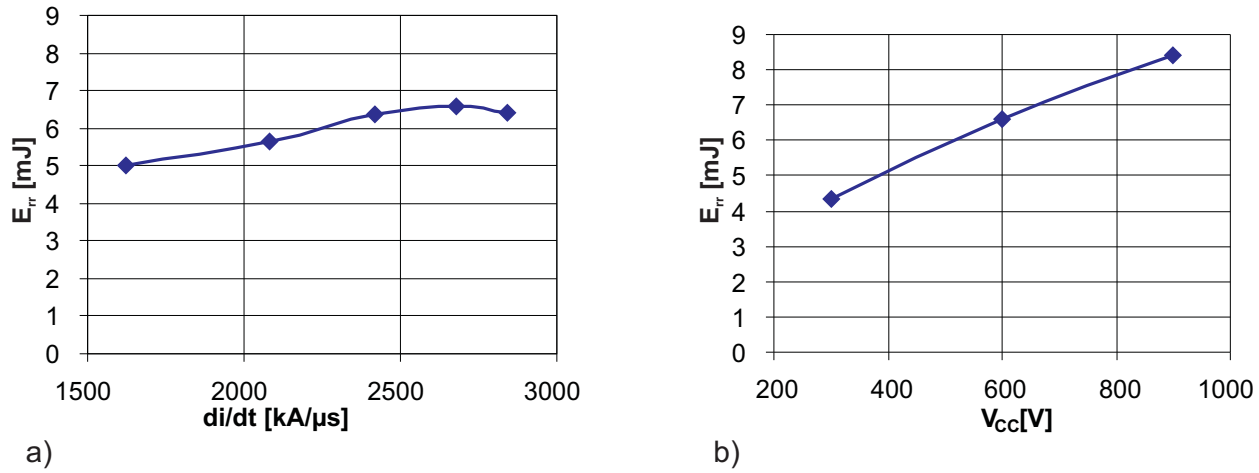


Figure 2.3.18 Dependencies of 100 A/1200 V CAL diode switching losses;
a) on di/dt (@100 A, 600 V, 150 °C);
b) on the DC link voltage (@100 A, R_G=1 Ω → 2700 A/µs, 150 °C)

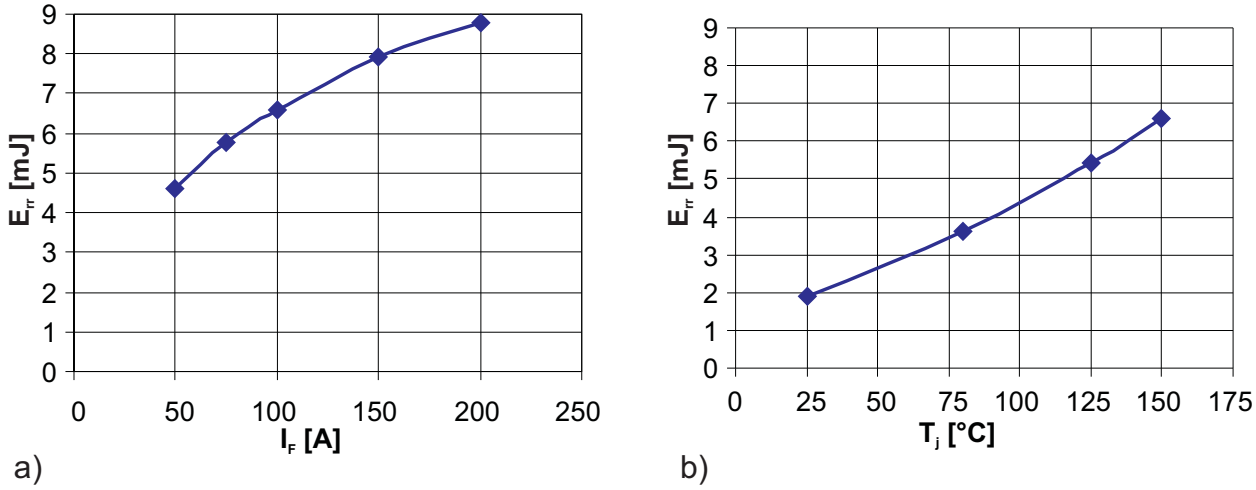


Figure 2.3.19 Dependencies of switching losses of a 100 A/1200 V CAL diode;
a) on I_F (R_G=1 Ω, 600 V, 150 °C);
b) on junction temperature (100 A, 600 V, R_G=1 Ω)

2.3.3.3 Dynamic ruggedness

Apart from soft switching behaviour, an equally important requirement for freewheeling diodes for a voltage of 1000 V and above is dynamic ruggedness. Figure 2.3.17b shows that almost the entire DC link voltage is taken up by the diode while it is still conducting a substantial tail current. If the IGBT is switched very steeply (low gate resistance R_G) the reverse peak current and tail current will rise, at the same time causing a faster decrease in V_{CE} at the IGBT, which is then present in the diode with a correspondingly higher dv/dt. The electric field can only spread within the depleted area ($t_2 – t_4$ in Figure 2.3.11 and Figure 2.3.12); here, extreme field intensities occur and avalanche breakdown in the semiconductor at voltages far below reverse voltage level (dynamic avalanche) are inevitable. Dynamic ruggedness is the ability of a diode to manage high rates of rise of commutation current di/dt and a high DC link voltage at the same time. An alternative to dynamic ruggedness would be to limit the di/dt of IGBT or to limit the maximum peak reverse recovery current of the diode, which amounts to the same. This will inevitably result in higher switching losses.

While the space charge region spreads, the empty part of the n^- region will have a current I_R flowing through it. Electrons and holes are generated at the pn-junction by dynamic avalanche. The holes move through the highly doped p-region. The electrons, however, move though the n--region, resulting in the following effective doping:

$$N_{eff} = N_D + p - n_{av}$$

Here, n_{av} is the density of the electrons generated by dynamic avalanche, moving from the pn-junction through the space charge region. The electrons partly compensate the hole density, thus counteracting the avalanche effect. With small forward currents, the reverse current will also decrease and consequently the hole density p. However, since the switching components have a higher dv/dt at low currents, the stress caused by dynamic avalanche may be higher, especially for small currents.

2.4 Power MOSFET and IGBT

2.4.1 Structure and functional principle

Power MOSFET and IGBT chips have up to 250,000 cells per mm^2 (50 V power MOSFET) or 50,000 cells per mm^2 (1200 V IGBT) with a chip surface of 0.1 to 1.5 cm^2 (Figure 2.4.1).

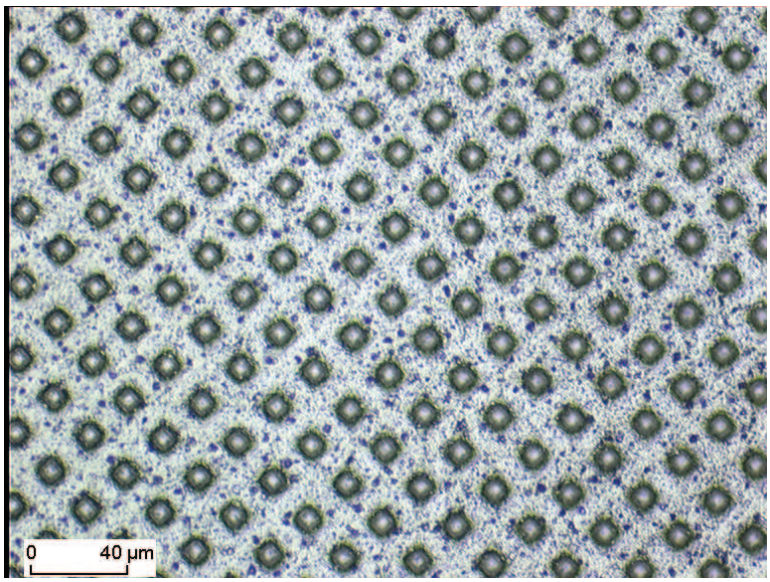


Figure 2.4.1 Cell structure (emitter metallisation) of a Trench IGBT3

For transistors based on the same technological concepts, the control regions of MOSFET and IGBT cells have an almost identical structure. As shown in Figure 2.4.2 and Figure 2.4.3, p-charged wells are embedded in an n^--region which has to take up the space charge region during off-state. Their doping is low in the edge areas (p^-) and high in the centre (p^+). These wells contain layers made of n^+ silicon which are connected to the aluminium-metallised source (MOSFET) or emitter (IGBT) electrode. A control region (gate) is embedded in a thin SiO_2 insulation layer above the n^+ regions, consisting of n^+ polysilicon, for example.

In power electronics, the vertical structures depicted in Figure 2.4.2 and Figure 2.4.3 are used. Here, the load current of each cell is conducted vertically through the chip outside the channel. This manual only describes transistors of the *n-channel enhancement type* used almost exclusively), where a *conducting channel with electrons as charge carriers* (majority carrier) is formed in a *p-conducting silicon material* when a *positive control voltage* is applied. Without a control voltage, these components would block (self-blocking transistors).
Other kinds of power MOSFET are *p-channel enhancement types* (negative control voltage in p-silicon influencing a channel containing positive charge carriers /self-blocking) and *n-channel and p-channel depletion types (depletion transistors)* which are in on-state without any control voltage (self-conducting). In these transistors, the control voltage generates a space charge zone that cuts off the channel and interrupts the main current flow. These types are used in some applications; these will not, however, be discussed in more detail in this manual.

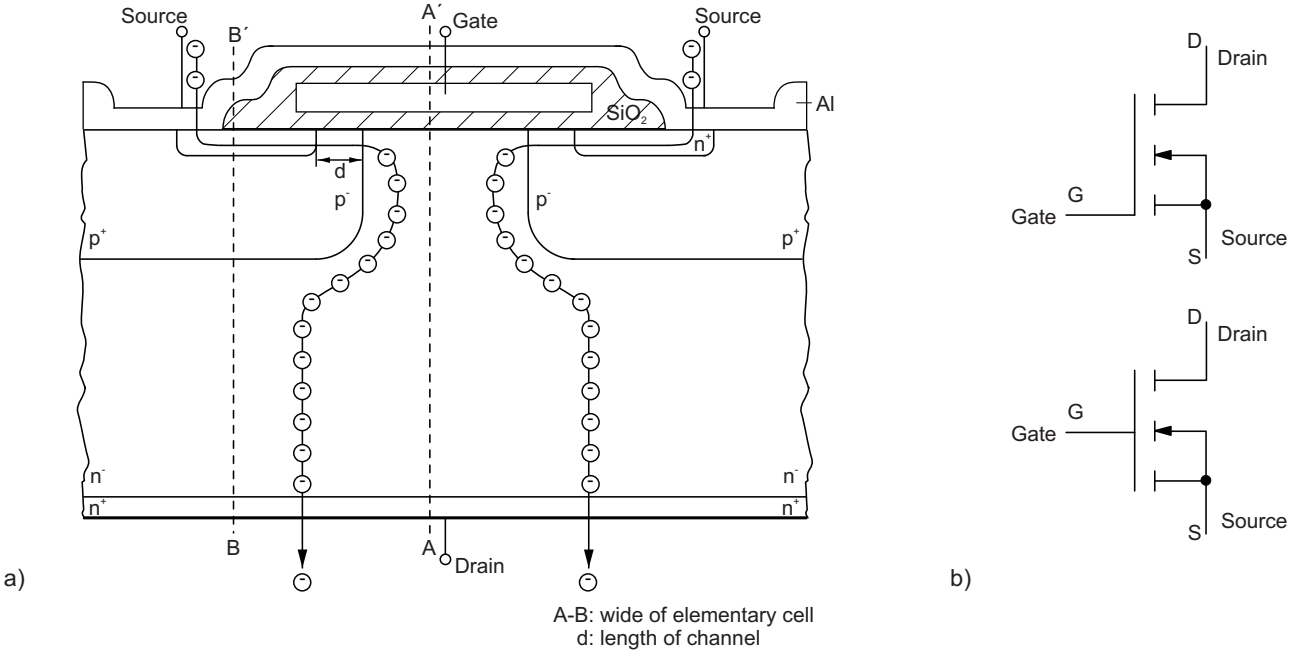


Figure 2.4.2 Power MOSFET with vertical structure and planar gate; a) Charge carrier flow in on-state; b) Circuit symbols

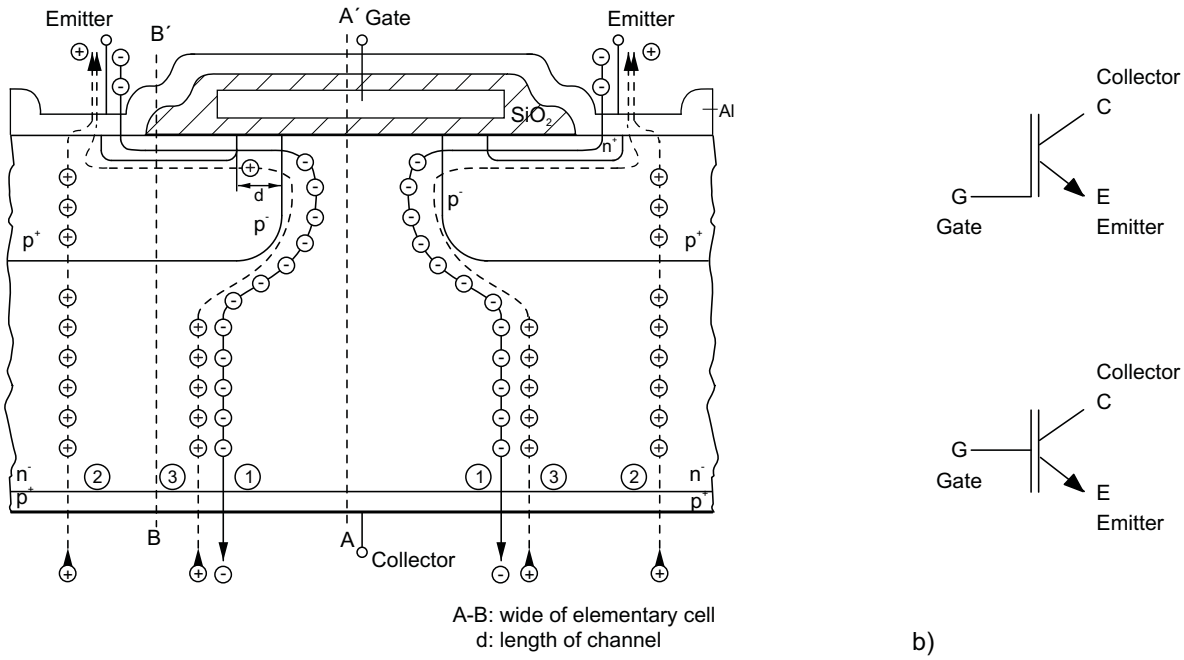


Figure 2.4.3 IGBT with vertical structure and planar gate;
a) Charge carrier flow in on-state;
b) Circuit symbols

The huge differences in properties found in power MOSFET and IGBT result from the different structures used with regard to the third electrode (MOSFET: drain / IGBT: collector), resulting in different functional principles. When a sufficiently high positive control voltage is applied between gate and source (MOSFET), or emitter (IGBT), an n-conducting channel is formed within the p-region below the gate terminal. This channel conducts electrons from the source or emitter through the n^--drift area to the bottom terminal, where they deplete the charge carrier region. In power MOSFET, these electrons alone conduct the main current (drain current). Since they are majority carriers in the n^- drift area, the highly resistive n^- region will not be flooded by bipolar charge carriers; MOSFET are unipolar components.

While the structure of an IGBT largely corresponds to that of a power MOSFET up to the n^--region, the underside of the IGBT consists of a p^+-conducting area carrying the collector terminal. The effect of this additional n^+ field stop layer located (in most IGBT concepts) between the n^-- and p^+ region will be discussed in more detail later.

As soon as electrons enter the p^+ area of the collector region, positive charge carriers (holes) will be injected from the p^+ area to the n^- area. The injected holes will flow directly from the drift area to the emitter-p-contact, as well as laterally below the channel and the n^+well to the emitter. Thus, the n^--drift area is flooded with holes (minority carriers); this charge carrier enhancement conducts the biggest part of the main current (collector current). The main current depletes the charge carrier region, which results a decline in collector-emitter voltage. This means that, unlike MOSFET, IGBT are bipolar components.

The flood of minority carriers in the high-resistance n^- region causes a lower on-state voltage of the IGBT than in the case of the power MOSFET. For this reason, IGBT can be designed for much higher voltages and currents while having similar chip areas to MOSFET. On the other hand, the minority carriers must be dissipated from the n^- drift area again during turn-off, or they have to recombine there (switching losses).

2.4.2 IGBT

The p-storage charges Q^s, which recombine during turn-off in the n^- region, have an almost linear characteristic in the low-current range and rise in proportion to the forward current in the rated current and overcurrent range in accordance with a square root function [14].

$Qs \sim I^{0.8...1}$ in the lower on-state current range
$Qs \sim I^{0.5}$ in the rated and overcurrent range
$Qs \sim V_{(BR)CE}^{2...2.7}$.

Storage charge enhancement and depletion processes cause switching losses, storage effects (storage time) and a collector "tail current" during turn-off. In practice, IGBT properties are strongly influenced by the parasitic elements in the real IGBT structure. To understand these real properties and possible failure mechanisms, it is therefore indispensable to look at the equivalent circuit diagram of the IGBT (Figure 2.4.4).

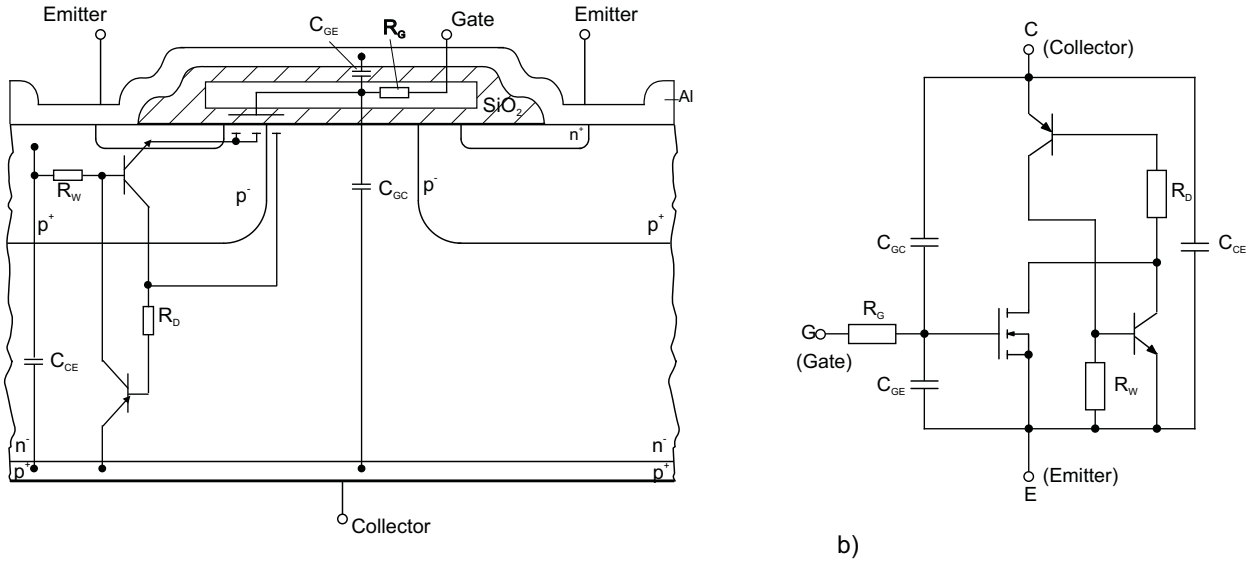


Figure 2.4.4 IGBT cell (NPT structure, planar gate) including the key parasitic elements;
a) Parasitic elements in the cellular structure;
b) Equivalent circuit diagram with parasitic elements

The physical causes and designations of the parasitic capacitances and resistances shown in Figure 2.4.4 are evident in Table 2.4.1.

Symbol	Designation	Physical Description
C_{GE}	Gate-emitter capacitance	Overlapping gate and source metallisation; dependent on gate-emitter voltage; independent of collector-emitter voltage
C_{CE}	Collector-emitter capacitance	Junction capacitance between n^- drift area and p-well; dependent on cell surface, breakdown voltage and collector-emitter voltage
G_{GC}	Gate-collector-capacitance	Miller capacitance; generated by overlapping of gate and n^--drift area
R_G	Internal gate resistance	Polysilicon gate resistance; additional series resistors are often needed in modules with several transistor chips to minimise oscillations between chips
R_D	Drift resistance	Resistance of the n^- region (base resistance of the PNP transistor)
R_W	Lateral resistance of the p-well	Base-emitter resistance of the parasitic bipolar NPN transistor

Table 2.4.1 Physical causes and designations of IGBT parasitic elements

Apart from internal capacitances and resistances, the equivalent circuit diagram of the IGBT also shows an "ideal MOSFET", an NPN transistor at the gate side: n^+ emitter region (emitter) / p^+ well (base) / n-drift area (collector) with the lateral resistance of the p^+ well below the emitters as base-emitter resistance R_W and - in the sequence p^+-collector area (emitter) / n-drift area (base) / p^+ well (collector) - a PNP transistor, which, in combination with the NPN transistor, forms a thyristor circuit. This parasitic thyristor will latch up as soon as the following latch-up condition is met:

$$M \cdot (\alpha_{npn} + \alpha_{pnp}) = 1 \quad \text{where} \quad \alpha_{pnp}, \alpha_{npn} = \alpha_T \cdot \gamma_E$$

M: multiplication factor;
α_{npn}, α_{pnp}: current amplification in the individual transistors in the base circuit;
α_T: base transport factor;
γ_E: emitter efficiency

This would lead to a loss of IGBT controllability and, consequently, to its destruction. In principle, this can happen during stationary operation (when a critical current density is exceeded, which decreases as the chip temperature rises) or even during turn-off (dynamic latch-up due to the increased hole current compared to stationary on-state operation). Appropriate design measures will reliably prevent latch-up in all modern IGBT types under any permissible static and dynamic operating conditions; latch-up would only happen during turn-off if the rated current density was multiplied in value.

Suitable design measures are, for example, the reduction of the base-emitter resistance R_W of the NPN subtransistor by way of high doping of the p^+ well directly below the n-emitters and shortening of the n-emitter length to such an extent that the threshold voltage of the base-emitter diode of the NPN transistor cannot be reached under any permissible operating condition. Furthermore, the hole current (NPN transistor base current) is kept at a minimum by setting a low-current amplification in the PNP transistor. What must be noted here, however, is that a compromise has to be found between switching behaviour and ruggedness, on the one hand, and on-state properties, on the other.

2.4.2.1 Static behaviour

Figure 2.4.5 shows the output characteristics of an IGBT with an anti-parallel freewheeling diode and its transfer characteristic.

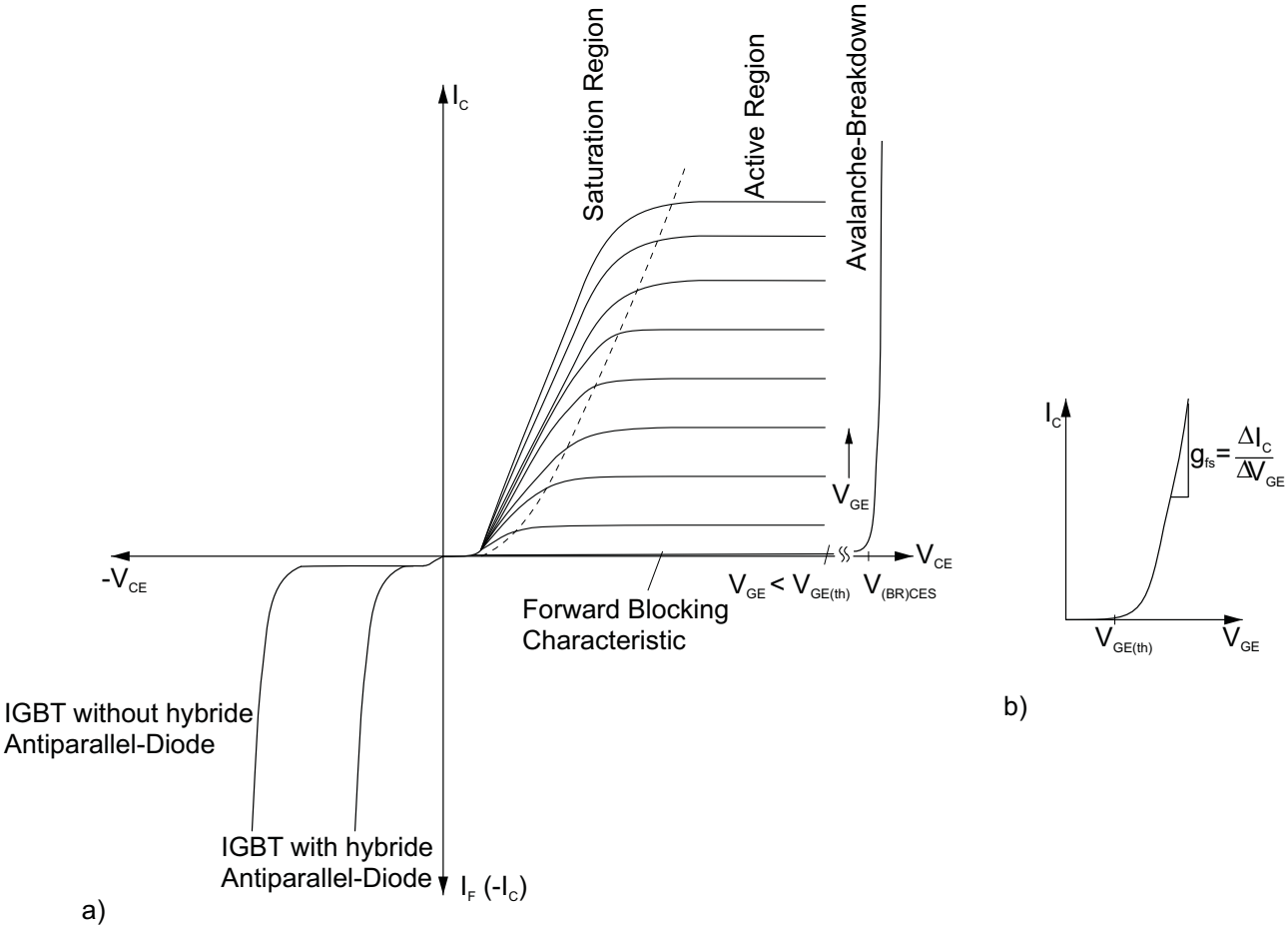


Figure 2.4.5 a) Output characteristics of an IGBT (n-channel enhancement type);
b) Transfer characteristic $I_C = f(V_{GE})$

The stationary switching states are as follows:

Forward off-state and avalanche breakdown

If a positive collector-emitter voltage V_{CE} and a gate-emitter voltage V_{GE} is applied below the gate-emitter threshold voltage level $V_{GE(th)}$, only a very small collector-emitter cut-off current I_{CES} flows between the collector and emitter terminal.

When V_{CE} rises, I_{CES} increases slightly at first. Above a specified, maximum rated collector-emitter voltage V_{CES}, there will be an avalanche breakdown of the PIN junction p^+-well / n-drift area / n^+-epitaxy layer (collector-emitter breakdown voltage $V_{(BR)CES}$). $V_{(BR)CES}$ roughly corresponds to the breakdown voltage V_{CER} of the bipolar PNP transistor in the IGBT structure. The multiplication current generated during avalanche breakdown in the collector-base diode can lead to IGBT destruction as a result of bipolar transistor turn-on. Base and emitter regions are, however, almost shorted by emitter metallisation; between them there is nothing but the lateral resistance of the p^+-well.

On-state (1st quadrant)

The forward on-state at a positive collector-emitter voltage V_{CE} and positive collector current I_C comprises two characteristic curve areas:

- Active region

With a gate-emitter voltage V_{GE} that hardly exceeds the gate-emitter threshold voltage $V_{GE(th)}$, a relatively high voltage share will be depleted through the channel owing to current saturation (horizontal part of the output characteristics). The collector current I_C is controlled by V_{GE}.

As a measure for the transfer behaviour as described in Figure 2.4.5b) the *forward transconductance* g_{fs} is defined as

$g_{fs} = \Delta I_C/\Delta V_{GE} = I_C/(V_{GE}-V_{GE(th)})$.

Forward transconductance rises in proportion to the collector current I_C and the collector-emitter voltage V_{CE}, and falls as the chip temperature increases. In the switching mode that is exclusively permissible for power modules working with several IGBT chips connected in parallel, the active region is only run through during turn-on and turn-off. Stationary module operation in the active region is not permissible, because $V_{GE(th)}$ falls when the temperature rises, meaning that even small differences between the individual chips may cause thermal instability.

- Saturation region

The saturation region, which corresponds to ON-state during switching operations (steep part of the output characteristics) has been reached when I_C is solely determined by the outer circuit. The on-state behaviour is charaterised by the residual voltage $V_{CE(sat)}$ (collector-emitter saturation voltage) of the IGBT. Flooding the n^- drift area with minority carriers causes the saturation voltage of an IGBT - from a certain reverse voltage level on - to be far lower than the on-state voltage of a comparable MOSFET. In the majority of modern IGBT structures, $V_{CE(sat)}$ rises in proportion to the temperature; only for IGBT designed according to the PT concept will $V_{CE(sat)}$ decline in the rated current range as the temperature increases.

Inverse operation (3rd quadrant)

In inverse operation, the pn-junction of the IGBT at the collector side is poled in reverse direction. The permissible blocking voltage of this PIN diode is no more than a couple of decavolts owing to various design conditions and the shaping of the marginal regions. Today, reverse-blocking IGBT modules are therefore equipped with fast series-connected diodes, whereas reverse-conducting IGBT modules used in standard applications are equipped with fast, anti-parallel diodes (inverse diodes). Thus, the on-state features of IGBT modules in inverse operation exclusively result from the properties of these hybrid inverse diodes. Chapter 2.4.2.3 contains information on the latest developments in reverse-conducting IGBT chips.

2.4.2.2 Switching behaviour

The switching behaviour of IGBT power modules is determined by their structural, internal capacitances and the internal and outer resistances. Contrary to the ideal of powerless voltage control via the MOS-gate, frequency-dependent control power is required owing to the recharge currents of the internal capacitances which are needed for switching.

Furthermore, the commutation processes are affected by the parasitic connection inductances present in the components and connections and generated by connecting transistor chips in power modules; they induce transient overvoltages and may cause oscillations due to the circuit and transistor capacitances, cf. chapter 5.

The switching behaviour of IGBT can be described as resulting from the transistor's internal capacitances and resistances:

When the IGBT is turned off, C_{GC} is low and approximately equal to C_{CE}. During on-state, C_{GC} will increase rapidly as soon as the gate-emitter voltage has exceeded the collector-emitter voltage; this rapid increase is due to inversion in the enhancement layer below the gate regions.

The datasheets normally list the input and output capacitances C_{ies}, C_{res} and C_{oes} (low-signal capacitances) of the transistor in OFF state (see Table 2.4.2).

	IGBT
Input capacitance	$C_{ies} = C_{GE} + C_{GC}$
Reverse transfer capacitance (Miller capacitance)	$C_{res} = C_{GC}$
Output capacitance	$C_{oes} = C_{GC} + C_{CE}$

Table 2.4.2 Definition of the low-signal capacitances of an IGBT

To calculate the switching behaviour, this data can only be utilised to a very limited extent, since the input and reverse transfer capacitance ($V_{CE} < V_{GE}$) will increase enormously in a fully switched transistor, for example. In order to determine switching times and the gate charge by approximation, the gate charge diagram included in the datasheets, as shown in Figure 2.4.7, is used (for explanations please refer to chapter 3.3.3).
Below, the IGBT switching behaviour when"hard" switching ohmic-inductive loads with continuous load current - i.e. the time constant of the load L/R is far greater than the cycle 1/f of the switching frequency - is looked at from a qualitative point of view.

Figure 2.4.6a) shows the typical waveforms of collector current and collector-emitter voltage as a function of the gate control voltage V_{GE}, Figure 2.4.6b) shows the typical waveform of the operating point for hard turn-on and turn-off as a graph $i_c = f(v_{CE})$. Since the behaviour of power MOSFET deviates from this in very few respects only, Figure 2.4.6b) refers to both components – the specifics of MOSFET are explained in chapter 2.4.3.2.

Typical of "**hard switching**" is that during turn-on and turn-off, both transistor current and transistor voltage are high for a short time; this is due to the fact that a freewheeling diode in the load circuit prevents the current from cutting off as a result of the load inductance:
- When the transistor is turned on, the freewheeling diode can only pick up reverse recovery voltage (turn off) once the load current has completely commutated to the transistor. The collector current therefore has to reach the load current level before the collector-emitter voltage can fall to the on-state value.
- When the transistor is turned off, the freewheeling diode can only take up the load current (turn on) once it has reached on-state voltage polarity. To this end, the collector-emitter voltage has to exceed the commutation voltage level before the collector current can drop to the cut-off current value.

In contrast to thyristors of any type, transistors can handle such modes of operation without passive snubber circuits thanks to the "dynamic" junction which is generated in the drift area during switching operations.

In a transistor, however, a considerable amount of switching energy is dissipated:

$$E_{on}, E_{off} = \int_{t_{on},\, t_{off}} u \cdot i \, dt$$

By means of passive snubber circuit (which are rarely used nowadays), the operating point curve can be brought closer to the axes. Switching losses are "shifted" from the transistor to the snubber, causing the total efficiency to decrease in most cases.
Since the "widest" possible operating point waveform is influenced by many (non-ideal) effects in the transistor and not just by current/voltage markers and switching time, the SOA (**S**afe **O**perating **A**rea) is given in the datasheets for different operating conditions (cf. chapter 3.3.4).

Apart from the non-ideal properties of transistors and diodes, passive circuit components also influence switching losses and operating point waveforms to a high degree. Their impact will be discussed in chapter 5 in more detail.

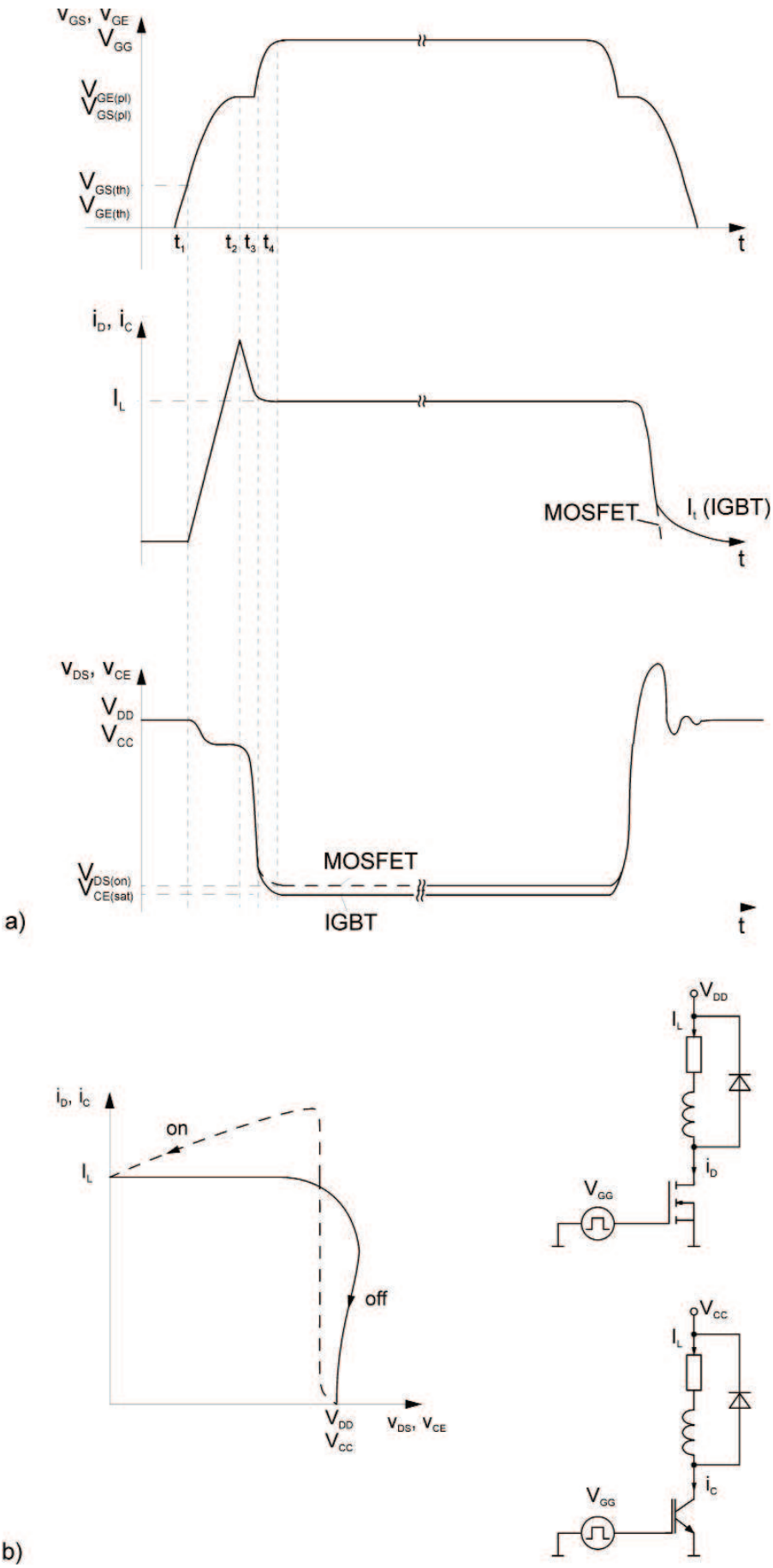


Figure 2.4.6 Typical "hard" switching behaviour of power MOSFET and IGBT (ohmic-inductive load with freewheeling circuit); a) Current and voltage waveforms; b) Operating point waveforms and measurement circuit

As shown in Figure 2.4.6, the collector-emitter voltage declines within some 10 ns to a value that is equivalent to the voltage drop over the n^--drift area when the IGBT is turned on. Then the n^--area is flooded by positive charge carriers from the p-collector region; after a period ranging from several hundred ns to some µs, the dynamic saturation voltage $V_{CE(sat)dyn}$ will have dropped to the value of the on-state voltage $V_{CE(sat)}$.

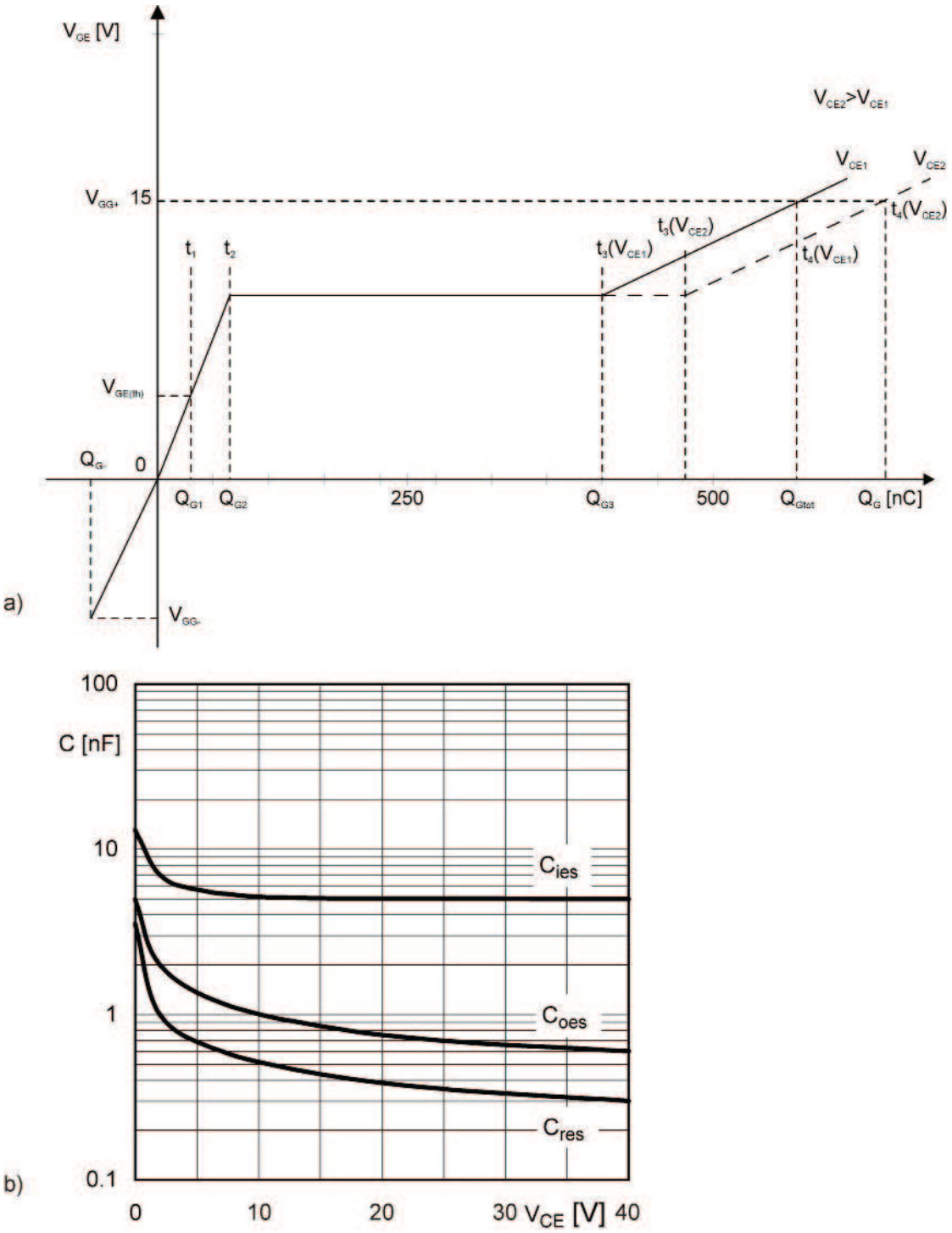


Figure 2.4.7 a) Gate charge diagram of an IGBT; b) IGBT low-signal capacitances

Turn-on: switching interval 0...t_1 (blocked transistor)

The gate current i_G starts flowing when the control voltage is applied.
At first, i_G charges only the gate capacitance C_{GE} until it reaches the charge quantity Q_{G1}; the gate-emitter voltage V_{GE} rises in line with the time constant determined by the input capacitance of the IGBT and the gate resistance. Since V_{GE} is still below the threshold voltage $V_{GE(th)}$, no collector current will flow during this period.

Turn-on: switching interval t_1...t_2 (collector current rise)

After the threshold voltage $V_{GE(th)}$ (t_1) has been reached, the collector current will start to rise. In the same way, V_{GE}, which is coupled to the collector current in the active IGBT operating area by means of the transconductance g_{fs} with $I_C = g_{fs} * V_{GE}$, increases until it reaches $V_{GE1} = I_C/g_{fs}$ (time t_2). Since the freewheeling diode can only block the current at t_2, V_{CE} does not drop significantly before t_2. At $t = t_2$, charge Q_{G2} will have flowed into the gate.

During this time interval, most of the turn-off losses are generated in the IGBT. This is because, as long as i_C is below the load current I_L, a certain share of I_L must continue to flow through the freewheeling diode. This is why, the collector-emitter voltage v_{CE} cannot drop noticeably below the operating voltage V_{CC}. The difference between V_{CC} and V_{CE} outlined in Figure 2.4.6 is mainly caused by transient voltage drops across the parasitic inductances of the commutation circuit.

Turn-on: switching interval t_2...t_3 (transistor fully switched on in the active operating area, flat phase)

When the freewheeling diode is turned off, V_{CE} will almost drop to its on-state value $V_{CE(sat)}$ by t_3. Between t_2 and t_3, the collector current and gate-emitter voltage are still coupled through the transconductance; v_{GE} therefore remains roughly constant. While v_{CE} drops, the gate current i_G recharges the Miller capacitance C_{CG} with the charge (Q_{G3}-Q_{G2}). By $t = t_3$, an amount of charge equal to Q_{G3} will have flowed into the gate.

After the entire load current I_L has been commutated to the IGBT, the freewheeling diode will start to block. Owing to the reverse recovery time of the freewheeling diode, however, the IGBT collector current i_C initially continues to rise above I_L during turn-off of the freewheeling diode by a value equal to I_{RRM} and dissipates the reverse recovery charge Q_{rr} of the freewheeling diode (cf. Definitions on switching times and explanations on characteristics I_{RRM}, Q_{rr} and E_{rr} relating to inverse diodes, as provided in chapter 3.3).

Turn-on: switching interval t_3...t_4 (saturation area)

At t_3, the IGBT is now turned on, its operating point has passed through the active operating area and has reached the border of the saturation area. V_{GE} and I_C are no longer coupled by g_{fs}. The charge quantity (Q_{Gtot} -Q_{G3}) now supplied to the gate causes the further rise in V_{GE} up to the level of the gate control voltage V_{GG}. Immediately after its steep drop, the collector-emitter voltage v_{CE} has not yet reached its static on-state value V_{CEsat}. Depending on V_{GG} and I_C, this value will be reached as soon as the n^- drift area starts to be flooded after several hundred nanoseconds or several microseconds. This "dynamic saturation phase $V_{CE(sat)dyn}$ = f(t)" s the period required for (bipolar) minority charge carrier flooding (conductivity modulation) of the wide n^--region of the IGBT.

Turn-off

During the turn-off operation, the processes described above are reversed: charge Q_{Gtot} must now be dissipated from the gate with the aid of the gate current. In this process, the internal capacitances are recharged to such an extent that the charge carrier influence in the channel area will vanish. This helps to quickly reduce any neutrality interference in this area; the collector current drops steeply to begin with. After the emitter current has stopped, however, many p-charge carriers generated by injection from the IGBT collector area are still present in the n-drift area. They must now recombine or be reduced to zero by backward injection, which causes a more or less strong collector tail current. Since this current tail will only decline within µs after the collector-emitter voltage has started to rise, its shape and length significantly determine the turn-off losses of the IGBT during hard switching.

Overshooting of v_{CE} over V_{CC}, which was indicated in Figure 2.4.6, results mainly from the parasitic inductances in the commutation circuit. It grows in proportion to the increasing turn-off speed–di_c/dt of the IGBT. The more the transistor application deviates from the "ideal" case of a "hard switch" discussed here (e.g. owing to parasitic components in the commutation circuit), the more "blurry" the step-form of the gate-emitter curve becomes. The intervals "decoupled" during hard switching will then merge more and more, and any description of the switching behaviour becomes more complex.

2.4.2.3 IGBT – Concepts and new directions of development

Since IGBT were invented, their basic principles have been utilised in different concepts. IGBT chips have therefore been further developed in separate ways, pursuing the objectives and taking the directions outlined for chip technology in chapter 2.1. In order to both reduce costs by reducing (shrinking) chip area and to get even closer to the physical limits, three main paths have been followed in the further development of IGBT chips.

- Finer cell structure / chip area reduction / increase in max. current density
- Reduced chip thickness
- Increase in permissible chip temperature.

Every IGBT concept must – adapted to its main applications – achieve a balance between various conflicting component properties, e.g. as shown in the example in Figure 2.4.8:

- a) Between on-state voltage $V_{CE(sat)}$ and turn-off power loss E_{off},
- b) Between on-state voltage $V_{CE(sat)}$ and short-circuit behaviour (SCSOA, cf. chapter 3.3.4).

The limits for a) are pushed further in the latest IGBT concepts, e.g. SPT+ (ABB), IGBT4 (Infineon) and CSTBT (Mitsubishi), by increasing the concentration of free charge carriers among the n-emitter cells. One negative consequence, however, is often the very steep decline in collector current during turn-off with the resultant side-effects as regards EMC, for instance. The trade off in b) is improved by a continuous reduction in chip thickness and the introduction of weakly doped field stop layers. The IGBT cell pitch has a crucial impact on its properties. This determines, among other things, the influence the MOS channel has on conductivity modulation.

Figure 2.4.8 [15] shows, using the example of a 1200 V IGBT in Trench-Gate technology, how $V_{CE(sat)}$ or collector current density $J_{C(sat)}$ depend on the cell pitch (distance between adjacent gate centres) for T_j = 125°C.

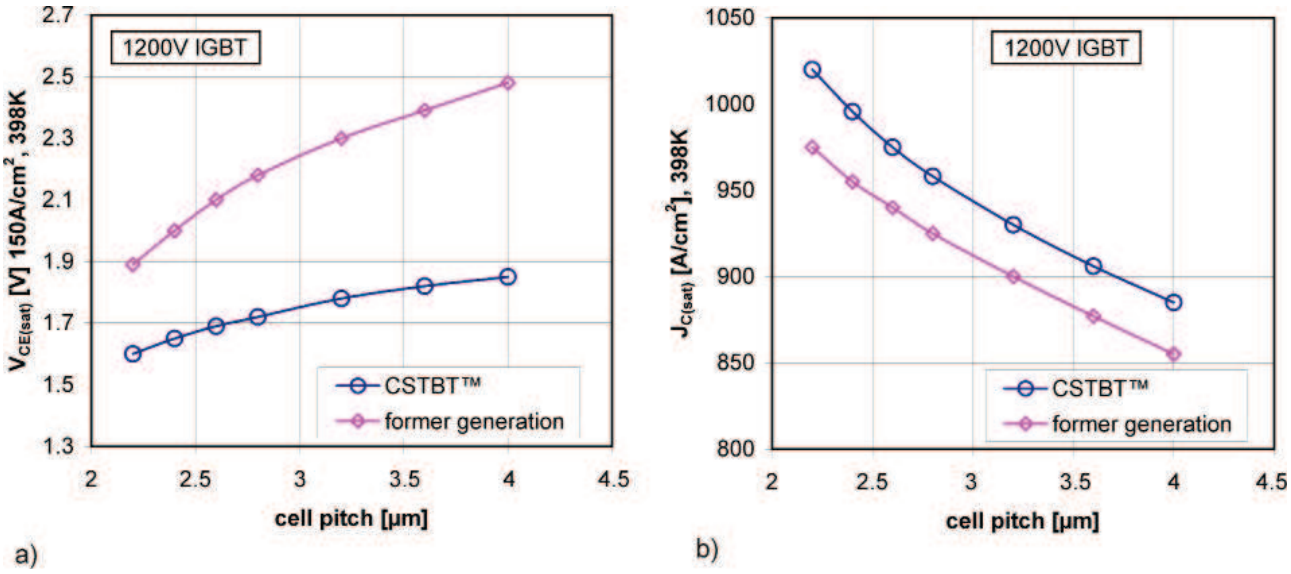


Figure 2.4.8 a) Dependency of the on-state voltage $V_{CE(sat)}$ of a 1200 V IGBT on the cell pitch for T_j = 125°C; b) Dependency of the collector current density $J_{C(sat)}$ of a 1200 V IGBT on the cell pitch for T_j = 125°C [15]

Figure 2.4.9 shows the development of chip size and on-state voltage for different component generations using 1200 V / 75 A IGBT chips from Infineon as an example.

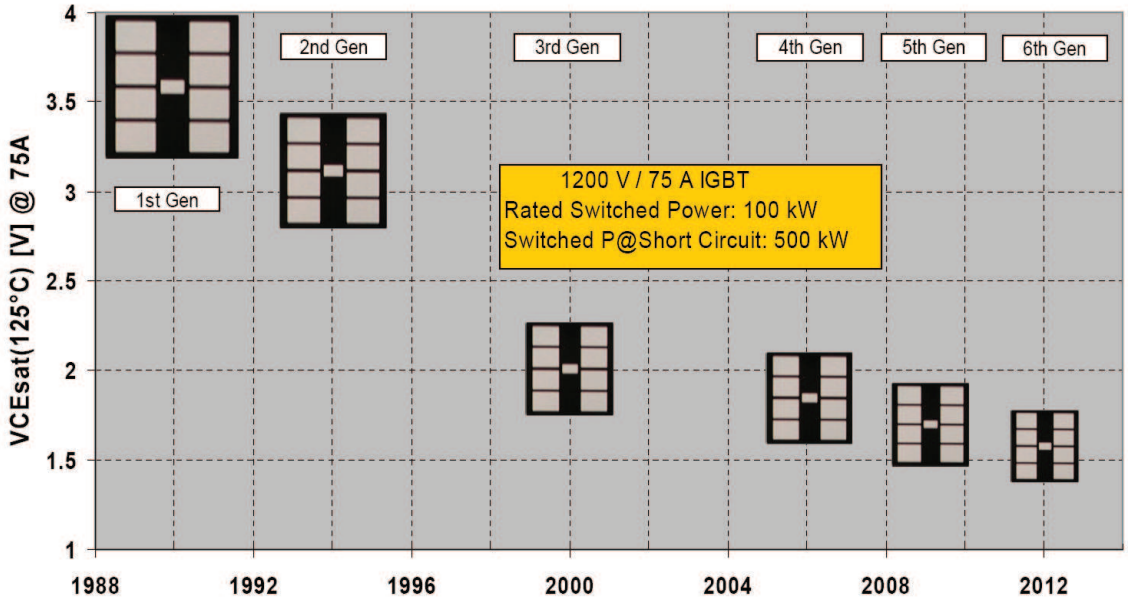


Figure 2.4.9 Development of chip size and on-state voltage of 1200 V / 75 A IGBT chips from Infineon [16]

To enable system costs (cooling, chip area) to be reduced, a crucial development target is to increase the permissible chip temperature. This was achieved by Infineon, for example, for IGBT up to 1700 V in the IGBT4 chip generation, raising the temperature from 150°C to 175°C; 200°C is planned for future IGBT generations. An increase in the IGBT operating temperature, however, means that the freewheeling diode (inverse diode), too, has to be suitable for this temperature; this is increasing the requirements that IGBT module packaging has to fulfil; cf. chapter 2.5.

The pictures below illustrate the most important IGBT concepts, which shall be briefly described below. Detailed explanations on the physical correlations are provided in [17], et al.

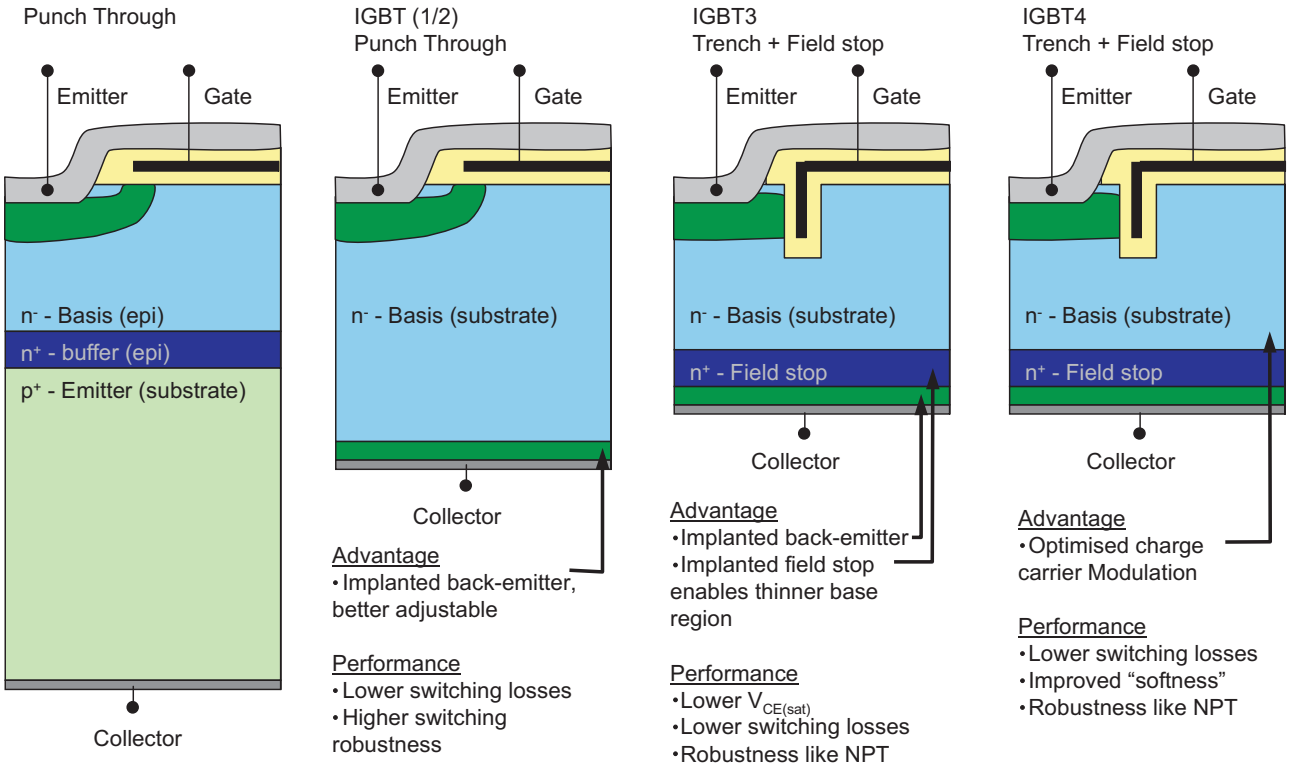


Figure 2.4.10 IGBT concepts, basic properties and off-state field intensity characteristics (acc. to [18])

PT concept

The first "**P**unch **T**hrough" (PT) concept, which is still used today as a result of continuous developments, uses a p^+-substrate as a base material , n^+ and n^- region being applied by means of epitaxy. Today, PT-IGBT can also have a trench-gate structure, as shown in Figure 2.4.10. In forward off-state, the space charge region comprises the entire n^--region. In order to keep the epitaxy layer as thin as possible even for high blocking voltages, the field at the end of the n^- drift area is reduced by a highly doped n^+ buffer region.

PT-IGBT have a high emitter efficiency for holes in the p^+ layer drifting into the n^- drift area, because the substrate is relatively thick and highly doped. The PNP current gain has to be reduced via the base transport factor (n^- drift area, n^+ buffer), which is achieved by reducing the charge carrier lifetime in the n^+ layer by increasing the recombination centres (e.g. gold doping or electron beam radiation). The hole current amounts to 40...45% of the total current.

NPT concept

The basis of "**N**on **P**unch **T**hrough" (NPT) IGBT, which was soon introduced by numerous manufacturers, is a thin, weakly doped n^- wafer; the collector-side p^+ zone is created by way of back implantation. Here, the n^- drift area is so wide that in forward off-state, the electric field is fully depleted in the n^- drift area up to the maximum permissible off-state voltage and cannot – in contrast to the PT concept – spread over the entire n^- region.

NPT-IGBT have a very thin collector-side p^+ emitter region, which results in a low emitter efficiency (γ_E = 0.5) of the PNP subtransistor - it is not necessary to lower the base transport factor by reducing charge carrier life time. The hole current amounts to 20...25% of the total current. In contrast to PT-IGBT, the saturation voltage of NPT-IGBT has a positive temperature coefficient, improving both the current symmetry between the cells in single chip and between chips connected in parallel. Switching times for hard switching are comparatively shorter and less dependent on temperature; overcurrents can be better cut off as a result of improved internal current limiting. On the date of creation of this paper, SEMIKRON was using the IGBT2 generation in older NPT-IGBT product series.

SPT- and SPT+ concept

The "**S**oft **P**unch **T**hrough" (SPT)-IGBT by ABB is a further development of the NPT concept. Here, too, the base material is a thin, weakly doped n^- wafer; the p^+ region at the collector is generated by back implantation. Here, an additional p^+region has been implanted as a field stop layer above the collector n^+ region. This reduces the thickness of the drift area – like the highly doped n^+ buffer layer in the PT-concept – by diminishing the electric field at the end of the n^- drift area in front of the collector region. Since this layer needn't curb the high emitter efficiency as is the case in the PT-IGBT, but has to reduce the field intensity only, it is less highly doped than the n^+ buffer of the PT-IGBT.

With the same forward off-state voltage, the thickness w_B of the n^- drift area can be significantly reduced in comparison to an NPT-IGBT; this also considerably cuts the on-state voltage (~ w_B) of the drift area. The positive temperature coefficient of the on-state voltage and the high component ruggedness are maintained. Figure 2.4.11 shows a cross-sectional view of an SPT-IGBT as well as a comparison of PT-NPT and SPT-IGBT chip thickness.

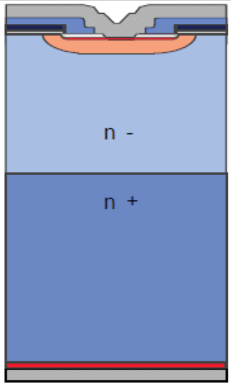
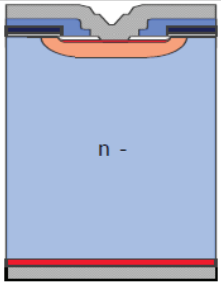
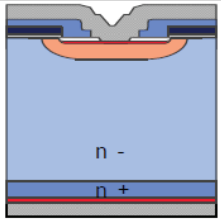
	Punch Through (PT)	Non - Punch Through (NPT)	Soft Punch Through (SPT)
Structure			
Features	Some devices show snappy turn-off at high V_{DC}	Positive temperature coefficient of on-state Extremely rugged	Positive temperature coefficient of on-state Extremely rugged Low losses
Material	Epitaxial	Float Zone	Float Zone

Figure 2.4.11 Structure of an SPT-IGBT compared with a PT and NPT IGBT [19]

The next development known as SPT+ (Figure 2.4.12) contains additional n-regions which are arranged in the n^- drift area around the p-channel areas, so that they can impede the drain of minority carriers in the on-state (hole barrier). This increases the charge carrier density in on-state in order to reduce the on-state voltage without significantly impairing the switching behaviour. At the n^-/n junction between drift area and additional n-region, a diffusion voltage of approximately 0.17 V will occur, preventing hole drain (hole barrier). In order to produce neutrality, electrons continue to be supplied from the channel area; the concentration of free charge carriers increases.

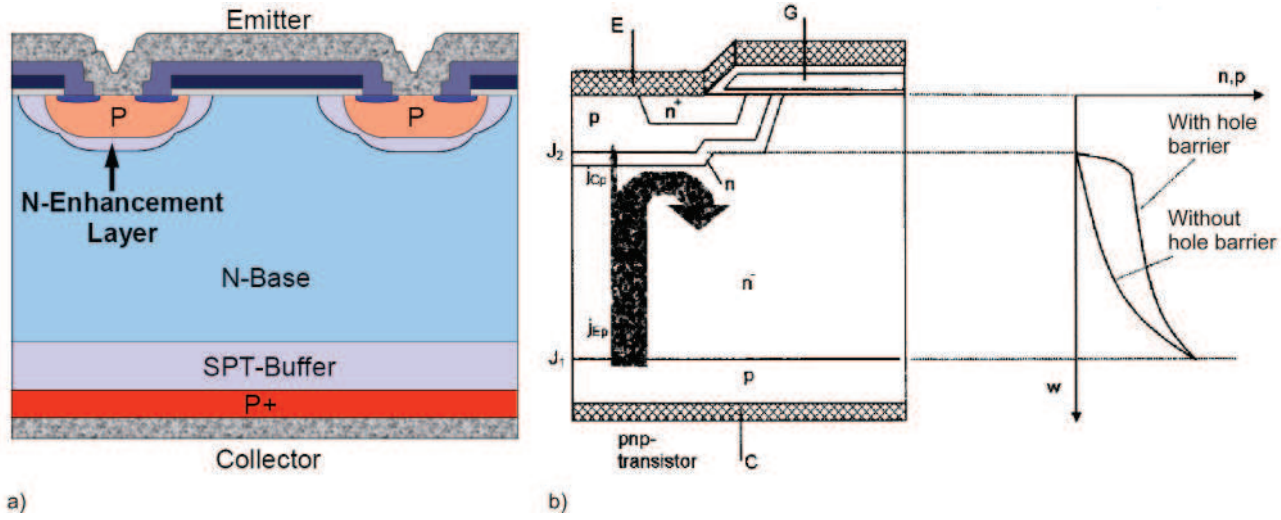


Figure 2.4.12 a) Structure of an SPT+ IGBT [20]; b) Effect of the hole barrier [17]

NPT concept with field stop layer and trench-gate structure

For these very common IGBT chips, a field stop layer was added to the NPT concept and the planar gate was replaced by a vertical trench-gate structure (Figure 2.4.10).

The basis here continues to be a thin, weakly doped n^- wafer into which an additional n^+ region has been implanted as a field stop layer on the back above the p^+ region of the collector. This reduces the thickness of the drift area – like the highly doped n^+ buffer layer in the PT-concept – by diminishing the electric field at the end of the n^- drift area in front of the collector region. Since this layer needn't curb the high emitter efficiency as is the case in the PT-IGBT, but has to reduce the field intensity only, it is less highly doped than the n^+ buffer of the PT-IGBT.

With the same forward off-state voltage, the thickness w_B of the n^- drift area can be significantly reduced in comparison to an NPT-IGBT; this also considerably cuts the on-state voltage (~ w_B) of the drift area. The positive temperature coefficient of the on-state voltage and the high component ruggedness are maintained. During turn-off, the tail current is initially somewhat higher than for an IGBT without field stop layer, but then it drops faster.

The vertical gate arrangement in the shape of a trench inside every IGBT cell allows for a vertical channel track in the p-well. Since the active silicon area is enlarged, better control of the channel cross-section is possible and thus a lower channel resistance can be obtained. For a given silicon area, the cell area can be reduced even further. This is why higher current densities, lower forward losses, a higher latch-up strength, lower switching losses and higher breakdown voltages can be obtained than in IGBT with planar gate structures.

In the IGBT4 generation from Infineon, the latest generation when this manual was written, cell pitch (i.e. the distance between the gates of neighbouring cells) was further reduced compared to its predecessor generation IGBT3, meaning that the cells were shrunk in size. Cell optimisation and chip thickness reduction has helped to improve the static and dynamic properties. However, smaller chips also mean a higher thermal contact resistance $R_{th(j-c)}$ or $R_{th(j-s)}$. The performance increase achieved in comparison to the IGBT3 therefore largely results from the higher permissible chip temperature of 175°C as compared with 150°C for IGBT3. Chips are now available with different settings between static and dynamic properties for different requirements:

- IGBT4 T4: particularly short switching times for modules with rated currents between 10 A and 300 A
- IGBT4 E4: low forward and switching losses for modules from 150 A to 1000 A
- IGBT4 P4: "soft" switching behaviour and particularly low forward losses for high-current IGBT modules above rated currents of 900 A.

At the time of publication, SEMIKRON was using IGBT3 chips in older product series and IGBT4 chips T4 and E4 in new product series.

CSTBT concept

A combination of the hole barrier above the drift zone and the trench-gate structure can be found in the **C**arrier **S**tored **T**rench Gate **B**ipolar **T**ransistor (CSTBT) from Mitsubishi (Figure 2.4.13). In these IGBT, which were formerly also known as **I**njection **E**nhanced **G**ated **T**ransistors (IEGT), the charge carrier injection among the n-emitters is increased by a "hole barrier", as described for the SPT^+ concept. The additional n-doped region is inside the trench-gate structure below the p-base areas. Positive charge carriers are enhanced below the hole barriers, which results in an effective resupply of electrons from the channel and thus a local increase in free charge carrier concentration.

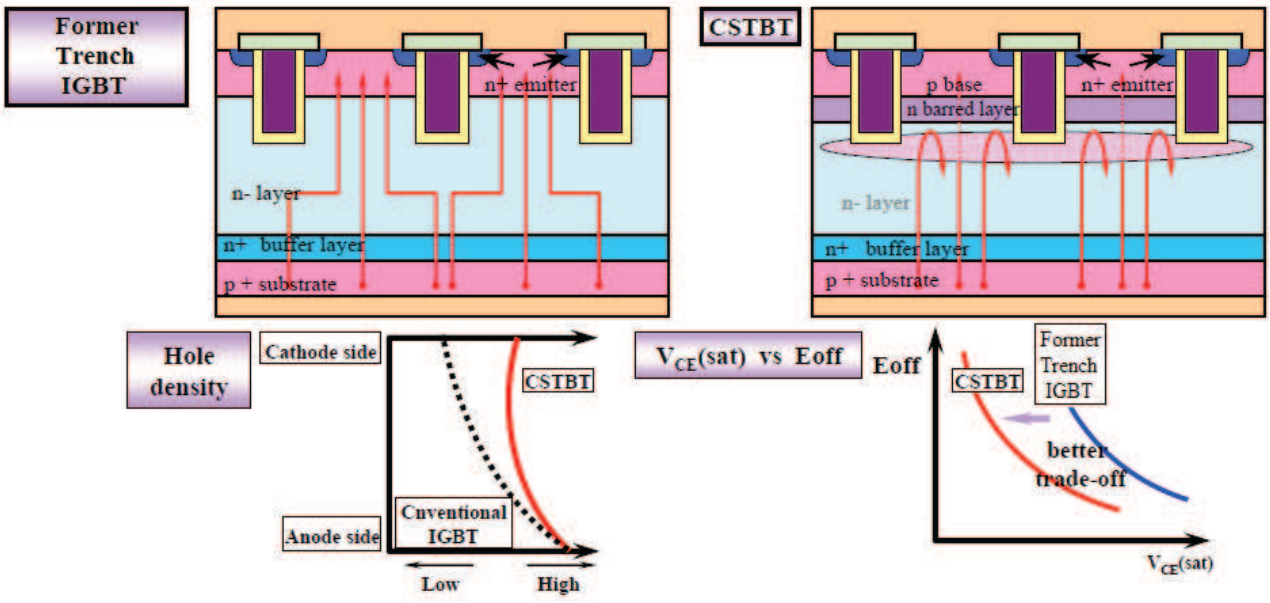


Figure 2.4.13 Basic structure, charge carrier distribution in on-state and trade-off between on-state voltage $V_{CE(sat)}$ and turn-off losses E_{off} in conventional Mitsubishi Trench IGBT and CSTBT [21]

In the meantime, Mitsubishi has applied the CSTBT concept to NPT technology as well, in order to be able to use less expensive thin wafers made of homogenous n material instead of epitaxy material.

Plugged cells

Rather than bonding individual trench cells, but short-circuiting the polysilicon in the gate area with the emitter metallisation instead (plugged cells) a further improvement in IGBT features can be achieved. Increasing the cell spacing and reducing the p-areas increases charge carrier concentration at the emitter, affecting the on-state voltage to a greater extent than the increased voltage drop over the channel area as a result [22]. Another advantage of plugged cells is the lower collector current in the event of a short circuit as compared to conventional Trench-IGBT.

RC-IGBT

Various manufacturers are developing reverse-conducting IGBT chips which can be loaded with the same current density in IGBT and diode mode. These are known as **R**everse **C**onducting IGBT (RC-IGBT). The aim is to reduce the use of anti-parallel freewheeling diode chips (hybrid-connected in the module), which has the following advantages:

- Improved performance per module area
- Increased overload capability (surge withstand strength)
- Improved parallel switching capability
- Increased $R_{th(j-c)}$ diode/IGBT ratio
- Reduction in temperature ripples per chip
- Improved flexibility for optimal thermal properties in power module

Figure 2.4.14 shows the basic structure of an RC-IGBT using the SPT concept from ABB. In its basic structure, n^- shorts have been integrated into the p^+ collector region. This enables the reverse conductivity of the integrated MOSFET to be used as an inverse diode.

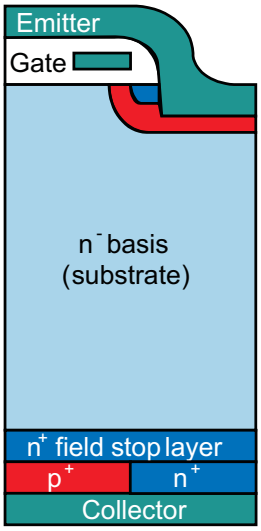


Figure 2.4.14 Structure of an RC-IGBT from ABB [23]

Hole injection from the p^+ collector region into the IGBT section also has to be performed when voltages and currents are low. Various structural measures help to attain low turn-off losses and soft recovery behaviour in the diode across the entire temperature range; IGBT latch-up is prevented. For this purpose, it is necessary to set very precise doping profiles for the p-emitter regions and the p^+/n^+ collector regions. The cells are thus not designed with highly doped p^+ regions but a fine structure of p-regions in order to obtain a lower injection efficiency. Local control of the p-charge carriers by means of implantation or proton irradiation allows for diode turn-off losses to be reduced without affecting the blocking voltage and the IGBT losses too much. Another way of reducing diode turn-off losses is to introduce a MOS-controlled diode (**B**imode **I**nsulated **G**ate **T**ransistor BIGT). Nowadays, RC-IGBT with blocking voltages of between 600 V and 3300 V are set to go into production. There is still a lot of room for improvement, especially in diode turn-off behaviour.

ESBTs

The **E**mitter **S**witched **B**ipolar **T**ransistor (ESBT) is not an IGBT, but a monolithic cascode circuit made of an NPN bipolar transistor and power MOSFET and was originally developed for applications with high switching frequencies at high operating voltages. Figure 2.4.15 shows its principle structure and the equivalent circuit.

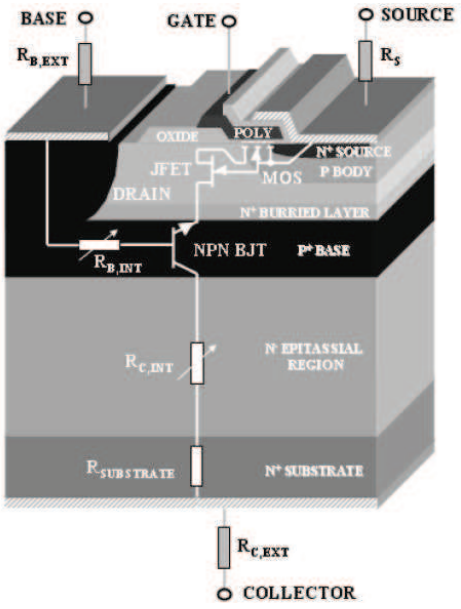


Figure 2.4.15 ESBT structure and equivalent circuit [24]

Circuits based on a cascode comprising a low-volt MOSFET and high-volt bipolar transistor were already being employed in discrete components or hybrid-integrated layouts in the eighties. The MOSFET is located in the emitter circuit of the bipolar transistor (series connection). In ON-state, the bipolar transistor and MOSFET are fully controlled. The ESBT on-state voltage is the sum of the on-state voltages of the high-volt bipolar transistor and low-volt MOSFET.

The ESBT is controlled by the MOSFET gate, the base of the bipolar transistor is permanently connected to a voltage source via resistors. During turn-off, the MOSFET opens the emitter circuit of the bipolar transistor and the collector current flows through the base to the driver voltage source until all charge carriers in the bipolar transistor have been discharged or recombined and the collector current is extinguished. Since the emitter is disconnected by the MOSFET during turn-off, there is no risk of a second breakdown of the bipolar structure; the base current extends the limits of the RBSOA (cf. chapter 3.3.4) as compared to regular switching, and component turn-off is possible up to the limiting value V_{CB0} of the collector-base diode. MOSFET gate control enables the driver output to be comparatively low.

2.4.3 Power MOSFET

While the drain-source ON-resistance $R_{DS(on)}$ of low-voltage MOSFET is composed of individual cellular resistances with shares of approx. 5% to 30%, some years ago more than 90% of the $R_{DS(on)}$ of MOSFET using higher reverse voltages resulted from the n^- epitaxial area resistance. For the dependency of $R_{DS(on)}$ on the power MOSFET drain-source breakdown voltage $V_{(BR)DSS}$, the following equation applied:

$$R_{DS(on)} = k \cdot V_{(BR)DSS}^{2,4...2,6}$$

where k: material constant, e.g. $k = 8{,}3 \cdot 10^{-9}\ A^{-1}$ for 1 cm² chip area

i.e. the on-state voltage

$V_{DS(on)} = I_D \cdot R_{DS(on)}$ where I_D: drain current

was far higher for transistors with a blocking voltage above around 400 V than that of a comparable IGBT.

The compensation principle in new MOSFET concepts developed as of 1999 (Superjunction MOSFET, see chapter 2.4.3.3) enabled the link between blocking voltage and doping of the n^- region to be broken, thus drastically reducing its resistance. According to [25], for such power MOSFET, the equation

$$R_{DS(on)} = k \cdot V_{(BR)DSS}^{1,3}$$

now represents a far lower dependency of the on-state voltage on the blocking voltage.
For MOSFET applications in practice, its purely ohmic output characteristic is advantageous without the threshold voltage of bipolar components. The essential advantage that the unipolar MOSFET has over to bipolar components is, however, that there are no storage effects, because the majority charge carriers are exclusively responsible for charge transfer; extremely short switching times can be achieved.
In practice, power MOSFET properties are strongly influenced by the parasitic elements in the real structure. To understand these real properties and possible failure mechanisms, the equivalent circuit diagram of the power MOSFET (Figure 2.4.16) must be considered.

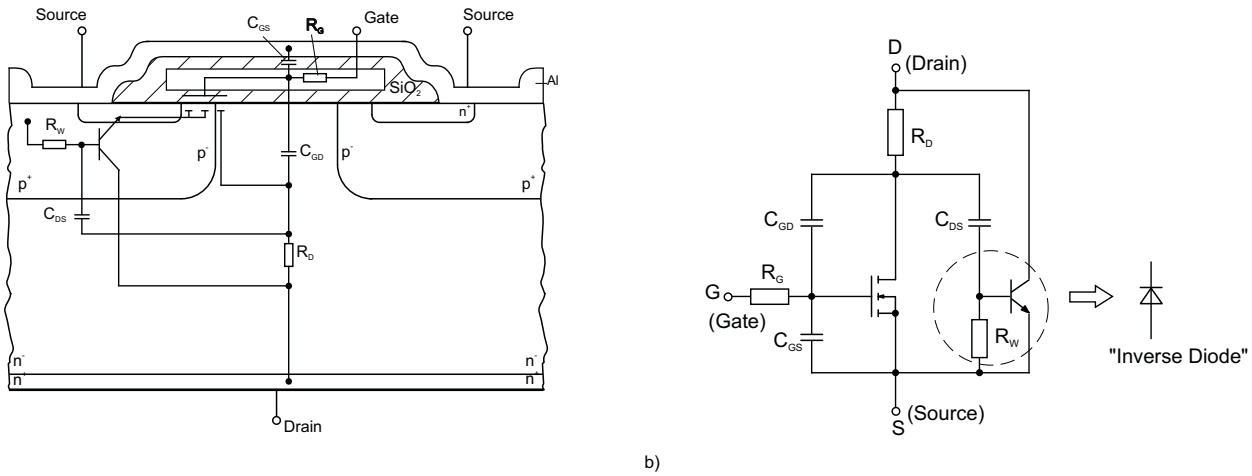


Figure 2.4.16 Power MOSFET cell including the key parasitic elements
a) Parasitic elements in the cellular structure; b) Equivalent circuit diagram with parasitic elements

The physical causes and designations of the parasitic capacitances and resistances shown in Figure 2.4.16 are evident in Table 2.4.3.

Symbol	**Designation**	**Physical Description**
C_{GS}	Gate-source capacitance	Overlapping gate and source metallisation; dependent on gate-source voltage; independent of drain-source voltage
C_{DS}	Drain-source capacitance	Junction capacitance between n^- drift area and p-well; dependent on cell surface, breakdown voltage and drain-source voltage
C_{GD}	Gate-drain capacitance	Miller capacitance; generated by overlapping of gate and n^- drift area
R_G	Internal gate resistance	Polysilicon gate resistance; additional series resistors are often needed in modules with several transistor chips to minimise oscillations between chips
R_D	Drain resistance	Resistance of n^- region; often the main part of MOSFET on-state resistance
R_W	Lateral resistance of the p-well	Base-emitter resistance of the parasitic bipolar NPN transistor

Table 2.4.3 Physical causes and designations of MOSFET parasitic elements

Apart from internal capacitances and resistances, the equivalent circuit diagram of the power MOSFET also shows an "ideal MOSFET", an NPN transistor at the gate side: n^+ source region (emitter) / p^+ well (base) / n-drift area (collector) with lateral resistance of the p^+-well below the emitters as base-emitter resistance R_W. R_W and the base-to-collector connection of the parasitic bipolar transistor form the inverse diode, which makes the power MOSFET reverse-conducting.

2.4.3.1 Static behaviour

Figure 2.4.17 shows the output characteristics of a power MOSFET with structural reverse conductivity ("inverse diode"), freewheeling diode and its transfer characteristic.

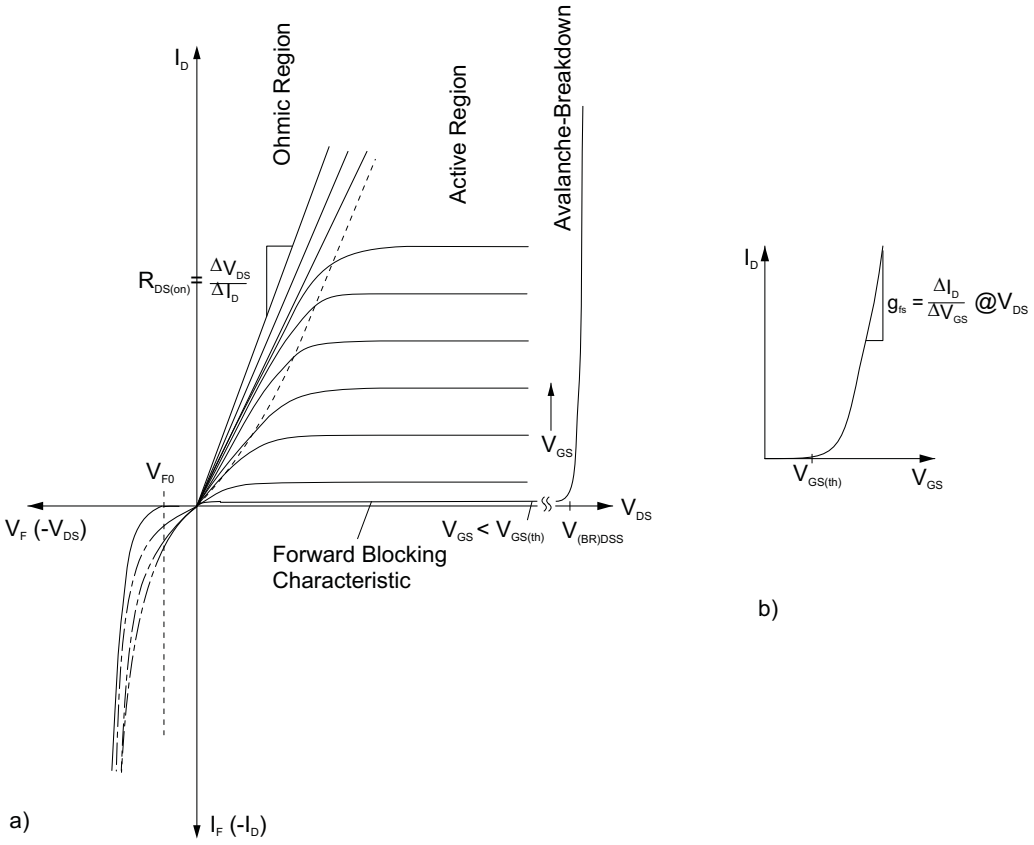


Figure 2.4.17 a) Output characteristics of a power MOSFET (n-channel enhancement type)
b) Transfer characteristic $I_D = f(V_{GS})$

The stationary switching states are as follows:

Forward off-state and avalanche breakdown

If a positive drain-source voltage V_{DS} and a gate-source voltage V_{GS} below the gate-source threshold voltage level $V_{GS(th)}$ is applied, only a very small cut-off current I_{DSS} will flow between the drain and source terminal. When V_{DS} rises, I_{DSS} increases slightly at first. Above a specified, maximum rated drain-source voltage V_{DSS} there will be an avalanche breakdown of the PIN junction p^+-well / n^- drift area / n^+ epitaxy layer (drain-source breakdown voltage $V_{(BR)DSS}$). Physically speaking, $V_{(BR)DSS}$ corresponds roughly to the breakdown voltage V_{CER} of the parasitic bipolar NPN transistor in the MOSFET structure, generated by the following sequence of layers: n^+ source region (emitter) / p^+-well (base) / n^- drift area / n^+ epitaxy layer drain region (collector).

The multiplication current generated during avalanche breakdown in the collector-base diode can lead to MOSFET destruction caused by bipolar transistor turn-on. Base and emitter regions are, however, almost shorted by the emitter metallisation; between them there is nothing but the lateral resistance of the p^+-well. Various design-related measures, e.g. small MOSFET cells, a homogenous cell field, low-ohmic p^+-wells, optimum outer structures and very homogenous technological processes, can produce a very low breakdown current per cell which - under precisely specified conditions - will not yet trigger turn-on of the bipolar transistor structure. For these "avalanche-resistant" MOSFET chips, the datasheets specify a permissible avalanche energy E_A for single pulses or periodic load (limited by the maximum rated chip temperature).

Since absolute symmetry cannot be guaranteed for power modules working with several MOSFET chips connected in parallel, it is not permissible to use more than the maximum E_A value guaranteed for a single chip.

On-state (1st quadrant)

The forward on-state at a positive drain-source voltage V_{DS} and positive drain current I_D comprises two characteristic curve areas:

Active region (pinch-off area)

With a gate-emitter voltage V_{GE} that hardly exceeds the gate-emitter threshold voltage $V_{GE(th)}$, a relatively high voltage share will be depleted through the channel owing to current saturation (horizontal part of the output characteristics). The drain current I_D is controlled by V_{GS}. As a measure for the transfer behaviour as described in Figure 2.4.17b) the forward transconductance g_{fs} is defined as

$g_{fs} = \Delta I_D/\Delta V_{GS} = I_D/(V_{GS}-V_{GS(th)})$.

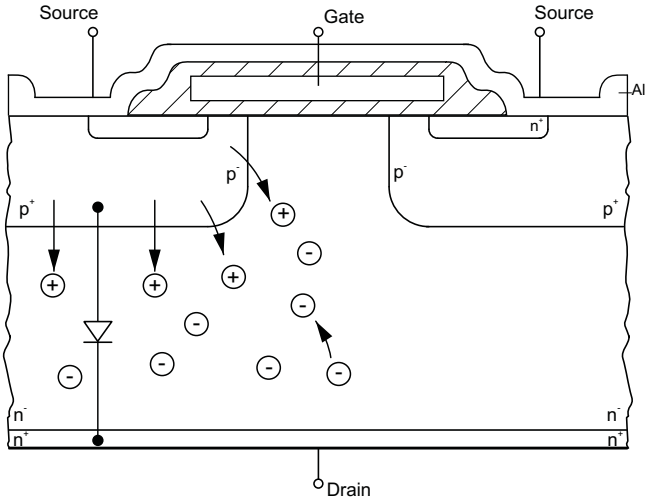
Forward transconductance rises in proportion to the increase in drain current I_D and the drain-source voltage V_{DS} and falls as chip temperature increases. In the switching mode that is exclusively permissible for power modules working with several MOSFET chips connected in parallel, the pinch-off area is only run through during turn-on and turn-off. Stationary module operation in the pinch-off area is not permissible, because $V_{GS(th)}$ drops when the temperature rises, meaning that even small differences between the individual chips may cause thermal instability.

Ohmic characteristic area

The ohmic characteristic area (steep part of the output characteristics), which corresponds to ON-state during switching operations, is reached when I_D is determined by the outer circuit only. On-state behaviour is charaterised by the drain-source on-resistance $R_{DS(on)}$ as a quotient of changing drain-source voltage V_{DS} and drain current I_D. The on-resistance $R_{DS(on)}$ is dependent on the gate-source voltage V_{GS} and the chip temperature. In the operating temperature range of a MOSFET, $R_{DS(on)}$is almost doubled in the range between 25°C and 125°C, cf. chapter 3.4.3.

Inverse operation (3rd quadrant)

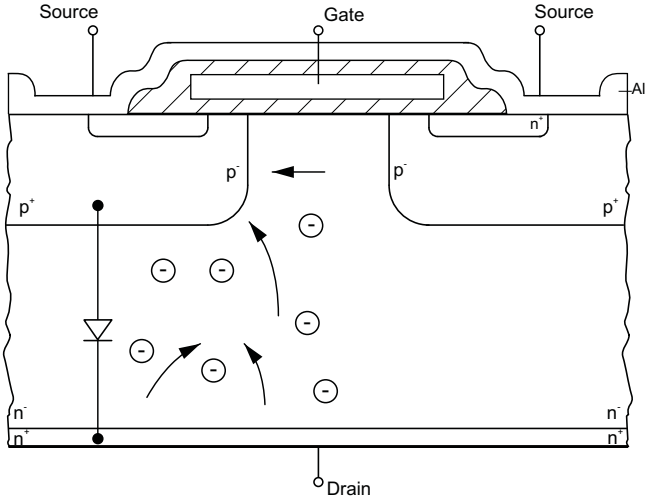
In inverse mode, the MOSFET has a diode characteristic at $V_{GS} < V_{GS(th)}$ (continuous curve in Figure 2.4.17). This behaviour is caused by the parasitic diode in the MOSFET structure; the on-state voltage of the collector-(source)-base-(drain)-pn-junction ("inverse diode"). The bipolar current flow through this diode determines the on-state behaviour of the MOSFET in reverse direction, when the channel is closed (Figure 2.4.18a).



V_{GS} = 0 V

V_{DS} = $-V_F$

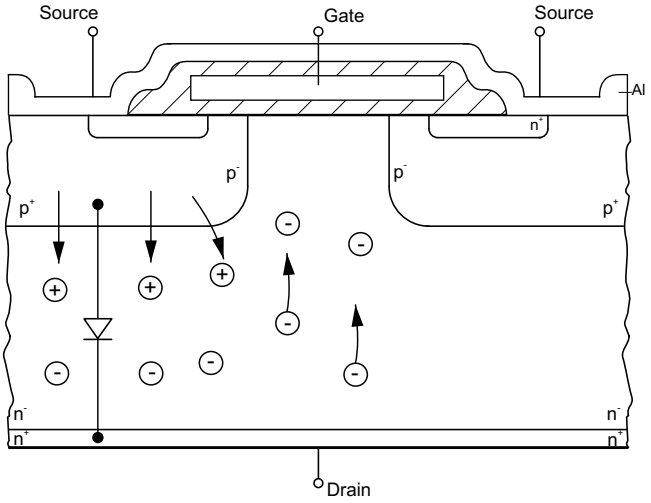
a)



$V_{GS} > V_{GS(th)}$

$V_{DS} > -V_{F0}$ (z.B. -0.2 V)

b)



$V_{GS} > V_{GS(th)}$

$V_{DS} < -V_{F0}$ (z.B. -0.7 V)

c)

Figure 2.4.18 Inverse operation of a power MOSFET [26] ; a) Closed channel (bipolar current flow); b) Open channel and low negative V_{DS} (unipolar current flow); c) Open channel and high negative V_{DS} (combined current flow)

Generally speaking, the bipolar inverse diode can be utilised within the current limits specified for the MOSFET. Practice, however, often shows that
- inverse diodes cause relatively high on-state losses which must be dissipated together with the MOSFET losses and
- that the poor turn-off behaviour and relatively low dv/dt limits of these PIN diodes are responsible for the practical application limits of MOSFET bridge circuits in processes that require hard switching.

As shown in Figure 2.4.18, the MOSFET channel can also be conductively controlled when a negative drain-source voltage is present, provided that a gate-source voltage is applied above the threshold voltage level.

If the drain-source voltage is then externally limited - e.g. by connecting a Schottky diode in parallel - to values below the threshold voltage of the inverse diode, the inverse current will remain a unipolar electron flow (majority carrier flow) from drain to source. Consequently, the switching behaviour corresponds to that of MOSFET. The inverse current depends on $-V_{DS}$ and V_{GS} (Figure 2.4.18b).

Operation according to Figure 2.4.18c occurs, if the channel is additionally controlled while the bipolar inverse diode is conducting (drain-source voltage above threshold voltage level). This results in a lower on-state voltage than for a simple parallel connection for diode and MOSFET, since the injected charge carriers laterally diffuse as well, thus improving MOSFET conductivity.

Today, this behaviour is made use of in low-voltage power supply systems, where "synchronous rectifiers" with integrated MOSFET can be used instead of conventional diode rectifiers. If MOSFET are triggered during the conducting phase of their inverse diode, switch-mode power supplies with < 15 V output voltage, for example, may substantially gain in efficiency owing to the extremely low on-state voltage (some 10 mV) compared to conventional diode rectifying (on-state voltage several 100 mV).

2.4.3.2 Switching behaviour

The switching behaviour (switching velocity, losses) of MOSFET power modules is determined by their structural, internal capacitances and the internal and terminal resistances. Contrary to the ideal of powerless voltage control via the MOSFET gate, frequency-dependent control power is required; this is owing to the recharge currents of the internal capacitances which are needed for switching. Furthermore, the commutation processes are affected by the parasitic connection inductances present in the components and connections and generated by connecting transistor chips in power modules; they induce transient overvoltages and may cause oscillations due to the circuit and transistor capacitances, cf. chapter 5.

The switching behaviour of power MOSFET can be described as resulting from the transistor's internal capacitances and resistances:

When the MOSFET is turned off, C_{GD} is low and approximately equal to C_{DS}.

During on-state, C_{GD} will increase rapidly as soon as the gate-source voltage has exceeded the drain-source voltage; this is due to inversion in the enhancement layer below the gate regions.

Datasheets (cf. chapter 3.4.3) normally list the low-signal capacitances C_{iss}, C_{rss} and C_{oss} of the turned-off transistor, see Table 2.4.4.

	Power MOSFET
Input capacitance	$C_{iss} = C_{GS} + C_{GD}$
Reverse transfer capacitance (Miller capacitance)	$C_{rss} = C_{GD}$
Output capacitance	$C_{oss} = C_{GD} + C_{DS}$

Table 2.4.4 Definition of MOSFET low-signal capacitances

When calculating the switching behaviour, this data is of very limited use only, for reasons that have already been explained in detail for the IGBT. The "hard" switching behaviour of MOSFET when switching ohmic-inductive loads with continuous load current, i.e. the time constant of the load L/R is much greater than the cycle 1/f of the switching frequency, is looked at below. Figure 2.4.19 shows the basic waveforms of drain current and drain-source voltage in analogy to the IGBT described in the previous chapter.

Apart from the non-ideal properties of transistors and diodes, passive circuit components also influence switching losses and operating point waveforms to a high degree. Their influence will be discussed in more detail later in chapter 5.

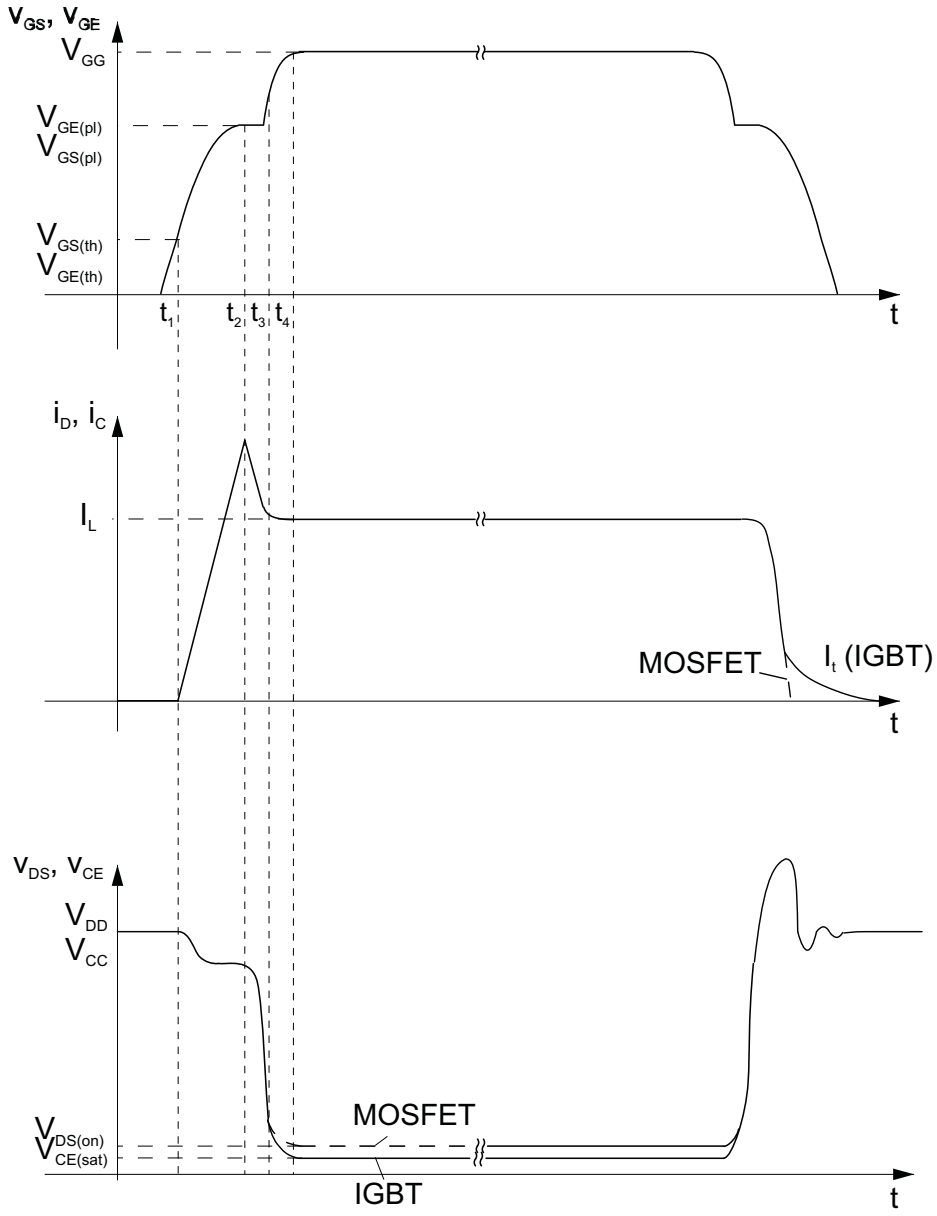


Figure 2.4.19 Typical "hard" switching behaviour of power MOSFET and IGBT when switching ohmic-inductive load with a freewheeling circuit (current and voltage waveforms)

Turn-on

As Figure 2.4.19 demonstrates, the drain-source voltage of the power MOSFET drops to the on-state voltage value within some 10 ns $V_{DS(on)} = I_D \cdot R_{DS(on)}$.

Turn-on: switching interval 0...t_1 (blocked transistor)

The gate current i_G starts flowing when the control voltage is applied. At first, i_G charges only the gate capacitance C_{GS} until it reaches the charge quantity Q_{G1}; the gate-source voltage V_{GS} rises in line with the time constant determined by the input capacitance of the MOSFET and the gate resistance. Since V_{GS} is still below the threshold voltage $V_{GS(th)}$, no collector current will flow during this period.

Turn-on: switching interval t_1...t_2 (drain current rise)

After the threshold voltage $V_{GS(th)}$ (t_1) has been reached, the drain current will start to rise. Similarly, V_{GS}, which is connected to the drain current in the MOSFET pinch-off area by means of the rate of rise g_{fs} with $I_D = g_{fs} \cdot V_{GS}$, will increase up to the value $V_{GS1} = I_D/g_{fs}$ (time t_2). Since the freewheeling diode can block the current at t_2 only, V_{DS} will not drop significantly before t_2 is reached. At $t = t_2$, charge Q_{G2} will have flowed into the gate.

The largest amount of turn-on losses is generated in the MOSFET during this time interval. As long as the i_D value is still below I_L and part of I_L still has to flow through the freewheeling diode, the drain-source voltage v_{DS} cannot drop far below the operating voltage V_{DD} during this period. The difference between V_{DD} and V_{DS} outlined in Figure 2.4.19 is mainly caused by transient voltage drops across the parasitic inductances of the commutation circuit.

Turn-on: switching interval t_2...t_3 (transistor fully switched on in the pinch-off area)

When the freewheeling diode is turned off, V_{DS} drops to the on-state value $_{\text{until } t}3$ $V_{DS(on)} = I_D \cdot R_{DS(on)}$ has been reached. Between t_2 and t_3, drain current and gate-source voltage are still coupled through the transconductance: V_{GS} remains roughly constant. While v_{DS} drops, the gate current i_G recharges the Miller capacitance C_{DG} with the charge (Q_{G3}-Q_{G2}). By $t = t_3$, an amount of charge equal to Q_{G3} will have flowed into the gate. After the entire load current I_L has been commutated to the MOSFET, the freewheeling diode will start to block. Owing to the reverse recovery time of the freewheeling diode, the MOSFET drain current i_D initially continues to rise above I_L during turn-off of the freewheeling diode (t_{rr}) by the amount I_{RRM} of the diode reverse current and dissipates the reverse recovery charge Q_{rr} of the freewheeling diode. For explanations of the characteristics I_{RRM}, Q_{rr} and E_{rr} for inverse diodes, see chapter 3.4.2.

Turn-on: switching interval t_3...t_4 (ohmic operating area)

At t_3, the MOSFET is now turned on and its operating point has passed through the pinch-off area and has reached the border of the ohmic operating area. V_{GS} and I_D are no longer coupled by g_{fs}. The charge quantity (Q_{Gtot} -Q_{G3}) now supplied to the gate causes the further rise in V_{GS} up to the level of the gate control voltage V_{GG}.

Turn-off

During turn-off, the processes described above run in reverse direction. Charge Q_{Gtot} has to be discharged from the gate with the aid of the gate current. In contrast to IGBT, power MOSFET do not use a negative gate voltage here but V_{GS} = 0 V, see chapter 5.
During *turn-off* only the internal capacitances of the power MOSFET have to be recharged to such an extent that there is no charge carrier influence left in the channel area. From this point on, neutrality interference in this area will quickly be reduced and the drain current will drop rapidly. The overshoot of v_{DS} over V_{DD} indicated in Figure 2.4.19 results mainly from the parasitic inductances of the commutation circuit and increases in proportion to the turn-off speed $-di_D/dt$ of the power MOSFET.
Likewise in the case of power MOSFET: the more the specific transistor application deviates from the "ideal hard switch" application described here, the more "blurry" the step-form of the gate-

source voltage curve becomes. The intervals "decoupled" during hard switching will then merge more and more, and any description of the switching behaviour becomes more complex.

2.4.3.3 Latest versions and new directions of development

Power electronics largely use the vertical structure shown in Figure 2.4.3, where gate and source terminals are located on the chip surface and the drain terminal is on the underside of the chip. The load current is conducted vertically through the chip outside the channel. The **VD**MOSFET version (**V**ertical **D**ouble **D**iffused MOSFET) introduced at the beginning of the eighties is still being used today and is being continuously improved on, e.g. reduction in cell dimensions. Depending on the application focus on "low" or "high" drain-source voltage, the key developments on the power MOSFET front have gone in two directions with significant structural differences:

Trench-Gate MOSFET

The example shown in Figure 2.4.20 illustrates the continuous development towards the Trench-MOSFET, which was introduced around 1997.

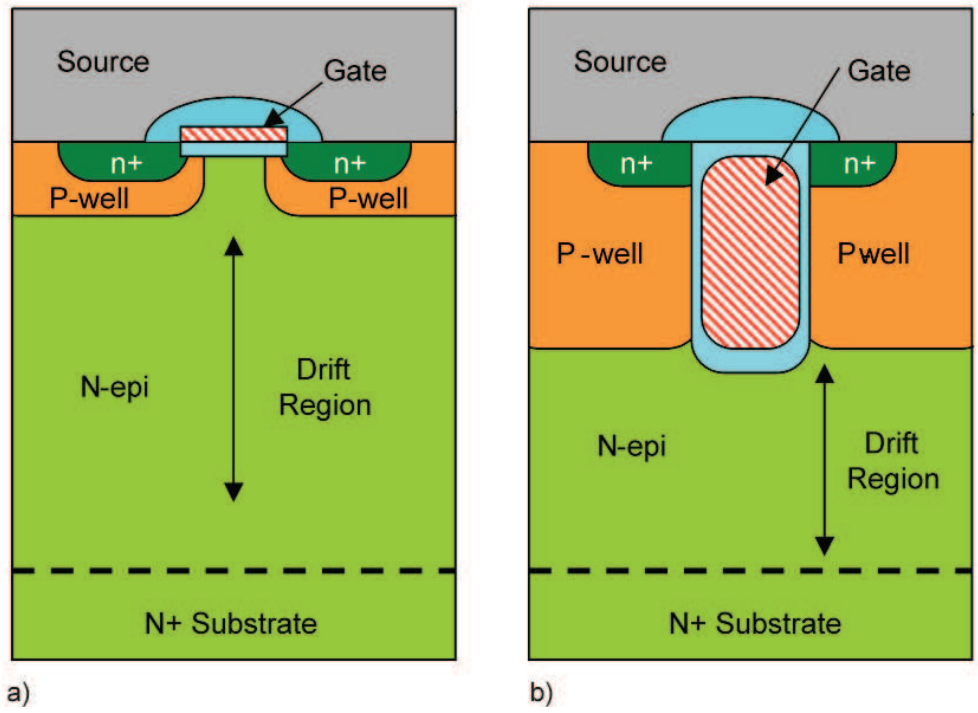


Figure 2.4.20 a) conventional VDMOSFET; b) MOSFET with trench-gate (Trench MOSFET) [27]

Similar to the development of the Trench IGBT, the insulated gate plates - and thus the channel area - are arranged vertically here; the distance to be covered by the electrons in the n-region is thus shorter. This enables a significant reduction in $R_{DS(on)}$ mainly in the lower voltage range compared to conventional structures.

Superjunction MOSFET

As mentioned at the beginning of this chapter, the "breakthrough" achieved in the reduction of $R_{DS(on)}$ was initiated in 1999 by Infineon with the development of the CoolMOS as the first "Superjunction" power MOSFET on the market.
The compensation principle used in superjunction components was developed for MOSFET with blocking voltages between 500 V and 1000 V. Figure 2.4.21 demonstrates the layout and functional principle of a CoolMOS.

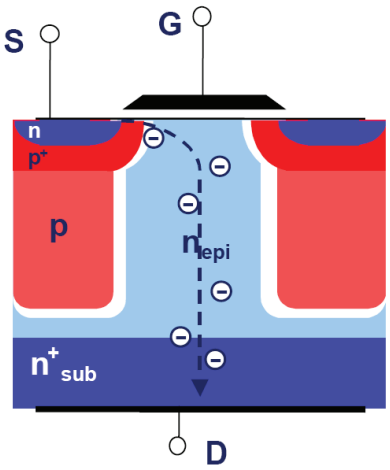


Figure 2.4.21 Layout and functional principle of a superjunction MOSFET (CoolMOS) [25]

With the aid of several epitaxy steps or lateral diffusion from trenches, high-doped conducting columns are injected into the low-doped n^- drift area. These columns are connected with the p-wells. Column doping is dimensioned such that the n-doping of the drift area is compensated for, resulting in a very low effective doping level.

In blocking state, the field is almost rectangular and can take up the maximum voltage level in relation to the thickness of the n^- region. Drift area doping can only be increased to such an extent that still allows for it to be compensated by the same amount of doping in the p-column ("compensation principle"). This overrides the interdependency of blocking voltage and doping density [17].

As a result, the thickness of the n^- drift area can be reduced substantially compared to conventional MOSFET, and drift area conductivity can be increased by way of higher doping. This means that the on-resistance $R_{DS(on)}$ will no longer increase to the power of 2.4...2.6, but almost linear to the breakdown voltage $V_{(BR)DSS}$; the on-state losses of high-blocking power MOSFET can be reduced significantly (to 1/3 - 1/5). Chip area, switching losses and gate capacitance / gate charge drop accordingly – for the same current capability. Figure 2.4.22 shows the differences in layout and properties for standard and superjunction power MOSFET.

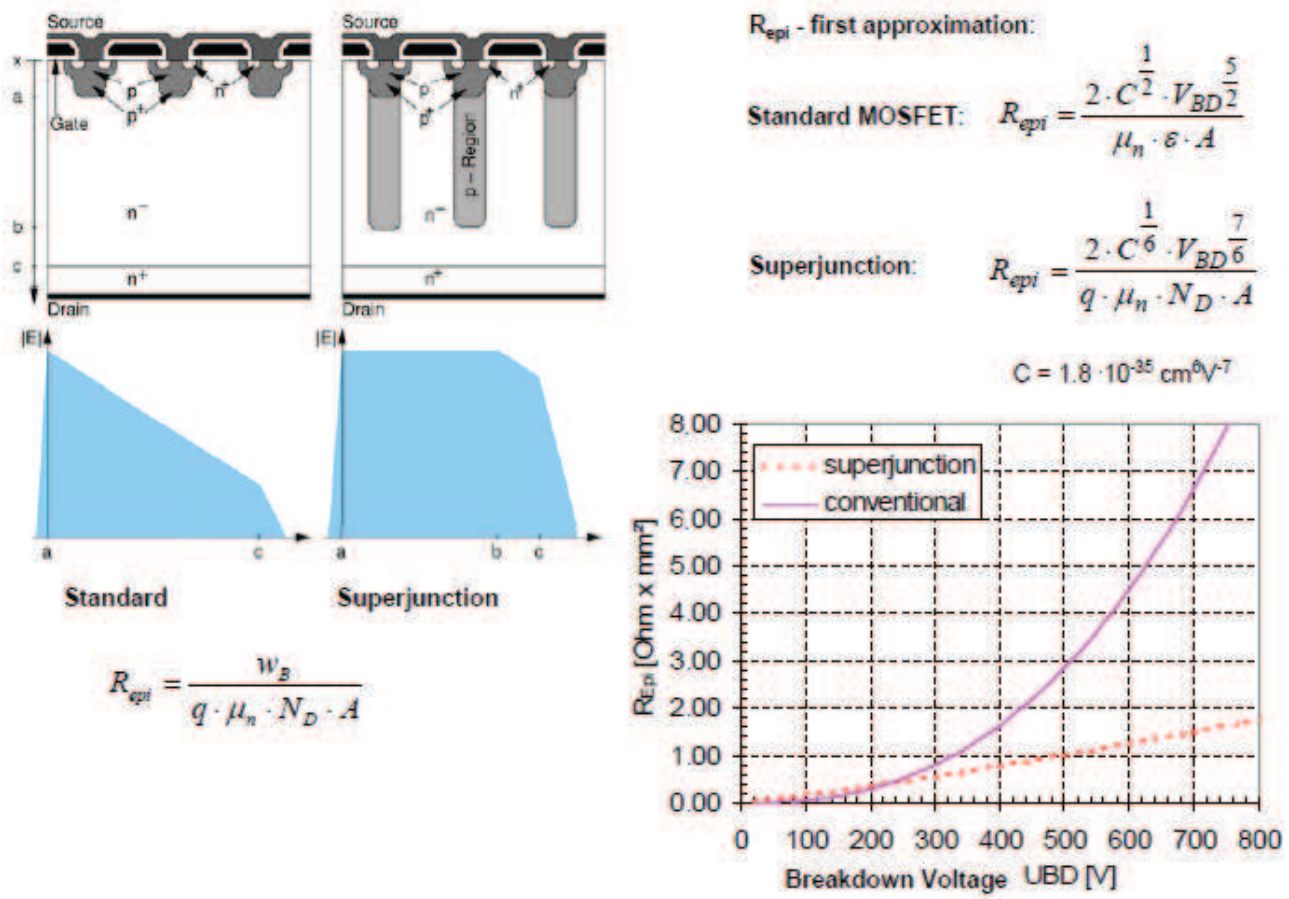


Figure 2.4.22 Comparison of standard and superjunction MOSFET [28]

Introduction of insulated field plates

In order to be able to transfer the superjunction principle to MOSFET for low voltages, technologies had to be developed that were much simpler and cheaper than those dealing with high-volt components. This challenge was met by Infineon, for example, with the product "OptiMOS", which is suitable for blocking voltages up to 300 V [29]. OptiMOS transistors have insulated field plates rather than p-columns built up in epitaxy processes. These field plates are arranged in trenches which are etched into the n^- drift area, insulated by a layer of silicon oxide and alternately connected to the source region and the polysilicon gate (Figure 2.4.23).

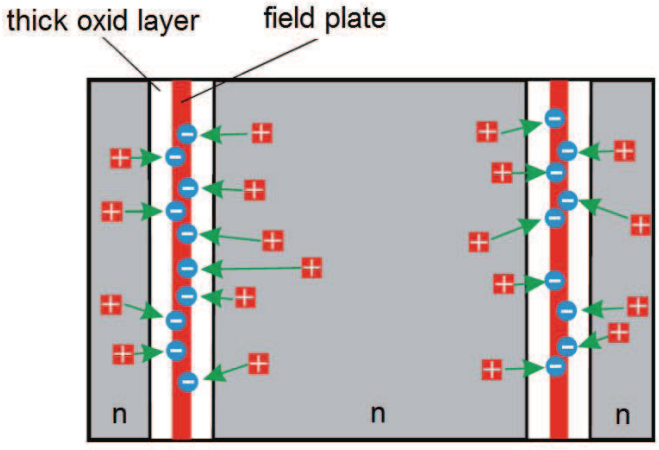


Figure 2.4.23 Principle layout of an OptiMOS [29]

Figure 2.4.24 shows the compensation effect of the field plates and the field intensity characteristics in y-direction compared to a conventional-type blocked pn-junction. The p-charge on the field plates compensates the doping of the n^- region so that it can be increased as described above. In

off-state, the triangular field shape of the simple structure becomes almost rectangular, permitting the reduction of the n^- layer thickness. Higher doping and reduced n^- drift area thickness brings about the advantages that superjunction MOSFET have over conventional structures, as detailed above.

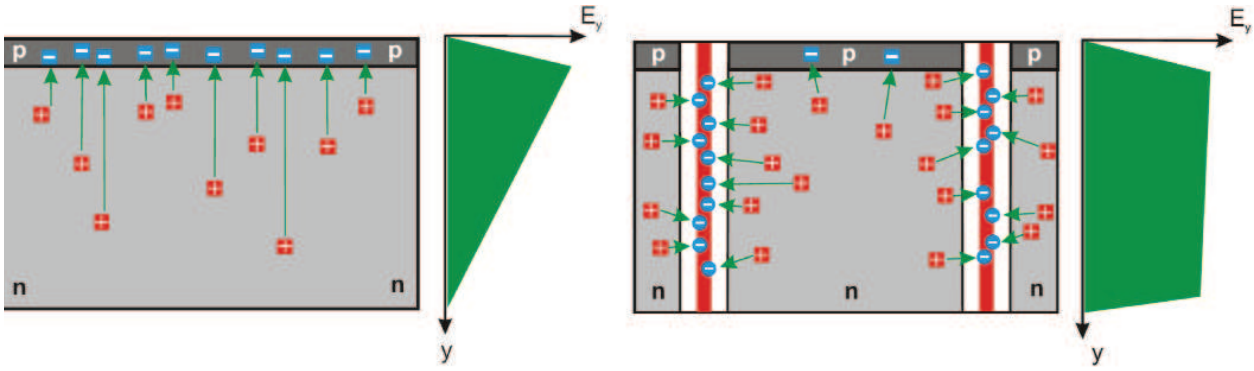


Figure 2.4.24 Field distribution in a conventional pn-junction and a pn-junction with field plates [29]

2.5 Packaging

Packaging has to fulfil the following main purposes:
- Provide electrical connection between one or more semiconductor chips and the circuit
- Dissipate the heat generated during chip operation to a cooling device
- Protect the semiconductor chip from harmful ambient influences
- Identify component type and terminals

Depending on the packaging technology used, power semiconductors can be divided into the following categories. In some components, solder connections are replaced by a sintered layer.

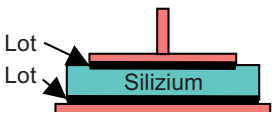
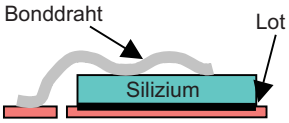
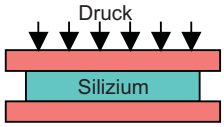
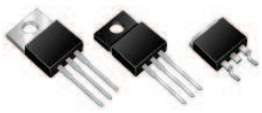
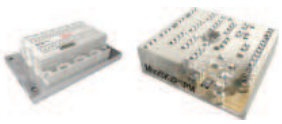
	Power semiconductors double-sided soldering	**Soldered/bonded power semiconductors**	**Power semiconductors with pressure contacts**
Technology / Functions			
Discrete power semiconductors (non-insulated)			
Insulated modules with base plate			
Insulated modules without base plate	-		-
IPM (intelligent power modules, insulated)	-		-

Table 2.5.1 Power semiconductor classification according to packaging technology

Innovations in packaging technology focus on a number of areas, including:
- Improvement of heat dissipation and thermal cycling capability
- Minimisation of inductances in the module and in the supply leads by means of suitable module designs
- Highly flexible packaging, easy customer assembly
- Greater degree of integration (converter circuits)
- Integration of monitoring, protection and driver functions

2.5.1 Technologies

2.5.1.1 Soldering

Soldering is the connection of two (metal) materials by means of liquid metal or a liquid alloy. Individual atoms in the solder then diffuse into the metal surface of the components to be soldered and a thin layer of an alloy made of solder and substrate is created. The prerequisite for void-free soldering quality are clean surfaces free from oxide for all connection components involved. For this purpose, fluxing agents are often used to clean surfaces; these agents are activated when the materials are warmed up for soldering. They also protect the surfaces from re-oxidation during soldering. Most fluxing agents must be removed again after soldering. Reducing gases, such as inert gas, can be used as fluxing agents. Applying a vacuum as soon as the solder has liquefied is a very good way of achieving void-free connections. Solder connections must conform with the RoHS Directive (Restriction of Hazardous Substances Directive) of the European Union.

A wide variety of soldering processes are available and are mainly distinguished by the manner in which heat is coupled to the part to be soldered. An interesting process method is the use of soldering pastes consisting of little solder balls and a paste-like fluxing agent. Using a dispenser, by screen or stencil printing, the paste is applied onto one of connection parts; the second partner (e.g. the chip) is pressed into the paste and the connection is heated until the solder melts (reflow soldering).

Large-area solder connections between materials with very different thermal expansion coefficients are critical (Table 2.5.4). The bimetal effect causes bending and, under thermal cycling, solder fatigue which will ultimately result in solder failure. For this reason it is not possible to solder large-area ceramic parts onto copper base plates, for example.

2.5.1.2 Diffusion sintering (low-temperature joining technology)

Diffusion sintering is a process which can replace soldering in many cases. It may be considered as being far superior to soldering in terms of its long-term reliability. At a temperature of around 250°C, fine silver powder is sintered under high pressure to form a low-porous silver bond layer (Figure 2.5.1) between the parts to be connected.

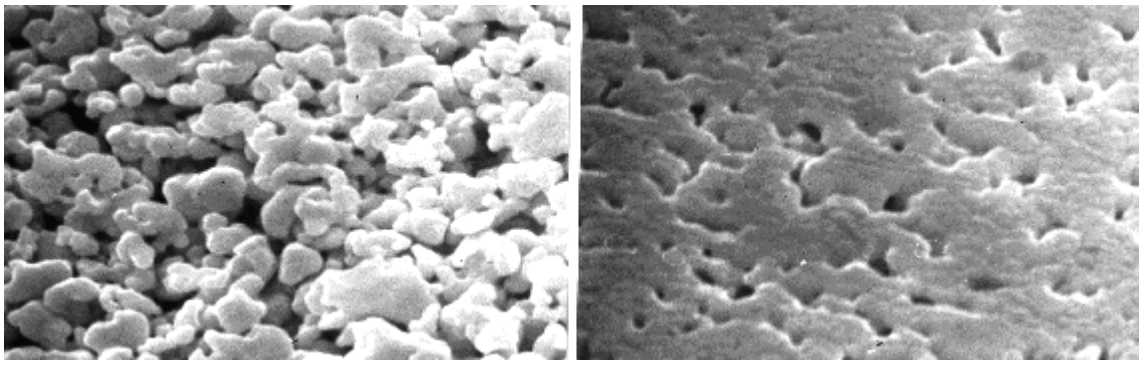


Figure 2.5.1 Silver powder before and after diffusion sintering

Sintered layers are stable up to the melting point of silver (962°C). Fluxing agent is not required. Sintered layers display better thermal, mechanical and electrical properties than solder (Table 2.5.2).

Property		Solder layer SnAg(3)	Ag sintered layer
Melting point	°C	221	962
Heat conductivity	W/mK	70	240
Electric conductivity	MS/m	8	41
Typical layer thickness	µm	90	20
Thermal expansion coefficient	ppm/K	28	19

Table 2.5.2 Comparison of important properties of SnAg(3) solder and diffusion-sintered silver.

The main advantage of the sintered layer is its resistance to temperature cycles; this is even true for high maximum temperatures. In contrast, solder tends to lose its strength when subjected too high stresses caused by temperature cycles. The great potential of sinter technology can best be demonstrated by specifying its homologous temperature. The homologous temperature (in%) of a material is defined as the ratio of operating temperature to melting point, both given in Kelvin. For homologous temperatures below 40%, materials are barely or not at all weakened by temperature. The creepage area lies between 40% and 60%. This is the area in which material properties are susceptible to mechanical stress. Above 60% their strength declines considerably; the material is regarded as unsuitable for this application (Table 2.5.3). The disadvantage of diffusion sintering is that only materials with a precious metal surface can be connected.

Homologous temperature for	Solder layer SnAg(3)	Ag sintered layer
Operating temperature 100°C (373 K)	76%	30%
Operating temperature 150°C (423 K)	86%	34%
Melting temperature (100%)	221°C (494 K)	962°C (1,235 K)

Table 2.5.3 Homologous temperature in% for SnAg(3) solder and a silver diffusion-sintered layer at two operating temperatures

In series production, sintering technology was first used to replace solders in chip-to-DBC connection. SKiM63/93 modules are the first fully solder-free modules. Sintering could also be used to eliminate the shortcomings of large-area DBC to base plate soldering [30] or those of wire bonded connections. Examples of the latter option are presented in Figure 2.5.2.

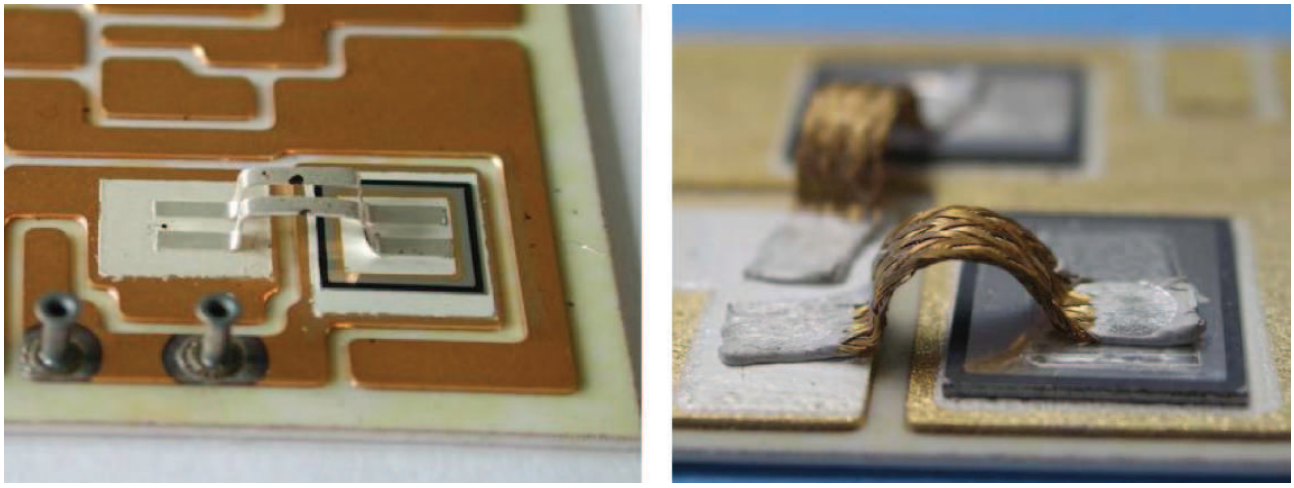


Figure 2.5.2 Sintered silver bands [31] or copper litz wires [32] as substitutes for conventional bond wire connections

2.5.1.3 Wire bonding

Wire bonding is often used to connect a power semiconductor chip face with other chips or connecting elements. This is a cold welding process where ultrasonic energy is used to connect an aluminium wire (about 100 µm to 500 µm thick) to a surface made of aluminium, copper or gold. This process takes place at room temperature. Since a bond wire is limited in its current capability, several bond wires are used in parallel for higher amperages. Stitching, i.e. multiple bonding of a wire on a surface, is employed to distribute the current more evenly on a chip (Figure 2.5.3).

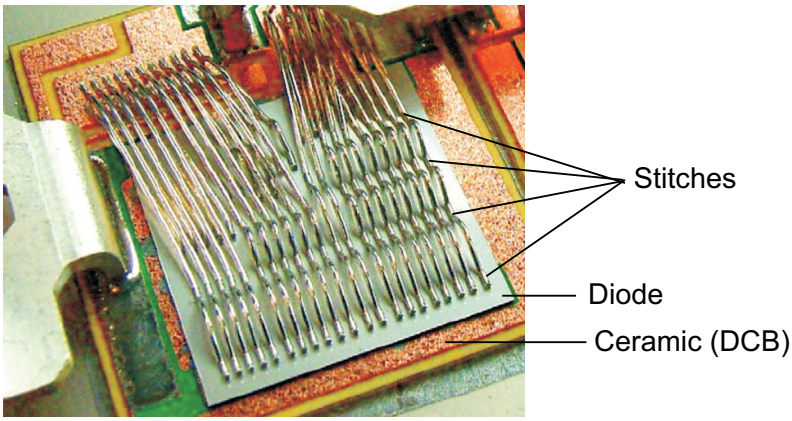


Figure 2.5.3 Many parallel, "multi-stitched" bond wires on a diode chip, 502 mm² face.

Since wire-bonding is a very flexible and cost-effective solution, this technology will remain the major connection method for chip surfaces in the near future.

2.5.1.4 Pressure contact

In contrast to soldering, diffusion-sintering and wire-bonding, pressure contacts are not metallurgical joints but a positive connection method. This means the pressure-contacted partners can be offset against each other and can glide on each other. Tensions that would arise in the case of metallurgical joints during temperature cycles owing to the different thermal expansion coefficients of the connection partners thus do not appear or to a very limited extent only. Pressure contacts do not display fatigue caused by temperature change, as is the case with soldered and wire-bonded connections. This explains the high reliability of pressure-contacted components. With a suitable design (disk cells), double-sided cooling can be obtained by clamping the component between two heat sinks, thus cutting the thermal resistance in half. A differentiation should be made between large-surface and small-surface ("dot-shaped") pressure contacts.

Large-surface pressure contact

Here, the surfaces of the parts being connected, which are pressed against each other under high force, must be clean and planar. In addition, the contact surfaces must not be prone to cold welding, because this would prevent them from "floating". This can be ensured by selecting suitable surface pairs. Examples of large-surface pressure contacts are disk cells or module/heat sink connections.

Small-surface pressure contact

Here, the contact area is line-shaped or almost dot-shaped. This extremely small contact area requires just a small force to apply high pressure to the contact area. The pressure is so high that oxide layers or other surface pollution of the small-surface contact partner can be penetrated, thus ensuring safe and reliable contact. In many modules, such contacts are used in the form of spiral springs for control terminals, as well as in MiniSKiiP modules.

SKiiP® technology

SKiiP® is a purpose-developed pressure-contact technology which provides advantages for all module power rating classes in terms of performance, service life, reliability and costs. The most important characteristic of SKiiP® is the elimination of soldered connections to the base plate

and terminals. For this purpose, the solid, 2 to 5-mm-strong copper base plate is done away with. Instead, the insulating substrate (DBC) - together with the soldered or sintered chips - is pressed directly onto the heat sink by the case, pressure elements or the terminals.

The main advantage of this layout is that there is no metallurgical joint between the ceramic substrate (thermal expansion coefficient is about 4 -7•10^{-6}/K) and the base plate (thermal expansion coefficient of copper is about 17.5•10^{-6}/K). This means there is no large-area soldering. This helps to avoid the high mechanical tension between base plate and ceramic parts that occurs in base plate modules due to temperature changes. Soldered terminals can also be replaced with pressure contacts. A number of module families covering a wide performance range are based on SKiiP® technology. Besides the SKiiP® module family, this includes all SKiM, MiniSKiiP, SEMITOP and most SEMIPONT modules.

2.5.1.5 Assembly and connection technology

Most power modules available today have cases containing screw, plug-in, solder or spring contacts (Figure 2.5.4).

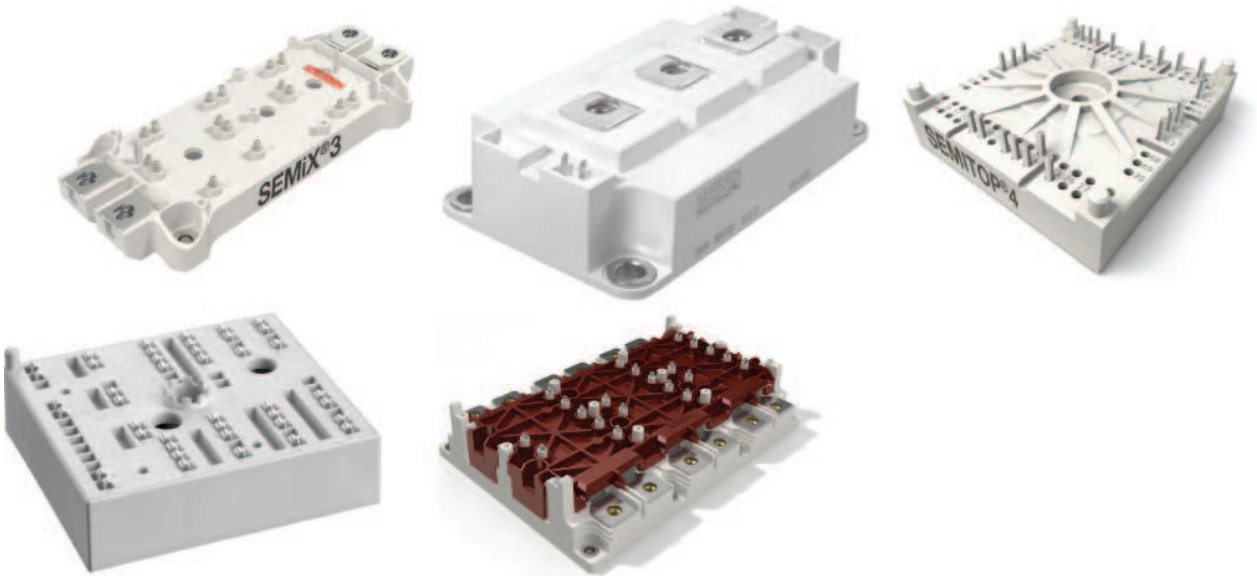


Figure 2.5.4 Transistor module designs (selection)

The highest degree of standardisation is found in module types with screw terminals. The main terminals may be contacted by busbars or sandwich assemblies. Additional terminals are often provided for control and sense-units (e.g. control-emitter, sense-collector) in order to minimise the influence of inductive voltage drop in the main circuit generated during switching. Auxiliary terminals are mostly designed as 2.8 mm flat strip plug connectors for wire connections, or with springs for direct driver circuit assembly on the PCB.

Components for direct PCB assembly are very important in the current range of up to about 100 A, because they offer cost advantages in production and automatic assembly. Optimised layout of connectors enables low-inductance assemblies. Solder pins (e.g. SEMITOP, ECONOPACK), press-fit contacts or spring contacts (e.g. MiniSKiiP) are used as connectors. Current capability for high load currents is achieved by connecting several terminals in parallel. What is problematic here is the large track cross-sections (required for high currents) and the introduction of maximum-length creepage paths on the PCB. This limits both component performance and application voltages.

The merits of spring contacts

Figure 2.5.5 Spring types for main and auxiliary contacts

Spring contacts have a number of advantages over solder and press-fit contacts with respect to PCB assembly.

- Better utilisation of the PCB area and easier routing, since "vias" are not required
- Easier assembly automation, since no large-surface components with tolerances have to be fitted into holes
- Assembly of the (heavy and expensive) power semiconductor and heat sink after soldering and PCB pre-testing
- Improved thermal cycling capability thanks to "free-moving" contacts
- Higher resistance to shock and vibration stress (no solder fatigue)
- Quasi-hermetically sealed contact is corrosion-proof
- No electromigration

Mechanical natural frequencies: The spring weight is so low that their natural frequencies (> 1 kHz) are far higher the mechanical oscillations produced in "heavy" power modules.

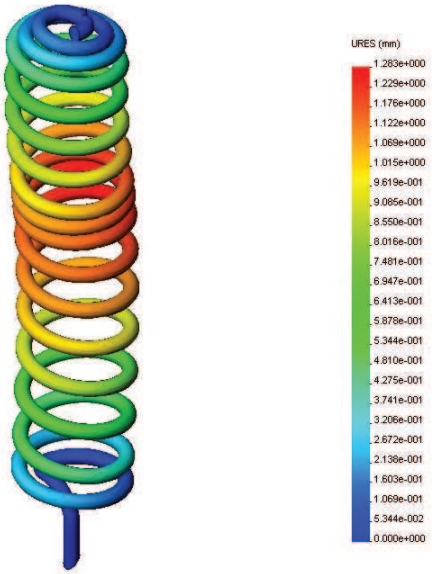


Figure 2.5.6 Natural frequency analysis of a non-loaded spring with a 1.1 kHz resonance frequency in Z-direction

Contact force: The spring contact contact force is about 2…10 kN/cm². This ensures safe and reliable contact even under shock stress of up to 100 G (SKiM63/93). This is within the range for screw connections and far higher than for plug-in contacts.

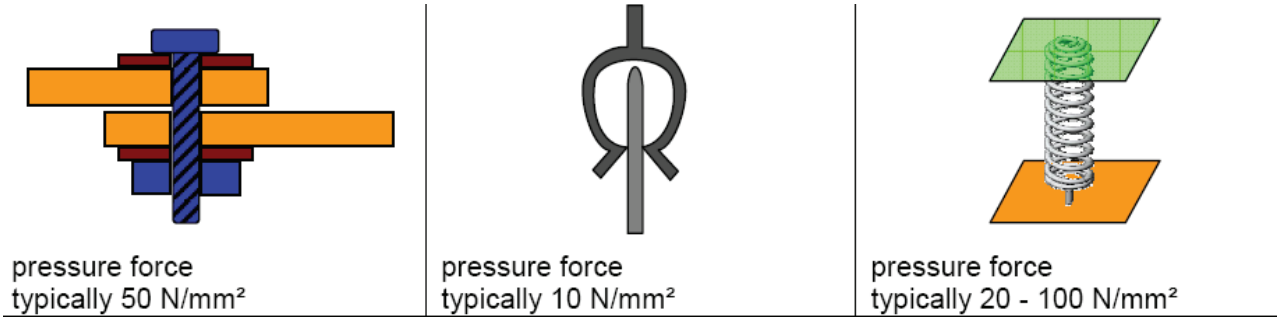


Figure 2.5.7 Comparison of contact pressures of detachable electrical connections (from left to right: screw, plug-in, spring contact)

Inductances: The inductance of a MiniSKiiP spring (Figure 2.5.5) only insignificantly higher than the one of a solder pin. Spiral springs, as used in the control circuit of SEMiX, SKiM and SKiiP, have a higher inductance. This lies within the range of 100 nH.

$$L = \mu \cdot n^2 \cdot \frac{\pi \cdot D}{4\sqrt{l^2 + D^2}} = 112\text{nH}$$

$\mu=\mu_0=1.26$ µH/m;
l=10 mm (length, pressed);
D=2 mm (inner diameter);
n=17 (number of windings);

This can be compared to connection wires of 10 cm in length, as are common in auxiliary terminals in modules with plug-in contacts. If the driver board is directly connected via the spiral springs, the total inductance composed of inner and outer inductance in the control circuit is even far lower than the wire-contacted interfacing of standard modules.

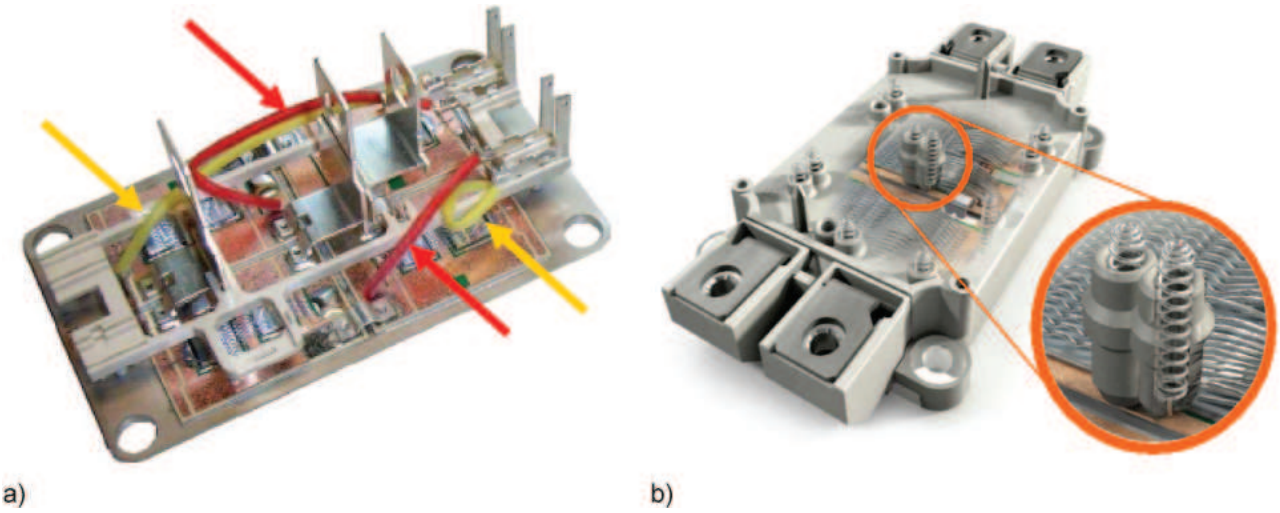


Figure 2.5.8 Control terminals of a SEMITRANS module (a) and a SEMiX module (b)

Landing Pad requirements: The springs have a silver-plated surface, the PCB landing pads must be tin-plated (chemically: Sn, HAL-Sn Hot Air Leveling) or coated with nickel / gold flash (>3 µ Ni, > 20 nm Au).

2.5.1.6 Modules with or without base plate

Some comparisons are rather inaccurate (e.g. [33]) since they compare the two technologies by examining a module with base plate to begin with and then simply removing the base plate to perform the comparison. Of course, both design variants must be constructed under totally different aspects. SEMIKRON offers both technologies, because both have advantages and disadvantages.

Base plate

Such modules are charaterised by the use of few large chips with good heat spreading through the base plate.

Advantages:
- Mechanically more robust during transport and assembly
- Larger thermal mass, lower thermal impedance within the range of 1 s

Disadvantages of modules with soldered or bonded chips (IGBT modules):
- Higher thermal resistance chip / heat sink $R_{th(j-s)}$, because base plate bending requires a thicker layer of thermal paste
- Reduced slow power cycling capability, since the large-area base plate solder pads are susceptible to temperature cycles
- Higher internal terminal resistances ($r_{cc'-ee'}$), since, for thermo-mechanical reasons, the design is based on small ceramic substrates that require additional internal connectors
- Increased weight

No base plate

Such modules use smaller chips and achieve thermal spreading on the heat sink thanks to heat sources which are better spread.

Advantages:
- Lower thermal resistance, because layers are omitted, even contact with the heat sink, thinner thermal paste layers
- Improved thermal cycling capability, because of removal of solder fatigue in base plate soldering (bec. no base plate!)
- Smaller chips; lower temperature gradient over the chip means a lower maximum temperature and less stress under power cycling conditions
- Few large ceramic substrates with low terminal resistance

Disadvantages
- No heat storage
- Processable chip size is limited, resulting in more parallel connections
- Increased requirements for thermal paste application

Eliminating the thermo-mechanical stress between base plate and ceramic substrate, rather than connecting several small substrates soldered onto a common base plate into one circuit with the aid of additional connection elements, enables very large ceramic substrates to be used in modules with no base plate (Figure 2.5.9).

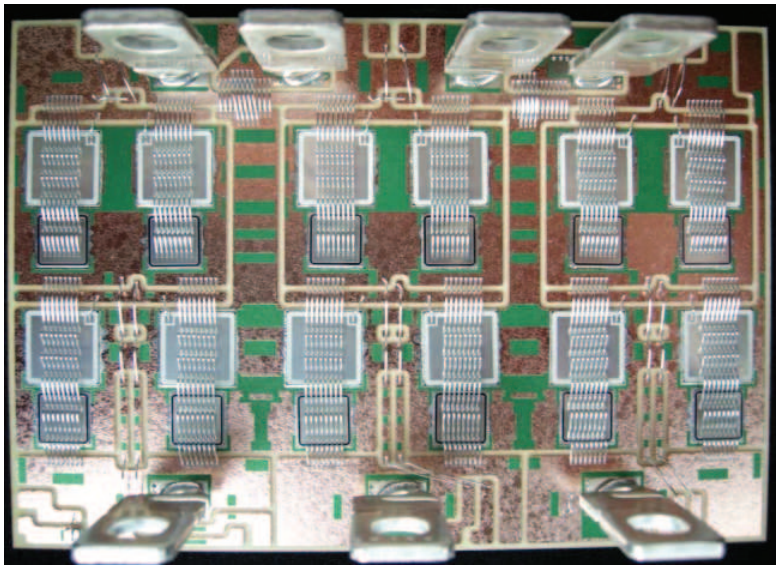


Figure 2.5.9 Large DBC substrate (115 mm x 80 mm), equipped with the chips of a 350 A / 1200 V IGBT three-phase bridge and angle connectors

What is also important is that the ceramic substrates are not completely rigid, but can be bent a little without breaking. This ensures that, when pressure is applied, the substrates can properly adapt to heat sinks that are not ideally even. The crucial point here is that insulating substrate is not pressed onto the heat sink at the corners only but at many different points, e.g. in the centre and along the periphery, and also next to and in between the chips. This ensures good adaptation of the DBC substrate to the heat sink surface. As a result, the thermal paste - which makes the contact with the heat sink - may be much thinner (about 20…30 µm) than for conventional modules which are only pressed onto the heat sink with screws at the corners or at the edges. For these standard modules, thermal paste thickness must be 70 µm to 120 µm in order to prevent air bubbles between the module and heat sink surfaces which will never be ideally plane. This much thinner thermal paste layer results in a lower static thermal resistance in SKiiP® modules than in standard modules. The transient resistance of SKiiP® modules, however, is slightly higher in the time range between 0.1 s and 1 s.

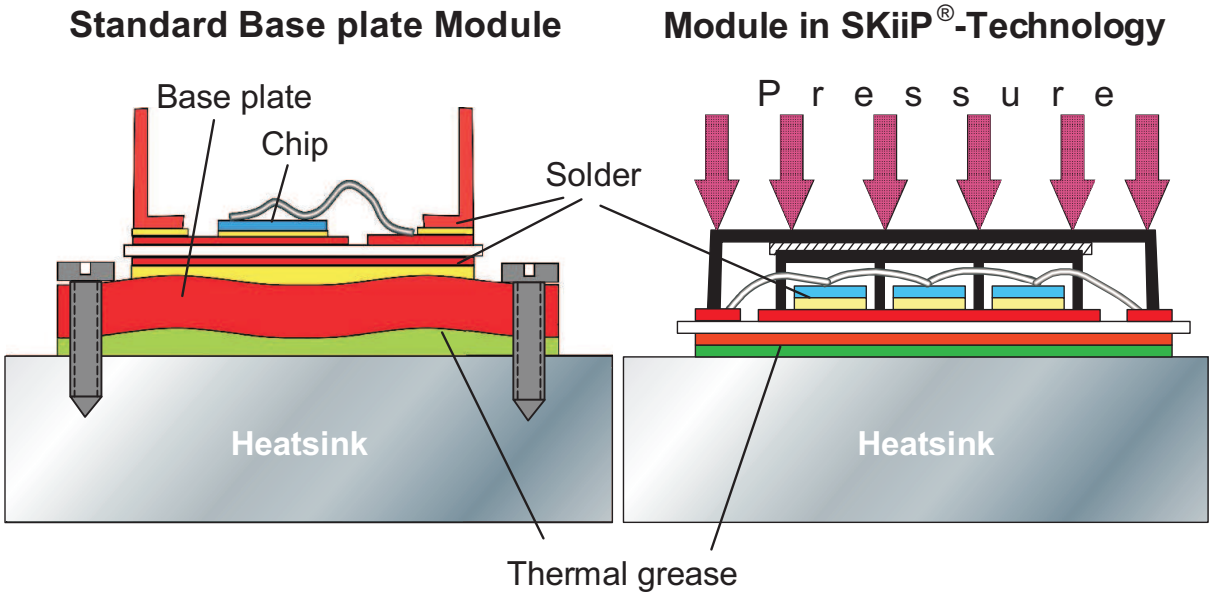


Figure 2.5.10 Base plate bending and thermal paste requirements regarding thickness for a conventional module (left) and a module in SKiiP® technology (right)

2.5.2 Functions and features

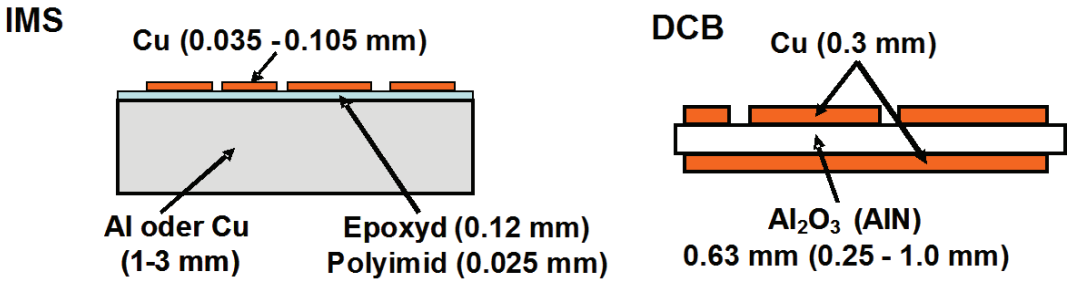
2.5.2.1 Insulation

Plastic materials are used as an insulating material for components with electrical isolation between live parts and the base plate (semiconductor modules); ceramic insulators are used in the higher power range. Plastic materials, usually thin layers of polyimide or epoxy, have a much higher thermal resistance than ceramic insulators. One example of plastic insulation is IMS substrates (**I**nsulated **M**etal **S**ubstrates, Figure 2.5.11). IMS substrates are used mainly in the low-cost / low-power range and are charaterised by direct contact between the insulating material and the module base plate. The upper copper layer is attached as a foil and structured by etching. The main advantages of IMS technology are low costs, filigree track structure (possible integration of driver and protection devices) and high mechanical substrate stability.

One disadvantage of this very thin insulating layer, however, is the relatively high coupling capacitances towards the mounting surface. Furthermore, the extremely thin upper copper layer only provides for comparably low heat spreading. This can be improved by adding metallised heat spreading layers underneath the chips or Al particles to the insulation layer.

DBC substrates (**D**irect **B**onded **C**opper) are most commonly used for ceramic insulation. Here, the insulator is often made of aluminium dioxide Al_2O_3; the double-sided metal layers are made of copper. The metal / ceramic connection is made at temperatures of just above 1,063°C with the aid

of low-viscosity copper / copper oxide eutectic. AMB ceramics (**A**ctive **M**etal **B**razing) are almost equivalent to DBC substrates. These are produced by soldering copper or aluminium foils on to the aluminium oxide or aluminium nitride (AIN) ceramic with the aid of titaniferous hard solder. The track structure for the module circuitry is etched into the upper copper surface. The underside of the DBC ceramic substrate is soldered to the module base plate or directly pressed onto the heat sink surface by means of suitable case designs.



a) b)

Figure 2.5.11 Comparison of IMS (a) and DBC (b) structure

The advantage of ceramic substrates is that their thermal expansion coefficients are very close to that of silicon. By way of contrast, IMS expansion is determined by the base plate material (copper or aluminium), resulting in high tension between substrate and soldered-on silicon chip when temperature changes occur (chapter 2.7). The move towards ever higher voltage ranges places increasing demands on IGBT modules to provide high insulation voltages and a high partial discharge stability. Dielectric strength and partial discharge stability are dependent on the thickness, the material and homogeneity of the chip bottom insulation, the module case and filling materials and sometimes on the chip arrangement, too. Present-day transistor modules are subject to insulation test voltages between 2.5 kV_{eff} and 9 kV_{eff}, verified for every module during production.

Figure 2.5.12 shows the maximum attainable insulation voltages for different insulating substrates when using common standard substrate thicknesses.

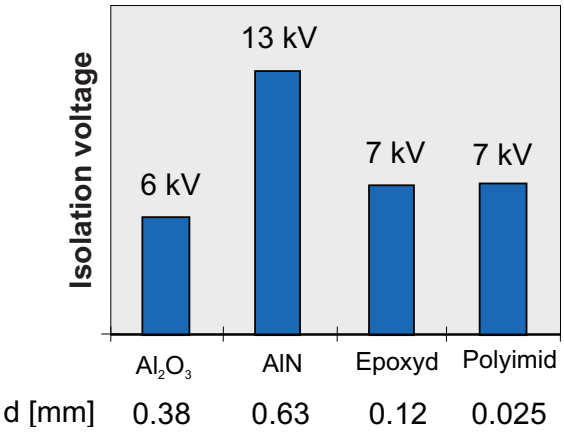


Figure 2.5.12 Insulation voltages for different insulating substrates

2.5.2.2 Heat dissipation and thermal resistance

In order to utilise the theoretical current capability as far as possible, power losses have to be optimally conducted through the connection layers - and for modules also through the insulation layers - to the heat sink. The quality of dissipation for the heat losses P_{tot} generated during forward on-state and blocking state and during switching is expressed by the temperature difference

$$\Delta T_{j\text{-}s} = T_j - T_s$$

between chip (chip temperature T_j) and heat sink (heat sink temperature T_s) which is as low as possible. It is quantified as the (stationary) thermal resistance $R_{th(j\text{-}s)}$ or (transient) thermal impedance $Z_{th(j\text{-}s)}$.

$$R_{th(j-s)} = \frac{T_j - T_s}{P_v}$$

In the past, a "v" for "virtual" preceded the index of the junction temperature (T_{vj}), since "the" junction temperature does not exist, but merely an equivalent measurement or computed value.

For modules with base plate, the value for the outer thermal resistance or impedance is specified as $R_{th(c\text{-}s)}$ or $Z_{th(c\text{-}s)}$ (base plate to heat sink) and is distinguished from the inner value $R_{th(j\text{-}c)}$ or $Z_{th(j\text{-}c)}$ (chip to base plate):

$$R_{th(j\text{-}s)} = R_{th(j\text{-}c)} + R_{th(c\text{-}s)}$$

$$Z_{th(j\text{-}s)} = Z_{th(j\text{-}c)} + Z_{th(c\text{-}s)}$$

For modules without base plate, it is not possible to measure these values separately without seriously interfering with the thermal system. For this reason, only the total resistance between chip and heat sink is specified for these components. Low-power components are also specified with reference to the ambient temperature. Figure 2.5.13 shows a schematic of a module with base plate. The rating equation for thermal resistance

$$R_{th} = \frac{d}{\lambda \cdot A}$$

(d = material thickness, λ = heat conductivity, A = heat flow area)

can be used to deduce which inherent module quantities influence the heat dissipation capability or $R_{th(j\text{-}s)}$ and $Z_{th(j\text{-}s)}$.

- Chip (area, thickness, geometry and layout)
- DBC substrate design (material, thickness, structure on the substrate upper)
- Material and quality of the chip/substrate connection (solder, adhesive, ...)
- Presence of a base plate (material, geometry)
- Rear soldering of the substrate to the base plate (material, quality)
- Module assembly (surface qualities / thermal contact to heat sink, thickness and quality of thermal paste or thermal foil)

In conjunction with the equation for thermal capacitance:

$$C_{th} = s \cdot V$$

the elements of the thermal equivalent circuit can be calculated from the geometry layer by layer (s = heat storage characteristic, V = volume). Heat spreading must be factored in to area and volume calculations. A conflicting effect that has to be considered is mutual chip heating in complex power modules (thermal coupling). The calculated theoretical thermal resistance value will often be lower than the actual measured value. The reason for this often lies in the uncertainties observed in heat spreading and thermal coupling, as well as impurities at the border layers which have not been considered in the modelling. For this reason, this type of modelling is not particularly well suited to complex power electronic systems. Normally, the computed R_{th} values are adjusted to the measured total of R_{th} with the aid of a weighting factor.

Material	Heat conductivity λ [W/(m*K)]	Heat storage characteristics [kW/(m³*K)]	Thermal expansion coefficient α [10^{-6}/K]
Silicon	148	1650	4.1
Copper	394	3400	17.5
Aluminium	230	2480	22.5
Silver	407	2450	19
Molybdenum	145	2575	5
Solders	~70	1670	15 – 30
Al_2O_3-DBC	24	3025	8.3
AlN DBC, AlN-AMB	180	2435	5.7
AlSiC (75% SiC)	180	2223	7

Table 2.5.4 Heat conductivity, heat storage characteristic and thermal expansion coefficient for materials that are frequently used for packaging

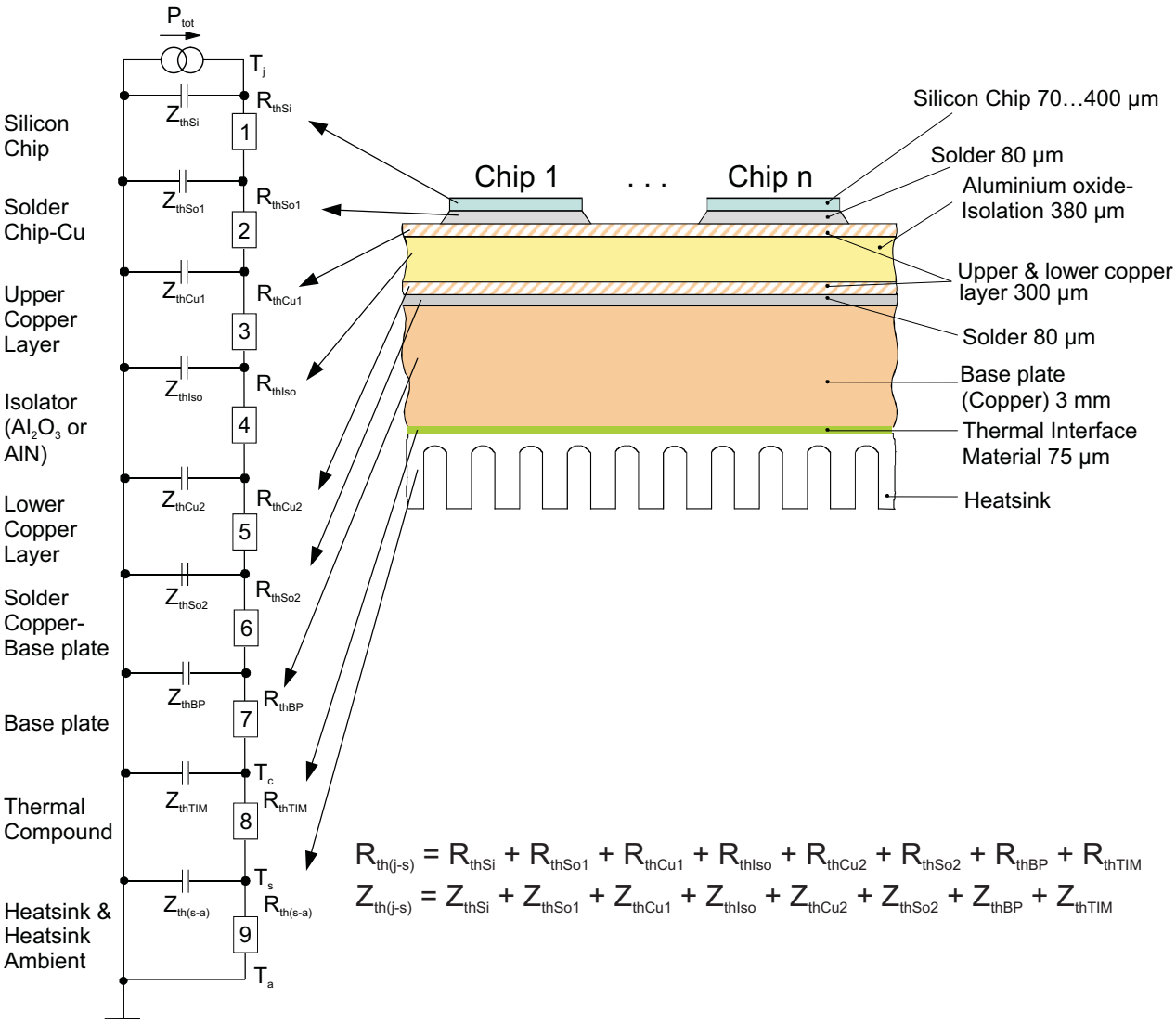


Figure 2.5.13 Basic structure of a power semiconductor module and physical modelling of the thermally relevant layers

In combination with the cooling and ambient conditions, $R_{th(j-s)}$ determines the maximum module ratings for thermal losses. The development of power semiconductor modules is therefore always associated with the reduction of the number of layers, the reduction of layer thickness (0.63 mm → 0.38 mm for ceramics) and the use of materials with improved thermal conductivity (AlN, graphite). This development, however, is limited by insulation voltage and mechanical strength requirements.

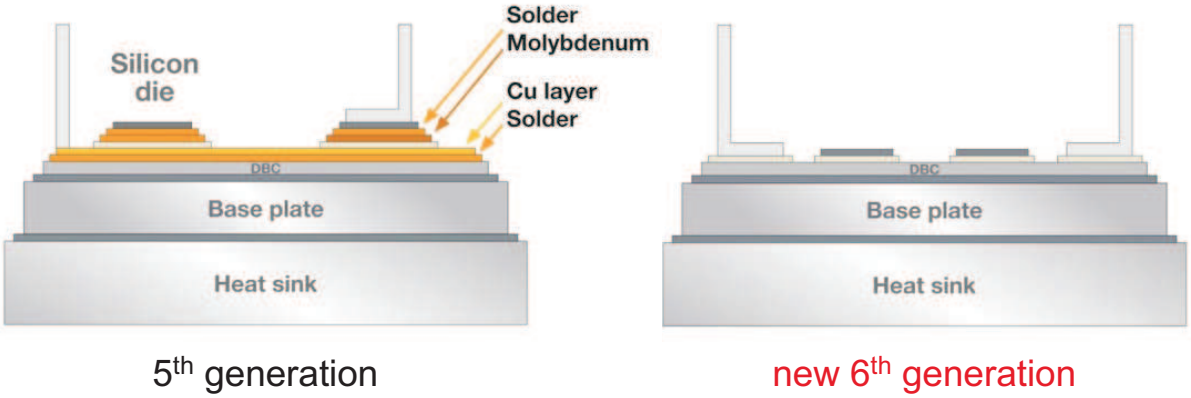


Figure 2.5.14 Development of Semipack rectifier bridges: thermal resistance reduced by the omission of layers

Heat spreading

Figure 2.5.15 shows a computed value for the temperature curve in the individual layers of a module without base plate with undisturbed heat spreading. Here, the thermal conductivity of the individual layers and the heat flow area has been taken into account. Consequently, enlarging this area by improving heat spread would reduce the thermal resistance of the subsequent layer. Although a thinner copper layer would lead to a lower thermal resistance in a one-dimensional model, in the real three-dimensional space R_{th} would in fact increase as a result of reduced heat spreading. Thicker metal layers in the DBC substrate provide thermal advantages; however, they also increase thermal stress within the substrates.

Heat spreading depends not only on the material properties of the given layer, but also on those of the subsequent layer. A sufficiently high potential (temperature difference) must build up so that the heat flow can overcome a poorly conducting layer. This will then result in increased transverse heat conduction (heat spreading) in a layer with good thermal conductivity located above.

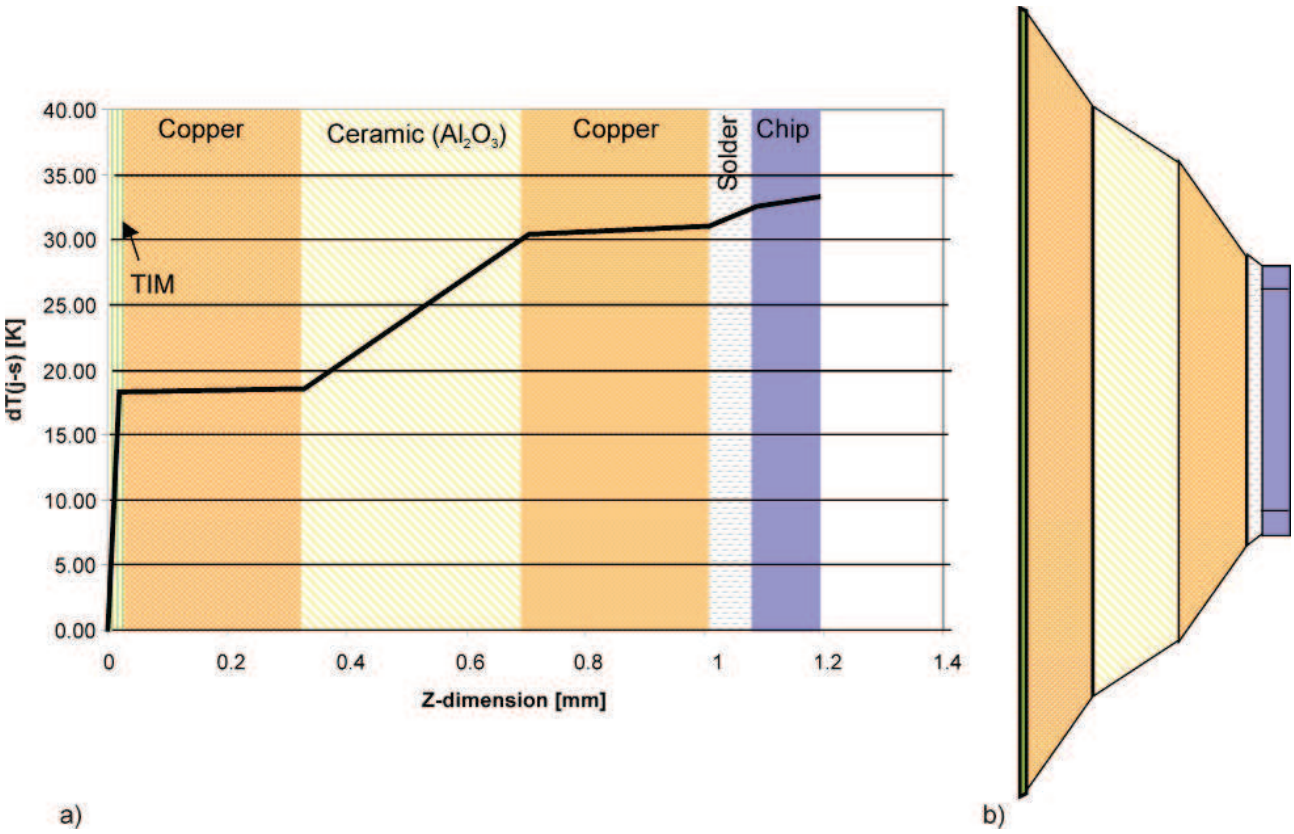


Figure 2.5.15 Layer structure with heat spreading (b) and typical temperature profile (a) for a module without base plate (0.38 mm Al_2O_3ceramic, 25 µm thermal paste, TIM)

A reduction in thermal resistance could be obtained using materials with particularly good transverse thermal conductivity, whereas solutions such as "Silicon on Diamond SOD" will probably continue to be reserved for niche markets [34].

Proportion of thermal resistance caused by the layers

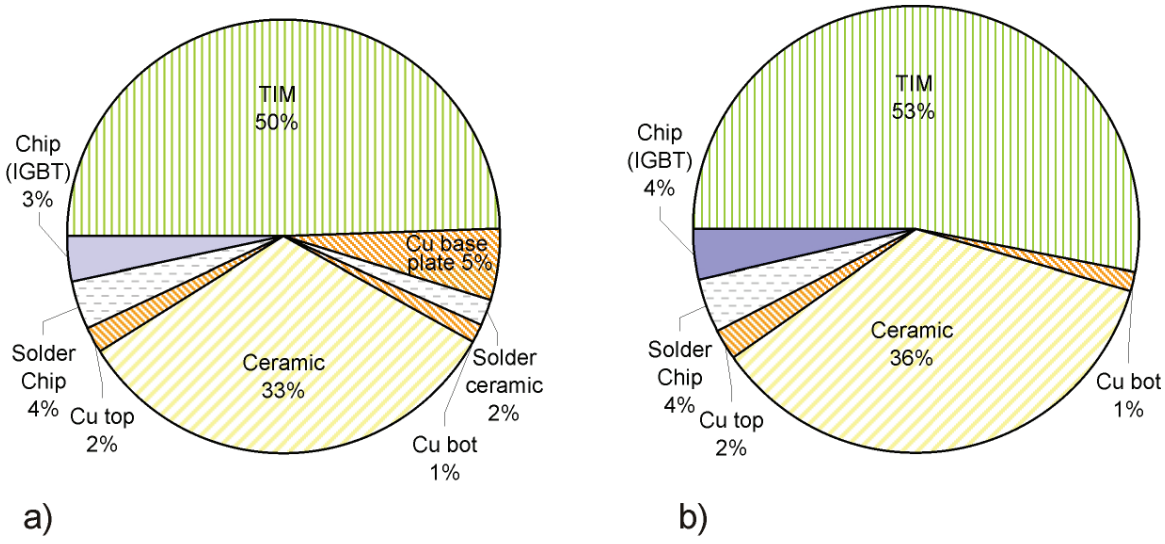


Figure 2.5.16 Influences on the internal thermal resistance of a 1200 V power module, chip surface 9 mm * 9 mm: a) for DBC substrates (Al_2O_3) on Cu base plate, 100 µm TIM; b) for DCB substrates (Al_2O_3) without Cu base plate, 25 µm TIM

Figure 2.5.16 illustrates the shares for the aforementioned variables affecting $R_{th(j-s)}$ for the most common module layouts described in chapter 2.5.4 using Al_2O_3 Direct Bonded Copper (DBC) substrates with or without copper base plate.

In both cases, the biggest share of the thermal resistance (approx. 50%) from chip to heat sink is caused by the thermal paste (TIM – **t**hermal **i**nterface **m**aterial). This seems strange at first, since the base plate promises better heat spreading and thus a lower influence from the thermal paste layer. However, base plates never come into full contact with the heat sink across the entire surface owing to inevitable bending due to the ceramic soldering. This effect is known as the bimetal effect and occurs when two materials with different coefficients of thermal expansion are joined by soldering. It cannot be compensated for even with pre-bent base plates. Bending is not constant but varies over time, since the solder flows, thus relieving some of the stress. Bending also changes as a function of the application temperature, even an ideally shaped base plate would only rest on the heat sink at one temperature point.

Base plates that are bent in this way are only pressed onto the heat sink by means of low-force pressure screws positioned at the edges (Figure 2.5.18). This is why much thicker layers (typically 100 µm…200 µm) of the poorly conducting thermal paste are needed [35]. This problem becomes ever more critical the bigger the module is. In Figure 2.5.17, the four nests of the soldered DBC substrate are clearly visible. Sometimes attempts are made to reduce this bending using split base plates, where each DBC segment is allocated a separate base plate segment [36].

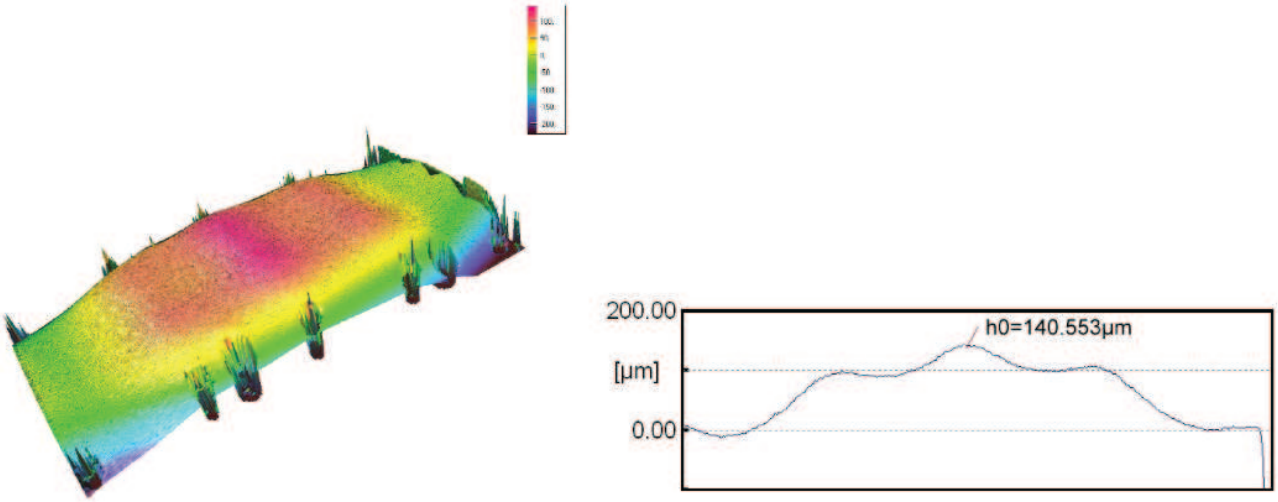


Figure 2.5.17 Measurement of PrimPack FF650R17IE4 base plate by Infineon

Despite the high thermal conductivity of the material (Cu: λ = 393 W/(m*K)) the base plate also accounts for a considerable share of the module thermal resistance due to its thickness (2.5...5 mm). Thinner base plates will only reduce this share to a limited extent, since the effect of reducing base plate thickness is decreased spreading of the temperature field and thus a reduction of the area through which the heat passes under the chips. Modules in the upper performance range (>= 1000 A) use AlSiC base plates in conjunction with AlN ceramics. This is necessary in order to match the thermal expansion coefficients of the ceramic and base plate (α: AlN 5.7 ppm, AlSiC 7 ppm, Cu 17 ppm → also see chapter 2.7 Reliability). The poorer thermal conductivity of AlSiC (λ = 180 W/(m*K)) compared to copper increases the thermal resistance, reducing heat spreading.

As mentioned a number of times before, omitting the base plate has proven to be the most effective way of eliminating the thermo-mechanical stress between base plate and ceramic, as well as bending. The lack of heat spreading in the copper material is partially compensated for by the eliminated resistances of base plate and rear soldering. Much more important, however, is that such layouts make a tighter seat of the chip on the heat sink possible. This permits a drastic reduction of the thermal paste layer to 20…30 µm. To this end, pressure elements press the DBC substrate onto the the heat sink at many points, close to the chips.

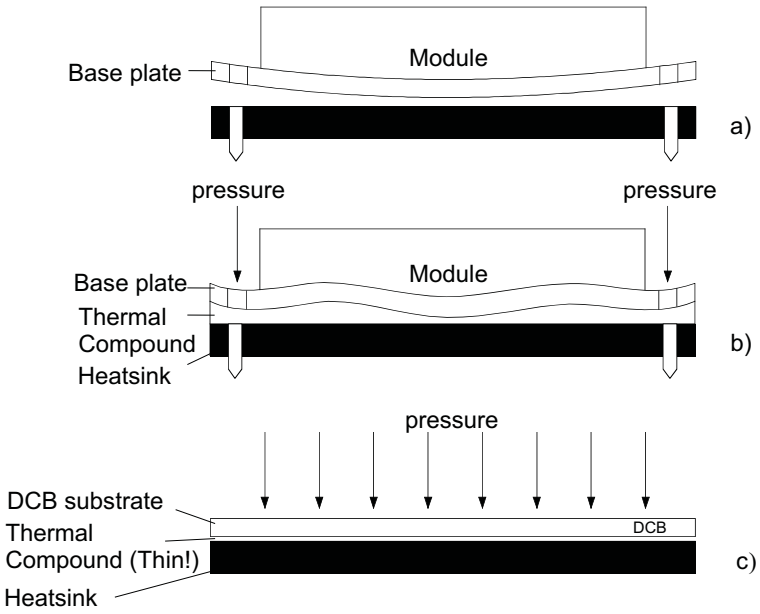


Figure 2.5.18 Problems arising through contact of power module to heat sink
a) Module with base plate prior to assembly (base plate with convex bending)
b) Module with base plate after assembly (highly exaggerated!)
c) DBC module without base plate (e.g. SEMITOP, SKiiP, MiniSKiiP)

Module insulation accounts for the biggest part of the internal thermal resistance. The alternative, however - for example external insulation by means of foil - would be even worse. Compared to today's standard type Al_2O_3 with a purity of 96% (thermal conductivity λ = 24 W/(m*K)), improvements can be achieved by using highly pure Al_2O_3 (λ = 28 W/(m*K)) or aluminium nitride (AlN, λ = 180…200 W/(m*K)), for example. The far better thermal conductivity of AIN reduces the module thermal resistance considerably, meaning that amperage ratings are higher. Unfortunately, this is true for the costs as well. The use of modules with improved thermal conductivity is often dispensed with for cost reasons. For this reason, AIN is largely preferred for modules with high insulation voltages (thicker insulating ceramics), since increased dielectric strength plus better thermal conductivity can be utilised at the same time.

Solder connections between chip and substrate - and (if applicable) substrate and base plate - also contribute a little to the thermal resistance. Omitting the base plate or replacing these layers by a thinner, sintered silver layer boasting better thermal conductivity could even half this share. The thermal resistance share for metal substrate areas depends mainly on the structure of the upper copper area, which is used as chip carrier and internal electrical connection system for the module. While the lateral heat flow in the copper substrate layer on the heat sink is virtually unaffected, heat spreading is limited by the geometric dimensions of the copper layers under the chips. For example, in [37] it was determined that for a 42 mm² chip on an Al_2O_3 DBC ceramic substrate, the value $R_{th(j-c)}$ increases by around 15%, if the copper area equals the chip area, as compared with a case with unimpaired heat spreading.

The thermal resistance accounted for by the silicon chips increases in proportion to the thickness of the chips, which is determined by the forward blocking voltage and the chip technology. The size of the chip areas also determines the area through which the heat passes between chip and base plate or heat sink.

Chip size effects

In accordance with the equation for thermal resistance, R_{th} should decline in inverse linear proportion to the chip area. In real layouts, however, an increase in the chip area-to-circumference ratio will reduce the relative temperature spread. If a chip sized 9 mm x 9 mm is divided into 9 segments, the inner segment with an edge length of 3 mm x 3 mm will have no room for heat spreading. This effect results in the dependency of the thermal resistance $R_{th(j-c)}$ on the chip area A_{Chip} as shown in Figure 2.5.19.

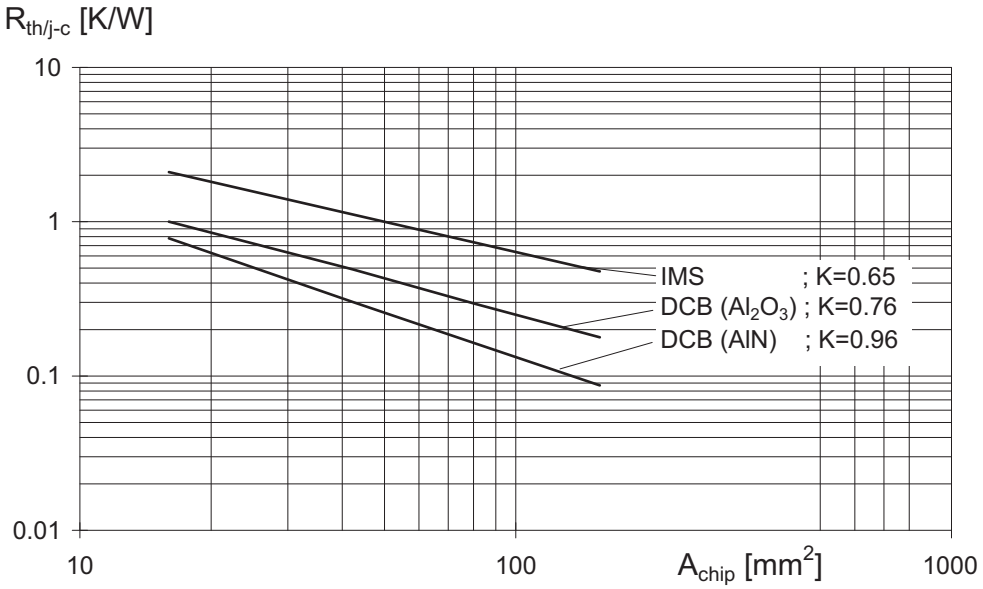


Figure 2.5.19 Dependency of thermal resistance $R_{th(j-c)}$ on chip area A_{Chip} [37]

For high substrate thermal conductivity (e.g. AlN DBC) this effect is less marked. The poorer the heat conductivity of the ceramic substrate, the more marked the non-linearity of the $R_{th(j-c)}$ dependency will become. This correlation also applies to the influence of module assembly on the heat sink, which is done using thermal paste or thermal foils. The relatively low thermal conductivity of λ = 0.8 W/m*K (example: Wacker P12) for this layer causes a thermal transient resistance $R_{th(c-s)}$ between module base plate and heat sink. Besides the thickness d of the thermal paste layer, the relative share of $R_{th(c-s)}$ in the thermal resistance $R_{th(j-s)}$ between chip and heat sink will also rise if chip area is enlarged.

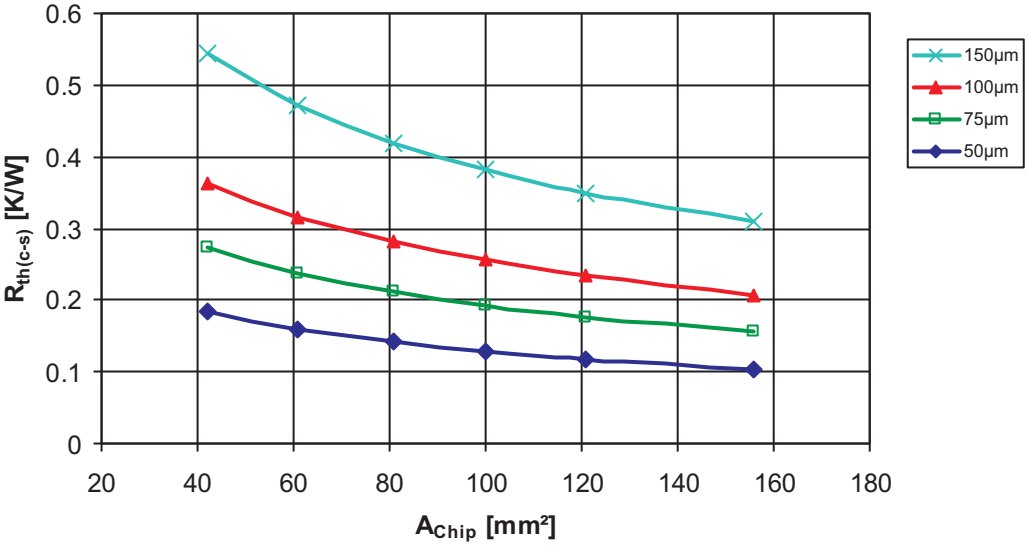


Figure 2.5.20 $R_{th(c-s)}$ of a base plate module in relation to a single chip as a function of the chip area and thickness of the thermal paste layer for undisturbed heat spreading

Due to the heat spreading effect, the thermal resistance will only be reduced by 25% if the chip area is doubled (100 µm: 120 mm² = 0.235 K/W; 60 mm² = 0.315 K/W); according to the dimensioning equation for R_{th}, a 50% reduction would be expected. Figure 2.5.20 demonstrates the huge influence that optimum mounting technology has on thermal properties (thin thermal paste layer). This figure also shows that thermal limits prevent the use of bigger chips for enhanced power output. For this reason, the maximum chip sizes currently used in power modules are between 30 mm² (IMS) and 150 mm² (Al_2O_3 DBC). Higher power output can be reached by distributing heat sources (parallel connection of as many chips as possible).

Thermal coupling

For the sake of small module geometry, more or less intensive chip thermal coupling has to be accepted if transistor and diode chips are to be positioned close to one another. According to calculations in [37], an increase in the chip temperature caused by thermal coupling of heat flow, e.g. on Al_2O_3 DBC, can always be expected if distance a of the chips equals

$$a = 0{,}6 \cdot \sqrt{A_{Ch}}$$

For the example using 36 mm² chips in Figure 2.5.21 this would be true for a distance of 3.6 mm or above. This data may serve as a guideline, but depends on the heat spreading layers in the module in individual cases.

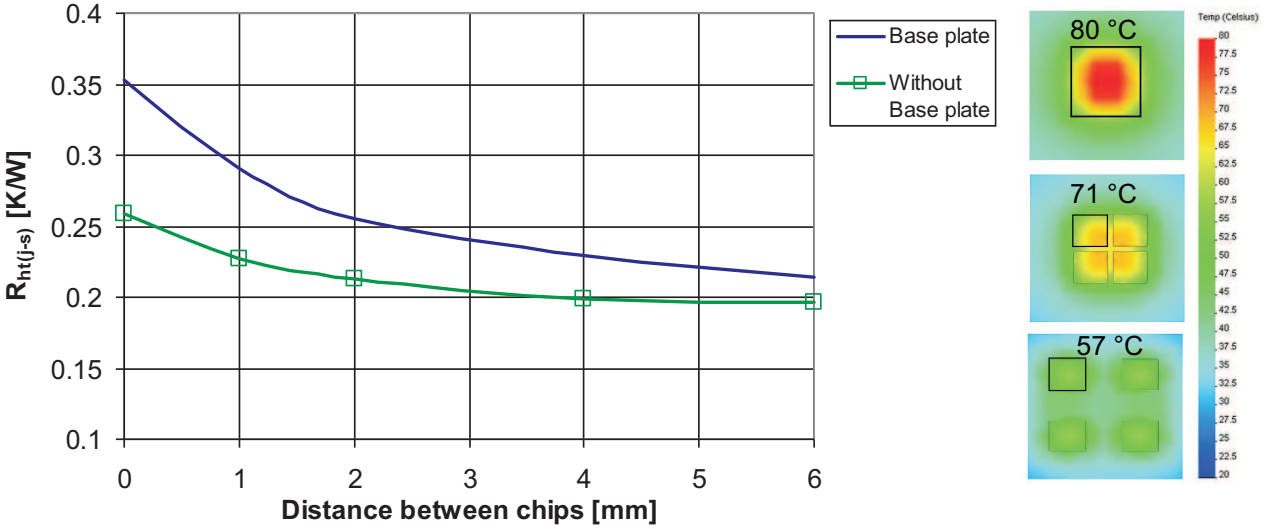


Figure 2.5.21 Thermal resistance $R_{th(j-s)}$ of four 36 mm² chips as a function of the chip distance; (thermal paste thickness: with base plate 100 µm, without 25 µm), right: simulation of chip temperatures assuming same power loss and chip area but increasing distance (0 mm, 1 mm, 6 mm)

Depending on the closeness of the chips, thermal coupling
- will appear on the upper side of the DBC metallisation (e.g. fully equipped modules with maximum rated current in case class)
- over the base plate (e.g. IGBT + inverse diode of standard IGBT modules)
- over the heat sink

Thermal impedance

As already mentioned above, in addition to the static behaviour of power modules, the dynamic thermal behaviour of power modules, which is charaterised by the thermal impedance Z_{th}, is also of major importance. Figure 2.5.22 shows the development of thermal impedances $Z_{th(j-c)}$ over time for a module containing an Al_2O_3 DBC substrate for different chip areas.

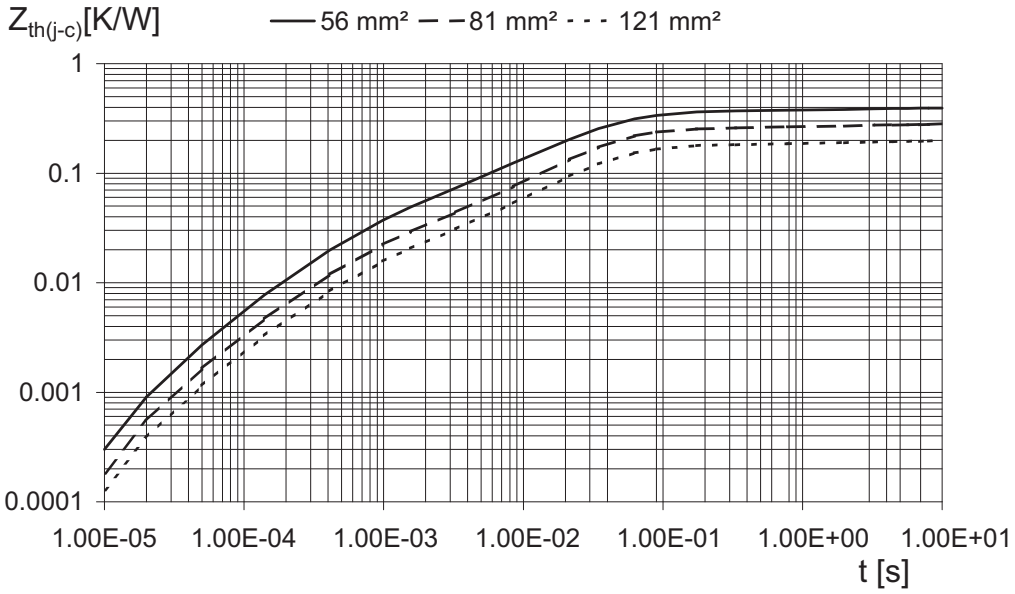


Figure 2.5.22 Time curve of thermal impedances $Z_{th(j-c)}$ of a module with Al_2O_3 DBC substrate for different chip areas [37]

For the given module structure, the Z_{th} curves for different chip areas may be shifted against one another, i.e. the absolute values will change in proportion to the chip area, however without influencing the time constants of the exponential functions. Consequently, thermal impedances for different chip areas, like thermal resistances, may be calculated in a given structure with the aid of the following equation:

$$Z_{th(j-c)2} = Z_{th(j-c)1} \cdot \frac{R_{th(j-c)2}}{R_{th(j-c)1}}$$

Thermal impedances of modules with or without a base plate are similar as long as heat build-up takes place inside the chip and the DBC substrate (Figure 2.5.23). For times > 100 ms both curves differ over time. While the base plate module has thermal advantages in the time range up to 1…2 s owing to the heat storage capability of the copper plate, the module without base plate has advantages for longer periods owing to the reduced R_{th} value.

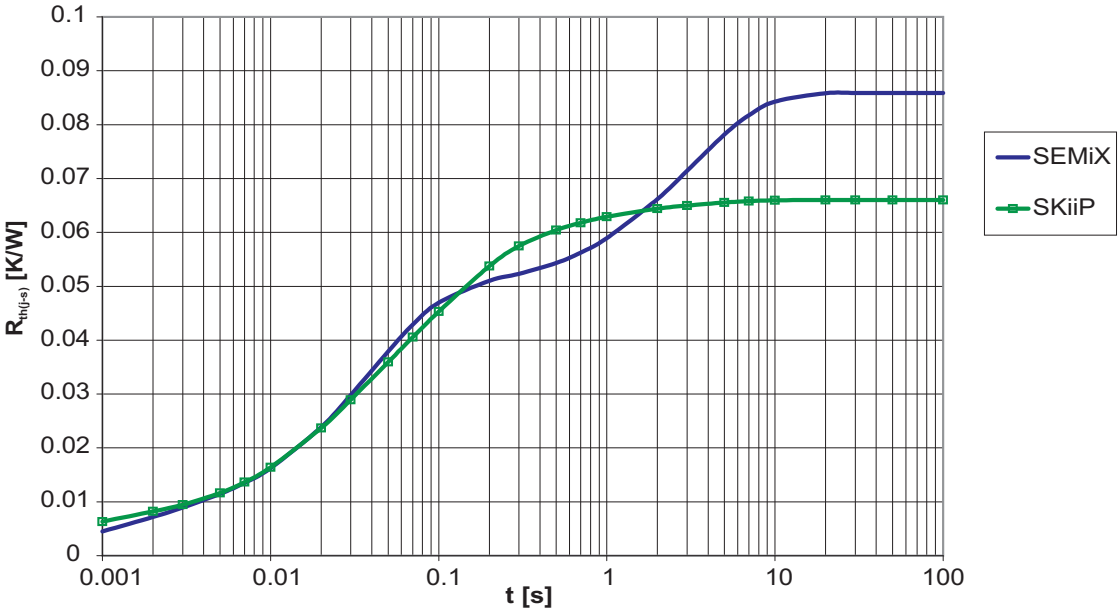


Figure 2.5.23 Comparison of thermal impedances of a 600 A / 1200 V module with base plates (SEMiX4) and without base plate (SKiiP4); reference point: drill hole in the heat sink 2 mm below the surface

2.5.2.3 Power cycling capability

Power cycling, especially at duty cycle operation, e.g. in traction, elevator and pulse applications, will subject the internal connections in a module to thermal cycling, such connections being:
- Bonded connections
- Rear chip soldering
- DBC / base plate soldering
- And substrate lamination (Cu on Al_2O_3 or AlN)

The different length expansion coefficients of the layers cause thermal stress during production and operation, which will eventually lead to material fatigue and wear and tear; module life (number of possible switching cycles) is reduced in proportion to the rising amplitude of the chip temperature fluctuation during these cycles.

Failure mechanisms, the quantitative correlation between module lifetime and temperature, current carrying capacity and time, as well as measures taken to increase module lifetime are described in chapter 2.7.

2.5.2.4 Current conduction to the main terminals

Improved semiconductor properties (chip shrinkage) result in ever higher current ratings and power densities for the same module area. The terminals of older standard IGBT packages, in particular, are now reaching the limits of their current carrying capacity. This partially calls for current limiting due to terminal heating (specification of an $I_{t(RMS)}$ = maximum current flowing through the terminals). Losses in the terminals can be calculated with the aid of the parameter $r_{cc'-ee'}$. These occur in addition to the chip losses and are normally not negligible. A SEMITRANS 3 module ($r_{cc'-ee'}$=0.5 mΩ) , for instance, would produce terminal losses of approx. 80 W at 400 A.

$$P = I_{rms}{}^2 \cdot r_{cc'-ee'} = 400A^2 \cdot 0{,}5m\Omega = 80W$$

The current carrying capacity is particularly low for high-bonded terminals which are compound-filled in packages (Econopack), since in this case there is only a poor thermal connection to the DBC substrate. An advantage of this technology, however, lies in the mechanical connection in the case. This makes the terminals more robust and resistant to external forces and moments (such as torque and bending moments).

Soldered angle connectors or solder pins are in direct contact with the DBC substrate, thus displaying better heat dissipation. The disadvantage of these soldered connectors is the more complex production process ("preform soldering" or second soldering with particular chip requirements as regards soldering capability). Users will notice a higher susceptibility to mechanical and thermo-mechanical stress. Examples of this are the standard IGBT modules in 63 mm and 34 mm packaging (SEMITRANS) or the SEMiX family.

In spring contacts, the high specific resistance of the spring material limits the amperage; higher amperages require parallel spring connections (e.g. MiniSKiiP with ca. 20 A per spring). Springs have good thermal and electrical contact thanks to the quasi-hermetically sealed metal-to-metal contact.

Large-area pressure contacts, such as those found in disc cells, are ideal contacts. Pressed angle connectors, however, also provide excellent thermal and electrical contact thanks to numerous pressure spots. They are non-wearing as regards thermo-mechanical stress. A disadvantage of this is that the outer mechanical forces have to be absorbed by the package. This means that a more complex design is needed, as is the case in SKiiP or SKiM63/93.

2.5.2.5 Low-inductance internal structure

With the example of a halfbridge module, Figure 2.5.24 shows the key internal parasitic inductances in a module resulting from the necessary connections between chips and to the module terminals (bond wires, internal connection wires, lugs and angle connectors).

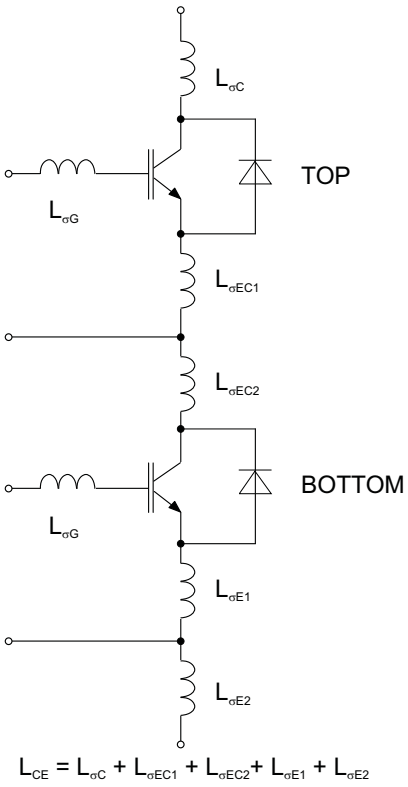


Figure 2.5.24 Parasitic inductances in a dual IGBT module
$L_{\sigma G}$: parasitic gate inductances
$L_{\sigma C}$: parasitic TOP-collector inductance
$L_{\sigma EC}$: parasitic connection inductance between TOP-emitter and BOTTOM-collector
$L_{\sigma E}$: parasitic BOTTOM-emitter inductance
L_{CE}: total parasitic inductance between TOP-collector and BOTTOM-emitter

Minimisation of these inductances, which induce overvoltages during turn-off and cause a slow-down of di/dt current rise during turn-on, as well as inductive coupling of control and power circuit, will directly affect the performance of power modules. Furthermore, parasitic inductances in modules with internally parallelled chips may cause uneven dynamic utilisation of the chips and oscillations between the chips. Chapter 5.4 will discuss the impact on the electrical behaviour in more detail.

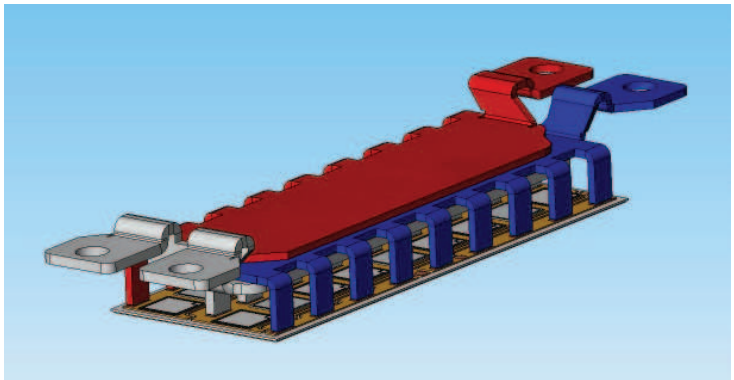


Figure 2.5.25 Internal busbar system of a SKiM93 (red :+DC, blue: –DC, grey: AC)

Possible design measures to reduce internal inductance are parallel current routing in the +DC and -DC terminal and parallel routing of load current paths. An example of such a design is shown in Figure 2.5.25. The internal busbar system ensures magnetic coupling of the main inductanc-

es $L_{\sigma C}$ and $L_{\sigma E2}$. During current commutation between +DC and -DC, the magnetic field needn't change much, which is commensurate with low inductance. The many parallel current paths leading to the individual chips reduce the inductances of the connection parts, which cannot be designed in "sandwich" constructions. The main share of the remaining inductance is generated by the external screw points. Here, overlapping current routes must be abandoned in order to ensure clearances in air and creepage distances at the outer terminals. Figure 2.5.26 shows a switching operation with voltages at different chip positions and the DC terminals. The internal voltage difference is 150 V, which enables an inductance from +DC to –DC of about 20 nH to be calculated for the measured rate of current rise. You can also see that barely any voltage differences exist between the individual chip positions, which indicates an extremely low inductance in the vicinity of the sandwich busbar system.

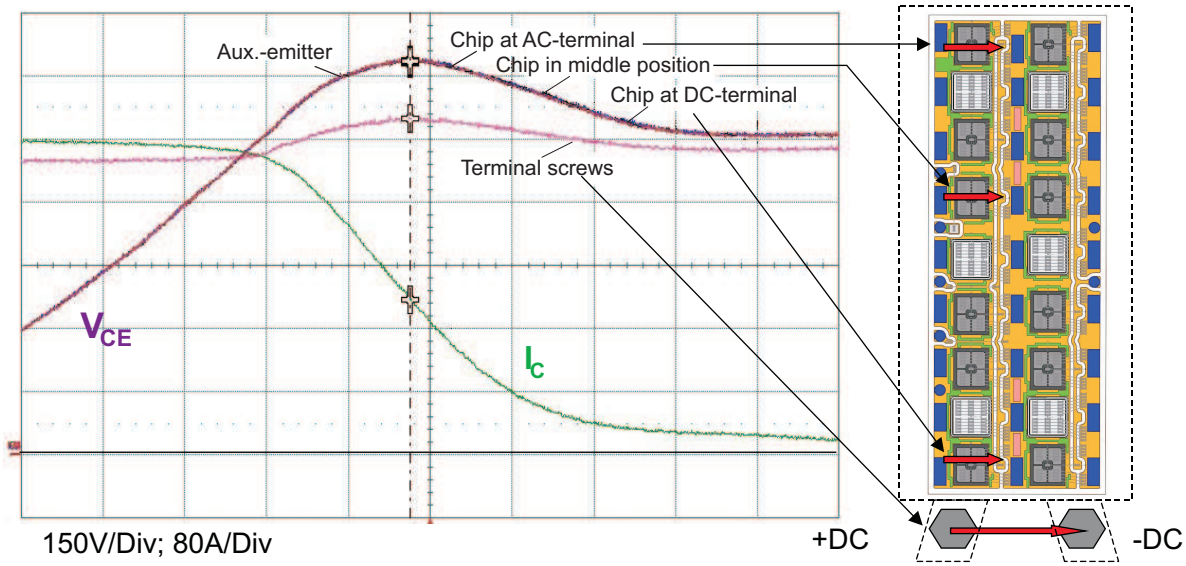


Figure 2.5.26 Overvoltage reading in the SKiM93 during turn-off at different chip positions and the outer terminals at 6.7 kA/µs, time scale = 20 ns/Div

For applications, the internal turn-off overvoltage is lost with respect to the maximum voltage to be utilised. Users must ensure that the turn-off voltages measured at the outer terminals plus the voltage drop over the internal inductances is always lower than the blocking voltage of the semiconductors. The auxiliary emitter terminal may be used to measure voltages for the "BOTTOM" switch. This terminal is closer to the chip and therefore provides a better picture of the turn-off overvoltage than the main emitter terminal (also see [AN1]).

2.5.2.6 Coupling capacitances

The short rates of rise of current and voltage within the ns-range that can be achieved in MOSFET and IGBT modules generate electromagnetic interference with frequencies well into the MHz range. For this reason, the parasitic elements that are typical in the internal and external propagation paths in the module exert considerable influence on the radio interference voltages generated. Suitable insulation materials, small coupling areas or conductive shields can reduce, for example, asymmetrical interference [38]. In addition to this, the internal connections in the module have to be structured such that malfunctions caused by outer stray fields or transformatory coupling into control lines are ruled out.

Another aspect is the "earth current", i.e. the current $i_E = C_E \cdot dv_{CE}/dt$ flowing through the normally earthed heat sink to the protective earth connector due to capacitance C_E of the insulating substrate as a result of the dv_{CE}/dt of the IGBT during switching. Capacitances can be calculated using the equation for plate capacitors:

$$C_E = \frac{\varepsilon \cdot A}{d}$$

d (thickness) Al_2O_3: 0.38 mm or 0.63 mm; AlN: 0.63 mm;
$\varepsilon = \varepsilon_0 \cdot \varepsilon_r = 9.1 \cdot 8.85e^{-12}$ F/m (Al_2O_3 and AlN);

The following shares of substrate area can be estimated for a halfbridge module:
- 40% "+DC"
- 40% "AC" and
- 15% "-DC"

The connection potential to earth and its amplitude when switched will depend on the earthing concept for the connected load. Suitable measures (e.g. Y-capacitors) must be taken to create a current path in the converter that closes a circuit close to the semiconductor; this must be done to ensure that current i_E does not flow through the controller and monitoring units. This earth current would be identified as a fault by a residual current protective device and may trigger this device. For installations where high leakage currents occur for functional reasons, special labelling requirements and mandatory minimum cross sections for the protective conductors exist (EN 50178, EN 61800-5-1).

Figure 2.5.27 compares the capacitances of the most common substrate materials in their standard thicknesses. The deviating dielectric constants and the standard thicknesses depending on thermal conductivity (thickest substrate material being AlN with 630 µm, thinnest substrate required in IMS structures, with 120 µm for epoxy insulation and 25 µm for polyimide insulation) result in different capacitances C_E and thus different limits for the maximum switching speed dv_{CE}/dt for a maximum permissible earth current i_E.

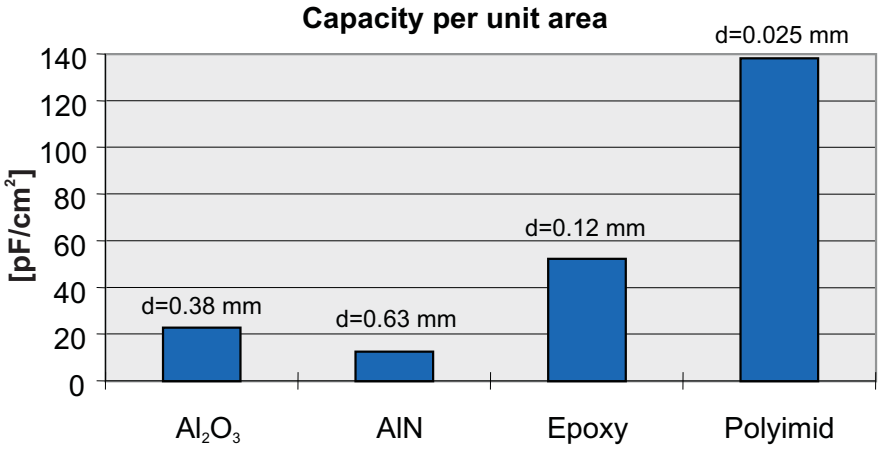


Figure 2.5.27 Capacitance per unit area for different insulating substrates

2.5.2.7 Circuit complexity

Optimal complexity cannot be defined in general. On the one hand, complex modules will reduce equipment costs and minimise problems encountered when several components are to be combined in one circuit (parasitic inductances, interference, incorrect wiring). On the other hand, increasing complexity restricts module usability, rendering modules less general-purpose (think production quantities). Testing will become more extensive and the costs per module will increase. As the number of integrated components and connections increases, modules will be more likely to fail and the amount of circuitry that will have to be replaced in the event of faults will increase. Driver, sensor and protection assemblies in modules have to meet considerable requirements regarding their thermal stability and electromagnetic compatibility.

Up to now, none of the following module configurations has gained acceptance as a "global standard" with respect to driver integration. The general-purposeness of power modules is greatly impaired by the integration of increasing driver functions; power modules are in fact becoming more and more like sub-systems. On the one hand, "intelligent" modules are aiming at real mass production markets (consumer, automotive); on the other hand, markets where many similar applica-

tions can be covered with innovative module systems consisting of similar basic units are also being targeted. In the latter case, despite inevitable redundancies, users can still profit from reduced system costs thanks to the synergies provided by module manufacturer.

Considering the arrangement of IGBT and diodes in the most commonly used power modules, the configurations shown in Figure 2.5.28 have managed to gain a strong footing, meeting the demands of most applications in power electronics and drive technology.

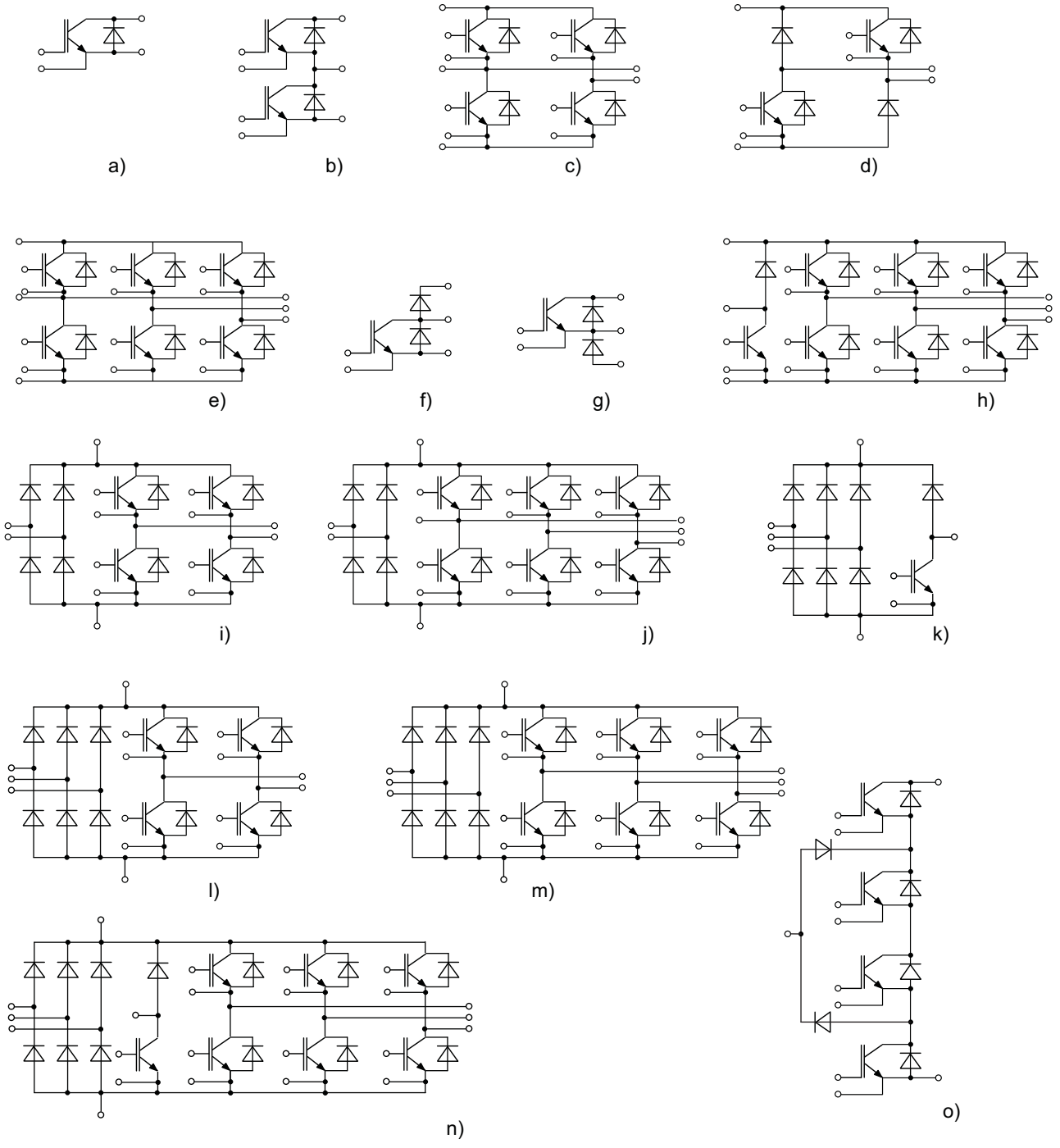


Figure 2.5.28 Important configurations for power modules with IGBT and diodes

To identify the circuit topologies shown in Figure 2.5.28, the SEMIKRON component designations contain the following letter combinations:

a) GA: single switch, consisting of IGBT and hybrid inverse diode (for MOSFET modules here and in the other configurations, mostly just a parasitic inverse diode). In case of external bridge circuits, the inverse diodes reciprocally act as freewheeling diodes.
b) GB: dual module (phase module, halfbridge module) consisting of two IGBT and hybrid diodes (freewheeling diodes)
c) GH: H-bridge with two arms consisting of IGBT and freewheeling diodes
d) GAH: asymmetrical H-bridge with two diagonal IGBT with hybrid inverse diodes (freewheeling diodes) and two freewheeling diodes across the other diagonal
e) GD: 3-phase bridge (sixpack, inverter) with three arms consisting of IGBT and freewheeling diodes
f) GAL: chopper module with IGBT, inverse diode and freewheeling diode on the collector side
g) GAR: chopper module with IGBT, inverse diode and freewheeling diode on the emitter side
h) GDL: 3-phase bridge "GD" with chopper "GAL" (brake chopper)
i) B2U diode rectifiers (to charge the DC link, semi-controlled B2H configurations with 2 thyristors at the +DC are often used instead of pure diode bridges) and IGBT H-bridge
j) B2U diode rectifier and IGBT inverter (three-phase bridge)
k) B6U diode rectifier and IGBT chopper "GAL" (IGBT and freewheeling diode on the collector side)
l) B6U diode rectifiers (to charge the DC link, semi-controlled B6H configurations with 3 thyristors at the +DC are often used instead of pure diode bridges) and IGBT H-bridge
m) B6U diode rectifier and IGBT inverter (three-phase bridge)
n) B6U diode rectifier, IGBT chopper "GAL" and IGBT inverter (three-phase bridge)
o) Phase module of a three-level inverter

2.5.2.8 Defined and safe failure behaviour in the event of module defects

In the event of module malfunction (e.g. caused by erroneous control signal), the total energy stored in the DC-link capacitors will be transferred, in a voltage-supplied circuit, for example, in the module case. Once the bond wires have melted, a large part of this energy is stored in the generated plasma, which may cause the module to explode. In conventional transistor modules this may cause circuit interruption, short-circuit of the main terminals or even bridging of the insulation path. The resultant high kinetic energy could distribute plasma and particles of the module case across the module surroundings. Module case designs must limit the dangers involved where possible and ensure safe module rupture (e.g. by defined particle distribution).

There are developments in this field that ensure, for example, that up to a defined energy level of 15 kJ, no particles will leave the module; even at 20 kJ the case might break, but no solid metal particles would be hurled into the surroundings [39]. IEC 60747-15 provides no definitions for a case rupture current or case rupture energy for power semiconductor modules.

2.5.2.9 Environmentally compatible recycling

Today’s power modules usually refrain from using toxic materials (e.g. BeO) and the number of materials used is kept as low as possible. Cases and other materials are flame-resistant and must not release toxic gas during burn-out (UL approval). In the recycling process, the module has to be dismantled and separated into metal and non-metal components. This must be easily achievable. For this reason, newer modules are cast solely using elastomeric materials (soft moulding). All semiconductor modules produced by SEMIKRON conform to RoHS.

2.5.3 Discrete devices

2.5.3.1 Small rectifiers

Small rectifiers often have a plastic case and solderable metal terminals. The semiconductor is connected to the terminals either by soldering on both sides or soldering on one side and wire bonding on the other. The device is predominantly cooled through the connecting wires or surfaces, to a lesser extent through heat dissipation from case to air. A differentiation is made between wired components and SMD components.

Wired components

As the name suggests, current is fed through the wires. In addition to this, a cooling lug which is electrically connected to the anode may help to improve cooling. Cooling devices are mounted by putting the connecting wires through metallised holes in the PCB and soldering them to the conductor tracks at the rear (Figure 2.5.29).

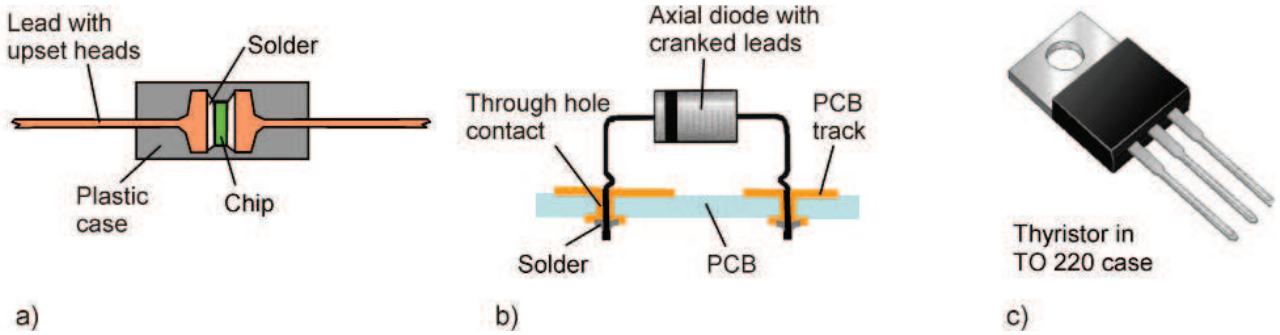


Figure 2.5.29 a) Structure of an axial diode (diagram); b) Mounting of axial diode on a PCB; c) Wired component with cooling and mounting plate

SMDs

SMD (**S**urface **M**ounted **D**evices are made in many different cylindrical or block-shaped designs. When SMDs are used, the PCB can be equipped very densely and, more importantly, on both sides. PCBs for SMD parts are often printed with solder paste and soldered in reflow technique after chip assembly. SMD parts on the underside of a mixed-assembly PCB are first glued to the underside and then wave-soldered together with the conventionally equipped parts (Figure 2.5.30).

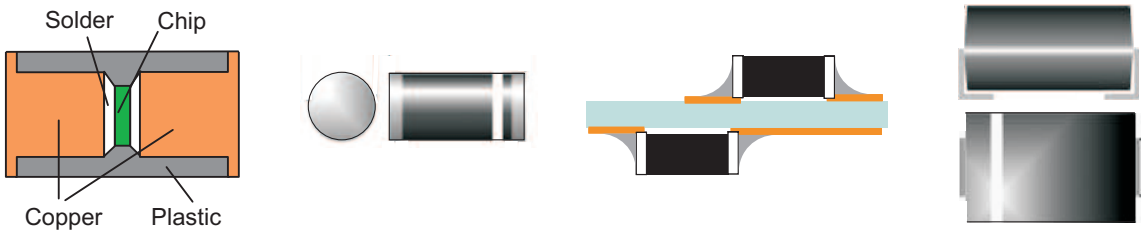


Figure 2.5.30 From left to right: Layout of a Metal Electrode Faces (MELF) diode, view of a MELF diode, double-sided PCB assembly of MELFs, block-shaped SMD diode

The thermal resistance of SMDs is far lower than that of wired components due to the more solid connection parts.

2.5.3.2 Stud-mounted diodes and stud thyristors

This design is charaterised by a solid copper hexagon with threaded stud which is used to screw the component onto a heat sink and discharge the heat generated at the chip. A glass or ceramic cap with a bushing for the cathode terminal ensures hermetical case sealing. Case parts are joined by welding or brazing. The chip is directly soldered onto the copper, or a disk made of molybdenum (thermal expansion coefficient $5*10^{-6}$/K) is soldered between the silicon and copper to prevent high mechanical tension in the semiconductor as a result of significant differences in the expansion coefficients for silicon ($4.1*10^{-6}$/K) and copper ($17.5*10^{-6}$/K) (Figure 2.5.31).

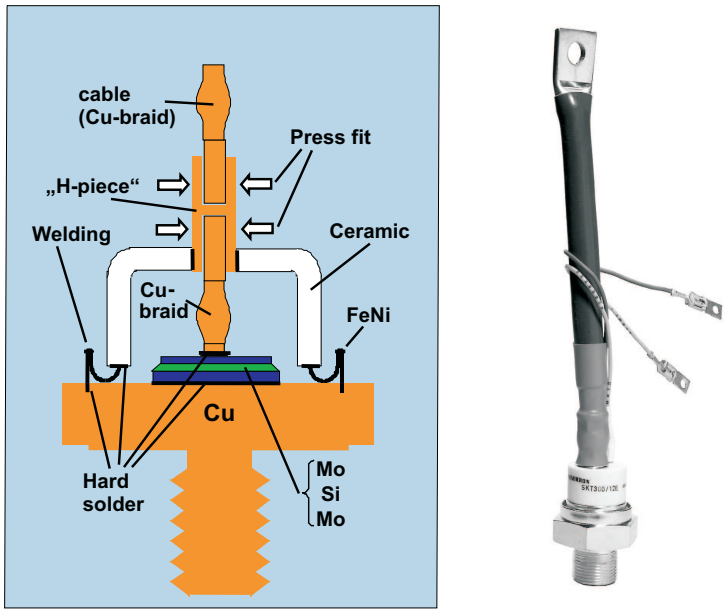


Figure 2.5.31 Sectional view of a stud-mounted diode and example of a stud thyristor

Stud-mounted diodes and thyristors are very reliable and robust, last not least due to their hermetically sealed cases. Thanks to the close thermal coupling of the active component with a solid copper part, transient and thermal resistances are very low. The disadvantage is that the heat sink is not insulated but connected to the anode.

2.5.3.3 Disk cells

Disk cells are also hermetically sealed components, but can be cooled from one or both sides. When two-sided cooling is applied, the thermal resistance is about half as high as that of the same silicon chip in a screw-mounted case. For two-sided cooling, however, two heat sinks and a clamping device are required. Disk cells are pressure-bonded components, meaning that the semiconductor is not connected to the connection parts by metallurgical joining but by means of pressure. Pressure contacts are extremely reliable and durable parts, since there are no solder layers which might show fatigue during frequent temperature cycling. The silicon chip is often joined with a molybdenum disk by means of aluminium alloying or sintering (Figure 2.5.32), but layouts also exist where the semiconductor chip floats freely between two molybdenum disks. The case ring is made of ceramics, glass, or in some rare cases plastic. Disk cell packages are only used for high-performance diodes and thyristors (some 100 A up to several kA). The voltage range stretches from a few 100 V (welding diodes) to a blocking voltage of some kV.

One particular kind is the IGCT (**I**ntegrated **G**ate **C**ommutated **T**hyristor) featuring thyristors that can be turned off. Their control unit must have especially low-inductance connections and be powerful at the same time. For this reason, disk cell and driver board are only supplied in combination [40].

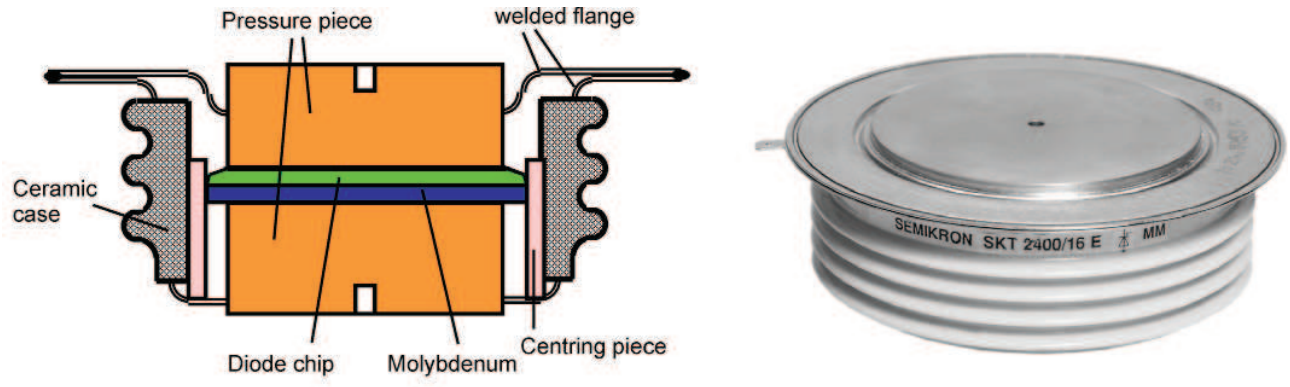


Figure 2.5.32 Sectional view of a disk cell and view of a thyristor disk cell

2.5.3.4 SEMiSTART®

For the SEMiSTART®, two discrete thyristors have been connected in antiparallel to form one component. The cathode of the first thyristor is connected to the anode of the second thyristor through the first heat sink. The anode of the first thyristor is connected to the cathode of the second thyristor through another heat sink. The whole structure is pressure-bonded; disk springs serve to store pressure. The auxiliary contacts are spiral spring contacts. The thyristors are not insulated against the heat sink but have threaded holes for principal current connection. Owing to its high short-time overload capability, SEMiSTART® is mainly used in soft starters. The r.m.s. values for the currents permissible for 20 seconds are 560 A up to 3080 A; the blocking voltage is 1800 V.

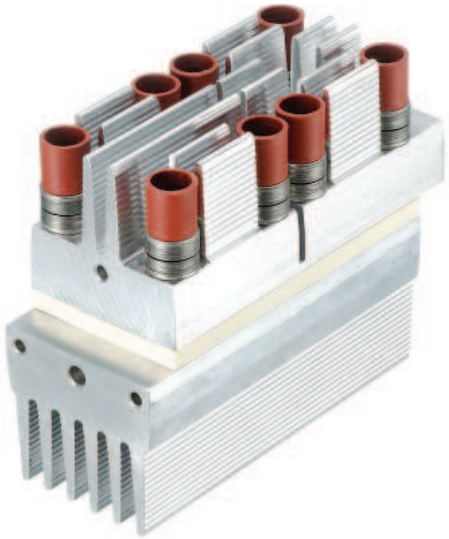


Figure 2.5.33 SEMiSTART®, two thyristors connected in antiparallel without insulation in pressure contact design

2.5.4 Power modules

2.5.4.1 Basics

Normally, circuitry in power electronics does not just contain a single power semiconductor component, but is almost always composed of several components. When discrete devices are used, several of them, including their corresponding heat sinks, must be combined into one assembly. Since the heat sinks are conductively connected to one terminal each of the corresponding semiconductor component, they must be electrically isolated during assembly. The electrical connections are made by cables or busbars. This construction is very costly in terms of the material, volume and labour time involved. A completely new way is opened up by the idea to put the necessary insulation of the individual components into the component itself rather than into the mechanical structure of the module. Such power modules are charaterised by the separation of the paths for current and heat flow. Internal insulation with good heat dissipation capability ensures that the metal base is electrically isolated from the circuit which is connected to the outer terminals and that the heat from several components can be dissipated potential-free to a common cooling device (Figure 2.5.34).

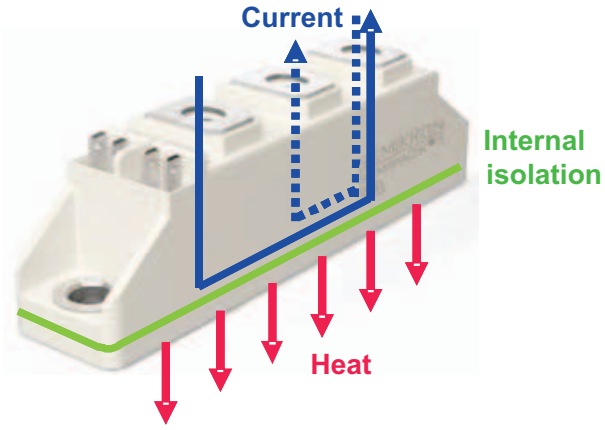


Figure 2.5.34 Principle behind a power module exemplified by a SEMIPACK ® halfbridge module (phase module, dual module) with two series-connected diodes/thyristors

Modules may contain line rectifier diodes, fast diodes, thyristors, MOSFET or IGBT as semiconductors. The complexity of the internal circuitry ranges from a single semiconductor to a maximum of 20 semiconductor functions (chapter 2.5.2.7). In addition, some modules comprise passive components, such as temperature sensors, resistors and capacitors. Power modules with integrated driver functions are referred to as **I**ntelligent **P**ower **M**odules (IPM).

Very common are halfbridge modules (dual modules, phase modules) with the connection sequence ~ / + / -/ for the main terminals. This configuration allows for any circuits typical in power electronics to be created from several of these modules and simple connection elements. Even the first semiconductor power module, the SEMIPACK® (1975), had this connection geometry. Figure 2.5.35 demonstrates in an exemplary drawing the layout of such a halfbridge module integrating thyristors in solder technology. A plastic case is glued on the module body and so much silicone gel is applied that insulation requirements are met permanently. Please note that most casing materials are not fully impermeable by infrared light. This means that the off-state current has a higher value in a bright environment, e.g. sunshine, than in complete darkness. This does not affect module functionality or reliability.

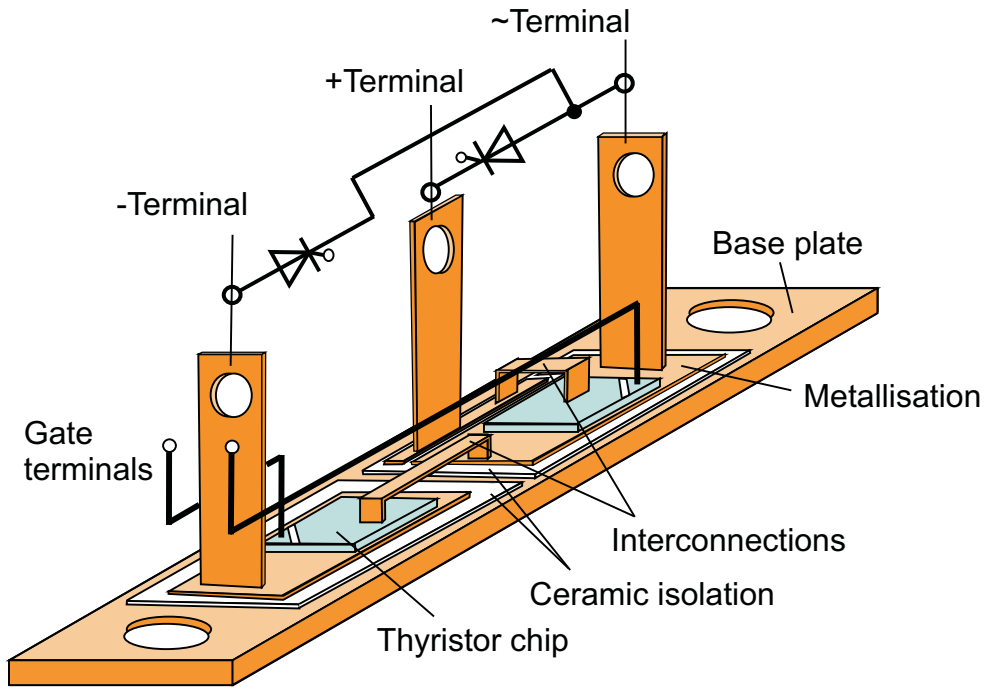


Figure 2.5.35 Schematic layout of a thyristor-halfbridge module

Besides these halfbridge circuits, modules with 1-phase and 3-phase bridge circuits are very common both as rectifiers and inverters. Modules containing a rectifier bridge plus inverter and brake chopper are normally referred to as CIB modules (**C**onverter **I**nverter **B**rake, the rectifier here being called a "converter"). Other module configurations are available for special applications.

2.5.4.2 Module families containing diodes and thyristors

SEMIPACK®

SEMIPACK® is the "father" of all power semiconductor modules. It was introduced in 1975 by SEMIKRON. Since then it has been expanded into a component family with mean forward currents ranging from 15 A to 1200 A and is continuously adapted to given market requirements in a number of versions. All SEMIPACK® modules have a copper base plate.

Configuration	Abbreviation	Description
SKET	ET	1 thyristor
SKKD	D	Halfbridge with 2 series-connected diodes
SKKE	E	1 diode
SKKH	H	Halfbridge with diode and thyristor (thyristor "on top")
SKKL	L	Halfbridge with diode and thyristor (thyristor "at the bottom")
SKKT	T	Halfbridge with 2 series-connected thyristors
SKMT	M	Midpoint connection of 2 thyristors, cathodes connected
SKNH	N	Midpoint connection of thyristor and diode, anodes connected

Table 2.5.5 Overview of circuit topologies available in SEMIPACK case

SEMIPACK®	Mean forward current	Reverse voltage	Configurations	Technology	Main current terminals
SEMIPACK®0	15 A	600 V – 1600 V	D, E, H, T	Chips soldered on both sides	Plug
SEMIPACK®1	28 A – 119 A	800 V – 2200 V	D, E, H, L, T, M, N	Chips soldered on both sides	Screws
SEMIPACK®2	122 A – 212 A	800 V – 2200 V	D, E, H, T	Chips soldered on both sides	Screws
SEMIPACK®3	250 A – 380 A	800 V – 2200 V	D, E, H, T	Chips, soldered / bonded or with pressure contacts	Screws
SEMIPACK®4	330 A – 600 A	800 V – 2200 V	E, ET	Chip, pressure contact	Screws
SEMIPACK®5	570 A – 701 A	800 V – 2200 V	D, H, T	Chips, pressure contact	Screws
SEMIPACK®6	740 A – 1180 A	1400 V – 2200 V	E, ET	Chip, pressure contact	Screws

Table 2.5.6 Overview of SEMIPACK case names and connection technology

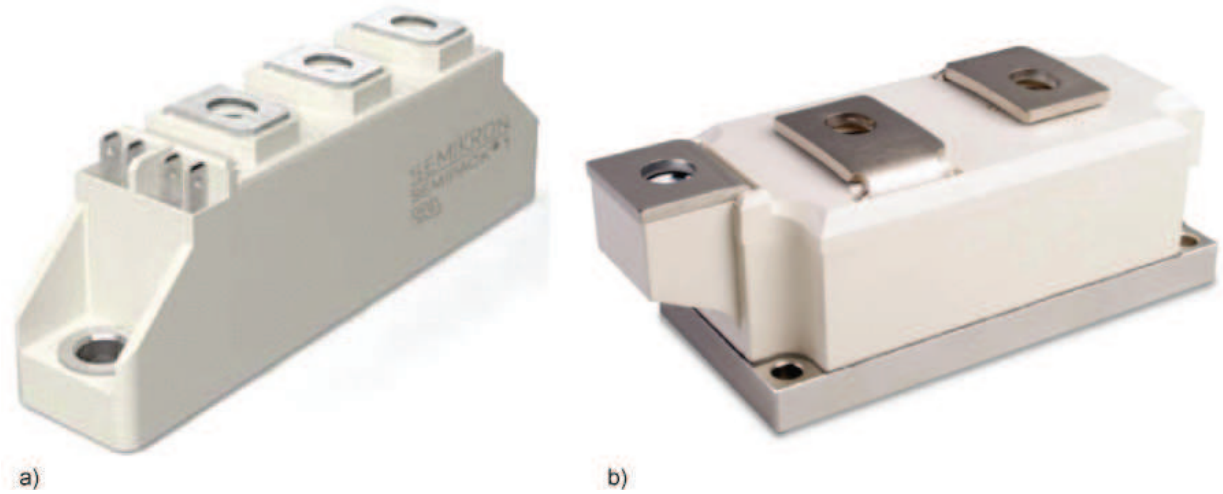


Figure 2.5.36 a) SEMIPACK®1 (soldered chips, soldered / bonded top side, aux. spring contacts)
b) SEMIPACK®5 (pressure-contact chips)

SEMIPACK®fast

This name is used for fast diodes available in D, E, M and N configurations in the case types SEMIPACK®1 and 2, or SEMITRANS®4. Blocking voltages range from 200 V to 1700 V.

SEMIPONT®

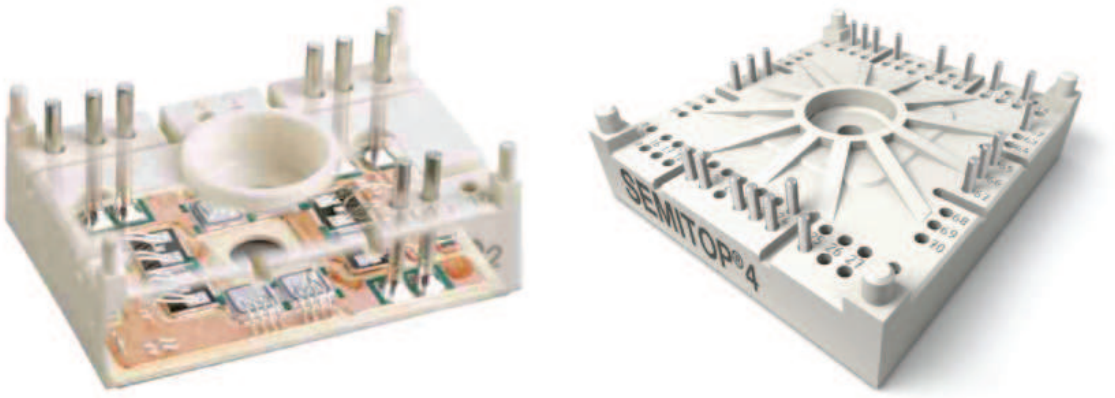
Single-phase and three-phase rectifier modules with a DC output current from 2 A to 210 A and blocking voltages from 200 V to 1800 V form the SEMIPONT® family. In addition to pure diode bridges for uncontrolled rectifying, semi-controlled and fully controlled thyristor bridges with/without brake chopper or freewheeling diode are also available. 3 antiparallel thyristor pairs in one case can be used to form AC switches (W3C circuits).

Depending on the amperage, modules are available in many case types with plug-in, solder or screw connections. Some designs have copper base plates. Especially in the lower power range, the chips are soldered onto a DBC ceramic substrate which is pressed on the heat sink by the case and the fastening screw(s).

Figure 2.5.37 Examples of SEMIPONT® designs

SEMITOP®

This module family comprising 4 case sizes does not feature a copper base plate. Just one screw is needed to press the module on the heat sink. Current and control terminals feature solder pin connections. Apart from circuits with IGBT (chapter 2.5.4.3)), a number of configurations are available that incorporate diodes and thyristors, e.g. single-phase and three-phase uncontrolled, semi-controlled and fully controlled bridges, single-phase, two-phase and three-phase AC switches and many other variants. With blocking voltages from 600 V to 1600 V, the r.m.s. currents or the DC mean values lie between 25 A and 210 A.



a) b)

Figure 2.5.38 SEMITOP®1, semi-transparent case (a) and SEMITOP®4 as semi-controlled three-phase bridge with brake chopper (b)

SEMiX®

These modules with copper base plate, which are designed for higher power output, come with halfbridges and three-phase bridges with diode and thyristor circuits. With a module height of 17 mm, they are mainly intended for use with SEMiX® IGBT modules. With a blocking voltage of 1200 V or 1600 V, the current densities lie between 170 A and 340 A. What should be pointed out here is the very easy mounting of PCBs used to drive the thyristor above the module by way of spring contacts.

Figure 2.5.39 Examples of SEMiX® modules

2.5.4.3 Module families including IGBT and freewheeling diodes

SKiiP®

This is now the 4th generation SKiiP (**S**emi**k**ron **i**ntegrated **i**ntelligent **P**ower) since its commercial launch in the middle of the nineties. Figure 2.5.40 shows the structure of a SKiiP module.

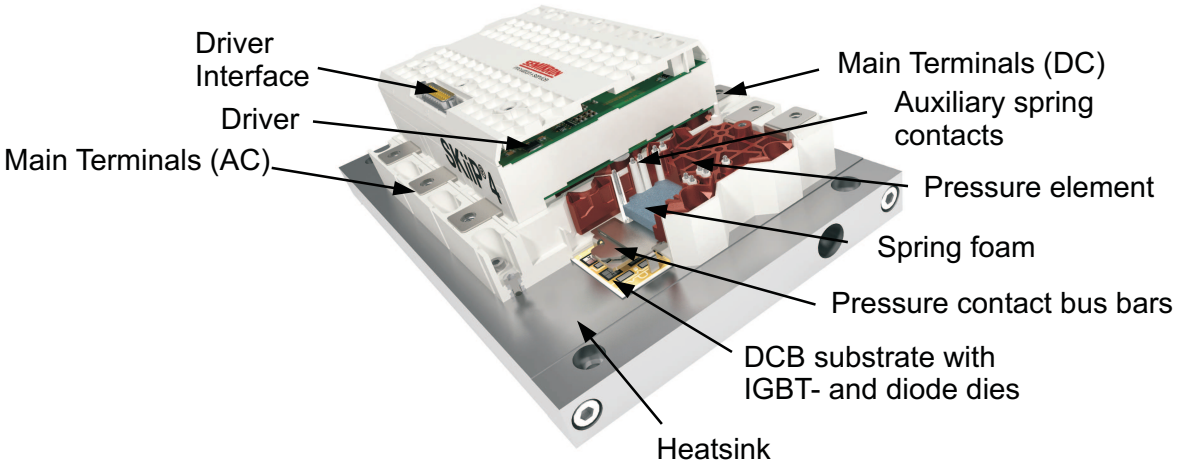


Figure 2.5.40 Basic structure of a 4th-generation SKiiP

In contrast to conventional transistor modules, the DBC substrates carrying the IGBT and diode chips are not soldered onto a copper base plate, but are pressed almost across the entire surface directly onto the heat sink by means of an elastic spring element. The electrical connection of the DBC to the terminals is made by pressure contacts and low-inductance tracks. The DC bars are offset in height and designed for the connection of external laminated, low-inductance busbars. A metal plate filled in plastic compound serves as a pressure element and shield for the driver circuit, which is also integrated into the SKiiP case.

By parallelling many, relatively small IGBT chips and with optimal chip-to-heat sink contact, the thermal resistance R_{th} may be reduced considerably compared to standard modules, since the heat is spread evenly across the heat sink. Besides transistor and diode chips, temperature sensors are also integrated into the DBCs; temperature sensor output signals directly affect driver operation (temperature limit) and - due to analogous amplification in the driver - can also be used for external evaluation. The AC connectors of SKiiP modules accommodate current sensors as measuring units for overcurrent and short-circuit protection of the IGBT. Signal processing and linking is done by the internal driver in the SKiiP, which is positioned above the pressure plate. The potential-free current signals may also be used as actual values for external measuring units and control loops.

Four case sizes (2, 3, 4 and 6 IGBT halfbridges) and their matching driver components can be used to build H-bridges or three-phase bridges in 1200 V and 1700 V technology with the aid of simple external connections, for example. Converter performance without external parallel connection covers a range of 100 kW up to 1.5 MW.

Advantages of SKiiPs over conventional modules are, for example:
- About twice the temperature cycling capability in long-term use
- Reduced thermal resistance by direct heat transfer between chip, DBC and heat sink
- Very compact designs with high power density
- Low switching overvoltages due to consistent low-inductance structure, i.e. high permissible DC-link voltage and reduced interference
- Optimal matching of the intelligent driver integrated in SKiiP
- Pre-assembly of power modules on heat sink, optimum thermal paste application in screen printing process
- Low-inductance converter design by way of parallel current paths (4x 600 A halfbridge modules rather than 2x 2400 A single switches)
- Manufacturer-side load testing on complete systems.

In Table 2.5.7 3rd and 4th generation SKiiP cases are listed. Besides the heat sink shown below, SKiiPs may also be mounted on other air or water-cooled heat sinks.

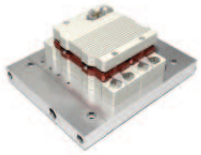
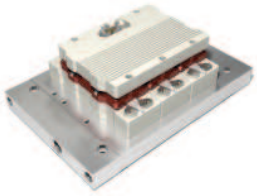
SKiiP3 1200 V / 1700 V			
Halfbridges	2	3	4
I_C	1000 A	1500 A	2000 A
SKiiP4 1200 A / 1700 V			
Parallel IGBT halfbridges	3	4	6
$I_{C@TS=25°C}$	1800 A	2400 A	3600 A

Table 2.5.7 Case designs for 3rd and 4th generation SKiiPs

SKiM

SKiM modules have no base plate and are designed for the medium power range between SKiiP and MiniSKiiP applications. This module features SKiiP technology throughout. SKiM63/93 is the first IGBT module to contain no solder whatsoever. The elimination of all solder connections results in 5 times the thermal cycling capability compared to standard soldered modules with base plate. Thanks to its compactness, this module, which was originally developed and qualified for the automotive industry, is also an interesting solution for standard drives in the power range from 30 kW to 150 kW. The main terminals are located at the front ends, leaving plenty of space for the driver board on top. It is mounted without solder by means of spring contacts.

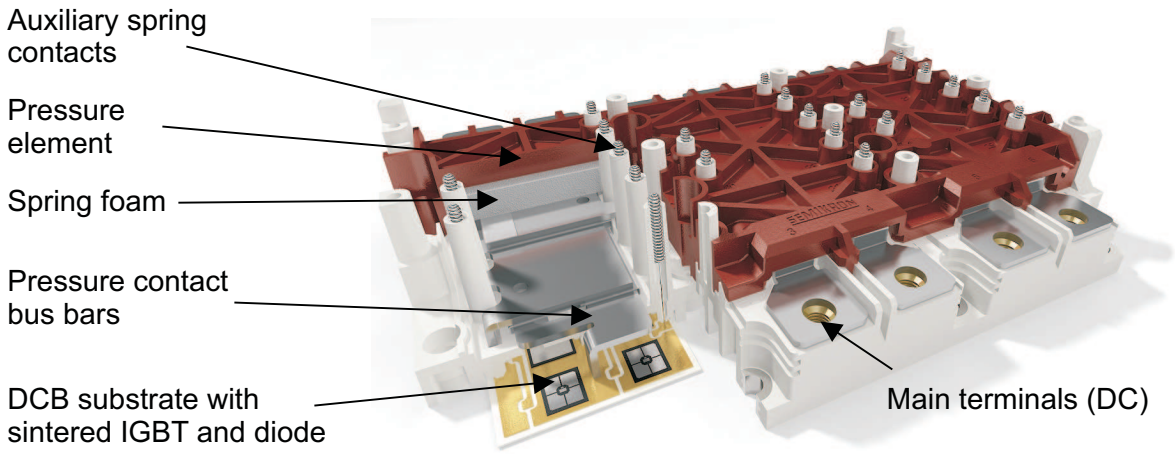


Figure 2.5.41 Cross section of a SKiM63 module

Like its predecessors, SKiM4 and SKiM5, this module contains a three-phase bridge circuit (GD, 6-pack). Non-standard versions as choppers (3-phase GAL/GAR for asymmetrical H-bridges, e.g. for reluctance motor applications) or as phase modules for three-level inverters (**M**ulti **L**evel **I**nverter, MLI) also exist. SKiM is available in the voltage classes 600 V, 1200 V and 1700 V.

SEMITRANS®

SEMITRANS is the name for transistor module cases whose most important types have been standardised in case widths of 34 mm and 61 mm in accordance with IEC 60191-2. These modules feature a copper base plate whose main terminals are designed as exterior screw contacts (exception: SEMITRANS 6). Owing to the centre position of the DC terminals, which are highly symmetrical in relation to chip connection (very good current distribution between parallel chips), these modules are especially low-ohmic and low-inductive compared to the 17-mm-high modules with load terminals at the front ends (SEMiX). Auxiliary terminals are mostly designed as "fast-on" plug-in contacts (exception: SEMITRANS 4). Apart from a few MOSFET modules, IGBT and soft recovery diodes are used in the voltage classes 600 V, 1200 V and 1700 V. These modules are part of the medium power range with current classes ranging from 20 A (GD, 6-pack) to 800 A (GA, single switch).

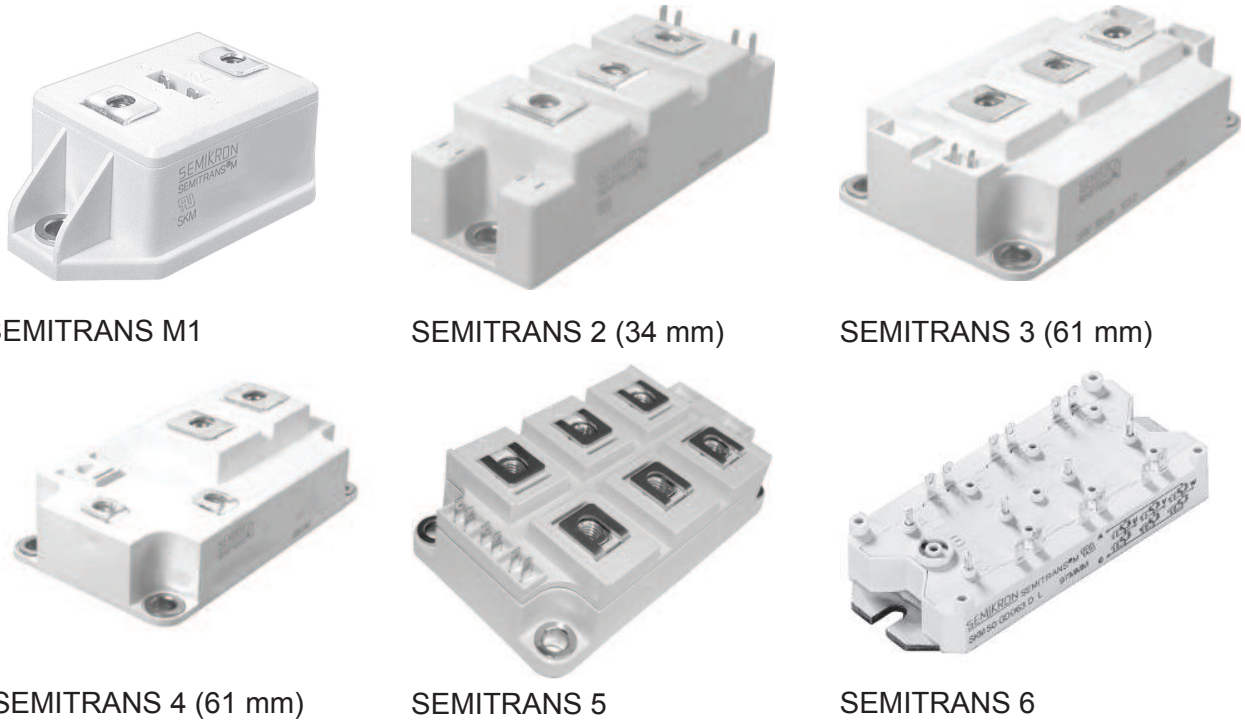


Figure 2.5.42 Case designs in the SEMITRANS family

SEMiX®

This module family with base plate, which is part of the same power range as SEMITRANS, is mainly charaterised by its extremely flat design (17 mm in height), the position of the main terminals at the front ends and easy mounting of the driver board directly on top of the module using spring contacts.

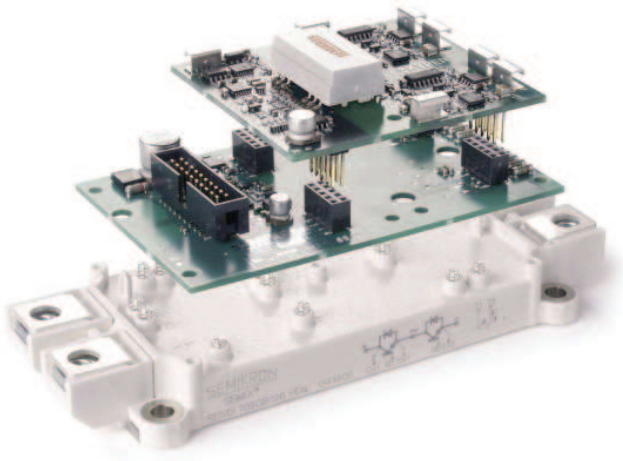


Figure 2.5.43 SEMiX3 with easy and space-saving driver assembly (SKYPER) above the module, connection by springs

This case design has become a quasi-standard, at least in terms of the basic dimensions and the position of the main terminals. SEMIKRON offers four case sizes as halfbridge modules (SEMiX1 to 4 - Figure 2.5.44) and two cases sizes as 3-phase bridge versions, too (GD, 6-pack – SEMiX13 and SEMiX33). The case sizes SEMiX3 and SEMiX33, in particular, are offered with similar performance features by various manufacturers. Module sizes 1 and 4 extend the power range in the lower and upper regions. Using rectifier bridges of the same height, complete converter circuits can be made in a very flat and space-saving designs.

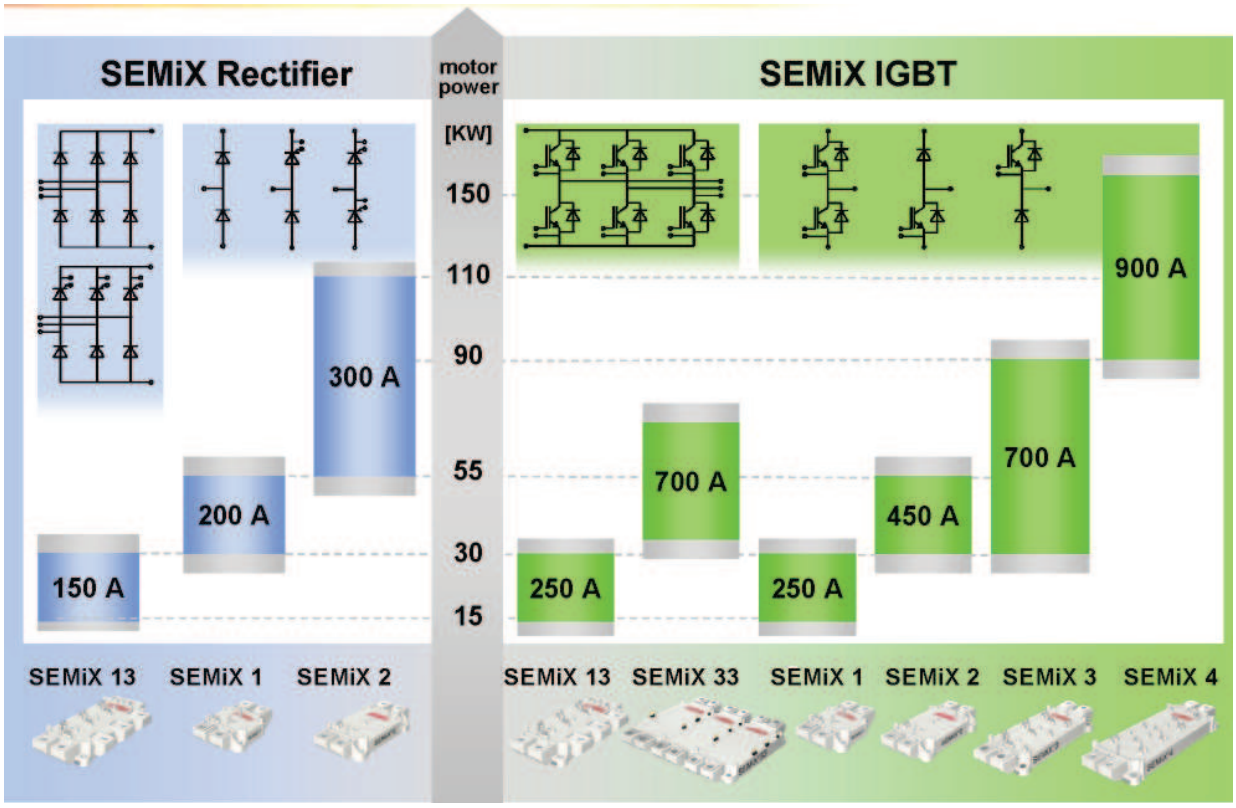


Figure 2.5.44 Overview of case types, performance range and integrated circuit topologies in SEMiX case

The internal structure of a SEMiX module is shown in Figure 2.5.45. Depending on the module size, identical DBC substrates are connected in parallel. Each DBC substrate contains a pair of IGBT and the corresponding inverse diodes. SEMiX modules come in the conventional module design with copper base plate, soldered ceramic substrates, soldered and bonded chips and soldered terminals and intermediate links. Non-standard here are spring contacts for the auxiliary terminals and the integrated temperature sensor (NTC).

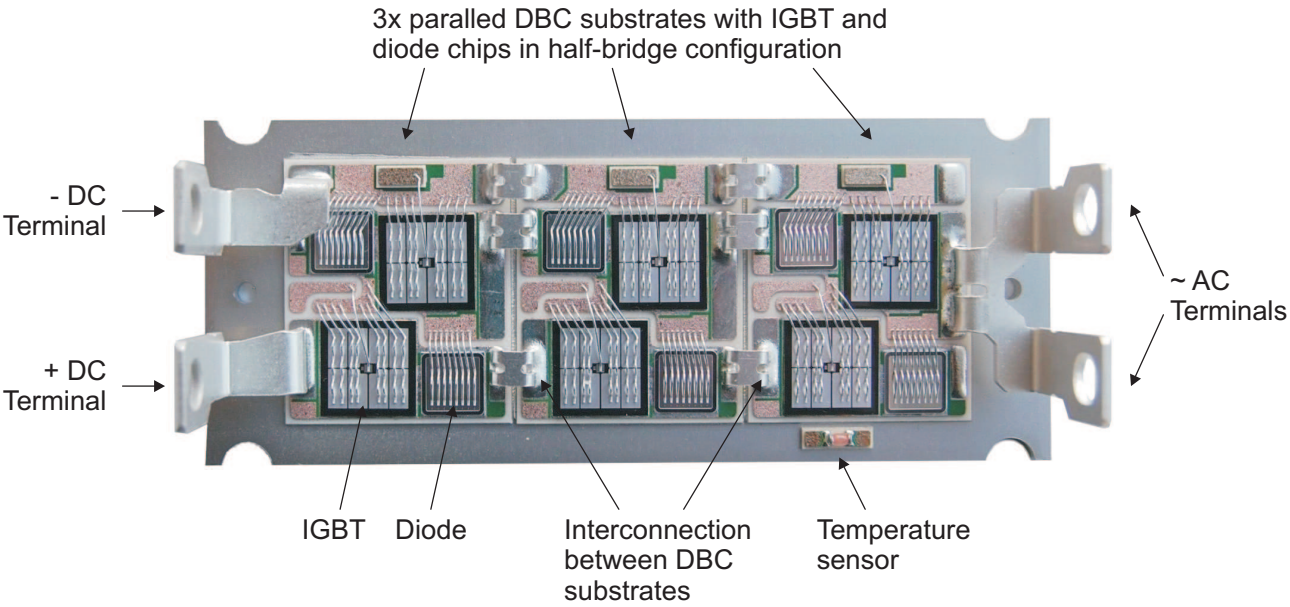


Figure 2.5.45 Internal structure of a SEMiX3 module

MiniSKiiP

Pressure-contact MiniSKiiP are IGBT modules in SKiiP technology for the lower power range, boasting flexibility and easy assembly. The basic structure of this module is shown in Figure 2.5.46.

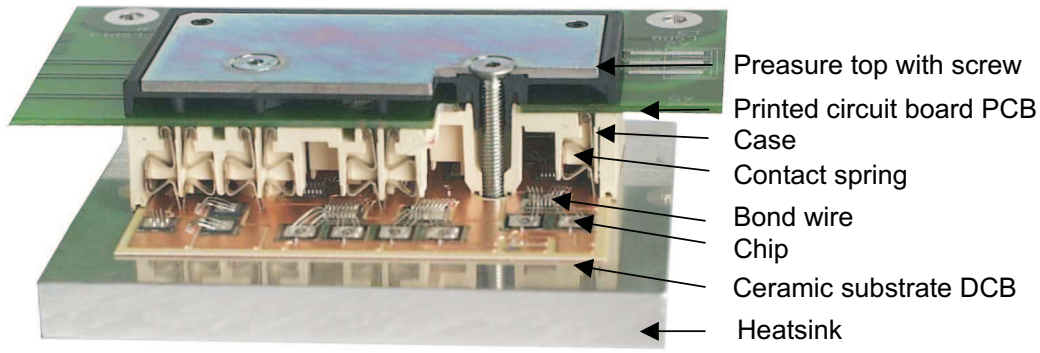


Figure 2.5.46 MiniSKiiP layout

MiniSKiiPs are composed of:
- DBC insulation substrate with soldered and wire-bonded semiconductor chips (e.g. IGBT, MOSFET, diodes, thyristors) and other components such as current and temperature sensors
- the silicone filled case with integrated contact springs and glue-bonded DBC
- hard plastic cover with pressure plate

One or two screws are used for the entire electrical and thermal connections (to the heat sink), making a detachable, friction-locked connection between SKiiP cover, PCB, MiniSKiiP and heat sink. The contact springs have several functions: they make the electrical connection between the power semiconductor circuit on the DBC and the other circuits on the base PCB, and also serve as pressure spring pad for pressing the DCB onto the heat sink in the mounted state.

The large number of springs spread over the entire MiniSKiiP surface ensures even pressure between component and heat sink, which ensures a low thermal contact resistance. For the current range above 20 A, the contacts are connected in parallel. The multitude of spring shafts results in a high degree of flexibility concerning the creation of many different circuits for drives and power supply systems, as well as other applications.
Four case sizes designed for different power ranges are available in the 2nd generation, ranging from MiniSKiiP 0 (600 V IGBT, rated current up to 20 A) to MiniSKiiP 3 (600 V and 1200 V IGBT, rated currents up to 150 A).

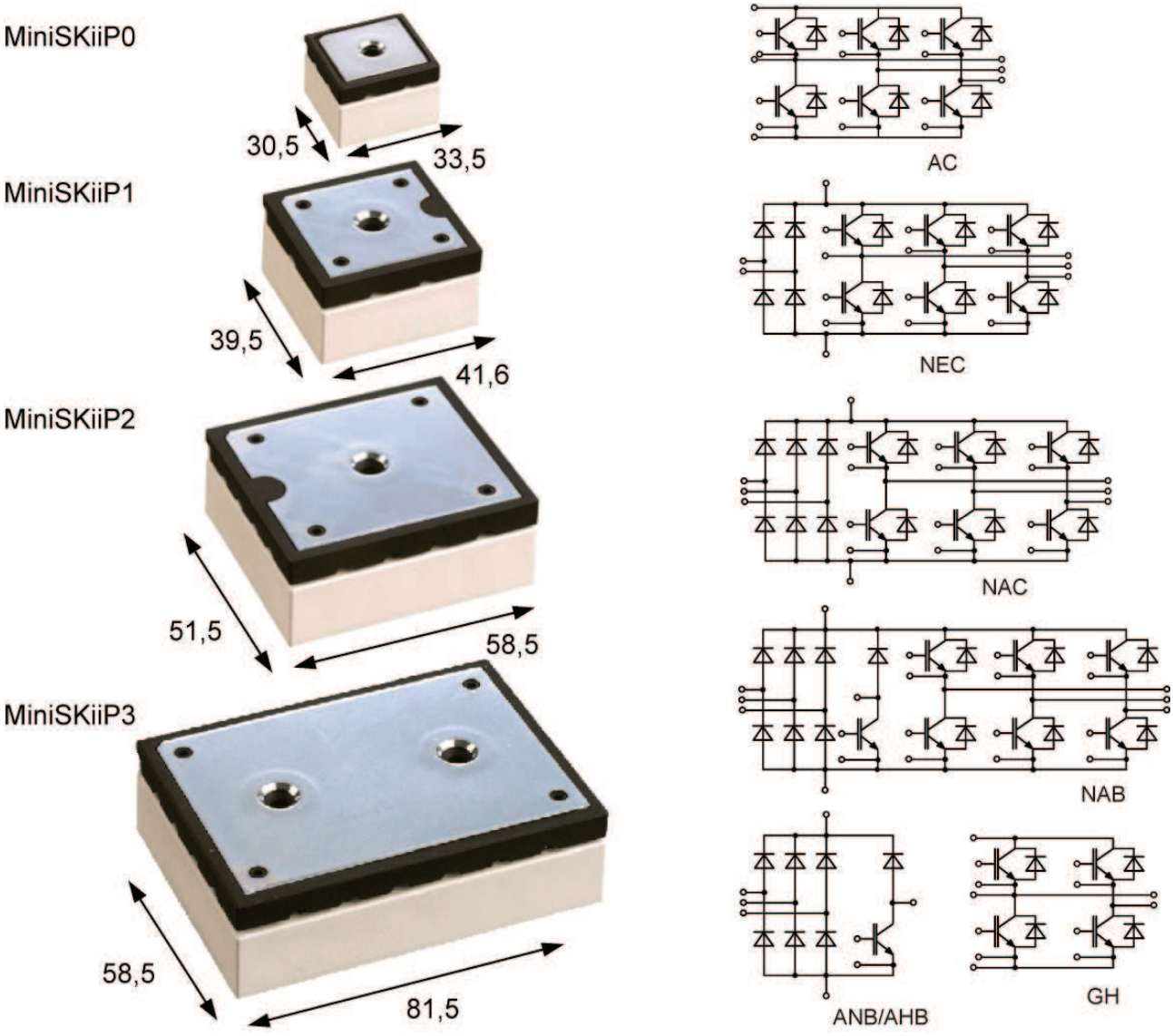


Figure 2.5.47 Standard MiniSKiiP designs (dimensions in mm) and circuits

SEMITOP

The aforementioned SEMITOP module series comes in 4 case sizes (Figure 2.5.38). Like the SKiiP, SKiM and MiniSKiiP, SEMITOP also belongs to those modules without copper base plate that generate large-surface pressure across the DBC-to-heat sink connection using a special type of plastic case. A single screw makes a friction-locked connection between module and heat sink. Unlike in MiniSKiiP, contact with the PCB is made by solderable pin connectors.

Since a maximum of 12 power components can be integrated in such a small module, SEMITOP modules are preferred in low-power applications with low space requirements. The space between the solder pins can be fully utilised to accommodate other PCB components.

2.6 Integration of sensors, protective equipment and driver electronics

A few examples of the integration of peripheral functions in power modules are described below. These are arranged in order of degree of integration.

2.6.1 Modules with integrated current measurement

Firstly, current measurements in modules are taken to protect the power semiconductors from overcurrent, and secondly, the current signal is also required for current control loops. Rough monitoring is sufficient for the first task, which is why the semiconductor itself can be utilised as a current sensor ($V_{CE(sat)}$ monitoring). The latter must be very accurate (2%…5%), very dynamic (response times ~ 1 µs) and requires a frequency range from DC to some 10 kHz.

Current shunts

Current shunts for taking direct measurements are integrated into the emitter path (-DC) of IGBT modules or placed at the AC output. The three square components in Figure 2.6.1 show a solution for current measurement in the emitter path of three low-side IGBT in a three-phase inverter module. Evaluation must be performed using a differential amplifier in the driver electronics stage. The connecting pads at the sides ensure low-inductance coupling with the main current path.

The problem with the use of shunts is the discrepancy between the low measurable voltage range in a disturbed environment and the losses in the shunt. A 5 mΩ shunt has a voltage drop of just 100 mV at 20 A, but 2 W losses. With such a power loss, the limits for PCB assembly have been reached. Shunts that are integrated in the DBC provide the advantage that the heat loss can be directly dissipated through the heat sink. This extends the usable current range on the PCB from approx. 20 A to approx. 50 A. The disadvantage here is that "precious" DBC space is lost.

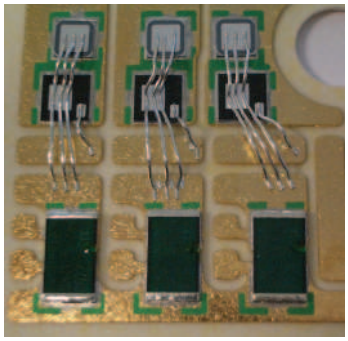


Figure 2.6.1 Current shunts (made by Isabellenhütte) in the emitter path of a MiniSKiiP IGBT module

Current sensors

For currents above 50 A, electrically insulated transmitters operating according to various principles are used (transformer, Hall effect, magneto-resistive effect). SKiiP uses compensating transducers (Figure 2.6.2), which are charaterised by high precision, a wide frequency range and a high overload capability. Sensor evaluation is part of the IPM electronics and the protection concept. In the principle presented here, the magnetic field of the main current is measured in an air gap of the transmitter core and, with the aid of an amplifier, a current is impressed on an auxiliary winding which compensates the magnetic field to zero. The compensation current is a direct map of the main current. It is possible to measure DC current and detect the direction of current flow.

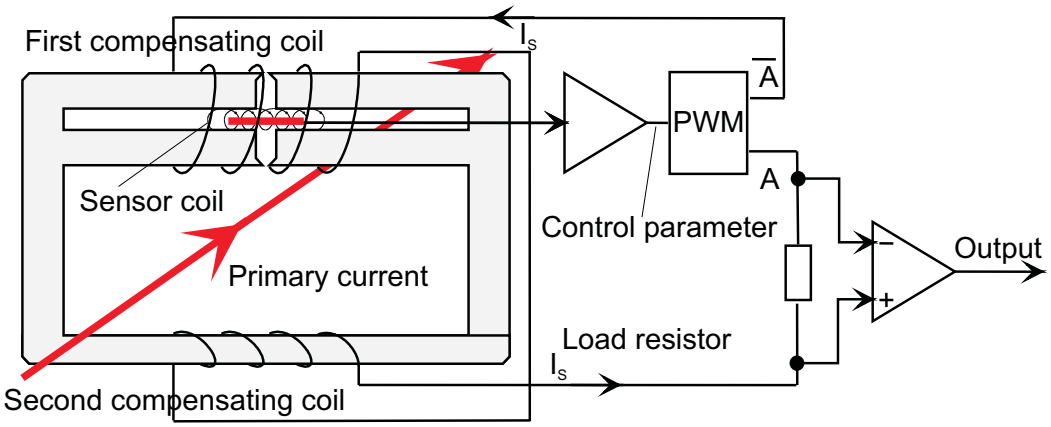


Figure 2.6.2 Operating principle of the compensation current sensor in SKiiP IGBT modules

Sense IGBT modules

These IGBT require special chip types for which a measurement current that is proportional to the main current is withdrawn via a small number of separately connected cells. These IGBT require special chip bonding and signal conditioning which is not available in SEMIKRON modules. Compared to solutions with shunts in the emitter circuit, a much higher measuring resistance may be selected here. In contrast to overcurrent protection provided by V_{CE} monitoring, either shorter dead-times are required or none at all. A disadvantage here is the lack of precision as well as the temperature dependency of the measurement method, meaning that it can only be employed for protection purposes.

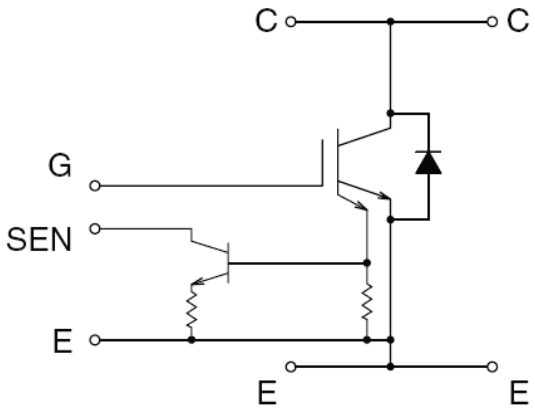


Figure 2.6.3 Sense IGBT [41]

2.6.2 Modules with integrated temperature measurement

Modules with a high degree of integration increasingly use simple PTC (**P**ositive **T**emperature **C**oefficient) or NTC temperature sensors (**N**egative **T**emperature **C**oefficient) in SMD designs or as chip sensors. The PTC sensor of type SKCS2Typ100 is used in MiniSKiiP, in some SEMITRANS and SEMITOP modules, as well as in SKiM4/5 and SKiiP2/3. At 25°C, the sensor has a resistance of 1000 Ω and a typical temperature coefficient of 0.76%/K.

$$R(T) = 1000\Omega \cdot (1 + A \cdot (T - 25°C) + B \cdot (T - 25°C)^2)$$

where $A = 7{,}635 \cdot 10^{-3}\ °C^{-1}$ and $B = 1{,}731 \cdot 10^{-5}\ °C^{-2}$

The measurement tolerance of the sensor in the measured current range 1 mA … 3 mA is max. ± 3% at 25°C, max. ± 2% at 100°C.

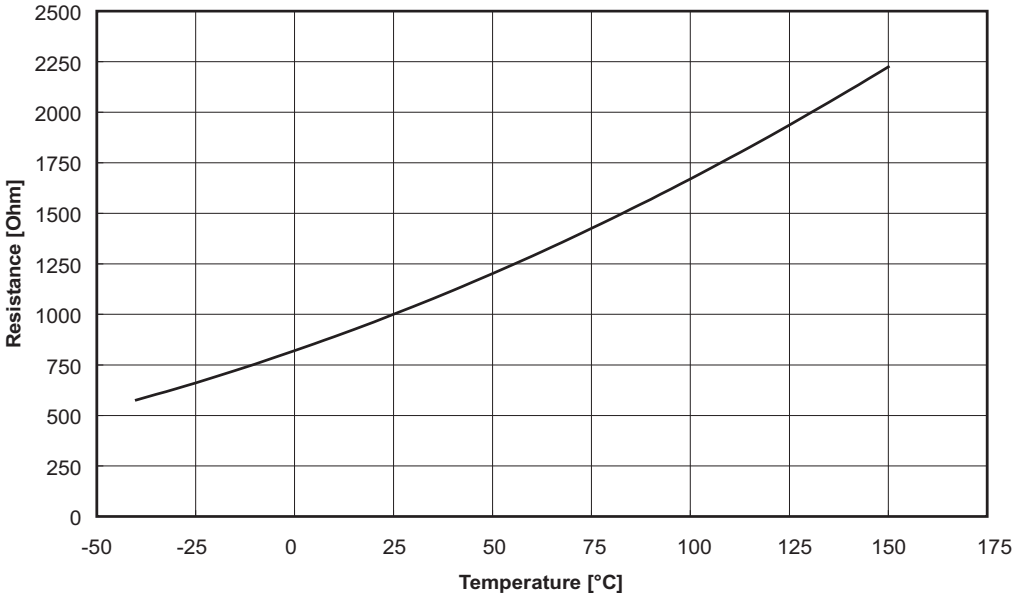


Figure 2.6.4 Characteristic curve of the PTC temperature sensor, type SKCS2Typ100

An NTC sensor, e.g. of type KG3B-35-5, is used in SEMiX components, some SEMITOPs, as well as in SKiM63/93 and SKiiP4. The individual product groups use sensors with different characteristics. For details on the characteristic parameters, see the datasheets. For example, the sensor in SEMiX IGBT modules has a resistance of 5 kΩ at 25°C and a resistance of 493 Ω at 100 °C. The measurement tolerance of the sensor in the measured current range 1 mA … 3 mA is max. ± 5% at 100°C. Owing to its exponential characteristic, the sensor is more suitable for protection than for temperature measurement.

$$R(T) = R_{100} \cdot e^{B_{100/125} \cdot \left(\frac{1}{T} - \frac{1}{T_{100}} \right)}$$

where R_{100} = 0.493 kΩ (± 5%)
$B_{100/125}$ = 3550 K (± 2%)
T_{100} = 373.15 K [T -in Kelvin]

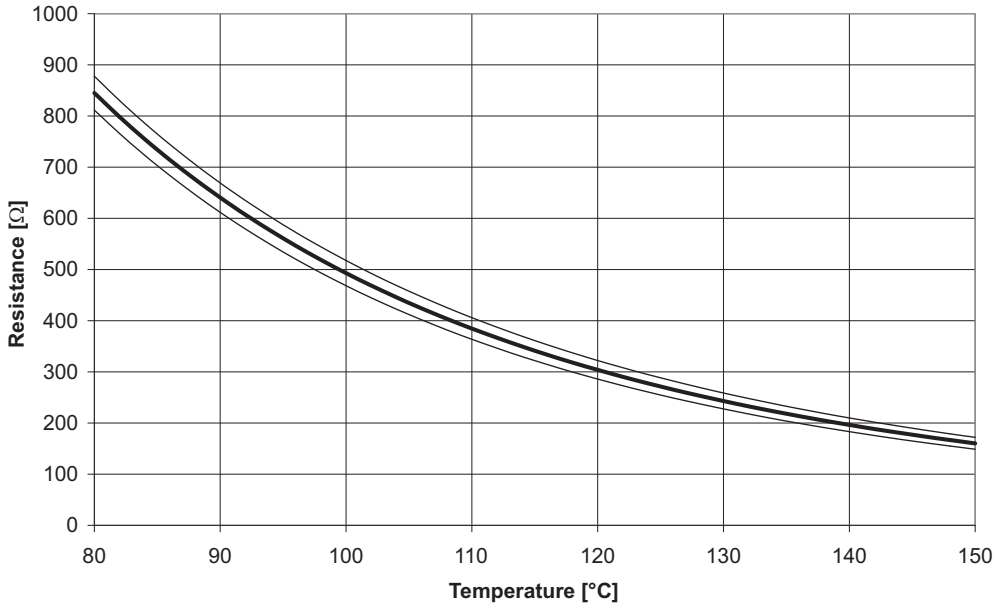


Figure 2.6.5 NTC sensor characteristic in its relevant temperature range incl. tolerance

In modules, the sensors are insulated and soldered on the DBC ceramic substrate close to the chips. For modules with base plate, the sensors approximately render the base plate temperature; sensors in modules without base plate approximately capture the heat sink temperature. Ideally, the vertical heat flow between the measuring point and the heat sink areas under the hottest chips is statically negligible. A suitable evaluation circuit provides static overtemperature protection by active driver control or by analogue signal processing. However, there are considerable dynamic time delays, represented for example in the long time constants of thermal impedance $Z_{th(j-r)}$ in the SKiiP3 (shares of t > 200 s for air-cooled systems, > 50 s for water-cooled systems). For this reason, an insulated temperature sensor cannot provide protection from short-time overload.

High-quality protection in terms of dynamics is possible with IPM solutions (see SKiiP4 in the following chapter). The protective function can be carried out at the secondary side of the driver and thus at high potential. The sensor can therefore be placed on the same copper pad as the power semiconductors, directly beside the heat source. Measurements are much closer to the chip temperature, although not yet equal. The biggest advantage, however, is that the greatest time constant of $Z_{th(j-r)}$ is now in the range of 1 s, thus enabling much better protection from short-time overload. Digital signal transmission in the SKiiP4 nevertheless provides an analogue temperature sensor signal at the driver interface, which meets the requirements of reinforced insulation.

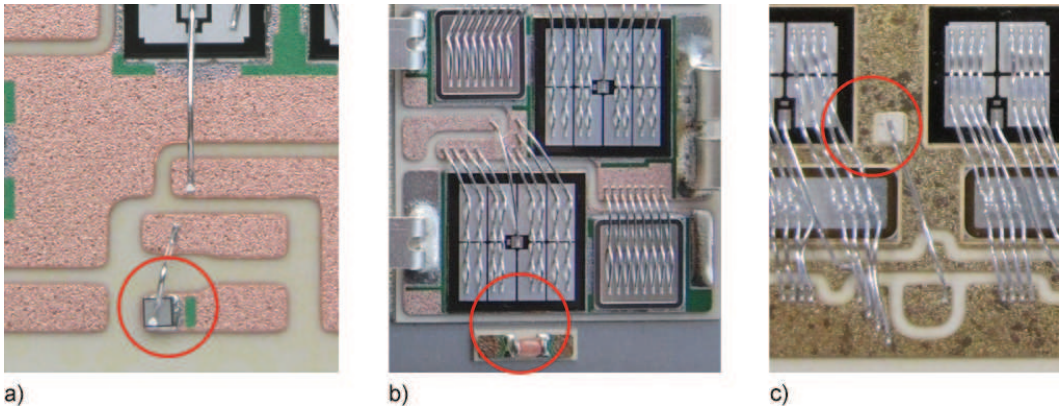


Figure 2.6.6 Temperature sensors in power semiconductor modules, a) Insulated PTC chip in a MiniSKiiP (0.7 mm clearance); b) Insulated NTC component in a SEMiX (1.6 mm clearance); c) non-insulated chip sensor on collector potential in SKiiP4 module

With the exception of the SKiiP4 described above, all temperature sensors have a basic insulation, but do not meet the requirements for reinforced insulation. The insulation clearances are between 0.7 mm and 1.6 mm; the required insulation voltage is achieved by filling the modules with silicone gel. Insulation clearances are so small (Figure 2.6.6 MiniSKiiP example) that in the event of a fault, plasma - and thus high electrical potential - might be present at the sensor. For this reason, the insulation of the temperature sensor is regarded basic insulation only, as per EN 50178. Additional circuits are necessary to obtain the safety grade "Safe Electrical Insulation" described in this standard.

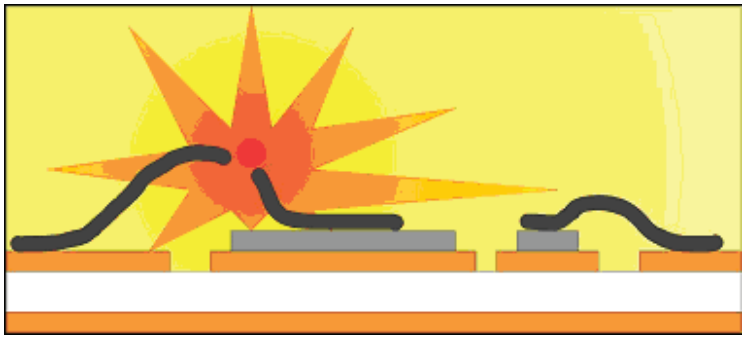


Figure 2.6.7 Possible voltage flashover to the insulated temperature sensor if a bond wire melts as a result of a fault

2.6.3 IPM (Intelligent Power Module)

In addition to IGBT and freewheeling diodes, IPM modules are able to integrate more components for drivers and protective units (IPM minimal configuration) as well as complete inverter control units. Advantages are their high degree of integration and a higher degree of reliability in comparison to relevant discrete structures thanks to ASIC solutions. A disadvantage for the user consists in the fact that he will normally not be able to influence the switching features and logic functions. IPM are therefore often designed specifically for the individual application (ASIPM = **A**pplication **S**pecific **IPM**. SEMIKRON SKiiP and MiniSKiiP IPM are modules with integrated logic functions in two performance classes.

The SKiiP modules which were already described in chapter 2.5 with regard to packaging contain a driver unit that integrates all the necessary protective and monitoring functions. This driver is a SMD-PCB that is located directly above the power modules. Driving and power supply can be performed on potential of the superordinate control system. The SKiiP driver unit integrates the necessary potential separation, a switched-mode power supply and the driver output stages. SKiiPs feature current sensors in the AC outputs and temperature sensors, as well as DC-link monitoring (SKiiP3 optional). The driver acquires the signals transmitted by the sensors for the purpose of overcurrent, short-circuit, overtemperature and overvoltage protection, as well as faults resulting from supply-undervoltage. An error status signal and standardised analogue voltage signals for the actual AC output current value, the actual sensor temperature and the DC-link voltage are available on separate potentials at the driver connector for evaluation in the superordinate control circuit. Overcurrent protection is ensured by the current sensors as well as bridge-shorting protection by way of V_{CE} monitoring. The logic for the control signals provides short-pulse suppression and interlocking of the control signals for a bridge arm.

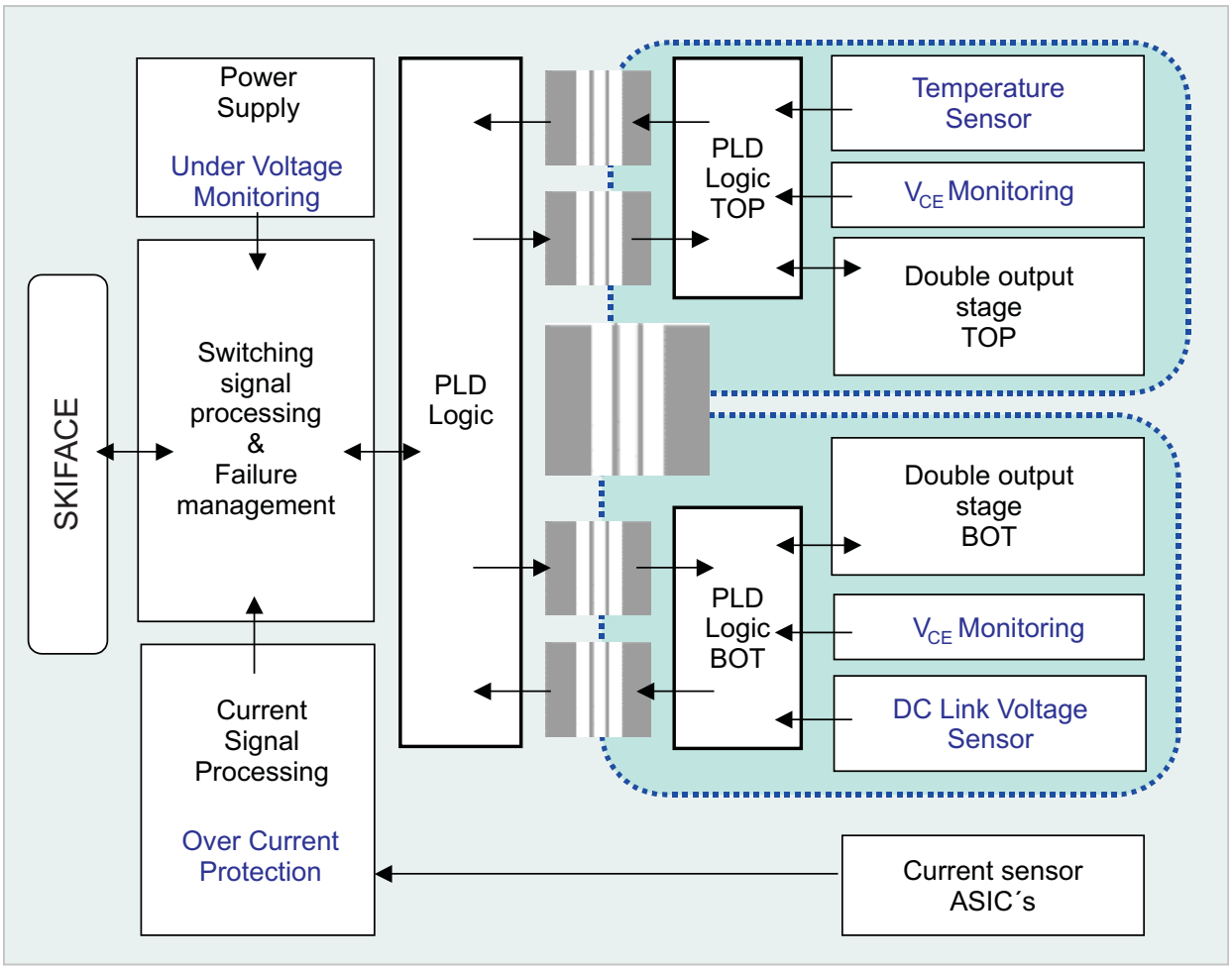


Figure 2.6.8 Block diagram of SKiiP4 IPM driver functions using digital driver logic

MiniSKiiP IPM are equipped with a high-volt driver IC in SOI (**S**ilicon **o**n **I**solation) technology. A two-level "level shifter" enables the operation of 1200 V IGBT in addition to the customary 600 V type series. The IGBT may be driven with controller potential without further insulation. "Down-level shifters" also tolerate negative emitter potential up to –50 V, which may be caused by inductive voltage drops during switching. Without this additional feature, IPM would often fail.

Secondary side power supply is provided by means of a bootstrap circuit. Undervoltage monitoring has been integrated for protection. Measurement voltages of external shunts in the DC path can be evaluated by the driver for overcurrent monitoring.

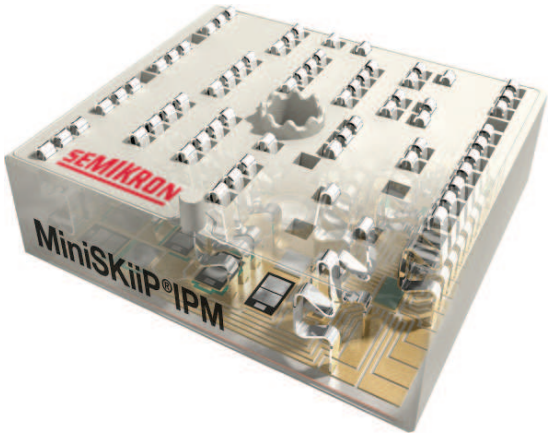


Figure 2.6.9 MiniSKiiP IPM with SOI driver IC directly mounted on the DBC

2.7 Reliability

Reliability, i.e. maintaining the characteristics relevant to operation over a defined period of time, is one of the most important quality features of power modules. On the one hand, power modules are highly utilised electrically and thermally; on the other hand, premature failure may cause dangers, direct and consequential damage and, last but not least, high costs. Owing to the comparably small batch sizes, often extremely long service life requirements (10...30 a) and complex test specifications, reliability is very difficult to properly evaluate. Reliability statements are possible thanks to

- exact control of all influences on production processes
- reliability testing under conditions very close to practical application in order to discover typical failure mechanisms
- testing the components within the system while monitoring the most important parameters

In the context of reliability, the term "Design for Reliability" is often heard [42]; this ultimately means that when a power electronic assembly is designed, component (here the power semiconductor) aging is already factored in. Exactly so much safety must be considered that the maximum values of the components at the end of their forecast service life meet the minimum requirements for this assembly. To be able to do so, however, accurate data on the different manifestations of aging is needed [43].

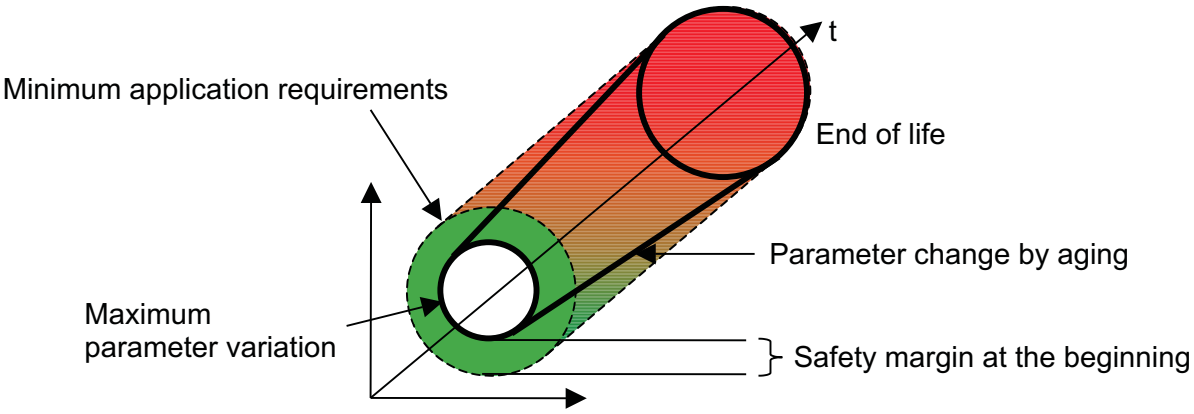


Figure 2.7.1 Design process for reliability. Target: to sufficiently factor in safety and reliability at the beginning of the service life to ensure that product requirements are still met at the end of service life.

Some selected tests for power modules will be presented in the following chapter. SEMIKRON's certified quality assurance system in compliance with ISO 9001 and VDA 6 Part 1 will, however, not be discussed in greater detail.

2.7.1 MTBF, MTTF and FIT rate

The FIT rate (**F**ailure **i**n **t**ime) refers to the number of times a system fails during one hour in operation. Normally, this value is standardised to 10^{-9} h.

$$FIT = \lambda = \frac{n_f}{N \cdot t}$$

n_f = number of failures; N = number of components in operation; t = monitoring period

Premature failure and failure at the end of service life are not considered for analysis, if possible. The failure rate corresponds to the flat section of the "bathtub curve" with constant failure rate (ideal case). The MTBF value (**M**ean **t**ime **b**etween **f**ailure) refers to the mean expected time between two failures. The MTBF value is the reciprocal of the FIT rate.

$$MTBF = MTTF = \frac{1}{\lambda}$$

In connection with power semiconductors, it is generally better to specify the MTTF value (**m**ean **t**ime **t**o **f**ailure), since MTBF refers to the time between two repairs. As repair time is obsolete, both values are identical. In contrast to components for signal processing which are in duty a million times, there is only a weak data basis for power semiconductors. Besides the significantly lower quantities in the field, information on operating hours and conditions is rarely available for returned products. Wikipedia (de.wikipedia.org/wiki/Failure_In_Time) gives a FIT rate of 50…60*10^{-9} hours for power transistors and diodes; this corresponds to an MTTF value of $2 \cdot 10^7$ h. This value applies mainly to discrete devices and modules with no more than two integrated components (SEMIPACK, SEMITRANS). Higher integrated components also have a higher failure rate.

The Arrhenius effect is often mentioned in the context of FIT rates, which means that the failure rate increases exponentially over temperature (cf. next chapter). This statement is only conditionally true, since it only considers temperature-dependent failure mechanisms.

2.7.2 Accelerated testing according to Arrhenius

Accelerated service life tests assume that a process which is triggered by an activation energy is exponentially dependent on the temperature according to the Arrhenius equation. In Figure 2.7.17, the necessary test period is indicated on the Y-axis which would be required for a specific ΔT in the power cycling test. A "slow" power cycling test with ΔT = 30 K would thus take 30…100 years. This process can be speeded up if the temperature is increased during testing and the results are then transferred to "normal" operating conditions.

$$N = B \cdot e^{\frac{-E_A}{k_b \cdot T}}$$

E_A = activation energy, k_b = Boltzmann constant, T = absolute temperature

If a failure rate N for a temperature-related failure mechanism is known, the characteristic for an entire temperature range can be calculated by adjusting factor B and the activation energy.

2.7.3 Standard tests for the product qualification and postqualification

The objectives of reliability tests are:
- To ensure general product quality and reliability
- To establish the limits of systems by exposing them to various test conditions
- To ensure process stability and reproducibility of production processes
- To evaluate the impact of product and process changes on reliability

The following tests are minimum requirements for the product release of power modules. The following standard tests are being made for release and re-qualification of new and/or redeveloped modules to be augmented by further product-specific reliability tests. Reliability tests are destructive tests made on a number of production samples.

	Standard test conditions for:	
Reliability Test	**MOS/IGBT Products**	**Diode/Thyristor Products**
High Temperature Reverse Bias (HTRB) *IEC 60747*	1,000 h, 95% $V_{DC(max)}/V_{CE(max)}$, 125°C ≤ T_c ≤ 145°C	1,000 h, DC, 66% of voltage class, 105°C ≤ T_c ≤ 120°C
High Temperature Gate Bias (HTGB) *IEC 60747*	1,000 h, ± $V_{GS(max)}/V_{GE(max)}$, $T_{j(max)}$	not applicable
High Humidity High Temperature Reverse Bias (THB) *IEC 60068-2-67*	1,000 h, 85°C, 85% RH, V_{DS}/V_{CE} = 80%, $V_{DC(max)}/V_{CE(max)}$, max. 80 V, V_{GE} = 0 V	1,000 h, 85°C, 85% RH, V_D/V_R = 80% V_{Dmax}/V_{Rmax}, max. 80 V
High Temperature Storage (HTS) *IEC 60068-2-2*	1,000 h, $T_{stg(max)}$	1,000 h, $T_{stg(max)}$
Low Temperature Storage (LTS)*IEC 60068-2-1*	1,000 h, $T_{stg(min)}$	1,000 h, $T_{stg(min)}$
Thermal Cycling (TC) *IEC 60068-2-14 Test Na*	100 cycles, $T_{stg(max)} – T_{stg(min)}$	25 cycles $T_{stg(max)} – T_{stg(min)}$
Power Cycling (PC) *IEC 60749-34*	20,000 load cycles, ΔT_j = 100 K	10,000 load cycles, ΔT_j = 100 K
Vibration *IEC 60068-2-6 Test Fc*	Sinusoidal sweep, 5 g, 2 h per axis (x, y, z)	Sinusoidal sweep, 5g, 2 h per axis (x, y, z)
Mechanical Shock *IEC 60068-2-27 Test Ea*	Half sine pulse, 30 g, 3 times each direction (±x, ±y, ±z)	Half sine pulse, 30g, 3 times each direction (±x, ±y, ±z)

Table 2.7.1 Overview of SEMIKRON reliability tests, test conditions and relevant standards

Before, during and after test completion, relevant component parameters are measured in order to estimate the test influence on component lifetime. Faulty means that the component shows the following change:

Thyristors / diodes

Direct reverse current / direct off-state current I_{RD}/I_{DD}:	+ 100% above the upper limit
Gate trigger voltage / current V_{GT} / I_{GT}:	+ 10% above the upper limit
On-state / forward voltage V_T / V_F:	+ 10% above the upper limit

IGBT / MOS

On-resistance / saturation voltage $R_{DS(on)}$, V_{CEsat}:	+ 20% of start value
Max. change in threshold voltage $V_{GS(th)}$, $V_{GE(th)}$:	± 20% of the limits
Gate leakage current I_{GSS} / I_{GES}:	+ 100% above the upper limit
Drain-source current / collector-emitter cut-off current I_{DSS} / I_{CES}:	+ 100% above the upper limit

All modules

Internal thermal resistance junction to case $R_{th(j-c)}$:	+ 20% of start value
Isolation test voltage V_{isol}:	specified limit

A datasheet describes a product at the point of shipping to the customer. Changes that occur throughout the product lifetime are not covered in the datasheet. This is in conflict to some documents of the semiconductor standard IEC 60747 which requires (latest amendment) that the upper parameter limits be met even after completion of the endurance tests.

2.7.3.1 High Temperature Reverse Bias Test (HTRB), High Temperature Gate Bias Test (HTGB), High Humidity High Temperature Reverse Bias Test (THB)

These three tests are primarily used for qualifying the respective chips regarding their blocking capability, the passivation and gate oxide quality. They are performed in climatic chambers with voltage applied. Leakage or respectively reverse currents are monitored during testing. After test completion, the static electrical parameters are queried as described above.

2.7.3.2 High and low temperature storage (HTS, LTS)

Storage at extreme temperatures ensures above all the case quality when exposed to high thermal stress. At the end of the test, the cases must not show any signs of damage (e.g. cracks).

2.7.3.3 Temperature cycling test (TC)

In this test, components are periodically moved up and down between a cooling chamber and a heating chamber with the aid of a lift cage (Figure 2.7.2). The component is passively heated up. Test times are relatively long so that all parts of the sample will have adopted the chamber temperature. This test shall detect critical mechanical stress in the case itself and between layers with different thermal expansion coefficients. In particular large solder areas between DBC and copper base plate are under stress. The test simulates passive heating up caused by day and night change or by heat curves of the cooling medium. 100 changes between minimum and maximum storage temperature are usually required for industrial applications (-40°C/+125°C). Modern components with sintered chips and without base plate will attain 1,500 changes and more.

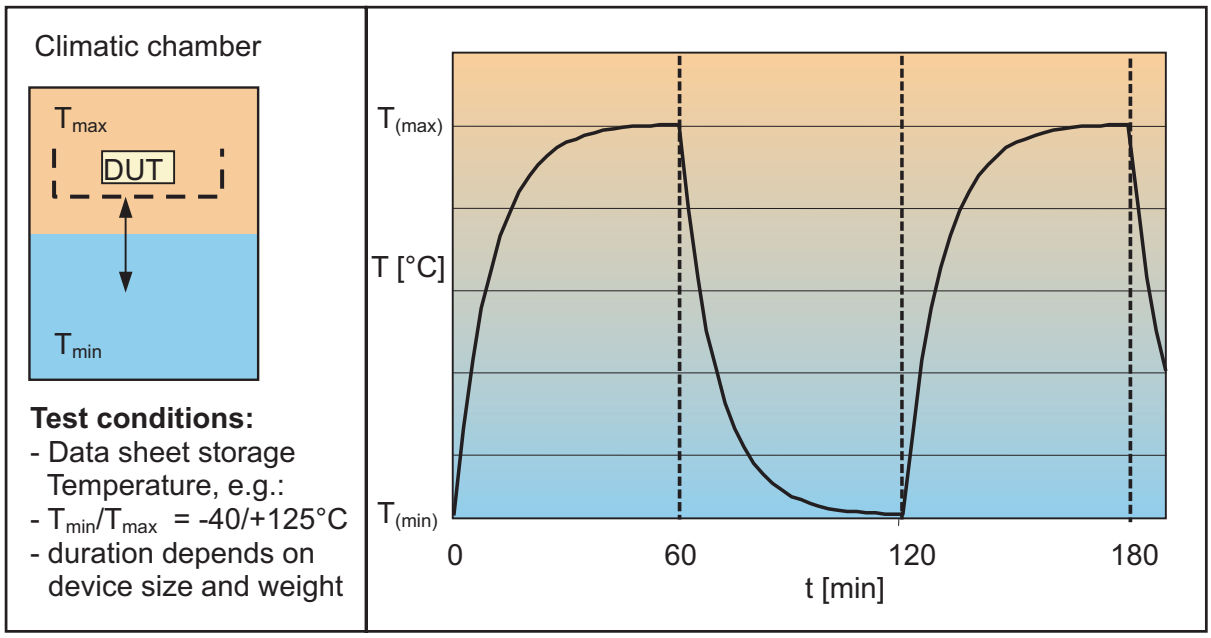


Figure 2.7.2 Temperature cycling test: test set-up and measurement method

2.7.3.4 Power cycling test (PC)

During the power cycling test, components are actively heated up by losses in the semiconductor and cooled down again with the aid of cooling equipment (Figure 2.7.3)

To heat the component up, a constant DC current equalling the rated current is injected into the component. The cycle time is between some seconds and some 10 seconds. Active heating produces a temperature gradient from the chip to the case and the cooling medium.

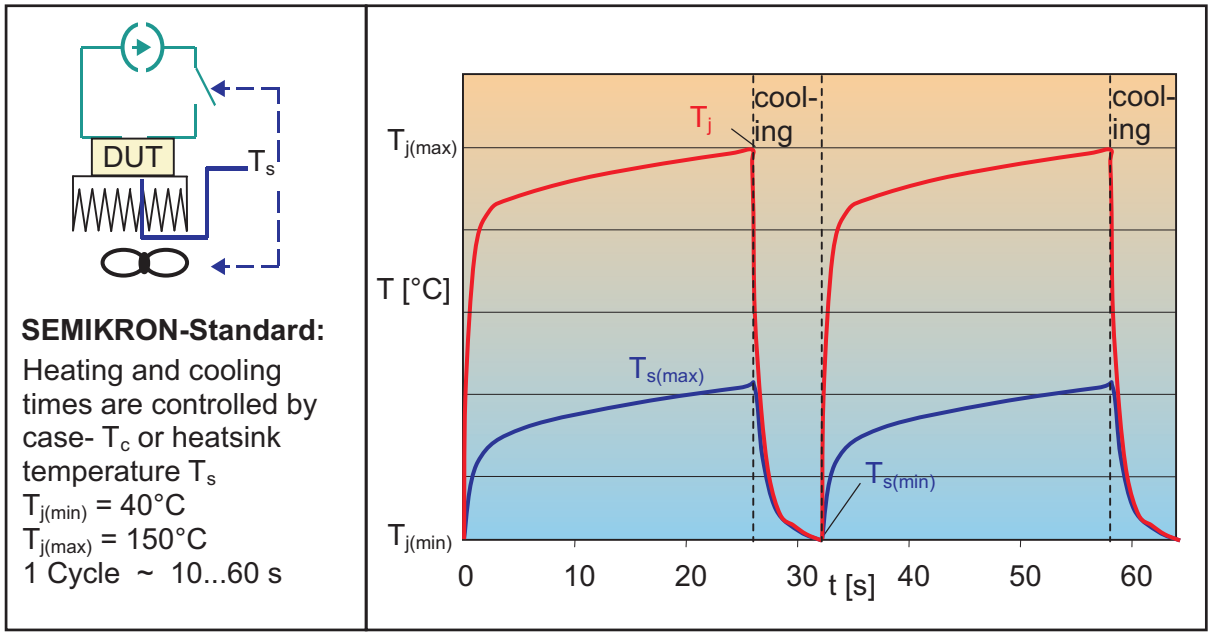


Figure 2.7.3 Power cycling test: test set-up and measurement method

This test shall detect thermo-mechanical stress between layers with different thermal expansion coefficients. Connections between chip and DBC as well as bond wire connections are particularly subject to stress because they heat up most. The test simulates active heating up of the semiconductors as they would be exposed to during normal operation due to different kinds of stress. The result is presented in form of characteristic curves for the maximum number of cycles as a function of temperature differences. The curves are based on the simplified assumption of uniform failure mechanisms over the entire temperature range. In order to speed up testing, tests are performed

with high ΔT values (e.g. for ΔT = 80 K and ΔT = 110 K) and extrapolated to small temperature differences to estimate the component lifetime in real applications.

2.7.3.5 Vibration test

Vibration tests are performed in a frequency range between 10 Hz and at least 1000 Hz using an acceleration force of 5 g. Increased acceleration is possible. Depending on the test equipment, there may be limitations regarding the minimum frequency to be used in connection with high acceleration. The test purpose is to find weak points in the mechanical construction, for example:
- Mechanical aging of spring contacts
- Stability of solder contacts in case of vibrating masses
- Cracks in cases / structural parts

A low test current monitors safe contact of all auxiliary and main terminals during testing. No additional vibrating masses (cables, DC-link capacitors) have been fitted to the samples, as it would often be the case later in real applications. Comparable tests using the set-up of the final application are recommended and may result in different maximum accelerations.

Figure 2.7.4 SKiiP system on a vibrating plate

2.7.4 Additional tests for spring contacts

Additional tests for contact reliability even under extreme conditions are performed to qualify spring contacts [44].

2.7.4.1 Micro-vibration (fretting corrosion)

Contact surfaces may corrode under electrical load and the influence of micro-vibrations. Material abrasion is caused which may result in contact failure. The test objective is to check whether good electrical contact is ensured for the specific combination of spring material and recommended contact surface of the PCB until the end of service life. The test simulates vibrations through a piezo actuator (Figure 2.7.5) (frequency: 1 Hz, amplitude: 50 µm). The contacts are monitored during testing. In order to suppress "clean-burning" of the contacts (i.e. re-establishing good contact), currents are limited to 20 mA and voltages to 20 mV.

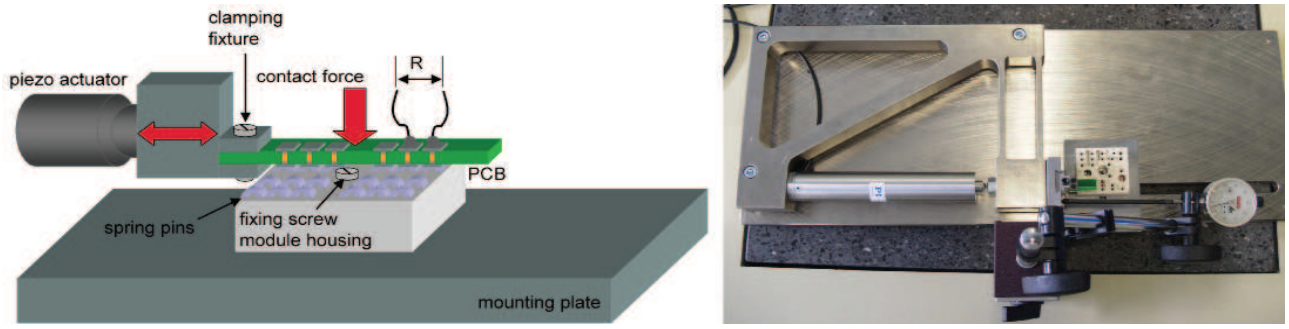


Figure 2.7.5 Schematic drawing and photograph of the micro-vibration test, exemplary test of MiniSKiiP springs

According to [45], a spring contact is considered "good" if the contact resistance after 100,000 movements is < 10 mΩ. The springs of the 2nd generation MiniSKiiP will survive more than 4.5 million movements.

2.7.4.2 Corrosive atmosphere (pollution gas test)

In a sealed chamber, components are exposed to aggressive atmosphere for several hundred hours. This is an accelerating test which shall simulate the corrosive effect of environmental impact with the aid of extreme ambient conditions.

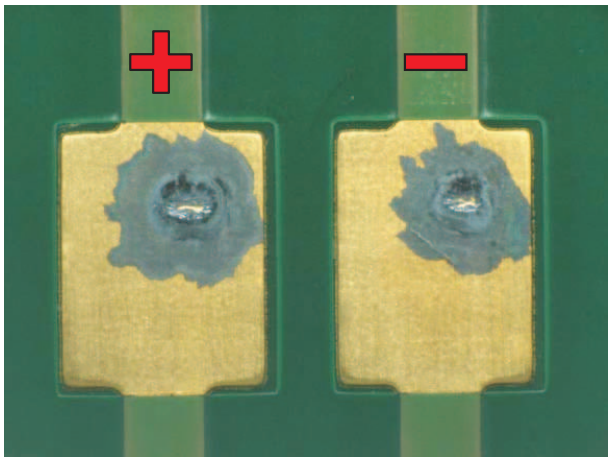


Figure 2.7.6 Pollution gas test of MiniSKiiP springs on a PCB (3 ppm H_2S, 40°C, 80% RH, 2,000 h, 15 V)

Figure 2.7.6 shows the contact surfaces of a MiniSKiiP PCB after successful testing. In order to test simultaneously whether there is the hazard of electromigration for this combination of metals (PCB / spring contact), voltage is applied to the sample. There are no signs of electromigration visible (ion migration towards the electric field). What is visible are grey spots on the Ni / gold flash of the PCB because of the corrosive atmosphere caused by the tarnish protection of the spring and black traces of oxidation. These are largely symmetrical around the contact point. The metal / metal contact areas in the middle are clearly visible as well. Owing to the high pressure of the springs against the landing pads, these are almost hermetically sealed against the outer atmosphere. Reliable contact will also be ensured after the test [46].

2.7.4.3 Contact-to-PCB temperature cycling

In this test, the contact of a power semiconductor module is exposed to extreme temperature fluctuations when mounted or soldered. The solder contact breaks due to its rigid connection after about half the test period, the flexible spring contact survives the test of 2,000 temperature cycles from -40°C to +125°C.

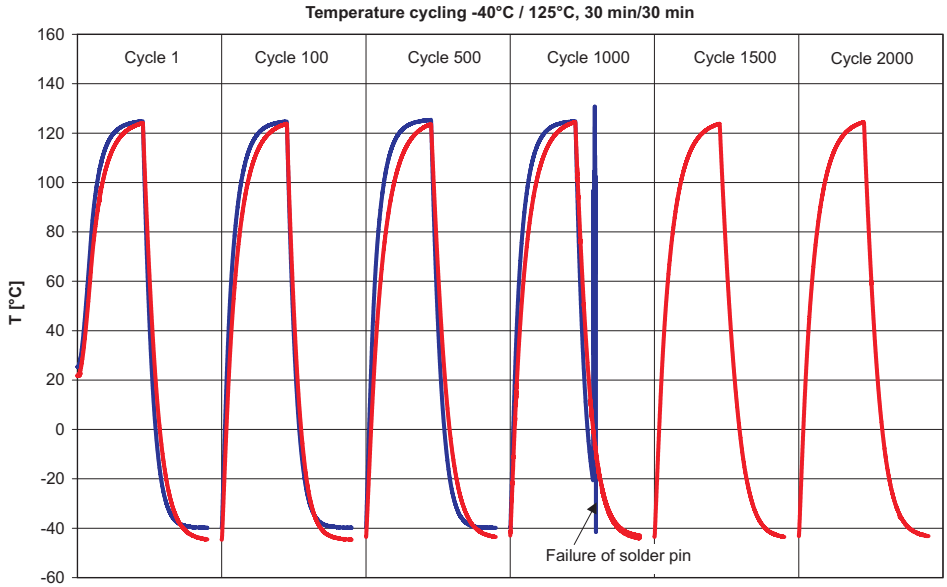


Figure 2.7.7 Contact reliability comparison of solder pin and spring contact (HAL-Sn PCB, Ag spring pin, Ni / Au-flash DBC) after mounting on a PCB subject to temperature cycling.

2.7.5 Failure mechanisms during power cycling

The thermo-mechanical stress between materials with different expansion coefficients CTE leads to aging of connections when they are exposed to temperature changes. Which of the mechanisms will eventually cause component failure depends on the load and cooling conditions. The further the connection is away from the chip, the longer it takes to heat it up completely. The worse the power semiconductor is cooled, the more all layers are raised to the temperature level of the chip. It is therefore useful for an increase of the power cycling capability to make improvements to the most exterior source of failure (= closest to the heat sink). Damage here will increase the ΔT of all connections located above and cause them to fail as well. The development of modules without base plate eliminated "base plate solder" as the source of failure in the Nineties. The introduction of sinter technology to replace chip solder pushes the failure limit for this type of connection further up and makes the bonded connections the weakest link in the chain. The improvements of bonded connections introduced in recent years now result in significantly higher power cycling figures than technically feasible 10 to 15 years ago. Figure 2.7.8 explains the structural details relevant to the life of an IGBT.

Figure 2.7.8 explains the structural details relevant to the IGBT module life.

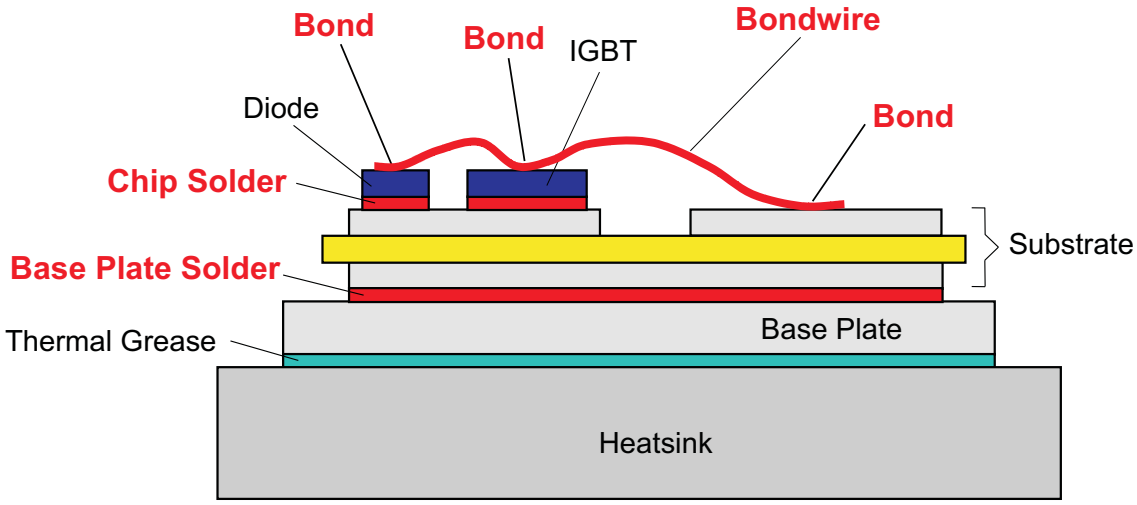


Figure 2.7.8 Structural details of an IGBT module (connections that are relevant to module lifetime are marked red)

Figure 2.7.9 and Figure 2.7.8 show that the solder connection of the substrate to the copper base plate is the most critical connection, since it covers by far the biggest area (given average differences in the thermal expansion coefficients of the adjacent materials). For this reason, high-quality solders and sophisticated soldering procedures have to be applied in order to avoid deformation and destruction of the module plates also in case of high temperature cycling amplitudes. In addition, DBC substrates are often divided up to keep the absolute difference of the expansion coefficient as small as possible by reducing the solder areas. Other module developments are replacing copper as base plate material by a material with a smaller expansion coefficient (such as AlSiC) or eliminate it completely.

Figure 2.7.9 shows the theoretical linear expansion for different layers with an edge length of 1 cm. The bars show the differences true to scale. Huge differences in length are an indication of considerable stress. On the left, the temperature ratios of a typical application condition are assumed with T_c=80°C and T_j= 125°C. The temperature gradient in the module has the effect that the copper base plate will only extend to about double the length of the chip despite its 4-fold CTE. Whereas passive heating up, e.g. caused by cooling water in the car, results in linear expansions that correspond to the CTE ratios, as shown on the right. The table also demonstrates that an AIN ceramic substrate is better adapted to silicon. In turn, the stress between AIN ceramics and copper base plate is increased so that this combination can be used with restrictions only, or not at all. AIN ceramics and AlSiC base plate constitute a better combination under the aspect of module service life. Al_2O_3 ceramics is in between the thermal expansion of Si and Cu and therefore makes an ideal intermediate layer for modules with a copper base plate. Bond wires are not connected via large-area joints. The linear expansion shown here results in wire bending. The comparably small bond foot, however, is subject to particular stress due to the great difference in the CTE of silicon chip and aluminium bond wire.

Material	CTE 10^{-6}/K	T [°C]	ΔT [K]	Δl Power Cycling	T [°C]	ΔT [K]	Δl Temperature Cycling
Chip (IGBT) Si	3,5	125	100	3.5µm	125	100	3.5µm
AIN -DCB	8,2	105	80	6.6µm	125	100	8.2µm
Al_2O_3 - DCB	10,7	105	80	8.6µm	125	100	10.7µm
AlSiC base plate	7	80	55	3.8µm	125	100	7µm
Cu base plate	17	80	55	9.4µm	125	100	17µm
Bond wire Al	23	100	75	17.2µm	125	100	23µm

Figure 2.7.9 Linear expansion of different material layers in a power semiconductor module with an assumed edge length of 1 cm. Left: for a temperature gradient in the module as for a typical power cycle; right: for heating up the entire module as for temperature cycling with identical ΔT

Solder fatigue on the base plate

Large-area soldering of a module base plate is stressed in particular in slow processes and intense heating up. At first, the solder connection will start cracking at the corners. As a result, the thermal resistance of the module will increase. This may cause chip overheating and speed up other failure mechanisms so far that they will then produce a failure. The quality of base plate soldering is safeguarded by temperature cycling tests.

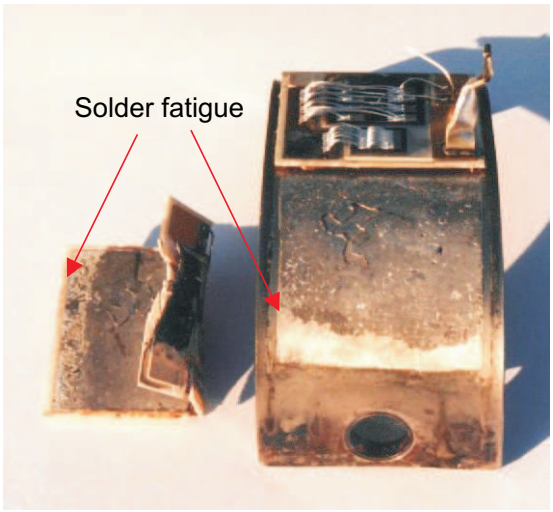


Figure 2.7.10 34 mm module with torn off DBC (light-coloured areas show solder fatigue)

It has become very obvious that one of the main causes for wear and tear can be eliminated by doing without a base plate and the necessary soldering, as long as the heat transfer from the substrate to the heat sink can be sufficiently ensured by other means and the disadvantages of reduced heat spreading can be compensated. This has been achieved with SKiiP, MiniSKiiP, SEMITOP and SKiM technologies (see chapter 2.5).

Solder fatigue in chip soldering

Solder fatigue in chips mostly appears together with damage of the bond wires. The more the whole module heats up, the more the solder connection is strained. Solder fatigue leads to an increase in R_{th} and the chip temperature, which in turn will cause higher losses and thus a higher temperature difference ΔT in the IGBT. In the end, the aging process is accelerated.

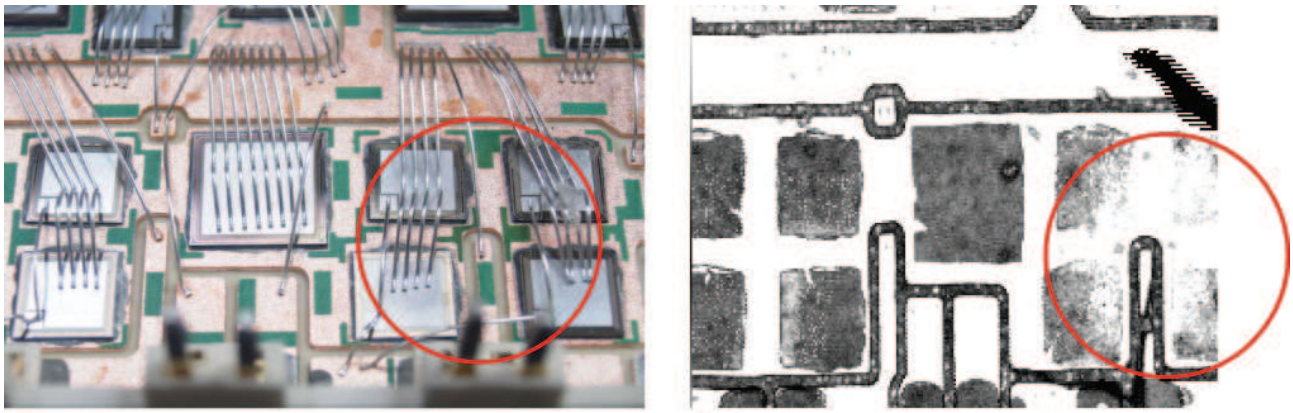


Figure 2.7.11 Chip solder fatigue caused by power cycling test, a) Photograph, b) Ultrasound image

The four IGBT chips (Figure 2.7.11) on the right of the DBC substrate underwent power cycling, the other IGBT chips and CAL diode chips on the left did not. In the ultrasound image (SAM = **S**canning **A**coustic **M**icroscope), delamination after power cycling can be seen. The four parallel, jointly current-carrying IGBT have their hottest spot in the centre. It can be clearly seen that delamination starts right there at the inner corners. For larger chips, the temperature gradient over the chip area might result in damage at the centre where the temperature ΔT is highest, rather than at the edges, as is usually the case [47]. This effect will become more and more important in the future with an increase of the permissible chip temperature (e.g. to 175°C) and the resulting higher ΔT. The temperature cycling capability of the backside soldering of the chips to the substrate can be improved by

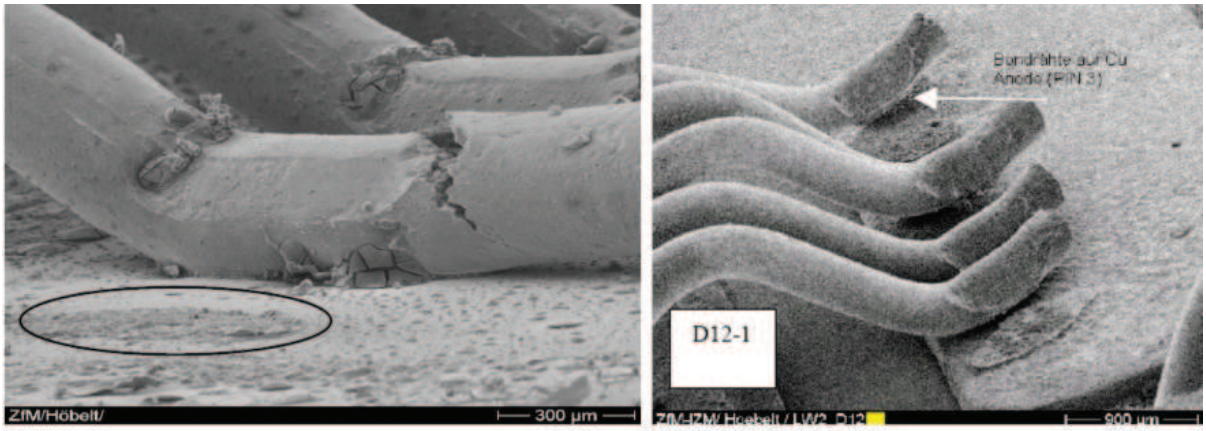
- using AlN substrates whose thermal expansion coefficient differs less from that of Si than is the case with Al_2O_3

- substituting the soldering with low-temperature joining technique. The connection between chips and substrate is made by sintering silver powder at comparably low temperature and high pressure, which will already minimise thermal stress between the materials during production.

Bond wire lift-off or breakage

In comparison with copper and silicon, aluminium has a relatively high thermal expansion coefficient. This damages the welded connection of the bond feet ("lift-off") and, due to changes in the length of the bond wires, even the kink at the bond foot becomes damaged ("heel crack"). Further movement is caused by temperature-related bending of the module base plates and in addition to thermal movement also by mechanical stress (e.g. owing to high current surges). The soft moulding with silicone applied in the power modules will absorb these mechanical vibrations.

Since power modules with rated currents > 10 A per chip have more than one bond wire positioned in parallel, a loss of bond wire contact will not immediately result in component failure. Contact losses will become noticeable by a escalation of the forward voltage in the power cycling test. Those parallel, not yet fully destroyed bond wires must now carry additional current, the bond feet will be heated up even more. Thus their aging process is further accelerated. In the last bond wire left, the current density will then be so high that the metallisation will start melting, an internal arc will occur and eventually the chip will be destroyed. A pure circuit interruption ("open terminals"), however, is very rare in practice.



a) b)

Figure 2.7.12 Bond wire damage; a) Breakage and lift-off at the marked area; b) Failure due to bond wire lift-off [48]

The main weak points of bond connections are the aluminium bond wire area right above the ultrasonic bonds, whose crystalline structure is impaired by bonding. Thanks to new wire alloys, improved bonding tools and optimised control of the bonding processes over time, the bond lifetime could be doubled in recent years. Thus, [49] has proven the correlation between the angle of inclination of the bond wire and the maximum number of possible power cycles. The angle of inclination is proportionate to the loop height to width ratio.

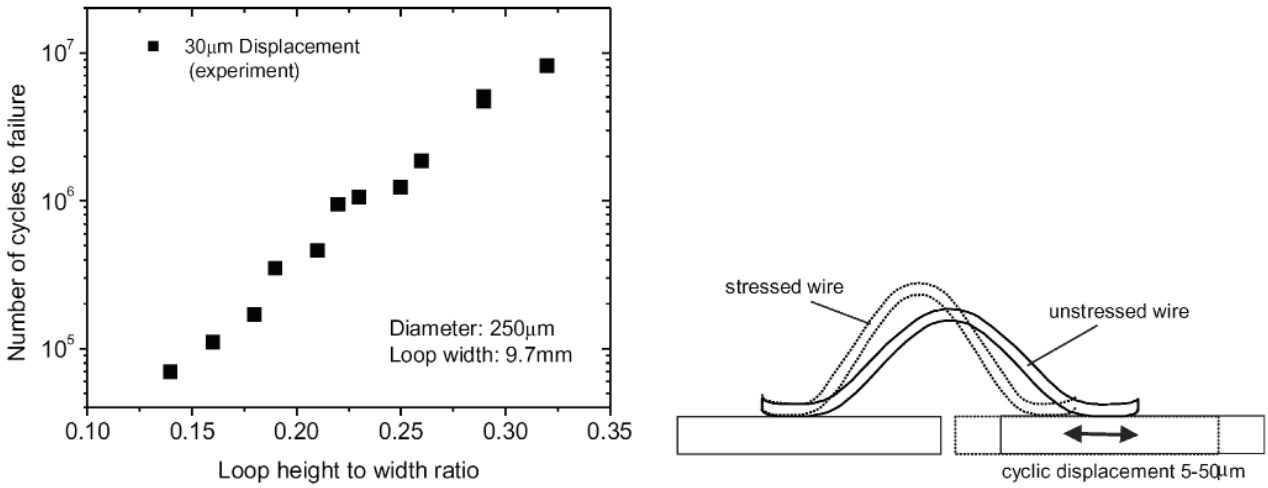


Figure 2.7.13 Function of bond wire loop height to width ratio in relation to power cycling capability [49]

"Bond wire failure" can be eliminated as cause of failure by using double-sided pressure contact, as is found in disk cells, for example. Bond connections in IGBT and diode disc cells have been replaced by pressure contacts with an inherent higher temperature cycling capability [50].

Reconstruction of chip metallisation

This is another aging process that is induced by power cycling. This process is accelerated by high current amplitudes. Changes in the chip metallisation gradually increase the chip resistance causing additional losses, higher ΔT and a worse adherence of the bond wires, thus accelerating the failure process. Limiting the repetitive current load (I_{CRM}) is therefore necessary.

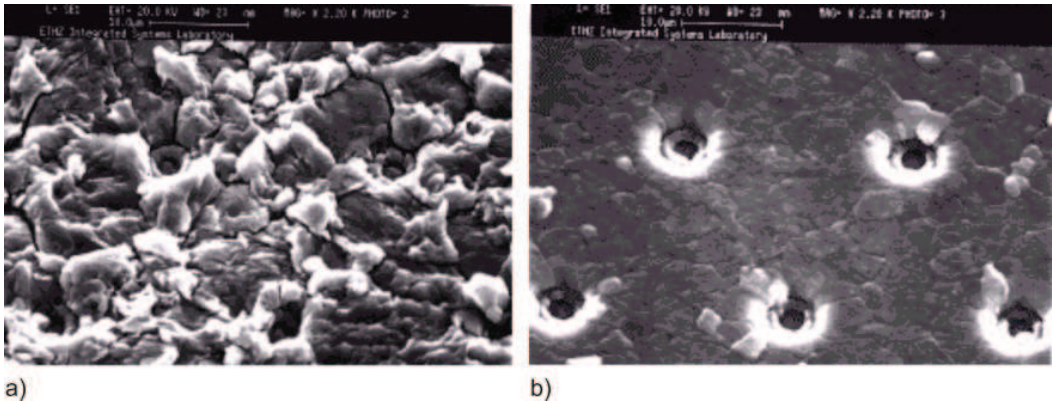


Figure 2.7.14 Reconstruction of chip metallisation, a) before and b) after power cycling [51]

2.7.6 Evaluation of temperature curves regarding module lifetime

As mentioned here and in chapter 2.5 (Packaging), all internal connections of power modules are subject to aging caused by temperature fluctuations. The fatigue of material as well as wear and tear is caused by thermal stress due to the different expansion coefficients of the connected materials. Module lifetime or respectively, the number of possible temperature cycles, declines as a function of the rising ΔT_j.

Alterations of power loss below a frequency of some 100 Hz will no longer be smoothed by the transient thermal impedance of the chips and will lead to a minimal temperature fluctuation in the module (chapter 5.2 Balance of power losses). At this frequency, however, ΔT is so small and low-energy that it is counterbalanced by elastic deformations, or the aging effect is so weak that it is unimportant for lifetime evaluations. During normal operation at frequencies of few Hz and especially at duty cycle operation, such as prevailing in traction, lift and pulse applications, the internal connections in a module will be exposed to temperature cycling, such connections being:

- Bonded connections
- Rear chip soldering
- DBC / base plate soldering
- And substrate lamination (Cu on Al_2O_3 or AlN)

Therefore, it is important for thermal dimensioning to check whether ΔT_j is so high that the projected number of power cycles will not be reached. In this case, the temperature difference $\Delta T_j = T_{j(max)} - T_{j(min)}$ during the power cycles under analysis constitutes the rating criterion for the power module and not the maximum permissible chip temperature $T_{j(max)}$.

The correlation between the possible number of power cycles n and the temperature cycling amplitude ΔT_j is determined by many parameters. Corresponding measurements require a lot of time and effort. The first extensive tests in which the dependency of temperature cycling on the mean temperature T_{jm} was verified were published in the LESIT Study in the late 1990s [52]. With the aid of parameter adjustment for A, α and the activation energy E_a the study results with respect to lifetime function can be analytically calculated using the following equation:

$$N_f = A \cdot \Delta T_j^{\alpha} \cdot e^{\left(\frac{E_a}{k_b \cdot T_{jm}}\right)}$$

adjusted parameters for the points in Figure 2.7.15: $A=3.025 \cdot 10^5$, α = -5,039, $E_a=9.891 \cdot 10^{-20}$ J, k_b – Boltzmann constant, ΔT_j & T_{jm} [K]

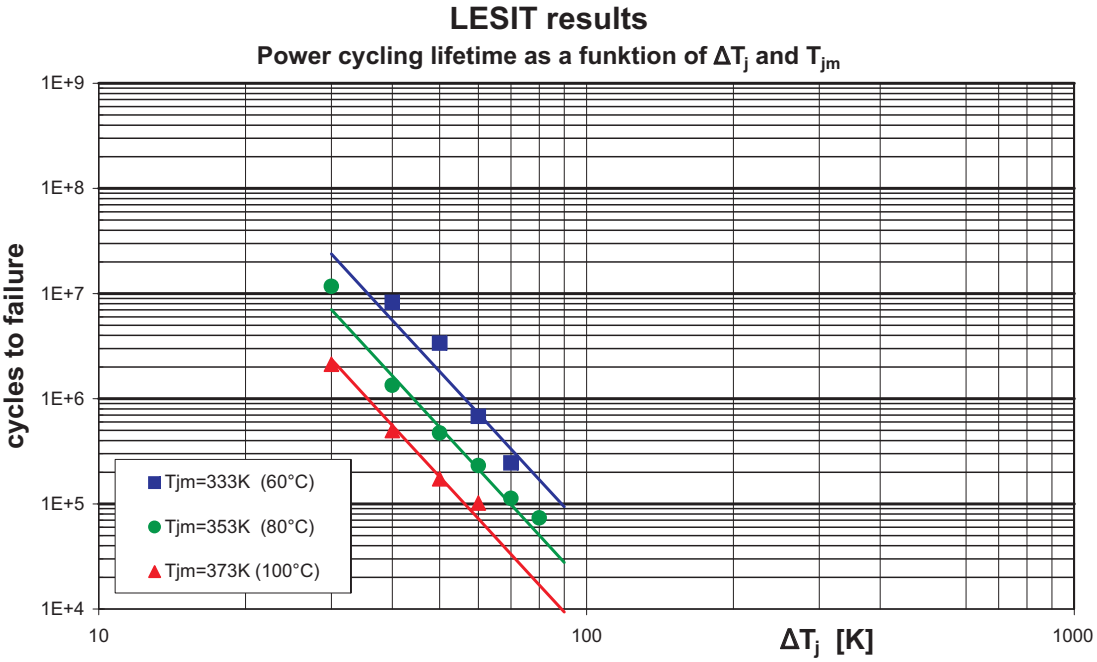


Figure 2.7.15 Power cycling curves as established for power modules in dependency of different mean temperatures in the LESIT Study [52]

As Figure 2.7.15 demonstrates, the number of possible power cycles for ΔT_j > 30 K declines by a power of ten for every increase in temperature cycling amplitude by 20...30 K. Periodical power cycling within seconds or minutes thus requires temperature cycling amplitudes below 30 K. These curves were established with modules from various manufacturers and represent the past state of the art. Packaging has improved, so that present-day power semiconductor modules will attain higher power cycling values. These values have been summarised for IGBT modules in two groups in the following illustrations.

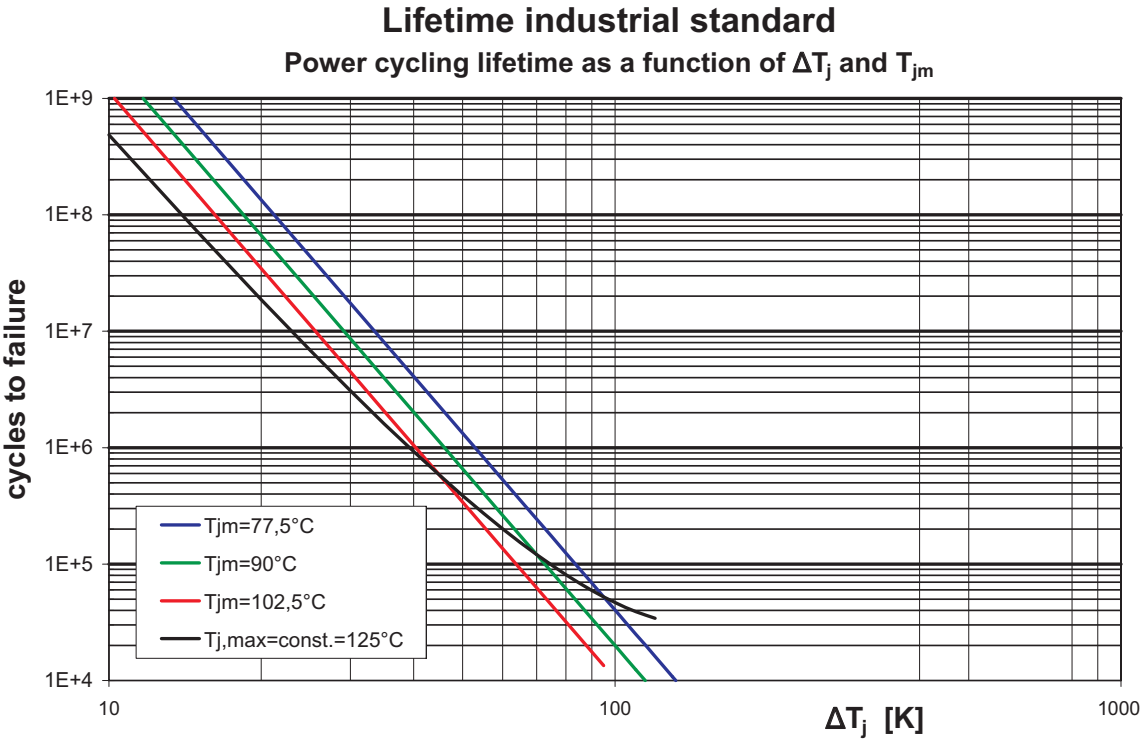


Figure 2.7.16 Dependency of the power cycling value n as a function of the temperature cycling amplitude ΔT_j and the mean temperature T_{jm} for all of the IGBT modules that do not use IGBT4 chips (as per 2009); also see the following diagram

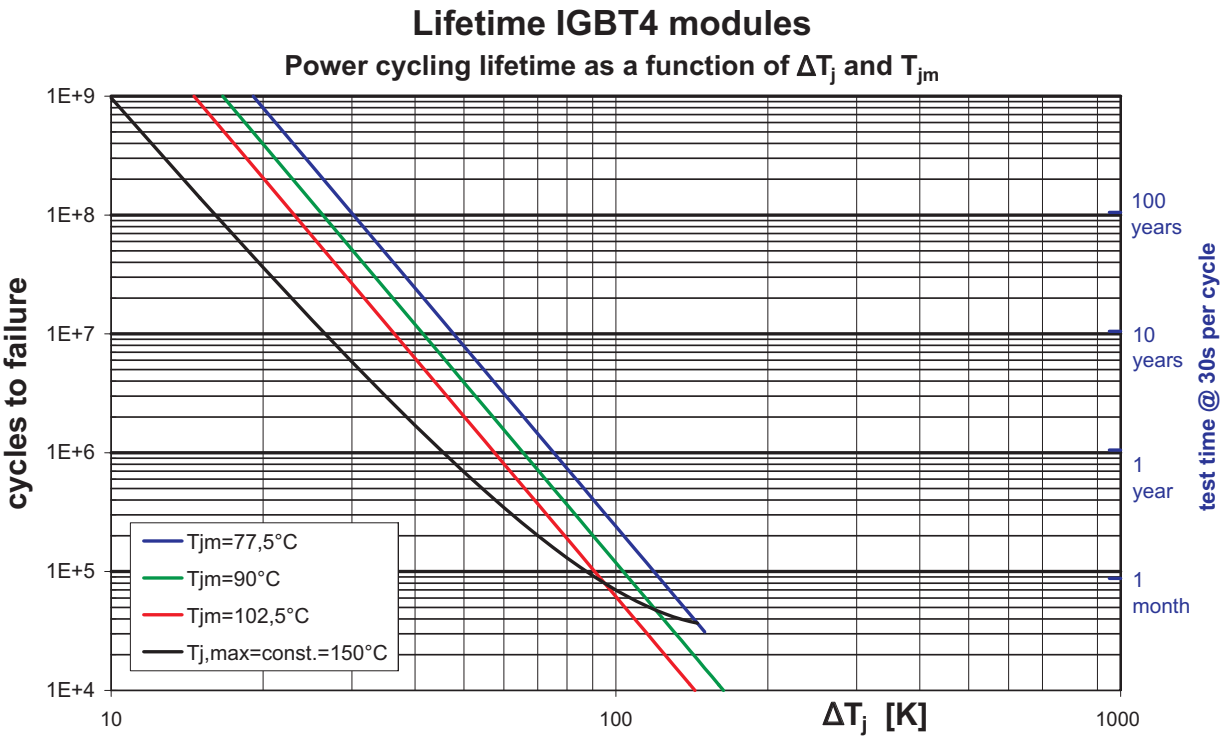


Figure 2.7.17 Dependency of the power cycling value n for IGBT4 modules as a function of the temperature cycling amplitude ΔT_j and the mean temperature T_{jm} (date: 2009); right: the necessary test duration for a cycle time of 30 s

The LESIT curves consider the effect of the mean temperature or respectively, the temperature level where the temperature cycling takes place. Many test results indicate, however, that other parameters, such as pulse duration t_{on} and the current amplitude I_B will influence the test results just as much as packaging parameters such as bond wire thickness and bond wire angle of inclination or chip and solder thicknesses. In [53] an extended model based on the analysis of a great

number of tests is shown. Parameters, validity limits and coefficients are listed in the following table:

$$N_f = A \cdot \Delta T_j^{\beta_1} \cdot \exp\left(\frac{\beta_2}{(T_{j,min} + 273)}\right) \cdot t_{on}^{\beta_3} \cdot I_B^{\beta_4} \cdot V_C^{\beta_5} \cdot D^{\beta_6}$$

Parameters	Symbol	Unit	Limits	Coefficient	Value	Comment
Technology Factor	A				2.03E+14	Standard
Technology Factor	A				9.34E+14	IGBT4
Temperature difference	ΔT	K	45…150	$\beta 1$	-4.416	
Min. chip temperature	$T_{j(min)}$	°C	20…120	$\beta 2$	1285	
Pulse duration	t_{on}	s	1…15	$\beta 3$	-0.463	
Current per bond foot	I_B	A	3…23	$\beta 4$	-0.716	
Voltage class/100	V_C	V	6…33	$\beta 5$	-0.761	
Bond wire diameter	D	µm	75…500	$\beta 6$	-0.5	

Table 2.7.2 Parameters and limits for the calculation of power cycles using the equation above

Example: Let us assume a given number of power cycles N_f and a test duration $t_{on(test)}$. If a component would be used for a different pulse duration $t_{on(application)}$ in the application, this would equal to

$$N_{application} = N_{test} \cdot \left(\frac{t_{on(application)}}{t_{on(test)}}\right)^{\beta_3}$$

This means, if the application pulse duration is 1/10 of the test pulse duration, the lifetime would roughly triple. This model gives a good impression of the impact of various parameters on power cycling figures, but it is only suitable to a limited extent in order to calculate concrete lifetime values isolated from any other parameter. The reason are physical constraints, since not all of the parameters are independent of each other. For example, a small ΔT_j is not possible in the event of high currents and long pulse durations. Or, as assumed for the pulse duration in our example, an identical ΔT would require different current values for different pulse durations t_{on}.

3 Datasheet Ratings for MOSFET, IGBT, Diodes and Thyristors

3.1 Standards, symbols and terms

3.1.1 Standards

The practical usage of symbols and terms and their meaning is described in the international standard IEC 60747 "Discrete Semiconductor Devices". Detailed information on the parameters, minimum requirements for datasheet ratings and test methods is provided in the standard's product-specific sections.

- IEC 60747-1 General (letter symbols and terms)
- IEC 60747-2 Diodes
- IEC 60747-3 Thyristors
- IEC 60747-8 Field effect transistors
- IEC 60747-9 IGBT
- IEC 60747-15 Isolated power semiconductor devices

Other important standards applicable to semiconductor devices:

- IEC 60191-2 Mechanical standardisation of semiconductor devices, Part 2: Dimensions (standardised case drawings)
- DIN EN 50178 Electronic equipment for use in power installations (insulation tests, partial discharge)
- IEC 60664 Insulation coordination for equipment within low-voltage systems (clearance and creepage distances)
- IEC 60721 Classification of environmental conditions
- IEC 60068 Environmental testing (specification of test conditions)
- IEC 60749 Mechanical and climatic test methods

The following specifications and standards do not correspond with international standards in use, but are applicable to particular markets:

- UL94 Flammability tests for plastic parts used in devices and appliances
- UL508C Power conversion equipment
- MIL-STD-750E Test methods for semiconductor devices

3.1.2 Letter symbols and terms

Voltages: Two index letters are used to designate the terminals between which the applied voltage is measured. If the potential of the terminal designated with the first index letter is positive versus the terminal designated with the second index letter (reference potential), the applied voltage is positive, e.g. V_{CE}.

- C collector
- E emitter
- G gate
- D drain
- S source
- K cathode
- A anode

For diodes, the forward on-state voltage is indexed with "F" rather than "AK" ("forward" positive anode potential versus cathode potential); "R" is used to designate the reverse blocking voltage ("reverse" positive cathode potential versus anode potential). In the case of transistors, an additional third index letter may be used to determine the wiring status between the terminal with index 2 and a non-designated third terminal, e.g. V_{CES} indicates that the IGBT is "short-circuited between gate and emitter". The following abbreviations are permissible:

- S: short circuit
- R: resistance to be specified;
- V: external voltage to be specified;
- X: resistance and external voltage to be specified

Index letters may be followed or preceded by other indices to specify further parameters; these may (or may not) be in parenthesis and may be in upper or lower case, e.g. $V_{(BR)DS}$or $V_{GE(th)}$or V_{CEsat}):
- (BR): breakdown voltage;
- sat: saturation voltage;
- (th): threshold voltage;
- clamp: clamping voltage limited by external circuits.

Supply voltages are marked with double index letters, e.g. V_{GG} (supply voltage of a gate-emitter circuit), V_{CC}, V_{DD}.

Currents: Here, the index letter used designates the terminal at which the current enters the component (e.g. G=Gate, C=Collector) (e.g. I_G stands for gate current). Positive values specify positive currents. For diodes, "F" is used for forward on-state currents (anode-cathode) and "R" for reverse currents (cathode-anode). Exceptions to this rule of thumb are reverse and leakage currents, where a second index letter is used to designate the second terminal at which the reverse voltage is applied. In analogy to the indices used for voltages, an additional third index letter may describe the wiring status between terminal 2 and a non-designated third terminal, e.g. I_{GES}. Index letters may be followed or preceded by other indices; these may (or may not) be in parenthesis and may be in upper or lower case, e.g.:
- av: average value;
- rms: effective value (root mean square);
- M: peak value (maximum);
- R: periodic (repetitive);
- S: non-periodic (spike);
- puls: pulsed (direct current).

Thermal parameters: Temperatures are always indicated with a capital T. The following index letters are the most commonly used in the context of temperatures:
- j junction, formerly also "vj" for virtual junction
- c case (here, the heat-dissipating base plate is meant)
- s sink, formerly also "h" for heatsink
- r reference point (usually an integrated temperature sensor)
- a ambient (usually refers to the coolant temperature)

Temperature differences, thermal resistances (R_{th}) and impedances (Z_{th}) are designated with two hyphenated index letters describing the reference points between which they apply, e.g. $\Delta T_{(j-a)}$ or $R_{th(c-s)}$.

Mechanical parameters: These parameters refer predominantly to the assembly of components. Important mechanical parameters are torques (M) for screw terminals and heatsink connections, tractive forces (F) at terminals and surface characteristics of contact areas.

Other symbols: The terminology used for other electrical, thermal and mechanical parameters is largely based on the terminology for voltages and currents. Switching states (turn-on, turn-off) may also be specified with index letters (usually in brackets).

3.1.3 Maximum ratings and characteristics

Maximum ratings and characteristics are provided in the form of tables and may additionally be published in the form of diagrams.

Maximum ratings

The maximum module ratings indicated in the datasheets are extreme electrical, thermal and mechanical load values which are permissible without risk of destruction. Nevertheless, even within these limits every component is subject to the "usual" aging processes. All maximum ratings are determined under precisely defined conditions. It is mandatory to cite these in the datasheets. Deviating ambient conditions may result in different ratings, whose interdependencies are known to a certain extent only. Maximum ratings are absolute values, i.e. exceeding even one single rating may result in component destruction, even if other ratings have not been stretched to the limit. Apart from the "static" maximum ratings, "dynamic" maximum ratings also exist, i.e. limits for the permissible course of the characteristic (current/ voltage) during switching. Unless otherwise specified, the datasheet ratings apply to a chip or case temperature of 25°C; higher temperatures usually require derating.

Characteristics

The characteristics describe the component properties determined under certain (normally application-specific) measuring conditions. Here, too, the characteristics are based on very precise ambient conditions. As ambient conditions are not standard in given applications, it is imperative that they be explicitly specified in the datasheets. Characteristics are often given as typical values with a scattering range. The reference temperatures (chip or case temperature) are usually 25°C and a second, high temperature of, for example, 125°C or 150°C. For other temperatures, temperature dependencies have to be taken into account (cf. chapter 2).

3.1.4 Component (type) designation system

Case form	Current grade (& case size)	Circuit abbreviation	Blocking voltage (*100V)	Chip
SKM	200	GB	12	6
(Mini)SKiiP	39	AC	12	T4
SK	30	GD	06	5
SEMiX	453	GAL	12	E4
SKiM	606	GD	06	6
SKiiP	1814	GB	17	E4

In most cases (with the exception of MiniSKiiP) the current grade is the rated current at a specific case or heatsink temperature in A. The last digit of the current grade identifies the case type. Example: SEMiX453… is a 450A component in a SEMiX3 case.

The most important circuit identifiers for IGBT modules are as follows (also see chapter 2.5.2.7):
- GB half-bridge branch
- GA single switch
- GD/AC three-phase bridge
- GAL/GAR single switch with freewheeling diode for chopper (DC-DC converter) circuits

Further details on the various case types are given in the "Technical Explanations".

3.2 Rectifier diodes and thyristors

The datasheet ratings referred to in this chapter are not necessarily available for every component.

3.2.1 Temperatures

Virtual junction temperature T_j

This refers to temperature assigned to an area inside a semiconductor device where a virtual heat source provides thermal output originating from electrical power losses. The virtual junction temperature T_j is a virtual parameter and cannot be measured directly. It constitutes a theoretical average value from which the actual temperature at a chip pn-junction can differ significantly. This effect increases linear to chip size.

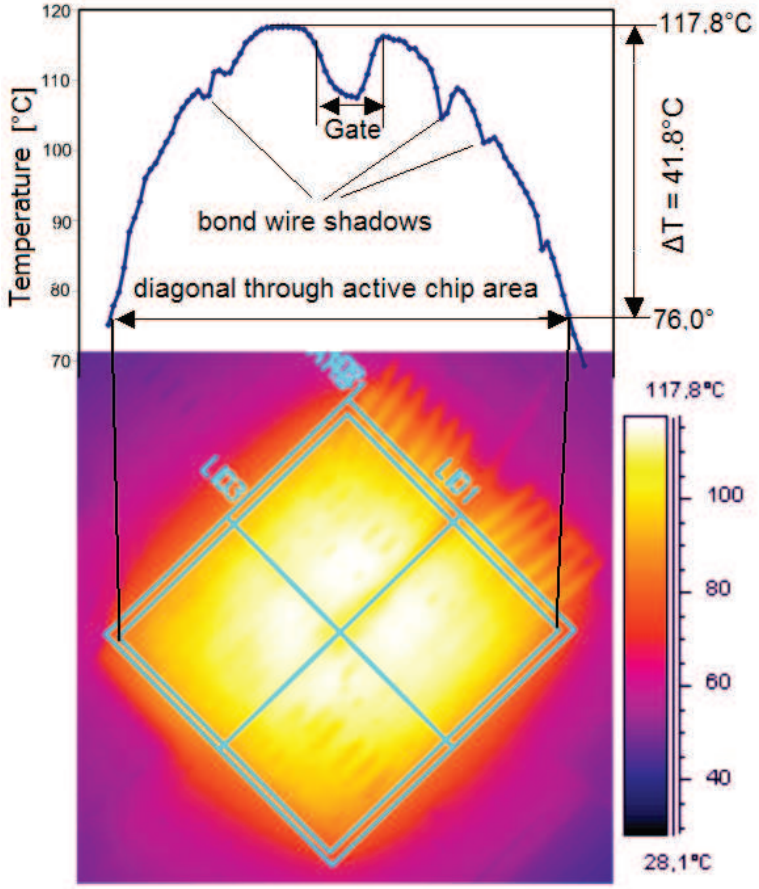


Figure 3.2.1 The bottom part of the illustration shows the infrared image of a live, bonded chip with an active area of 12x12 mm²; the scale on the right represents the assignment of temperatures to pseudo colours. The upper part of the illustration shows the evaluation of the infrared image in reference to the temperature measured across the chip

Figure 3.2.1 shows the temperature spread measured across a live chip. This reveals the large difference in temperature ($\Delta T = 41.8°C$) between the edges of the chip and the hot spot. The characteristic clearly shows the non-conducting gate area, as well as the heat absorbing activity of the bond wires. The temperature measured with the standard method using the negative temperature coefficient of the forward on-state voltage is equal to the average local chip temperature either measured across the active chip area with an infrared spectrophotometer or calculated by simulation.

Figure 3.2.2 describes the measurement method used to measure the virtual junction temperature T_j in any bipolar component. For low currents, the temperature coefficient of the on-state voltage will be negative. The linear dependency of the on-state voltage V_{ce} at constant current on temperature is shown on the right. If the on-state voltage is known, for example $V_{ce}(1)$ at 25°C and $V_{ce}(3)$ at 150°C, the chip temperature X can be easily calculated from the measured on-state voltage $V_{ce}(2)$ (provided the measurement current is constant).

$$T_{j(X)} = 25°C + \frac{V_{CE}(2) - V_{CE}(1)}{V_{CE}(3) - V_{CE}(1)} \cdot (150°C - 25°C)$$

The maximum virtual junction temperature is the most crucial limiting value for power semiconductors and the reference temperature for most characteristics at the same time. The virtual junction temperature T_j can be calculated from the (measurable) case temperature, the power losses and the thermal resistance (given in the datasheet) to check whether it is within the permissible limits (also see chapter 4.1).

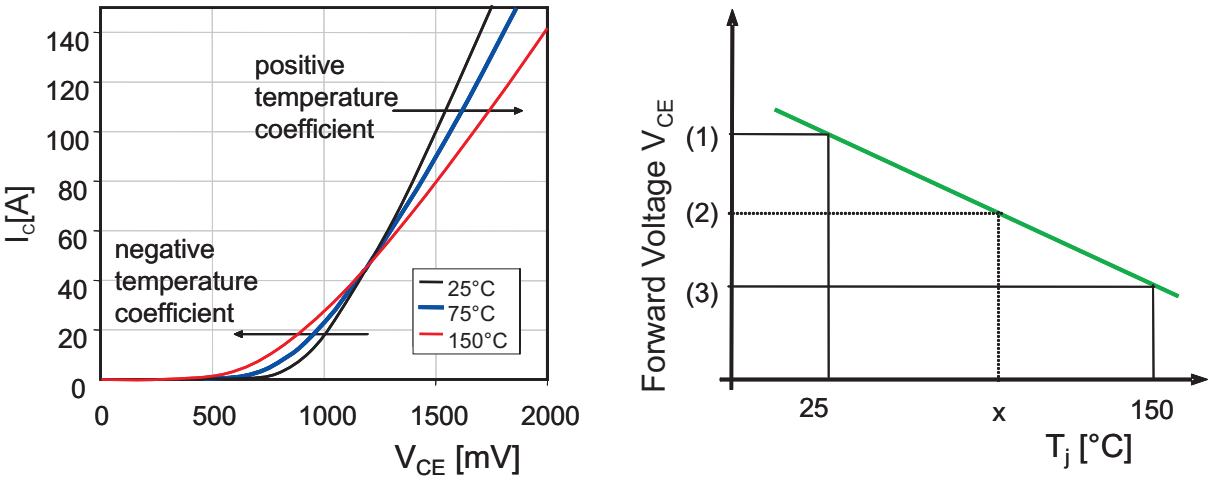


Figure 3.2.2 Temperature dependency of the forward voltage V_{ce} of a bipolar device

Case temperature T_c, reference point temperature T_r

Temperature at a fixed reference point of the case. For low-power devices in plastic enclosures, a difference is made between the case temperature (measured on the surface of the plastic case) and the reference point temperature T_r (taken at a fixed reference point of a terminal). For metal enclosed devices, both terms are interchangeable. For devices with an integrated temperature sensor, T_r designates the sensor temperature.

Heatsink temperature T_s

Temperature of the heatsink. The temperature T_s is taken at a fixed reference point inside the heatsink or on the heatsink surface next to a power semiconductor.

Ambient temperature T_a

Temperature at which the coolant (e.g. air) flows towards the semiconductor device or its cooling system. The coolant flow may be induced by convection (natural cooling) or effected by a fan or pump (forced cooling). As for liquid cooling, T_a indicates the temperature of the liquid coolant. Sometimes T_w is also used.

Operating temperature range

Permissible case, ambient, coolant or heat carrier temperatures within which the semiconductor device may be subjected to electrical load. The upper limit of the operating temperature is identical to the maximum permissible virtual junction temperature. At this point the permissible electrical load tends to zero, and all of the above-mentioned temperatures will be equal to the maximum permissible virtual junction temperature.

Storage temperature range T_{stg}

Temperature range within which a semiconductor device which is not under electrical load may be stored or transported.

3.2.2 Thermal impedance and thermal resistance

The thermal impedance is defined as a quotient of the time function of a temperature difference divided by the impressed power dissipation. In the datasheets this value is given as a function of time in the form of a diagram.

$$Z_{th}(t) = \frac{T_1(t) - T_2(t)}{P}$$

The static upper range value is the actual thermal resistance. This is indicated in the datasheets in the form of a characteristic. Depending on the choice of temperature detection points, distinctions are made. For example:

- $Z_{th(j-c)}$ / $R_{th(j-c)}$ junction-case
- $Z_{th(c-s)}$ / $R_{th(c-s)}$ case-heatsink
- $Z_{th(s-a)}$ / $R_{th(s-a)}$ heatsink-ambient
- $Z_{th(j-a)}$ / $R_{th(j-a)}$ junction-ambient

Since T_c and T_s depend on the position of the detection point, their shares of the total thermal resistance may vary. The total thermal resistance, however, is always calculated as follows (this also applies to Z_{th}):

$$R_{th(j-c)} + R_{th(c-s)} + R_{th(s-a)} = R_{th(j-a)}$$

The thermal resistance may be used to calculate true constant quantities, as well as average temperatures of periodic functions. Normally, however, the current conducted through a semiconductor device and, consequently, the power losses, are time-dependent parameters. In line rectifiers, the losses and temperatures vary within the bounds of the line frequency around a mean value. The virtual junction temperature T_j is higher under peak load than under direct current load or if calculated with a mean power loss P_{FAV}/P_{TAV} and R_{th}. The temperature fluctuation range depends on the current waveform and the current flow time within a cycle. With help of the thermal impedance, the effective junction temperature $T_j(t)$ can be calculated for any given duration of power dissipation. The datasheets of older components still contain auxiliary values. This is owing to the restricted methods of calculation at that time. These values should enable the user to factor in the load-dependent power loss and temperature fluctuation based on the operating frequency. Although not correct from a physics point of view, the static resistance R_{th} is used as a mathematical aid and is multiplied by a corrective factor in order to project the mean temperature to the maximum temperature value (Figure 3.2.3). The resulting value R_{th}, which is given either as a pure operand or in the form of a diagram, applies to the given current waveform and the lead angle for a frequency range of 40…60 Hz. In other words, **Rec120** stands for "rectangular current with a current flow time of 120°".

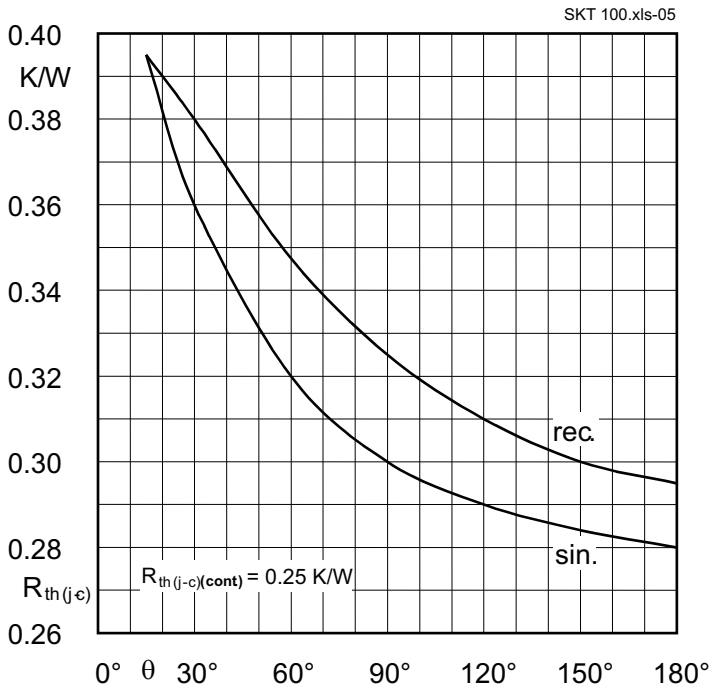
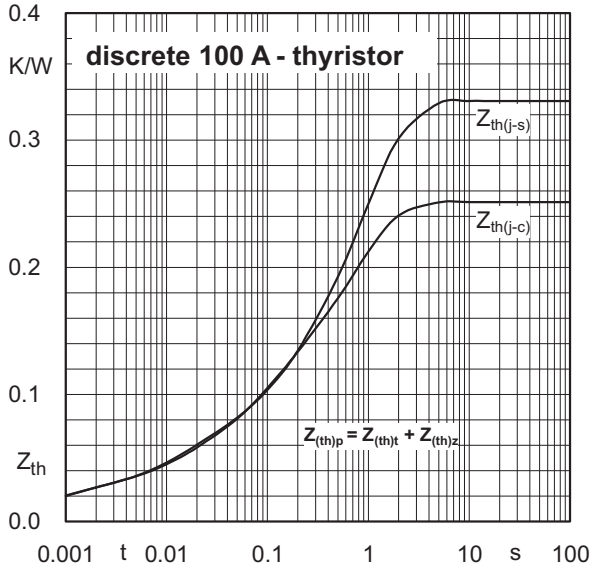


Figure 3.2.3 $R_{th(j-c)}$ of a discrete 100A thyristor multiplied by a corrective factor to calculate the temperature fluctuation as a function of the current conduction angle Θ and current waveform

Similar auxiliary parameters are, for example, the thermal **pulse impedance $Z_{th(p)}$** and the thermal **supplementary impedance $Z_{th(z)}$**.

$Z_{th(p)} = Z_{th} + Z_{th(z)}$

The thermal impedance is used to calculate the temperature change at a specified point in time after power dissipation has been effective. For this purpose, the mean on-state power dissipation P_{TAV} is normally averaged over one line frequency cycle. This temperature rise is also superposed by a fluctuation at operation frequency. This fluctuation can be calculated analytically using the thermal impedances for individual pulses and pulse sequences (see chapter 5.2.2.3 "Junction temperature during short-time operation"). Although not correct from a physics point of view, the thermal impedance is indicated with a supplementary value in former datasheets in order to infer the maximum temperature from the average dissipated power. For example, Figure 3.2.4 gives such supplementary impedances for different current conduction angles and waveforms.



Θ	$Z_{(th)z}$ (K/W)	
	sin.	rec.
360°	-	0
180°	0.03	0.04
120°	0.04	0.06
90°	0.05	0.075
60°	0.07	0.10
30°	0.11	0.13
15°	0.145	0.145

Figure 3.2.4 Z_{th} to case ($Z_{th(j-c)}$) and to heatsink $Z_{th(j-s)}$ of a discrete 100 A thyristor, and mathematical auxiliary parameter $Z_{th(z)}$ to calculate the temperature fluctuation at line frequency for different current conduction angles and waveforms

3.2.3 Mechanical data

Mechanical data is also included in the data sheets. The dimensions of the component are entered in the dimension drawing. The drawing also contains the internal and / or standard case designations. Very often, datasheets will also contain device photos. Furthermore, datasheets include weight (w or m) and maximum / minimum torques for device connection to the heatsink M_s and for securing terminals M_t. The maximum permissible acceleration a is likewise included in the datasheets.

3.2.4 Rectifier diodes

3.2.4.1 Maximum ratings

Non-repetitive peak reverse voltage V_{RSM}

Maximum instantaneous value of a spike reverse voltage pulse of less than 1 ms (Figure 3.2.5).

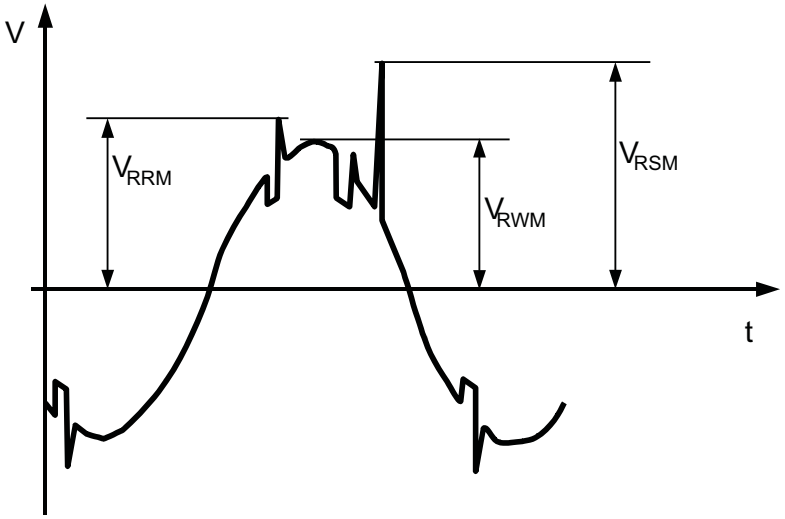


Figure 3.2.5 Example of voltage characteristic with crest working reverse voltage V_{RWM}, repetitive peak reverse voltage V_{RRM} and non-repetitive peak reverse voltage V_{RSM}.

Repetitive peak reverse voltage V_{RRM}

Maximum instantaneous value of repetitive reverse voltage pulses of less than 1 ms (Figure 3.2.5). All reverse voltage maximum ratings are applicable from 25°C to the maximum junction temperature T_j.

Mean forward current I_{FAV}

Maximum permissible forward current, averaged over a full operating cycle. This value depends on the current characteristic, the current conduction angle and the cooling conditions. For this reason, it is often given in the form of a set of curves in relation to the case temperature (or the ambient temperature for low-power diodes) (Figure 3.2.6). The mean forward current is assigned particular importance as an orientation value for one half sine wave of half a load cycle (current conduction angle 180°) at a case temperature of between 80°C and 100°C (45°C ambient temperature for low-power diodes).

The maximum permissible virtual junction temperature is reached under mean forward current load. For this reason, **overload is not permissible** under such operating conditions. Overload to the level of the surge forward current is permissible in the event of malfunction only (which should be a seldom occurrence in a rectifier diode lifetime). Due to possible changes in cooling conditions (e.g. dust deposits), increase in ambient temperature or heat build-up from adjacent components, the recommended current load for operation is 80% of mean forward current maximum. The mean forward current rises proportionate to the decrease in case temperature and breaks off at maximum RMS forward current (150 A in this case), since this must not be exceeded during continuous operation even at low case temperatures T_c. Example: At half sine waves I_{FAV} is calculated as follows:

$$I_{FAV} = \frac{I_{FRMS}}{\pi/2} = \frac{150\ A}{1{,}57} = 95{,}5\ A$$

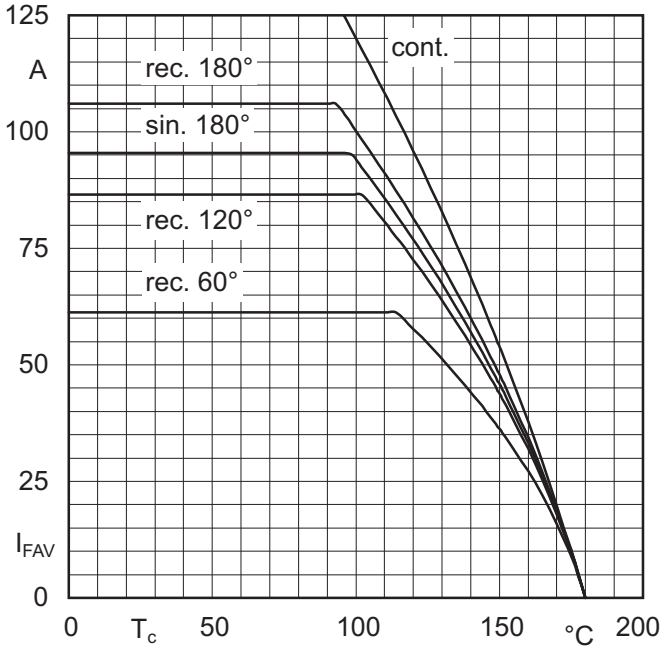


Figure 3.2.6 Mean forward current I_{FAV} of a 70 A rectifier diode as a function of the case temperature T_c. 180, rectangular pulses 180°, 120°, 60°: rec. 180, rec. 120, rec. 60)

RMS forward current I_{FRMS}

Effective forward current, averaged over a full operating cycle. The maximum rated RMS on-state current is applicable to any current characteristic, conduction angle or cooling conditions. It depends on the current carrying capacity of the connections inside the diode case, as well as on the external terminals.

Surge forward current I_{FSM}Surge forward current IFSM

Forward current surge peak in the form of a half sine wave lasting 10 or 8.3 ms (50 or 60 Hz) which the diode is able to withstand without being damaged in the event of a malfunction (short-circuit), provided this does not occur too often during the diode lifetime. The rating for 8.3 ms will be about 10% higher than the rating for 10 ms. The surge on-state current is the maximum current that all devices from a specified set of samples have barely survived without damage during the product qualification process. Additional values may be given for half sine waves under 8.3 ms or for several consecutive half sine waves (Figure 3.2.7, also referred to as limiting overload characteristics).

If a rectifier diode is exposed to surge forward current load, the junction temperature may temporarily rise to as much as 400°C. Should, however, a reverse voltage occur immediately after a diode has been exposed to surge current load (self-healing short-circuit), the maximum surge forward current is lower than if no subsequent reverse voltage is involved.

Values greater than 10 ms apply to half sine waves lasting 10 ms that occur in succession at intervals of 20 ms.

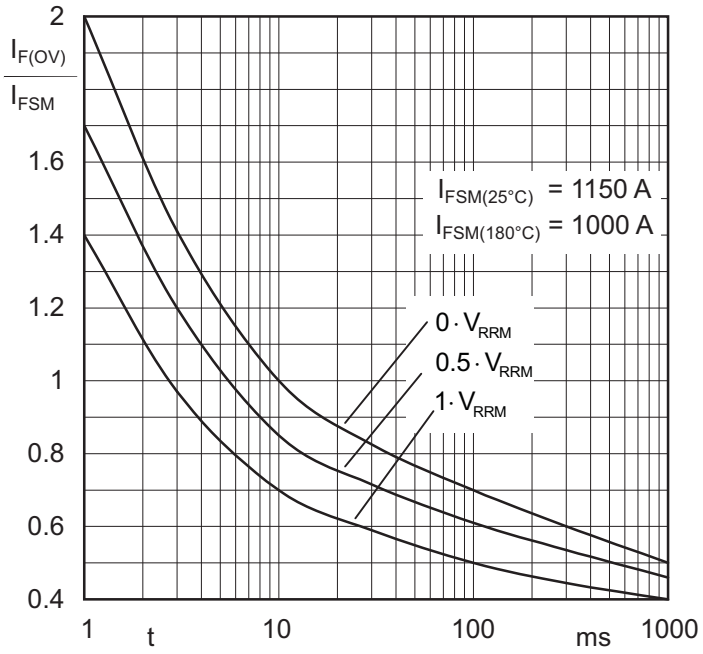


Figure 3.2.7 Overcurrents $I_{F(OV)}$ permissible in the event of malfunction of a 70 A diode in relation to a surge forward current I_{FSM} lasting 10 ms under different reverse voltage conditions directly following the last half sine wave; shown over time t.
- 0 • V_{RRM}: no repetitive peak reverse voltage involved,
- ½ • V_{RRM}: half load of the permissible repetitive peak reverse voltage,
- 1 • V_{RRM}: full load of permissible repetitive peak reverse voltage.

Peak load integral i²t

Reference parameter used to select fuses required for short-circuit protection (also see chapter 4.4). The peak load integral is calculated from the surge forward current I_{FSM} as follows:

$$\int_0^{t_{hw}} i_{FS}^2 \, dt = I_{FSM}^2 \cdot \frac{t_{hw}}{2}$$

t_{hw} stands for the duration of the half sine wave under I_{FSM}. Consequently, $t_{hw}/2 = 0.005$ s at 50 Hz. At frequencies of 50 or 60 Hz, i²t is almost identical, since I_{FSM}, which is 10% higher at 60 Hz, is offset by the shorter t_{hw}: $1.1^2 \cdot 8.3 \approx 10$.

Non-repetitive peak reverse power dissipation P_{RSM} (for avalanche rectifier diodes)

Maximum instantaneous value for power dissipation caused by a non-repetitive reverse current pulse. This value is given as a function of the pulse duration at a virtual junction temperature which corresponds to 80% of the mean forward current permissible at specified cooling and operating conditions (Figure 3.2.8).

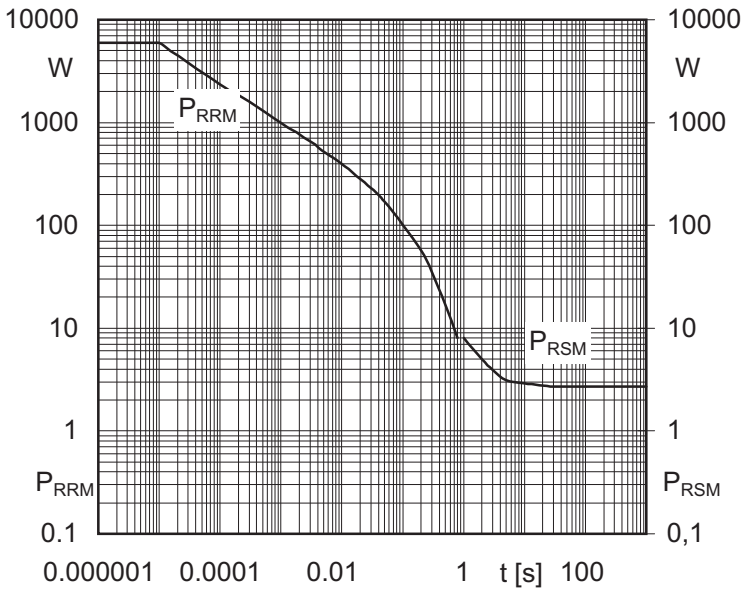


Figure 3.2.8 Non-repetitive peak reverse power dissipation P_{RSM} (t < 1 s, forward current load 0.8 •I_{FAV}) and peak repetitive reverse power dissipation P_{RRM} (t > 1 s, no forward current load) of a 20 A avalanche rectifier diode as a function of time t.

3.2.4.2 Characteristics

(Direct) forward voltage V_F

Voltage at the terminals induced by a forward current I_F. The maximum forward voltage V_F is used for comparative and control measurements and is given for a specified forward current I_F and a virtual junction temperature of 25°C. A forward characteristic is also normally specified, i.e. forward current (instantaneous values) i_F over forward voltage (instantaneous values) v_F at 25°C, as well as at maximum virtual junction temperature (Figure 3.2.9).

Threshold voltage V_{T0},V_{F0}

Voltage at the point of crossover between an approximation line of the forward characteristic and the voltage axis (Figure 3.2.9).

Forward slope resistance r_f

Resistance calculated from the inclination of the straight lines approximating the forward characteristic. To calculate the forward power dissipation, the forward characteristic is replaced by a straight line, which satisfies the equation $v_F = V_{(T0)} + r_f \bullet i_F$ (Figure 3.2.9). As a rule, $V(_{T0)}$ and r_f are given for a forward slope resistance characteristic corresponding to the forward characteristic at maximum operating temperatures for a diode with maximum forward voltage V_F at 25°C, as applicable to the routine test. In a hot state, the forward slope resistance characteristic intersects the forward characteristic at 1 x I_{FAV} and 3 x I_{FAV} (blue dots in Figure 3.2.9).

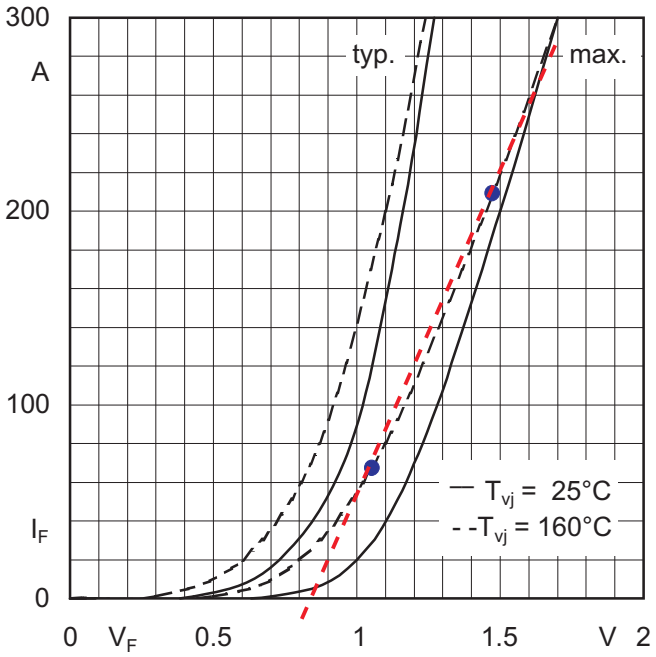


Figure 3.2.9 Forward characteristics (typical and maximum values) of a rectifier diode at two different virtual junction temperatures T_j; dotted red line = forward slope resistance used to determine $V_{(T0)}$ and r_f; r_f results from the line inclination

Forward power dissipation P_F

Power dissipation due to the on-state current. Usually, the mean forward power dissipation P_{FAV} is averaged over a full operating cycle and given as a function of the mean forward current I_{FAV} displayed in the form of a set of curves for half sine waves and rectangular currents with different conduction angles (Figure 3.2.10). The forward power dissipation instantaneous value P_F and the mean value P_{FAV} are determined from the threshold voltage $V_{(T0)}$ and the forward slope resistance r_f as follows:

$$P_F = V_{(T0)} \cdot i_f + r_f \cdot i_F^2$$

$$P_{FAV} = V_{(T0)} \cdot I_{FAV} + r_f \cdot I_{FRMS}^2$$

$$\frac{I_{FRMS}^2}{I_{FAV}^2} = \frac{360°}{\Theta} \quad \text{for rectangular pulses}$$

$$\frac{I_{FRMS}^2}{I_{FAV}^2} = \frac{\pi^2}{4} \quad \text{for half sine waves}$$

where Θ is the current conduction angle; i_f, I_{FAV} and I_{FRMS} designate the instantaneous, mean and RMS values of the forward current whose power losses are to be determined.

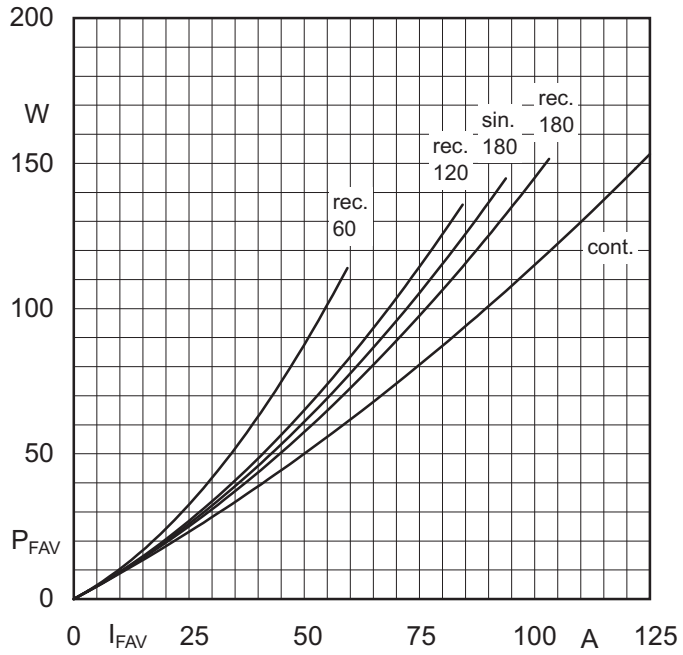


Figure 3.2.10 Mean forward power dissipation P_{FAV} over mean forward current I_{FAV} of a 70 A diode for pure direct current (cont.), half sine waves 180° (sin. 180) and rectangular current pulses 60° (rec. 60) to 180° (rec. 180)

Recovered charge Q_{rr}

Total charge which flows from the diode to the outer circuit after having switched over from a defined forward current load to a defined reverse current load. The recovered charge depends on the rate of fall of the decaying current $-di_F/dt$, the mean forward current I_{FM} effective at the point of switching and the virtual junction temperature (Figure 3.2.11).

Peak reverse recovery current I_{RRM}

Reverse current peak after passing over from forward to reverse current load (applies to circuits with unimpeded current decay) (Figure 3.2.11). The maximum possible peak reverse recovery current can be calculated from the recovered charge Q_{rr} and the current fall rate $-di_F/dt$ using the following equation ($Q_f \rightarrow 0$):

$$I_{RRM} \leq \sqrt{2 \cdot Q_{rr} \cdot \left(-\frac{di_F}{dt} \right)}$$

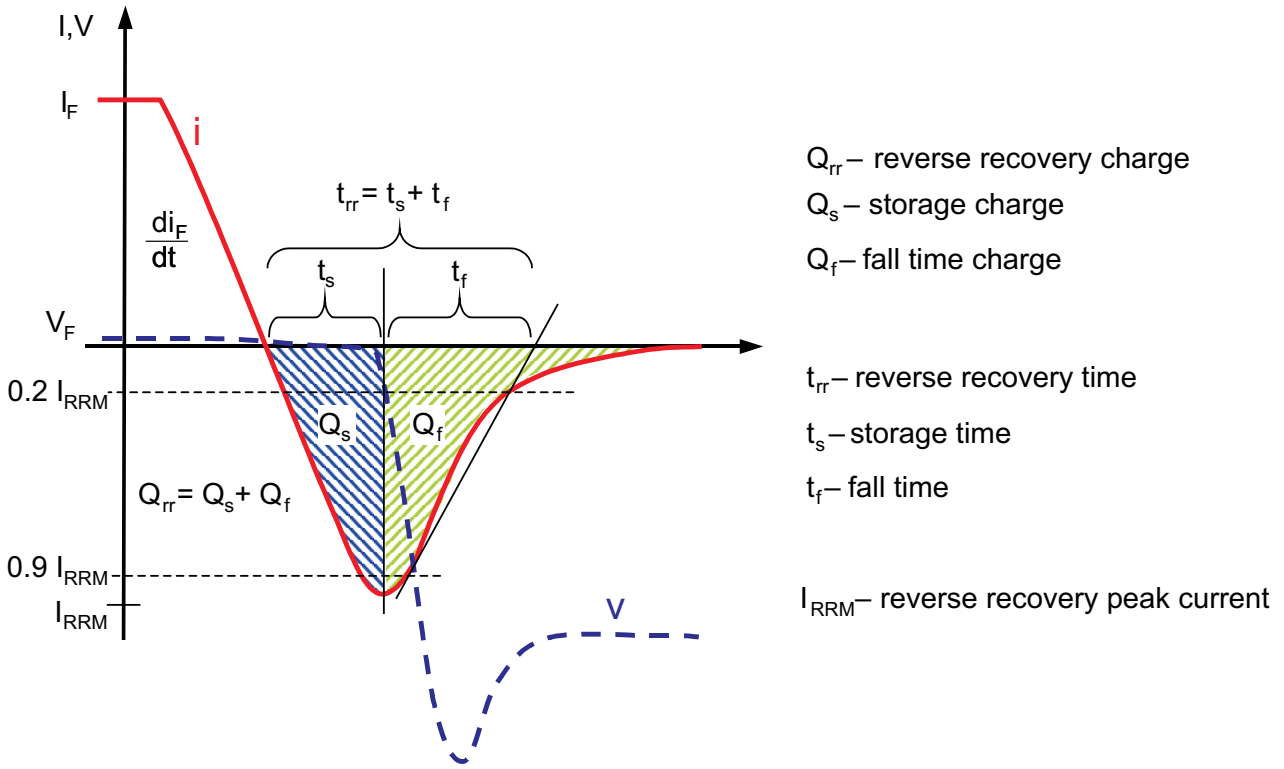


Figure 3.2.11 Current and voltage characteristics of a rectifier diode passing over from conductive to blocking state.

Reverse recovery time t_{rr}

The time it takes for the reverse current to reach its stationary value after sudden switchover from conductive to blocking state (

). t_{rr} is calculated from Q_{rr} and I_{RRM} according to the following equation:

$$t_{rr} \approx \frac{2 \cdot Q_{rr}}{I_{RRM}}$$

Fall time t_f

Time interval where the reverse current drops from peak reverse recovery level I_{RRM} to its stationary value.

$$t_f \approx \frac{2 \cdot Q_{rr}}{I_{RRM}} - \frac{I_{RRM}}{\left(-\frac{di_F}{dt}\right)}$$

Storage time t_s

Time interval from zero crossing to peak reverse recovery current.

$$t_S \approx \frac{I_{RRM}}{\frac{di_F}{dt}}$$

Forward recovery time t_{fr}

The time it takes for the reverse voltage to reach its stationary value after sudden turn-on of a specified forward current.

Breakdown voltage $V_{(BR)}$ for avalanche rectifier diodes

Reverse voltage at which the avalanche breakdown occurs, causing a sudden rise in the reverse current (Figure 2.2.2). This value is given as a minimum value for 25°C. The breakdown voltage increases in proportion to the temperature.

Reverse current I_R

The maximum reverse current at 25°C and at a voltage corresponding to the maximum permissible repetitive peak reverse voltage V_{RRM} is given.

3.2.4.3 Diagrams

This chapter provides important information on the diagrams contained in the datasheets. If a diagram is explained in more detail elsewhere, reference to this will be given.

Mean forward power dissipation P_{FAV} and case temperature T_c

Figure 3.2.12 shows the mean forward power dissipation P_{FAV} inside the device generated in dependence of the mean forward current I_{FAV} for the different current waveforms (also see chapter 3.2.4.2 Characteristics). For the mean forward power dissipation P_{FAV} (Y-axis on the left), the case temperature T_c is permissible (Y-axis on the right). The recommended mean forward current is 0.8 · I_{FAV}.

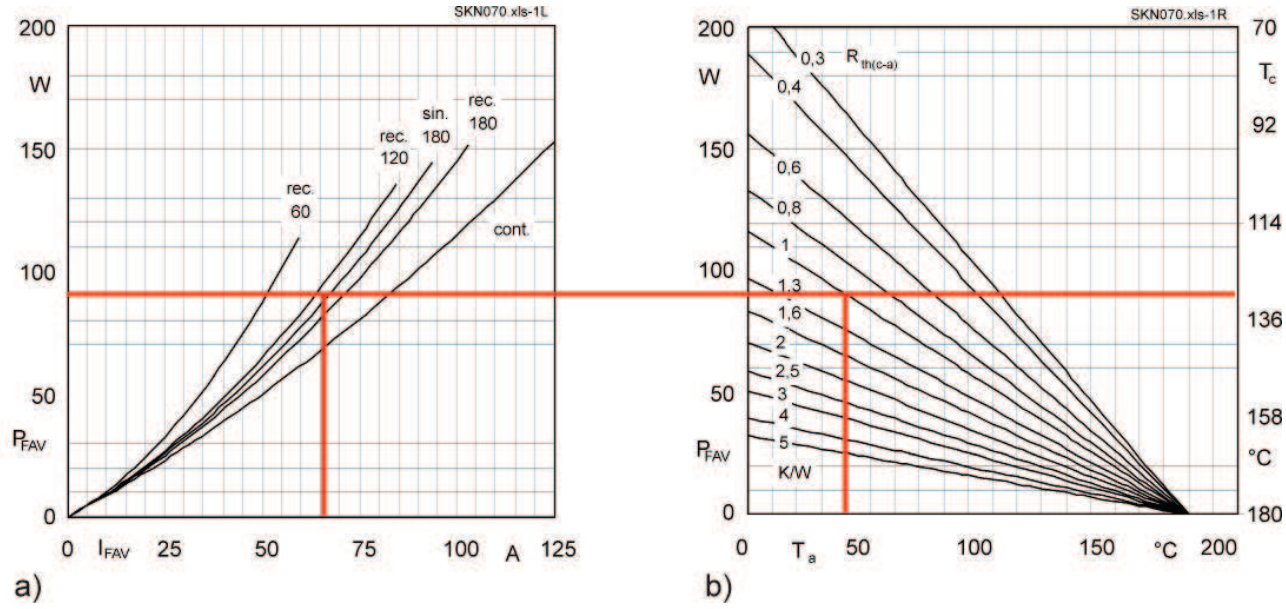


Figure 3.2.12 a) Mean forward power dissipation P_{FAV} over mean forward current I_{FAV} for different current waveforms; b) Case temperature T_c over ambient temperature T_a; the parameter is the thermal resistance case-to-air $R_{th(c-a)}$ of a 70 A diode

The example marked in red in Figure 3.2.12 can be red as follows: the case temperature must not exceed 130.5°C for an ambient temperature T_a = 40°C and a thermal resistance case-to-air $R_{th(c-a)}$ = 1 K/W. For an internal mean forward power dissipation P_{FAV} = 90 W, the diode pn-junction is heated to the maximum permissible temperature of 180°C. Power dissipation is caused by an average sinusoidal half-wave current of 67 A.

Mean forward current I_{FAV} over case temperature T_c

See Figure 3.2.6 in chapter 3.2.4.1 Characteristics. This chapter also refers to the maximum RMS forward current I_{FRMS}, which must not be exceeded, irrespective of the current waveform, conduction angle or cooling conditions.

Forward characteristics

See Figure 3.2.9 in chapter 3.2.4.2. The typical and maximum values at ambient (25°C) and high temperature are shown.

Limiting overload characteristics

See Figure 3.2.7: The diagram shows the maximum overload forward current $I_{F(OV)}$ (peak value) divided by the surge forward current for 10 ms I_{FSM} as a function of the load duration t at 50 Hz sinusoidal half-wave current. Parameter: peak value of the reverse voltage effective between the sinusoidal half-waves.

3.2.5 Thyristors

3.2.5.1 Maximum ratings

Non-repetitive peak reverse voltage V_{RSM}

Maximum instantaneous value of a spike reverse voltage pulse of less than 1 ms (Figure 3.2.5).

Repetitive peak off-state voltage V_{DRM}
Repetitive peak reverse voltage V_{RRM}

Maximum instantaneous value of repetitive reverse voltage pulses of less than 1 ms (Figure 3.2.5).

Mean on-state current I_{TAV}

Maximum permissible forward current, averaged over a full operating cycle. This value depends on the current characteristic, the current conduction angle and the cooling conditions. It is therefore often given in the form of a set of curves in dependence of the case temperature (Figure 3.2.13). The mean forward current is assigned particular importance as an orientation value for one half sine wave of half a load cycle (current conduction angle 180°) at a case temperature of approx. 85°C.

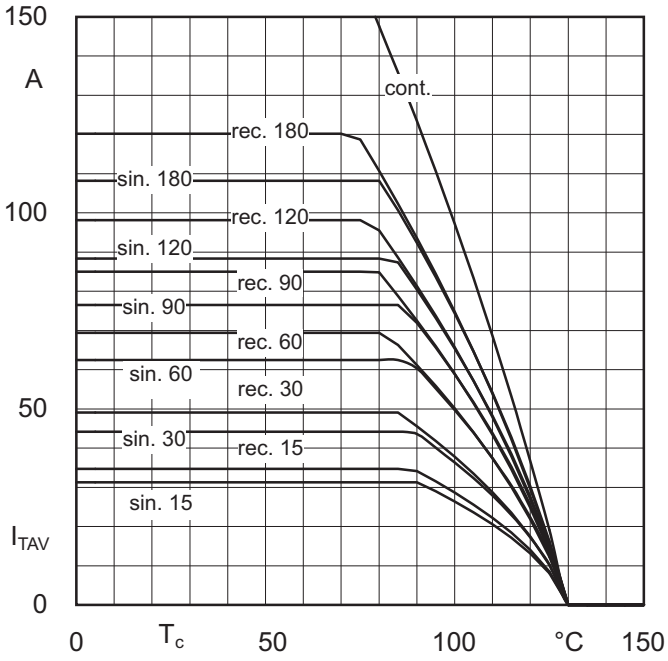


Figure 3.2.13 Mean on-state currents I_{TAV} of a 100 A thyristor over case temperature T_c for direct current (cont.), rectangular pulses (rec.) and (controlled) half sine waves (sin.) with different current conduction angles Θ

The maximum permissible virtual junction temperature is reached under mean forward current load. For this reason, **overload is not permissible** under such operating conditions. Overload to the level of the surge forward current is permissible in the event of malfunction only (which should be a seldom occurrence in the lifetime of a thyristor). Due to possible changes in cooling conditions (e.g. dust deposits), increase in ambient temperature or heat build-up from adjacent components, the recommended current load for operation is 80% of mean forward current maximum. The mean on-state current rises in proportion to the decrease in case temperature and breaks off at maximum RMS forward current (here: 150 A), since this may not be exceeded during continuous operation.

RMS on-state current I_{TRMS}

Effective forward current, averaged over a full operating cycle. The maximum rated RMS on-state current is applicable to any current characteristic, conduction angle or cooling conditions. This value depends on the current carrying capacity of the connections inside the thyristor case and the external terminals.

Surge forward current I_{TSM}

On-state current surge peak in the form of a half sine wave of 10 or 8.3 ms (50 or 60 Hz), which the thyristor is able to withstand without being damaged in the event of malfunction (short-circuit), provided this does not occur too often in the thyristor service life. For a surge duration of 8.3 ms, this value will be about 10% higher than for a surge duration of 10 ms. The surge on-state current is the maximum current that all devices from a specified set of samples have barely survived without damage during the product qualification process.

Additional values may be given for half sine waves under 8.3 ms or for several consecutive half sine waves (also referred to as limiting overload characteristics). Values greater than 10 ms apply to half sine waves lasting 10 ms that occur in succession at intervals of 20 ms. If a thyristor is subjected to surge on-state current load, the junction temperature may temporarily increase to as much as 400°C. For this reason, the forward blocking capability is temporarily impeded. Should a reverse voltage occur immediately after a thyristor has been subjected to surge on-state current (self-healing short-circuit), the permissible surge on-state current peak value will be lower than if a subsequent reverse voltage is not involved (Figure 3.2.14):

- $0 \cdot V_{RRM}$: no reverse voltage
- $½ \cdot V_{RRM}$: half of the permissible repetitive peak reverse voltage
- $1 \cdot V_{RRM}$: full load of permissible repetitive peak reverse voltage.

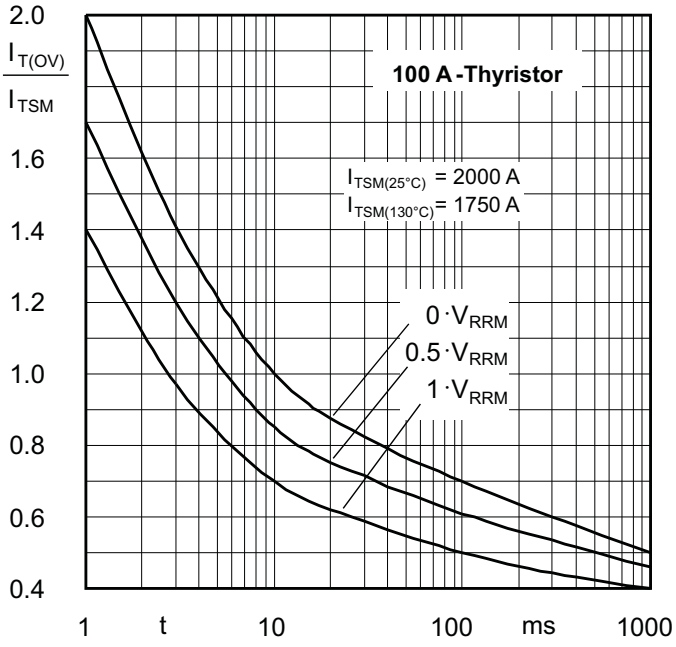


Figure 3.2.14 Permissible overload on-state currents $I_{T(OV)}$ in relation to surge on-state current I_{TSM} for a duration of 10 ms for different reverse voltage conditions directly following the last sinusoidal half-wave as a function of time t.

Peak load integral i^2t

Reference parameter used to select fuses required for short-circuit protection (also see chapter 4.4). The peak load integral is calculated from the surge forward current I_{TSM} as follows:

$$\int_0^{t_{hw}} i_{TS}^2 \, dt = I_{TSM}^2 \cdot \frac{t_{hw}}{2}$$

Here, t_{hw} stands for the duration of the half sine wave under I_{TSM} gilt. Consequently, $t_{hw}/2 = 0.005$ s at 50 Hz. At frequencies of 50 Hz or 60 Hz, i²t is almost identical, since I_{TSM}, which is 10% higher at 60 Hz, is offset by the shorter t_{hw}: $1.1^2 \cdot 8.3 \approx 10$.

Critical rate of rise of on-state current $(di/dt)_{cr}$

Maximum rate of rise of on-state current which the thyristor is able to withstand without being damaged. This depends on the operating frequency, the peak on-state current, the off-state voltage directly before thyristor firing, as well as on the size and rate of rise of the gate pulses. What must also be taken into account is the fact that the thyristor is loaded with a high discharge current at turn-on induced by an RC-snubber connected in parallel to the thyristor for overvoltage protection.

The values given apply to frequencies of 50 to 60 Hz, a current amplitude which is three times the mean on-state current (for half sine waves at a case temperature of 85°C) and gate pulses of five times the gate trigger current with a rising edge of at least 1 A/µs without RC snubber. The critical di/dt rises at lower current amplitude and temperature and falls at low or slow-rising gate trigger current and higher repetition frequency. Amplifying gate thyristors can reach very high $(di/dt)_{cr}$ values (also see chapter 2.2.2.4).

Peak gate power dissipation P_{GM}

Maximum permissible power dissipation caused by the thyristor gate current. It depends on the gate pulse duration (Figure 3.2.21).

Average gate power dissipation P_{GAV}

Maximum permissible power dissipation caused by the thyristor gate current, averaged over a full operating cycle.

For temperature limits see chapter 3.2.1 "Temperatures".

3.2.5.2 Characteristics

On-state voltage V_T

Voltage at the main terminals induced by a forward on-state current I_T. The maximum forward voltage V_T is used for comparative and control measurements and is given for a specified forward current I_T and a virtual junction temperature of 25°C. The maximum on-state voltage v_T is used for comparative and control measurements and is given for a specified on-state current i_T at 25°C as well as at the maximum virtual junction temperature (Figure 3.2.15).

Threshold voltage $V_{T(T0)}$

Voltage at the point of crossover between an approximation line of the forward characteristic and the voltage axis (Figure 3.2.15).

On-state slope resistance r_TOn-state slope resistance rT

Resistance calculated from the inclination of the straight lines approximating the forward characteristic (Figure 3.2.15). To calculate the on-state power dissipation, the on-state characteristic is replaced by a straight-line which is determined from $v_T = V_{T(T0)} + r_T \cdot i_T$. As a rule, $V_{T(T0)}$ and r_T are given for an on-state slope resistance characteristic which corresponds to the on-state characteristic at the maximum virtual junction temperature for a thyristor whose on-state voltage V_T has its maximum value as applicable to the routine test at at 25°C. In a hot state, the forward slope resistance characteristic intersects the forward characteristic at 1 x I_{FAV} and 3 x I_{FAV} (blue dots in Figure 3.2.15).

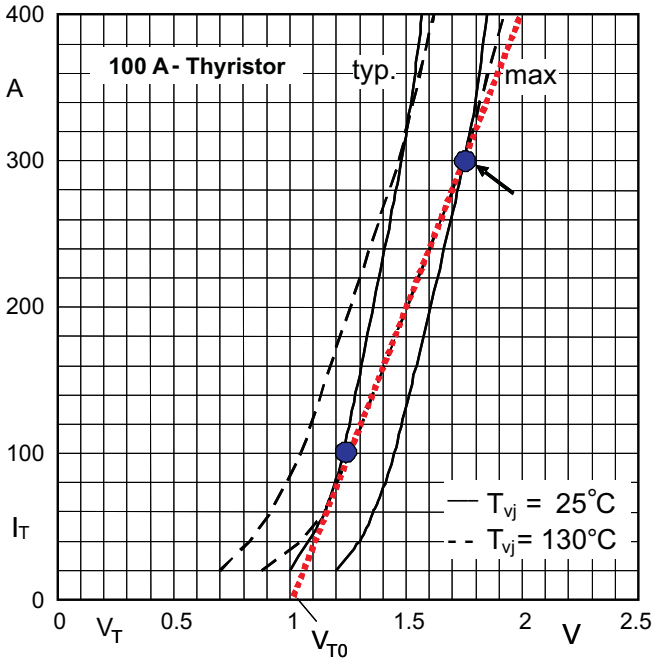


Figure 3.2.15 Thyristor on-state characteristics (typical and maximum) at two different virtual junction temperatures T_{vj}; the arrow shows the test limit; dotted red line = on-state slope resistance used to determine $V_{(T0)}$ and r_T; r_T results from the straight line inclination

On-state power dissipation P_T

Power dissipation due to the on-state current. Usually, the mean on-state power dissipation P_{TAV} is averaged over a full operating cycle and given as a function of the mean on-state current I_{TAV} displayed in the form of a set of curves for (controlled) half sine waves and rectangular currents with different conduction angles (Figure 3.2.16).

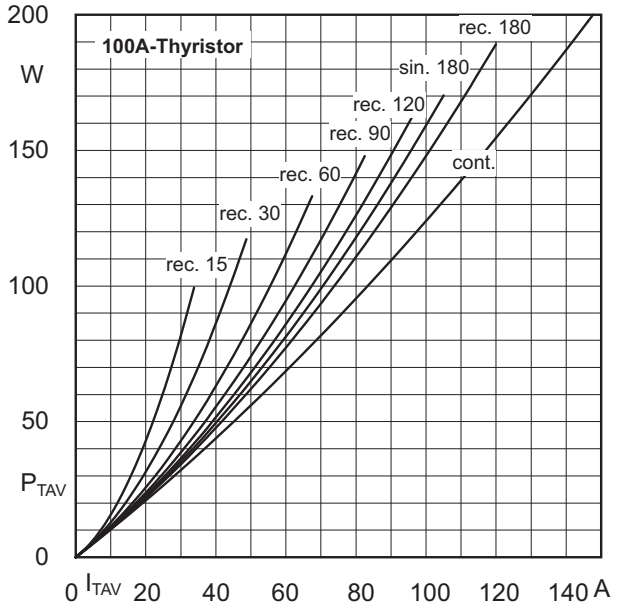


Figure 3.2.16 Mean on-state power dissipation P_{TAV} as a function of the mean on-state current I_{TAV} for pure direct current (cont.), 180° half sine waves (sin.180) and rectangular current pulses from 15° to 180° (rec. 15 to 180).

The on-state power dissipation instantaneous value P_T and the mean value P_{TAV} are determined from the threshold voltage $V_{T(T0)}$ and the on-state slope resistance r_T as follows:

$$P_T = V_{T(T0)} \cdot i_T + r_T \cdot i_T^2$$

$$P_{TAV} = V_{T(T0)} \cdot I_{TAV} + r_T \cdot I^2_{TRMS}$$

$$\frac{I^2_{TRMS}}{I^2_{TAV}} = \frac{360°}{\Theta}$$ for rectangular pulses

$$\frac{I^2_{TRMS}}{I^2_{TAV}} \approx 2.5 \cdot \frac{180°}{\Theta}$$ for controlled phases.

Here, Θ the current conduction angle, I_T, I_{TAV} and I_{TRMS} designate the instantaneous, mean and effective values of the forward current whose power losses are to be determined.

Exact values for controlled phases are:

Θ	180°	120°	90°	60°	30°	15°
$\frac{I^2_{TRMS}}{I^2_{TAV}}$	2.47	3.5	4.93	7.7	15.9	31.8

Direct reverse current I_{RD}, blocking current I_{DD}

The maximum reverse current at 125°C and at a voltage corresponding to the maximum permissible repetitive peak reverse voltage V_{RRM} is given. The direct reverse current is extremely temperature-dependent. For every 10 K increase in temperature, this value increases by a factor of 2 - 2.5.

$$I_{DD}(T_j) = I_{DD\_25°C} \cdot \left(\frac{T_j - 25°C}{10°C} \right)^{2...2,5}$$

The direct reverse current rises almost linear to the chip area.

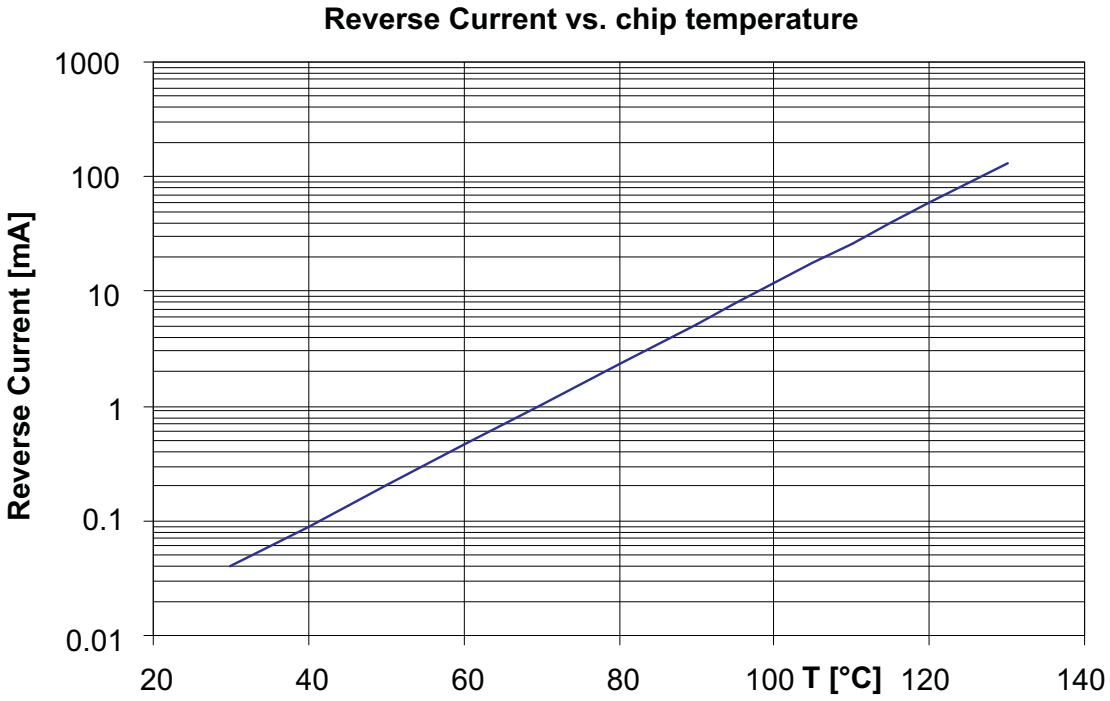


Figure 3.2.17 Thyristor direct reverse current as a function of T_j

Holding current I_H

The minimum on-state current required to maintain the thyristor in on-state. This is given as a 98% value of the typical current distribution under the following conditions:

- 6 V driving voltage in the main circuit
- resistive load
- 25°C virtual junction temperature (at higher temperatures I_H decreases).

Latching current I_L

The minimum on-state current required to maintain the thyristor in the on-state at the end of the gate trigger pulse. If the thyristor is not triggered to latching current level at the end of the gate pulse, it will turn off again. The latching current is given as a 98% value of the typical current distribution under the following conditions:
- 6 V driving voltage in the main circuit,
- resistive main circuit,
- rectangular gate pulse 10 µs in duration and five times the peak gate trigger current; if the gate trigger current falls below this value, I_L will increase.
- gate circuit resistance R_G = 33 Ω, 25°C virtual junction temperature; at higher temperatures I_L is smaller.

Gate-controlled turn-on time t_{gt}

Time interval during which the thyristor switches from its blocking state to forward on-state as a result of a gate trigger pulse. The gate-controlled turn-on time is measured from the moment when the gate pulse is triggered until the moment when the on-state voltage has dropped to 6 V (Figure 3.2.18).

Gate-controlled delay time t_{gd}

Time interval between the moment when the gate pulse is triggered and the moment when the forward voltage (instantaneous value) v_F has dropped to 90% of its initial value V_D (Figure 3.2.18). The maximum values and the typical variation range are given in a characteristic (Figure 3.2.19) as a function of the gate current pulse under the following conditions:
- rectangular gate current pulse lasting 10 µs,
- the initial value for the direct off-state voltage V_D equals half the repetitive peak off-state voltage V_{DRM},
- after firing the main circuit will be loaded with approximately 10% of the mean on-state current permissible at a case temperature of 85°C,
- virtual junction temperature = 25°C.

Gate-controlled rise time t_{gr}

Difference between gate-controlled turn-on time and gate-controlled delay time: $t_{gt} = t_{gd} + t_{gr}$.

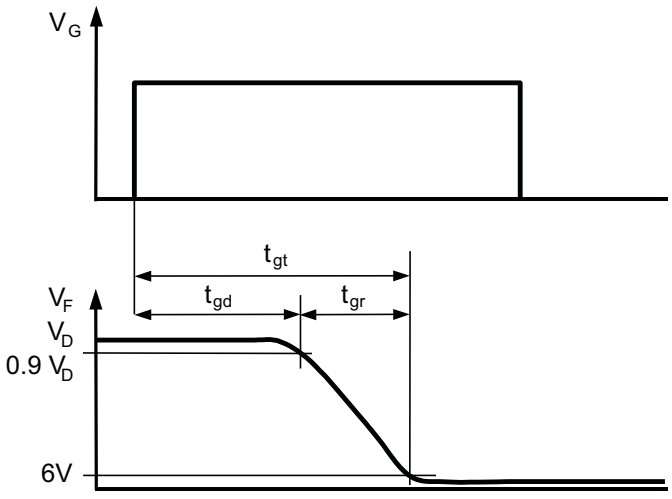


Figure 3.2.18 Gate voltage v_G and forward voltage (instantaneous values) v_F at the moment of thyristor triggering.

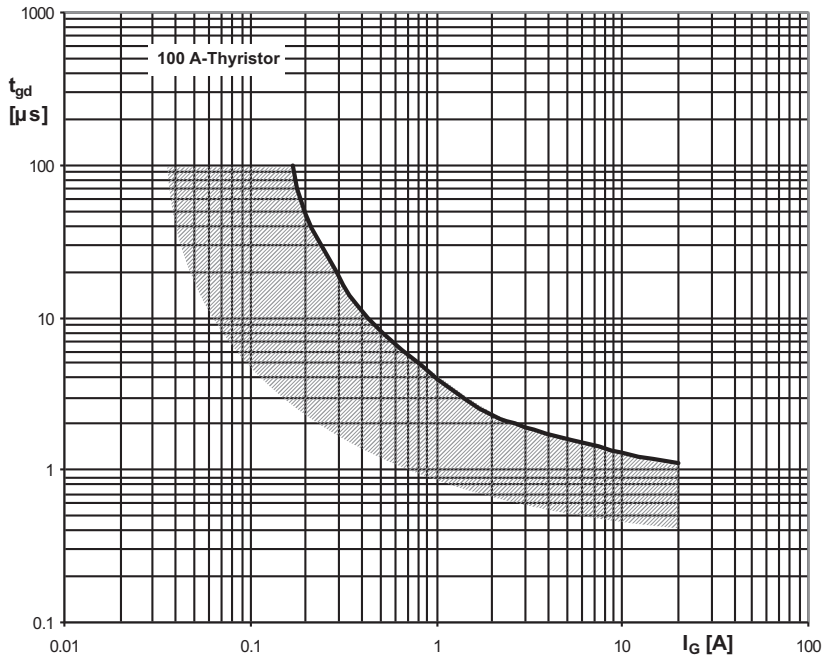


Figure 3.2.19 Typical dependency of a thyristor gate-controlled delay time t_{gd} on gate current I_G; the shaded area represents the variation range.

Recovered charge Q_{rr}
Peak reverse recovery current I_{RRM}
Reverse recovery time t_{rr}
Fall time t_f

See chapter 3.2.4.2 Rectifier diode characteristics and Figure 3.2.11.

Repetitive peak off-state current I_{DRM}

Maximum rated value at the maximum permissible repetitive peak off-state voltage at 25°C.

Gate trigger voltage V_{GT} and gate trigger current I_{GT}

Minimum gate current and gate voltage required to ensure that each thyristor of the given type is triggered (Figure 3.2.21). These parameters are subject to the following conditions:
- ≥6 V driving voltage in the main circuit,
- resistive main circuit,
- rectangular gate current pulse of at least 100 µs,
- virtual junction temperature = 25°C.

Gate pulses under 100 µs will effect an increase in the minimum gate trigger current and voltage values by a factor of 1.4 to 2. The driver unit should ensure that the trigger current value given in the datasheet is exceeded by a factor of four or even five.

As for amplifying gate thyristors, a high rate of rise in the main current will provoke a temporary counter voltage at the gate terminal as a consequence of the voltage spread across the thyristor chip layers. In the case of insufficient driving voltage or too high a driver output resistance, the temporary counter voltage may suppress or even temporarily reverse the gate current (Figure 3.2.20). This may damage the thyristor. The driver dimensioning must therefore comply with the power requirements.

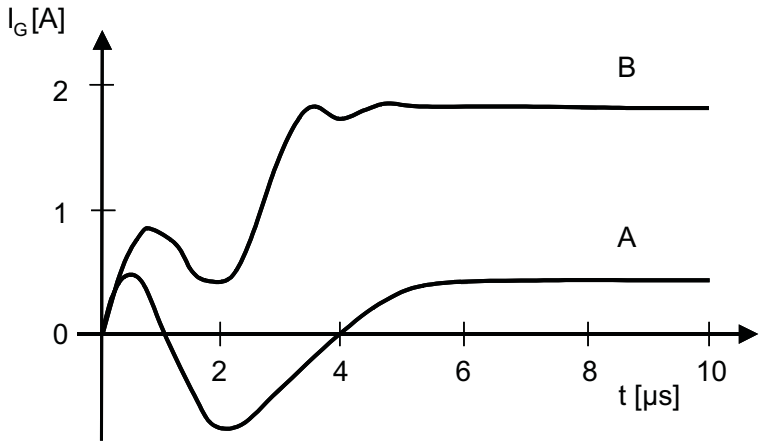


Figure 3.2.20 Gate current I_G over time, triggered by an insufficiently (curve A) and a sufficiently designed (curve B) driver unit.

Highest gate non-trigger current I_{GD}, highest gate non-trigger voltage V_{GD}

Gate current and gate voltage at which none of the thyristors of a specific type are triggered (Figure 3.2.21). These parameters are subject to the following conditions:
- ≤ 6 V driving voltage in the main circuit,
- rectangular gate current pulse of at least 100 µs,
- maximum virtual junction temperature.

For direct off-state voltages of around 100 V and more, the gate non-trigger current decreases as shown in Figure 3.2.22.

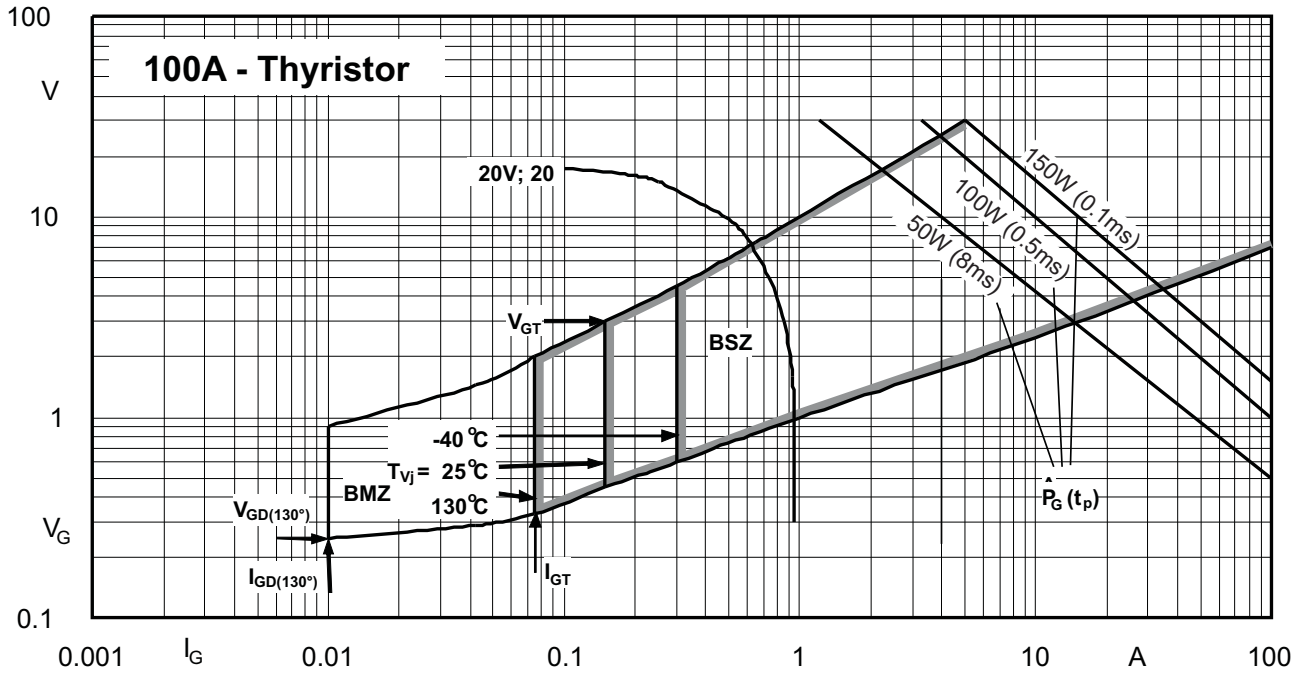


Figure 3.2.21 Trigger current (I_G) over trigger voltage (V_G)of a 100 A thyristor (spread) with areas of possible and safe triggering. $\hat{P}_G(t_p)$ is the maximum permissible peak gate power dissipation at a gate current pulse duration t_p; the curve labelled "20 V; 20 Ω" is the characteristic of a trigger device for 20 V no-load voltage and 20 Ω internal resistance.

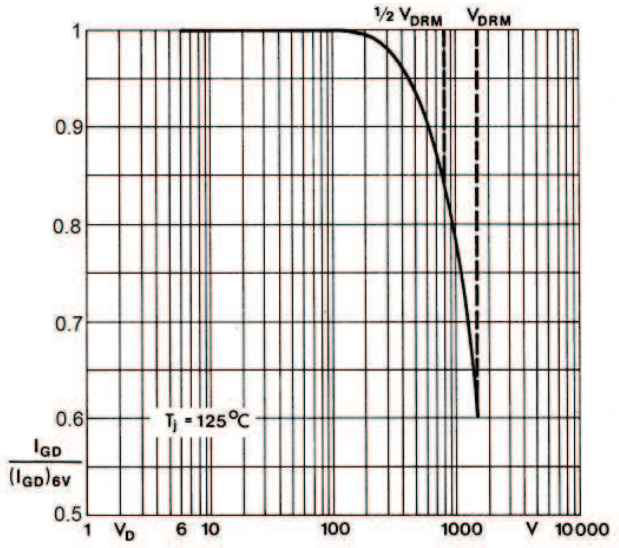


Figure 3.2.22 Gate non-trigger current I_{GD} at V_D = 6 V as a function of off-state voltage V_D; typical characteristic for a thyristor with a max. repetitive peak off-state voltage V_{DRM} = 1600 V

Critical rate of rise of on-state voltage $(dv/dt)_{cr}$

Maximum rate of rise of the on-state voltage at which the thyristor is not triggered. This is normally given under the following conditions:
- exponential rise to a voltage V_0 which equals ⅔ of the repetitive peak off-state voltage V_{DRM}
- open gate circuit
- maximum virtual junction temperature T_j

If the temperature T_j decreases, the critical rate of rise of off-state voltage will increase.

Circuit-commutated turn-off time t_q

In a commutation process within the main circuit, this is the time interval between the moment when the decreasing on-state current passes through zero and the earliest reapplication of off-state voltage, after which the thyristor does not turn on again (Figure 3.2.23). For phase control thyristors, typical values are normally given, whereas for fast thyristors the circuit commutated turn-off time is always given as a maximum value.

The circuit commutated turn-off time t_q depends on the following operating conditions:
- tt_q increases in proportion to the peak on-state current I_{TM} before commutation
- t_q decreases in proportion to the rising rate of fall of the on-state current $-\frac{di_T}{dt}$
- t_q increases in proportion to the virtual junction temperature T_{vj} (Figure 3.2.24),
- t_q decreases in proportion to the falling rate of rise of the off-state voltage $\frac{dv_D}{dt}$ (Figure 3.2.25)
- t_q increases in proportion to the decreasing peak reverse voltage V_{RM} (Figure 3.2.26).

In circuits with an inverse diode connected directly in parallel to the thyristor, the reverse voltage amounts to a few volts only and the circuit commutated turn-off time increases by a factor of approx. 1.8 in accordance with Figure 3.2.26. This factor is, however, subject to a considerable manufacturing tolerance.

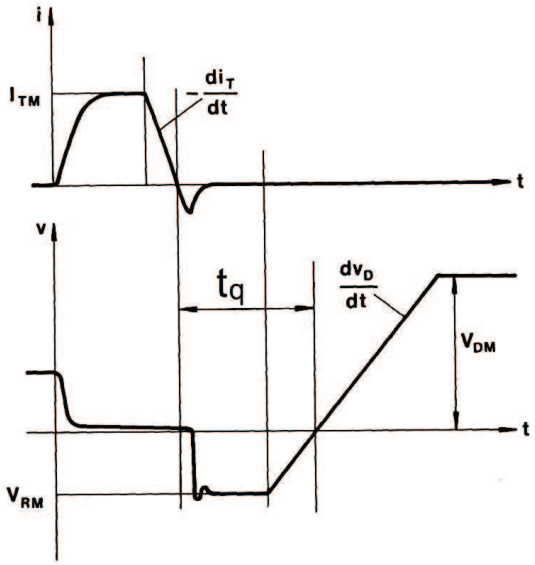


Figure 3.2.23 Main current i and main voltage v of a thyristor over time during commutation from on-state to off-state; the circuit commutated turn-off time t_q is the shorted time interval during which an applied direct off-state voltage will not trigger the thyristor

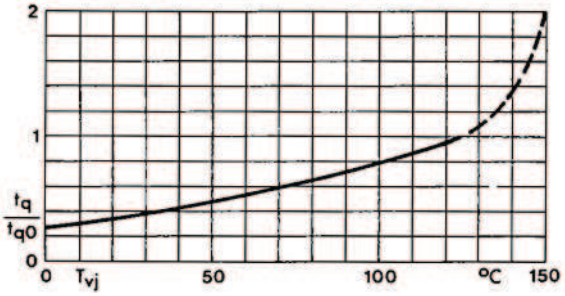


Figure 3.2.24 Typical characteristic of circuit commutated turn-off time t_q (where t_{q0} at T_j = 125°C) over virtual junction temperature T_j.

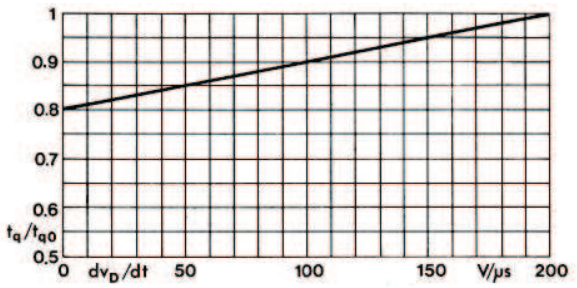


Figure 3.2.25 Typical characteristic of circuit commutated turn-off time t_q (where dv_D/dt = 200 V/µs) over rate of rise of the repetitive on-state voltage dv_D/dt.

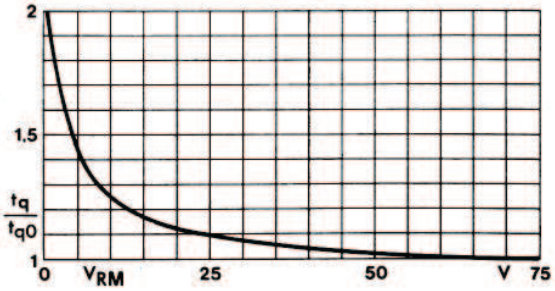


Figure 3.2.26 Typical characteristic of circuit commutated turn-off time t_q (where t_{q0} at $V_{RM} \geq 75$ V) over peak reverse voltage V_{RM}.

3.2.5.3 Diagrams

This chapter provides important information on the diagrams contained in the datasheets. If a diagram is explained in more detail elsewhere, reference to this will be given.

Mean on-state power dissipation P_{TAV}, ambient temperature T_a and mean on-state current I_{TAV}

Figure 3.2.27 shows the mean on-state power dissipation P_{TAV} generated inside the device in dependence of the mean on-state current I_{TAV} for the different current waveforms.

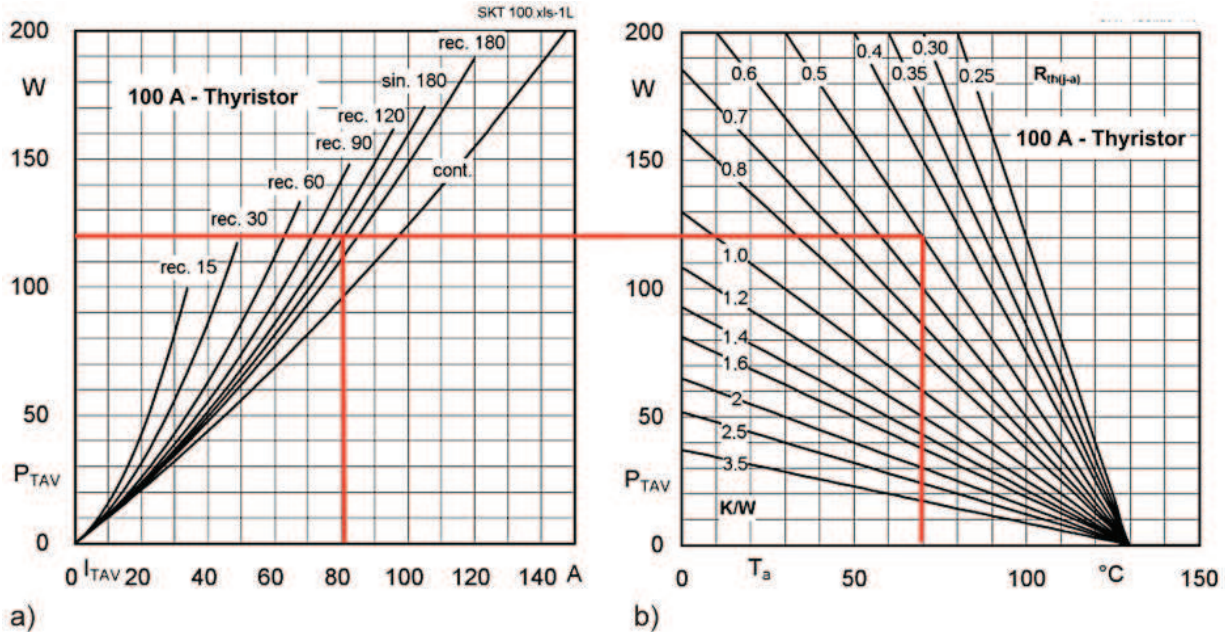


Figure 3.2.27 a) Mean on-state power dissipation P_{TAV} over mean on-state current I_{TAV} for different current waveforms; b) Permissible ambient temperature T_a over thermal resistance junction-to-ambient $R_{th(j-a)}$ including the contact thermal resistance case-to-heatsink

The example marked in red in Figure 3.2.27 can be read as follows: For an ambient temperature T_a = 70°C and a thermal resistance of junction to ambient $R_{th(j-a)}$ = 0.5 K/W, the power losses must not exceed 120 W. Under these circumstances, the thyristor pn-junction is heated to the maximum permissible temperature of 130°C. A sinusoidal half-wave current with a mean on-state value I_{TAV} = 80 A produces these power losses (see chapter 3.2.5.2 Characteristics). It is recommended that a mean on-state current of 0.8 · I_{TAV} is not exceeded at all or very briefly only.

Mean on-state current I_{TAV} over case temperature T_c

See Figure 3.2.13 in chapter 3.2.5.2 Characteristics. This chapter also refers to the maximum RMS forward current I_{FRMS}, which must not be exceeded, irrespective of the current waveform, conduction angle or cooling conditions.

Reverse recovery charge

The reverse recovery charge Q_{rr} over rate of current fall during turn-off commutation -di/dt is shown in Figure 3.2.28 for different on-state currents I_{TM}. The data is used, for example, to design the sweep-out circuit.

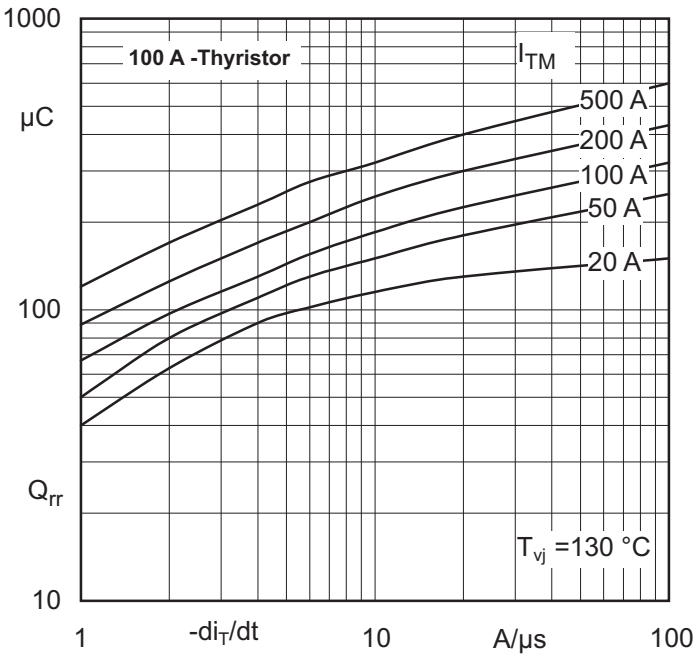


Figure 3.2.28 Reverse recovery charge Q_{rr} over rate of current fall during switch-off commutation -di/dt for different on-state currents I_{TM}.

3.2.6 Diode and thyristor modules

3.2.6.1 Maximum ratings and characteristics

Most values given in the datasheets refer to discrete diodes and thyristors. For modules integrating both thyristor and diode, usually values such as direct on-state voltage and permissible currents are given for thyristors only, since the ratings of the diode are usually better. The following parameters are also given in the datasheets:

Insulation test voltage V_{iso}

V_{iso} is the RMS value of a 50 Hz AC voltage at which 100% of the modules are tested. The value specified refers to a test duration of 1 minute. For a test duration of 1 second, the insulation test voltage will be 20% higher. Attention must be paid to the fact that, in AC voltage measurements, a capacitive current is conducted through the insulator which looks like a leakage current. Such capacitive current does not occur in DC current measurements.

Thermal resistance $R_{th(j-c)}$

The thermal resistance between chip and module case is given for different current waveforms (cont. = DC, sin.180° = sinusoidal half-waves and rec.120° = rectangular current with a current conduction angle of 120°) as well as for the entire module and for a single chip.

Thermal resistance $R_{th(c-s)}$

The thermal resistance between module base plate and heatsink is also given for the entire module and for a single chip. This value applies to the use of thermal paste in the recommended thickness.

3.2.6.2 Diagrams

Power dissipation over current, as well as ambient temperature T_a over thermal resistance of junction to ambient $R_{th(j-a)}$ including the contact thermal resistance case to heatsink are indicated in the form of double characteristics for the following:

1/2 module (one single chip), mean on-state power dissipation P_{TAV} as a function of the mean on-state current I_{TAV} for different current waveforms

1 module, total power dissipation P_{Vtot} as a function of the maximum rated RMS current I_{RMS} at full cycle conduction

2 modules in a two-pulse bridge circuit (B2), total power dissipation P_{Vtot} as a function of the maximum direct output current of the complete circuit I_D for resistive load (R) and inductive load (L)

3 modules in a six-pulse bridge circuit (B6) and in a three-phase ac-controller (W3), total power dissipation P_{Vtot} as a function of the direct current I_D or the maximum rated RMS current per phase I_{RMS}.

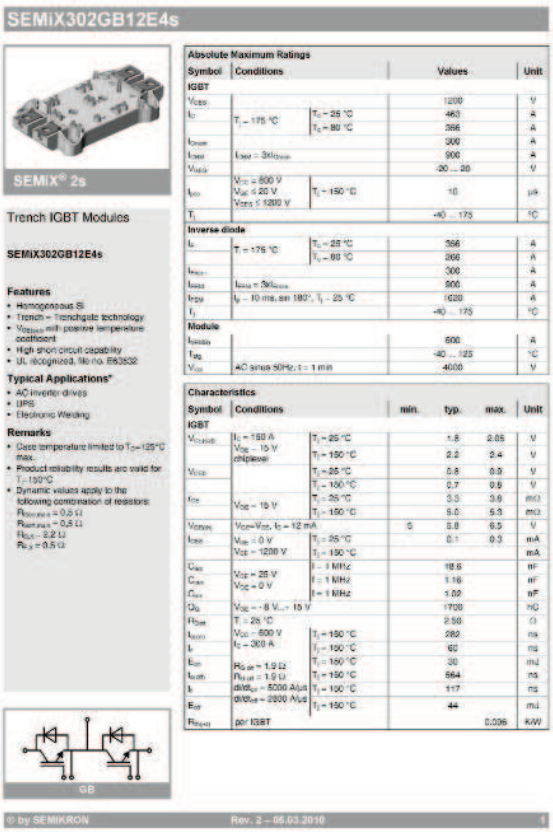
The diagrams for 1, 2, and 3 modules must be read as follows: For the total power dissipation P_{Vtot} (plotted on the left), the permissible case temperature T_c (shown on the right) is applicable. All other characteristics correspond to those for discrete diodes and thyristors.

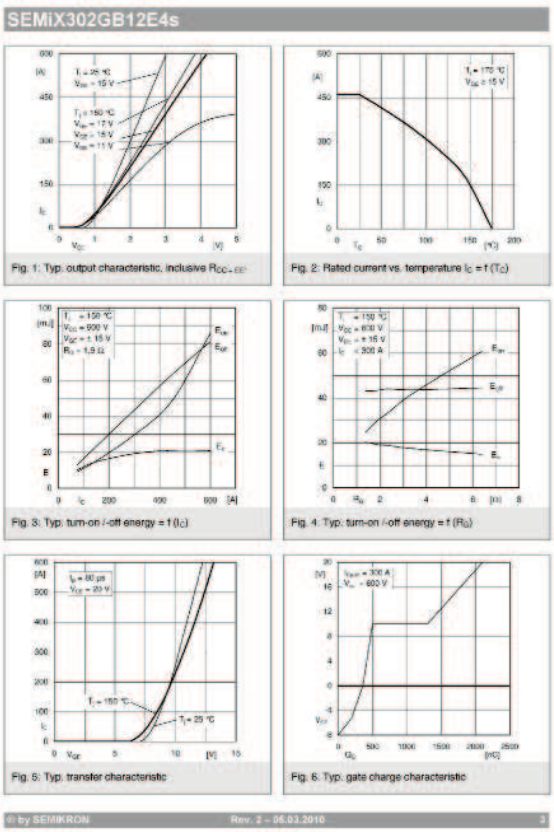
3.3 IGBT modules

When selecting IGBT modules or comparing their properties using datasheet parameters, it must be borne in mind that, owing to the different specification conditions, the values given in the datasheets of different semiconductor manufacturers are comparable to a certain extent only. In many cases, owing to the complex, application-specific interaction between different module features, additional measurements will be necessary.

Due to the developments over the past few decades, SEMIKRON datasheets also have differences with regard to datasheet layout, data content and specifications for the different generations of IGBT modules and different module designs. Since this data is to be standardised as part our product maintenance measures, the following information essentially refers to the latest datasheets issued in January 2010, i.e. the latest IGBT4 chip generation is referred to in the context of IGBT modules, cf. Figure 3.3.1. Where applicable, different datasheet structures for the datasheets of older modules which are still being produced will be pointed out expressly.

In many cases, key data such as maximum ratings and characteristics that is applicable to every different product type withing a certain product range, as well as application notes for SEMIKRON IGBT modules are not included in the product-type-specific datasheets. Instead, these are included in the "Technical Explanations" of the respective product range, e.g. the notes on safe operating areas detailed in chapter 3.3.4.





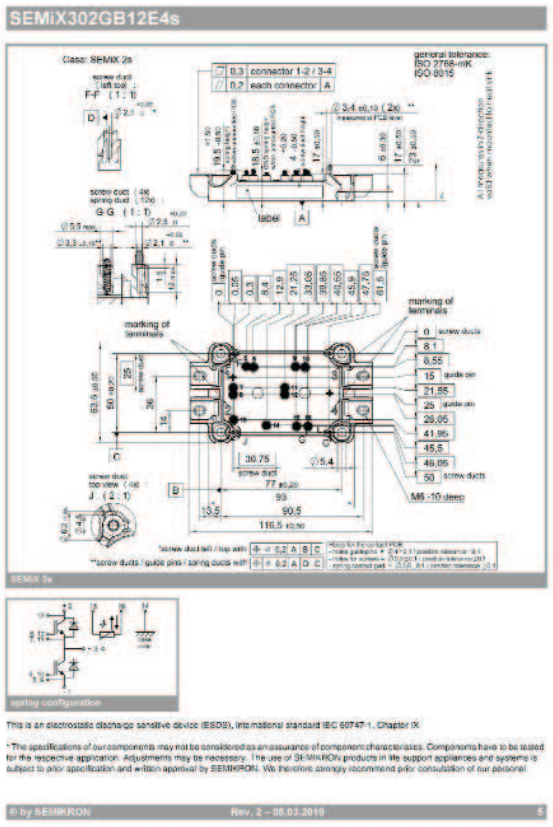


Figure 3.3.1 Datasheet layout for SEMIKRON IGBT modules

In addition to the module designation and a photo of the module, the datasheet cover contains the maximum ratings and characteristics in the form of tables which are usually continued on the next page. If applicable, the characteristics are given as minimum, typical and maximum values.

General information on the module is given under "Features" and "Typical Applications" in the shaded area to the left of the maximum ratings and characteristics. The "Remarks" section contains important information that is relevant to the datasheet specifications, e.g. operating or measurement conditions. This also includes basic diagrams of the internal circuits (e.g. half-bridge GB, chopper module GAL, cf. chapter 2.5.2.7) of the topologies described in the datasheet. The datasheet date of issue is given on all pages in the shaded footer.

The data given in the tables are followed by the diagrams usually comprising two pages. The numbering of the diagrams [Figure 1…] is based on a general numbering structure, i.e. the diagrams in a datasheet will not necessarily be numbered consecutively. The last page of the datasheet contains the module drawing including dimension data, as well as a basic diagram of the internal circuits showing the terminal layout.

The diode connected directly in parallel to the IGBT is called the inverse diode. The freewheeling diode is positioned in the bridge arm where the IGBT is not. This is of no relevance to half-bridge modules, since the inverse diode of the first IGBT serves as a freewheeling diode for the second IGBT. The freewheeling diode in chopper modules (GAL/GAR), however, may boast higher values than the inverse diode.

3.3.1 Maximum ratings

In the datasheets, the maximum ratings are specified separately for each individual component of an IGBT module (IGBT, diode, case, temperature sensor, if available). All ratings for IGBT and diodes refer to one switch (arm), irrespective of the number of IGBT or diode chips actually connected in parallel per switch (arm) in the transistor module.

Absolute Maximum Ratings				
Symbol	**Conditions**		**Values**	**Unit**
IGBT				
V_{CES}			1200	V
I_C	T_j = 175 °C	T_c = 25 °C	463	A
		T_c = 80 °C	356	A
I_{Cnom}			300	A
I_{CRM}	I_{CRM} = 3xI_{Cnom}		900	A
V_{GES}			-20 ... 20	V
t_{psc}	V_{CC} = 800 V $V_{GE} \leq$ 20 V $V_{CES} \leq$ 1200 V	T_j = 150 °C	10	µs
T_j			-40 ... 175	°C
Inverse diode				
I_F	T_j = 175 °C	T_c = 25 °C	356	A
		T_c = 80 °C	266	A
I_{Fnom}			300	A
I_{FRM}	I_{FRM} = 3xI_{Fnom}		900	A
I_{FSM}	t_p = 10 ms, sin 180°, T_j = 25 °C		1620	A
T_j			-40 ... 175	°C
Module				
$I_{t(RMS)}$			600	A
T_{stg}			-40 ... 125	°C
V_{isol}	AC sinus 50Hz, t = 1 min		4000	V

Figure 3.3.2 Datasheet excerpt: maximum ratings of an IGBT module

3.3.1.1 IGBT maximum ratings

Collector-emitter voltage V_{CES}

Maximum voltage between the collector and emitter terminals of the IGBT chips with gate-emitter short-circuited; parameters: chip temperature T_j = 25°C. The maximum collector-emitter voltage decreases in proportion to the temperature owing to the temperature dependency of the breakdown voltage. Irrespective of the load conditions, the sum of the collector-emitter supply voltage V_{CC} and the switching overvoltage $\Delta V_{CE} = L_\sigma \cdot di_C/dt$ must not exceed voltage V_{CES} (L_σ: sum of the parasitic inductance in the commutation circuit), cf. chapter 5.1.

Continuous collector current I_C

Maximum permissible continuous direct current over the collector output at which the permissible chip temperature is reached. Parameter: case temperature T_c = 25°C / 80°C, heatsink temperature T_s = 25°C / 70°C for modules without base plate; for modules which can be soldered in PCBs (SEMITOP) also maximum PCB temperature at the output terminals; chip temperature $T_j = T_{j(max)}$

I_C for IGBT modules with base plate is determined from

$I_C = P_{tot(max)}/V_{CE(sat)}$ where $P_{tot(max)} = (T_{j(max)} – T_c)/R_{th(j-c)}$,

and for modules without base plate from

$I_C = P_{tot(max)}/V_{CE(sat)}$ where $P_{tot(max)} = (T_{j(max)} – T_s)/R_{th(j-s)}$.

Since I_C designates a static maximum value, it is not relevant to switching operation.

Nominal chip current I_{Cnom}

Rated current of IGBT chips indicated in the chip manufacturer's datasheet ("Continuous collector current limited by $T_{j(max)}$") multiplied by the number of IGBT chips per switch connected in parallel in the module.

Repetitive peak collector current I_{CRM}

Peak current value at collector output during pulse operation.

I_{CRM} corresponds to the peak current indicated in the IGBT chip manufacturer's datasheet ("pulsed collector current limited by $T_{j(max)}$") multiplied by the number of IGBT chips per switch connected in parallel in the module. This parameter is independent of the pulse duration and must be adhered to, even if the maximum chip temperature is not reached. Otherwise the chip metallisation will be damaged and premature chip ageing will occur. In many datasheets I_{CRM} is indicated as $2 \cdot I_{Cnom}$; this corresponds to the former specified peak collector current I_{CM}.

For IGBT4 chips (T4, E4) currently used in SEMIKRON IGBT modules, $I_{CRM}$is specified as 3 x I_{Cnom} by the chip manufacturer. For a gate resistance specified at the nominal operating point and a high DC link voltage, it is not always possible to turn these currents off without exceeding the collector-emitter voltage V_{CES}. As shown in relevant tests, repetitive turn-off of such high currents may cause early desaturation of the hottest chips and, consequently, involve high power losses. SEMIKRON therefore recommends turning off currents above the admissible value specified for the predecessor chip generation with $2 \cdot I_{Cnom}$ within RBSOA as an exception only and provided that suitable countermeasures are taken, e.g. DC link voltage reduction, active clamping, very slow turn-off or turn-off power dissipation reduction. Such action is likely to involve substantial losses which must be taken into account when designing the semiconductor.

Gate-emitter voltage V_{GES}

Maximum voltage between the gate and emitter terminals of the IGBT chips; parameters: case temperature T_c = 25°C

Maximum turn-on time during short-circuit t_{psc}

Maximum duration of desaturation caused by overcurrent or short-circuit at a specified supply voltage, collector-emitter voltage and chip temperature; parameters: collector-emitter supply voltage V_{CC}, maximum gate-emitter voltage V_{GE}, maximum collector-emitter voltage V_{CES}, chip temperature T_j (for the latest Infineon chips < $T_{j(max)}$).

Operating temperature range T_j; $T_{j(min)}$....$T_{j(max)}$

Permissible IGBT chip temperature within which the IGBT module may be operated; especially under permanent load the chip temperature should be kept at least 25 K below $T_{j(max)}$.

3.3.1.2 Maximum ratings of integrated inverse diodes (freewheeling diodes)

Inverse diode forward current I_F

Maximum rated direct reverse current at collector output; parameters: case temperature T_c = 25°C / 80°C, heatsink temperature T_s = 25°C / 70°C for modules without base plate; also maximum PCB temperature at the output terminals of modules which can be soldered onto PCBs (SEMITOP); chip temperature $T_j = T_{j(max)}$

Nominal diode chip current I_{Fnom}

Rated current of the diode chips used as indicated in the chip manufacturer's datasheet ("Continuous direct current (diode) limited by $T_{j(max)}$") multiplied by the number of chips connected in parallel in the module per switch.

Repetitive peak forward current of the inverse diode I_{FRM}

Today's SEMIKRON modules feature $I_{FRM} = 3 \cdot I_{Fnom}$, where I_{Fnom} is the rated current of the chips used as indicated in the chip manufacturer's datasheet ("forward current limited by $T_{j(max)}$"), multiplied by the number of diode chips connected in parallel in the module per switch.

Surge forward current I_{FSM}

If the CAL inverse diodes are used as line rectifiers, their non-repetitive short-time overload capability is definitive for the choice of protective circuits. As is the case with conventional rectifier diodes, the surge forward current I_{FSM} is the forward current surge peak in the form of a 50 Hz sinusoidal half wave which the diode is able to withstand without being damaged in the event of a malfunction (short-circuit), provided this is does not occur too often during the diode lifetime. If a rectifier diode is exposed to surge forward current load, the chip temperature may temporarily rise to as much as 400°C. Therefore, should a reverse voltage occur immediately after a diode has been exposed to surge current load, the permissible surge forward current peak will be lower than if no subsequent reverse voltage is involved. The duration of single or several subsequent phases can be determined from the surge forward current characteristics, also for conventional diodes (Figure 3.3.3). Parameter: chip temperature T_j

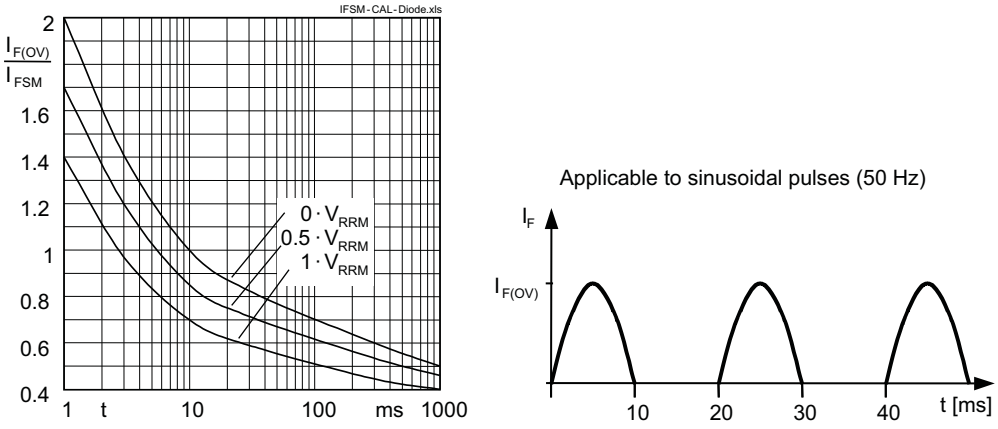


Figure 3.3.3 Surge forward current characteristics: Overload forward currents $I_{F(OV)}$ permissible in the event of a malfunction as a function of time related to surge forward current I_{FSM} at 10 ms under different reverse voltage conditions directly after the last half sine wave.

The peak load integral required for the choice of fuses can be determined from I_{FSM} as follows (also see chapter 3.2.4.1 or 4.4.6.)

$$\int_0^{t_{hw}} i_{FS}^2 \, dt = I_{FSM}^2 \cdot \frac{t_{hw}}{2}$$

t_{hw} : Duration of the sinusoidal half wave for which I_{FSM} applies (e.g. 10 ms at 50 Hz)

Operating temperature range T_j; $T_{j(min)}$....$T_{j(max)}$

Permissible inverse diode chip temperature range within which the IGBT module may be operated. Under permanent load, the chip temperature should be kept to at least 25 K below $T_{j(max)}$.

3.3.1.3 Maximum module ratings

RMS on-state current $I_{t(RMS)}$

Maximum on-state current effective value, averaged over a full operating cycle; the maximum rated RMS on-state current is applicable to any current characteristic, conduction angle or cooling conditions. It depends on the current carrying capacity of the internal connections and the external terminals of the IGBT module.

Storage temperature range T_{stg}; $T_{stg(min)}$....$T_{stg(max)}$

Temperature range within which the module may be stored or transported without being subject to electrical load; $T_{stg(max)}$ is the maximum permissible case temperature for SEMIKRON modules in application.

Soldering temperature T_{sol} for the output terminals (for modules with soldered terminals)

Maximum temperature to which the output terminals may be exposed when soldered onto a PCB; parameter: exposure time; see assembly instructions in chapter 6.3.4

Insulation test voltage V_{isol}

RMS value of the permissible test voltage (50 Hz AC voltage) between the short-circuited terminals and insulated module base plate; parameter: test duration (1 min or 1 s); for details see chapter 5.1.1.2

3.3.2 Characteristics

In the datasheets, the characteristics are likewise specified separately for each individual component of an IGBT module. Again, all characteristics refer to one switch, irrespective of the number of parallelled IGBT or diode chips per switch in the transistor module.

3.3.2.1 IGBT characteristics

Characteristics						
Symbol	**Conditions**		**min.**	**typ.**	**max.**	**Unit**
IGBT						
$V_{CE(sat)}$	I_C = 150 A V_{GE} = 15 V chiplevel	T_j = 25 °C		1.8	2.05	V
		T_j = 150 °C		2.2	2.4	V
V_{CE0}		T_j = 25 °C		0.8	0.9	V
		T_j = 150 °C		0.7	0.8	V
r_{CE}	V_{GE} = 15 V	T_j = 25 °C		3.3	3.8	mΩ
		T_j = 150 °C		5.0	5.3	mΩ
$V_{GE(th)}$	V_{GE}=V_{CE}, I_C = 12 mA		5	5.8	6.5	V
I_{CES}	V_{GE} = 0 V V_{CE} = 1200 V	T_j = 25 °C		0.1	0.3	mA
		T_j = 150 °C				mA
C_{ies}	V_{CE} = 25 V V_{GE} = 0 V	f = 1 MHz		18.6		nF
C_{oes}		f = 1 MHz		1.16		nF
C_{res}		f = 1 MHz		1.02		nF
Q_G	V_{GE} = - 8 V...+ 15 V			1700		nC
R_{Gint}	T_j = 25 °C			2.50		Ω
$t_{d(on)}$	V_{CC} = 600 V I_C = 300 A $R_{G\ on}$ = 1.9 Ω $R_{G\ off}$ = 1.9 Ω di/dt_{on} = 5000 A/µs di/dt_{off} = 2800 A/µs	T_j = 150 °C		282		ns
t_r		T_j = 150 °C		60		ns
E_{on}		T_j = 150 °C		30		mJ
$t_{d(off)}$		T_j = 150 °C		564		ns
t_f		T_j = 150 °C		117		ns
E_{off}		T_j = 150 °C		44		mJ
$R_{th(j-c)}$	per IGBT				0.096	K/W

Figure 3.3.4 Datasheet excerpt: characteristics of an IGBT module

Collector-emitter saturation voltage $V_{CE(sat)}$

Saturation value of collector-emitter voltage (on-state voltage drop of the active IGBT) for a specified collector current I_C(usually at I_{Cnom}); parameters:$_C$, gate-emitter voltage V_{GE}, chip temperature, e.g. T_j = 25°C/150°C.

At rated current, the $V_{CE(sat)}$ value of IGBT modules manufactured by SEMIKRON increases in proportion to temperature. $V_{CE(sat)}$ values included in the more recent datasheets usually refer to chip level (see relevant notes under "Conditions"). To calculate the saturation voltage across the main terminals, the voltage drop across the module lead resistors (bonding wires, terminals, ...) $R_{CC'+EE'}$ (explained under module layout characteristics) must be taken into account; when calculating chip losses, in contrast, this may be neglected.

Collector-emitter threshold voltage V_{CE0} and on-state slope resistance r_{CE} of the forward characteristic approximation

To calculate the forward losses, the elements of an equivalent straight line are given in the datasheets as

$$V_{CE(sat)} = f(I_C) = V_{CE0} + r_{CE} \cdot I_C$$

i.e. the equivalent straight line of a diode characteristic is used to approximate the saturation voltage characteristic. Figure 3.3.5 gives a definition of V_{CE0} and r_{CE}: r_{CE} is the slope of the line which results when $V_{CE(sat)}$ at 25% I_{Cnom} is connected with $V_{CE(sat)}$ at I_{Cnom}. V_{CE0} is the point where this line crosses the axis I_C = 0. Parameter: collector current I_C, Gate-emitter voltage V_{GE}, chip temperature, e.g. T_j = 25°C/150°C.

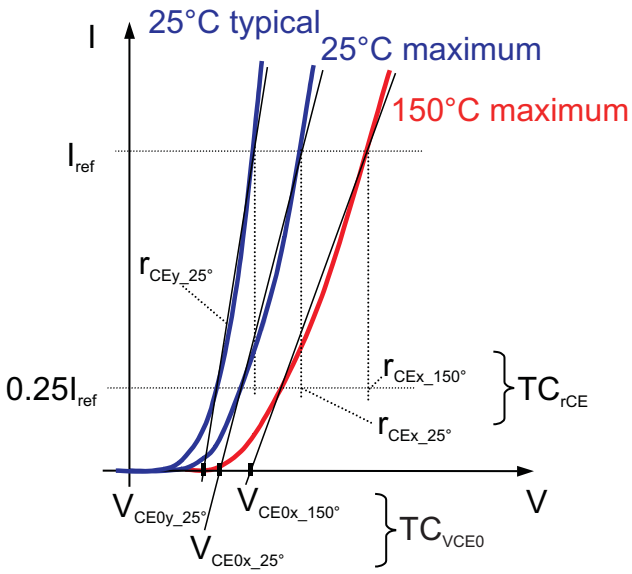


Figure 3.3.5 forward characteristics of an IGBT and definition of the elements of an equivalent straight line

Gate-emitter threshold voltage $V_{GE(th)}$

Gate-emitter voltage above which considerable collector current will flow; parameter: collector-emitter voltage $V_{CE} = V_{GE}$, collector current I_C, case temperature $T_c = 25°C$.

Collector-emitter cut-off current I_{CES}

Collector-emitter blocking current with gate-emitter short-circuited ($V_{GE} = 0$) and collector-emitter voltage $V_{CE} = V_{CES}$; parameter: chip temperature, e.g. Tj = 25°C/150°C; I_{CES} rises from few µA at 25°C to some mA at T_j= 125°C. Depending on V_{CES} this value multiplies by 1.5 to 2 every 10 K of temperature rise. For modules with an integrated inverse diode, the blocking currents of both components are indicated only once as a common parameter I_{CES}.

Input capacitance C_{ies}

Low-signal capacitance between collector and emitter with gate-emitter short-circuited for AC current; parameters: Collector-emitter direct voltage V_{CE}, measuring frequency f = 1 MHz, case temperature $T_c = 25°C$.

Output capacitance C_{oes}

Low-signal capacitance between gate and emitter with collector-emitter short-circuited for AC current; parameters: collector-emitter direct voltage V_{CE}, measuring frequency f = 1 MHz, case temperature $T_c = 25°C$

Reverse transfer capacitance (Miller capacitance) C_{res}

Low-signal capacitance between collector and gate; parameters: collector-emitter direct voltage V_{CE}, measuring frequency f = 1 MHz, case temperature $T_c = 25°C$

Gate charge Q_G

The gate charge Q_G is the total charge required to transduce the IGBT from off-state (gate-emitter voltage $V_{GE} = V_{GE(off)}$) to saturation state ($V_{GE} = V_{GE(on)}$), see Figure 3.3.6. Parameter: case temperature $T_c = 25°C$, supply voltage V_{CC}, gate-emitter voltages $V_{GE(off)}$ and $V_{GE(on)}$. The gate charge is almost independent of the chip temperature and only slightly dependent on the supply voltage.

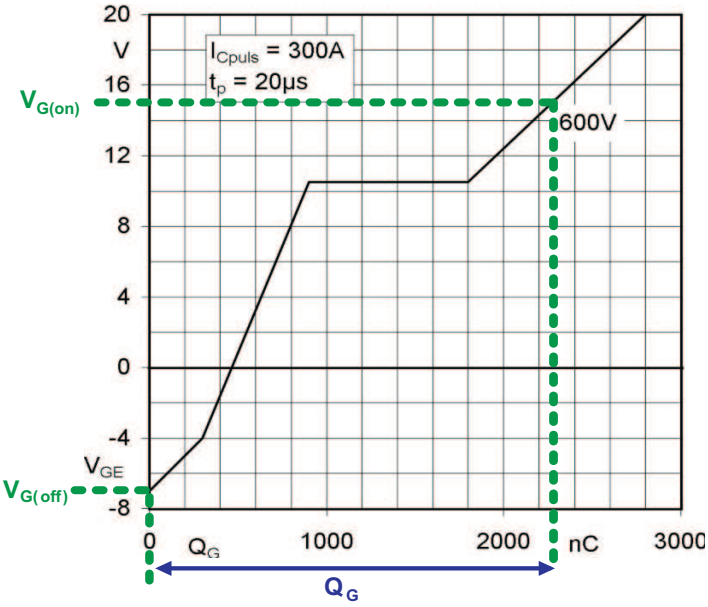


Figure 3.3.6 Gate charge characteristic of an IGBT

From Q_G using $I_{G(AV)} = Q_G \cdot f_s$ (f_s: switching frequency), the mean gate current supplied by the driver $I_{G(AV)}$ can be determined.

Internal gate resistance R_{Gint}

Parameter: chip temperature T_j = 25°C (R_{Gint} is temperature-dependent.)

Today, many IGBT chips are equipped with integrated gate resistors to avoid oscillations between paralleled chips. gives the resistances for IGBT4 chips. Table 3.3.1 gives the resistances for IGBT4 chips.

Nominal chip current I_{Cnom}	Gate resistance R_{Gint}
75 A	10.0 Ω
100 A	7.5 Ω
150 A	5.0 Ω

Table 3.3.1 Resistances of integrated gate resistors in IGBT4 chips (Infineon)

Consequently, the internal gate resistors of IGBT modules with paralleled IGBT chips are connected in parallel as well, where R_{Gint} is the total resistance resulting from paralleling. When configurating the driver circuit based on a minimum gate resistance or maximum gate peak current, the sum of the external gate resistances R_{Gon}, R_{Goff} and the internal gate resistance R_{Gint} given in the datasheet must be taken into account.

Switching times $t_{d(on)}$, t_r, $t_{d(off)}$, t_f and energy dissipation E_{on}, E_{off}

Parameter: supply voltage V_{CC}, collector current I_C, gate control voltages V_{GG+}, V_{GG-} (or V_{GE}), external gate resistances R_{Gon}, R_{Goff}, rate of rise of collector current di/dt_{on} during turn-on, or di/dt_{off} during turn-off, chip temperature T_j (switching times and losses rise in line with the junction temperature).

It must be noted that switching times, current and voltage characteristics, as well as switching losses are largely determined by the internal and external capacitances, inductances and resistances of the gate and collector circuit. For applications under operating conditions which differ clearly from the measuring conditions (e.g. capacitive load of motor cables, switching operations where $V_{GG(off)}$ = 0), the data given in the datasheets must be seen as a rough guideline only. In such cases, it is imperative that additional measurements be conducted in the real application environment to ensure safe layout of the circuitry.

Switching times indicated in IGBT datasheets are determined from a measuring circuit under ohmic-inductive load in accordance with Figure 3.2.14a. The load time constant L/R is high compared to the switching frequency cycle duration T = 1/f, meaning that the load inductance generates a continuous current. When the IGBT is in blocking state, this will flow through the freewheeling diode, commutate to the IGBT during turn-on and back to the freewheeling diode on turn-off (hard switching). Switching times refer to the gate-emitter voltage and collector current characteristics during turn-on and turn-off; cf. explanations on the physical background of current and voltage characteristics in chapter 2.4.2.2.

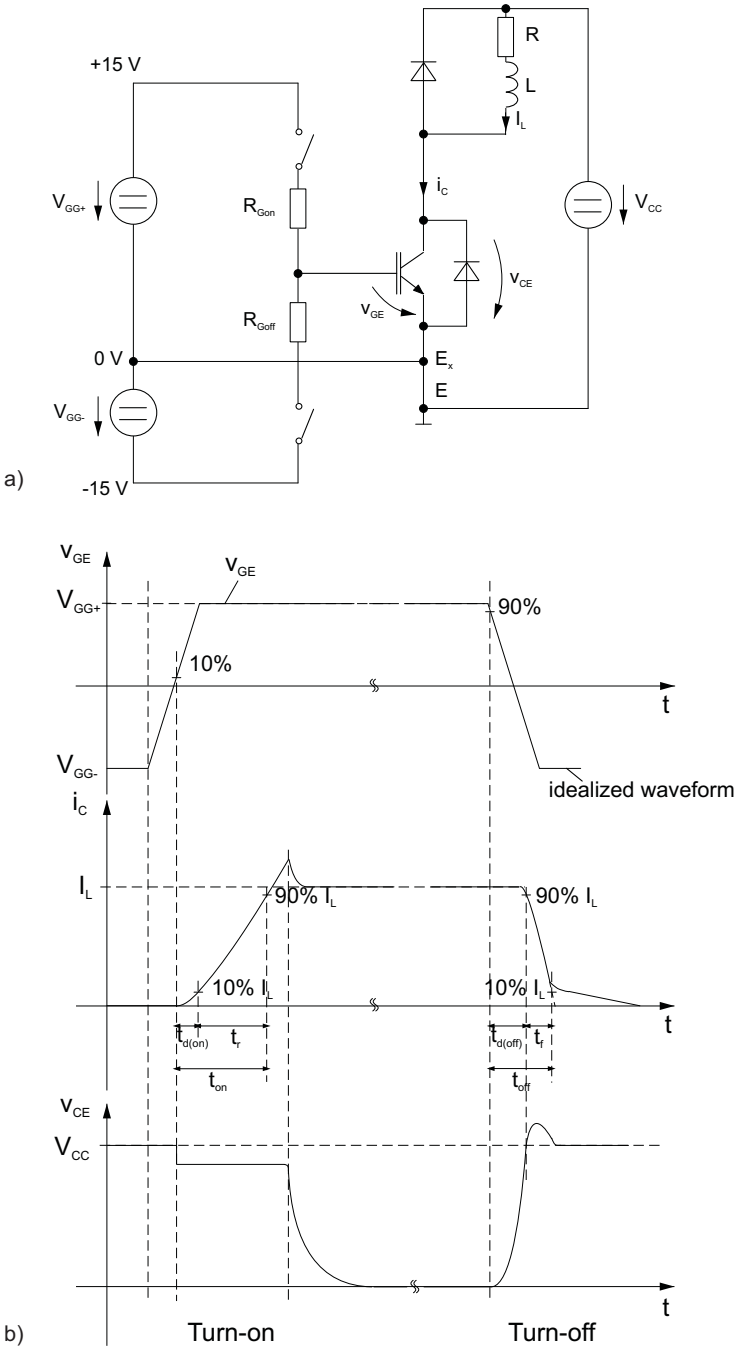


Figure 3.3.7 Switching times of IGBT: a) Measuring circuit; b) Definition of switching times under ohmic-inductive load

The **turn-on delay time $t_{d(on)}$** is defined as the time interval between the moment when the gate-emitter voltage v_{GE} has reached 10% of its end value and the collector current i_C has increased to 10% of the load current. During the subsequent **rise time t_r**, the collector current i_C increases from 10% to 90% of the load current. The sum of turn-on delay time $t_{d(on)}$ and rise time t_r is called **turn-on time t_{on}**.

In the datasheet characteristic "Typical power dissipation E_{on}, E_{off}, E_{rr} over collector current I_C", the parameter **turn-on power dissipation E_{on}** is given for a typical operating point. Switching losses can be determined by multiplying dissipation energy and switching frequency f: $P_{on} = f \cdot E_{on}$.

The turn-on power dissipation E_{on} given in SEMIKRON datasheets for IGBT modules also includes the power losses caused by the reverse peak current induced by the integrated freewheeling diode (peak reverse recovery current I_{RRM}). Furthermore, E_{on} comprises the integral of the turn-on power dissipation P_{on} up to the moment where the collector-emitter voltage V_{CE} has reached about 3% of the supply voltage V_{cc}, i.e. the power losses during dynamic saturation of the IGBT described in chapter 2.4.2.2 are also included. Figure 3.3.8 shows the characteristics of i_C and v_{CE} during real turn-on, including commutation to a conducting freewheeling diode.

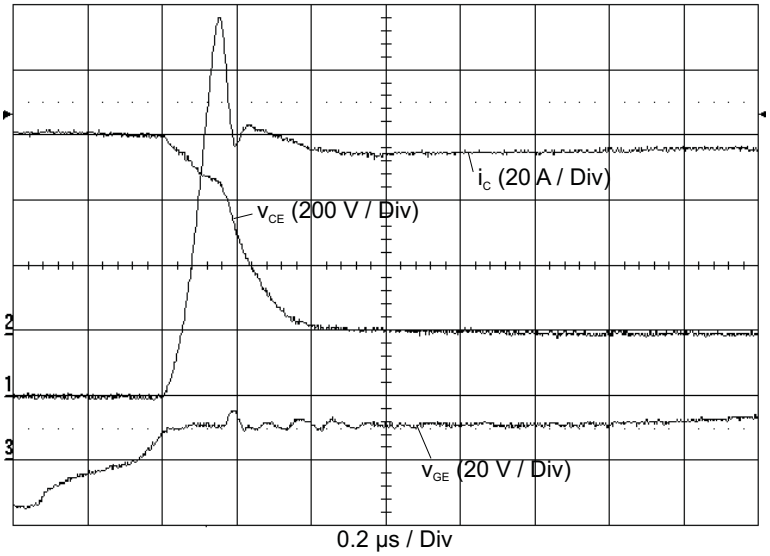


Figure 3.3.8 Turn-on of an IGBT (commutation to the conducting freewheeling diode)

The **turn-off delay time $t_{d(off)}$** is defined as the time interval between the moment when the gate-emitter voltage v_{GE} has dropped to 90 % of its turn-on value and the collector current has declined to 90 % of the load current value.

The **fall time t_f** is defined as the time interval during which the collector current i_C drops from 90% to 10% of the load current I_L. Overshooting of v_{CE} over V_{CC}, which was indicated in Figure 3.3.9, results mainly from the parasitic inductances in the commutation circuit. It grows in proportion to the increasing turn-off speed $-di_c/dt$ of the IGBT.

The sum of turn-off delay time $t_{d(off)}$and fall time t_f is called **turn-off time t_{off}**. Since at the defined end of t_{off} I_C will not have dropped to cut-off current level but will still amount to 10 % of the load current, the losses arising after t_{off} will still exceed the blocking losses. The collector current decreasing after t_{off} is called **tail current I_t** and results from the concentration of minority carriers in the n-zone, which is mainly reduced by means of recombination (see chapter 2.4.2.2). Nowadays, tail current I_t and **tail time t_t** values are not specified explicitly in the datasheets. The tail time t_t is not included in the turn-off time t_{off} by definition. Nevertheless, it contributes significantly to the switching losses; this is owing to the collector-emitter supply voltage V_{CC} which has already been applied during that time interval. Figure 3.3.9 shows a typical turn-off of an IGBT.

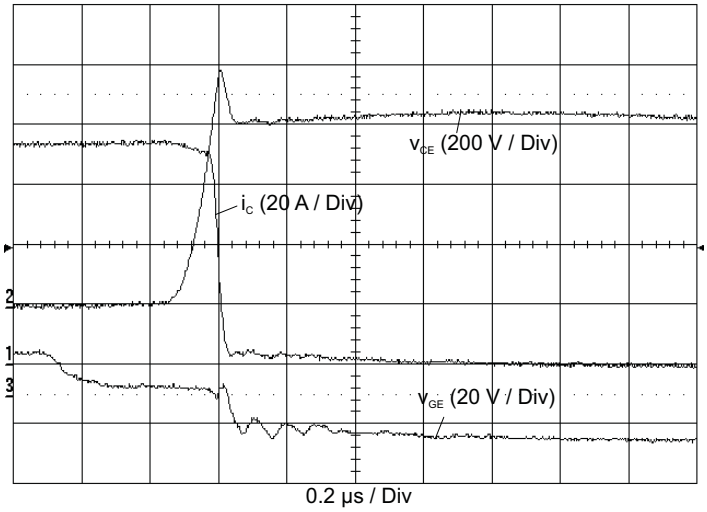


Figure 3.3.9 IGBT turn-off (commutation from the IGBT to a freewheeling diode)

In the datasheet characteristic "Typical power dissipation E_{on}, E_{off}, E_{rr} over collector current I_C", the parameter **turn-off power dissipation E_{off}** is given for a typical IGBT operating point. Switching losses can be determined by multiplying dissipation energy and switching frequency f: $P_{off} = f \cdot E_{off}$. In the turn-off energy dissipation E_{off} given in the datasheet for a SEMIKRON IGBT module, in addition to the actual losses that occur during the defined turn-off time $t_{off} = t_{d(off)} + t_f$ there are also tail current losses during tail current time t_t that occur up to the point when the collector current is 1% below the load current.

Thermal resistances $R_{th(j-c)}$ or $R_{th(j-s)}$ per IGBT

Thermal resistances characterise the static heat dissipation of an IGBT switch within a module, irrespective of the number of IGBT chips connected in parallel. Usually, several IGBT switches and freewheeling diodes are integrated in one module. For this reason, the following explanations refer briefly to the module as a whole. Figure 3.3.10 introduces the thermal models for modules with base plate (case rated devices) and without base plate (heatsink rated devices). Due to the power losses generated inside the module by the IGBT and the diodes, all of the chips are heated to $T_j = T_a + P_V \cdot \Sigma R_{th}$.

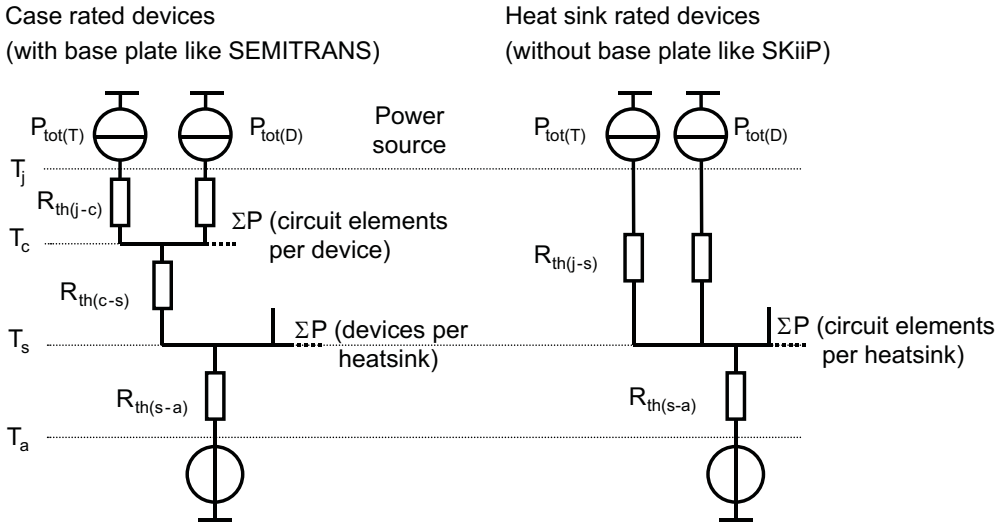


Figure 3.3.10 (Static) thermal models for modules with and without base plate

In a module with base plate, $R_{th(j-c)}$ describes the passage of heat between the IGBT chips (index j) and the module case (index c). $R_{th(j-c)}$ cannot be determined for modules without base plate (SEMITOP, SKiiP, SKiM, MiniSKiiP), which is why, in these cases, the thermal resistance $R_{th(j-s)}$ between the IGBT chips and heatsink is indicated for every IGBT switch.

$R_{th(j-c)}$ and $R_{th(j-s)}$ depend mainly on the chip area per switch and the heat transfer properties of the insulating DBC ceramic substrate. $R_{th(j-s)}$ is also determined by the thickness and properties of thermal layers between module and heatsink, as well as by the heatsink surface and the mounting torque of the fixing screws. The temperature differences ΔT over the thermal resistances are calculated for constant power dissipation P_T of the IGBT switches inside the module (irrespective of the number of paralleled chips) as follows:

Chip – base plate (module with base plate): $\Delta T_{(j-c)} = T_j - T_c = P_T \cdot R_{th(j-c)}$/IGBT switch
Chip – heatsink (module without base plate): $\Delta T_{(j-s)} = T_j - T_s = P_T \cdot R_{th(j-s)}$/IGBT switch

If the temperature of an integrated temperature sensor is referred to in the datasheet, it has to be taken into account that the sensor temperature lies between chip temperature T_j and case temperature T_c (for modules with base plate) or heatsink temperature T_s (for modules without base plate), respectively. In this case, the thermal model must be adapted similar to Figure 3.6.9 in chapter 3.6.1.3.

3.3.2.2 Characteristics of integrated hybrid inverse diodes (freewheeling diodes)

Characteristics						
Symbol	**Conditions**		**min.**	**typ.**	**max.**	**Unit**
Inverse diode						
$V_F = V_{EC}$	I_F = 300 A V_{GE} = 0 V chip	T_j = 25 °C		2.1	2.46	V
		T_j = 150 °C		2.1	2.4	V
V_{F0}		T_j = 25 °C	1.1	1.3	1.5	V
		T_j = 150 °C	0.7	0.9	1.1	V
r_F		T_j = 25 °C	2.2	2.8	3.2	mΩ
		T_j = 150 °C	3.3	3.9	4.3	mΩ
I_{RRM}	I_F = 300 A di/dt_{off} = 4300 A/µs V_{GE} = -15 V V_{CC} = 600 V	T_j = 150 °C		230		A
Q_{rr}		T_j = 150 °C		50		µC
E_{rr}		T_j = 150 °C		19		mJ
$R_{th(j-c)}$	per diode				0.17	K/W

Figure 3.3.11 Datasheet excerpt: characteristics of a hybrid inverse diode (freewheeling diode)

Forward voltage $V_F = V_{EC}$ of an inverse diode

Collector-emitter voltage drop in reverse direction; parameter: V_{GE} = 0 V; forward current I_F; chip temperature T_j; measurements taken at chip or terminal level. The forward characteristics in Figure 3.3.12 illustrate the temperature coefficient of V_F which changes from negative to positive in the rated current range.

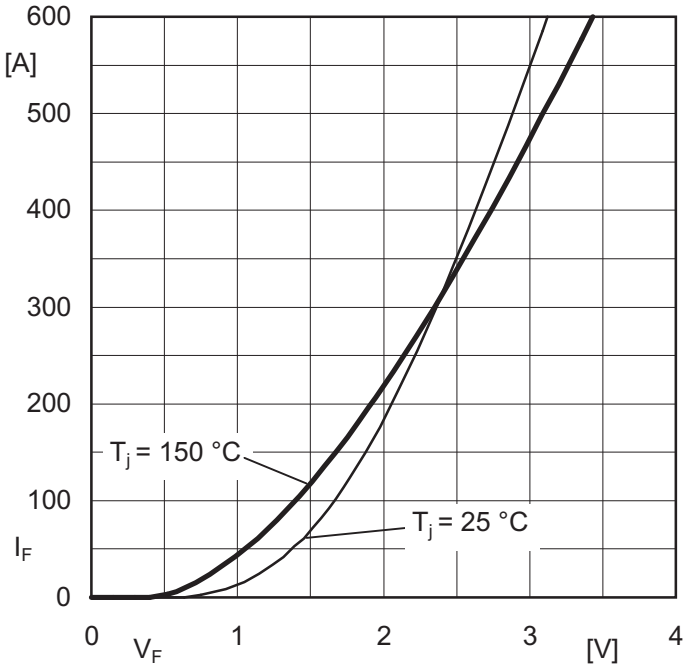


Figure 3.3.12 Forward characteristics of an inverse diode (CAL diode)

Threshold voltage V_{F0} of an inverse diode, forward slope resistance r_F of an inverse diode

To calculate the inverse diode forward losses, the elements of an equivalent straight line are indicated in the datasheets; here, the definitions correspond to those for V_{CE0} and r_{CE} as given in "IGBT Characteristics".

$V_F = f(I_F) = V_{F0} + r_F \cdot I_F$

Parameter: V_{GE} = 0 V, forward current I_F; chip temperature T_j; measurements taken at chips or terminals

Peak reverse recovery current I_{RRM} of an inverse diode

Peak value of the reverse current after inverse diode switchover from forward (parameter I_F) to reverse load, cf. Figure 2.3.8 and related explanations.

Parameters for dynamic diode characteristics I_{RRM}, Q_{rr} and E_{rr}: supply voltage V_{CC}, diode forward current I_F, control voltage V_{GG-} (or V_{GE}), rate of fall of the diode $-di_F/dt$ = rate of rise of collector di_C/dt during turn-on, chip temperature T_j)

Recovered charge Q_{rr} of an inverse diode

Total charge flowing from the diode to the outer circuit after switchover from forward to reverse load, i.e. the amount of charge that has to be taken up by the IGBT during turn-on; this depends on the forward current I_F prior to switching, the rate of fall of the decaying current $–di_F/dt$, and chip temperature T_j (For details see explanations on Figure 2.3.9 in chapter 2.3). Q_{rr} is highly dependent on temperature.

Turn-off energy dissipation E_{rr} of an inverse diode

In the datasheet characteristic "Typical power dissipation E_{on}, E_{off}, E_{rr} over collector current I_C", the parameter E_{rr} is given for a typical IGBT operating point. Switching losses of the inverse diodes during freewheeling operation can be determined by multiplying dissipation energy and switching frequency f: $P_{off} = f \cdot E_{rr}$.

Thermal resistances $R_{th(j-c)}$ or $R_{th(j-s)}$ per inverse diode

The explanations given for the characteristic "Thermal resistances $R_{th(j-c)}$ and $R_{th(js)}$ per IGBT" also apply to inverse diodes, provided the "IGBT" is replaced by "inverse diode" and P_T is replaced by P_D. If the temperature of an integrated temperature sensor is referred to in the datasheet, it has to be taken into account that the sensor temperature lies between chip temperature T_j and case

temperature T_c (for modules with base plate) or heatsink temperature T_s (for modules without base plate), respectively. In this case, the thermal model must be adapted similar to Figure 3.6.9 in chapter 3.6.1.3.

3.3.2.3 Module layout characteristics

Parasitic collector-emitter inductance L_{CE}

Sum of all parasitic inductances between collector (TOP) and emitter (BOT) terminal determined from the inductive voltage drop measured during switching. The partial inductances L_C and L_E depicted in Figure 3.3.13 represent the total inductances of the bond connections and terminals.

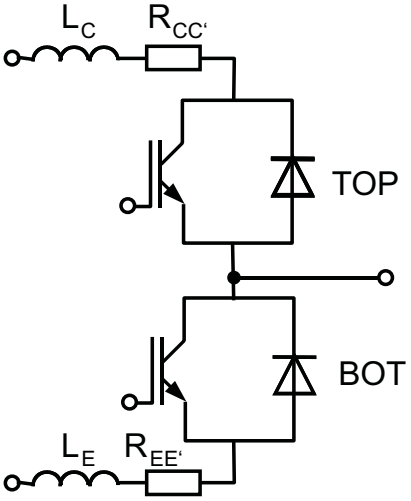


Figure 3.3.13 Parasitic inductances and resistances of an IGBT module $L_C + L_E = L_{CE}$, and $R_{CC'} + R_{EE'} = R_{CC'+EE'}$

Parasitic terminal-to-terminal ohmic resistances $R_{CC'+EE'}$

In recent datasheets, $V_{CE(sat)}$ is normally given at chip level (see relevant note under "Conditions"); for this reason the voltage drop across the module lead resistors (bond wires, terminals etc.) must be determined separately in order to calculate the saturation voltage across the main terminals. To do so, all partial resistances of one half-bridge module are pooled to obtain the terminal resistance $R_{CC'+EE'}$ indicated in the datasheet. Again, the partial resistances $R_{CC'}$ and $R_{EE'}$ depicted in Figure 3.3.13 also represent the sum of resistances of the bond connections and terminals.

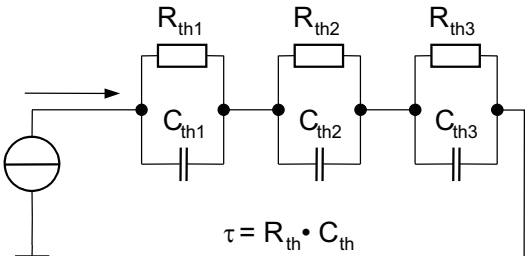
Thermal resistance $R_{th(c-s)}$ per IGBT module

In IGBT modules with base plate, the thermal resistance $R_{th(c-s)}$ describes the passage of heat between the module base plate (index c) and the heatsink (index s – cf. Figure 3.3.10, Case rated devices). This characterises the static heat dissipation of an IGBT module with one or more IGBT and freewheeling diodes and depends on the module size, heatsink and case surfaces, thickness and parameters of thermal layers between module and heatsink, as well as on the mounting torque of the fixing screws. The temperature difference ΔT_{c-s} between case temperature T_c and heatsink temperature T_s for constant power dissipation P_V of the integrated IGBT and diodes results in $\Delta T_{c-s} = T_c - T_s = \Sigma P_V \cdot R_{th(c-s)}$

In modules without base plate (SEMITOP, SKiiP, SKiM, MiniSKiiP) it is not possible to separately determine $R_{th(j-c)}$ and $R_{th(c-s)}$. Rather, only $R_{th(j-s)}$ can be specified per IGBT switch or diode (aggregated for all parallel chips) (Figure 3.3.10 - Heatsink rated devices). If the temperature of an integrated temperature sensor is referred to in the datasheet, it has to be taken into account that the sensor temperature lies between chip temperature T_j and case temperature T_c (for modules with base plate) or heatsink temperature T_s (for modules without base plate), respectively. In this case, the thermal model must be adapted similar to Figure 3.6.9 in chapter 3.6.1.3.

Thermal impedances $Z_{th(j-c)}$ or $Z_{th(j-c)I}$ per IGBT and $Z_{th(j-c)D}$ per inverse diode

In addition to the thermal resistances, thermal impedances which describe the dynamic heat dissipation behaviour are also included in the thermal equivalent circuit diagram (Figure 3.3.14). The thermal impedances Z_{th} are indicated either numerically as parameters R_i and τ_i of a thermal model with 3 or 4 time constants or in the form of diagrams [Figure 9]; (see Figure 3.3.23 and the corresponding explanations).



$$Z_{th} = \sum_{i=1}^{n} R_{thi} \cdot \left(1 - e^{\frac{t}{\tau_i}}\right)$$

Figure 3.3.14 Dynamic thermal model, where $\tau_i = R_{thi} \cdot C_{thi}$

Paralleled IGBT or diode chips are treated as one component. For modules without base plate, the module-specific impedance $Z_{th(j-c)}$ must be replaced with $Z_{th(j-s)I}$ per IGBT and $Z_{th(j-s)D}$ per inverse diode. If the temperature of an integrated temperature sensor is referred to in the datasheet, it has to be taken into account that the sensor temperature lies between chip temperature T_j and case temperature T_c (for modules with base plate) or heatsink temperature T_s (for modules without base plate), respectively. In this case, the thermal model must be adapted similar to Figure 3.6.9 in chapter 3.6.1.3.

Mechanical data M_s, M_t, w

The following mechanical data is provided in the datasheets:

Mounting torque M_s of the fixing screws (minimum and maximum values)
Mounting torque M_t of the terminals (minimum and maximum values)
Module weight w.

Characteristics of an internal temperature sensor R_{ts}, R_{100}, $B_{100/125}$, tolerance

The modules in various SEMIKRON product families (SEMiX, MiniSKiiP, SKiiP, SEMITOP, SKiM) are equipped with temperature sensors positioned next to the chips on the DBC ceramic substrate. Depending on their position, these sensors represent a temperature that is close to that of the base plate (for modules with base plate) or that of the heatsink (for modules with no base plate). Depending on the product family, PTC (**P**ositive **T**emperature **C**oefficient) or NTC (**N**egative **T**emperature **C**oefficient) resistors are used, the resistance of which rises or falls linear to the temperature. In the datasheets, temperature sensor specifications include the internal resistance R_{ts} or R_{100} at 25°C and 100°C, for a the measuring tolerance at 100°C and in some cases the coefficient $B_{100/125}$. The types of sensors used in specific products, as well as their properties are detailed in chapter 2.6.

3.3.3 Diagrams

Similar to the sequence in the datasheets, this chapter provides information on the diagrams in IGBT datasheets, which generally refer to one IGBT switch or freewheeling diode. Some diagrams presented here are not shown in all of the datasheets of all module families, as some are specific to certain module families. In cases where the diagram concerned is detailed in other chapters, this will be referred to.

[Fig. 1] Typical forward characteristics $I_C = f(V_{CE})$ including $R_{CC'+EE'}$

Output characteristics for T_j = 25°C and 125°C / 150°C in saturation region using parameter V_{GE} (Figure 3.3.15); the positive temperature coefficient of the collector-emitter saturation voltage $V_{CE(sat)}$ and the decrease of this voltage in line with the increase in gate-emitter voltage V_{GE}. In contrast to the tabular data, the voltage drop across the module terminals, i.e. $V_{CE(sat)}$ including voltage drops over the parasitic terminal resistances $R_{CC'+EE'}$ is illustrated in the characteristics.

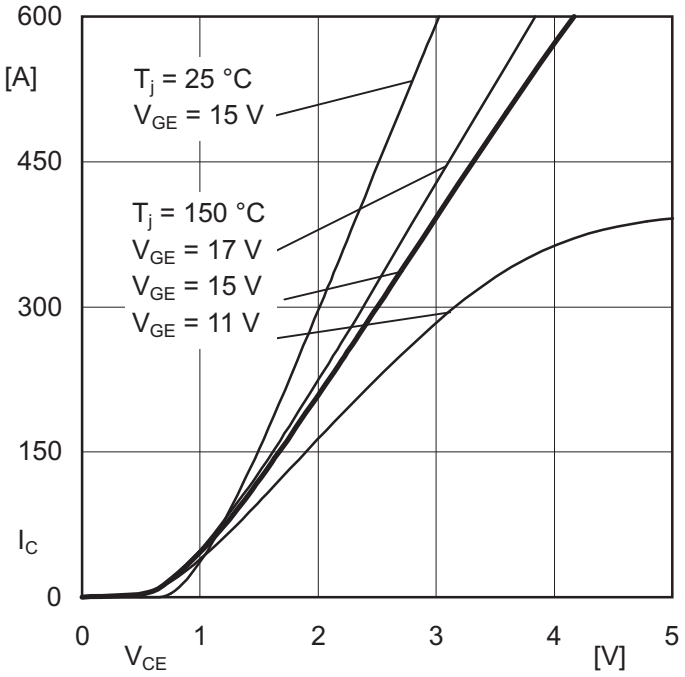


Figure 3.3.15 Typical output characteristics of an IGBT

The temperature coefficient of the forward on-state voltage $V_{CE(sat)}$ is already positive within the low-current range.

[Fig. 2] Collector current derating versus case temperature

Figure 3.3.16 shows the derating of the collector current (without additional switching losses) which is required if the case temperatures differ from the reference temperatures T_c = 25°C or 80°C given as a parameter for I_C. At temperatures above T_c = 25°C, the relation is: $I_C = (T_{j(max)} - T_c) / R_{th(j-c)} \cdot V_{CE(sat)}$. At case temperatures under T_c < 25°C , the maximum rated collector current is limited to the datasheet rating for I_C.

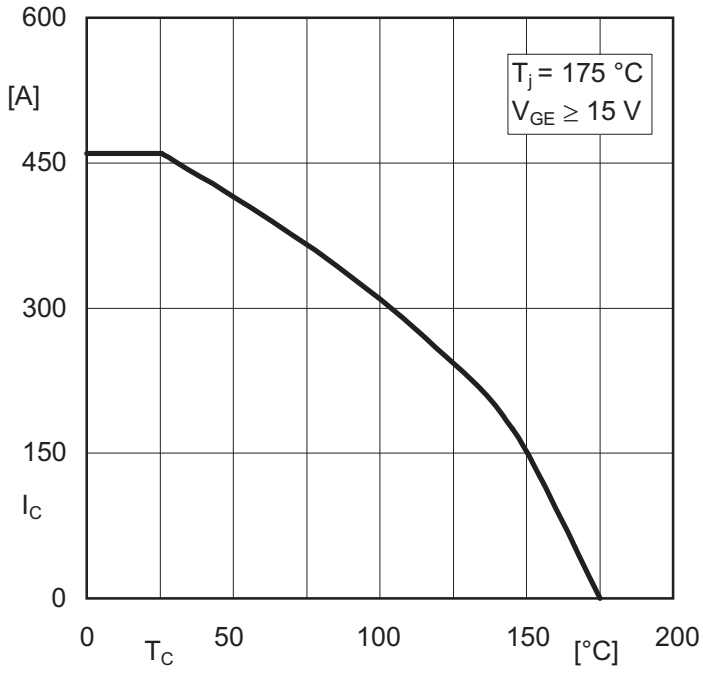


Figure 3.3.16 Derating of collector current versus case temperature

[Fig. 3] Typical switching energy E_{on}, E_{off} and E_{rr} as a function of the collector current I_C

Figure 3.3.17 shows the turn-on / turn-off power dissipation E_{on}, E_{off} of the IGBT at a typical operating point with the IGBT under high load, determined from a measuring circuit under ohmic-inductive load; also illustrated is the turn-off power dissipation E_{rr} of the inverse diode used as a freewheeling diode as a function of the collector current I_C. Switching losses can be determined by multiplying dissipation energy and switching frequency f.

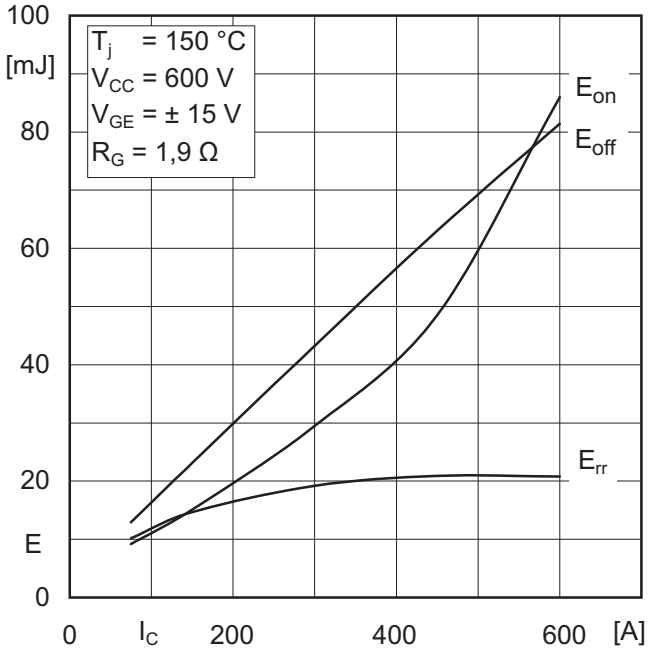


Figure 3.3.17 Turn-on/turn-off power dissipation of IGBT and freewheeling diode versus collector current

[Fig. 4] Typical switching energy E_{on}, E_{off} and E_{rr} versus external gate resistances R_G (R_{Gon}, R_{Goff})

Figure 3.3.18 shows the turn-on / turn-off power dissipation E_{on}, E_{off} of the IGBT at a typical operating point where the IGBT are under high load, determined from a measuring circuit under ohmic-inductive load for different external gate resistances R_G; also illustrated is the turn-off power dissipation E_{rr} of the inverse diode used in the module as a freewheeling diode as a function of the

gate resistance. Switching losses can be determined by multiplying dissipation energy and switching frequency f.

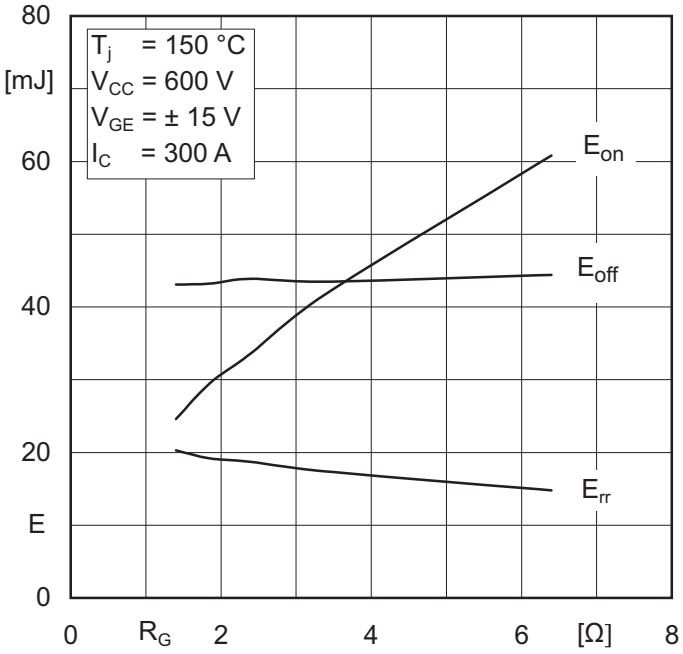


Figure 3.3.18 Turn-on / turn-off power dissipation of IGBT and freewheeling diode versus gate resistance

[Fig. 5] Typical transfer characteristic $I_C = f(V_{GE})$

The transfer characteristic in Figure 3.3.19 describes the behaviour of the IGBT in the active operating area at V_{CE} = 20 V (linear operation). The collector current is coupled with the gate-emitter voltage via $I_C = g_{fs} \cdot (V_{GE}-V_{GE(th)})$

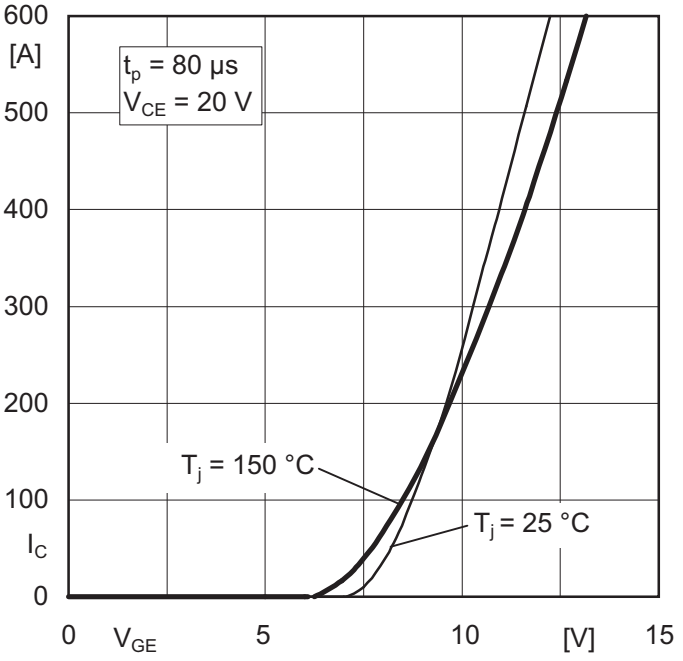


Figure 3.3.19 Transfer characteristic of an IGBT

[Fig. 6] Typical gate charge characteristic $V_{GE} = f(Q_G)$

Figure 3.3.20 shows the IGBT gate-emitter voltage V_{GE} as a function of the gate charge Q_G at 50% of the maximum permissible collector-emitter voltage V_{CE}. The gate charge characteristic illustrates the course of V_{GE} between off-state at a conventional negative gate-emitter voltage V_{GE} (e.g. -8 V) and on-state at maximum V_{GE}. This diagram may be used to determine the gate charge load Q_G required to transduce the IGBT from off-state to saturation state; also see Figure 3.3.6 and explanations.

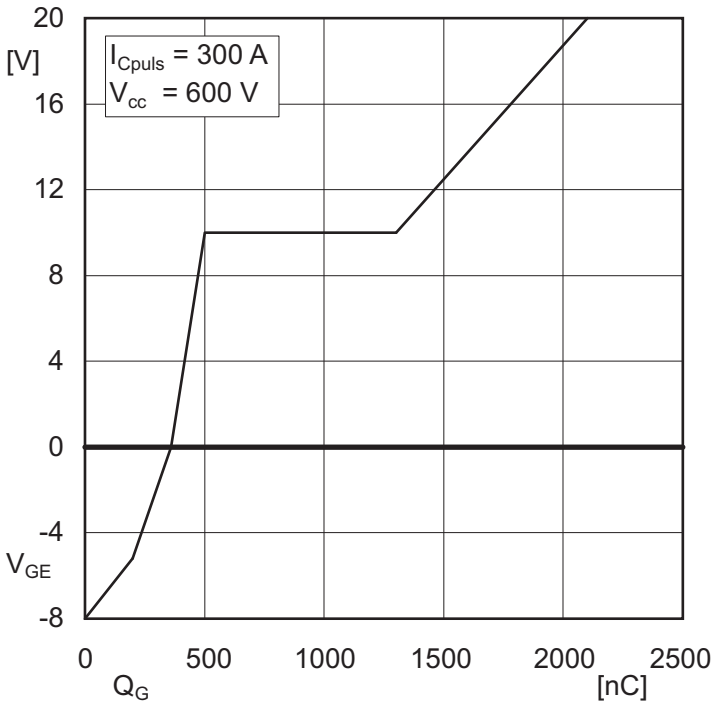


Figure 3.3.20 Gate charge characteristic of an IGBT

[Fig. 7] Typical dependency of the switching times on the collector current

Figure 3.3.21 shows the switching times $t_{d(on)}$ (turn-on delay time), t_r (rise time), $t_{d(off)}$ (turn-off delay time) and t_f (fall time) at a typical operating point determined from a measuring circuit under ohmic-inductive load as a function of the collector current I_C.

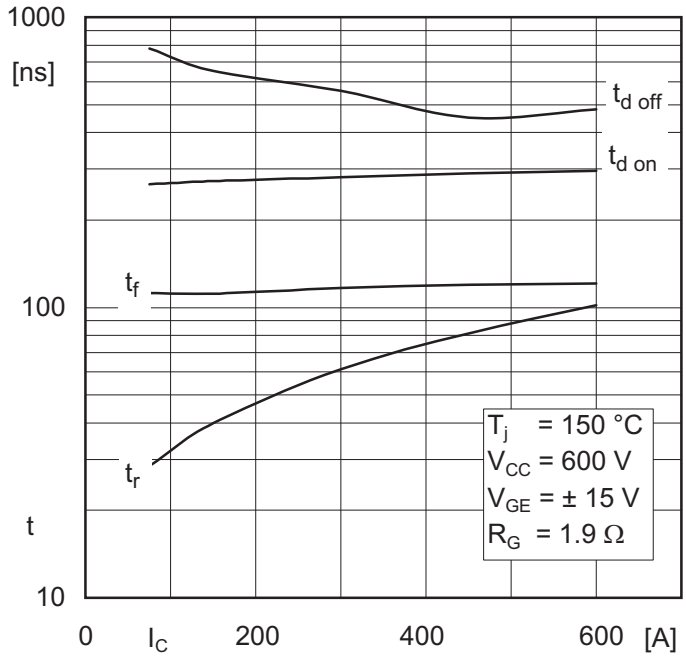


Figure 3.3.21 IGBT switching times versus collector current

[Fig. 8] Typical characteristic of the switching times versus external gate resistances R_G (R_{Gon}, R_{Goff})

Figure 3.2.22 shows the switching times $t_{d(on)}$ (turn-on delay time), t_r (rise time), $t_{d(off)}$ (turn-off delay time) and t_f (fall time) determined from a measuring circuit under ohmic-inductive load at a typical operating point for different external gate series resistances R_G as a function of the collector current I_C.

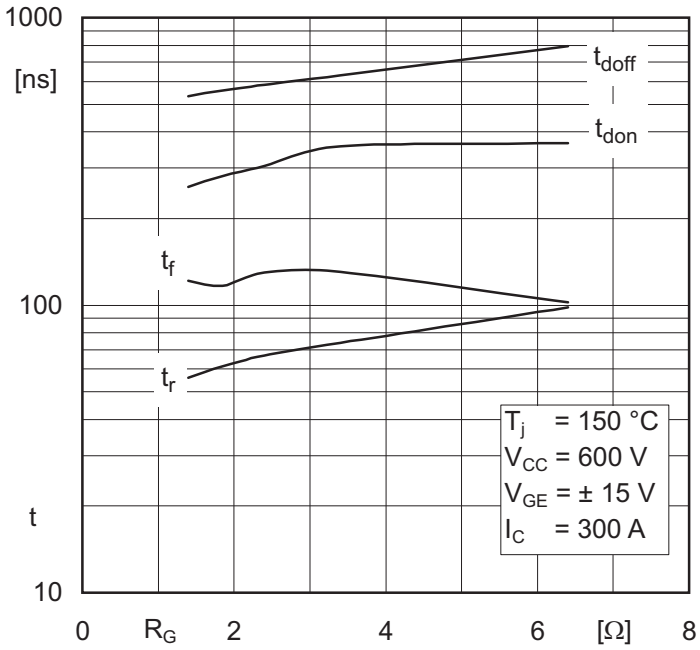


Figure 3.3.22 Switching times of IGBT and freewheeling diode versus gate resistance

[Fig. 9] Typical thermal impedances $Z_{th(j-c)}$ or $Z_{th(j-s)}$ of IGBT and inverse diode

Figure 3.3.23 shows the thermal impedances $Z_{th(j-c)}$ between chip and case using a double logarithmic scale, for an IGBT and inverse diode in single-pulse operation as a function of the pulse duration t_p; also see explanations on Z_{th} characteristics.
$Z_{th(j-c)}$ cannot be determined for modules without base plate (e.g. SEMITOP, SKiiPPACK, MiniSKiiP). For these modules, $Z_{th(j-s)}$ is indicated per IGBT or diode (aggregated for all paralleled chips) instead. The thermal impedances for single-pulse operation depicted in Figure 3.3.23 characterise the increase in chip temperature during a specified power dissipation pulse for a fixed base plate temperature ($Z_{th(j-c)}$) or heatsink temperature ($Z_{th(j-s)}$). After the chip temperature has a quasi-static value, $Z_{th(j-c)}$ or $Z_{th(j-s)}$ will reach their static end values $R_{th(j-c)}$ or $R_{th(j-s)}$.

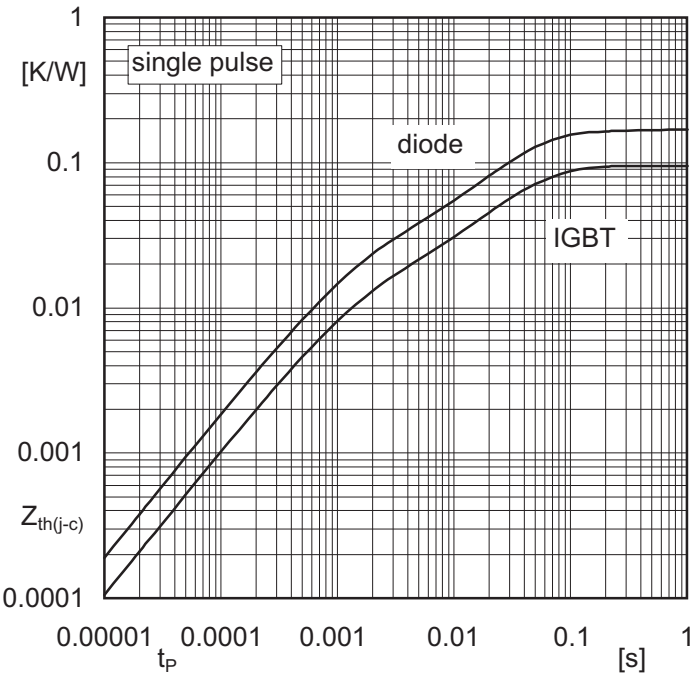


Figure 3.3.23 Thermal impedances of IGBT and inverse diode in a module with base plate

[Fig. 10] Typical inverse diode forward characteristic $I_F = -I_C = f(V_F)$ including $R_{CC'+EE'}$

Figure 3.3.24 shows the forward characteristics of an inverse diode at T_j = 25°C and 125 / 150°C (typical values). In contrast to the tabular data, the voltage drop across the module terminals, i.e.

V_F including voltage drops over the parasitic terminal resistances $R_{CC'+EE'}$ is illustrated in the characteristics. The different temperature coefficients of the forward voltage V_F can be seen: negative at low and positive at high currents.

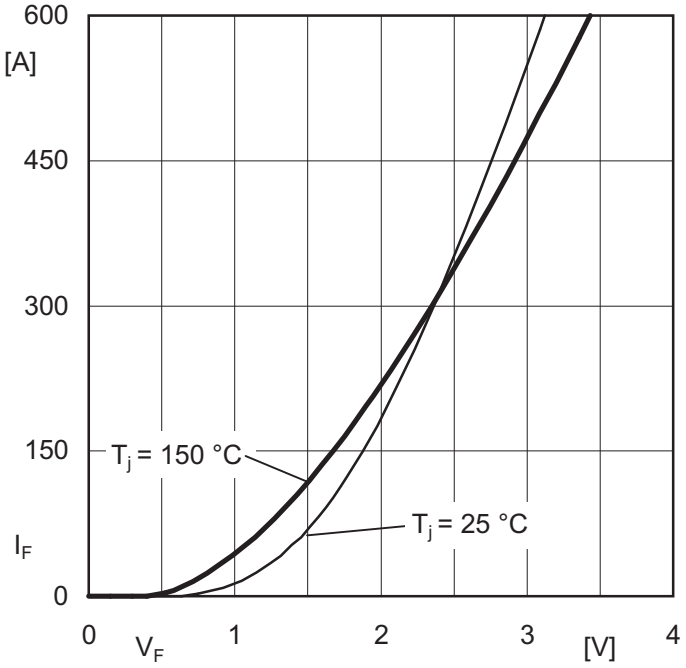


Figure 3.3.24 Forward characteristics of an inverse diode (CAL diode)

[Fig. 11] Typical peak reverse recovery current I_{RRM} of an inverse diode versus $-di_F/dt$ of the forward current I_F

Figure 3.3.25 shows typical ratings of the peak reverse recovery current I_{RRM} of the inverse diode at a typical operating point where the IGBT are under high load versus the rate of fall of the forward current $-di_F/dt$ at diode turn-off. The turn-on speed of the commutating IGBT (di_C/dt) determines the $-di_F/dt$ of the diode in dependence of the IGBT gate series resistance $R_g=R_{gon}$. For easy dimensioning, ratings for $R_G = R_{Gon}$ of the IGBT during turn-on are assigned to the diF/dt values in this diagram. The peak reverse recovery current of the freewheeling diode increases in proportion to collector current and di/dt.

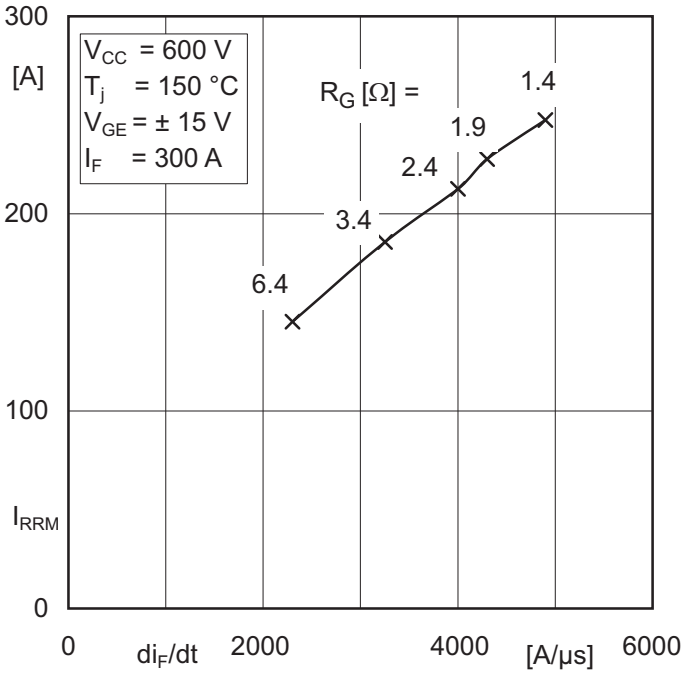


Figure 3.3.25 Peak reverse recovery current of the freewheeling diode (CAL diode) of an IGBT module

[Fig. 12] Typical recovered charge Q_{rr} of an inverse diode versus $-di_F/dt$ and forward current I_F before turn-off

Figure 3.3.26 shows typical ratings of the recovered charge Q_{rr} at a typical operating point where the IGBT are under high load versus rate of fall $-di_F/dt$ during diode turn-off and versus forward current I_F conducted before turn-off. $-di_F/dt$ is determined by the turn-on speed of the commutating IGBT (di_C/dt), which depends on the IGBT gate series resistance $R_G = R_{Gon}$ ist. For easy dimensioning, ratings for $R_G = R_{Gon}$ of the IGBT during turn-on are assigned to the di_F/dt – values in this diagram. The recovered charge of the freewheeling diode increases in proportion to the collector current and increases slightly as the di/dt increases.

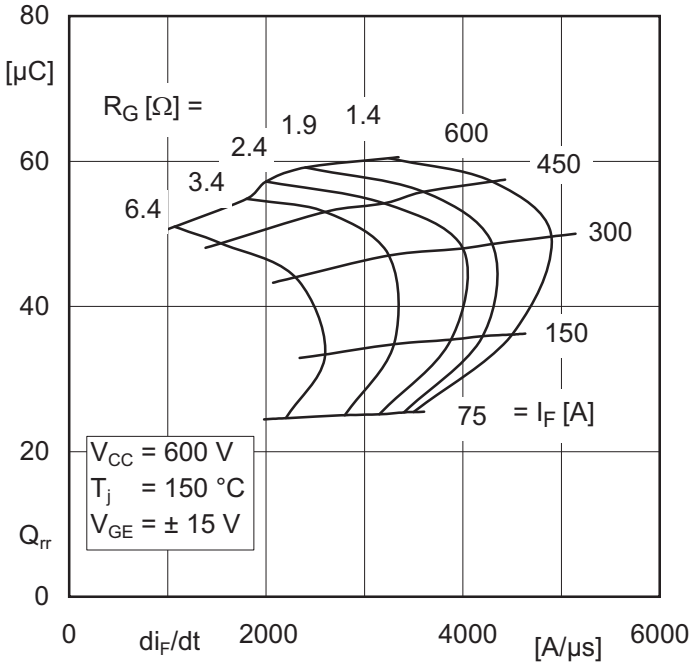


Figure 3.3.26 Recovered charge of the freewheeling diode (CAL diode) of an IGBT module

3.3.4 Safe operating areas during switching operation

Further information on the safe operating areas for SEMIKRON IGBT modules indicated in the datasheets is provided in the "Technical Explanations" on the respective product range at www.semikron.com. As explained in chapter 2.4, the IGBT has to reach a virtually rectangular characteristic i = f(v) between V_{CC} and I_L for hard switching applications. The SOA (**S**afe **O**perating **A**rea) diagrams indicate to what extent this may be realised during different operating states without risk of destruction.

SOA for turn-on and single-pulse operation
RBSOA (Reverse Biased SOA) for periodic turn-off
SCSOA (Short Circuit SOA) for non-periodic turn-off of short circuits

Most SOA diagrams refer to the chips, i.e. the specified maximum rated V_{CES} across the module terminals is reduced by the voltage induced by the parasitic module inductance L_{CE} during turn-off (RBSOA, SCSOA). This value must not be exceeded. In contrast to the chip-related data, the restriction of RBSOA and SCSOA limits over the module terminals therefore also depends on the driving conditions.

3.3.4.1 Maximum safe operating area during single-pulse operation and periodic turn-on (SOA)

Figure 3.3.27 shows the maximum curve $I_c = f(V_{CE})$ during single-pulse operation using a double logarithmic scale. The graph in Figure 3.3.27 refers to the limiting values of V_{CES} and I_{CRM}; see chapter Figure 3.2.13.

The SOA is limited by the following parameters:
- maximum collector current (horizontal limit);
- maximum collector-emitter voltage (vertical limit);

What is important is that the maximum ratings apply to currents which do not heat the IGBT to temperatures above the maximum chip temperature T_j = 150°C or 175°C. IGBT modules may be operated as switches only. Only during switching operation may IGBT modules touch the linear characteristic areas in the capacity of an active amplifier with $I_C = f(V_{GE})$. Analogous operation over a longer period of time is not permitted, since this would involve local overload due to the variation in the transfer characteristic among the IGBT cells or paralleled chips. For this reason, the diagonal characteristics contained in earlier datasheets featuring different pulse currents with maximum pulse duration and DC load to maximum power dissipation are no longer applicable.

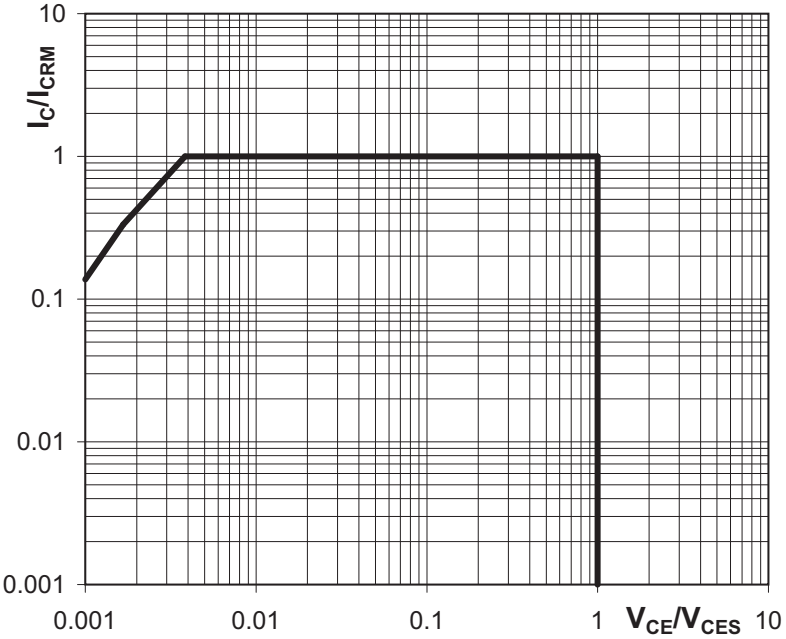


Figure 3.3.27 Maximum safe operating area $I_C = f(V_{CE})$ for single pulses and periodic turn-on (SOA); standardised and referenced to V_{CES} and I_{CRM}

3.3.4.2 Turn-off safe operating area (RBSOA)

During periodic turn-off, the IGBT may effect hard turn-off of $I_{Cpuls} = I_{CRM}$ under defined driver conditions until $T_{j(max)}$ has been reached, provided V_{CE} (chip) does not exceed V_{CES} level (for the influence of parasitic inductances and driver parameters, see chapter 5.4 and 5.6). In many datasheets I_{CRM} is indicated as $2 \cdot I_{Cnom}$; this corresponds to the former specified limit for collector current I_{CM}.

For IGBT4 chips (T4, E4) currently used in SEMIKRON IGBT modules, $I_{CRM}$is specified as 3 x I_{Cnom} by the chip manufacturer. Given the gate resistance specified for the nominal operating point and high DC link voltage, it is not always possible to turn these currents off without the collector-emitter voltage V_{CES} being exceeded. As shown in relevant tests, repetitive turn-off of such high currents may cause early desaturation of the hottest chips and, consequently, involve high power losses. Therefore, SEMIKRON recommends turning off currents above the permissible value specified for the predecessor chip generation with $2 \cdot I_{Cnom}$ within RBSOA as an exception only and provided that suitable countermeasures are taken, e.g. DC link voltage reduction, active clamping, very slow turn-off or turn-off snubber circuits. Such action is likely to involve high power losses which must be taken into account when designing the semiconductors. Figure 3.3.28 the turn-off safe operating area of an IGBT.

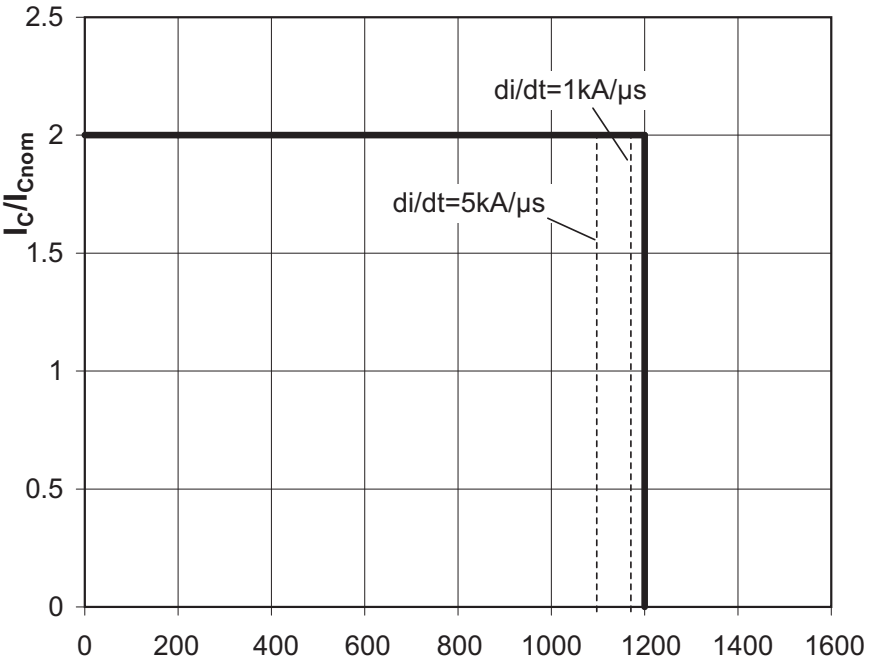


Figure 3.3.28 Turn-off safe operating area (RBSOA) of a 1200 V IGBT; $T_j < T_{j(max)}$; V_{GE}=+-15 V; $R_G=R_{G(nom)}$

The continuous line in Figure 3.3.28 shows the safe operating area at chip level. Owing to the voltage induced at the parasitic module inductances L_{CE} during turn-off, RBSOA decreases during turn-off in dependence of the collector current and the driver parameters; this value can be determined using the following equation:

$$V_{CEmaxT} = V_{CES} - L_{CE} \cdot \frac{I_C \cdot 0{,}8}{t_f(I_C)}$$

V_{CEmaxT}: maximum collector-emitter voltage at the module terminals

An example of the maximum permissible voltage at the terminals for a module inductance of 20 nH is shown as a broken line here.

3.3.4.3 Safe operating area during short circuit

Under certain conditions, the IGBT is essentially capable of turning off short circuits actively. In doing so, high power losses are generated by the IGBT working in the active operating area, causing a temporary increase in chip temperature to far beyond $T_{j(max)}$. However, the positive temperature coefficient of the collector-emitter voltage causes the circuit to stabilise and the short-circuit current is limited to $4…6 \cdot I_{Cnom}$.

When turning off a short circuit, the high short-circuit current induces a voltage at the parasitic inductances in the commutation circuit; this voltage must not cause V_{CES} to be exceeded. In order to limit the energy dissipation of the IGBT chips, short-circuit turn-off is subject to the following conditions:

- The short circuit has to be detected and turned off within max. 10 µs (6 µs for 600 V Trench IGBT).
- The time between two short circuits has to be at least 1 second.
- The IGBT must not be subjected to more than 1000 short circuits during its total operation time.
- The maximum chip temperature before a short circuit occurs is limited to 150°C; this is also true for IGBT4 ($T_{j(max)}$ = 175°C).
- The maximum voltage V_{CC} decreases, e.g. to 800 V for a 1200 V IGBT4.
- The prevailing $-di_c/dt$ maximum ratings must be controlled by the driver parameters and in extreme cases, they can be achieved by means of multi-state turn-off only ("soft turn-off", cf. chapter 5.1.1).
- If necessary, non-permissible increase in gate-emitter voltage during short-circuit turn-off will have to be prevented by clamping.

Figure 3.3.29 gives an example of the dependency of the permissible short-circuit current I_{SC} (in relation to I_{Cnom}) on the V_{CE}/V_{CES} ratio for a defined di/dt during turn-off. Here, too, it must be taken into consideration that the voltage at the terminals is exceeded by the chip voltage to the amount of $L_S \cdot di/dt$, meaning the maximum external voltage has to be reduced accordingly.

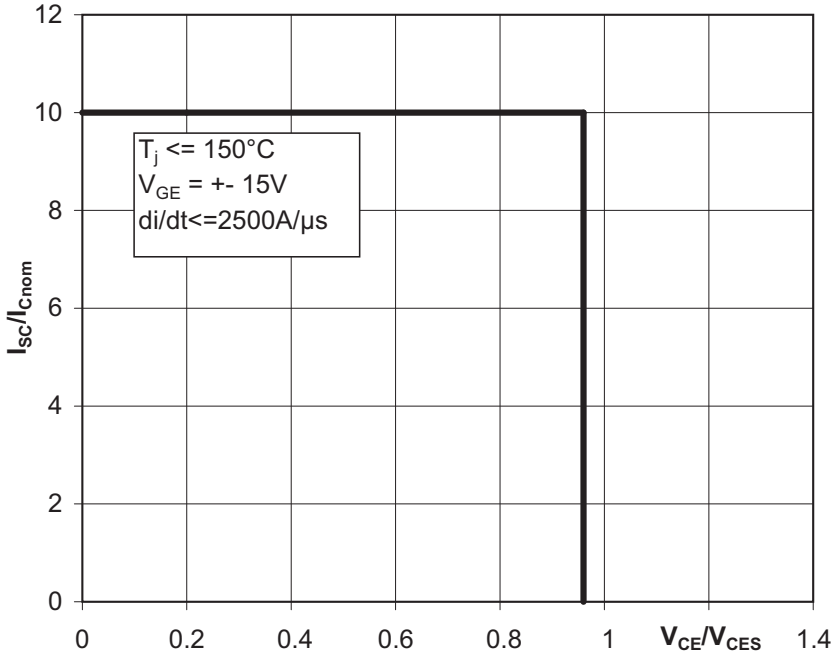


Figure 3.3.29 Safe operating area during short circuit (SCSOA)

3.4 Power MOSFET modules

When selecting MOSFET modules or comparing their properties using datasheet entries, it must be taken into account that the values given in the datasheets of different semiconductor manufacturers are only comparable to a certain extent, because the specification conditions may differ. In many cases, owing to the complex, application-specific interaction between different module features, additional measurements will be necessary.

Due to developments in the past decades, SEMIKRON datasheets are different with regards to the datasheet layout, data content and specifications for various generations of MOSFET modules and a variety of module designs. Since this data is to be standardised as part our product maintenance measures, the following information essentially refers to the latest datasheets issued in January 2010. Where applicable, different datasheet structures for the datasheets of older modules which are still being produced will be pointed out expressly. The basic datasheet layout is equivalent to that of IGBT modules introduced at the beginning of chapter 3.3.

Important data such as maximum ratings and characteristics valid for all different types of SEMIKRON power MOSFET modules are not included in the type-specific datasheets, but are part of the "Technical Explanations" on the respective product range.

3.4.1 Maximum ratings

In the datasheets, the maximum ratings are specified separately for each module component (or module function, such as forward conduction behaviour and negative conduction of MOSFET). All ratings refer to one switch, irrespective of the number of MOSFET chips per switch actually connected in parallel in the transistor module.

Absolute Maximum Ratings		T_s = 25 °C, unless otherwise specified	
Symbol	**Conditions**	**Values**	**Units**
MOSFET			
V_{DSS}		100	V
V_{GSS}		± 20	V
I_D	T_s = 25 (80) °C; 1)	80 (60)	A
I_{DM}	t_p < 1 ms; T_s = (80) °C; 1)	(120)	A
T_j		- 40 ... + 150	°C
Inverse diode			
I_F = - I_D	T_s = 25 (80) °C;	80 (60)	A
I_{FM} = - I_{DM}	t_p < 1 ms; T_s = (80) °C;	(120)	A
T_j		- 40 ... + 150	°C
T_{stg}		- 40 ... + 125	°C
T_{sol}	Terminals, 10 s	260	°C
V_{isol}	AC, 1 min (1s)	2500 / 3000	V

Figure 3.4.1 Datasheet excerpt: maximum ratings of a MOSFET module

3.4.1.1 Maximum forward ratings of power MOSFET

Drain-source voltage V_{DSS}

Maximum voltage between the drain and source terminals of the MOSFET chips with gate-source short-circuited; parameters: case temperature T_c = 25°C, heatsink temperature for modules without base plate T_s = 25°C.

Owing to the temperature dependency of the breakdown voltage, the maximum drain-source voltage decreases in proportion to the temperature. Irrespective of the load conditions, the sum of the collector-emitter supply voltage V_{DD} and the switching overvoltage $\Delta V_{DS} = L_\sigma \cdot di_D/dt$ must not exceed voltage V_{DSS} (L_σ: sum of the parasitic inductance in the commutation circuit), cf. chapter 5.1.

Gate-source voltage V_{GSS}

Maximum voltage between the gate and source terminals of the MOSFET chips; parameters: case temperature T_c = 25°C.

Continuous drain current I_D

Maximum permissible continuous direct current over the collector output at which the permissible chip temperature is reached. Parameter: case temperature T_c = 25°C / 80°C, heatsink temperature T_s = 25°C / 80°C for modules without base plate; for modules which can be soldered in PCBs (SEMITOP) also maximum PCB temperature at the output terminals; chip temperature $T_j = T_{j(max)}$

I_D for modules with base plate is determined from

$I_D^2 = P_{tot(max)}/R_{DS(on)}$ mit $P_{tot(max)} = (T_{j(max)} – T_c)/R_{th(j-c)}$,

and for modules without base plate from

$I_D^2 = P_{tot(max)}/R_{DS(on)}$ mit $P_{tot(max)} = (T_{j(max)} – T_s)/R_{th(j-s)}$.

Since I_D designates a static maximum value, it is not relevant to switching operation.

Peak value of a pulsed drain current I_{DM}

Peak value of current at the drain output during pulse operation; parameters: pulse duration t_p, case temperature T_c = 25°C or 80°C and pulse / break ratio.

Operating temperature range T_j; $T_{j(min)}$....$T_{j(max)}$

Permissible IGBT chip temperature range for IGBT module operation; the chip temperature should be kept at least 25 K below $T_{j(max)}$, especially for permanent load conditions.

3.4.1.2 Maximum ratings of the inverse diodes (power MOSFET ratings in reverse direction)

Inverse diode forward current (continuous drain current in reverse direction) $I_F = -I_D$

Maximum rated direct reverse current at drain output; maximum ratings and parameters are identical to those for forward direction.

Repetitive peak forward current of the inverse diode $I_{FM} = -I_{DM}$

Peak value of drain current during pulse operation; maximum ratings and parameters are identical to those in forward direction.

Operating temperature range T_j; $T_{j(min)}$....$T_{j(max)}$

Permissible IGBT chip temperature range for IGBT module operation; the chip temperature should be kept at least 25 K below $T_{j(max)}$, especially under permanent load. The maximum ratings and parameters correspond to those for forward direction.

3.4.1.3 Maximum module ratings

Storage temperature range T_{stg}; $T_{stg(min)}$....$T_{stg(max)}$

Temperature range within which the module may be stored or transported without being subject to electrical load.

Soldering temperature T_{sol} for the output terminals (for modules with soldered terminals)

Maximum temperature to which the output terminals may be exposed when soldered onto a PCB; parameter: exposure time; see assembly instructions in chapter 6.3.4

Insulation test voltage V_{isol}

Effective value of the permissible test voltage (50 Hz AC voltage) between the short-circuited terminals and insulated module base plate; parameter: test duration (1 min or 1 s); for details see chapter 5.1.1.2

3.4.2 Characteristics

In the datasheets, the characteristics are specified separately for each module component (or module function, such as forward conduction behaviour and negative conduction of MOSFET). All characteristics refer to one switch, irrespective of the number of power MOSFET chips actually paralleled per switch in the transistor module.

3.4.2.1 Power MOSFET characteristics

Characteristics		T_s = 25 °C, unless otherwise specified			
Symbol	**Conditions**	**min.**	**typ.**	**max.**	**Units**
MOSFET					
$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 5,6 mA	100			V
$V_{GS(th)}$	V_{GS} = V_{DS}; I_D = 5,6 mA	2,5	3,3		V
I_{DSS}	V_{GS} = 0 V; V_{DS} = V_{DSS}; T_j = 25 °C			100	µA
I_{GSS}	V_{GS} = ± 20V ;V_{DS} = 0 V			100	nA
$R_{DS(on)}$	I_D = 80 A; V_{GS} = 10 V; T_j = 25 °C			7,5	mΩ
$R_{DS(on)}$	I_D = 80 A; V_{GS} = 10 V; T_j = 125 °C			13,5	mΩ
C_{CHC}	per MOSFET				pF
C_{iss}	under following conditions:		9,1		nF
C_{oss}	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz		1,8		nF
C_{rss}			1,6		nF
L_{DS}					nH
$t_{d(on)}$	under following conditions:		300		ns
t_r	V_{DD} = 50 V; V_{GS} = 10 V; I_D = 50 A		150		ns
$t_{d(off)}$	R_G = 56 Ω		1600		ns
t_f			160		ns
$R_{th(j-s)}$	per MOSFET (per module)			1,1	K/W
Inverse diode					
V_{SD}	I_F = 50 A; V_{GS} = 0 V; T_j = 50 °C		0,9		V
I_{RRM}	under following conditions:		24		A
Q_{rr}	I_F = 50 A; T_{vj} = 25 °C; R_G = 56 Ω		0,9		µC
t_{rr}	V_R = 65 A; di/dt = 100 A/µs		70		ns
Free-wheeling diode					
V_F	I_F = A; V_{GS} = V				V
I_{RRM}	under following conditions:				A
Q_{rr}	I_F = A; T_{vj} = °C				µC
t_{rr}	V_r = A; di/dt = A/µs				ns
Mechanical data					
M1	mounting torque			2,5	Nm
w			20		g
Case	SEMITOP® 3		T 16		

Figure 3.4.2 Datasheet excerpt: power MOSFET characteristics

Drain-source breakdown voltage $V_{(BR)DSS}$

Breakdown voltage between drain and source with gate-source short-circuited (V_{GS} = 0 V); parameters: reverse drain current I_{DSS}, case temperature T_c = 25°C.

Gate-source threshold voltage $V_{GS(th)}$

Gate-source voltage above which considerable drain current will flow; parameter: drain-source voltage V_{DS} = V_{GS}, drain current I_D, case temperature T_c = 25°C.

Zero gate voltage drain current I_{DSS}

Reverse current between drain and source with gate-source short-circuited (V_{GS} = 0 V) and maximum drain-source voltage V_{DS}; parameter: chip temperature, e.g. T_j = 25°C and 125°C; I_{DSS} rises by a factor 3...6 at temperatures between 25°C and 125°C.

Gate-source leakage current I_{GSS}

Leakage current between gate and source with drain-source short-circuited (V_{DS} = 0) and at maximum gate-source voltage V_{GS}; parameter: gate-source voltage V_{GS} = ±20 V.

Drain-source turn-on resistance $R_{DS(on)}$

Quotient of changing drain-source voltage V_{DS} and drain current I_D in a fully gate-controlled MOSFET at a specified gate-source voltage V_{GS} and specified drain current I_D (i.e. at "rated current"); in this forward state V_{DS} is proportional to I_D, during large-signal behaviour the forward on-state voltage $V_{DS(on)} = R_{DS(on)} \cdot I_D$. Parameter: gate-source voltage V_{GS} = 20 V, drain current I_D (i.e. "rated current"), chip temperature T_j = 25°C and 125°C ($R_{DS(on)}$ is extremely dependent on the temperature!).

Capacitance chip-case (base plate) C_{CHC}

Small signal capacitance between MOSFET chip and base plate with gate-source short-circuited; parameters: drain-source direct voltage V_{DS}, measuring frequency f = 1 MHz, case temperature T_c = 25°C

Input capacitance C_{iss}, output capacitance C_{oss}, reverse transfer capacitance (Miller capacitance) C_{rss}

Small-signal capacitances defined in analogy to the IGBT low-signal capacitances; cf. chapter 3.3.2.

Parasitic drain-source inductance L_{DS}

Inductance between drain and source, cf. chapter 3.3.2; parameters: drain-source direct voltage V_{DS}, case temperature T_c = 25°C.

Switching times $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

In contrast to IGBT, the switching times indicated in the datasheets of power MOSFET are determined under less realistic conditions, using a measuring circuit under ohmic load, as shown in Figure 3.4.3. The definition of switching times refers to the gate-source voltage characteristics, cf. Figure 3.4.3b) and Figure 2.4.19 in chapter 2.4.3.2, as well as explanations concerning the physical background of current and voltage characteristics during switching. Parameters: supply voltage V_{DD}, continuous drain current I_D, gate control voltages V_{GG+}, V_{GG-} (or V_{GS}), external gate resistances R_{Gon}, R_{Goff}, rate of rise of drain current $+di_D/dt$ during turn-on or rate of fall of drain current $-di_D/dt$ during turn-off and chip temperature T_j (switching times and losses rising with junction temperature).

What must be taken into consideration is that, in practice, switching times, current and voltage characteristics, as well as switching losses are largely determined by internal and external capacitances, inductances and resistances in the gate and collector circuit. This means that ratings provided in the datasheet can often be taken as a rough guide only, meaning that additional measurements in the real application environment will inevitably have to be carried out to ensure safe layout of the circuitry.

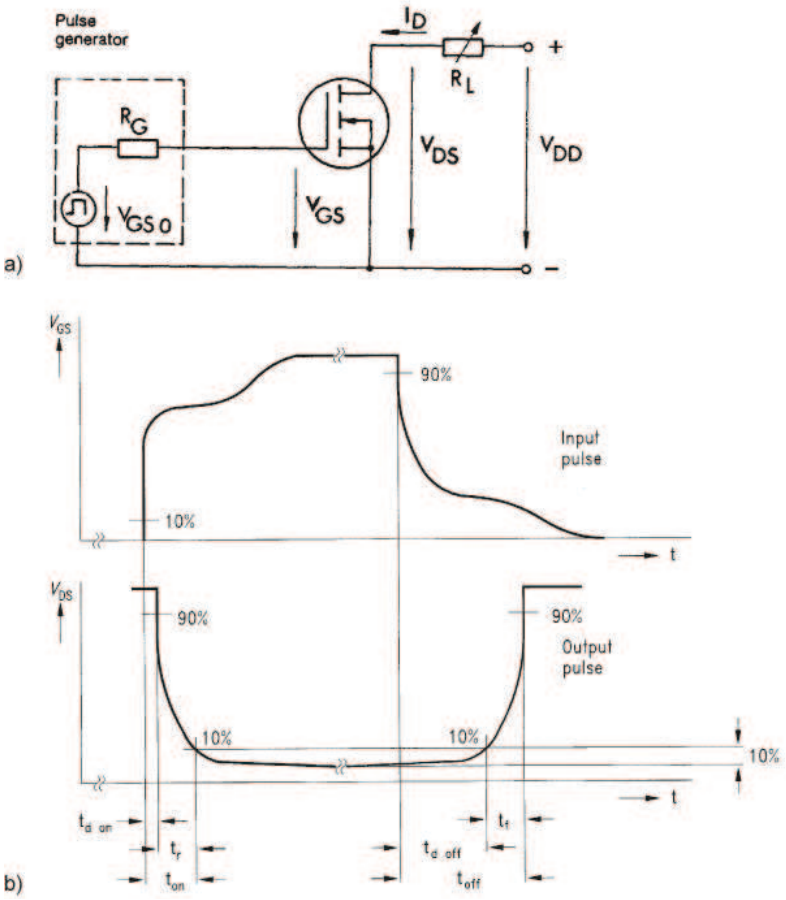


Figure 3.4.3 MOSFET switching times; a) Measuring circuit; b) Definition of MOSFET switching times under ohmic load

The **turn-on delay time $t_{d(on)}$** is defined as the time interval between the moment when the gate-source voltage v_{GS} has reached 10 % of its end value and the drain-source voltage V_{DS} has decreased to 90 % of the drain-source supply voltage V_{DD}. During the subsequent **rise time t_r** the drain-source voltage V_{DS} decreases from 90 % to 10 % of the drain-source supply voltage V_{DD}. The sum of **turn-on delay time $t_{d(on)}$** and **rise time t_r** is referred to as the **turn-on time t_{on}**. The **turn-off delay time $t_{d(off)}$** is defined as the time interval between the moment when the gate-source voltage v_{GS} has decreased to 90 % of its end value again and the drain-source voltage V_{DS} has risen to 10 % of the drain-source supply voltage V_{DD}.

The **fall time t_f** is defined as the time interval where the drain-source voltage V_{DS} rises from 10 % to 90 % of the drain-source supply voltage V_{DD}. The **turn-off time t_{off}** is defined as the sum of the turn-off delay time $t_{d(off)}$ and the fall time t_f.

Thermal resistances $R_{th(j-c)}$ / $R_{th(j-s)}$ per MOSFET and $R_{th(c-s)}$ per MOSFET module

Thermal resistances characterise the static heat transfer of a MOSFET switch within a module, irrespective of the number of chips connected in parallel. Usually, several MOSFET switches are integrated in one module. For this reason, the following explanations refer briefly to the module as a whole. Figure 3.3.10 introduces the thermal models for modules with base plate (case rated devices) and without base plate (heatsink rated devices). The power losses inside the module cause all of the chips to be heated to $T_j = T_a + P_V \cdot \Sigma R_{th}$.

$R_{th(j-c)}$ describes the passage of heat between the MOSFET of a switch (index j) and the module base plate (index c). In modules with base plate, $R_{th(c-s)}$ describes the passage of heat between module base plate (index c) and heatsink (index s). Since a separate determination of both resistances for modules without base plate (SEMITOP) is not possible, only the thermal resistance $R_{th(j-s)}$ between the chips of a switch and the heatsink is specified for each MOSFET switch.

$R_{th(j-c)}$ and $R_{th(j-s)}$ depend mainly on the chip area per switch and the heat transfer properties of the insulating DBC ceramic substrate. Furthermore, $R_{th(j-s)}$ is also determined by the thickness and properties of thermal layers between module and heatsink, as well as by the heatsink surface and the mounting torque of the fixing screws (cf. $R_{th(c-s)}$).

The temperature differences ΔT over the thermal resistances are calculated for constant power dissipation P_V in the MOSFET switches contained in the module (irrespective of the number of chips connected in parallel) as follows:

- Chip – base plate (module with base plate): $\Delta T_{(j-c)} = T_j - T_c = P_V \cdot R_{th(j-c)}$ per MOSFET
- Chip – heatsink (module with base plate): $\Delta T_{(c-s)} = T_c - T_s = \Sigma P_V \cdot R_{th(c-s)}$ per module
- Chip – heatsink (module without base plate): $\Delta T_{(j-s)} = T_j - T_s = P_V \cdot R_{th(j-s)}$ per MOSFET

3.4.2.2 Characteristics of inverse diodes (power MOSFET in reverse direction)

The forward and switching behaviour of the inverse diode is of importance every time the inverse diode is involved in commutation processes, e.g. when it is serves as a freewheeling diode in a bridge circuit. As explained in chapter 2.4, the load current is commutated in both directions between a switched MOSFET and the diode of the commutation circuit (freewheeling diode), which is the inverse diode of the second MOSFET at the same time.

Common parameters for the following characteristics: gate-source short-circuited (V_{GS} = 0 V), forward current of the inverse diode I_F, chip temperature T_j, as well as (for dynamic characteristics) repetitive reverse voltage of the inverse diode V_R (= drain-source supply voltage of the MOSFET V_{DD}), rate of fall of the diode forward current $-di_F/dt$ (rate of rise of the MOSFET gate current during turn-on) and the external gate resistance of the MOSFET R_G.

Forward voltage $V_F = V_{SD}$ of an inverse diode

Drain-source voltage drop in reverse direction measured at the terminals.

Peak reverse recovery current I_{RRM} of an inverse diode

Peak value of the reverse current after inverse diode switchover from forward (parameter I_F) to reverse load, cf. Figure 2.3.8 and related explanations.

Parameters for dynamic diode characteristics I_{RRM}, Q_{rr} and E_{rr}: supply voltage V_{DD}, diode forward current I_F, control voltage V_{GS}, rate of fall of the diode $-di_F/dt$ = rate of rise of drain current di_D/dt during turn-on, chip temperature T_j).

Recovered charge Q_{rr} of an inverse diode

Amount of charge flowing from the diode to the outer circuit after switchover from forward to reverse load; this charge has to be taken up by the MOSFET during turn-on. This depends on the forward current I_F prior to switching, the rate of fall of the decaying current $-di_F/dt$, and the chip temperature T_j; for details refer to Figure 2.3.8 and explanations in chapter 2.3. Q_{rr} is highly dependent on temperature (2 to 8-fold increase between 25°C and 150°C).

Reverse recovery time t_{rr}

The time it takes for the reverse current of the inverse diode to reach its stationary value after switchover from conductive to blocking state with $-di_F/dt$; for details see explanations on Figure 2.3.8 in chapter 2.3. t_{rr} is determined from Q_{rr} and I_{RRM} applying the following equation:

$t_{rr} \approx 2 \cdot Q_{rr}/I_{RRM}$

t_{rr} is highly dependent on temperature (initial value will almost double between 25°C and 150°C).

3.4.2.3 Mechanical module data

The following mechanical data is provided in the datasheets:

Mounting torque M_1, M_s of the fixing screws (minimum and maximum values),
Mounting torque M_2, M_t of the terminals (minimum and maximum values),
Module weight w.

3.4.3 Diagrams

Following the sequence of the datasheets, this chapter provides information on the diagrams in MOSFET module datasheets, which normally refer to one partial-MOSFET or freewheeling diode. Some diagrams presented here are not shown in all of the datasheets of all module families, as some are specific to certain module families. In cases where the diagram concerned is detailed in other chapters, this will be referred to.

[Fig. 1] Rated power dissipation P_D as a function of case temperature T_c

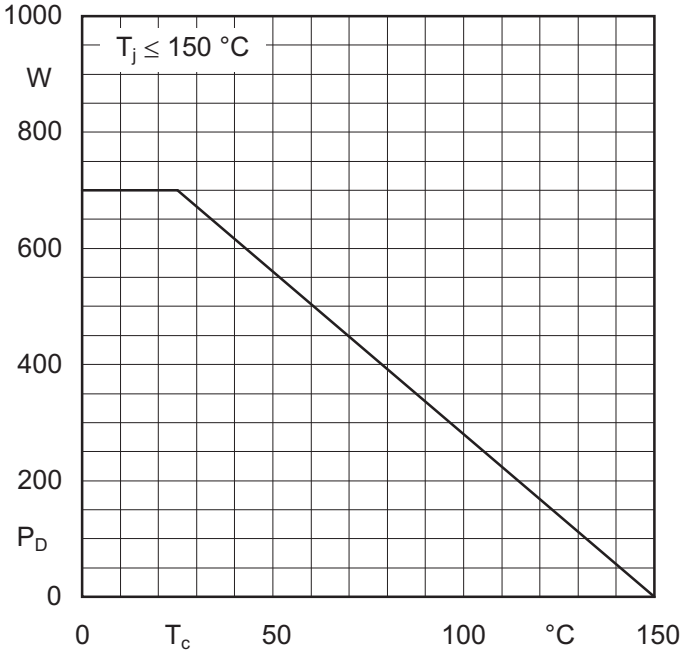


Figure 3.4.4 Maximum permissible power dissipation P_D versus case temperature T_c

Based on the maximum permissible rated power dissipation per MOSFET, $P_D(25°C) = (T_{j(max)} – 25K)/R_{th(j-c)}$ at $T_c = 25°C$, the function depicted in Figure 3.4.4 describes the power dissipation derating in dependency of the case temperature.

[Fig. 2] Maximum permissible safe operating area during single-pulse operation (SOA)

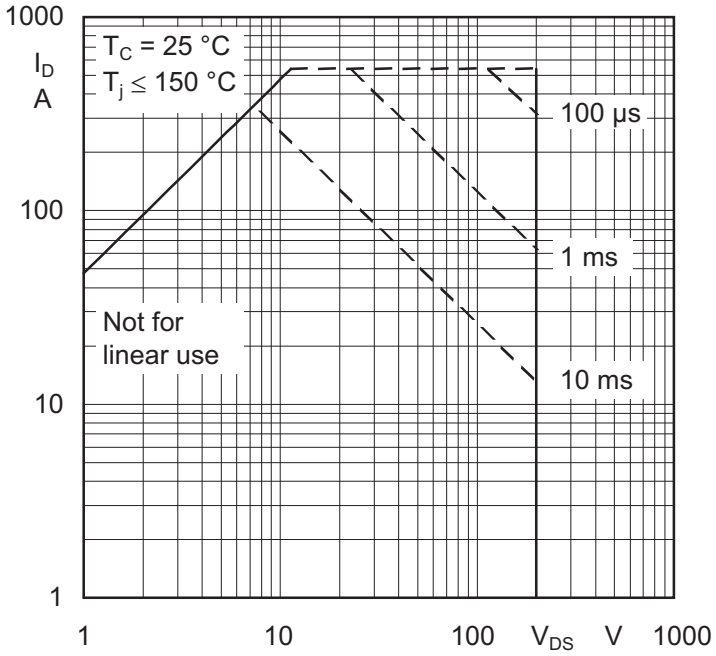


Figure 3.4.5 Safe operating area during single-pulse operation (SCSOA)

The MOSFET has to achieve an almost rectangular characteristic i= f(v) between V_{DD} and I_L during hard switching. The SOA (Safe Operating Area) diagrams indicate to what extent this may be realised during different operating states without risk of destruction. The diagrams and limitations provided in chapter 3.3.4 apply here by analogy. MOSFET modules may only touch the linear characteristic area during switching operation. Analogous operation over a longer period of time is not permitted, since asymmetries due to variation among the chips, as well as negative temperature coefficients of the threshold voltages might cause thermal instability.

[Fig. 3] Typical forward characteristics $I_D = f(V_{DS})$.

Figure 3.4.6 shows the output characteristic (typical values) based on the parameter V_{GS} (also see chapter 2.4.3).

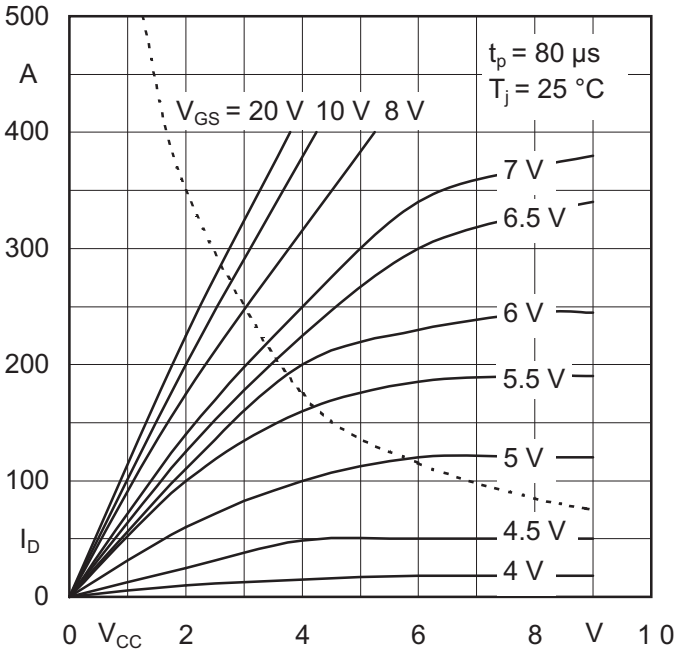


Figure 3.4.6 Typical forward characteristics $I_D = f(V_{DS})$

[Fig. 4] Typical transfer characteristic $I_D = f(V_{GS})$

The transfer characteristic depicted in Figure 3.4.7 describes the behaviour of the MOSFET in the active operating area at V_{DS} = 25 V (linear operation). The drain current is coupled with the gate-source voltage via $I_D = g_{fs} * (V_{GS} - V_{GS(th)})$.

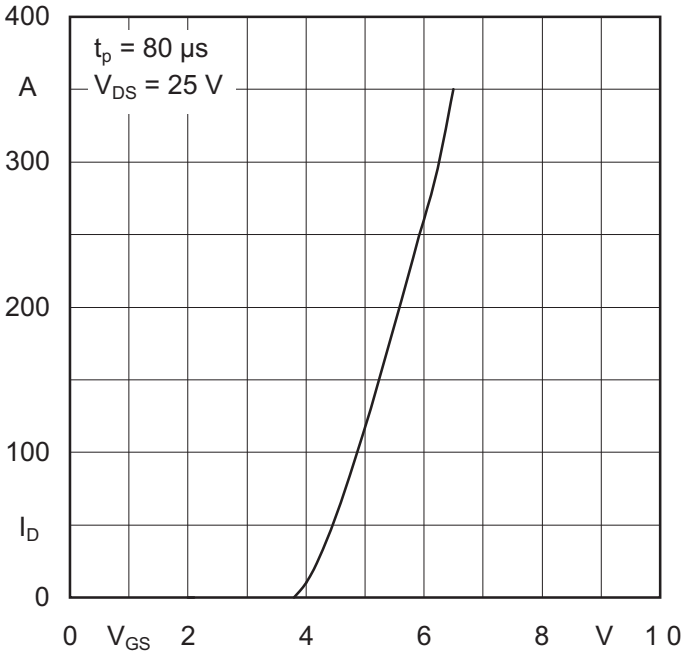


Figure 3.4.7 Typical transfer characteristic $I_D = f(V_{GS})$

[Fig. 5] Typical characteristic of ON-resistance versus chip temperature

Figure 3.4.8 shows the increasing ON-resistance $R_{DS(on)}$ versus temperature.

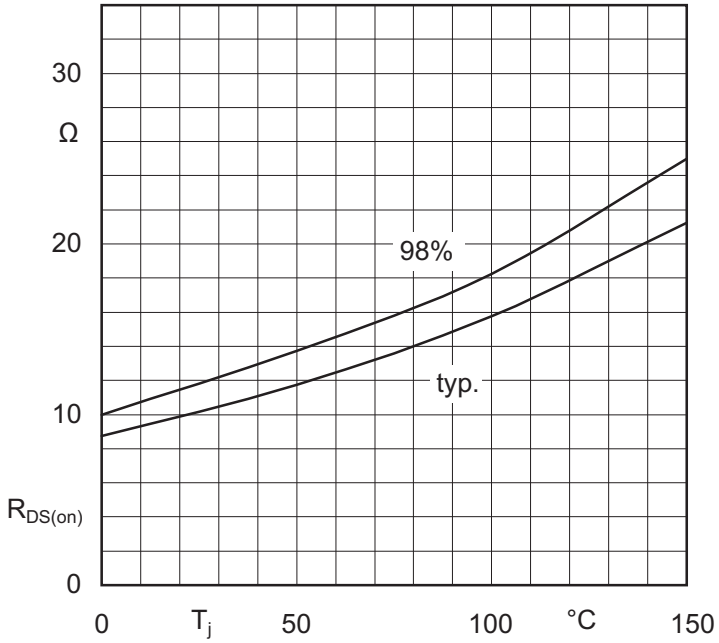


Figure 3.4.8 Typical characteristic of ON-resistance versus chip temperature

In the operating temperature range of 25...150°C, the $R_{DS(on)}$ roughly doubles. On the other hand, the positive temperature coefficient of the forward voltage offers advantages such as simplified paralleling capability and high ruggedness.

[Fig. 6] Drain current derating versus case temperature

Figure 3.4.9 shows the drain current derating (without additional switching losses) which is necessary if the case temperatures differ from the reference temperatures T_c= 25°C or 80°C indicated in the datasheet as a parameter for I_D. At temperatures above T_c = 25°C the relation is

$$I_D = \frac{T_{j(max)} - T_C}{R_{th(j-c)} \cdot V_{DS(on)}} = \sqrt{\frac{T_{j(max)} - T_C}{R_{th(j-c)} \cdot R_{DS(on)}}}$$

For case temperatures T_c < 25°C, the maximum rated drain current is limited to the datasheet rating for I_D.

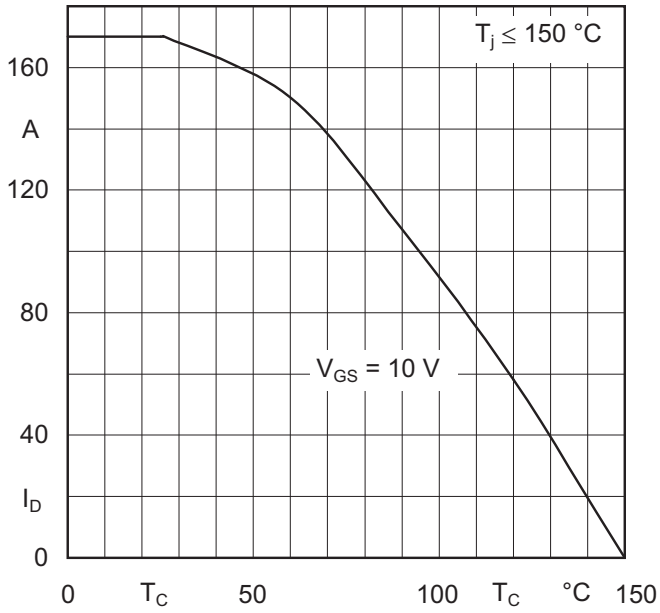


Figure 3.4.9 Drain current derating versus case temperature

[Fig. 7] Typical drain-source breakdown voltage versus temperature

As shown in Figure 3.4.10, the drain-source breakdown voltage $V_{(BR)DSS}$ of a MOSFET increases linear to the temperature. As the maximum rating indicated in the datasheets refers to T_j = 25°C, derating at low chip temperatures has to be accepted.

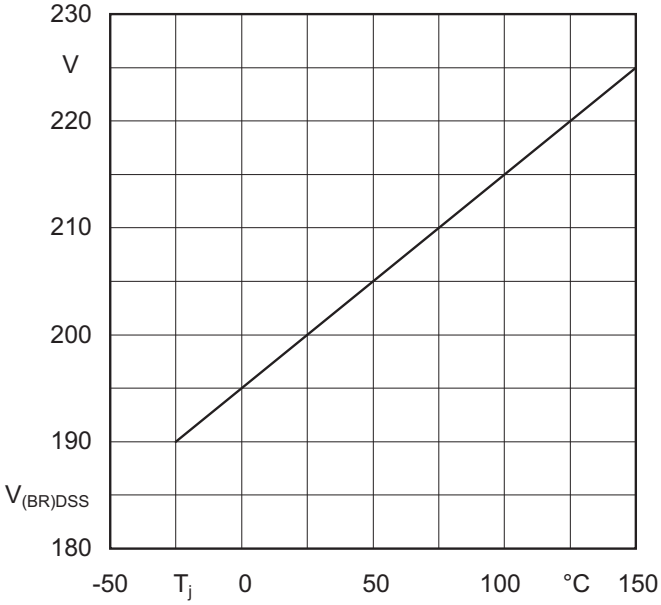


Figure 3.4.10 Typical drain-source breakdown voltage versus temperature

[Fig. 8] Derating of the permissible drain-source voltage versus rate of fall of the drain current

Overvoltages that occur at the internal module inductances (terminals, bond wires etc.) will increase if the turn-off time is shortened (rising $-i_{\Delta}/dt$), i.e. the drain-source supply voltage V_{DD} at which the MOSFET may switch decreases (also see chapter 5.1.1). This dependency is illustrated in Figure 3.4.11: $V_{DD} = f(-di_D/dt \approx I_D/t_f)$.

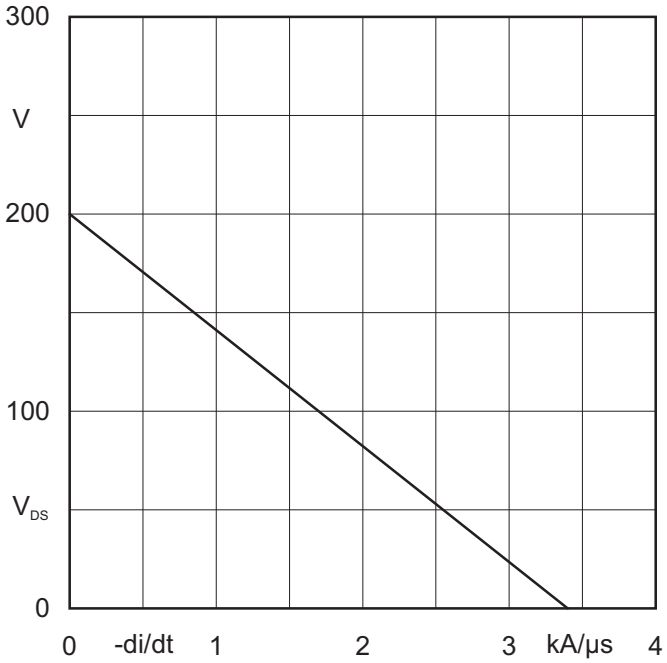


Figure 3.4.11 Drain-source voltage derating versus drain current rate of fall

[Fig. 9] Typical characteristic of the internal capacitances versus drain-source voltage

The causes and effects of internal capacitances in power MOSFET have been thoroughly discussed in chapter 2.4. The ratings given in the characteristics (also see parameters/ measurement conditions) and in Figure 3.4.12 show the dependency of the low-signal capacitances of a turned off MOSFET on the drain-source voltage. These are only of minor importance for the dimensioning of power switches, which should rather to be done on the basis of the gate charge diagram depicted in Figure 3.4.13.

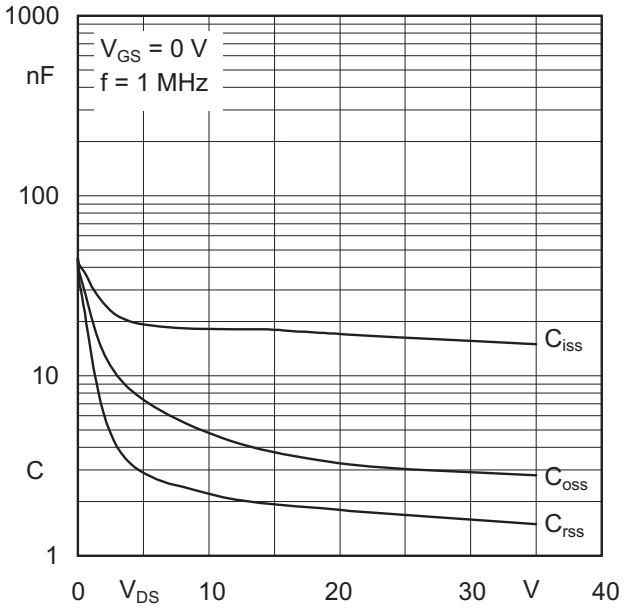


Figure 3.4.12 Typical characteristic of internal capacitances as a function of drain-source voltage

[Fig. 10] Typical gate charge characteristic $V_{GS} = f(Q_G)$

Figure 3.4.13 shows the characteristic of the MOSFET gate-source voltage V_{GS} as a function of the gate charge Q_G with the parameter drain-source supply voltage V_{DS}. The gate charge characteristic illustrates the course of V_{GS} between off-state where V_{GS} = 0 V and on-state at maximum V_{GS}. This diagram may be used to determine the gate charge load Q_G required to transduce the MOSFET from off-state to saturation.

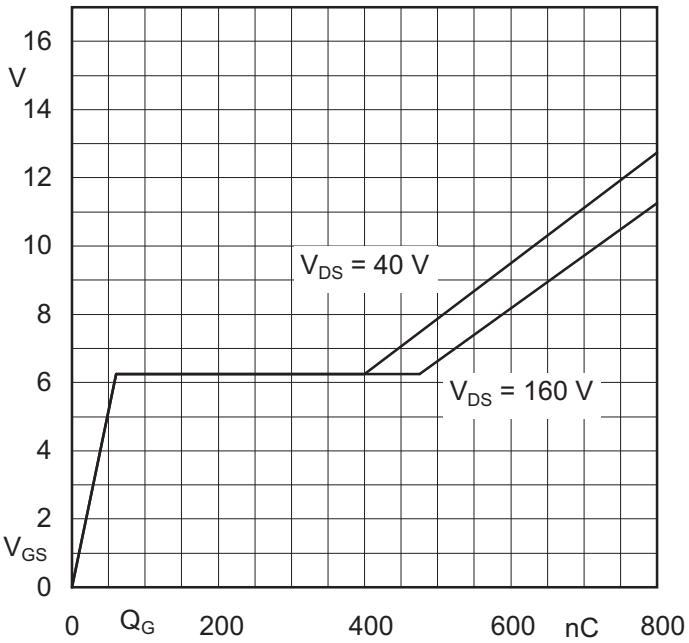


Figure 3.4.13 Typical gate charge characteristic $V_{GS} = f(Q_G)$

[Fig. 14] Gate-source threshold voltage versus temperature

The diagram in Figure 3.4.14 shows three curves with typical and limit values characterising the relationship between gate-source threshold voltage $V_{GS(th)}$ and MOSFET chip temperature T_j.

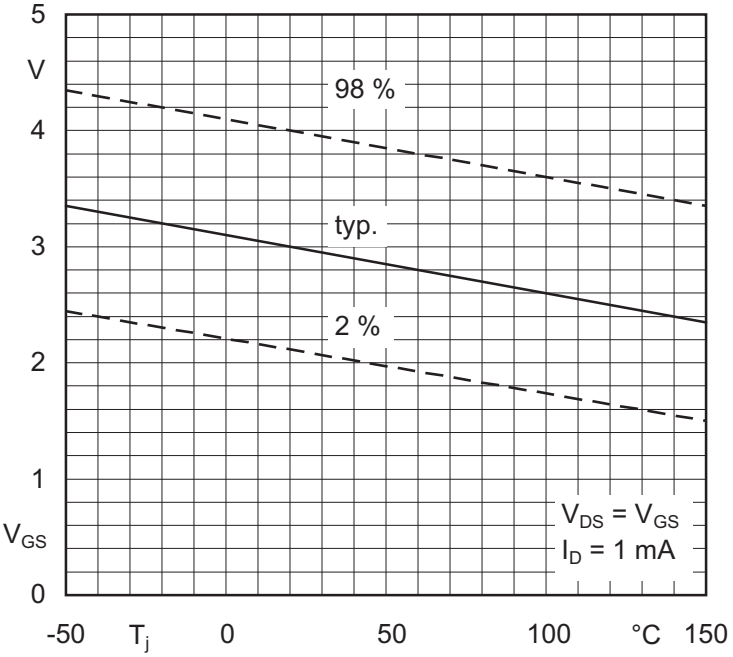


Figure 3.4.14 Gate-source threshold voltage versus temperature

$V_{GS(th)}$ will decrease linear to the increase in T_j. The temperature coefficient of the threshold voltage amounts to about –10 mV/K within the -50...+150°C temperature range. One of the reasons for this is that power MOSFET modules (with MOSFET consisting of paralleled chips with a number

of single cells) must not be operated in the active operating area, since the negative temperature coefficient of $V_{GS(th)}$ will counteract the symmetrical current distribution among the chips.

3.5 Supplementary information on CI, CB and CIB power modules

CI (**C**onverter **I**nverter) and CIB (**C**onverter **I**nverter **B**rake) structures are high-integration-level, user-friendly topologies that can be found in the MiniSKiiP and SEMITOP product families. Such modules feature a single-phase or three-phase uncontrolled or half-controlled bridge rectifier (**C**), a three-phase inverter (**I**) and - in the CIB version - an IGBT with freewheeling diode which serves as a brake chopper (**B**). In CB power modules, a third topology that is used in the MiniSKiiP, SEMITOP and SEMIPONT product lines, a single-phase or three-phase rectifier (**C**) and a brake chopper (**B**) are integrated. Figure 3.5.1 shows examples of these topologies.

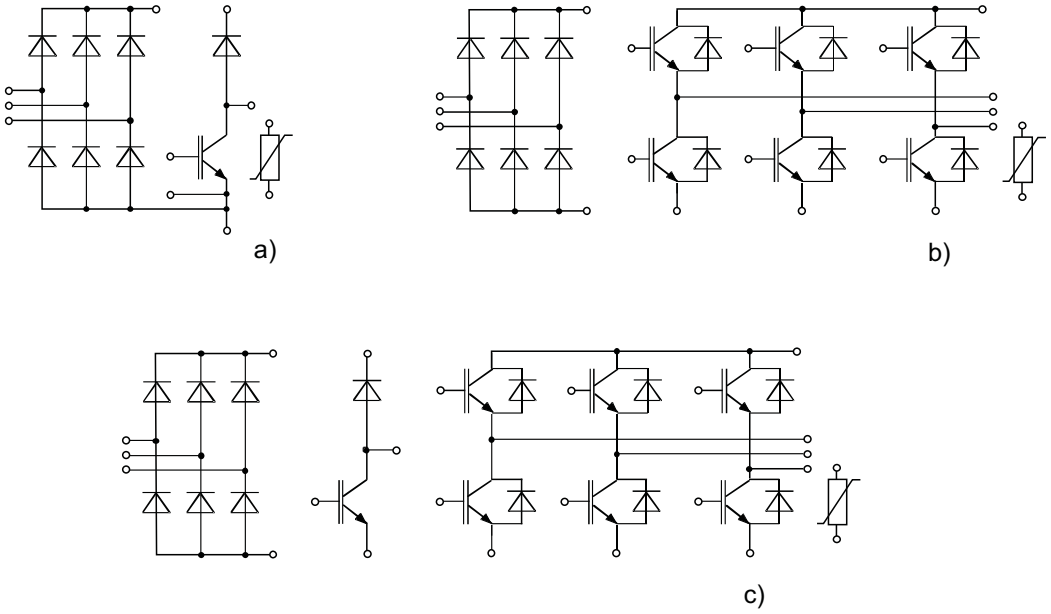


Figure 3.5.1 Examples of power module topologies a) CB, b) CI, c) CIB

Within each topology, the modules differ with respect to the circuit layout and the integration of temperature and current sensors. Closely related to this is a range of power modules with PFC (**P**ower **F**actor **C**orrection) boost converters with diodes with opposite polarity. Since such modules require high switching frequencies, the brake chopper IGBT is often replaced by a MOSFET. Table 3.5.1 describes the type designation system of SEMIKRON CI, CIB and CB power modules.

Designation	**Converter**		**Inverter**	**Brake**	**Temperature sensor**
	1-p	3-p			
MiniSKiiP					
SKiiPxxNABxxx		x	x	x	x
SKiiPxxNEBxxx	x		x	x	x
SKiiPxxNECxxx	x		x		x
SKiiPxxAHBxxx		x*		x	x
SKiiPxxANBxxx		x		x	x
SEMITOP					
SKxxBGDxxx	x		x		
SKxxBGDxxxT	x		x		
SKxxDGDxxxT		x	x		x

Designation	Converter		Inverter		Brake	Temperature sensor
	1-p	3-p				
SKxxDGDLxxxT		x	x		x	x
SKxxDGLxxx	x	x		x		
SKxxDHLxxx	x*			x		
SEMIPONT						
SKDxxx/xxLxx		x			x	x
SKDHxxx/xxLxx	x*					

* half-controlled rectifier bridge

Table 3.5.1 Type designation system of SEMIKRON CI, CIB and CB power modules

The datasheet ratings for inverter and brake chopper IGBT and diodes, the temperature sensor and the properties of CI, CIB and CB power modules correspond to those for IGBT modules provided in chapter 3.3. The same freewheeling diodes are used for inverters and brake choppers, whereas the chopper IGBT of some CIB modules may be smaller than the inverter IGBT. In such cases, the datasheet of another module type may be referred to in the relevant datasheet (Figure 3.5.2).

Absolute Maximum Ratings Ts = 25 °C, unless otherwise specified

Symbol	Conditions	Values	Units
IGBT - Inverter.For IGBT chopper maximum ratings, please refer to SK35DGDL12T4T			
V_{CES}		1200	V
I_C	T_s = 25 (70) °C	75 (60)	A
I_{CRM}	I_{CRM}= 3 x I_{Cnom}, t_p = 1 ms	150	A
V_{GES}		± 20	V
T_j		-40 ... +175	°C
Diode - Inverter,Chopper			
I_F	T_s = 25 (70) °C	60 (45)	A
I_{FRM}	I_{FRM} = 2xI_{Fnom}, t_p = 1 ms	150	A
T_j		-40 ... +150	°C
Rectifier			
V_{RRM}		1600	V
I_F	T_s = 70 °C	61	A
I_{FSM} / I_{TSM}	t_p = 10 ms , sin 180 ° ,T_j = 25 °C	700	A
I^2t	t_p = 10 ms , sin 180 ° ,T_j = 25 °C	2400	A^2s
T_j		-40 ... +175	°C
T_{sol}	Terminals, 10 s	260	°C
T_{stg}		-40 ... +125	°C
V_{isol}	AC, 1 min. / 1 s	2500 / 3000	V

Characteristics Ts = 25 °C, unless otherwise specified

Symbol	Conditions	min.	typ.	max.	Units
IGBT - Inverter.For IGBT chopper electrical characteristics, please refer to SK35DGDL12T4T					
V_{CEsat}	I_C = 50 A, T_j = 25 (150) °C		1,85 (2,2)	2,05 (2,45)	V
$V_{GE(th)}$	V_{GE} = V_{CE}, I_C = 1,7 mA	5	5,8	6,5	V
$V_{CE(TO)}$	T_j = 25 °C (150) °C		1,1 (1)	1,3 (1,2)	V
r_T	T_j = 25 °C (150) °C		15 (24)		mΩ
C_{ies}	V_{CE} = 25 V_{GE} = 0 V, f = 1 MHz		2,77		nF
C_{oes}	V_{CE} = 25 V_{GE} = 0 V, f = 1 MHz		0,2		nF
C_{res}	V_{CE} = 25 V_{GE} = 0 V, f = 1 MHz		0,16		nF
$R_{th(j-s)}$	per IGBT		0,65		K/W
$t_{d(on)}$	under following conditions		63		ns
t_r	V_{CC} = 600 V, V_{GE} = ± 15 V		65		ns
$t_{d(off)}$	I_C = 50 A, T_j = 150 °C		521		ns
t_f	R_{Gon} = R_{Goff} = 32 Ω		80		ns
E_{on}	inductive load		8,3		mJ
E_{off}			5		mJ
Diode - Inverter,Chopper					
V_F = V_{EC}	I_F = 50 A, T_j = 25(150) °C		2,22 (2,18)	2,54 (2,5)	V
$V_{(TO)}$	T_j = 25 °C (150) °C		1,3 (0,9)	1,5 (1,1)	V
r_T	T_j = 25 °C (150) °C		18,4 (25,6)	20,8 (28)	mΩ
$R_{th(j-s)}$	per diode		0,97		K/W
I_{RRM}	under following conditions		30		A
Q_{rr}	I_F = 50 A, V_R = 300 V		7,2		µC
E_{rr}	V_{GE} = 0 V, T_j = 150 °C		2,15		mJ
	$di_{F/dt}$ = 920 A/µs				
Diode - Rectifier					
V_F	I_F = 50 A, T_j = 25(150) °C		1,1		V
$V_{(TO)}$	T_j = 150 °C		0,8		V
r_T	T_j = 150 °C		6		mΩ
$R_{th(j-s)}$	per diode		0,9		K/W
Temperatur sensor					
R_{ts}	5 %, T_r = 25 (100) °C		5000(493)		Ω
Mechanical data					
w			60		g
M_s	Mounting torque		3,5		Nm

Figure 3.5.2 Datasheet excerpt with maximum ratings and characteristics of a SK50DGDL12T4 CIB module

The properties of rectifier diodes or thyristors are also given in the datasheet tables and diagrams. Explanations on the respective maximum ratings, characteristics and diagrams are included in the chapters 3.1...3.4.

3.6 Supplementary information on IPMs

In addition to the power semiconductors, IPMs (**I**ntelligent **P**ower **M**odules) also feature an integrated driver stage (complete or at least most of the driver circuit) with protective functions and sensors (MiniSKiiP IPM). SKiiP IPMs for high-power applications also include a cooling system, i.e. IGBT module and driver are joined in one unit which is mounted onto a heatsink. For this reason, IPM datasheets have additional data that is not included in other power module datasheets; this is because users do not have access to different parameters.

3.6.1 SKiiP

High-power SKiiP IPMs are available as phase modules, H-bridge modules, inverter modules and brake chopper inverter modules. Figure 3.6.1 shows the principle layout of a SKiiP IPM, while Figure 3.6.2 shows a block diagram of a phase with driver and protective functions.

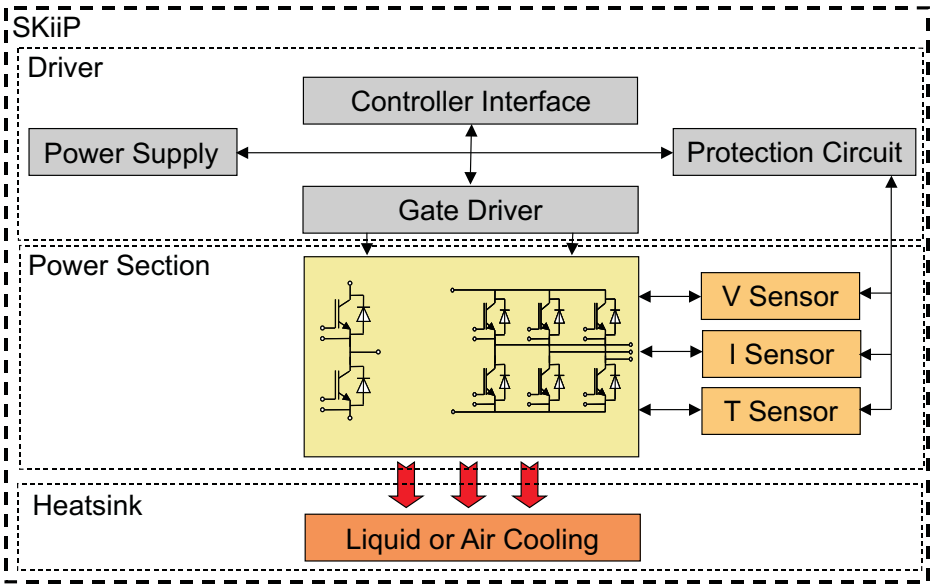


Figure 3.6.1 Principle layout of a SKiiP IPM (left: "GB" topology, right: "GD" topology)

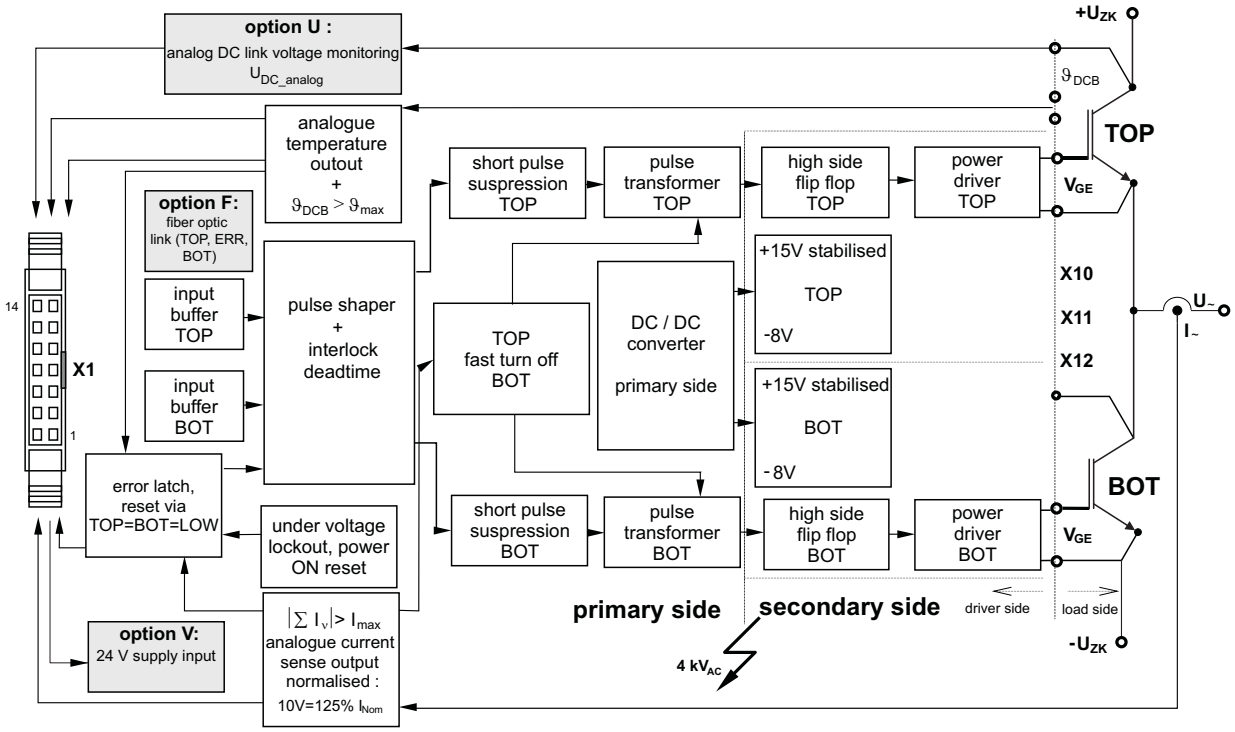
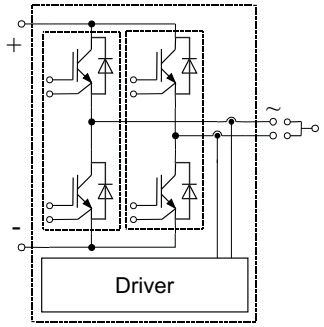


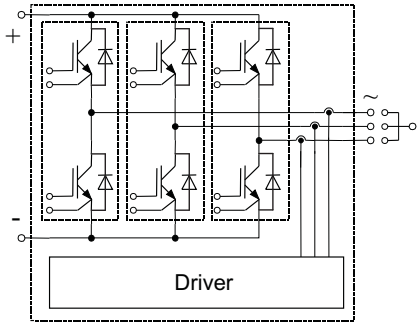
Figure 3.6.2 SKiiP phase block diagram with driver and protection circuitry

Three SKiiP generations are available at present: SKiiP2 with NPT-IGBT, SKiiP3 with Trench IGBT3 and SKiiP4 with Trench IGBT4. All SKiiP modules contain 2 to 4 (for SKiiP4 even 6) identical half bridges ("folds") mounted in a line on a heatsink with IGBT and diodes for either 1200 V or 1700 V reverse voltage. Figure 3.6.3 shows the range of circuit topologies: "GB" (half bridge), "GH" (2-phase H-bridge), "GD" (3-phase inverter) and "GDL" (3-phase inverter with brake chopper).

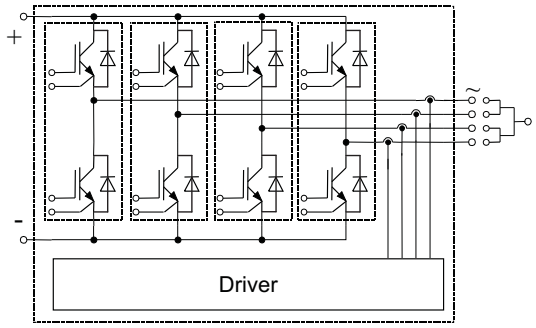
SKiiP: 2-fold "GB" (Case S2; S23)



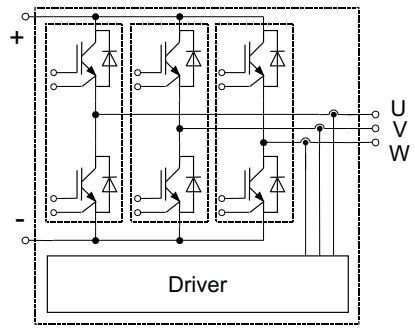
SKiiP: 3-fold "GB" (Case S3; S33)



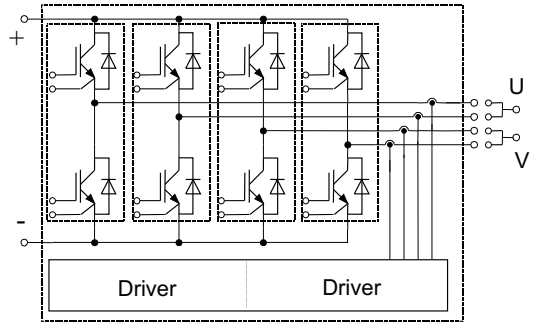
SKiiP: 4-fold "GB" (Case S4; S43)



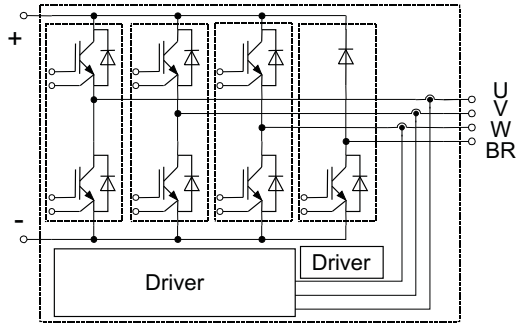
SKiiP: 3-fold "GD" (Case S3; S33)



only SKiiP2: 4-fold "GH" (Case S5GH)



only SKiiP2: 4-fold "GDL" (Case S5GDL)



only SKiiP4: 6-fold "GB"

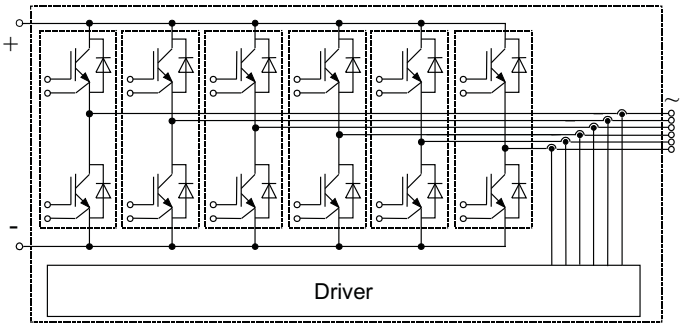


Figure 3.6.3 SKiiP topologies

Although the half bridges are controlled by a common driver, each half bridge is equipped with separate power terminals (DC+, AC, DC-) for connection at the customer's site (see example in Figure 3.6.4).

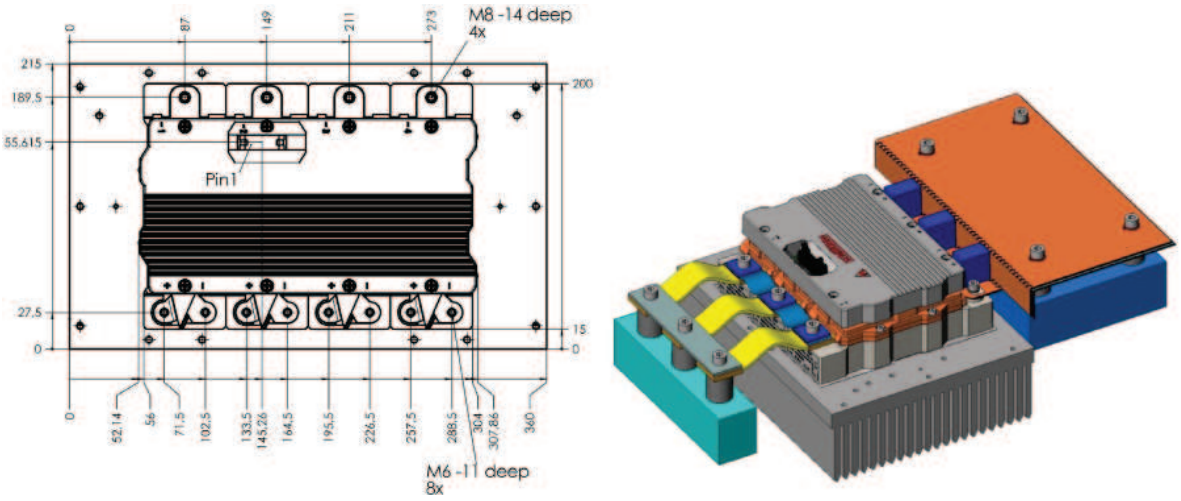


Figure 3.6.4 Power terminals of a SKiiP3

To guarantee optimal performance of SKiiP modules, the "Technical Explanations" provided for all SKiiP modules under www.semikron.com must be adhered to in addition to the type-specific data in the datasheets. Figure 3.6.5 gives an example of the basic datasheet layout of SKiiP modules.

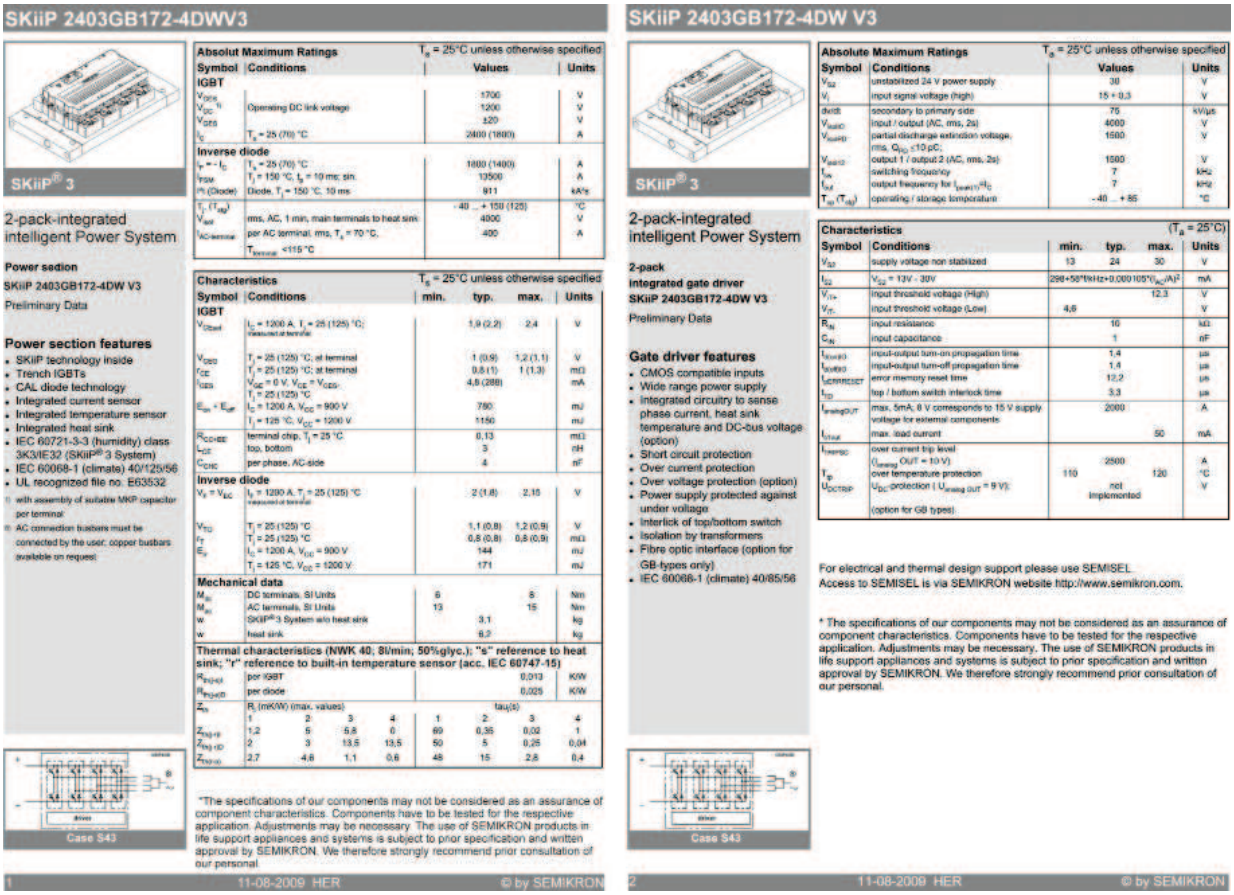


Figure 3.6.5 Datasheet layout for SKiiP modules

Unlike the datasheets for conventional power modules, SKiiP datasheets do not contain diagrams. In addition to the designation and a photo of the module, page 1 contains a description of the power section, as well as the respective maximum ratings and characteristics in the form of tables. The characteristics are divided into minimum, typical and maximum values. General information on the chip technology used and the integrated components is given in the shaded area to the left

of the maximum ratings and characteristics. Furthermore, this section provides information on climate classes, UL listing, explanations on footnotes, and a circuit diagram of the SKiiP module. The datasheet date of issue is given on all pages in the shaded footer. Page 2 features the maximum ratings and characteristics of the driver circuit. The greyed-out section provides additional driver properties and possible options.

3.6.1.1 Maximum ratings of the power section

In SKiiP datasheets, the maximum ratings are specified separately for the power section and the driver. All ratings for IGBT and diodes refer to one switch (arm), irrespective of the number of paralleled IGBT or diode chips per switch (arm) in the transistor module. The maximum ratings indicated in chapter 3.3 apply to IGBT and diodes.

DC link supply voltage V_{cc}

Parameter: heatsink temperature T_s = 25°C; maximum DC supply voltage applied between the DC terminals in a SKiiP module. This maximum rating will be applicable provided that the DC terminals are connected to adequate high-frequency (MKP) snubber capacitors (for selection refer to "Technical Explanations" and [AN1]).

If the DC and AC busbar system has a sufficiently minimal low-inductance design, the SKiiP module will be able to turn off short-circuits within the rated DC supply voltage range without that V_{CES} is exceeded across the chips. Information on the key busbar system properties and design are also included in the Technical Explanations and the application notes retrievable under www.semikron.com. V_{CC} may be exceeded briefly only and up to a maximum value of V_{CES} even for blocked IGBT.

RMS on-state current $I_{AC\ terminal}$, $I_{t(RMS)}$

Maximum current load applied to the power terminals of a half-bridge (fold) $I_{AC\text{-}terminal}$, which corresponds to $I_{t(RMS)}$ of an IGBT module (see chapter 3.3.1); parameter: heatsink temperature T_s = 70°C. Since the terminal temperature affects the operating temperature of the SKiiP driver, the maximum terminal temperature $T_{terminal}$ (< 115°C) is also given as a parameter.

3.6.1.2 Maximum ratings of a SKiiP driver

Absolute Maximum Ratings		T_a = 25°C unless otherwise specified	
Symbol	**Conditions**	**Values**	**Units**
V_{S2}	unstabilized 24 V power supply	30	V
V_i	input signal voltage (high)	15 + 0,3	V
dv/dt	secondary to primary side	75	kV/µs
V_{isolIO}	input / output (AC, rms, 2s)	4000	V
V_{isolPD}	partial discharge extinction voltage, rms, $Q_{PD} \leq$10 pC;	1500	V
V_{isol12}	output 1 / output 2 (AC, rms, 2s)	1500	V
f_{sw}	switching frequency	7	kHz
f_{out}	output frequency for $I_{peak(1)}=I_C$	7	kHz
T_{op} (T_{stg})	operating / storage temperature	- 40 ... + 85	°C

Figure 3.6.6 Datasheet excerpt: maximum ratings of a SKiiP driver

Driver supply voltage V_{s2}

Absolute maximum unstabilised supply voltage of the SKiiP driver.

Input signal voltage (HIGH) V_i

The maximum input signal voltage is derived from the high-level specification of the driver logic used to form the input signal.

Rate of rise of voltage on the secondary side dv/dt

Maximum rate of rise of voltage on the secondary side (power side) during IGBT switching under which the driver can still operate uninhibited.

Insulation test voltage V_{isolIO}

Effective value of the permissible test voltage (50 Hz AC voltage) between the short-circuited driver input and output terminals; parameter: test duration, e.g. t = 2 s.

Partial discharge extinction voltage V_{isolPD}

Effective value of the partial discharge extinction voltage (50 Hz AC voltage) between the short-circuited driver input and output terminals; parameter: maximum bpartial discharge $Q_{PD} \leq 10$ pC.

Insulation test voltage V_{isol12}

Effective value of the permissible test voltage (50 Hz AC voltage) between the BOT and TOP driver output terminals; parameter: test duration, e.g. t = 2 s.

Switching frequency f_{sw}

Maximum permissible PWM frequency limited by the maximum average output current $I_{G(AV)}$ of the driver supply voltage or driver power dissipation. Parameter: ambient temperature (datasheet rating at T_a = 25°C), derating at higher ambient temperatures as indicated in the "Technical Explanations" (Figure 3.6.7).

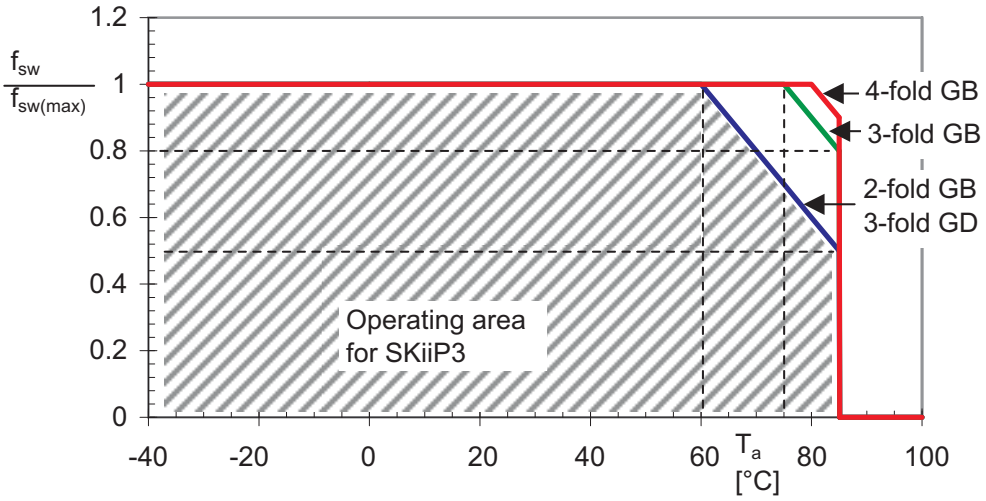


Figure 3.6.7 Derating of the maximum permissible switching frequency of a SKiiP3 at T_a > 25°C

Operating temperature range T_{op} and storage temperature range T_{stg}

See chapters 3.3.1 and 6.2; the maximum permissible operating and storage temperature of the driver is indicated for 85°C and is thus lower than the respective maximum rating T_{jmax} of the SKiiP power section.

Fundamental frequency of the output current f_{out}

Maximum permissible fundamental frequency of the output current limited by the properties of the integrated SKiiP current sensors and their evaluation electronics.

This rating is applicable to the pulse frequency f_{sw} of a SKiiP3 with PWM, provided that the amplitude $I_{peak(1)}$ of the current sensor's first harmonic does not exceed the rated current I_C. The amplitude for a rectangular signal may be calculated as follows:

$$I_{peak(1)} = \frac{\pi}{\sqrt{3} \cdot \sqrt{2}} \cdot I_{rms}$$

In addition, it has to be taken into account that $I_{AC\ terminal}$ is limited to 400 A RMS per half-bridge (fold) and that the maximum permissible collector current I_C is temperature-dependent. Furthermore, the output current of the SKiiP current sensor is limited with respect to its rate of rise di/dt (cf. Table 3.6.1).

SKiiP type	di/dt [A/µs] per AC terminal	di/dt [A/µs] for connected AC terminals
GD	150	----
2-fold	150	300
3-fold	150	450
4-fold	150	600

Table 3.6.1 Maximum permissible di/dt of SKiiP3

Other than with SKiiP3, the output frequency of the former SKiiP2 product series is restricted to $f_{out} \leq 1$ kHz, because the current sensors used are not capable of managing higher frequencies.

3.6.1.3 Characteristics of the SKiiP power section

The characteristics of the power section and the driver are also specified separately. Essentially, SKiiP datasheets correspond to those of IGBT modules with respect to their content and tabular layout, although in the SKiiP datasheets some parameters which apply to sections not accessible to the user are omitted, whereas other additional system-specific parameters are included.

Characteristics		T_s = 25°C unless otherwise specified			
Symbol	Conditions	min.	typ.	max.	Units
IGBT					
V_{CEsat}	I_C = 1200 A, T_j = 25 (125) °C; measured at terminal		1,9 (2,2)	2,4	V
V_{CEO}	T_j = 25 (125) °C; at terminal		1 (0,9)	1,2 (1,1)	V
r_{CE}	T_j = 25 (125) °C; at terminal		0,8 (1)	1 (1,3)	mΩ
I_{CES}	V_{GE} = 0 V, V_{CE} = V_{CES}, T_j = 25 (125) °C		4,8 (288)		mA
E_{on} + E_{off}	I_C = 1200 A, V_{CC} = 900 V		780		mJ
	T_j = 125 °C, V_{CC} = 1200 V		1150		mJ
$R_{CC+EE'}$	terminal chip, T_j = 25 °C		0,13		mΩ
L_{CE}	top, bottom		3		nH
C_{CHC}	per phase, AC-side		4		nF
Inverse diode					
V_F = V_{EC}	I_F = 1200 A, T_j = 25 (125) °C measured at terminal		2 (1,8)	2,15	V
V_{TO}	T_j = 25 (125) °C		1,1 (0,8)	1,2 (0,9)	V
r_T	T_j = 25 (125) °C		0,8 (0,8)	0,8 (0,9)	mΩ
E_{rr}	I_C = 1200 A, V_{CC} = 900 V		144		mJ
	T_j = 125 °C, V_{CC} = 1200 V		171		mJ
Mechanical data					
M_{dc}	DC terminals, SI Units	6		8	Nm
M_{ac}	AC terminals, SI Units	13		15	Nm
w	SKiiP® 3 System w/o heat sink		3,1		kg
w	heat sink		6,2		kg
Thermal characteristics (NWK 40; 8l/min; 50%glyc.); "s" reference to heat sink; "r" reference to built-in temperature sensor (acc. IEC 60747-15)					
$R_{th(j-s)I}$	per IGBT			0,013	K/W
$R_{th(j-s)D}$	per diode			0,025	K/W
Z_{th}	R_i (mK/W) (max. values)			tau_i(s)	
	1 2 3 4		1 2 3 4		
$Z_{th(j-r)I}$	1,2 5 5,8 0		69 0,35 0,02 1		
$Z_{th(j-r)D}$	2 3 13,5 13,5		50 5 0,25 0,04		
$Z_{th(r-a)}$	2,7 4,6 1,1 0,6		48 15 2,8 0,4		

Figure 3.6.8 Datasheet excerpt: SKiiP characteristics

Collector-emitter saturation voltage $V_{CE(sat)}$

cf. chapter 3.3.2.1

The rating refers to the saturation voltage measured at the power terminals of a SKiiP module, i.e. voltage drops across the internal module resistances $R_{CC'+EE'}$ (bond wires, terminals, …) are also included in $V_{CE(sat)}$. Parameter: I_C, T_j = 25°C/125°C.

Collector-emitter threshold voltage V_{CE0} and on-state slope resistance r_{CE} of the forward characteristic approximation

cf. chapter 3.3.2

The rating refers to the saturation voltage measured at the power terminals of a SKiiP module, i.e. voltage drops across the internal module resistances $R_{CC'+EE'}$ are included. Parameter: T_j = 25°C/125°C.

Capacitance between SKiiP and heatsink C_{CHC}

Capacitance between a SKiiP phase and the heatsink, measured between AC output and heatsink potential; parameter: case temperature T_c = 25°C.

Forward voltage $V_F = V_{EC}$ of an inverse diode

Collector-emitter voltage in reverse direction; see chapter 3.3.2

Mechanical data M_{dc}, M_{ac}, w

M_{dc}: Mounting torque of the DC terminals (minimum and maximum values)
M_{ac}: Mounting torque of the AC terminals (minimum and maximum values)
w: Weight of the SKiiP without heatsink and weight of SEMIKRON standard heatsink

Thermal impedances $Z_{th(j-r)I}$ per IGBT and $Z_{th(j-r)D}$ per inverse diode and $Z_{th(r-a)}$

The thermal impedances in SKiiP datasheets are indicated numerically as the parameters R_i and τ_i of a 4-time-constant model (cf. chapter 3.3.2). The integrated temperature sensor "r" is defined as the reference point for internal temperatures and heat flow in the SKiiP module. The sensor temperature lies between chip temperature and heatsink temperature (Figure 3.6.9). $Z_{th(j-r)I}$ and $Z_{th(j-r)D}$ designate the thermal impedances between IGBT or diode chips and the reference point (temperature sensor), $Z_{th(r-a)}$ describes the thermal impedance between temperature sensor and coolant.

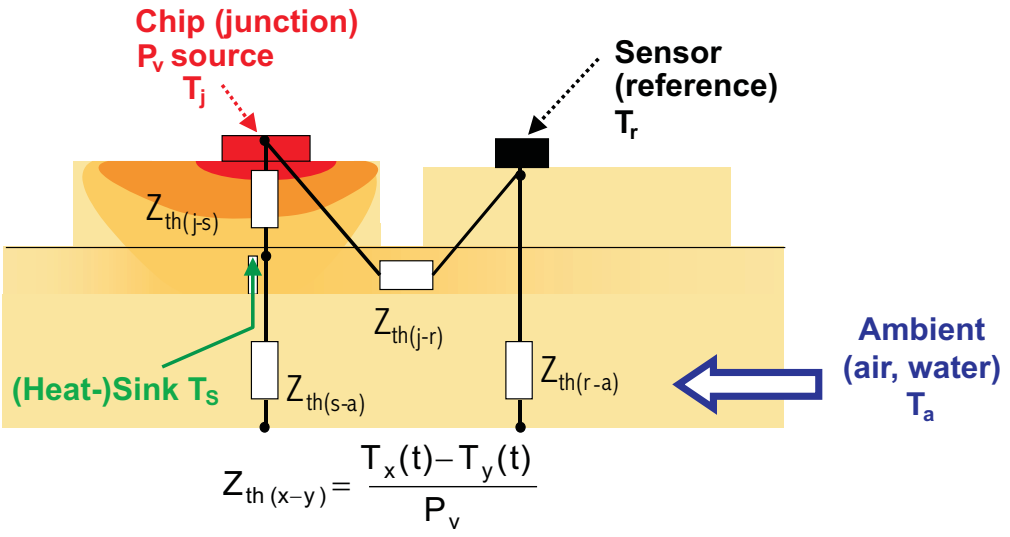


Figure 3.6.9 Thermal model of a SKiiP with temperature sensor

3.6.1.4 SKiiP driver characteristics

Characteristics					(T_a = 25°C)
Symbol	**Conditions**	**min.**	**typ.**	**max.**	**Units**
V_{S2}	supply voltage non stabilized	13	24	30	V
I_{S2}	V_{S2} = 13V - 30V		298+58*f/kHz+0,000105*(I_{AC}/A)^2		mA
V_{iT+}	input threshold voltage (High)			12,3	V
V_{iT-}	input threshold voltage (Low)	4,6			V
R_{IN}	input resistance		10		kΩ
C_{IN}	input capacitance		1		nF
$t_{d(on)IO}$	input-output turn-on propagation time		1,4		µs
$t_{d(off)IO}$	input-output turn-off propagation time		1,4		µs
$t_{pERRRESET}$	error memory reset time		12,2		µs
t_{TD}	top / bottom switch interlock time		3,3		µs
$I_{analogOUT}$	max. 5mA; 8 V corresponds to 15 V supply voltage for external components		2000		A
I_{s1out}	max. load current			50	mA
I_{TRIPSC}	over current trip level (I_{analog} OUT = 10 V)		2500		A
T_{tp}	over temperature protection	110		120	°C
U_{DCTRIP}	U_{DC}-protection ($U_{analog\ OUT}$ = 9 V); (option for GB types)		not implemented		V

Figure 3.6.10 Datasheet excerpt: SKiiP driver characteristics

Permissible driver supply voltage V_{S2}

The switching power supply unit used in latest SKiiP generations can be operated with an unstabilised supply voltage within the specified limits. If the lower limit is undercut, the error memory will be triggered and the ERROR OUT output will switch to HIGH and the IGBT will be turned off. The error memory is not reset until no further internal error signals are detected and both control signals have been set to LOW for at least $t_{pERRRESET}$, or until power-on reset occurs. The 24V raw voltage supply must be able to compensate for a minimum peak current load of 1.5 A; the voltage rise during turn-on must be linear without plateaus and under 2 s (for SKiiP3; SKiiP2 ≤ 50ms). Every turn-on induces a power-on reset for max. 150 ms (SKiiP3) during which time no switching signals may be applied to the SKiiP input. Parameter: ambient temperature T_a = 25°C.

Permissible driver supply voltage stabilised V_{S1} (SKiiP2 only)

Older SKiiP2 modules have an additional input for alternative supply with 15 V stabilised voltage within the rated limits. Like for the 24 V input, undervoltage protection is provided for the 15 V input, too. The 15 V voltage supply must be able to compensate for a minimum peak current load of 1.5 A; the voltage rise during turn-on must be linear without plateaus within or under 50 ms. Every turn-on induces a power-on reset for max. 130 ms during which time no switching signals may be applied to the SKiiP input. Parameter: ambient temperature T_a = 25°C.

Driver supply current I_{S2} and I_{S1} (I_{S1} for SKiiP2 only)

The current consumption of the SKiiP driver is dependent on the supply voltage, the switching frequency, the gate capacitance of the IGBT and the AC current detected by the compensating current sensors. For this reason, a specially formed equation with the variables switching frequency and AC current is included in the datasheet. The voltage supply should be dimensioned such that it exceeds the indicated current values by at least 20%. Parameter: ambient temperature T_a = 25°C.

High and low input threshold voltages V_{it+}, V_{it-}

Maximum LOW and minimum HIGH threshold voltage of control signals at the driver inputs according to applicable standards; parameter: ambient temperature T_a = 25°C.

Input resistance R_{IN} and input capacitance C_{IN}

Driver input properties; parameter: ambient temperature T_a = 25°C.

Turn-on and turn-off delay time $t_{d(on)IO}$ and $t_{d(off)IO}$

Delay times between driver input switchover and IGBT power section switching as caused by the internal driver signal run times. The delay times allow for the suppression of short interference pulses at the SKiiP input. Turn-on or turn-off signals with a pulse duration of < 625 ns are reliably suppressed, while signals of pulse durations of > 750 ns are reliably processed (see Figure 3.6.11). Parameter: ambient temperature T_a = 25°C.

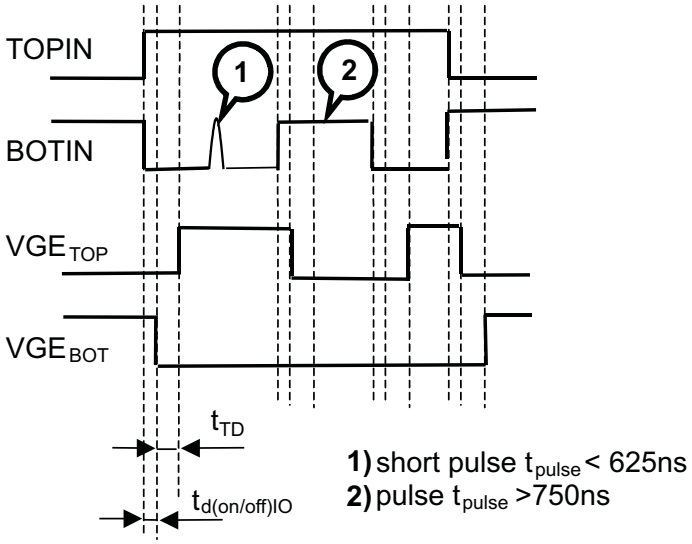


Figure 3.6.11 Principle behind short-pulse suppression in the SKiiP driver

Error memory reset time $t_{pERRRESET}$

There are different error signals which set the error memory of a SKiiP (e.g. overcurrent, overtemperature, driver undervoltage or, optionally, DC overvoltage); see "Technical Explanations SKiiP". Setting the error memory will cause the driver to turn off the IGBT. The error memory is not reset until no further internal error signals are detected and both control signals have been set to LOW for at least $t_{pERRRESET}$, or until power-on reset occurs. Parameter: ambient temperature T_a = 25°C.

TOP/BOTTOM switch interlock time t_{TD} during IGBT turn-on

Since the turn-on and turn-off processes differ in terms of duration, a dead time of a few µs has to be generated for every commutation process during which both driver outputs are interlocked. The interlock time generated by the SKiiP driver is indicated in the datasheet as t_{TD}. Parameter: ambient temperature T_a = 25°C.

Since the interlock period only starts at the moment when the IGBT is turned off, interlock times possibly generated by the controller will not prolong this period. As illustrated in Figure 3.6.12, the total delay time during IGBT turn-on corresponds to the total TOP/BOTTOM switch interlock time t_{TD} and driver delay time $t_{d(on)IO}/t_{d(off)IO}$.

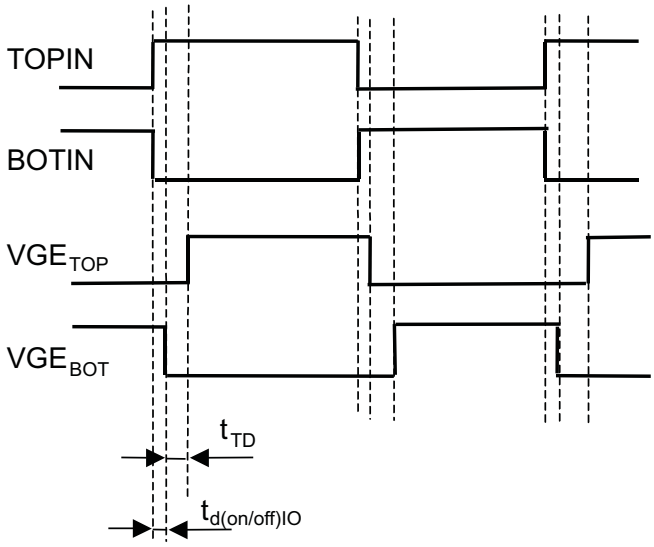


Figure 3.6.12 Delay times of SKiiP control signals

SKiiP AC output current for 8 V output signal at pin $I_{analogOUT}$

The output current conducted through the AC terminals is detected by the current sensors integrated in the SKiiP. Every half-bridge (fold) is equipped with its own current sensor. The output signals of these current sensors are combined to a general signal $I_{analogOUT}$ in the driver. The output voltage at every pin is 8 V for 100% of the current indicated as $I_{analogOUT}$ in the datasheet. As the drivers for SKiiP3 are identical with respect to the internal chip arrangement, but different regarding the DBC substrate (Al_2O_3: SKiiP xx1x… or AlN: SKiiP xx0x…), the current normalisation from $I_{analogOUT}$ to the AC output current is also identical, which implies, however, that the respective relation of the characteristic $I_{analogOUT}$ to the maximum rating I_C is different. Parameter: ambient temperature T_a = 25°C, maximum output load is 5 mA.

Maximum permissible output current at the 15 V output I_{s1out}

Both SKiiP2 and SKiiP3 feature an additional output to provide 15 V auxiliary voltage for external components, which, in the case of SKiiP2, is identical to the alternative output for 15 V supply voltage V_{S1}. I_{s1out} is the maximum current which can be provided by this terminal when supplied with 24 V (V_{S2}). Parameter: ambient temperature T_a = 25°C.

Overcurrent trip level I_{TRIPSC}

Among other protective functions, SKiiP offers overcurrent protection (OCP) as soon as the integrated current sensors detect an AC output current above a trip level of 125 % of the rated $I_{analogOUT}$. Irrespective of the SKiiP version, the OCP trip level thus corresponds to a voltage of 10 V applied at the $I_{analogOUT}$ terminal. For SKiiP modules with identical chip sets and different DBC substrates Al_2O_3 or AlN), it is therefore identical. Consequently, the relation between I_{TRIPSC} and maximum I_C varies depending on the DBC substrate used (see above). As soon as the trip level is reached, the error memory will be set with the ERROR OUT output switched to HIGH and the IGBT switched off.

The error memory is not reset until no further internal error signals are detected and both control signals have been set to LOW for at least $t_{pERRRESET}$, or until power-on reset occurs. Parameter: ambient temperature T_a = 25°C.

Ground fault trip level $I_{TRIPSLG}$

This function is offered in the SKiiP2 GD and GDL types only. If the AC output current exceeds the trip level indicated in the datasheet as $I_{TRIPSLG}$ = 30% of I_C (acc. to datasheet information), the error memory will be set, the ERROR OUT output switched to HIGH and the IGBT switched off. The error memory is not reset until no further internal error signals are detected and both control signals have been set to LOW for at least $t_{pERRRESET}$, or until power-on reset occurs.

Overtemperature threshold T_{tp}

The temperature T_r, which is approximately equal to the heatsink temperature, is detected by the temperature sensor integrated in the SKiiP module. As soon as T_r reaches the level of T_{tp} indicated in the datasheet, the error memory will be set, the OVERTEMP OUT and ERROR OUT outputs switched to HIGH, and the IGBT switched off. The error memory is not reset until no further internal error signals are detected and both control signals have been set to LOW for at least $t_{pERRRESET}$, or until power-on reset occurs.

Since T_{tp} (110…115…120°C) is not much lower than the maximum permissible chip temperature, safe thermal protection is not always guaranteed by the internal overtemperature protection alone in highly efficient cooling systems.

DC link voltage detection $U_{analogOUT}$ and DC link voltage trip level (overvoltage protection) U_{DCTRIP}

DC link voltage monitoring is optionally available for all SKiiP types except for SKiiP3 2GB. The actual DC link voltage is detected by means of high-ohmic differential measurement (5 MΩ, qualified according to EN 50178) on the low-voltage level. The maximum rating of V_{CC} corresponds to $U_{analogOUT}$ = 9 V ± 2%. As soon as the DC link voltage passes the maximum rating of V_{CC} (see datasheet, 900 V for 1200 V-SKiiP, 1200 V for 1700 V-SKiiP), the error memory will be set, the ERROR OUT output switched to HIGH, and the IGBT turned off. The error memory is not reset until no further internal error signals are detected and both control signals have been set to LOW for at least $t_{pERRRESET}$, or until power-on reset occurs.

A low-pass filter provides interference suppression for a time constant of 500 µs. This monitoring function is therefore not suitable for detecting extreme voltage jumps. Parameter: ambient temperature T_a = 25°C.

Properties of the SKiiP2 GDL brake chopper

The "GDL" SKiiP types of the older SKiiP2 series consist of a 3-phase inverter with an additional brake chopper, the characteristics and maximum ratings of which are not specified separately in the datasheets. Figure 3.6.13 shows the brake chopper block diagram.

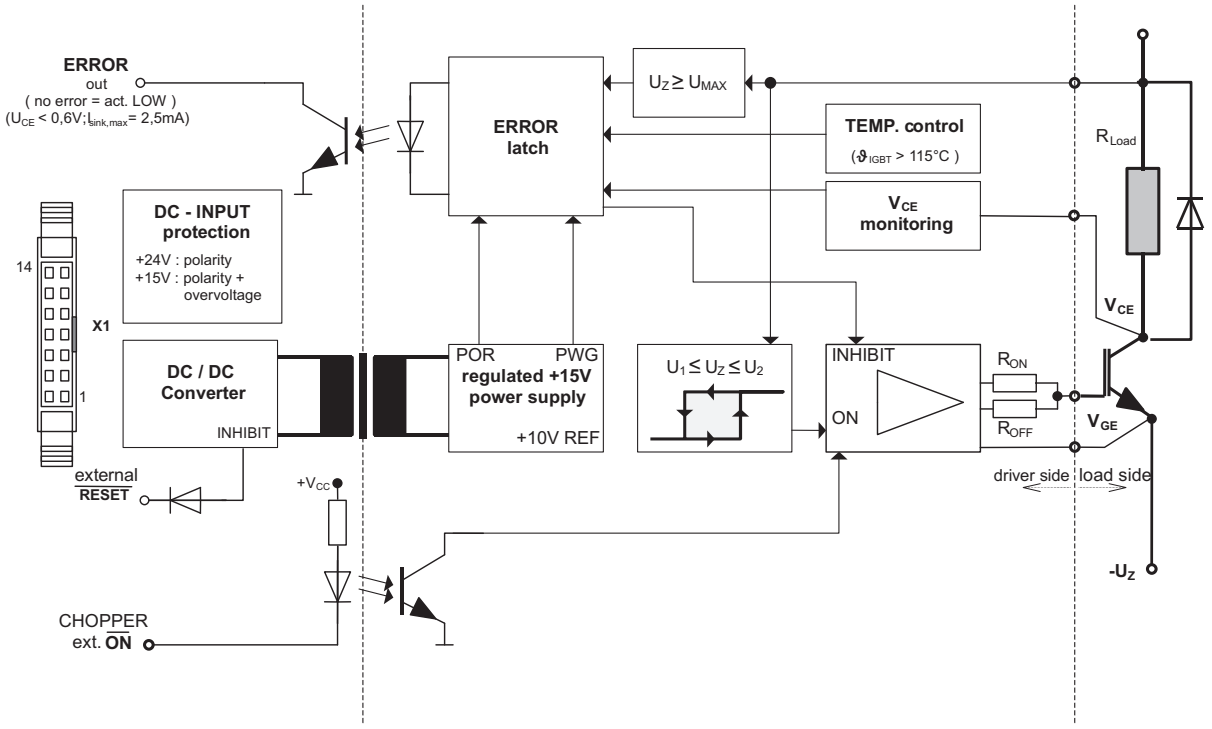


Figure 3.6.13 Block diagram of the SKiiP2 “GDL” brake chopper

The ON and OFF signals of the chopper IGBT are generated in dependency of the DC link voltage by a two-step controller. Typically, the minimum turn-on time is limited to 30 µs. Two different GDL versions are available for SKiiP2 1200 V (cf. Table 3.6.2).

Switching thresholds	Version E for V_N = 400 Vac	Version A for V_N = 460 Vac
V_{dmax}	730 V	860 V
V_{don} (Chopper ON)	681 V	802 V
V_{doff} (Chopper OFF)	667 V	786 V

Table 3.6.2 Switchover voltages of 1200 V SKiiP2 GDL brake choppers

Via the CHOPPER ext./ON input it is possible to turn on the brake chopper using an external trigger unit, provided the error memory is not set and the ERROR output is set to HIGH. The maximum external switching frequency is 5 kHz. The brake chopper features short-circuit protection via $V_{CE(sat)}$ monitoring, overtemperature protection (T_r = 115°C), driver voltage control and overvoltage monitoring functions (switching signal suppression above V_{dmax}); for detailed information see "Technical Explanations SKiiP" at www.semikron.com.

3.6.2 MiniSKiiP IPM

In addition to the MiniSKiiP power section, MiniSKiiP IPMs feature an integrated SOI driver for all the IGBT. State-of-the-art IPMs are nowadays capable of achieving a converter output power of up to around 15 kW and are available in inverter or CIB topologies in a MiniSKiiP2 case. The type designation code is similar to that for standard MiniSKiiP modules, but contains an additional "I" in the topology code, e.g. SKiiP 26NABI066V3 (600 V CIB IPM) or SKiiP 25ACI12T4V2 (1200 V inverter IPM). Figure 3.6.14 shows the layout and basic structure of a SKiiP 26NABI066V3.

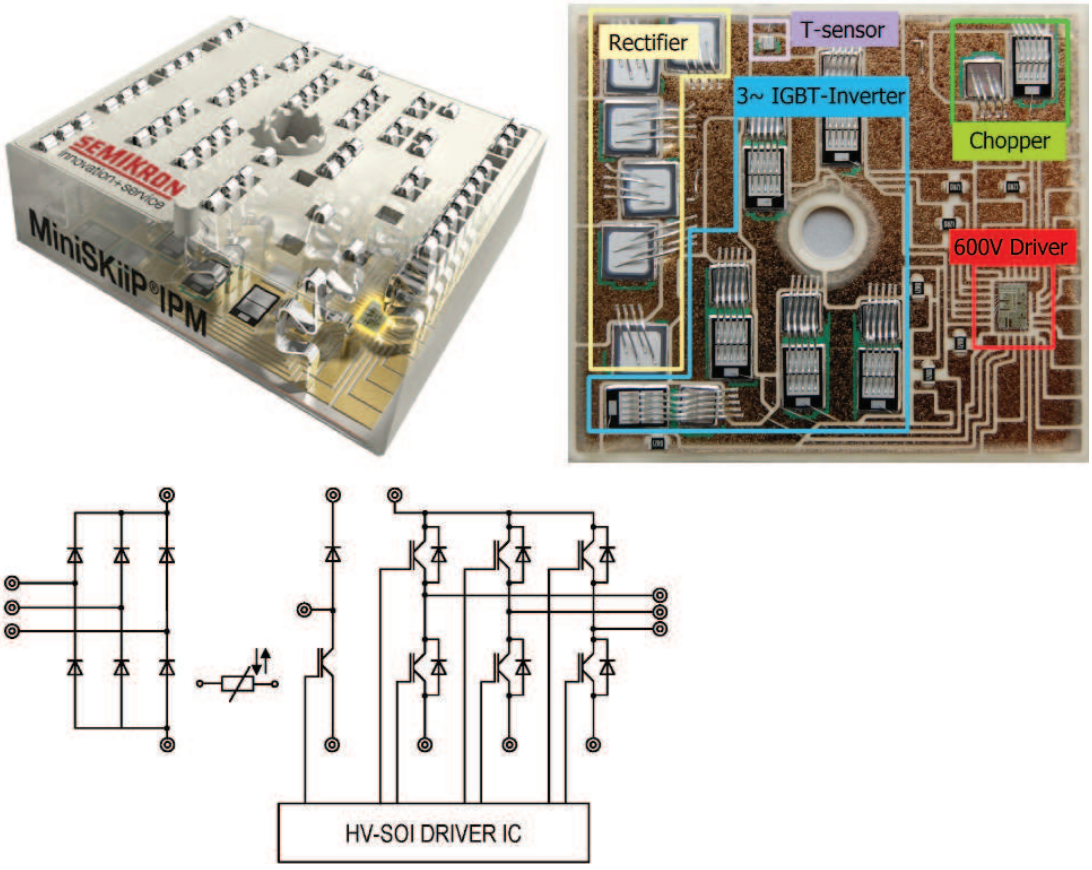


Figure 3.6.14 Layout and basic structure of a MiniSKiiP IPM in CIB configuration

The MiniSKiiP IPM datasheet contains maximum ratings and characteristics for the IGBT, diodes, driver and the complete system. Since the datasheet ratings for IGBT, diodes, temperature sensors and the system (case) basically correspond to the ratings for standard MiniSKiiP, only data relating to the driver is specified below.
For better clarification of the datasheet ratings, the specific MiniSKiiP IPM inputs and outputs listed in Table 3.6.3 shall be illustrated in Figure 3.6.15.

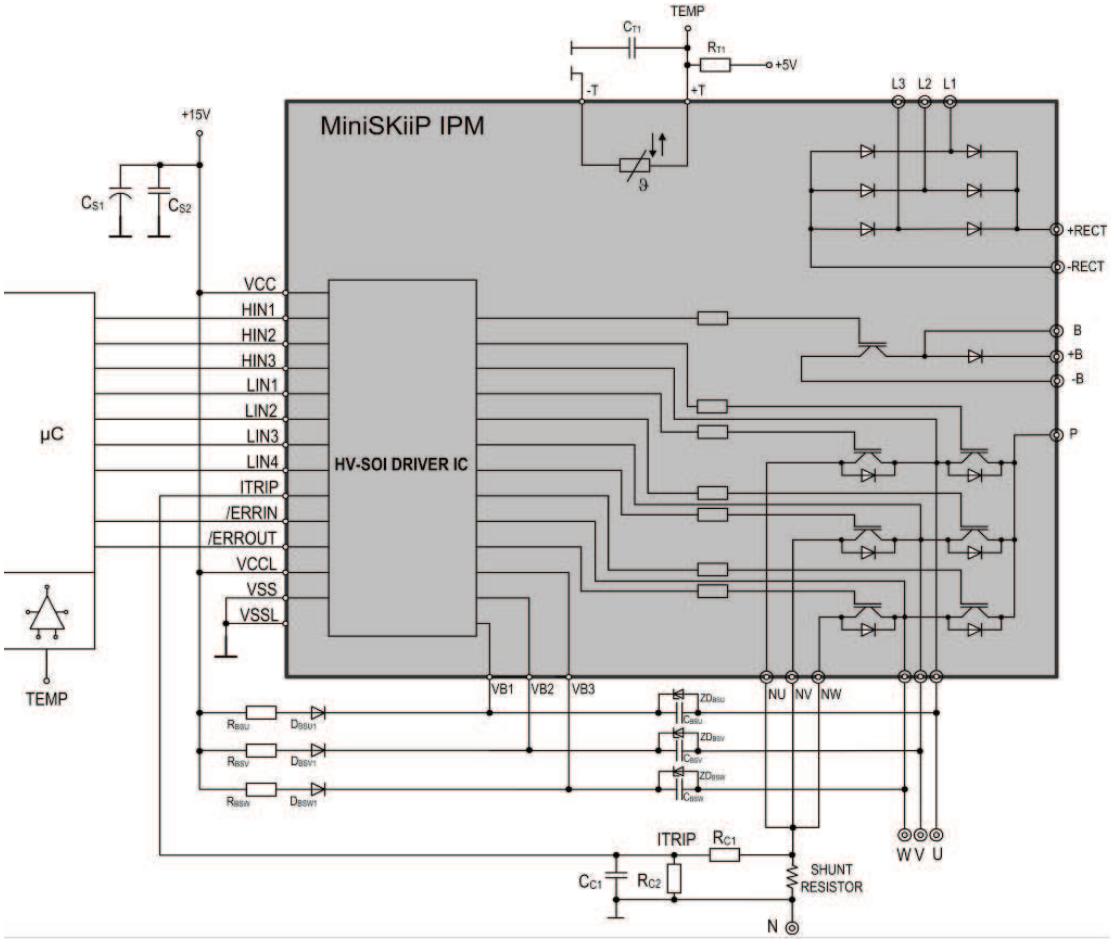


Figure 3.6.15 MiniSKiiP IPM (CIB inverter topology) incl. external circuit elements

Pin name	Pin description
V_{CC}	+ driver IC main supply voltage
V_{SS}	driver IC supply voltage ground
V_{CCL}	+ low-side IGBT supply voltage (external connection to V_{CC})
V_{SSL}	+ low-side IGBT supply voltage (external connection to V_{CC})
V_{B1}, V_{B2}, V_{B3}	bootstrap voltages for U, V, W phases of TOP IGBT
HIN1, HIN2, HIN3	PWM signal inputs for U, V, W phases of high-side switch
LIN1, LIN2, LIN3	PWM signal inputs for U, V, W phases of low-side switch
LIN4	PWM signal input for brake chopper switch (CIB types)
/ERRIN	external error/shut-down logic input (inverted)
ITRIP	comparator input for external current measurement (overcurrent shut-down)
/ERROUT	error logic output (inverted)
+T, -T	temperature sensor terminals (actual value)
L1, L2, L3	bridge rectifier AC inputs (CIB types)
+RECT, -RECT	bridge rectifier outputs for + and - DC link (CIB types)

Pin name	Pin description
P	+DC-link input
NU, NV, NW	- DC link input for U, V, W phases
U, V, W	U, V, W phase AC-outputs
+B, B, -B	brake chopper terminals +DC, collector, -DC (CIB types)

Table 3.6.3 Pins of a MiniSKiiP IPM inverter

For control and driver power transmission to the TOP IGBT of the U, V and W phases, level shifter / bootstrap circuits are used. Figure 3.6.16 shows the basic bootstrap circuit for the TOP IGBT of one phase, illustrating the function of the terminals V_{B1}, V_{B2} and V_{B3}.

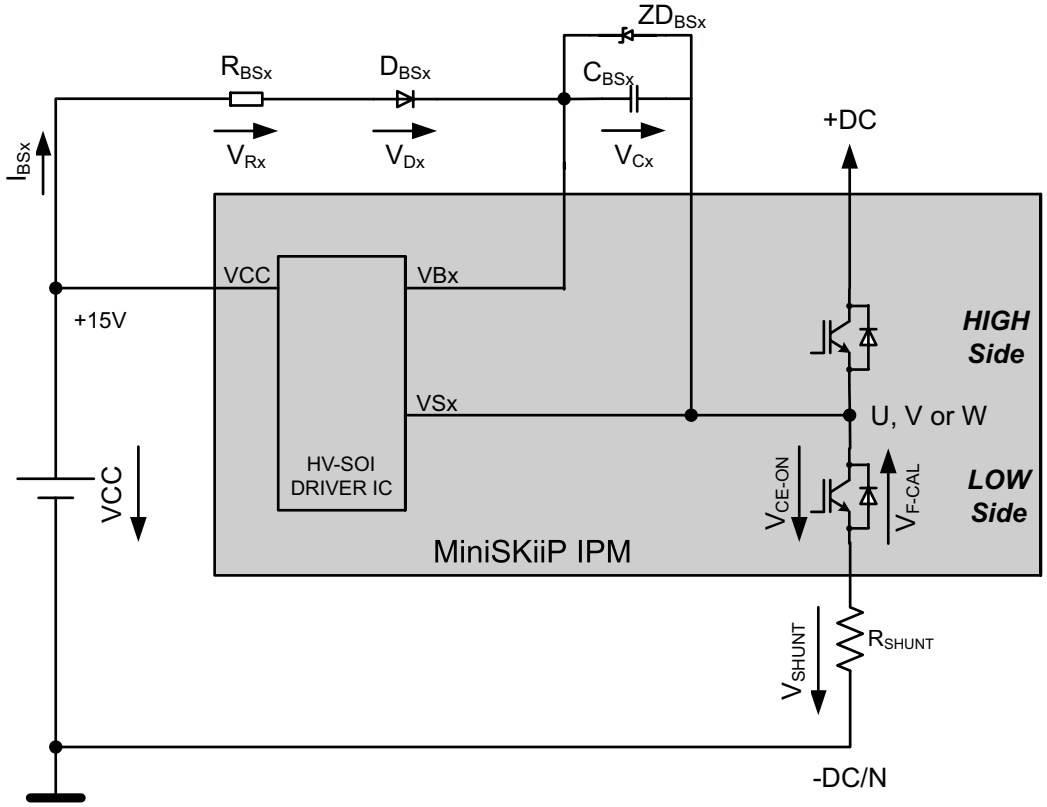


Figure 3.6.16 Basic bootstrap circuit of a TOP IGBT of one phase

Further details can be found in "Technical Explanations MiniSKiiP IPM" at www.semikron.com.

3.6.2.1 Maximum ratings of the MiniSKiiP IPM driver

Driver - Inverter, Chopper				
VCC	Applied between VCC-VSS, VCCL-VSSL		17	V
VBx	Applied between VB1-U, VB2-V, VB3-W		17	V
VSx	Voltage to VSS, t_p<500ns		-3 … 600	V
V_{in}	Applied between HIN1, LIN1, HIN2, LIN2, HIN3, LIN3, LIN4, /ERRIN - VSS		VSS-0.3 … VCC+0.3	V
V_{oErr}	Applied between /ERROUT-VSS		VSS-0.3 … VCC+0.3	V
$I_{max(EO)}$	Between /ERROUT-VSS		10	mA
V_{ITRIP}	Applied between ITRIP-VSS		VSS-0.3 … VCC+0.3	V
f_{max}			20	kHz

Figure 3.6.17 Datasheet excerpt: maximum ratings of the MiniSKiiP IPM driver

All maximum ratings indicated in the datasheet refer to a heatsink temperature of 25°C.

Driver supply voltage V_{cc}

Absolute maximum supply voltage applied between V_{CC} and V_{SS} or V_{CCL} and V_{SSL}

High-side "floating" supply voltage V_{Bx}

Absolute maximum voltage applied between the following terminals: V_{B1}-U, V_{B2}-V, V_{B3}-W

High-side "floating" supply offset voltage V_{Sx}

Maximum rating of transient voltage peak between terminals V_{SX} and V_{SS} ($V_{Sx} = V_{CES}$); parameter: pulse duration t_p < 500 ns.

Input signal voltage V_{in}

The maximum ratings for the input signal voltage applied between the HIN1, LIN1, HIN2, LIN2, HIN3, LIN3, /ERRIN and V_{SS} terminals result from the specified HIGH and LOW levels of the driver logic used to form the input signal.

/ERROUT output supply voltage V_{oErr}

ITRIP comparator input signal voltage V_{iTrip}

Absolute maximum supply voltage of the evaluation electronics to which the /ERROUT and ITRIP terminals may be connected (V_{SS} - 0.3 V < V < V_{SS} + 0.3 V).

/ERROUT output max. continuous current $I_{max(EO)}$

Maximum permissible continuous output current which may be collected from the /ERROUT terminal (open drain) and its turned-on output MOSFET (LOW level) via a drain resistance against V_{SS} .

Switching frequency f_{max}

Maximum permissible switching frequency limited by the maximum average output current $I_{G(AV)}$ of the driver supply voltage or driver power dissipation.

3.6.2.2 Electrical characteristics of the MiniSKiiP IPM driver

All maximum ratings indicated in the datasheet refer to a heatsink temperature of 25°C.

Driver						
VCC	Applied between VCC-VSS, VCCL-VSSL			15		V
ICC	VCC=15V, all logic inputs=open, VCC-VSS				5,0	mA
VBx	Applied between VB1-U, VB2-V, VB3-W			15		V
IBx	VBx=15V, V_{iH}=V_{iL}=0V			300		µA
V_{iT+}	Applied between HIN1, HIN2, HIN3, LIN1, LIN2, LIN3, LIN4, /ERRIN - VSS			1,9	2,4	V
V_{iT-}	Applied between HIN1, HIN2, HIN3, LIN1, LIN2, LIN3, LIN4, /ERRIN - VSS		0,8	1,1		V
V_{oErr}	Error Output Voltage Applied between /ERROUT-VSS				15	V
V_{UV}			10,3			V
V_{UVr}					12,1	V
$t_{d,ITRIP}$	Itrip to output propagation delay			690		ns
t_{SIS}	Short pulse suppression for signal inputs			420		ns
t_{TD}	Interlock Dead time			450		ns
f_{sw}				15	25	kHz

Figure 3.6.18 Datasheet excerpt: electrical characteristics of the MiniSKiiP IPM driver

Driver supply voltage V_{cc}

Nominal supply voltage applied between V_{CC} and V_{SS} or V_{CCL} and V_{SSL} as the basis of the driver specifications.

Driver supply current I_{cc}

Typical current intake of driver core and BOT drivers; parameter: V_{CC} = 15 V, V_{iH} = V_{iL} = 0 V.

High-side "floating" supply voltage V_{Bx}

Typical voltage applied between: V_{B1}-U, V_{B2}-V, V_{B3}-W.

High-side "floating" supply current I_{Bx}

Operating current from V_{Bx}; parameter: V_{Bx} = 15 V, V_{iH} = V_{iL} = 0 V.

Turn-on and turn-off threshold voltage V_{iT+} and V_{iT-} at the driver inputs

Typical switchover threshold voltage between the HIN1…3, LIN1…4, /ERRIN inputs and V_{SS}.

/ERROUT output supply voltage V_{oErr}

Typical output voltage of the error memory (between /ERROUT and V_{SS}) under nominal conditions; the /ERROUT will be set to LOW due to the errors "undervoltage" or "external error (/ERRIN = LOW)". Subsequent error memory reset is only possible when triggering errors no longer exist, the /ERRIN input has been on HIGH level for at least 9.5 µs, and the HIN1… 3 and LIN1…3 inputs have been set to LOW level likewise for a minimum of 9.5 µs.

Undervoltage threshold V_{UV}

If the driver supply voltage V_{CC} falls below the limit for V_{UV}, the integrated undervoltage protection will trigger an error signal, blocking the IGBT and setting the /ERROUT output to LOW.

Undervoltage threshold reset V_{UVr}

If the error memory has been set as a consequence of undervoltage, reset will only be possible once the driver supply voltage V_{CC} has exceeded V_{UVr}.

Overcurrent turn-off delay time $t_{d,ITRIP}$

Delay time between the moment when the overcurrent trip level I_{TRIP} is reached and the TOP and BOT IGBT is turned off; parameters: V_C = 15 V, V_{iH} = 3.3 V, V_{iL} = 0 V, V_{ITRIP} = 1 V.

Minimum input pulse width (short-pulse suppression) t_{SPS}

Minimum pulse width of input and output signals. Shorter pulses are suppressed.

IGBT interlock dead time t_{TD}

The MiniSKiiP IPM generates an interlock dead time of 450 ns.If both control inputs (HIN/LIN) of a channel are on HIGH level, the TOP and BOT-IGBT will be turned off. This event will not be indicated as an error.

4 Application Notes for Thyristors and Rectifier Diodes

4.1 Thyristor and Rectifier Dimensioning and Selection

The general guidelines given in chapter 5.1 are to be applied by analogy to the selection of thyristors, rectifier diodes and thyristor / diode modules. For operation at a line frequency of 50 / 60 Hz, any additional stresses caused by switching losses may be neglected. When selecting power semiconductors for actual applications, the following aspects have to be taken into account:
- Voltage load capacity,
- Current load capacity under the achievable cooling conditions and
- permissible operating areas

The aforementioned aspects must be factored into considerations for all stationary and short-time operating conditions (overload).

The maximum rated values given in the datasheets for blocking voltage, peak current and junction temperature must not be exceeded as a result of stresses under any static or dynamic conditions. The same applies to the limits specified for the case, e.g. vibration and shock resistance, resistance to extreme climatic conditions, insulation voltage in modules and assembly and mounting instructions. An exception with regard to the reverse voltage is avalanche-resistant diodes for a maximum avalanche power dissipation P_{RSM}; an exception relating to the junction temperature is a surge current event. To achieve a high degree of reliability and sufficient service life, the module capacity must factor in the intended number of load cycles at which notable temperature cycles occur (chapter 2.7). Furthermore, "serious" dimensioning is generally not based on the thermal capacity of the semiconductors up to the limit value $T_{j(max)}$ in order to leave a safety margin for cases that have not been considered in theory and for module ageing.

4.1.1 Reverse voltage

In diodes and thyristors, the on-state losses are less dependent on the voltage rating than is true for MOSFET and IGBT. Therefore, when selecting the component voltage class, the safety margin between the component reverse voltages that usually occur and the permissible reverse voltages must be sufficiently large. Normally, the following reverse voltages are selected for diodes and thyristors for line voltage V_N:

Line voltage V_N	Rectification	No-load direct voltage V_{di}	Reverse voltage V_{RRM}
110 – 125 V	B2	97 - 110 V	600 V
200 – 240 V	B2	180 – 220 V	800 V
400 – 460 V	B6	540 – 621 V	1200 – 1400 V
575 – 690 V	B6	770 – 932 V	1800 – 2200 V

Table 4.1.1 Recommended reverse voltage for thyristors and rectifier diodes in dependence of the rated current of the line

Ensure that at maximum voltage load, the maximum permissible module voltage is not exceeded. This applies in particular to stationary input voltage (rated voltage + tolerance, e.g. +10%) and transient overvoltage, provided these are not reduced by line filters, DC link capacitors and dc-side protective devices (suppressor diodes, snubbers, varistors). For transient voltage peaks, a slightly higher peak voltage (V_{RSM}) is often permissible. Note that the reverse voltage specified for 25°C is temperature-dependent and has a positive temperature coefficient. This value is dependent on the reverse voltage of the component itself and can amount to a few V/K.

4.1.2 Rectifier diodes

4.1.2.1 Thermal load in continuous duty

The forward current load in continuous duty is related to the product of the mean power dissipation P_{FAV} and total thermal resistance $R_{th(j-a)}$. This product must not exceed the difference between the ambient temperature T_a and the maximum permissible virtual junction temperature T_j:

$$P_{FAV} \cdot R_{th(j-a)} \leq T_j - T_a$$

The following general formula is used to calculate the power dissipation:

$$P_{FAV} = V_{F0}(T_j) \cdot I_{FAV} + r_F(T_j) \cdot I_{FRMS}^{\ 2}$$

For the typical diode current waveforms (180° sinusoidal, 120° rectangular), the current (wave) form factor can easily be calculated as follows:

$$F_I = \frac{I_{FRMS}}{I_{FAV}}$$

Thus, P_{FAV} still depends on one unknown only; in most cases, representation with I_{FAV} is selected:

$$P_{FAV} = V_{F0}(T_j) \cdot I_{FAV} + r_F(T_j) \cdot F_I^{\ 2} \cdot I_{FAV}^{\ 2}$$

These formulae form the basis of almost every component design software tool (see chapter 4.1.6). Nonetheless, datasheets contain numerous graphs and characteristics to help the user with product selection. Descriptions on how to use these characteristics are given below.

Low-power rectifier diodes

Datasheets often contain diagrams for these components that show the permissible I_{FAV} as a percentage of the rated on-state current as a function of the ambient temperature T_a (Figure 4.1.1).

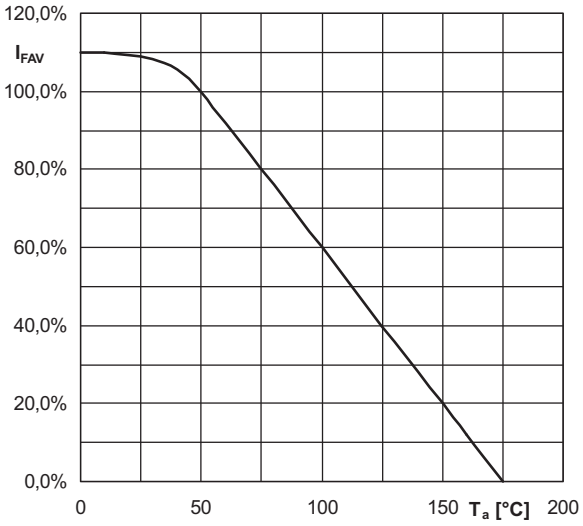


Figure 4.1.1 Permissible mean on-state current I_{FAV} (as percentage of I_{FAV} at T_a = 50°C) as a function of the ambient temperature T_a under the cooling conditions specified in the datasheet.

Power diodes

Here, diagrams such as that shown in Figure 4.1.2 are used to determine the permissible mean forward current for certain cooling conditions and vice-versa to determine the necessary cooling conditions for a given current. The curves on the left of Figure 4.1.2 end at the current densities that correspond to the max. permissible effective forward current I_{FRMS}, which limits the permissible on-state load even under optimum cooling conditions.

Example of the use of Figure 4.1.2: A 130 A diode is used in a six-pulse bridge circuit (B6). Required DC current 300 A in continuous duty; this corresponds to I_{FAV} = 100 A per diode. The current waveform in every leg is approximately rectangular with a conduction angle of 120° (rec.120). For I_{FAV} = 100 A, P_{FAV} = 122 W and the maximum permissible case temperature T_c = 137°C (blue line).

With a safety margin of 25% (red line with I_{FAV} = 125 A), the result is T_c = 120°C and P_{FAV} = 170 W. For this case, with a cooling air temperature T_a = 35°C, the maximum diode thermal resistance case-air $R_{th(c-a)}$ = 0.50 K/W. This includes $R_{th(c-s)}$ = 0.08 K/W. For the heat sink, this leaves $R_{th(s-a)}$ = 0.42 K/W.

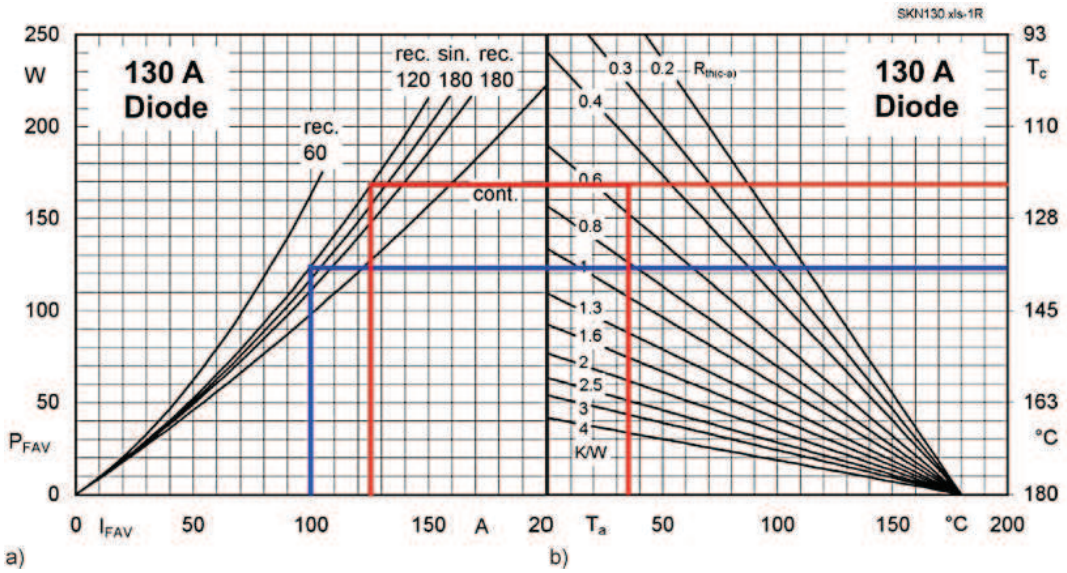


Figure 4.1.2 a) Mean forward power dissipation P_{FAV} over mean forward current I_{FAV} for different current waveforms; b) Case temperature T_c over ambient temperature T_a; the parameter is the thermal resistance case-to-air $R_{th(c-a)}$

4.1.2.2 Operation with short-time and intermittent load

To calculate the maximum permissible current load for short-time and intermittent operation, the curve for thermal impedance is given as a function of time; specifically, this is given for the diode ($Z_{th(j-c)}$ + $Z_{th(c-s)}$) and for the heat sink ($Z_{th(s-a)}$). If the values for thermal impedance for diode and heat sink are added, the total thermal impedance $Z_{th(j-a)}$ for the time observed is obtained.

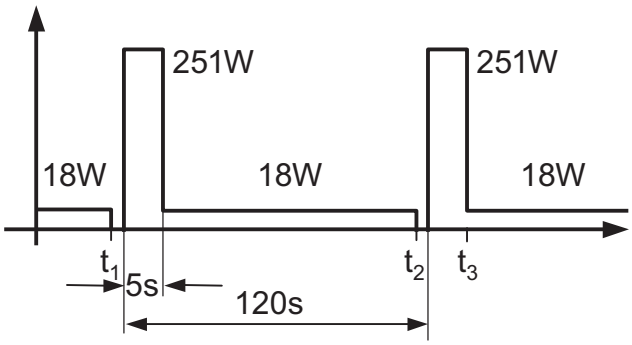


Figure 4.1.3 Power dissipation P_{FAV} over time for the example given. At the times t_1 and t_2, the diode is switched off and back on again immediately.

Calculation of junction temperature in short-time operation is likewise shown by way of an example: A **six-pulse bridge circuit** containing SKN 130 diodes on K 0.55 heat sinks is to deliver 500 A for 5 seconds after turn-on, after which the current will drop to a lower permissible value for continuous duty of 60 A. This is clearly short-time operation, since the stationary end temperature is not reached within the 5 seconds. One of the secondary conditions here should be that the diode is turned back on immediately after turn-off and that the increased current occurs for 5 seconds again. The shortest possible time between turn-on operations is 2 minutes. For 60 A direct current,

20 A flow per diode. This corresponds to power dissipation of 18 W (see Figure 4.1.2a). For 500 A, 167 A flows in each diode. The power dissipation for 167 A for a 120° rectangular current can no longer be derived from Figure 4.1.2. For this reason, the formula given in the section on datasheet ratings (chapter 3.2.2) is used:

$$P_{FAV} = V_{F0} \cdot I_{FAV} + r_f \cdot \frac{360°}{120°} \cdot I_{FAV}^2$$

The values for V_{F0} = 0.85 V and r_f = 1.3 mΩ are specified in the datasheet.

$$P_{FAV} = 0{,}85V \cdot 167A + 0{,}0013\Omega \cdot 3 \cdot 167A^2 = 251W$$

This results in the power dissipation shown in the characteristic in Figure 4.1.3. Heat sink pre-warming is determined by the average power dissipation calculated. The following applies to a max. ambient temperature of 45°C:

$$T_s = T_a + R_{th(s-a)} \cdot \left(P_{FAV1} \cdot \frac{t_{p1}}{T} + P_{FAV2} \cdot \frac{t_{p2}}{T} \right)$$

$$T_s = 45°C + 0{,}55\frac{K}{W} \cdot \left(251W \cdot \frac{5s}{120s} + 18W \cdot \frac{115s}{120s} \right) = 60°C$$

Now, as described in chapter 5.2, the equation used to calculate the maximum resulting virtual junction temperature T_{jM} (at time t_3) is applied. If the pause between turn-off and turn-on is short enough, a basic thermal load of 18 W can be assumed, superimposed by a power dissipation pulse of 251 W-18 W.

$$T_{jM} = T_s + P_{AV1} \cdot R_{th(j-s)} + (P_{AV2} - P_{AV1}) \cdot \sum_{\nu=1}^{n} R_{th\nu} \cdot \left(\frac{1 - e^{\frac{-t_{p1}}{\tau_{th\nu}}}}{1 - e^{\frac{-T}{\tau_{th\nu}}}} \right)$$

For precise calculations, the $Z_{th(j-a)}$ values which factor in the pulsing of junction temperature at the rate of the operating frequency have to be added to the $Z_{(th)z}$ values. As the values for the additional thermal resistance for line frequencies of 40 - 60 Hz constitute just a small part of the total thermal resistance, they are often neglected (Note: At higher frequencies this share is even smaller, while for low frequencies it cannot be neglected). The table for the additional thermal resistance is thus not included in the datasheets of many power diodes. For thyristors, as previously explained, $Z_{(th)z}$ must be factored into the calculation under all circumstances.

4.1.2.3 Load at higher frequencies

In line rectifiers switching losses are neglected. Here, the switching losses at 50 Hz are around 1...2% of the conducting losses and are thus covered by the design reserve. Up to around 200 Hz, the power dissipation curves from the previous chapter are to be used, as the increasing switching losses and the lower temperature ripple at higher line frequency compensate one another to some extent. For even higher frequencies, however, current derating is necessary. At 500 Hz, for example, additional losses of 15…20% of the switching loss share must be reckoned with.

4.1.2.4 Rated surge forward current for times below and above 10 ms

In the event of short circuit, the diode has to survive the surge current calculated from the line impedance and line voltage. A no-load capacitor as load is comparable with a short circuit. Figure 4.1.4 shows the overcurrents $I_{F(OV)}$ permissible in the event of an error (short-circuit) in relation to the surge forward current I_{FSM} for different reverse voltages. Normally, when a short circuit or high overload occurs, a fuse or another protective device is activated. After turn-off of the short-circuit current, no reverse voltage ($V_R = 0 \cdot V_{RRM}$) is present at the diodes through which current had previously been flowing. In certain cases, the short-circuit current is limited such that it can hold for a

certain time without damaging the diode and other parts of the circuit. Once this time has elapsed, the short circuit may be gone. Following the overcurrent, a reverse voltage V_R will be present at the diode. Depending on the size of this voltage, interpolation between the three curves may be performed ($0 \cdot V_{RRM}$: Without reverse voltage load; $0.5 \cdot V_{RRM}$: Load with half the peak reverse voltage; $1 \cdot V_{RRM}$: Load with maximum permissible periodic peak reverse voltage). Voltages $V_R > V_{RRM}$ are, of course, not permissible. Values greater than 10 ms apply to half sine waves lasting 10 ms that occur in succession at intervals of 20 ms.

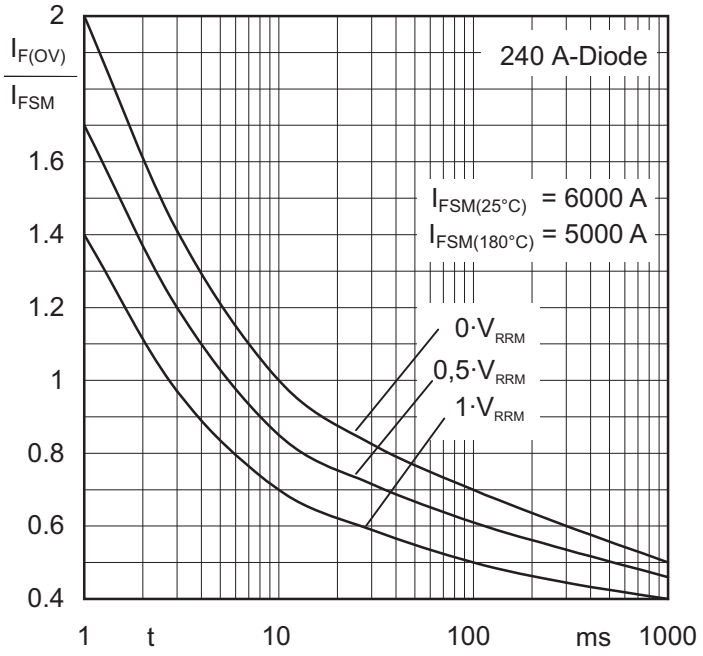


Figure 4.1.4 Permissible error-induced overcurrents $I_{F(OV)}$ in relation to surge forward current I_{FSM} for different reverse voltage conditions directly following the last sinusoidal half-wave as a function of time t

4.1.3 Thyristors

4.1.3.1 Load in continuous duty

As previously explained, in thyristors the pulsing of the virtual junction temperature in line with the operating frequency has to be taken into account when determining the limiting value of the mean forward current. In thyristors that change the conduction angle in order to control the output voltage, the result is rectangular pulses with shorter conduction angles under inductive load or "controlled" half sine waves for resistive load.

The I_{TAV}-P_{TAV}-R_{th} diagrams for thyristors (Figure 4.1.5) look similar to those for rectifier diodes (Figure 4.1.2). The same applies to thyristor handling. The difference is that in the case of thyristors it is not the heat sink thermal resistances $R_{th(c-a)}$, but the thermal resistances $R_{th(j-a)}$ of thyristor and heat sink that are indicated over the ambient temperature T_a. At the right hand edge of the picture, the maximum permissible case temperature can likewise not be specified because it depends on the conduction angle and is thus different for every curve. $R_{th(j-c)}$ used to calculate the maximum permissible case temperature can, however, be taken directly from a special graph (Figure 4.1.6). Here, the effective $R_{th(j-c)}$ values are shown in dependence of the conduction angle. With the increased values, the temperature ripple is taken into account, which swings around the mean junction temperature $T_{j(av)}$ calculated from the mean losses P_{TAV}. $R_{th(j-c)(cont.)}$ applies to pure DC current. The table shows the thermal resistances case to ambient $R_{th(c-a)}$ of the relevant heat sinks. If the gate dissipation in thyristors is not negligibly low, this must be taken into account when calculating total losses.

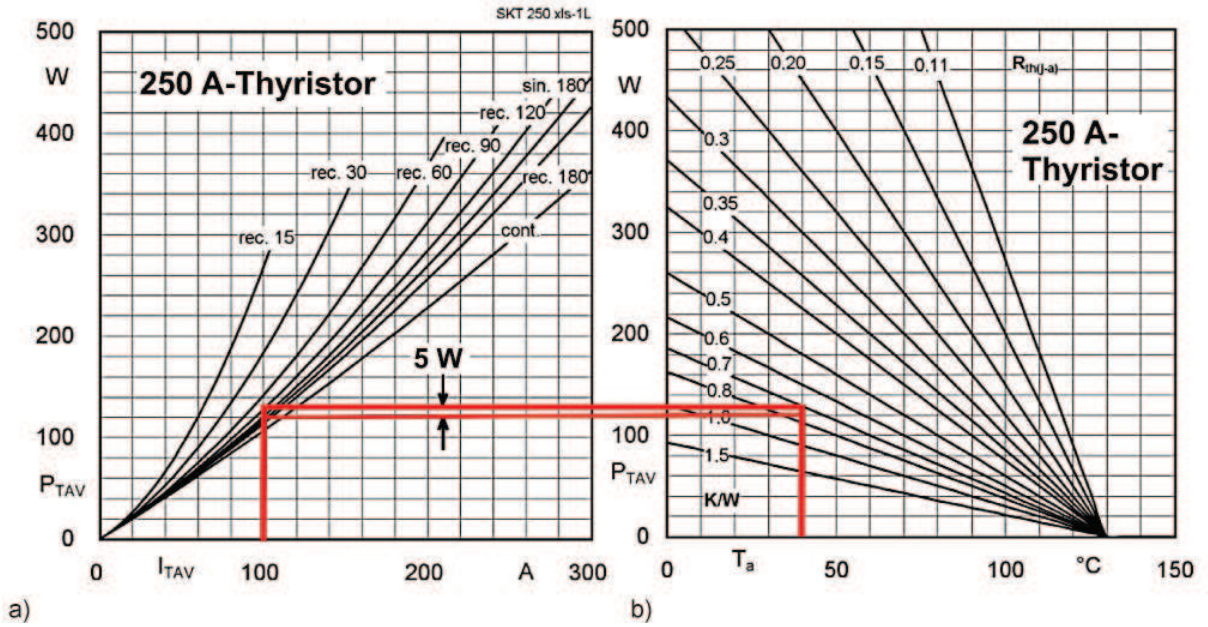


Figure 4.1.5 a) Mean forward dissipation P_{TAV} over mean forward current I_{TAV} for different conduction angles; b) Permissible power dissipation P_{TAV} over ambient temperature T_a and different $R_{th(j-a)}$.

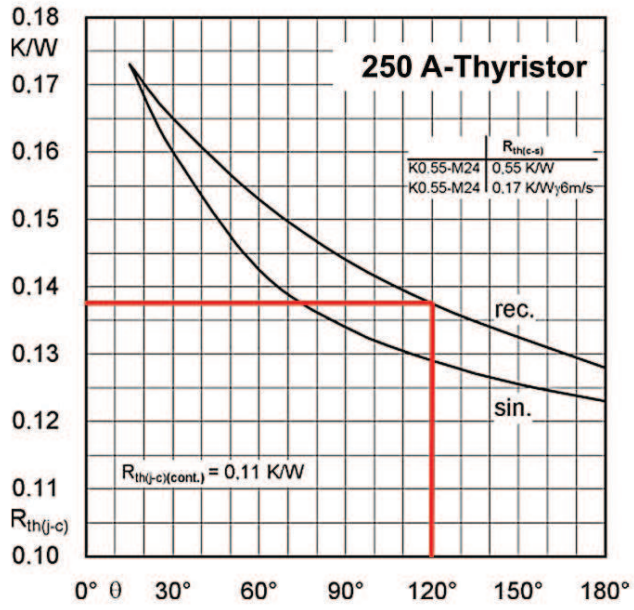


Figure 4.1.6 $R_{th(j-c)}$ as a function of the conduction angle Θ for controlled half sine waves (sin.) and rectangular pulses (rec.)

Dimensioning based on Figure 4.1.5 is explained by way of a basic example below. A six-pulse bridge circuit is supposed to deliver 300 A at maximum conduction angle. Natural air cooling is to be used. Heat sinks with $R_{th(s-a)}$ = 0.5 K/W thermal resistance for 100 W power dissipation are available. Which thyristor is suitable? Assuming the 300 A already contains sufficient reserve, i.e. no more reserve is needed, the mean forward current per thyristor is then 100 A. In accordance with Figure 4.1.5a, for rectangular currents of Θ = 120° conduction angle for I_{TAV} = 100 A a maximum power dissipation of 110 W can be expected. A medium-sized power dissipation of 5 W might occur, too. The power dissipation is now 115 W; let us turn to the diagram on the right. At an ambient temperature T_a = 45 °C, the total thermal resistance may not exceed $R_{th(j-a)}$ = 0.70 K / W (red line). Looking at Figure 4.1.6, for rectangular currents of Θ =120° this results in a thermal resistance $R_{th(j-c)}$ = 0.137 K/W. In addition, the junction thermal resistance $R_{th(c-s)}$ = 0.015 K/W and

the heat sink thermal resistance $R_{th(s-a)}$ of 0.5 K/W. This results in a total $R_{th(j-a)}$ = 0.652 K/W, which is less than 0.70 K/W.

In other words, this thyristor offers the necessary current capability. From Figure 4.1.7, for 100 A and a rectangular current of Θ = 120° this results in a maximum case temperature T_c = 115°C (as a cross-check). While Figure 4.1.5 is independent of the operating frequency, Figure 4.1.6 and hence Figure 4.1.7 applies for 40 to 60 Hz only. At higher frequencies, the AC thermal resistances approach the level of the DC thermal resistance, which is virtually reached at 500 Hz. To be on the safe side, Figure 4.1.6 is to be applied (unaltered) up to around 120 Hz.

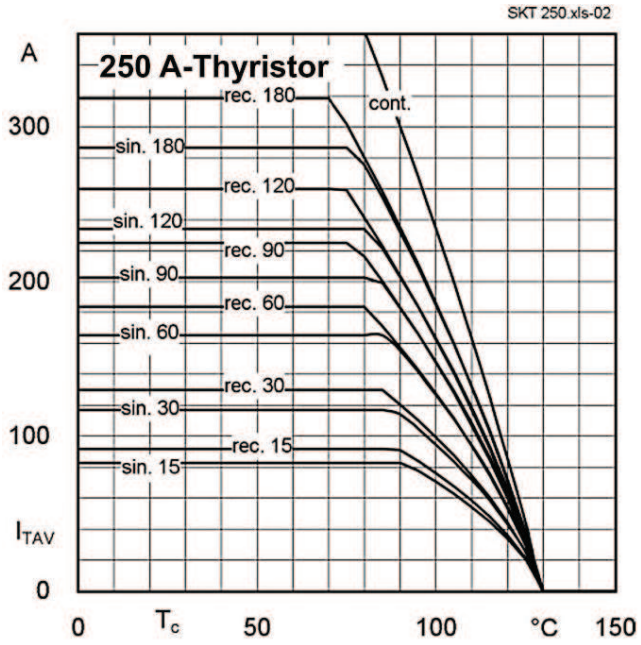


Figure 4.1.7 Mean forward current I_{TAV} as a function of the case temperature T_c for pure DC (cont.), controlled half sine waves (sin.) and rectangular pulses (rec.). Parameter: Conduction angle Θ

Thyristors in disc-type cases can have single or double-sided cooling. In accordance with this, for these thyristors the diagrams for thermal resistance as a function of conduction angle (analogous to Figure 4.1.6) have two pairs of curves for single-sided cooling (SSC) and double-sided cooling (DSS). Figure 4.1.5, in contrast, remains unaffected. Depending on the cooling, different values, which are derived from the thermal resistance diagrams, are used in the case of $R_{th(j-a)}$ only.

4.1.3.2 Operation with short-time and intermittent load

The permissible current load for short-time or intermittent operation is calculated for thyristors in the same way as for rectifier diodes (cf. chapter 4.1.2). The transient pulse thermal resistance $Z_{(th)p}$ required for calculation is obtained by adding the value obtained from the curves (example Figure 4.1.8) $Z_{(th)t}$ and the additional thermal resistance specified in the tables $Z_{(th)z}$. This additional share takes into account the pulsing of the junction temperature in line with the operating frequency.

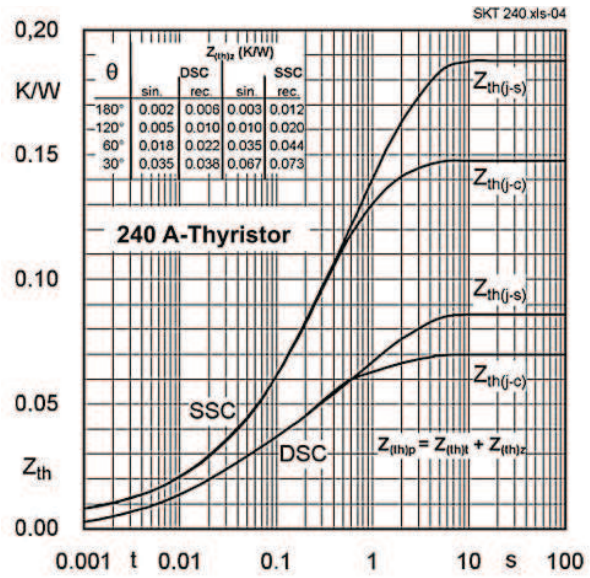


Figure 4.1.8 Z_{th} of a thyristor for SSC and DSC

4.1.3.3 Maximum surge on-state current for times below and above 10 ms

For thyristors, the same applies as for diodes (cf. chapter 4.1.2.4). In addition, it must be borne in mind that for the higher junction temperature that occurs during the surge on-state current load, thyristor controllability is lost temporarily. Thus, the thyristor behaves likes a rectifier diode, i.e. under voltage load it goes immediately into forward on-state.

4.1.3.4 Critical rate of rise of current and voltage

In addition to pure thermal rating, for thyristors care must be taken that the critical rate of rise of current $(di/dt)_{cr}$ and the critical rate of rise of voltage $(dv/dt)_{cr}$ are adhered to. The RC element that is normally connected in parallel to the thyristor, already induces a considerable di/dt. This is why the rate of rise of current caused by the rest of the circuit should lie far below the critical value. In rectifiers, even relatively small RC elements can result in a reduction of the voltage rate of rise to very low values that the thyristors can easily cope with. The same applies to a.c. power converters and circuit breakers. In inverters and especially in 4-quadrant converters, by way of contrast, the rapid drop in voltage when the thyristor is triggered causes steep voltage peeks at the thyristors of the other branches in forward direction. These voltage peaks are barely attenuated by the RC circuit since the only series resistance is the switching inductance. This is why, for such applications, thyristors with a high critical voltage rate of rise (1000 V/µs) are used.

4.1.3.5 Firing properties

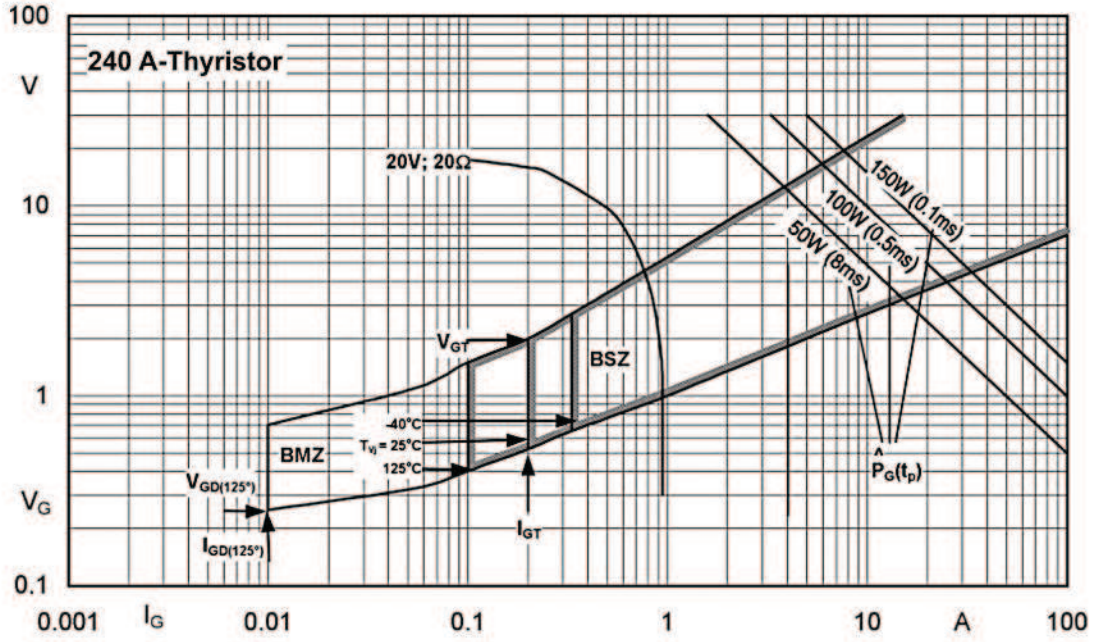


Figure 4.1.9 Gate voltage V_G as a function of the gate current I_G (stray range) showing areas of possible firing and safe firing for various virtual junction temperatures T_j.

Figure 4.1.9 shows the upper and lower limit of the area where the current / voltage characteristics lie between gate terminal and cathode terminal of the relevant thyristor type. The current and voltage of the firing pulse must be within the safe firing area, but must not exceed the power P_{GM} specified for different pulse durations t_p. Furthermore, trigger current and trigger voltage at -40°C, +25 °C and the maximum permissible virtual junction temperature, as well as the maximum permissible peak gate power dissipation P_{GM} are entered for trigger current pulses lasting 0.1 ms, 0.5 ms and 8 ms.

The trigger current actually used should be as far above the I_{GT} values entered as possible in order to ensure that the trigger process is still safe at cold temperatures. It goes without saying that the P_{GM} values are not to be exceeded. Furthermore, the rate of rise slopes for the trigger current pulses should have as steep as possible. Five times the value of I_{GT} and a rate of rise of at least 1 A/µs is recommended. For trigger pulses that lie below these values, the critical rate of rise of current $(di/dt)_{cr}$ drops drastically!

The necessary trigger pulse duration depends on the load in the main circuit. For ohmic load, a single short pulse lasting at least 10 µs is enough, since the current in the main circuit increases rapidly. Under inductive load, the current is only able to increase slowly. Normally, however, an RC element is connected in parallel to the thyristor, whose discharge current facilitates the thyristor trigger process. If this is not the case, long trigger pulses or, even better, sequences of short-time pulses are to be implemented. Further layout recommendations for trigger circuits are given in chapter 4.3.

4.1.4 Thyristor diode modules

For thyristor diode modules (SEMIPACK® components), chapter 4.1.1 (reverse voltage), 4.1.2 (rectifier diodes) and 4.1.3 (thyristors) correspondingly apply. Almost all of the data and curves contained in the catalogues apply to one thyristor or rectifier alone. The only differences relate to the choice of the necessary heat sink, because, unlike with single components, here several components are mounted on a common heat sink - at the very least the two thyristors and / or diodes integrated in one case, but very often several SEMIPACKs, i.e. four, six or even more components. The next two sub-sections explain the procedures for determining what type of heat sink to use.

Example: AC controller

A SEMIPACK SKKT 72 is to conduct a current of 120 A at maximum conduction angle as an AC controller. This results in I_{Tav} =120 A · root(2)/Pi = 52 A per thyristor. A minimum safety margin of 10% (=60 A) is recommended. Looking at Figure 4.1.10 (red line), for I_{TAV} = 60 A this results in power dissipation for the individual thyristor of P_{TAV} = 85 W (180° half sine waves). Assuming a maximum ambient temperature T_a = 40°C and a permissible junction temperature of 125°C, this results in the maximum permissible $R_{th(j-a)}$ = (125°C – 40°C) / 85 W = 1.0 K/W.

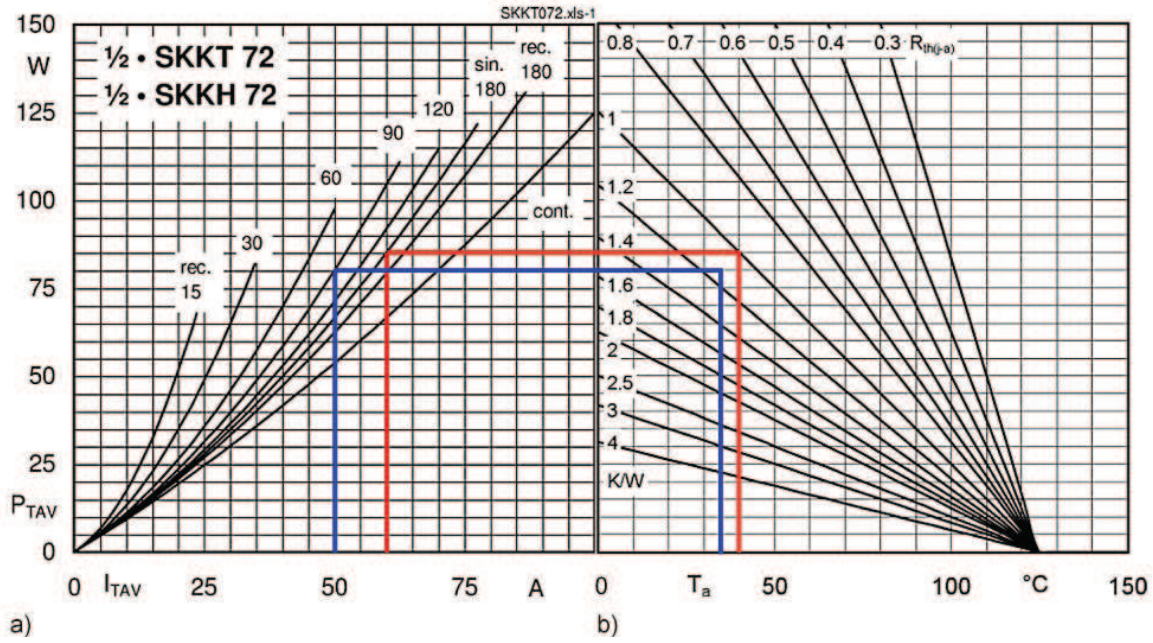


Figure 4.1.10 a) P_{TAV} as a function of the mean forward current I_{TAV} for half sine waves (sin. 180), pure DC (cont.) and for rectangular pulses (rec. 15 to 180); b) Permissible power dissipation P_{TAV} over ambient temperature T_a for different $R_{th(j-a)}$; all of this data applies to one thyristor alone.

According to the datasheet, for sinusoidal current and Θ = 180° a single thyristor has $R_{th(j-s)}$ = $R_{th(j-c)}$ + $R_{th(c-s)}$ = 0.37 K/W + 0.20 K/W = 0.57 K/W. For the heat sink, the remaining resistance per thyristor is $R_{th(s-a)}$ = 1.0 K/W - 0.57 K/W = 0.43 K/W. For 2 thyristors the resistance halves to 0.215 K/W. Thus, a heat sink with a thermal resistance of ≤ 0.215 K/W featuring a SEMIPACK (n = 1) and power dissipation of P_{tot} = 2 · 85 W = 170 W is required. As regards $R_{th(s-a)}$, one SEMIPACK is regarded as one heat source, just like a bridge rectifier (also see chapter 5.3.2.1 Number of heat sources), even though it contains several diodes or thyristors. The individual components are so close together in the case that heat loss is not evenly distributed across the entire length of the heat sink.

Example: Six-pulse fully-controlled bridge circuit

Three SKKT 72 are to deliver 135 A in a B6C circuit with a conduction angle of 90°. This means 45 A per thyristor. We will assume 50 A to allow for a safety margin. For 50 A and rectangular current with Θ = 90°, Figure 4.1.10 (blue line) results in P_{TAV} = 80 W. For ambient temperature T_a = 35°C, the resistance needed for one thyristor is $R_{th(j-a)}$ = 1.15 K/W. The values R_{th} = 0.41° K/W and $R_{th(c-s)}$ = 0.2 K/W are to be subtracted from this resistance value. For the heat sink, this leaves $R_{th(s-a)}$ = (1.15 - 0.41 - 0.20) / 6 =0.09 K/W. Thus, the heat sink requirement is: Resistance $R_{th(s-a)}$ =0.09 K/W for n = 3 heat sources. This is easier to achieve if enhanced air-cooling measures are used. A possible heat sink here would thus be P 3/300 F featuring a 120 m³/h fan.

4.1.5 Bridge Rectifiers

Bridge rectifiers are components which have every branch of a rectifier circuit in a single, compact case. Bridge rectifiers exist from a few amps to several hundred amps in different case types.

With a few exceptions, the heat losses are dissipated via a base plate or the DBC to a cooling plate or a heat sink. The necessary $R_{th(s-a)}$ of this cooling device plus $R_{th(c-s)}$ is specified as parameter $R_{th(c-a)}$ in Figure 4.1.11. For a given output DC current I_D and a certain ambient temperature T_a, this value can be determined directly from a graph such as Figure 4.1.11. Figure 4.1.11a shows total power dissipation P_{Vtot} (mean value) of a bridge rectifier as a function of the output DC current I_D. The R curve applies to resistive load, L for inductive load and the C curve for capacitive load for capacitance C_{max} specified in the datasheet for the charge capacitor. This process is the same as that described in chapter 4.1.2.1 for power diodes; the only difference is that here the values in the diagram refer to the compact rectifier as a whole.

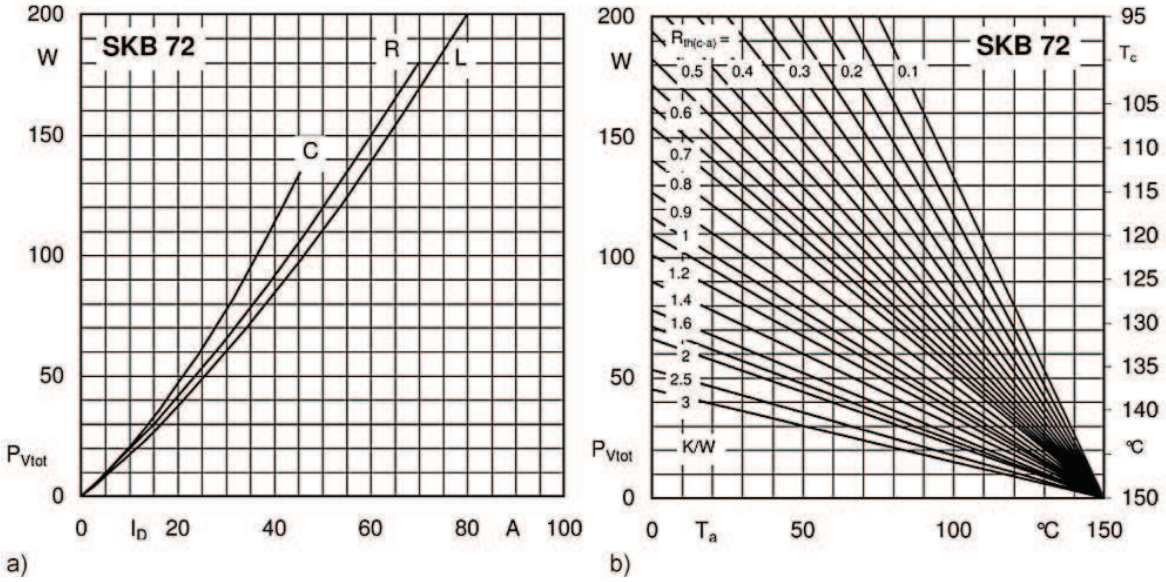


Figure 4.1.11 a) Power dissipation P_V of a silicon compact rectifier as a function of the rated DC current I_D for C, R and L load; b) Case temperature T_c over ambient temperature T_a for different $R_{th(c-a)}$

For the power dissipation P_{Vtot} (left Y-axis), the case temperature T_c is permissible (right Y-axis). A reduction in DC current to $I_N = 0.8 \cdot I_D$ is recommended.

4.1.6 SemiSel dimensioning software

General information on how to use this software was provided in chapter 5.2.3. To calculate the power dissipation of diodes and thyristors, SemiSel uses the equations given in chapter 4.1.2. The on-state characteristic is approximated using substitutional straight lines. In rectifier components, these values can be determined between the points rated current and triple rated current. Unlike IGBT, diodes and thyristors in bridge circuits are used far above their rated DC current (I_{TAV} / I_{FAV}), which is why a precise approximation in this area is particularly interesting. We recommend using maximum values for the calculations. This results in the mean losses for the component (similar to thyristors with the index "T").

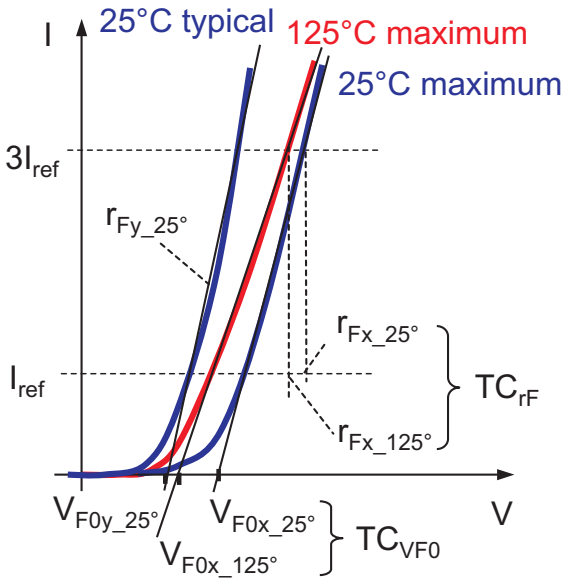


Figure 4.1.12 Approximation of on-state characteristic using substitutional straight lines for typical (y) and maximum (x) values

Current input (Figure 4.1.13) is done as circuit current (I_{out}) and is converted (proportionately) to the individual components. For rectifiers, ideal smoothed current is assumed. This can, however, be changed by increasing the effective value or the form factor. The form factor refers to the component current. The on-state characteristic used to calculate losses is temperature-dependent, which is why the software determines the actual losses iteratively by factoring in self-heating.

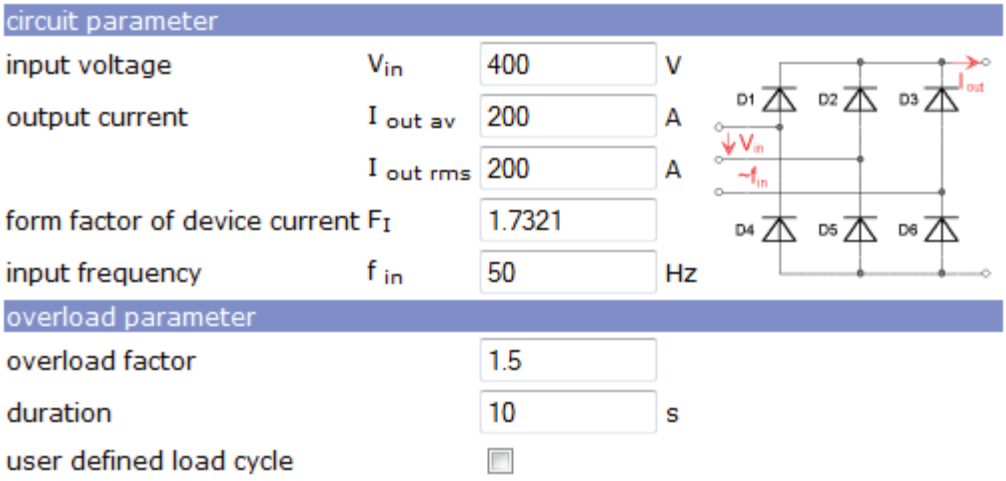


Figure 4.1.13 Example of parameter input for a rectifier bridge in SemiSel

The mean junction temperature T_j is calculated with the help of the thermal resistances:

$$T_j = P_{FAV} \cdot R_{th(j-s)} + R_{th(s-a)} \cdot \sum_n P_n + T_a$$

Where P_n represents the individual component losses on a common heat sink. The temperature ripple is not calculate using the line frequency. In diode rectifiers, the temperature ripple is taken into account in the recommended minimum reserve of $T_j = T_{j(max)}$-10 K. In thyristor circuits with very short current conduction times and very high amplitude, an additional check should be performed to ensure that $T_{j(max)}$ is not exceeded.

Of particular interest is the calculation of the losses and maximum temperatures for overcurrent (in relation to the rated current) lasting a certain time. Higher load simply results from increased power dissipation and consequently a higher junction temperature. The only thing that is different in the calculation as compared to rated conditions, is the fact that calculations are performed with a thermal impedance rather than thermal resistances:

$$T_j(t) = P_v(t) \cdot Z_{th(j-s)}(t) + Z_{th(s-a)}(t) \cdot \sum_n P_{v\_n}(t) + T_a$$

The program breaks down the overload pulse into time-discrete points and calculates the temperature characteristic up to the n-th point in a second iteration loop, always starting from t = 0. The result is time-dependent temperature characteristics for the component. For complicated load conditions, a load cycle in tabular form may be given (user-defined load cycle).

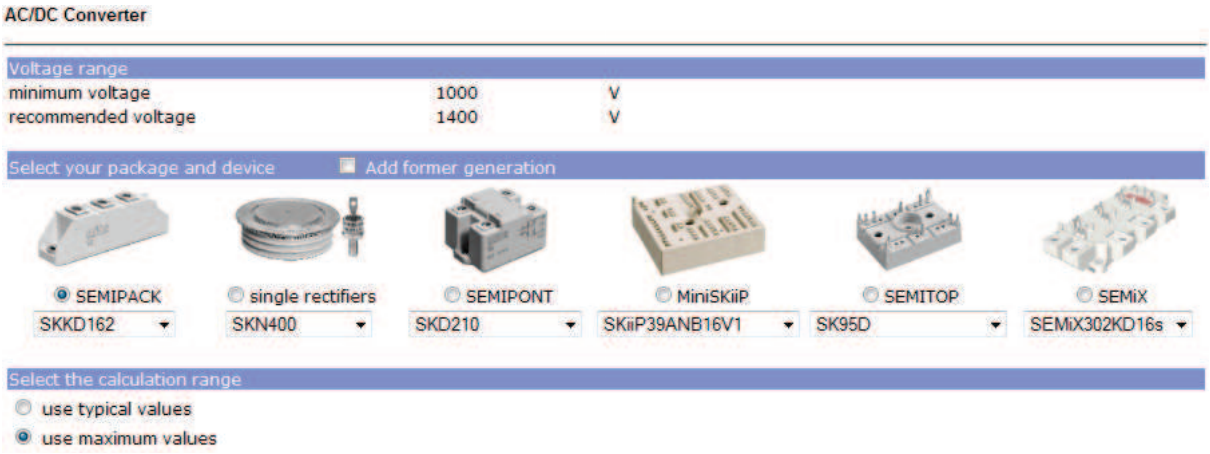


Figure 4.1.14 Selecting case type and current class for the available components (filter: voltage class)

Once a suitable component has been selected and the cooling conditions specified, the user obtains the individual losses per component and the sum of all components mounted on the heat sink, as well as the chip and heat sink temperatures.

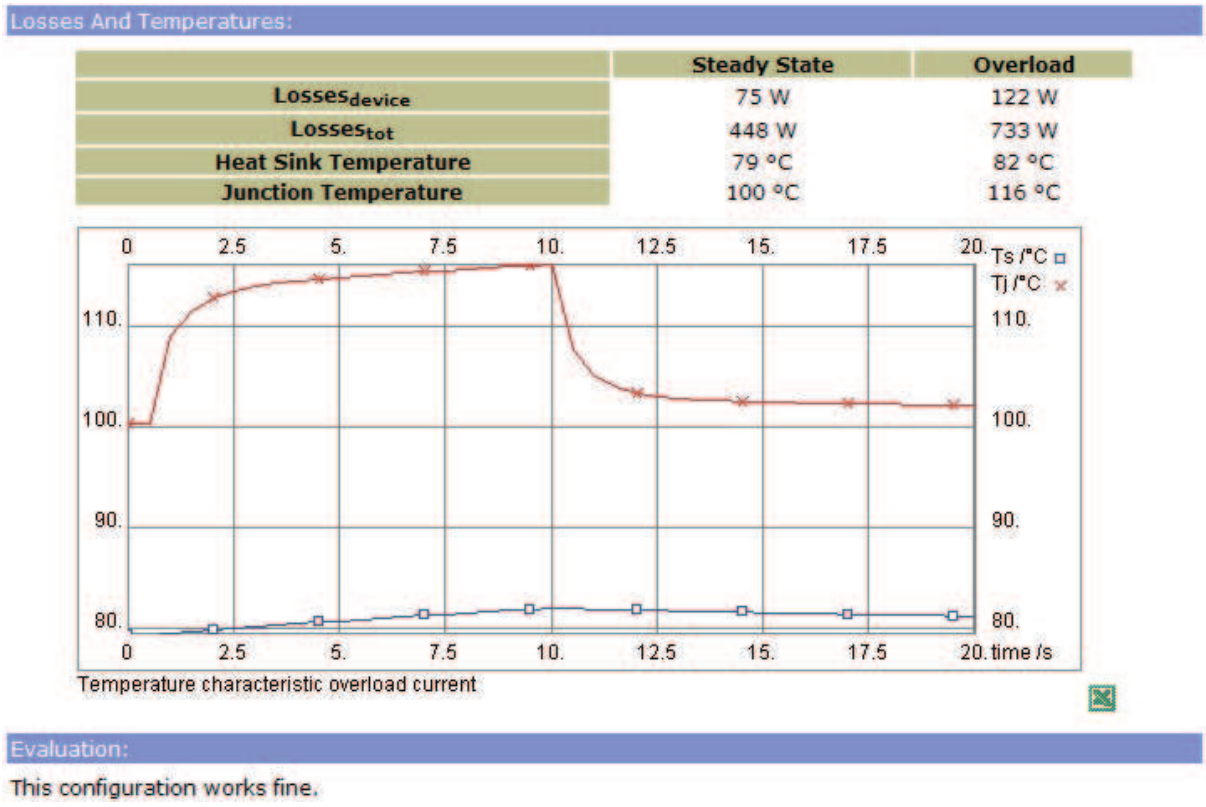


Figure 4.1.15 Results of loss and temperature calculations

4.2 Cooling rectifier components

This section looks at the specifics of rectifier cooling. This relates in particular to non-isolated discrete components. The statements made in chapter 5.3 with regard to IGBT modules apply likewise to rectifier modules with forced air cooling or water cooling.

4.2.1 Cooling low-power components

In semiconductors with low power ratings, i.e. especially in all those that are suitable for self-supporting PCB soldering, it is generally sufficient to dissipate the heat via the case surface and via the terminals. The tracks on the PCB that are used to solder the connections can also play a big role in dissipating the heat losses. For this reason, the junction to ambient resistances $R_{th(j-a)}$ specified for low-power components only apply on condition that the component is located directly on a PCB and that the tracks are of normal breadth (2-3 mm) and feature normal tin-plating across their entire area. Components with wire connections can also be integrated at a distance of 3-25 mm from the PCB. The thermal resistance R_{th} increases in proportion to the length of the wires. On the other hand, the thermal resistance R_{th} can be reduced by 25 to 30% by using extremely wide tracks with tin plating across their entire area. In this case, the component must be placed on to the PCB directly.

Low-power semiconductor devices with block-shaped plastic cases are sometimes mounted on to a cooling plate or chassis plate using a clamp. The permissible current load for this plate (with a certain minimum size) is provided in the datasheet. Sometimes, the thermal resistance $R_{th(j-r)}$ between the junction and a reference point r is specified at one of the terminals. During actual operation, the temperature T_r at these points and the power dissipation P that occurs in the component can be measured in order to check that the virtual junction temperature T_j does not exceed the maximum permissible value. The following applies: $T_j - T_r = P \cdot R_{th(j-r)}$. Another possibility is to solder such components at one or both terminals to small copper cooling plates (which have to feature natural isolation), calculated as described in chapter 4.2.2, in doing so achieving highly effective cooling otherwise only possible with metal-encased components. Finally, some low-power components are equipped with fixed assembly lugs or metal bases (e.g. TO220), which can either be connected to one of the terminals or isolated internally. For such components, the junction to "case" thermal resistance $R_{th(j-c)}$ is given in the datasheet; here, the "case" is the aforementioned assembly lug or the metal base. Such components are mounted, like metal-encased components, on cooling plates, heat sinks or cooling profiles (see chapters 4.2.2 to 4.2.4).

4.2.2 Cooling plates

Smallish power semiconductors (up to around 15 A mean forward current) can be mounted onto cooling plates in order to dissipate the heat losses. If a terminal is electrically connected to the component case, the cooling plate has to be electrically insulated. If, however, the case (which can also be a plastic case with metal base or metal mounting plate) is isolated from the electric connections, the cooling plate may be, for example, a part of the equipment case or of the assembly chassis. Figure 4.2.1 and Figure 4.2.2 give the cooling plate thermal resistances for different materials and material thicknesses in dependence of the area of the cooling plate. Here, the requirement is that the cooling plate is made of bare metal and approximately square (ratio of both edge lengths no greater than 2:3). The component sits in the centre of the plate as a point-contact source; the contact surface of the component is relatively small in relation to the cooling surface. If the shape differs greatly from a square, Figure 4.2.2a is to be taken into account. The mounting position of the plate plays a lesser role, provided just one stream of air can develop along the plate. Generally speaking, vertical mounting tends to have a lower thermal resistance R_{th}, while a horizontal position would obstruct the airflow and thus increase the resistance. If the plate is coated black, the thermal resistance R_{th} will drop by around 15% due to the improved heat radiation.

In order to determine the permissible power dissipation P, the thermal resistance of the cooling plate $R_{th(s-a)}$, the thermal resistance between component and cooling plate $R_{th(c-s)}$ and the internal component resistance $R_{th(j-c)}$ are to be added together. The following thus applies:

$$P = \frac{T_{vj} - T_a}{R_{th(j-c)} + R_{th(c-s)} + R_{th(s-a)}}$$

T_{vj} is the max. permissible virtual junction temperature,
T_a is the maximum expected temperature of the air flowing towards the cooling plate.

Here, the requirement is that no further heat generating components are attached to the cooling plate (otherwise the power dissipation P of these components must be factored in) and that the cooling plate is not additionally heated by heat radiation from adjacent heat sources.

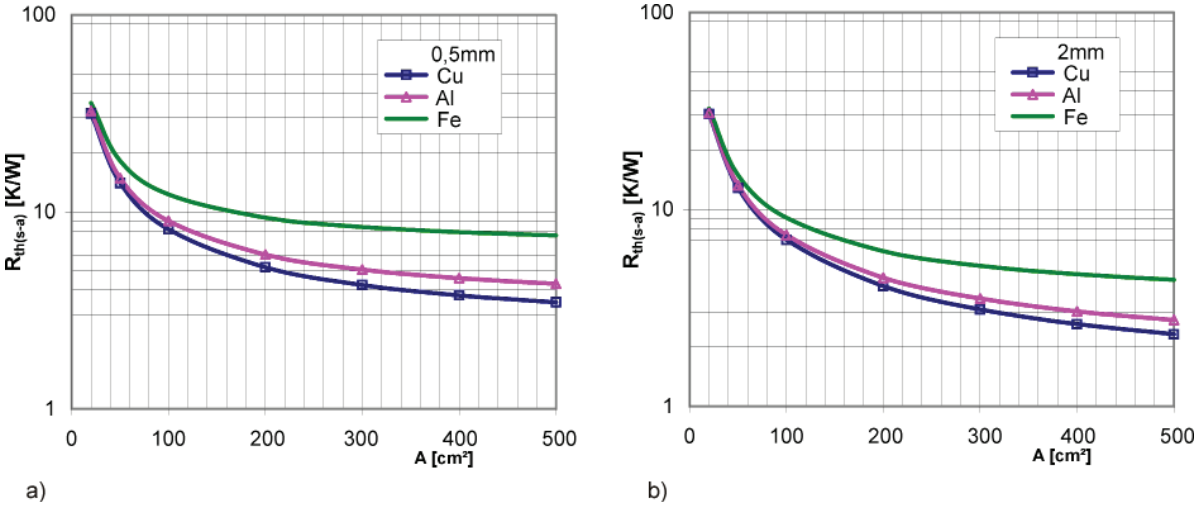


Figure 4.2.1 $R_{th(s-a)}$ for square bare cooling plates made of steel (Fe), aluminium (Al) and copper (Cu) over the area A for 0.5 mm plate thickness (left) and 2 mm plate thickness (right) for unobstructed airflow across the surface and approx. 40 K temperature difference $\Delta T_{(s-a)}$

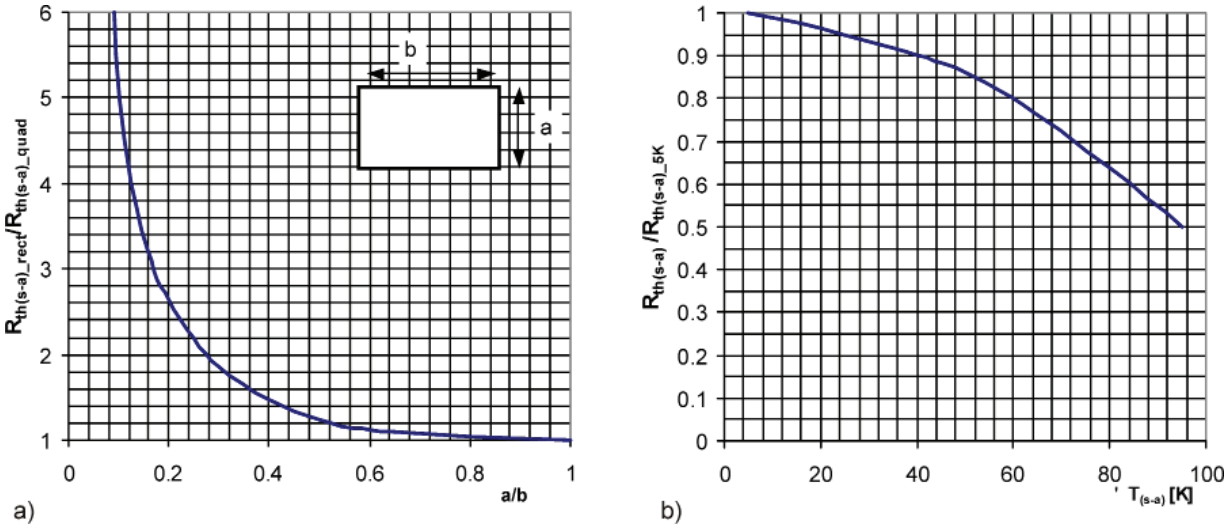


Figure 4.2.2 a) Relative change in $R_{th(s-a)}$ for non-quadratic cooling plates (r) in dependence of side length ratio a/b; b) Relative change in $R_{th(s-a)}$ of a cooling plate as a function of the temperature difference between cooling plate (T_s) and the inflowing air (T_a) in relation to a value at $T_s - T_a$ = 5 K

Figure 4.2.2b shows the influence of the cooling plate / air temperature difference on the thermal resistance R_{th} of the cooling plate. As the temperature difference increases, the heat dissipated to the environment by the cooling plate becomes more intensive; in other words, the thermal resistance of the cooling plate $R_{th(s-a)}$ drops.

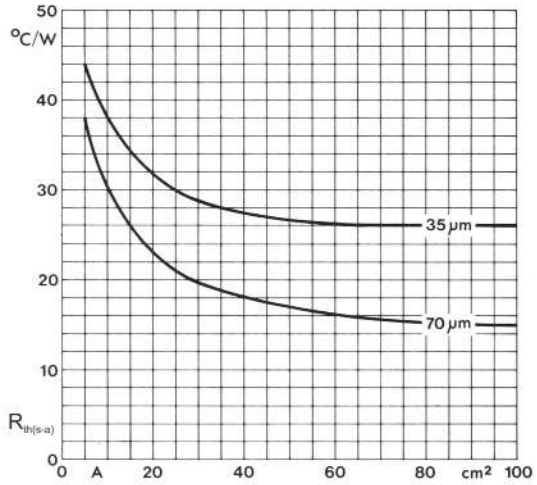


Figure 4.2.3 $R_{th(s-a)}$ of a 1.5 mm thick PCB copper lamination, single-sided lamination, layer thickness 35 µm and 70 µm, as a function of the area A. Any mounting position, provided unobstructed airflow across the entire surface is ensured.

PCB copper laminating can be seen as a cooling plate of sorts. In large -area designs with sufficient layer thickness, this can contribute substantially to heat dissipation. Figure 4.2.3 shows the thermal resistance of copper laminating as a function of the area, again for a roughly quadratic shape and low temperature difference to air. This applies to natural cooling air convection. The use of a fan can improve the cooling effect considerably. What must be noted is that no graphs can be given here owing to the numerous unknown influences. The only way to obtain reliable data on the thermal resistance of a given cooling plate for enhanced air cooling is to perform measurements on a device in an application-like setup.

The graphs shown in Figure 4.2.1 to Figure 4.2.3 apply on condition that the contact surface of the component is relatively small (almost point-contact) in relation to the size of the cooling plate. The problem, however, is that many components have relatively large contact surfaces. Provided that the use of thermal paste during assembly can ensure homogenous heat transfer to the cooling plate, this will result not only in low thermal resistance $R_{th(c-s)}$, but also low cooling plate thermal resistance R_{th}, especially for relatively thin plates which have low heat conductivity to the outer edges. In fact, owing to the large contact surface, the outer edges of the plate are better included in the heat dissipation process. This influence can be seen in Figure 4.2.4.

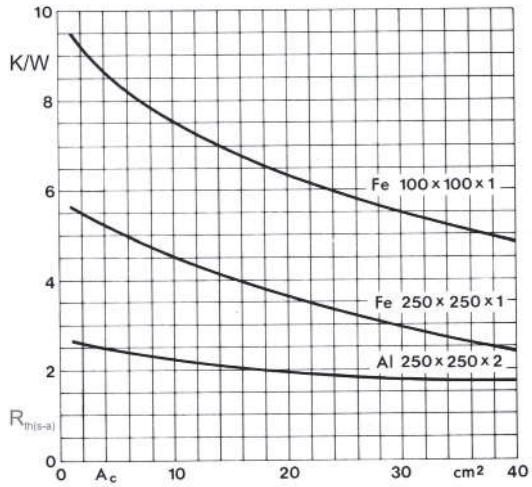


Figure 4.2.4 $R_{th(s-a)}$ of cooling plates with the given dimensions (in mm) made of steel (Fe) and aluminium (Al) as functions of the contact surface area A_c of the heat generating component for low cooling plate / air temperature difference. The cooling air must be able to flow unobstructed across the entire surface.

4.2.3 Heatsinks

For higher power semiconductor components (e.g. more than 15 A), cooling plates are no longer sufficient to fully utilise the current carrying capacity. Here, heat sinks or cooling profiles (fins) made of aluminium (in rare cases copper, too) with strongly ribbed surfaces are used (Figure 4.2.5). This increases in area for convection and heat radiation, spreads the heat flow, and attenuates transient thermal processes.

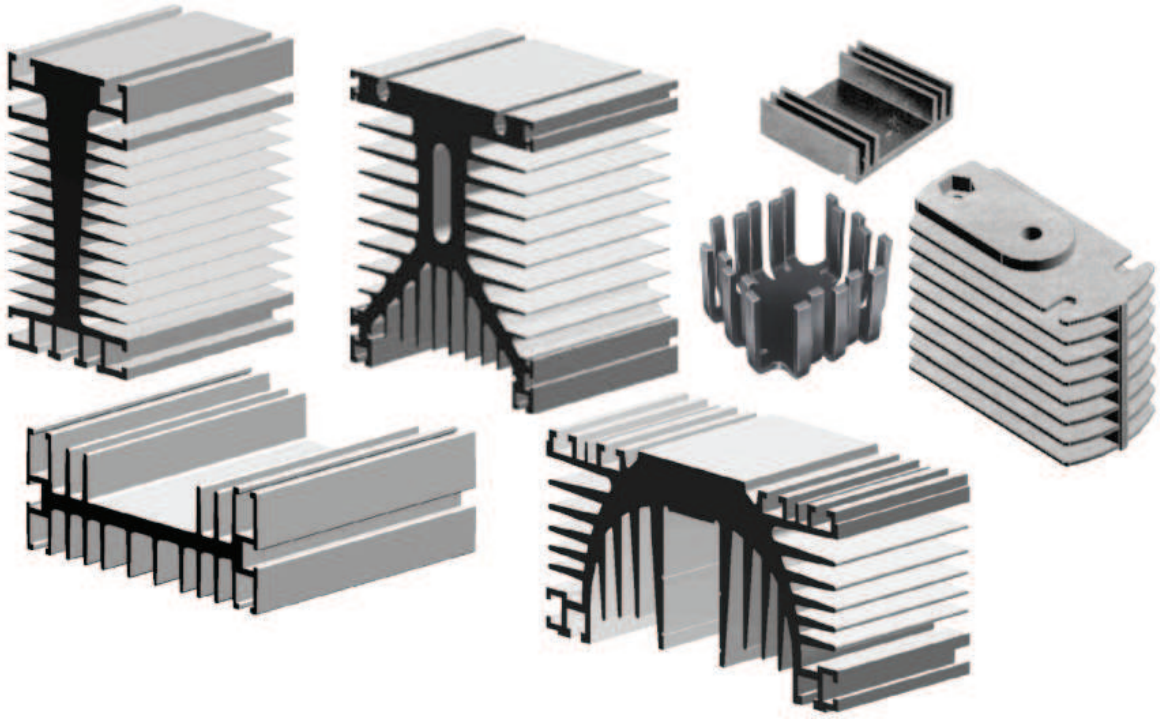


Figure 4.2.5 Examples of heat sinks and extruded cooling profiles for discrete power semiconductors, modules and disc cells.

Such heat sinks are suitable both for natural convection (heat is dissipated by the natural flow of air, i.e. by the rise of the heated air as a result of gravity) and forced air cooling (cooling air is moved by a fan), or are optimised for one of these types of cooling. Heat spread in the material has a considerable influence on the thermal efficiency of the heatsink. Therefore, optimized dimensioning is important for root thickness, number of fins, fin height and fin thickness:

- The root of a heat sink is the unfinned part of the mounting surface for the power components where the heat is spread.
- Heat dissipation takes place substantially via the fins of an air-cooled heat sink by means of radiation and convection.

For convection, the "ribbing" should be as high as possible in order to increase surface area, provided it does not hamper air flow speed and cause the heat transfer coefficient α to drop too much. Parallel fin areas, in contrast, obstruct thermal radiation, rendering them virtually ineffective. This is why heat sinks feature actinoid or radial fin arrangements to optimise heat radiation.

The thermal resistance of a heat sink is not a fixed parameter. In the case of air self-cooling, this value depends on the temperature difference between heat sink and air, i.e. on the power dissipated here. If power dissipation is increased, the heat sink is heated up better, i.e. the effective heat exchange areas are increased (Figure 4.2.6). If, for space reasons, several heat sinks are to be positioned on top of one another, care is to be taken that, in natural air cooled systems, the upper layers are fed warmer air than the others (cf. chapter 5.3.7 Thermal series connection). In the case of forced air cooling, the air heats up less strongly whilst flowing through the heat sink, meaning that the air can flow through several stacked heat sinks. Please note, however, that in this case the flow resistance increases, reducing the efficiency of the fan.

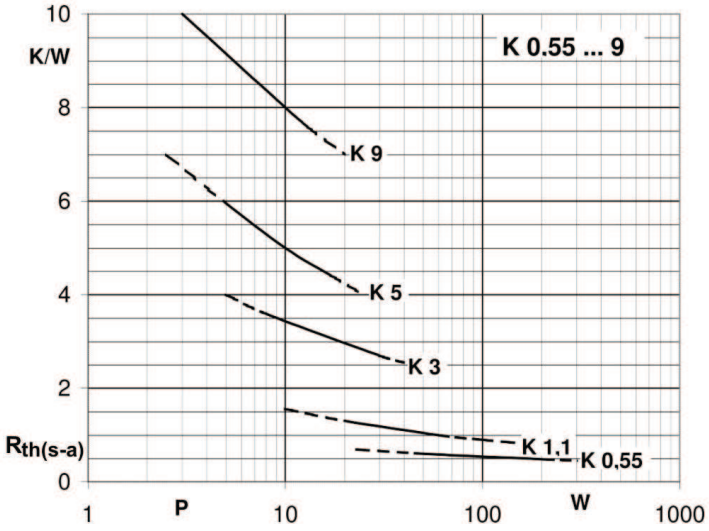


Figure 4.2.6 $R_{th(s-a)}$ in dependence of the dissipated power for several standard heat sinks

If the metal case is connected to one of the electric terminals of the semiconductor, the heat sink is included in the electric circuit, too. This means it has to be isolated; and permanent, good electric contact must be ensured. To this end, a nickel-plated copper plate is to be inserted between the semiconductor component and the aluminium heat sink; this plate serves as the electrical connection. If the heat sink itself is used as an electric conductor, the aluminium can be protected from contact corrosion using nickel or chrome plating. It goes without saying that before assembly, any existing aluminium oxide layers have to be removed from the assembly surface.

In addition to cast heat sinks, extruded profiles made of AlMgSi are often used to cool power semiconductors. Besides manufacturing-related benefits, these have the added advantage that, since you can cut any desired length from a long bar, the thermal resistance of the heat sink can be "adapted" to a required value to some extent. Figure 4.2.7 shows the thermal resistance R_{th} of a heat sink profile in various lengths for a centrally mounted heat source. Longer heat sink profiles may also be equipped with several semiconductor components. With non-isolated components, the possibilities are inherently determined by the circuit chosen; only components with the same potential may be mounted on a common heat sink, e.g. the cathodes on + DC of a bridge rectifier.

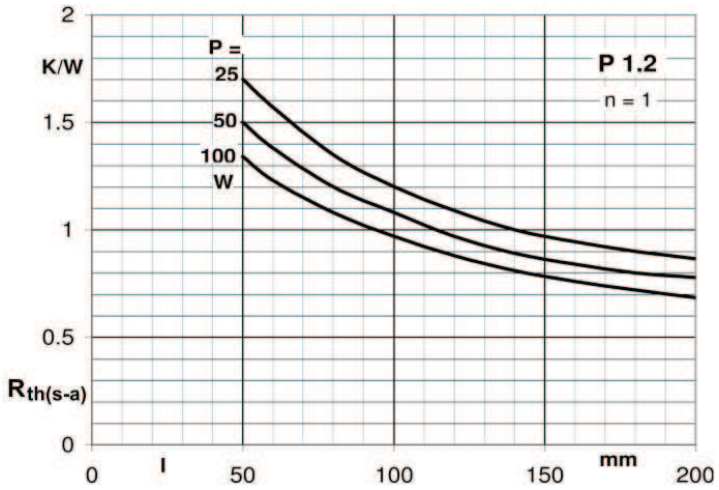


Figure 4.2.7 $R_{th(s-a)}$ for various lengths of P 1.2 heat sink with one centrally mounted component and various power dissipation levels P for natural cooling

To determine the thermal resistance of the heat sink profile equipped with several components, the heat sink can be virtually sawn and the R_{th} determined for each constituent part. If the components are distributed evenly along the length of the profile, this results in better heat distribution. This causes the value $R_{th(s-a)}$ to decrease in relation to the value which would result if the entire power

dissipation were concentrated on one single heat source. For the example in Figure 4.2.7 with 2 components of 50 W each on a common 200-mm-long heat sink, this would result in:

$$R_{th(s-a)} = \frac{R_{th(s-a)}\,(100\,\text{mm},\,50\,\text{W})}{2} = \frac{1{,}1\,\text{K/W}}{2} = 0{,}55\,\text{K/W}$$

By way of comparison, a single component with 100 W on a heat sink of the same length (200 mm) has $R_{th(s-a)}$ = 0.7 K/W. This effect is particularly evident with very long profiles and enhanced air cooling. The datasheets of many heat sink profiles contain diagrams which show the thermal resistance $R_{th(s-a)}$ as a function of the profile length and power dissipation for n components mounted on the heat sink profile.

To achieve double-sided cooling in disc cells and consequently half of the internal thermal resistance $R_{th(j-s)}$, the component is integrated between two heat sink profiles. The clamping device must be designed such that at least one of the heat sink fins is moveable so as to ensure that pressure distribution across the entire surface of the disc cell is even (Figure 4.2.8). For more details, see the assembly note in chapter 6.4.

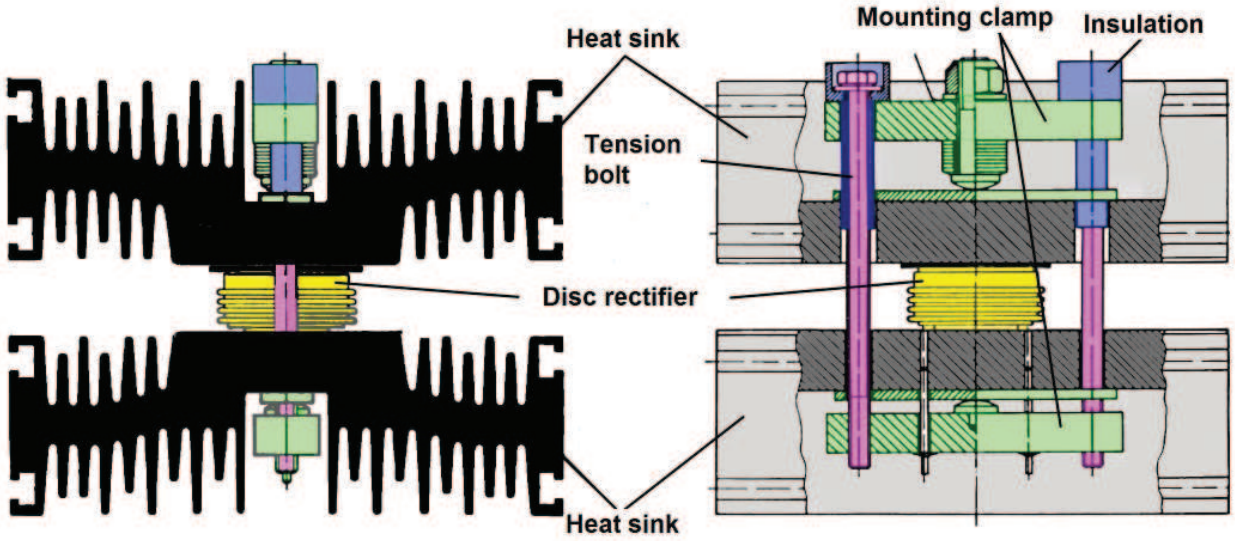


Figure 4.2.8 Double-sided cooling of disc cell using two heat sink profiles

4.2.4 Enhanced air cooling

For higher power dissipation (e.g. greater than 50 W) enhanced air cooling, which involves blowing the air through the heat sink profile using a fan / blower, is frequently used. Depending on the air flow volume, this causes a reduction in the heat sink thermal resistance R_{th} by between one third and one fifteenth and is virtually independent of the power dissipation. Coating or blackening the heat sink does not bring about any further improvement when forced cooling is used. The value $R_{th(s-a)}$, however, strongly depends on the volume of air flowing within the given time V_{air}/t or the mean cooling air velocity v_{air} (Figure 4.2.9).

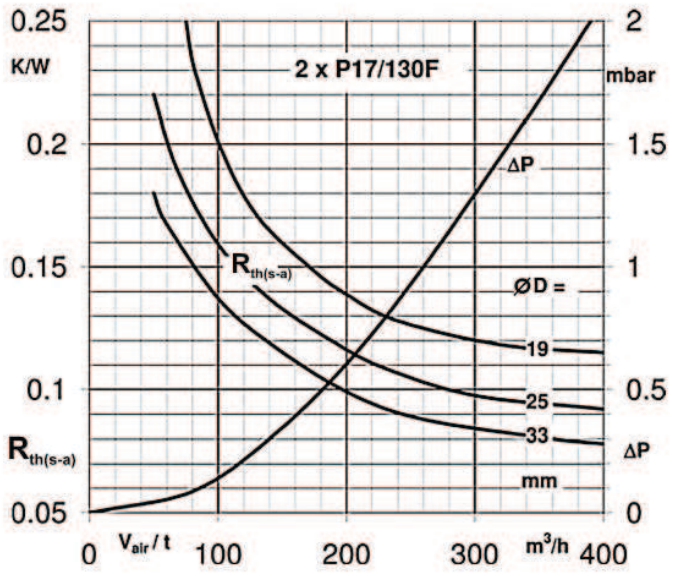


Figure 4.2.9 $R_{th(s-a)}$ of P17 heat sink of 130 mm in length for disc cells with double-sided cooling and pressure drop ΔP between air entry and exit as a function of the air volume in the given time V_{air}/t. ØD is the diameter of the contact element of the disc cell.

The mean cooling air velocity multiplied by the entry area A results in the cooling air volume per unit of time:

$$V_{air} \cdot A = \frac{V_{air}}{t} \left[\frac{m^3}{h}\right]$$

The requirement here: laminar flow. Between the fins of the heat sink, however, the air flow is normally turbulent. This is of advantage since this helps improve the heat transfer from the heat sink to the air. If there is turbulence, it won't be possible to obtain an accurate reading for the mean cooling air velocity. This is why this the specification of this value is of limited use only. To obtain the thermal resistance R_{th} of an intended heat sink arrangement with a certain fan, the first step is to map the specified pressure difference graph for the individual heat sinks Δp as a function of the cooling air volume V_{air}/t (Figure 4.2.9) into an equivalent curve for the entire arrangement. Any other pressure drop, e.g. caused by a filter, must also be taken into account. The fan characteristic is to be drawn into the same diagram. The point of intersection constitutes the pressure difference and air volume that will occur in actual application (Figure 4.2.10). The corresponding $R_{th(s-a)}$ can be derived from the heat sink graph (Figure 4.2.11).

If several components are mounted on a common heat sink (heat sink profile), the total power dissipation of all components and the thermal resistance R_{th} of the entire heat sink for n evenly distributed heat sources, as resulting from the air volume V_{air} / t derived from the point of intersection of the fan characteristic and heat sink characteristic, must be factored in (Figure 4.2.10).

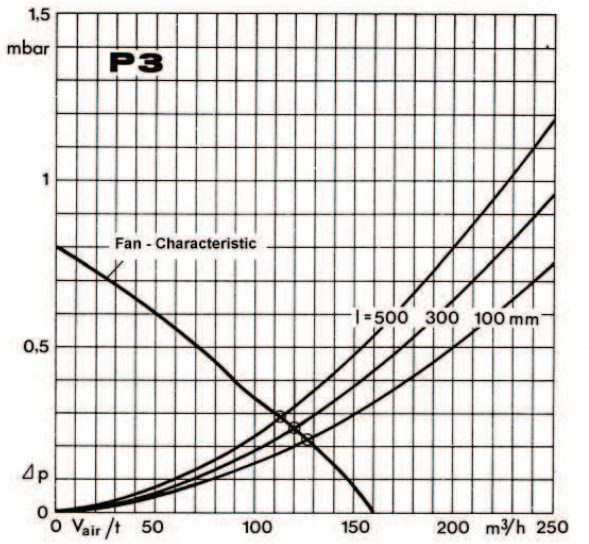


Figure 4.2.10 Diagrams showing pressure drop ∆p for different lengths l of P3 heat sink as a function of air volume V_{air}/t, as well as the volume of air moved by the fan as a function of the negative pressure (fan characteristic). The points of intersection constitute the resulting volume of air for the given combination of fan / heat sink profile.

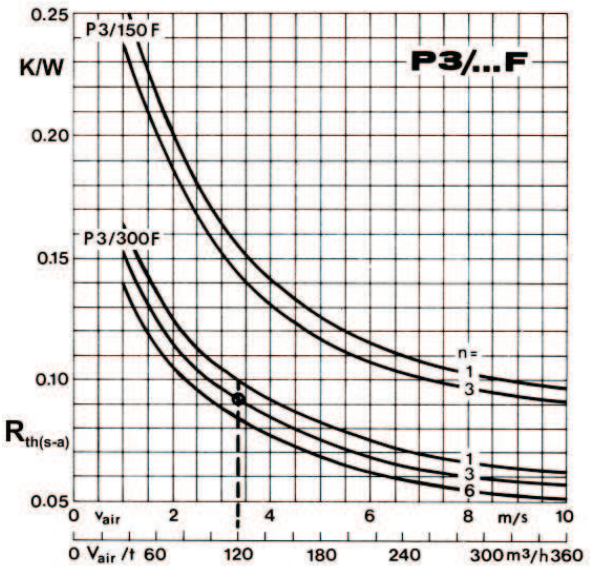


Figure 4.2.11 $R_{th(s-a)}$ for P3 heat sink profile in different lengths, equipped with n = 1 - 6 components, as a function of the air volume V_{air}/t or air velocity v_{air}

For an air volume of 120 m³/h, as derived from Figure 4.2.10 for the 300-mm-long heat sink profile with fan and n = 3, the thermal resistance $R_{th(s-a)}$ = 0.093 K/W.

With enhanced cooling, it is important to ensure that the air forced by the fan actually flows through (i.e. between) the fins of the heat sink. Larger spaces in between, which might be necessary for isolation reasons, should therefore be filled or covered.

4.2.5 Disc cells: water cooling

In liquid cooling systems, the heat transfer medium most commonly used is water or a mixture of water and anti-freeze; in some, rarer cases electrical insulating oil is used. Water can either form a closed circuit and be air-cooled by means of a heat exchanger, or fresh water is used which runs off after flowing through the cooling unit. Deionised water, which is characterized by low electric conductivity, can be used in closed circuits (cf. chapter 5.3.5.2). Freshwater has good natural electric conductivity. For this reason, in freshwater cooling systems for non-isolated components, sufficiently long water columns have to be used between the intake / drain which is located at the earth potential and the live cooling members, as well as between the cooling members themselves. This is necessary to keep the leakage currents small. And yet, electrolytic (material) removal and accumulation effects cannot be avoided. If need be, sacrificial protection can be used. This sacrificial anode - rather than the heat sinks - would corrode and would have to be replaced at given intervals.

4.3 Drivers for thyristors

The link between the electronic control components of a converter and the thyristors is the driver (driver circuit). The purpose of the driver is to generate suitable current pulses in order to drive the thyristors; the frequency, phase length, sequence, etc. of these pulses are affected by the signals delivered by the control electronics. As the thyristors in a converter circuit normally have different potentials (with differences of several hundred volts), the outputs of the driver device have to be isolated from one another. This is achieved with pulse transformers. A circuit diagram that includes a transformer is shown in Figure 4.3.1a; Figure 4.3.1b shows an equivalent circuit, while Figure 4.3.1c shows a typical drive signal.

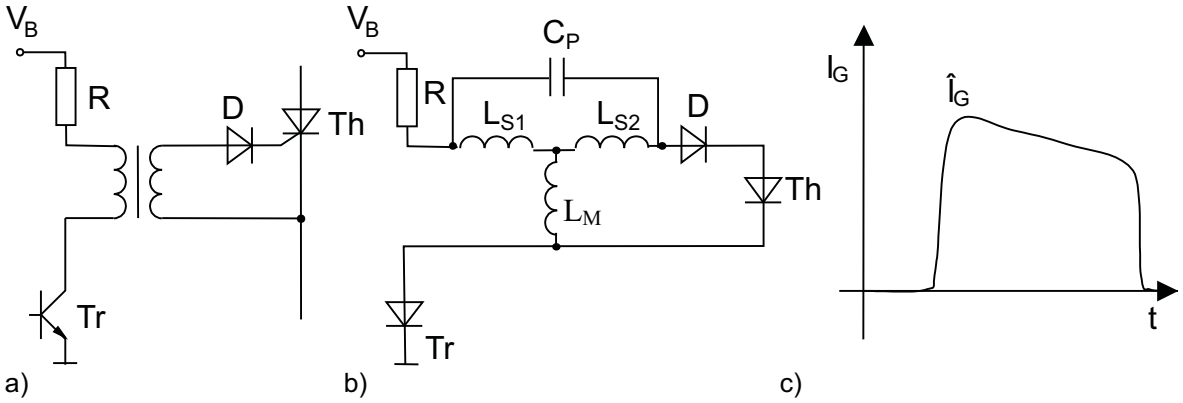


Figure 4.3.1 a) Drive circuit, b) Equivalent circuit; c) Time characteristic of drive signal

What is important is that positive trigger pulses are ruled out while the thyristor is poled in reverse direction (cathode potential is more positive than the anode potential). Such pulses will increase leakage current i_R and consequently the off-state power losses in the thyristor and may lead to overheating of the component.

4.3.1 Drive pulse shape

To ensure that the thyristor is triggered reliably and safely if the main current increases steeply (cf. "Critical rate of rise of current" in chapter 3.2.5), a trigger pulse with sufficient current amplitude ($\geq 5 \cdot I_{GT}$) and rate of rise (≥ 1 A / µs) is needed. Even if the current in the commutation circuit rises relatively slowly, the RC element connected in parallel for overvoltage protection will often mean that a fast-rising discharge current is driven through the thyristor at every trigger. Thus, we recommend that you always use sufficiently strong and steep drive pulses. This is particularly important for thyristors connected in parallel or series, since strong and steep drive pulses will improve synchronous triggering significantly. The exponential current rise is determined by the stray inductance of the pulse transformer L_S.

$$\frac{di}{dt_0} = \frac{V_B}{L_{S1} + L_{S2}}$$

where V_B is the driver supply voltage

To determine the resultant peak current for a driver with known values for short-circuit current ($I_K \sim V_B/R$) and no-load voltage ($V_0 \sim V_B$), the output characteristic determined from these values is entered into the trigger current / trigger voltage diagram for the relevant thyristor (e.g. Figure 3.2.22). In Figure 4.3.2 the same diagram is shown in a linear scheme for better understanding.

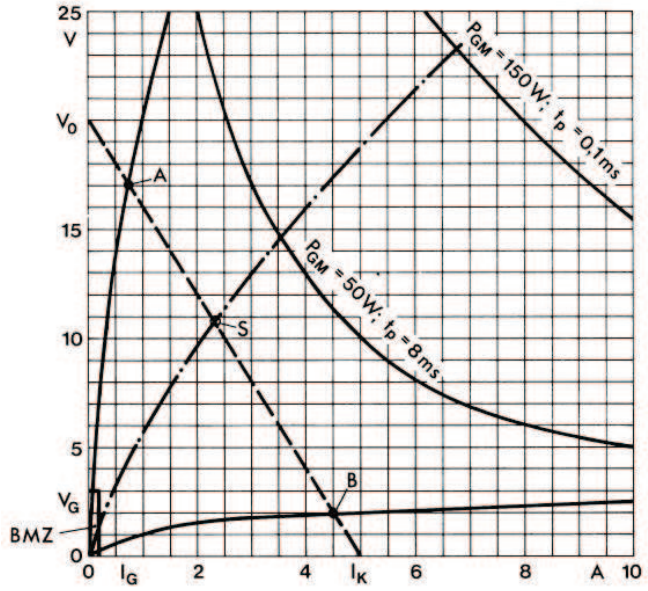


Figure 4.3.2 Gate current (I_G) – gate voltage (V_G) characteristic of a thyristor in linear scheme; dotted output characteristic, V_0 – no-load voltage and I_K – short-circuit current of the driver device; dash-dotted output characteristic of the control terminal – cathode of a typical thyristor

The actual input characteristics for the individual thyristors of the given type lie between the limiting characteristics in the diagram (dash-dotted line). Accordingly, the possible points of intersection with the output characteristic of the driver device lie between points A and B. The point of intersection of S with the output characteristic of the driver device results from the resulting drive pulse data, e.g.: 2.3 A; 10.7 V. The minimum duration of the drive pulses is 10 µs. In most cases, the latching current given in the datasheets applies to this pulse duration, too. The minimum trigger current and the latching current decrease for longer drive pulses.

For rectifiers with negative voltage, each thyristor cannot trigger until the instantaneous terminal voltage is higher than the negative voltage instantaneous value. Therefore, in order to achieve safe and reliable commutation, relatively long-lasting drive pulses are needed. An extreme cases is the AC converter under inductive load. Owing to phase displacement between current and voltage, a pulse duration of 180°- α is necessary, i.e. at 50 Hz for up to 10 ms. It goes without saying that the duration of the drive pulse should not be made unnecessarily long, since in combination with the necessary amplitude, this will lead to substantial control losses that then have to be factored in to the total thyristor losses. In addition, the maximum gate power dissipation P_{GM} contained in Figures 3.2.22 and 4.3.2 may not be exceeded under any circumstances. Otherwise the thyristor may be destroyed. Having said that, power dissipation values that lie well below these maximum values still have to be taken into account in thyristor dimensioning, as described in chapter 4.1.3.1. For the example above, P_v = 2.3 A · 10.7 V = 24.6 W.

What is more, the more power is needed, the more complex the driver unit becomes. For the driver transformer, long pulse duration means larger voltage / time area, i.e. a larger (and hence more expensive) driver unit. The pulse length of the usable driver signal is determined by the main inductance of the transformer.

$$i = \hat{I}_G \cdot e^{\frac{-t}{L_H/R}}$$

The main inductance of the transformer is determined by the permeability of the core material and is temperature-dependent. Very often the voltage / time area Vdt [µVs] is also given; this can then be used to calculate the maximum pulse duration. Figure 4.3.3 shows a typical characteristic for transformer voltage. The voltage / time area up to the saturation point is Vdt = t_p * $V_{p(av)}$. For the example shown, 16 V · 20 µs = 320 µVs.

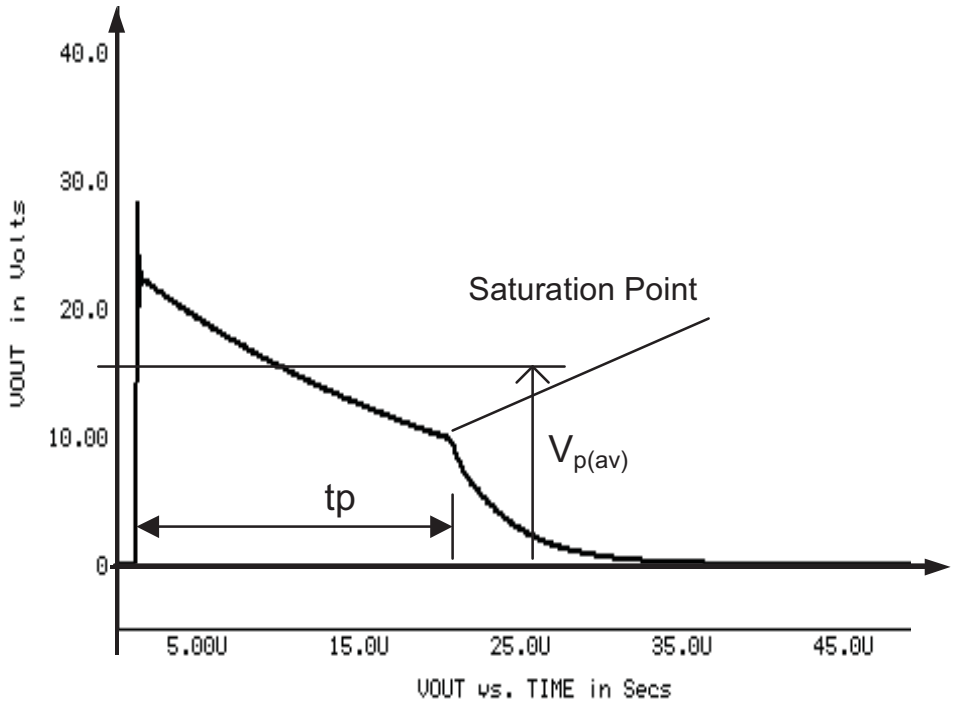


Figure 4.3.3 Typical output voltage characteristic for a pulse transformer (24 V supply voltage)

In application, drive pulses > 1 ms are barely achievable. For these reasons, in such cases a chain of short pulses is often used instead of a single long pulse (frequency 5…10 kHz). If the gaps between pulses cause interference, a second pulse chain can be superposed to achieve a gap-free long pulse. In any case, the transformer only needs to be dimensioned for the short duration of one of the pulses in the chain (e.g. for around 70 µs at 7 kHz).

Figure 4.3.4 shows several output-stage circuits for driver devices with the relevant pulse shapes. As you can see, a diode is connected between transformer and thyristor. This is intended to suppress negative drive pulses generated by backswing that the thyristor cannot cope with.

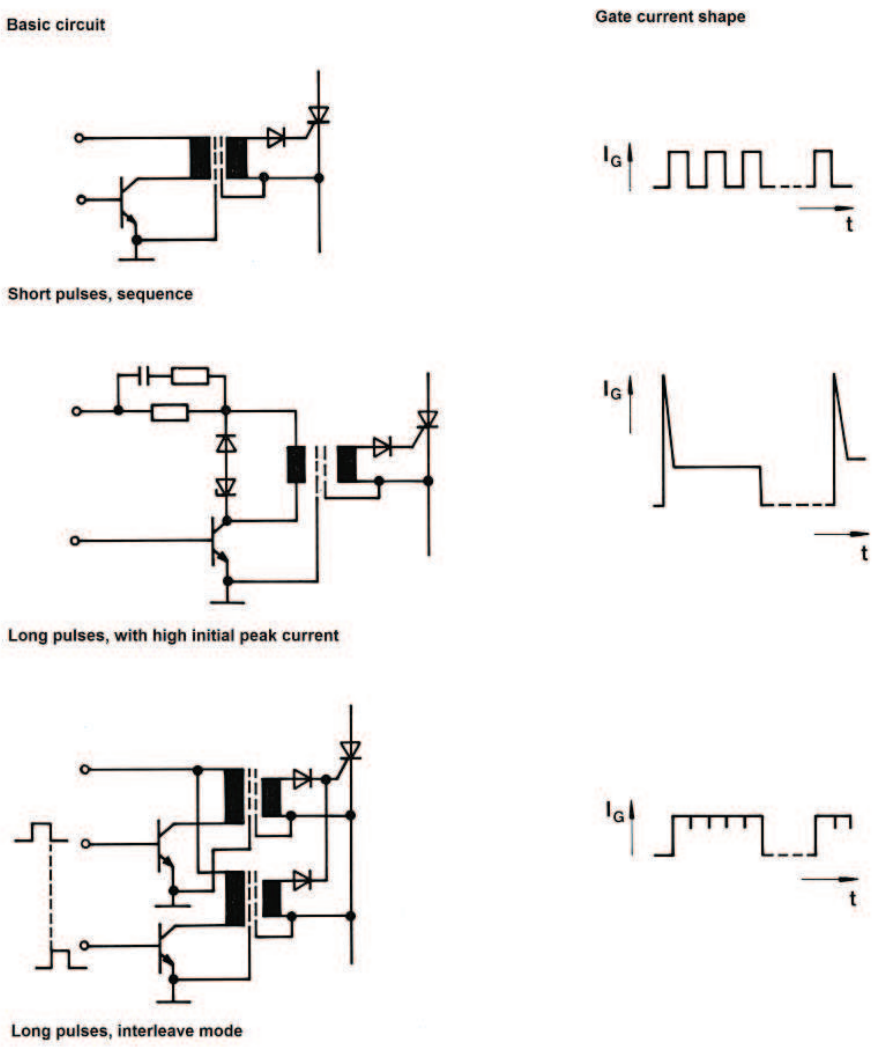


Figure 4.3.4 Output-stage circuits for driver units and typical pulse shapes.

4.3.2 Driving six-pulse bridge circuits

The thyristors in (fully controlled) six-pulse bridge circuits have a current conduction angle of 120° for continuous current. In the case of discontinuous current or indirect commutation through a free-wheeling diode, however, each current block disintegrates into two blocks with 60° distance to the starting times. In any case, when the device is turned on, two legs must be triggered at the same time. In six-pulse fully controllable bridge circuits, the driver devices therefore have to be able to deliver double pulses in a sequence of 60°.

4.3.3 Pulse transformers

In addition to the considerations on pulse duration and amplitude discussed in chapter 4.3.1, pulse transformers have to meet a number of other additional requirements. In bridge circuits, in particular, the cathode potentials of the individual thyristors are not only different but they also change rapidly in step with the operating frequency. Owing to the winding capacitances C_P of the transformers, recharge currents occur which flow through the control circuits of the thyristors and might trigger the thyristors at the wrong moment. This is particularly dangerous in inverter operation. To prevent this, pulse transformers have to be very low in capacitance and use dual shielding. One shield is connected to the earth potential of the driver device; the other is connected to the cathode terminal of the thyristor (cf. Figure 4.3.4).

The pulse transformers have to have an isolation voltage that corresponds to the nominal operating voltage. For 400 V networks 2.5 kV is common, while for 690 V networks 4 kV is typical (cf.

EN 50178). In accordance with the isolation voltage, the transformers must demonstrate the corresponding air and creepage distances between the terminals (IEC 60664).

Winding conditions other than 1:1 will enable level adjustments between primary and secondary side. Further common ratios are 2:1 or 3:1.

4.3.4 Pulse generation

To generate drive pulses, enable phase comparison with the terminal voltage, synchronisation, etc. integrated circuits are used which greatly facilitate the design of driver devices. Owing to the power that can be dissipated by an integrated circuit, however, it is not possible to directly extract a drive pulse with sufficient power. Rather, an output amplifier stage has to be added between IC output and driver transformer.

An important requirement here is drive pulse symmetry. Any asymmetry generates additional harmonic content and DC current components. On the other hand, the harmonics and voltage peaks (commutation notches and turn-off overvoltage) generated by the working converter itself must not influence the function of the driver device. Thus, sufficient decoupling is to be ensured.

4.4 Fault behaviour and diode / thyristor protection

4.4.1 General voltage surge protection

Semiconductor components are known for being sensitive to overvoltage. If the maximum rated voltages given in the datasheet are exceeded, the component might be destroyed. For this reason, the components have to be protected from any excess voltage that might occur in any of the circuits, i.e. the voltage surges have to be reduced to levels which are below the maximum rated values for the given component. Resistors and capacitors (RC elements), as well as certain semiconductor components such as varistors and silicon avalanche diodes have proven to be a reliable way of ensuring this.

The use of RC networks turns the inductors in the circuit to series resonant circuits, converting the steeply increasing voltage peaks into attenuated oscillations of low amplitude. As a result, the energy of the overvoltage is forced to decrease at low level over an extended period of time, rather than within a brief period of time at high power.

All of the remaining aforementioned circuit components make use of the non-linear resistance behaviour. Their internal resistances decrease as the voltage increases. In combination with the circuit resistors and inductors, these form non-linear voltage dividers which let through the low voltages almost without attenuation, while higher voltages above a certain level are strongly attenuated. Here, too, the overvoltage energy is distributed over a longer period; it is almost fully absorbed by the damping components alone.

The overvoltage protection components can be integrated on the AC side of the switch assembly, on the DC side or parallel to the individual switches. The advantages and disadvantages of the different arrangements will be discussed separately for each individual circuit component.

4.4.2 Overvoltage protection using resistors and capacitors

4.4.2.1 Snubbers for single switches

The most obvious way of protecting the semiconductor elements from overvoltage is to arrange the resistors and capacitors directly parallel to the individual switches (Figure 4.4.1). This ensures that the component is always protected, regardless where the overvoltage comes from. And yet this method is not always ideal; in certain cases this alone will not suffice.

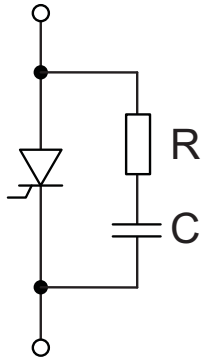


Figure 4.4.1 Snubber for a single thyristor

Uncontrolled rectifier circuits

In uncontrolled rectifier circuits, a single-switch snubber is normally not economical. Instead, protective circuitry on the AC side is selected (Figure 4.4.2a) and, if necessary, additional circuitry on the DC side (Figure 4.4.2b), since this means that fewer components are needed. In uncontrolled bridge circuits, it is normally sufficient to include a snubber on the DC side only, since two bridge legs are constantly conductive and connect the AC side with the DC side.

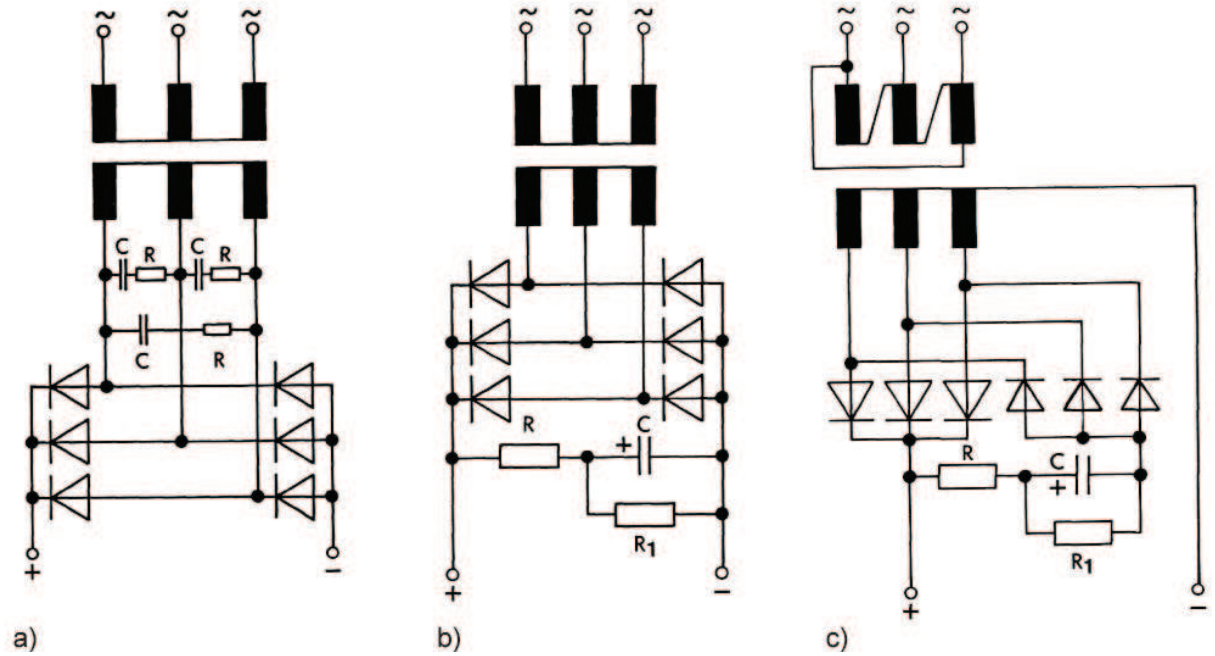


Figure 4.4.2 Snubber circuit for a diode assembly: a) on the AC side; b) on the DC side c) midpoint connection by adding auxiliary diodes to the bridge circuit

In one-way circuits (mid-point circuits) it often makes sense to use a second identical on-way circuit with low-power auxiliary diodes. Together with the main legs, this results in a bridge circuit where the snubber components can be arranged on the DC side (Figure 4.4.2c).

Controllable switches (thyristors)

While in non-controllable rectifier circuits, single-switch snubbers are rather the exception, in controllable circuits single-switch snubbers are used as a rule. This is down to the fact that thyris-

tors have to be protected not only from excessive non-permissible surges, but also - and more importantly - from the steep rate of rise. A very steep increase in voltage can trigger the thyristor unwanted.

Further, a thyristor snubber can also be necessary to facilitate thyristor triggering in the case of inductive loads and discontinuous current. This can also be achieved, however, with a DC-side snubber. The use of a single-thyristor snubber is, however, limited because the capacitors discharge through these networks during triggering and thus cause undesired stress with a steep current rate of rise (di/dt stress). In thyristor assemblies for low current densities and high voltages where relatively small capacitance and high-ohmic resistances are sufficient, this di/dt stress is still relatively low, meaning that here a single-switch snubber alone if often enough. This is to be dimensioned like an AC side snubber (cf. 4.4.2.2 Dimensioning guidelines).

With thyristor assemblies intended for higher current densities, however, the capacitances needed to ensure protection from high-energy overvoltages are so high and the optimum resistances so low that a high non-permissible thyristor di/dt caused by capacitor discharge during triggering would result. Thus, sufficient protection cannot be provided by switch-level snubbers alone. In this case, the solution is to use an AC side snubber (if need be with additional DC side circuitry).

Whether in such cases an additional switch-level snubber dimensioned as described above is necessary depends on the properties of the circuit and the thyristor itself. If thyristors with a considerable critical voltage rate of rise are used, additional single-switch snubbers are often not required if an AC side - and if needed DC side - snubber is used.

For assemblies intended for very high power, in particular for parallel thyristor circuits, it can be of advantage to connect the RC circuit via an auxiliary bridge (Figure 4.4.3). The additional costs of these auxiliary bridges are compensated for to some extent by using a less expensive electrolytic capacitor and a damping resistor with a low power rating. What must be borne in mind here, however, is that when an auxiliary bridge is used, the discharge current surge needed for safe thyristor triggering under inductive load is no longer flowing. Recommended resistance and capacitance values for single-switch snubbers are given in the catalogues or can be calculated using the following guidelines.

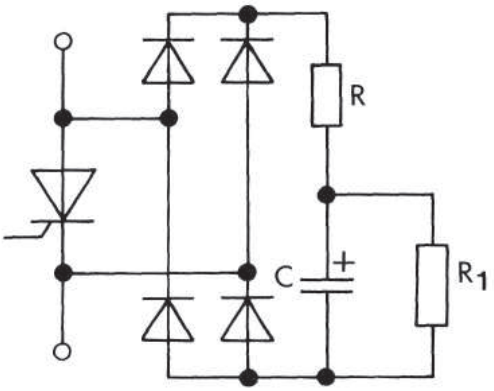


Figure 4.4.3 Single-thyristor snubber networks using an auxiliary bridge

Parallel thyristors

Owing to the unavoidable variation in trigger delay times, which cannot be reduced to below a certain value even with strong trigger pulses with a steep rate of rise, parallel thyristors will never fire simultaneously. For this reason, in parallel thyristor assemblies, suitable measures are needed to prevent the snubber capacitances of all of the remaining thyristors from discharging through the thyristor that fires first since this could lead to destruction. Notes on this are provided in the following sections "Snubber circuits using auxiliary diodes" and "Snubbers using series reactors".

Half-controlled rectifiers

In half-controlled circuits switch snubbers are used according to the same principles as for fully controlled circuits. In particular, the same resistances and capacitances are to be used for diode

snubber circuits as for thyristor snubbers. Under no circumstances are the snubber circuit elements intended for pure diode assemblies sufficient.

Freewheeling paths

Freewheeling diodes or silicon diodes in freewheeling paths of controllable converter circuits are to be protected just like the thyristors in the main legs.

Dimensioning guidelines for single-switch snubbers

The following dimensioning guidelines for single-switch snubbers apply on condition that the snubber circuit is only intended to provide protection from the overvoltages caused by the hole storage effect (HSE). If additional high-energy overvoltages, for example those that occur when the freewheeling transformer is turned off, have to be attenuated, the resistances and capacitances are to be calculated on the basis of the guidelines described in chapter 4.4.2.2 AC side snubbers / Dimensioning guidelines.

On the assumption that around half of the energy represented by the recovered charge Q_{rr} is transferred to the circuit in the form of an overvoltage, the most favourable values for capacitance and attenuating resistance R can be calculated as

$$C = \frac{Q_{rr}}{V_v \cdot \sqrt{2}} \qquad R = \sqrt{\frac{L_s}{C}}$$

C: Capacitance (in µF); L_S: Total inductance in the circuit (in µH);
R: Resistance (in Ω); V_v: Effective terminal voltage (in V);
Q_{rr}: Recovered charge (in µC).

In addition, it should be considered that the current amplitude during discharge of C via R and the thyristor must not be greater than 50 A; the amount is determined by the voltage at the moment of firing and the resistance R. If need be, the value for R has to be selected above the value that results from the equation above. The resulting overvoltage damping is, of course, not quite as favourable. The power dissipation P_R imin the damping resistor R can be calculated using the following formula:

$$P_R = \sqrt{2} \cdot V_V \cdot Q_{rr} \cdot f + k_1 \cdot C \cdot V_V^2 \cdot f$$

$k_1 = 0$	for switches in uncontrolled rectifier circuits
$k_1 = 2 \cdot 10^{-6}$	for switches in controlled single-pulse and double-pulse midpoint circuits, as well as half-controlled two-pulse bridge circuits and AC controllers
$k_1 = 3 \cdot 10^{-6}$	for switches in controlled three-pulse and six-pulse midpoint circuits, as well as fully-controlled two-pulse bridge circuits and AC controllers
$k_1 = 4 \cdot 10^{-6}$	for switches in controlled six-pulse bridge circuits
Q_{rr}:	Recovered charge (in C; not µC!)
V_v:	Effective terminal voltage (in V)
f:	Operating frequency (in Hz)
C:	Capacitance (in µF)

When selecting the resistor, please note that the rating specified by the manufacturer may refer to various surface temperatures. It is advisable to dimension for a surface temperature of max. 200°C.

Snubber circuits using auxiliary diodes

In some cases, it is possible or even necessary to use auxiliary diodes in the snubber circuits when connecting thyristors with RC elements. For example, using the circuit shown in Figure 4.4.4a, the rate of rise of the forward blocking voltage can be ideally attenuated by the components R and C, while for discharge of capacitor C during thyristor triggering an additional resistance R_z is effective which limits the current surge to a harmless level. In reverse direction, R_z is effective too, meaning that in this direction the reduction of surge voltages is not ideal.

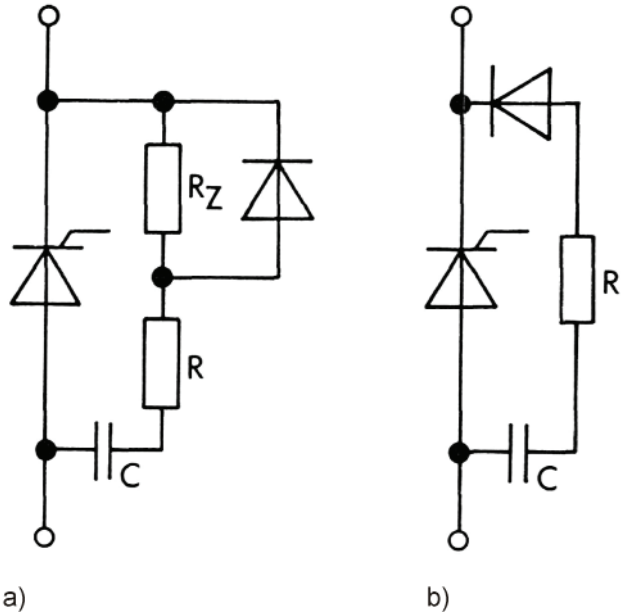


Figure 4.4.4 Snubber circuits for thyristor control: single-switch snubbers based on auxiliary diodes

In self-commutated rectifiers, overvoltage suppression is often not needed in reverse direction, since it is already suppressed by the regenerative arm. In such cases, the circuit shown in Figure 4.4.4b, where the snubber is effective in forward direction only and an optimum layout is possible, can be used. Here, capacitor discharge does not happen during thyristor triggering at all.

If thyristors are connected in parallel, the different trigger delay times would cause the snubber capacitors of all of the remaining thyristors to fully discharge through the first thyristor that fires. This must be avoided at all costs. For this reason, in parallel thyristor circuit arrangements - and in many cases for individual high-power thyristors as well - the single-switch snubber circuit comprising an auxiliary bridge as shown in Figure 4.4.3 is used. This may be relatively complex. It offers, however, optimum protection in both voltage directions and removes the shortcomings of a simple RC snubber at the same time. Dimensioning guidelines for single-switch snubbers comprising an auxiliary bridge are shown in chapter 4.4.2.2 / Auxiliary bridge snubbers.

Snubber circuits featuring series reactor

In parallel thyristor connections, series reactors are often used in series with the thyristors in order to achieve even current distribution in stationary state and under short-time overload and short-circuit conditions (Figure 4.4.5). At the same time, these series reactors - in combination with the RC snubber - are particularly effective in limiting the peak values, even in the rate of rise of overvoltage. This is very important, especially in converters in six-pulse bridge configuration. At the same time, these series reactors prevent the snubber capacitors of the remaining parallel thyristors from discharging via the thyristor that fires first. This is why the use of series reactors does not normally require an auxiliary bridge. To attenuate oscillations, a resistor is often connected in parallel to the series reactor.

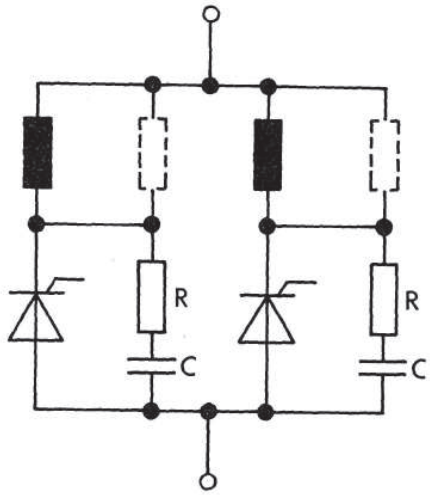


Figure 4.4.5 Single-switch snubber circuit for parallel thyristors using series reactors

Series connected thyristors or rectifier diodes

For series connected silicon rectifier diodes or thyristors, single-switch snubbers with RC elements not only have the effects discussed above, but fulfil an additional function, too. Owing to the variation in reverse recovery time, the single switch that blocks first is at risk of having to take up a high voltage that is not permissible for a single switch alone. With series connected thyristors, there is an additional risk: directly before firing, the thyristor that goes over into on-state last might have to take up an inadmissibly high forward voltage that would result in uncontrolled "break-over" and may damage the thyristor.

Both of these risks must be ruled out using a snubber circuit with RC elements. The right dimensioning for these RC elements can be calculated using the dimensioning guidelines given for single-switch snubbers. The recommended capacitor capacitance, however, is double the value calculated in this way. Of course, in addition to this "dynamic voltage distribution", static voltage distribution by means of parallel resistors is needed. These resistors can be selected such that a current roughly the size of the maximum rated reverse current specified in the datasheet for the thyristor or diode flows through each resistor. The voltage increase over the stationary voltage that occurs when the last thyristor is fired or the first switch blocks can be seen in Figure 4.4.6.

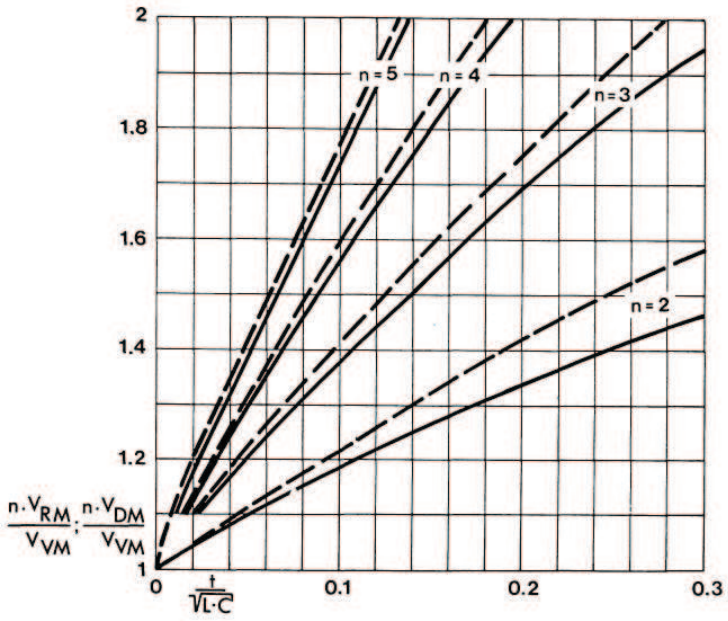


Figure 4.4.6 Time characteristic of the voltages V_{DM} or V_{RM} across the thyristor fired last (___) and turning off first (- - - -) for n series connected thyristors (V_{VM}: Crest value for total terminal voltage, L: Inductance in the commutation circuit, C: Thyristor snubber capacitance).

4.4.2.2 AC side snubber

Very high voltage spikes occurs when transformers are turned on and off under low load or no load at all. In controllable converter circuits, in addition to these occasional non-periodic switching operations, periodic switching operations caused by the thyristor firing also occur. This is particularly true for diode assemblies which have to work in connection with an AC converter on the primary side of the rectifier transformer. For these reasons, particular attention must always be given to the snubber on the AC side (Figure 4.4.2a).

As mentioned in chapter 4.4.2.1, in thyristor assemblies of small current density and high voltage, it may be possible for the single-switch snubber to be rated such that it provides sufficient protection from the the high-energy voltage spikes that occur across the inductor of the transformer or the series reactor. Normally, however, even in thyristor assemblies with single-switch snubbers, an additional snubber circuit is needed on the AC side.

Snubbers for the individual switches can be rated in accordance with chapter 4.4.2.1, provided there are no inductors between the thyristors and the AC side snubber circuit. In diode assemblies, on the other hand, a DC side snubber is often sufficient.

Snubber on the primary side of a high-voltage transformer

In rectifiers for the generation of high voltages, the AC side snubber is often placed on the primary side of the transformer (Figure 4.4.7). In this case, the capacitance and resistance values calculated according to the following dimensioning guidelines are to be converted on the basis of the transmission ratio of the transformer.

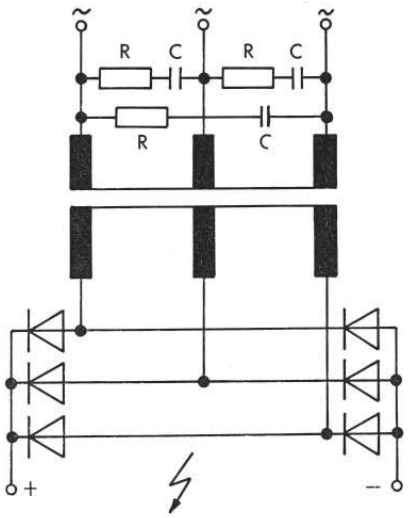


Figure 4.4.7 Primary-side snubber of a high-voltage transformer

Dimensioning guidelines for AC side snubbers

The most favourable values for capacitance C and damping resistance R can be calculated approximately using the following formulae:

$$C = 170 \cdot \frac{\varepsilon \cdot P_T}{k_2 \cdot f \cdot V_V^2}$$

$$R = \frac{k_3}{C \cdot f} \cdot 10^3$$

The power dissipation P_v in the resistor R can be approximated with

$$P_V = 1{,}2 \cdot k_2 \cdot V_V^2 \cdot f^2 \cdot C^2 \cdot R \cdot 10^{-10} \text{ [W]}$$

P_T [VA]: Transformer power rating; ε [%]: Relative magnetising current of the transformer; V_v [V]: AC voltage effective at the RC element; C [µF]: Capacitance; R [Ω]: Resistance;

f [Hz]: Frequency, for k_2 the following values are to be used:

$k_2 = 1$ for all single-phase circuits

$k_2 = 2$ for three-phase circuits and snubber on the DC side or using an auxiliary bridge

$k_2 = 3$ for three-phase circuits and snubber on the AC side

The factor k_3 can be seen in Figure 4.4.8a as a function of the rated power of the transformer P_T. If the magnetising current ε of the transformer is not known, approximated values as a function of P_T can be derived from Figure 4.4.8b.

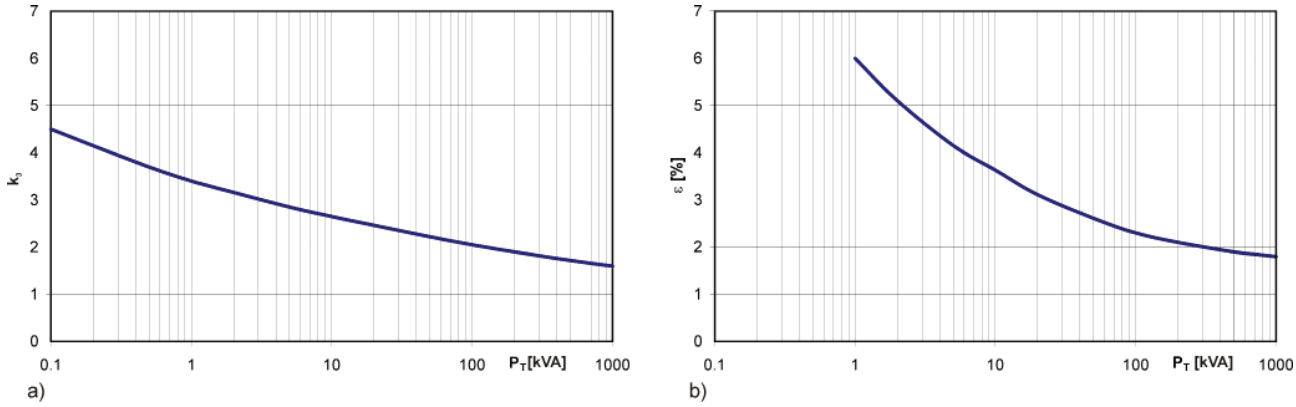


Figure 4.4.8 a) Factor k_3 as a function of the rated power P_T of the converter transformer; b) Magnetising current ε (as a percentage of the rated current) of a converter transformer as a function of its rated power P_T.

Auxiliary bridge snubber

In 3-phase circuits, in particular, it is often favourable to use a single RC element connected via an auxiliary bridge rather than the three RC elements otherwise needed. A circuit such as this can be seen in Figure 4.4.9.

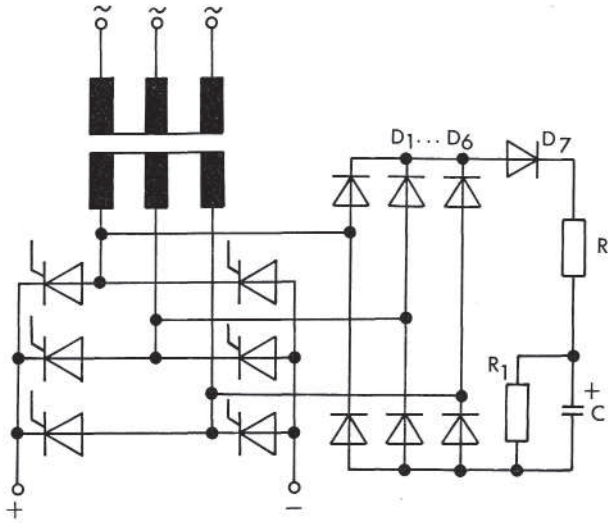


Figure 4.4.9 AC side snubber circuit using auxiliary bridge and auxiliary diode

Capacitance C and resistance R can be calculated using the following equations for primary side snubbers. The rating of the resistor R, however, only needs to be around 2 W. The additional diode D_7 is not needed in every case. It is responsible for reducing the load on R and C caused by harmonics (especially in circuits with phase-control). The discharge resistance R_1 ensures that the capacitor discharges quickly after device turn-off. This resistance is approximately selected as

$$R_1 \approx \frac{1}{C \cdot f} \cdot 10^7$$

The power dissipation $P_{V(R1)}$ is approximately

$$P_{V(R_1)} = \frac{2 \cdot V_V^2}{R_1}$$

The capacitance C is to be used in µF.

The auxiliary diodes D_1. . .D_7 are to be selected such that the max. rated surge current (for the related conduction time t ≈ R • C) is double the size of the peak value I_{LM} of the load current which flows into the capacitor C at turn-on. In the worst case scenario (turn-on at the moment of voltage peak value), if this is set at at

$$I_{LM} = \frac{V_V \cdot \sqrt{2}}{R} ,$$

the actual value is far lower; this is owing to the remaining ohmic and inductive resistances in the circuit which are not taken into account here. Diodes or compact rectifiers with surge forward currents of 150 A to 300 A (for t = 10 ms) should suffice in almost every case. Heat sinks or heat plates are not necessary, since the continuous load on the auxiliary diodes is very low.

Rectifier circuits without galvanic isolation from AC power supply

Often rectifier circuits are designed such that only an autotransformer and / or a choke lies between the diode or thyristor assembly and the AC power supply. In this case, the choke has to fulfil several tasks, which the transformer would normally do "in addition", i.e. in addition to providing galvanic isolation from the power supply and changing the operating voltage:

- Limitation of short-circuit current during fuse operating time
- Avoiding voltage decrease in the network during commutation
- Reducing peak values and rate of rise of line voltage spikes in combination with the overvoltage protective components

In order to fulfil these tasks, the inductance L of the choke has to be big enough to result in a short-circuit voltage of at least 4% of the operating voltage V_V.

In other words:

$$L \geq \frac{4}{100} \cdot \frac{V_V}{2\pi f \cdot I_V}$$

Here, I_V is the effective phase current. In 3-phase circuits, each phase naturally needs one choke such as this. In circuits with an autotransformer, the choke is not needed if the wiper cannot be adjusted to the end of the winding, meaning that a sufficiently large part of the winding is always between line and rectifier.

The AC-side snubber of the transformerless rectifier can be rated using the same rules as for circuits with transformers. The rated output power P_T is to be set to the value calculated from the phase voltage V_V and phase currents I_V for an imaginary transformer. Likewise, the ε value to be used is the value corresponding the rated output power P_T of the imaginary transformer.

Snubbers for AC voltage converters (W1C)

W1C circuits comprise two antiparallel thyristors; the following, however, applies to a circuit comprising one thyristor with antiparallel diode. This is always equipped with a snubber circuit, in the simplest case comprising one common RC element (Figure 4.4.10). If each of the antiparallel components has its own fuse protection, then each must also be equipped with its own RC element (Figure 4.4.10b); i.e. the RC element calculated from the equations below is evenly distributed to the two switches. RC elements with one capacitor greater than 1 µF have to be connected using an auxiliary diode.

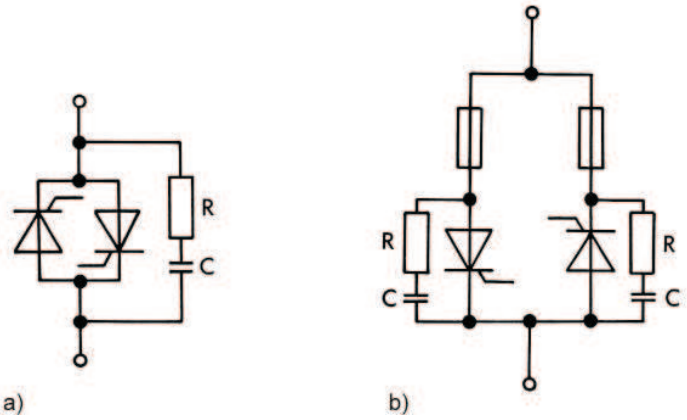


Figure 4.4.10 Snubber for AC controller; right: with individual fuses

The values for capacitor C and resistor R can be determined using the following formulae:

$$C \approx 700 \cdot \frac{I_V}{V_V^2} \qquad R \approx \frac{9000}{C \cdot V_V}$$

The power dissipation P_R in the resistor R can be approximately calculated as

$$P_R \approx 3 \cdot 10^{-6} \cdot C \cdot V_V^2 \cdot f$$

4.4.2.3 DC side snubber circuits

Diode assemblies

As mentioned several times already, for diode assemblies in bridge configurations it is normally enough to add a snubber to the DC side if the diode assemblies are not already connected to a low-inductance voltage DC link. The resistors and capacitors are rated either according to the guidelines provided in chapter 4.4.2.2 or in this chapter, depending on whether the surge voltages to be attenuated are on the AC or DC side. If there is any possibility of the rectifier being conductive even when the load is turned off or disconnected, a discharge resistor has to be used.

In rectifiers with permanent capacitive load, this load will function as an overvoltage snubber, meaning that no additional snubber circuits are needed. If, on the other hand, there is a ripple filter choke or fuse between the rectifier and capacitive load, a snubber circuit for overvoltage will have to be integrated directly at the rectifier in addition.

For diode assemblies in midpoint configurations, it often makes sense to set up the snubber similar to an AC-side snubber with auxiliary bridge, with one half of the auxiliary bridge being formed by the principal arms of the rectifier. Small auxiliary diodes are added to the other half of the auxiliary bridge. Note that the resistors and capacitors, as well as the auxiliary diodes are to be rated in the same way as for an AC-side snubber. What must be borne in mind, however, is that such snubbers do not provide protection from overvoltages that affect the rectifier from the DC side.

Thyristor assemblies

In thyristor assemblies, an AC-side snubber and single-switch snubbers will normally be integrated, meaning DC snubbers can often be dispensed with. In individual cases, however, they might still be necessary. Sometimes, the single-switch snubbers are not necessary and one DC and one AC side snubber can be used instead. The latter functions as a capacitive base load at the same time, ensuring that the thyristors fire without any problems under unfavourable operating conditions. The capacitor and resistor value can be calculated according to the following "dimensioning guidelines".

Inverters

In inverters, a battery or buffer capacitor is often connected on the DC side, meaning no DC snubber circuit is needed.

Dimensioning guidelines

The best effect is achieved if the following conditions are fulfilled:

$$R + R_L = 2 \cdot \sqrt{\frac{L_L}{C}}$$

(Figure 4.4.2b). If

$R = R_L$

is selected, this results in

$$C = \frac{L_L}{R_L^2}$$

L_L: Load inductance (in µH);
R_L: Ohmic resistance in the load (in Ω);
C: Snubber capacitance (in µF);
R: Damping resistance (in Ω).

In many cases, it will suffice to use a smaller capacitor. In this case, R should be selected such that the aforementioned equation applies approximately.

The power dissipation P_V in the damping resistor R can be calculated as

$$P_V = \frac{V_{ALT}^2 \cdot R}{R^2 + \left(\frac{10^6}{2\pi \cdot f_{ALT} \cdot C}\right)^2}$$

V_{ALT}: Effective AC voltage superimposed on the DC output voltage [V]
f_{ALT}: Frequency of the AC voltage [Hz]. All of the remaining parameters as above.

If a discharge resistor R_1 (Figure 4.4.10) is needed (discharge of C through load is not always guaranteed), this is to be rated to

$$R_1 \approx \frac{1}{C \cdot f} \cdot 10^7 \ [\Omega]$$

f [Hz] is the operating frequency. This must be rated to at least

$$P_{V(R_1)} = \frac{V_D^2}{R_1}$$

V_D [V] is the DC voltage.

4.4.3 Overvoltage protection using varistors

Varistors are voltage-dependent resistors. They consist of a semiconductor material which, like ceramic, is pressed in pulverised form and then sintered to create a solid disc. Their effect is based on the existence of numerous random pn-junctions at the contact points between the little fragments or grains. Most varistors are made of zinc oxide ZnO, which is why they are also known as metal-oxide varistors (MOV).

The resistance of a varistor decreases as the voltage increases. In combination with a constant series resistance, this functions as a voltage divider with a divider ratio (attenuation factor) that increases in line with input voltage increase. It goes without saying that an arrangement such as this is suitable for attenuating overvoltage. For brief voltage peaks, the series resistor can be replaced by an inductor. In converters featuring transformers, this is the stray inductance of the relevant transformer winding; in cases of direct connection to the mains, this is the inductance of the series reactor as per chapter 4.4.2.2, which, of course, is necessary here, too. Varistors can be used to attenuate overvoltage on the AC side or on the DC side, or even as single-switch snubbers.

A typical characteristic of a ZnO varistor, as given by the manufacturer, can be seen in Figure 4.4.11. This can be used to derive the corresponding peak voltage for a given peak current. Over and above this, the manufacturer specifies a maximum permissible peak current, which must not be exceeded even for a very short pulse duration. The following steps are to be taken for component dimensioning:

- Selecting a varistor with suitable operating voltage (specified by the manufacturer as an effective value): For non-sinusoidal operating voltage, the crest value must not exceed that of a sinusoidal voltage with the specified effective value. This also applies to DC voltage pulses. For smoothed DC voltage, the maximum permissible value specified in the datasheet must be observed.
- Determining the limiting voltage from the current / voltage characteristic of the selected ZnO varistor. To do so, the peak value of the maximum expected inrush current has to be determined. In transformers, this is the magnetising current converted according to the ratio of windings; in inductors in general this is the maximum value of current that prevails directly before a sudden interruption. The periodic peak reverse voltage of the semiconductor component to be protected has to be higher than the limiting (clamping) voltage determined in this way.
- Determining the total mean losses and comparing against the maximum permissible value specified in the manufacturer datasheet (at the given ambient temperature).

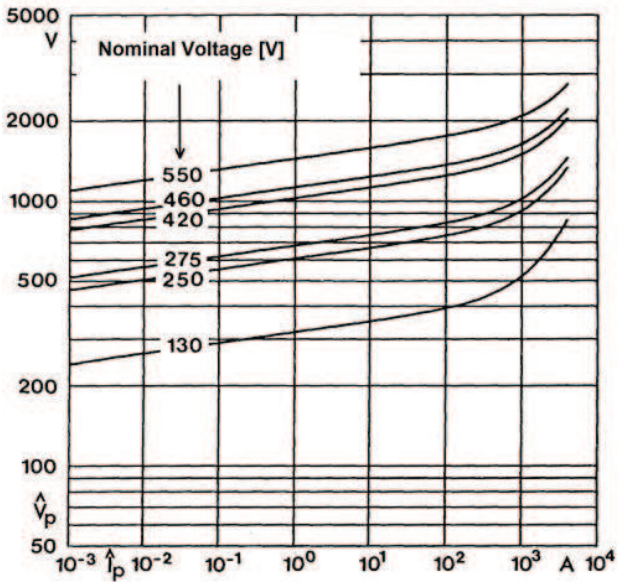


Figure 4.4.11 Current / voltage characteristic of a ZnO varistor (pulsed)

In ZnO varistors, the fundamental frequency power losses are normally negligibly low.

One shortcoming of varistors is that they do not attenuate the voltage dv/dt. Thus, in thyristors with low dv/dt values, an additional RC snubber is needed.

4.4.4 Snubber circuits based on silicon avalanche diodes

Silicon avalanche diodes (Figure 4.4.12) differ from conventional silicon rectifier diodes in that the steep increase in reverse current above a certain voltage (breakthrough voltage) does not come from the breakthrough effects on the surface of the silicon element, but is caused by the avalanche effect in the entire space charge zone of the pn-junction. In normal rectifier diodes, reverse current pulses of relatively low current density and duration may destroy the diodes; this is due to the concentrations of reverse current at the individual points on the surface. Avalanche diodes, in contrast, can cope with reverse current pulses resulting in power dissipation in the low-kW range.

a) b)

Figure 4.4.12 Circuit symbols for avalanche diode (a) and bipolar suppressor diode (b)

4.4.4.1 Avalanche rectifier diodes featuring self-protection

Like normal rectifier diodes, avalanche rectifier diodes can be used in a wide variety of circuits; owing to their lack of sensitivity towards brief stress in reverse direction, snubber circuits are often not needed for overvoltage protection. In particular, in high-voltage applications, avalanche rectifier diodes can be connected in series without the use of snubbers circuits usually required for static and dynamic current distribution.

The manufacturer specifies the breakthrough voltage $V_{(BR)}$ as well as the maximum rated reverse current and peak reverse power dissipation P_{RSM} - normally as a function of pulse duration. The dimensioning must ensure that the breakthrough voltage lies far above the peak operating voltage with regard to superimposed periodic voltage peaks. The outputs of the non-periodic overvoltage pulses - provided they exceed the breakthrough voltage - lie below the max. rated peak reverse power dissipation for the given pulse duration. The breakthrough voltage increases as the virtual junction temperature T_j rises in accordance with the following equation:

$$V_{(BR)1} = V_{(BR)0} \cdot [1+1.2 \cdot 10^{-3} \cdot (T_1 - T_0)]$$

Where $V_{(BR)0}$ is the breakthrough voltage at temperature T_0 and $V_{(BR)1}$ is the breakthrough voltage at temperature T_1.

4.4.4.2 Avalanche diodes as protection for other components

If avalanche diodes are to be used to protect other semiconductor components, in particular normal rectifier diodes, thyristors, IGBT or MOSFET, it is vital that not only a certain minimum but also a maximum breakthrough voltage is complied with. In addition, a certain rate of rise for the off-state characteristic in the breakthrough region must be guaranteed. Such diodes are referred to as controlled avalanche diodes; they are also incorrectly known as high-voltage Zener diodes.

Controlled avalanche diodes are available in various different versions, i.e. as controlled avalanche rectifier diodes, controlled avalanche clamping diodes, or (transient voltage) suppressor diodes. While the former can be used as normal rectifier diodes and / or to protect other components, clamping diodes function solely as protective elements for other semiconductor components and cannot be used in forward direction. For use in AC voltage circuits, there are also bipolar suppressor diodes (Figure 4.4.12), which consist of diodes connected back to back in series that are independent of the polarity. If controlled avalanche rectifier diodes are loaded in forward direction, it must be borne in mind that the mean value for maximum permissible periodic off-state losses naturally decreases by a value equal to the mean forward power dissipation caused by the on-state current load. Examples of circuits with controlled avalanche diodes can be seen in Figure 4.4.13.

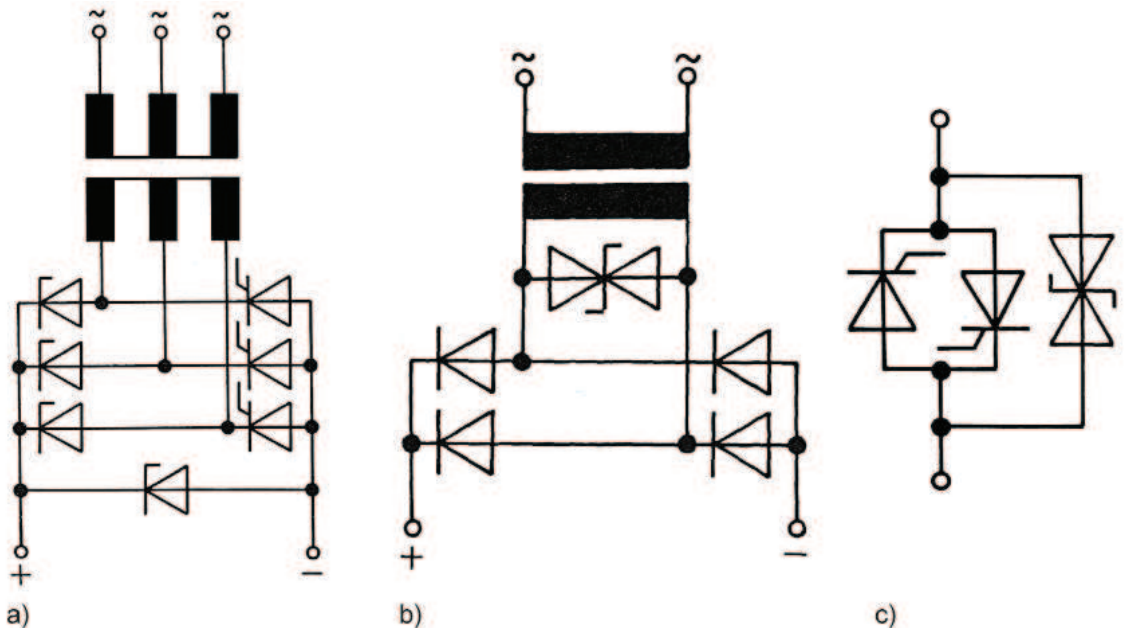


Figure 4.4.13 a) Half-controlled six-pulse bridge circuit with controlled avalanche rectifier diodes that protect the thyristors from overvoltage at the same time; b) AC side protection of a 2-pulse bridge-circuit featuring a bipolar suppressor diode; c) AC voltage controller snubber featuring a bipolar suppressor diode

Clamping diodes (transient voltage suppressors) are used mainly to protect thyristors and IGBT, especially in devices used in high-voltage and high-power applications where they have the advantage over RC snubbers of being small in size and having lower energy consumption. With series connected components, in particular, they can be used in place of the RC elements required for dynamic current distribution. What must be considered here is that avalanche diodes do not affect the voltage rate of rise. An additional RC element might therefore be needed for thyristor snubber circuits; this is to be dimensioned in accordance with chapter 4.4.2.1.

4.4.4.3 Restrictions in application range

Generally speaking, silicon avalanche diodes cannot cope with high-energy surge voltages, such as those that occur when transformers are turned off under no-load. In such cases, RC snubber elements are therefore needed either in place of or in addition to the avalanche diodes.

4.4.4.4 Case types

Small silicon avalanche diodes have cases with wire connections or are meant for soldering onto PCBs (SMD). Larger diodes feature standard cases with screw studs. They are also available as bridge circuits. Clamping diodes also come in symmetrical cases similar to fuses that contain two pn-junctions connected in series with opposite polarity. Such bipolar suppressor diodes have symmetrical characteristics; one such diode is therefore sufficient to protect a thyristor.

4.4.5 Overcurrent protection for diodes and thyristors

Here, the term overcurrent refers to a current load acting on the power semiconductor that, given the existing cooling conditions, would lead to the destruction of the component unless the current is turned off in time by means of suitable devices. Unlike a short-circuit, which is dealt with in the next chapter, this is not a current that rises steeply within a few milliseconds.

Such overload cannot be caused solely by an unforeseen current increase (overcurrent), it could also be caused by an unintentional change in cooling conditions. As a result, the component cannot cope with currents that are normally permissible when cooling is properly ensured. Examples of improper cooling are blocked fan slits, fan breakdown or, in water-cooled systems, malfunction in coolant supply. A number of well-established protective devices for overload conditions such as these are described below. Here, a differentiation must be made between protective devices which trigger as a result of unintentional current increase only and those which respond when the cooling system is not functioning properly, as well as devices which provide protection in both cases.

4.4.5.1 Devices for protection from overcurrents

Power circuit breakers

Power circuit breakers are the most common form of overload protection. There are switches with thermal, magnetic and thermo-magnetic tripping. Similar to fuses, their response times are dependent on the overcurrent and lie within the range of under 1 s; the response time for high overcurrent is shorter. Manufacturers show this ratio in the form of a characteristic that can be then compared with the overcurrent capability (current rating) of the semiconductor component. Note that the trip current of power circuit breakers and the currents in the current / time curves for safety fuses are always effective values, while the maximum surge current of the semiconductor components are peak values of sinusoidal half waves. Thus, if comparisons are to be made, these values first have to be converted into effective values.

Throughout the entire possible time period, the trip current of the power circuit breaker has to be lower than the permissible overcurrent of the semiconductor component in the case of error. If this cannot be achieved for the entire period, an additional protective device - normally a semiconductor fuse - has to be integrated for the period not covered.

Fuses

Fuses are intended first and foremost to provide short-circuit protection (cf. chapter 4.4.6). In certain circumstances, however, the fuse may also provide protection from overload in the aforementioned sense of the word. To determine this, a comparison is to be made between the fuse current / time curve for the given period and the permissible overcurrents for the protected semiconductor component in the event of an error. It might be necessary to cover any remaining time in which the fuse in question does not provide protection with an additional protective device.

Suppression of driver signal

In controllable circuits, it makes sense to implement overcurrent protection by influencing the driver unit. When overcurrents occur that are not intended for operation, the trigger pulses are either fully suppressed, or the driver unit is designed such that the current is limited to a permissible level in any given conditions. The requirement for the use of the driver unit as protection is, of course, that the thyristor controllability is maintained long enough (i.e. the maximum permissible virtual junction temperature is not exceeded) for the driver protection to take effect. For short-circuit currents that rise steeply within one semi-oscillation, for example, protection via the driver unit is not possible.

4.4.5.2 Protective devices for malfunctions in the cooling device

Wind vane relays

With enhanced air cooling, wind vane relays which trigger a protective component or influence the driver unit under error conditions can be used to protect the power semiconductors from overload should the fan break down or the fan vents be blocked.

Water flow monitors

In water-cooled systems, flow monitors or flow indicators can be used to monitor the coolant flow.

4.4.5.3 Devices that respond to both overcurrent and cooling unit malfunctions

The destruction of power semiconductors in overload conditions always happens due to excessive non-permissible temperatures, regardless of whether the overload results from overcurrent or malfunctions in the cooling unit. This is why it makes sense to use devices to protect the semiconductor devices that respond directly to this temperature increase.

Bimetal thermostats

Bimetal thermostats contain bimetal discs which, at a certain factory-set temperature, snap from one position to the next, opening or closing a contact in the process (Figure 4.4.14). They normally have screw studs with which they are screwed onto the heat sink, establishing the closest possible thermal contact with the semiconductor components as possible. If several semiconductor components are to be protected by way of separate heat sinks, each of the heat sinks will in some cases require its own thermostat. The contacts are connected in series or parallel, depending on whether they open or close.

Bimetal thermostats can be used for natural or forced air cooling, as well as for water-cooled systems. In the latter case, it makes sense to use an additional thermostat which suppresses or completely blocks the coolant supply if a certain heat sink temperature is not reached. This will ensure that no condensation accumulates on the isolated parts of the semiconductor components.

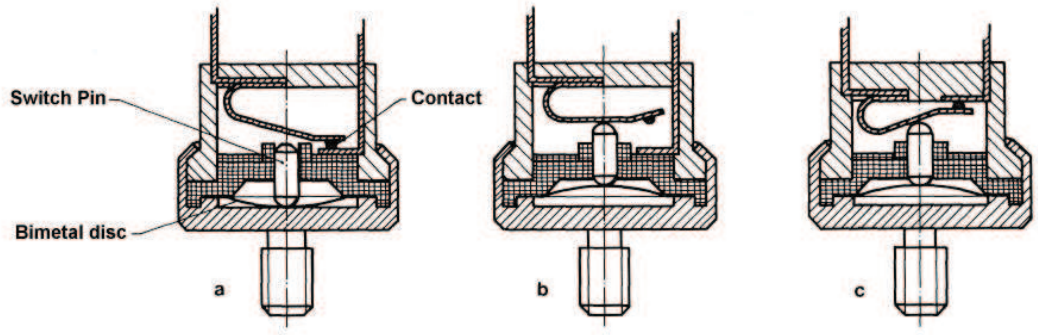


Figure 4.4.14 Bimetal thermostat for screw-connection to a semiconductor heat sink; a) Design with opening contact in neutral position; b) Same design after the response temperature has been exceeded. The centre of the bimetal disc clicks upwards, opening the contact; c) Design with closing contact once the response temperature has been exceeded.

Temperature-dependent resistors

Temperature-dependent resistors have the advantage over bimetal thermostats that they respond to temperature changes more quickly, resulting in a minor safety margin between the operating current and the minimum current required to trip the protective device. An additional electronic circuit is needed to convert the change in resistance into a signal that can, for example, trigger a protective device.

Temperature-dependent resistors can also be integrated into power modules, for example soldered onto the insulating substrate. Integrated sensors such as these respond far more quickly than the sensors on the heat sink; having said that, these are definitely not enough to detect increases in chip temperature caused by steep overcurrents before chip damage occurs. The silicon-based resistors used have either a positive temperature coefficient (PTC) where the resist-

ance increases as temperature increases, or a negative temperature coefficient (NTC) where the resistance decreases as temperature increases.

4.4.6 Short-circuit protection for diodes and thyristors

IGBT and MOSFET clamp the current in the event of a short circuit to around 6 to 8 times the rated current and are not damaged by the short circuit current if the component is turned off within 6 -10 µs via the gate. Diodes and thyristors, in contrast, do not limit short-circuit current. For this reason, external measures have to be take to ensure short-circuit protection.

The silicon chip of a thyristor or rectifier diode has a very low thermal capacity, which is why strong, fast rising overcurrents that often occur in short circuit conditions can destroy this part within just a few milliseconds. For this reason, normal low-voltage fuses, including quick-blow fuses, are not suitable for protecting rectifier diodes and thyristors from being destroyed by short circuits. Instead, purpose-developed fuses - which are available as fast-blow, super-fast blow and ultra-fast blow fuses - or simple semiconductor fuses have to be used.

The most common causes of short-circuits in converters are:
- Short circuit in the load or the connecting lines between the converter unit and load
- Short-circuit in a rectifier diode or thyristor due to loss of blocking ability (sudden failure)
- Loss of stability in inverters or converters due to trigger error

If a semiconductor fuse is connected in series to each rectifier diode and each thyristor, where the diodes and thyristors are used in the main legs of the converter circuit, the diodes and thyristors can be protected in all of the above short-circuit cases. At the same time, all other components in the main circuit are also protected, since chokes, transformers, resistors etc. are far less sensitive to overcurrents than the semiconductor components.

In bridge circuits, two power semiconductors each have a common AC terminal. For this reason they can be protected by a common fuse in the AC supply line (Figure 4.4.15b). This is known as a phase or AC side fuse. This has the advantage that fewer fuses are needed and that the switching voltage that occurs when the fuse element melts does not put any load on to the semiconductor components. For high current load on thyristors or rectifier diodes, as may be the case in systems with forced cooling, and high operating voltage at the same time, it may well be difficult to find a fuse with sufficient rated current (effective current in the phase √2 times higher than in each of the two arms) and with an operating i²t, on the other hand, that is lower than that of each of the two semiconductor components. In this case, each bridge arm must be allocated its own fuse (Figure 4.4.15a). In AC controllers a common fuse normally suffices, too (Figure 4.4.15b2).

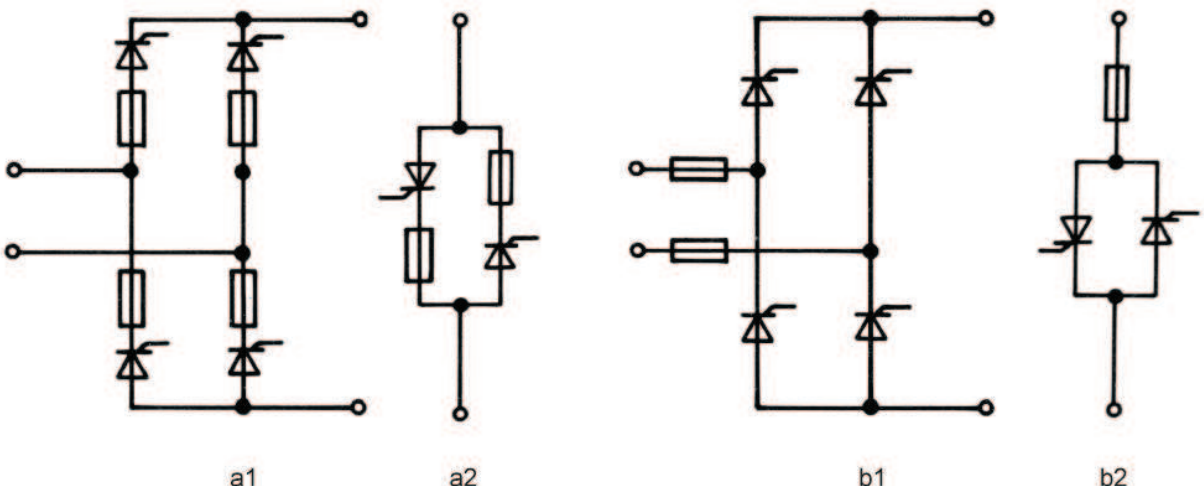


Figure 4.4.15 Possible arrangements for semiconductor fuses in a converter bridge (a1 and b1) and for an AC controllers (a2 und b2); a) Arm fuse or b) Phase fuse

If rectifier diodes or thyristors are connected in parallel for high power densities, each semiconductor component is equipped with a fuse. The advantage of this is that if one component or fuse

suddenly fails, the device will remain fully functional - with less power accordingly. The internal resistances of the fuses will also compensate somewhat for the differences in the characteristics of the semiconductor components, meaning the current distribution - in short-circuit conditions - will be more homogenous.

For short-circuit protection using blow-out fuses, short circuits are assumed to occur very seldom only. There are, however, applications where load short-circuit happens more frequently. In this case, a DC side high-speed circuit breaker, a power circuit breaker or another device to block the driver pulses of the thyristor (driver signal blocking) is needed on the load side. This has to be in addition to the fuses also needed because of the other short-circuit possibilities mentioned before. The converter circuit can, of course, be rated such that in the event of a load short circuit, until the switch responds, the overcurrent permissible for the semiconductor component cannot be exceeded. For driver signal blocking, the thyristor controllability must be ensured for the longest possible period of time up to the point of zero current crossing. Furthermore, the protective device on the load side has to be rated such that it responds faster than the thyristor or rectifier diode blow-out fuses. This is referred to as selectivity.

4.4.6.1 Semiconductor fuses: terms and explanations

Fuse

Fuses are protective elements that melt a fuse element, in doing to opening the electric circuit if the current exceeds a given level during a given period of time.

Fuse mount

This is a fixed integrated part of the fuse that contains the contact socket for the fuse link.

Fuse link

This part of the fuse contains the fusible element and has to be replaced after the fuse has been operational before it can function again (Figure 4.4.16). In semiconductor fuses, the fuse mount is often not needed. In this case, the fuse link and the fuse itself are identical.

Indicator

Device that shows the control state of the fuse link.

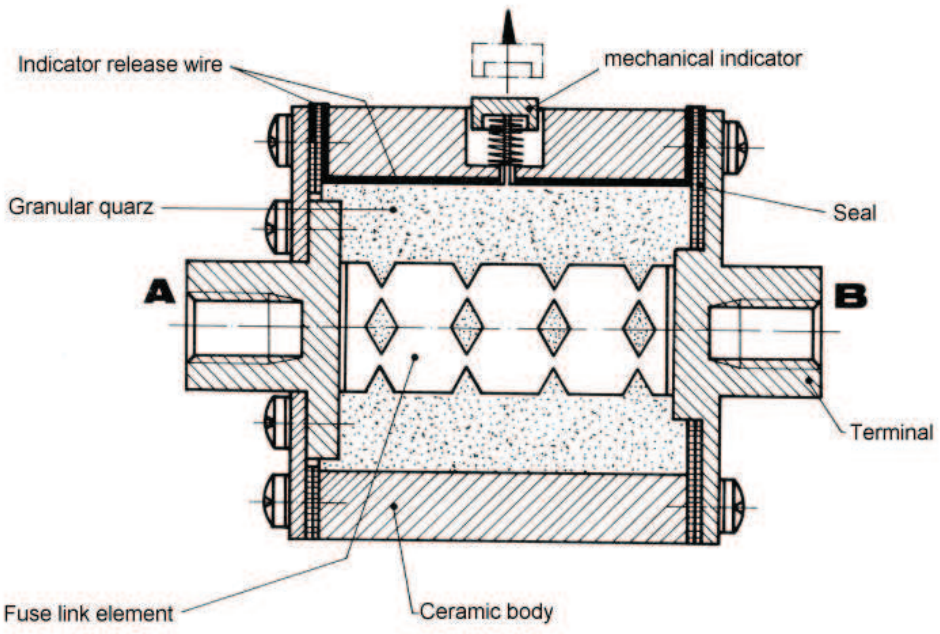


Figure 4.4.16 Cross-section of a semiconductor fuse link

Fuse-link striker

This is released when the fusible element melts in order to activate a signal device or similar device. This might double as the indicator. In circuits with parallel rectifier diodes or thyristors, the response voltage of the fuse-link striker must be less than 1 V.

Rated voltage V_N

Maximum permissible voltage with maximum 10% permissible short-time increase. If the rated voltage is an AC voltage, this will be specified as an effective value. This applies to a sinusoidal voltage of 50 - 60 Hz. For non-sinusoidal voltage, neither the effective nor the crest value of the operating voltage may exceed the rated voltage or their sqrt(2) value√.

Rated current I_N

Maximum permissible operating current with which the fuse mount may be continually subject to without changes that may be detrimental to function.

Rated breaking capacity I_{PM}

Maximum prospective current that a fuse can turn off under certain conditions (e.g. recovery voltage).

Let-through current (of a fuse) $I_{(LT)}$

The maximum instantaneous current which is reached during fuse operation, if this turn-off prevents the prospective current from reaching its maximum value (Figure 4.4.17). Note that this value for current has nothing to do with the forward current of a rectifier diode or thyristor!

Prospective current I_P

Current which occurs if one imagines the fuse being replaced by an impedance-free conducting connection (dotted line in Figure 4.4.17).

Prospective short-circuit current I_{PS}

Effective prospective current under short-circuit conditions directly behind the fuse. This value might be needed to determine the precise arcing i^2t value.

Pre-arc time t_{pa}

Time between the onset of a current that is large enough to melt the fusible element and the emergence of the arc (Figure 4.4.17).

Arcing time t_a

Time that elapses between the generation of the arc and its (final) extinction.

Operating time t_{op}

Sum of the pre-arcing time and the arcing time.

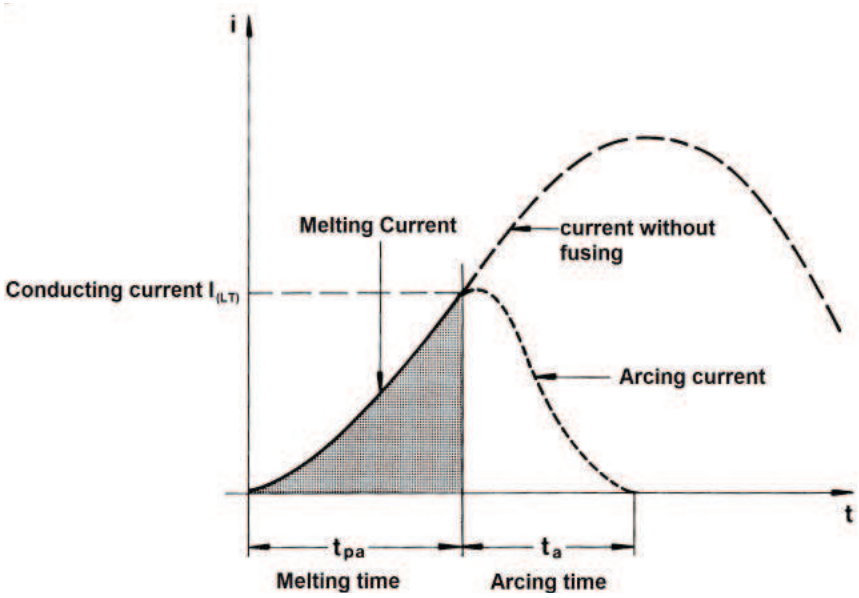


Figure 4.4.17 Current characteristic for short-circuit "turn-off" by a semiconductor fuse with current clamping (let-through current smaller than the peak prospective current); Pre-arc time + arcing time = operating time

Time / current characteristic

Curve of the virtual pre-arc time or operating time as a function of the effective prospective current under certain conditions. This normally applies to 20°C initial temperature.

Pre-arc i²t value $(i^2t)_{pa}$

Integral of the square of the prospective current over pre-arc time:

$$(i^2t)_{pa} = \int_{t_0}^{t_{pa}} I_P^2 \, dt$$

This depends on the initial temperature and the prospective short-circuit current. It is not time-dependent for pre-arc times of less than 10 ms.

Extinction i²t value $(i^2t)_a$

Integral of the square of the prospective current over arcing time:

$$(i^2t)_a = \int_{t_{pa}}^{t_a} I_P^2 \, dt$$

This depends on the recovery voltage, the prospective current and the power factor.

Operating i²t value $(i^2t)_{op}$

Sum of the pre-arc i²t and the arcing i²t values.

Virtual time t_{vpa}, t_{va}, t_{vop}

Resulting time if an i²t value is divided by the square of the prospective current, e.g.:

$$t_{va} = \frac{(i^2t)_a}{I_P^2}$$

In accordance with the various i²t values, virtual values for pre-arc time, arcing time (extinction time) and operating time are obtained.

Switching voltage V_{aM}

Peak voltage which occurs at the terminals of the fuse during fuse operation. This depends on the operating voltage and the power factor of the electric circuit. The quicker a fuse "clears", the higher the switching voltage.

Recovery voltage V_{WRMS}

Voltage that occurs at the terminals of a fuse once the current has cut off.

Current limiting

Short-circuit current cut-off using a fuse, where the let-through current is smaller than the peak prospective short-circuit current (Example Figure 4.4.17). Whether current limiting takes place depends not only on the properties of the fuse but also on the amount of prospective short-circuit current I_{PS}, as well as on the operating frequency. For small I_{PS}, the pre-arc time is longer than a quarter of an oscillation; likewise for operating frequencies greater than around 100 Hz. In this case, current limitation cannot happen.

4.4.6.2 Dimensioning semiconductor fuses

The following fuse-related data are to be borne in mind when dimensioning semiconductor fuses:

- Rated current
- Rated voltage
- Operating i²t value
- Switching voltage

The influence of this data on the choice of suitable fuse is discussed in the following paragraphs in the order given above.

Dimensioning semiconductor fuses on the basis of the rated current

At rated current, a fuse link can be continually loaded under certain circumstances, i.e. at 20°C ambient temperature, unobstructed air convection and maximum 1.6 A/mm² current density in the connected lines. For higher ambient temperatures and smaller wire diameters, as commonly found in converter devices, the current is to be reduced. In almost every case, a reduction to 90% of the rated current level is enough. In enhanced air cooled systems, fuses may be subjected to currents that are greater than the rated current level. Some manufacturers give conversion equations or diagrams for this.

To check that the fuse is not subject to overload under the load and cooling conditions prevalent in the device, manufacturers recommend measuring the voltage for full load once exactly 5 seconds after turn-on (V_{5s}) and once again 2 hours after turn-on (V_{2h}); it goes without saying that this must be done for exactly the same current. Owing to the temperature dependency of the fuse link resistance, these voltage values provide information on the temperature that the fuse link develops in application. The fuse is not overloaded if the following applies:

$$\frac{V_{2h}}{V_{5h}} \cdot \frac{1 + 0{,}004 \cdot T_a}{1{,}14} \leq N$$

Here, T_a always the supply air temperature in °C and N is a constant of the relevant fuse which is given by the manufacturer. This formula may differ slightly from one manufacturer to the next.

The rated current is the effective sinusoidal AC current. For non-sinusoidal current, as is usually the case in semiconductor fuses, the same effective value will normally be permissible. In cases where one is forced to fully utilise the rated current, even if the current is very different from the sine waveform, the manufacturer ought to be consulted.

Semiconductor fuses are used for rated currents of up to 630 A; in some, non-standard cases they are made for up to around 1600 A. For higher operating currents, two fuses have to be connected in parallel. In this case, either fuse mounts with low-tolerance fuse link resistances selected by the manufacturer are to be used or, for non-selected fuse mounts, a maximum of 80% rated current

may be used. In addition, symmetrical wiring is essential, since even the smallest of differences in the distances to the supply point or in line lengths can lead to non-homogenous current distribution. If any doubt exists, the manufacturer should be consulted.

In parallel fuse configurations, not only the rated current naturally doubles, but also the let-through or cut-off current, i.e. the current required to cut-off within a given time. The i²t will quadruple as a result. This applies to both the pre-arc i²t and the operating i²t value.

The rated current continues to apply for frequencies of between 40 and 60 Hz. Below this range, a reduction in current may be required. The manufacturer is to be asked about this. Dimensioning fuses for **short-time** or **intermittent operation** (with or without base load) is problematic. If the duty cycle time t_s (sum of all conduction intervals $t_1 + t_2 + \ldots$ plus any pauses) is less than a minute and the maximum overcurrent is no greater than 2.5 times the rated current, the following mean load current I_{RMS}, which can be calculated from the equation below, can be expected:

$$I_{RMS} = \frac{I_{RMS1} \cdot t_1 + I_{RMS2} \cdot t_2 + \ldots}{t_s}$$

Where I_{RMS1} is the effective current during time t_1 etc.

If the duty cycle time is longer than 1 minute, the area in which the maximum current that occurs is to be seen as continuous current is approached. Depending on the size of the fuse, this is the case for conduction intervals longer than 10 to 20 minutes. Figure 4.4.18 shows an alignment chart used to determine graphically the permissible overcurrent for intermittent operation.

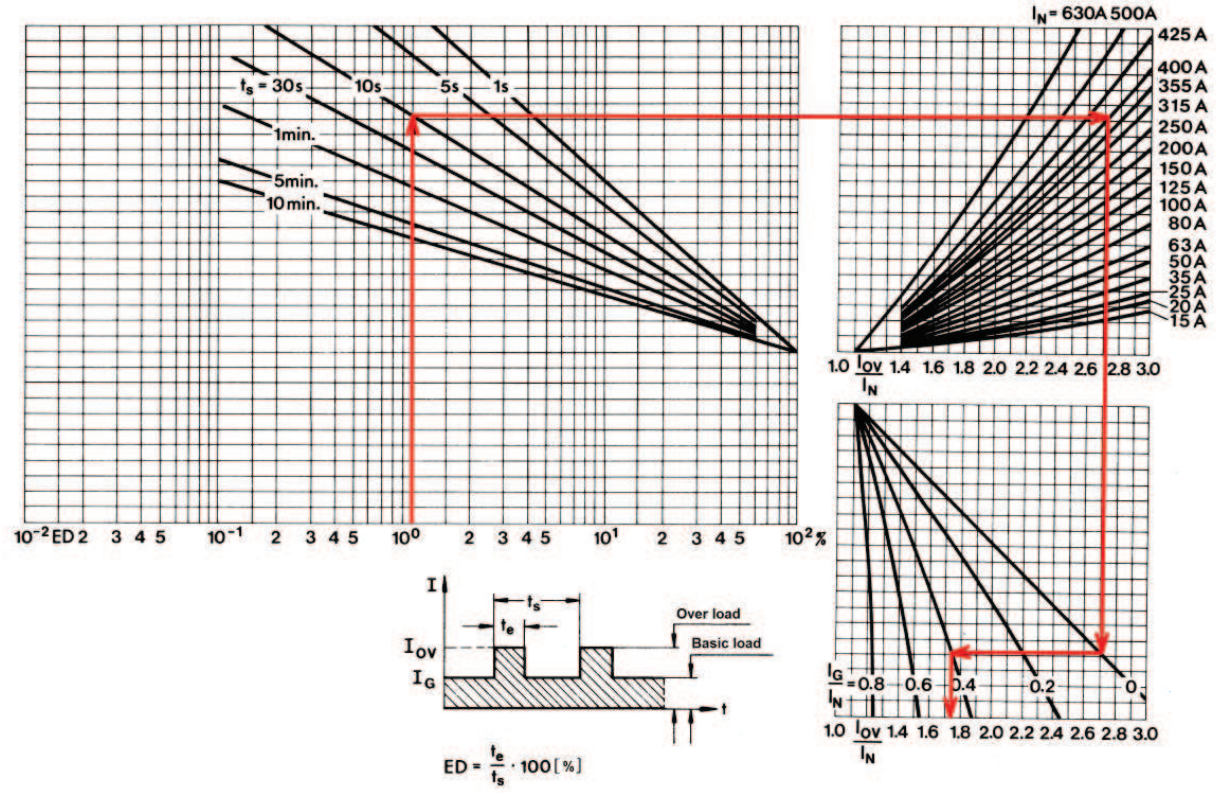


Figure 4.4.18 Alignment chart for the determination of the permissible overcurrent of semiconductors fuses in intermittent operation with and without load

Sample reading: ON duration = 10%, duty cycle time t_s = 10 s, fuse rated current I_N = 400 A, base-load current $I_G = 0.4 \cdot I_N$: Go from the point of intersection of the curve for t_s = 10 s with 10% ON duration in the left-hand diagram and move horizontally to the right to the point of intersection with the curve for I_N = 400 A. From here move vertically to the point of intersection with the curve for $I_G/I_N = 0$. From here, horizontally to the point of intersection with the curve for $I_G/I_N = 0.4$. The corresponding x-coordinate is the desired result: $T_{OV} = 1.75 \cdot I_N$ is the permissible overcurrent.

For overcurrents that are greater than 2.5 the rated current, a differentiation must be made between load that occurs occasionally (seldom) and periodically or frequently at least. For occasional currents, it is enough to use the pre-arc characteristic to determine whether the overcurrent will definitely not cause the fuse link to melt. Here, ensure that this characteristic applies to 20°C initial temperature. In other words, both the increased ambient temperature and the base load from which the overcurrent comes have to be taken into account if necessary. For overcurrents that occur frequently or even periodically and that are greater than 2.5 times the rated current, endurance tests have to be performed to establish the current capability of the fuse. The manufacturer must be consulted if there is any doubt whatsoever.

Dimensioning on the basis of the rated voltage

Semiconductor fuses are usually intended for AC voltage. The rated voltage is always the effective value of sinusoidal AC voltage of 50 - 60 Hz. If a fuse link intended for AC voltage is used for DC voltage, only 0.5-0.8 times the rated voltage is permissible as maximum DC supply voltage, depending on the fuse type. Once again, the manufacturer must be consulted if there is any doubt. Semiconductor fuses are available for rated voltages of up to 2000 V, in some cases for us to 3000 V. If for some reason the series connection of two or more fuses cannot be avoided, the following must be borne in mind:

- The short-circuit current has to be so high that the pre-arc time is shorter than 10 ms.
- A maximum of 90% of the sum of the rated voltages of all fuses may be utilised.
- Fuses that are connected in series must be of the same make and model.
- If one fuse mount has to be replaced, all other fuse mounts in the series connection have to be replaced as well, even if these are fully functioning.

Dimensioning on the basis of the operating i²t value

The operating i²t value of a fuse link is specified by the manufacturer for 20°C initial temperature as a function of the recovery voltage and for a certain prospective short circuit current and power factor (Figure 4.4.19). It reaches its maximum at a recovery voltage equal to the full rated voltage. For DC current, the actual operating value also depends on the time constants τ = L/R of the short-circuit.

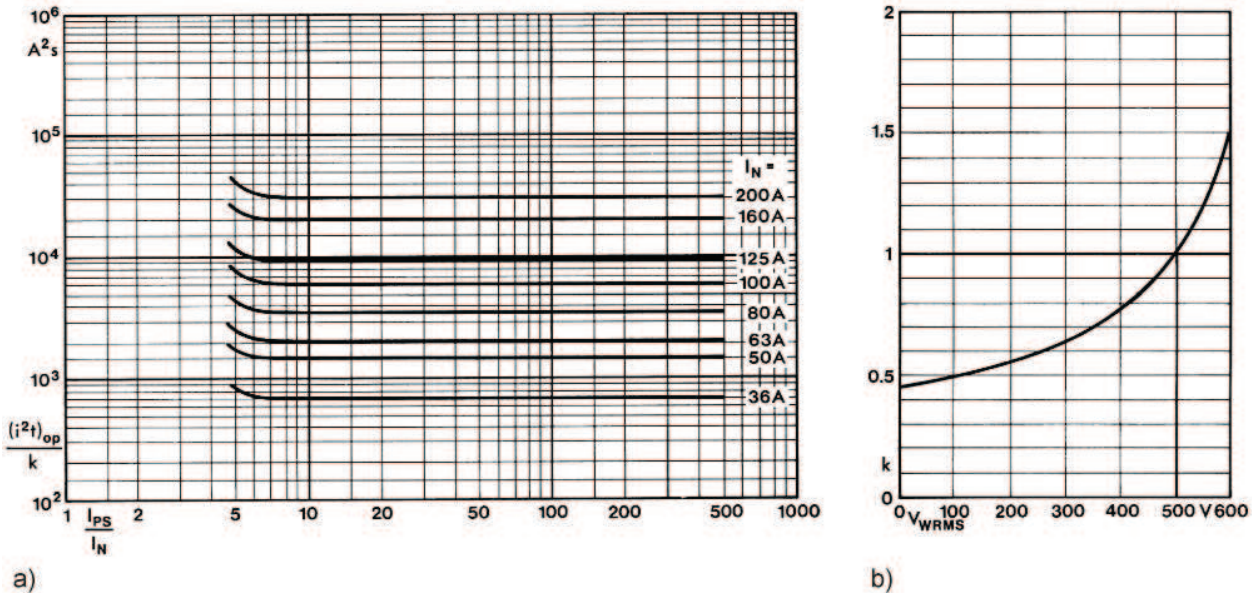


Figure 4.4.19 a) Operating i²t values $(i^2t)_{op}$ divided by the factor k, as a function of the prospective short-circuit current I_{PS}, in relation to the fuse rated current I_N for semiconductor fuses of 35 A - 200 A; b) Factor k as a function of the recovery voltage V_{WRMS}

The curves in Figure 4.4.19 apply to a power factor cos φ = 0.15. Sample reading: The fuse rated current is I_N = 125 A; the prospective short-circuit current I_{PS} = 20 I_N; the recovery voltage V_{WRMS} = 410 V. Diagram a) results in

$$\frac{(i^2t)_{OP}}{k} = 1 \cdot 10^4\,A^2s$$,

diagram b) results in k = 0.8. Therefore: $(i^2t)_{OP} = 0.8 \cdot 10^4\ A^2s = 8000\ A^2s$ is the desired operating i²t value of the fuse.

Besides rated current and rated voltage, the operating i²t value is a critical parameter for selecting a semiconductor fuse. In the given conditions, this value must be smaller than the i²t value for the semiconductor component to be protected. Here, it is normally enough to compare the value for the "cold" fuse (initial temperature 20°C), as always specified, with that of the "cold" semiconductor component (virtual junction temperature T_j = 25°C), since the i²t value of the fuse decreases more than that of the semiconductor component as the pre-load increases.

In the short-circuit region, i.e. at least ten times the rated current, semiconductor fuses have operating times of 5 - 10 ms. The i²t values for rectifier diodes and thyristors apply for 8 - 10 ms. If the fuse operating time is below 8 ms, it is advisable to work on the basis of a 10 - 20% lower i²t value for the semiconductor component. The operating i²t value of the fuse, in contrast, is not time-dependent within this range of time. Furthermore, the strong dependence of the operating i²t value on the power factor of the given short-circuit electric circuit must be observed. Figure 4.4.20 shows a typical example. Short-circuit electric circuit in converter circuits often have power factors of around 0.3 - 0.35. For example, if the operating i²t value of the fuse applies to cos φ ≥ 0.2, virtually every practical application is included.

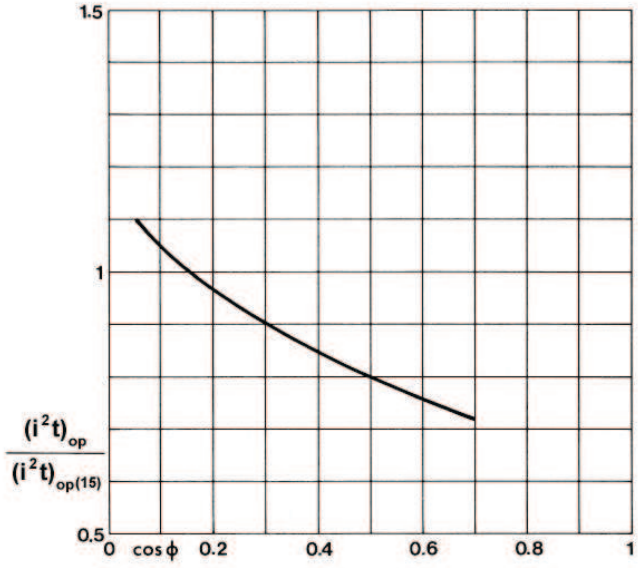


Figure 4.4.20 Operating (i²t) value of a semiconductor fuse, in relation to the value for cos φ = 0.15, shown as a function of the power factor cos φ

As already mentioned, the operating i²t value is given as a function of the recovery voltage (Figure 4.4.19). It must be borne in mind that in converter circuits often two fuses are connected in series in the short-circuit circuit (Figure 4.4.21). In this case, the recovery voltage is only around half the value of the voltage driving the short circuit. Owing to voltage distribution which may be somewhat non-homogenous, it is advisable to use 60% of the voltage rating for each fuse.

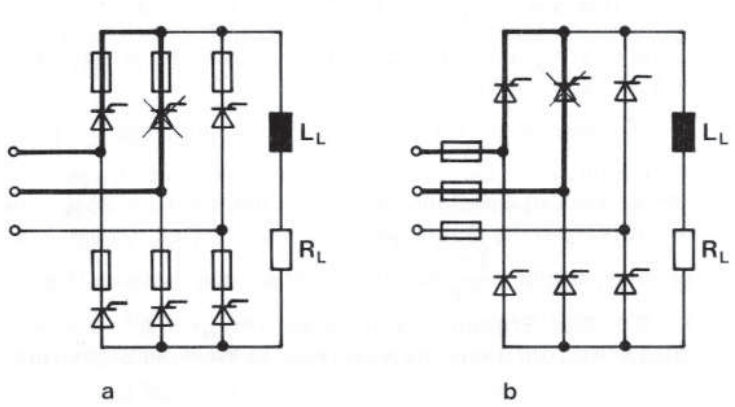


Figure 4.4.21 Short-circuit electric circuit for loss of blocking capability of a thyristor in a 6-pulse bridge circuit with arm fuses (a) and phase fuses (b). In both cases, two fuses are connected in series in the short circuit. This applies to shorts in the load, as can be seen.

Owing to the dependency of the operating i²t value on the recovery voltage in relation to the rated voltage, a particularly low i²t value can normally be achieved for a specified rated current, if a fuse mount with higher rated voltage is used than is actually needed. The recovery voltage is then just a fraction of the rated voltage and the operating i²t value correspondingly low. What should be borne in mind here, however, is that when the rated voltage of the fuse increases, the switching voltage does, too. Thus, in the cases where the switching voltage puts load on the semiconductor components in reverse direction (see Dimensioning on the basis of the switching voltage), this approach has its limits.

If a commutation error occurs in a converter due to a trigger error, the input and output voltage are added together. In this case, the voltage driving the short circuit is then approximately identical to 1.8 times the AC operating voltage. For this reason, the selected fuses have to have correspondingly high rated voltages and the increased recovery voltage has to be taken into account when determining the operating i²t value.

In circuits with parallel connected rectifier diodes and thyristors, if the sole purpose of the fuse is to "remove" a randomly failing semiconductor component from the circuit, the i²t value of the fuse may be greater than that of the semiconductor component which is useless anyway. This value should, however, be selected as small as possible in order to prevent too high a short-circuit current from destroying the failed component externally and the resulting arc from crossing over to adjacent parts.

Dimensioning on the basis of the switching voltage

When a fuse is tripped, an overvoltage will occur across the fuse - this is known as the switching or switched voltage. This value depends on the amount of recovery voltage and the power factor (Example Figure 4.4.23). As shown in the two examples in Figure 4.4.22, there are circuits where the switching voltage of the tripped fuse puts individual thyristors or diodes under load, and circuits where this is not the case. If two fuses are connected in series in a short-circuit electric circuit, their switching voltages may be added together (worst case scenario). For this reason, it is important to establish whether semiconductor components are able to be subjected to such load from the switching voltage and whether double the switching voltage load is permissible. An example of failure of thyristor 2 can be seen in Figure 4.4.22. At the moment of short circuit, thyristors 1 and 5 are conducting. With arm circuit fuses (a) thyristor 4 is subjected to a load equalling the sum of the switching voltages of fuse 1 and 2; thyristors 3 and 6 are subjected to the switching voltage from fuse 2 only. With phase fuses (b), the switching voltages of the fuses are shorted through the conducting thyristor 1 and short-circuited thyristor 2 as opposed to the remaining thyristors.

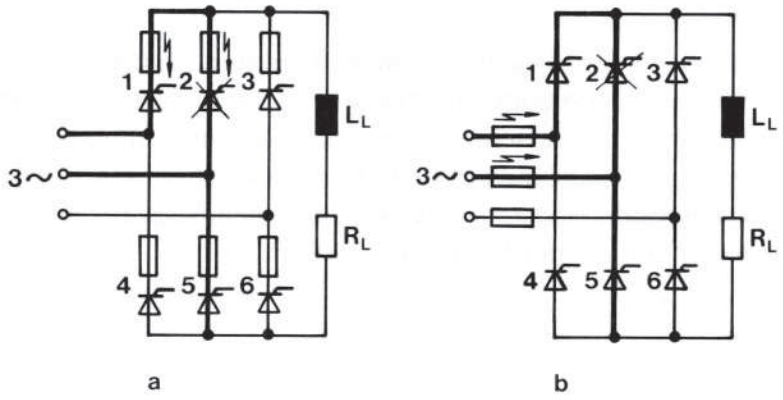


Figure 4.4.22 Switching voltages across the tripped fuses in the case of a short circuit induced by failure of thyristor 2 to block

In bridge circuits, it can be generally said that switching voltages that occur across the arm fuses do not subject the semiconductor components to any load, while with arm fuses the remaining working thyristors or diodes are subjected to the switching voltages of two fuses connected in series. Thus, in this case, semiconductor components with sufficiently high non-repetitive peak reverse voltages are used; it goes without saying, however, that the effect of the overvoltage snubber circuit (which exists in most cases) has to be factored in, too.

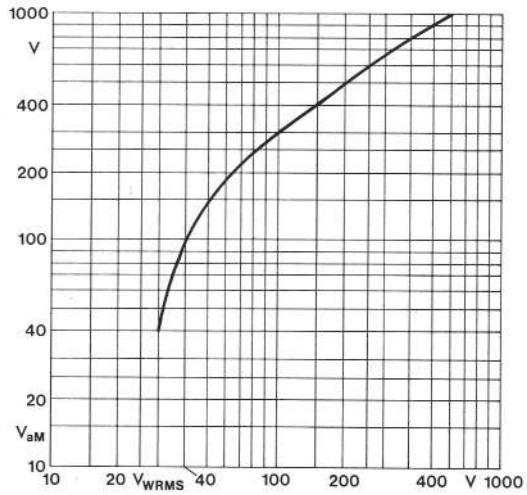


Figure 4.4.23 Peak value V_{aM} of the switching voltage of a semiconductor fuse with 500 V rated voltage as a function of the recovery voltage (effective value) V_{WRMS}

High-speed DC circuit breaker

In rectifiers, where frequent shorts in the load are to be expected, a high-speed DC circuit-breaker is to be integrated on the load side, since the frequent replacing of fuses is costly and time-consuming. The right type of replacement fuses have to be available at all times, etc. The semiconductor fuses needed to provide additional protection in the event of failure of a semiconductor component, on the one hand, and the high-speed DC circuit-breaker, on the other hand, have to be selected such that if the load is shorted, the circuit breaker is activated before any of the semiconductor fuses melt. This is referred to as selectivity of the various short-circuit devices. In this case, selectivity is given if the time / current characteristic of the high-speed DC circuit-breaker runs below the pre-arc / current characteristic (not the operating time / current characteristic!) of the fuse throughout the entire range in question.

4.5 Series and parallel connection of diodes and thyristors

4.5.1 Parallel connection of thyristors

In parallel thyristor circuit arrangements, homogenous current distribution is required from the moment of firing and throughout the entire current flow time. For this purpose, steeply rising trigger pulses of sufficient amplitude (see "Critical current rate of rise"), as well as symmetrical line impedances in the main circuit are needed. When connecting thyristors in parallel, it makes sense to arrange them by smallest possible forward voltage difference. To take into account any remaining asymmetry, we recommend operating the parallel thyristors with no more than 80 % of the calculated maximum rated value for mean forward current. It may be necessary to limit the rate of rise of current in the individual thyristor using chokes.

4.5.2 Series connection of thyristors

To increase the off-state or blocking voltage, thyristors can be connected in series. Here, even voltage distribution must be ensured - using parallel resistors for blocking and off-state and using parallel RC elements for commutation (cf. chapter 4.4.2 Series connection). The parallel resistors have to be rated such that the current that flows through the resistors is is 5…10 times the thyristor off-state current in hot state. To ensure that the thyristor firing is as simultaneous as possible, sufficiently high, steep-rising trigger pulses are required. The voltage load on each thyristor should be at least 10 % lower than for individual operation.

4.5.3 Parallel connection of rectifier diodes

Parallel diode circuits must be as symmetrical as possible in order to achieve even current distribution in the electric circuit (connection point, wiring and wire length); this will rule out substantial differences in line impedances. It makes sense to arrange parallel diodes by the smallest possible difference in forward losses. To take into account any remaining asymmetry, we recommend operating the parallel rectifier diodes with no more than 80% of the calculated maximum rated value for mean forward current.

4.5.4 Series connection of rectifier diodes

To increase the blocking-state voltage, diodes may be connected in series. Especially when "many" diodes are connected in series, in most cases homogenous voltage distribution has to be forced: in blocking-state by using parallel resistors; during commutation using parallel RC elements (cf. chapter 4.4.2 Series connection). The parallel resistors have to be rated such that the current that flows through the resistors is 5…10 times the diode blocking-state current in hot state. These measures may not be necessary in series connected avalanche diodes. The voltage load on each diode should be at least 10% lower than for individual operation.

5 Application Notes for IGBT and MOSFET Modules

5.1 Selecting IGBT and MOSFET modules

The following sections will discuss some questions which are important for a successful selection of power modules containing IGBT or MOSFET. Corresponding information on diodes and thyristors was already included in the chapters 4.1 and 4.2. When selecting power modules for a specific application, the following factors must be taken into consideration:

- voltage carrying capability,
- current carrying capacity of transistors and freewheeling diodes under the feasible cooling conditions and in conjunction with the switching frequency,
- insulation requirements specified by standards, such as insulation between module base plate and terminals and, if available, internal sensors (current, voltage, temperature),

in every stationary and short-time operating condition (e.g. overload). Under no static or dynamic condition may the stress lead to situations where the limits specified for reverse recovery voltage, peak current, chip temperature and maximum rated operating point waveform in the datasheets are exceeded (cf. chapter 3.3.4 "SOA"). The same applies to the limits specified for the module case (e.g insulation voltage, vibration strength, resistance to extreme climates, mounting instructions). In the interest of reliability and sufficient module lifetime, module utilisation must also factor in the intended number of load cycles where significant temperature changes occur (cf. chapter 5.2 and 2.7).

As already detailed in the previous sections, many properties of power modules change in proportion to increases in temperature. Furthermore, dimensioning for "normal operating conditions" assumes that the semiconductor is not used up to the temperature limit $T_{j(max)}$. This is done in order to keep a margin for overload conditions and to be able to revert to the static and dynamic characteristics guaranteed for $T_{j(max)}$ - 25 K in the datasheets.

5.1.1 Operating voltage

5.1.1.1 Blocking voltage

Since most power modules are used in DC voltage links which are AC-voltage supplied via single-phase or three-phase rectifier bridges, the blocking voltages of IGBT and MOSFET modules are adjusted to common line voltage levels for general-purpose use (600 V, 1200 V, 1700 V).

For this reason, a rough selection is first made in the DC link from line voltage (control angle 0° for controlled rectifiers) V_N or no-load direct voltage V_{CC} (V_{DD}) as given in Table 5.1.1:

V_N//V	Rectification	V_{CC},V_{DD}/V	V_{DSS}, V_{CES}/V
24	B2	22	50
48	B2	44	100
125	B2	110	200
200...246	B2	180...221	500, 600
400...480	B6	540...648	1200
575...690	B6	777...932	1700

Table 5.1.1 Line voltage levels, ideal no-load direct voltages and recommendations for the selection of IGBT or MOSFET modules

Afterwards, it is necessary to check whether under maximum voltage stress, i.e.
- the rectified value of the highest static input voltage (rated voltage + rated voltage tolerance) or output voltage of an active line rectifier (cf. chapter 5.1.3) or PFC boost converter,
- transient line overvoltage, as far as it has not yet been reduced by line filters, DC link capacitors and circuits on the DC side (suppressor diodes, snubbers, varistors),
- DC link voltage peaks as a result of oscillations between the inductances and capacitances of the voltage supply, e.g. line filters, chokes, capacitors) under certain operating conditions,
- limiting voltage of a DC link chopper, if available;
- turn-off overvoltage (example: IGBT) V_{CC} + ΔV with

$\Delta V \approx L_\sigma \cdot 0.8\ I_{max} / t_f\ (I_{Cmax})$

where

L_σ:	Sum of all parasitic inductances in the commutation circuit
I_{max}:	Highest collector current to be turned off (mostly for active short-circuit turn-off)
$t_f\ (I_{Cmax})$:	Fall time of collector current at ICmax

the blocking voltage is not exceeded.

In most datasheets, the limit values V_{CES} or V_{DSS} are given as limit values for the chip and not the module. The internal module inductance L_{CE} or L_{DS} (e.g. 20...30 nH), which is also specified in most datasheets, is part of L_σ. Thus, the maximum voltage $V_{CEmax,T}$ or $V_{DSmax,T}$ present at the module terminals must be limited, for example, to

$V_{CEmax,T} \leq V_{CES} - L_{CE} \cdot 0.8\ I_{Cmax} / t_f\ (I_{Cmax})$

i.e. for the DC link voltage including every possible stationary or transient overvoltage, the following must be true, for example:

$V_{CCmax} \leq V_{CES} - L_\sigma \cdot 0.8\ I_{Cmax} / t_f\ (I_{Cmax})$

cf. chapters 3.3 and 3.4.

For IGBT modules, the voltage applied to the chips can be approximately verified by performing measurements between the terminals C_x and E_x.

Such a measurement during active overcurrent / short-circuit switching – as demonstrated in Figure 5.1.1 – shows that IGBT4 chips only permit the switching of relatively low overcurrents in the case of high DC link voltages (e.g. when braking, or feeding from a pulsed rectifier / boost converter) and a low external gate resistance R_{Goff}, without V_{CEmax} being exceeded. To turn off an IGBT4 in the event of a short circuit (e.g. when $I_C \geq 2 \cdot I_{Cnom}$), we therefore recommend a relatively high R_{Goff}, e.g. > 20 Ω for a 300 A module, if the short-circuit current to be turned off is significantly higher than the I_{Cnom} of the module; for details see chapter 3.3.1.

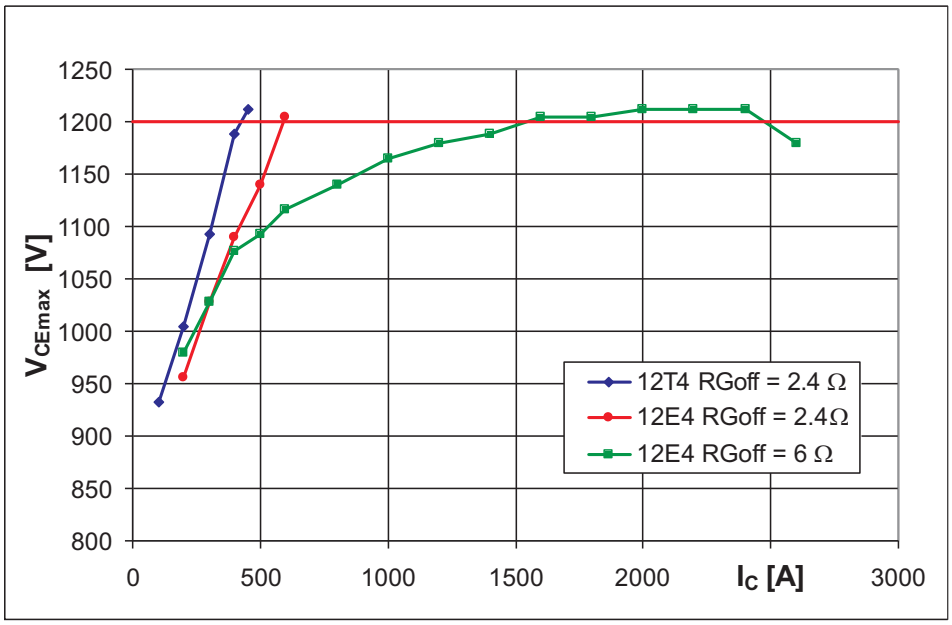


Figure 5.1.1 Voltage load of 450 A IGBT modules at chip level containing T4 or E4 chips, with V_{CC} = 800 V and T_C = 25°C upon short circuit turn-off

In applications with IGBT4 modules, please note that the turn-off overvoltage does not drop as it used to in earlier IGBT generations when the external gate resistance R_{Goff} is slightly increased over the value recommended in the datasheet; rather, it rises to begin with, although t_f virtually does not rise at all. Only for very large R_{Goff} (see above for soft turn-off) is this tendency reversed. Figure 5.1.2 shows the voltage load V_{CEmax} of a 1200 V /400 A IGBT module with T4 chips at chip level during short-circuit turn-off as a function of the external gate resistance R_{Goff} with 2 different case temperatures.

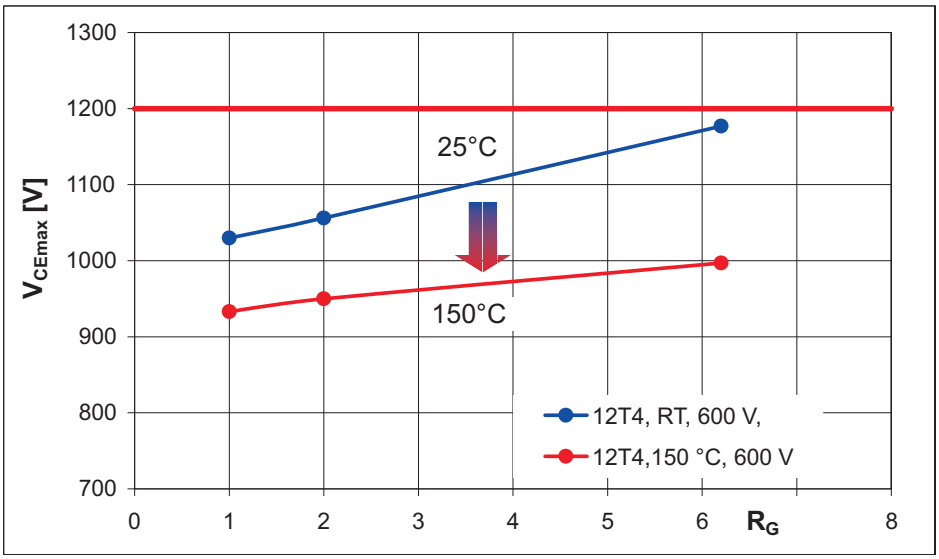


Figure 5.1.2 Voltage load V_{CEmax} of a 1200 V /400 A IGBT module with T4 chips at chip level at V_{CC} = 600 V and turn-off of $I_C = 2 \cdot I_{Cnom}$ = 800 A and different external gate resistances and temperatures

Since the switching times of transistors and diodes rise in proportion to the temperature, di/dt and thus overvoltages increase in all parasitic inductances when the temperature falls. In addition, the reverse recovery voltage of IGBT, MOSFET and freewheeling diodes is reduced in relation to the falling temperature owing to the temperature dependency of the avalanche breakdown voltage. Since V_{CES} and V_{DSS} have been specified for T_C = 25°C in the datasheet, additional margins may have to be considered for use at significantly lower temperatures.

Another property of the current IGBT4 generation is the dependency of the switching overvoltage dV_{CE} on the DC link voltage V_{CC}. As demonstrated in Figure 5.1.3, dV_{CE} rises in line with V_{CC}, meaning that IGBT4 circuit dimensioning must be tested by way of measurements in which the highest possible DC link voltage is applied.

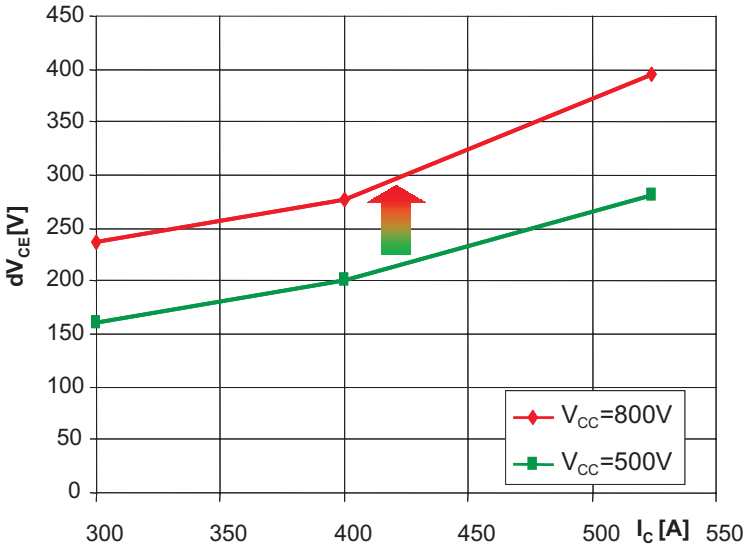


Figure 5.1.3 Impact of the DC link voltage on turn-off overvoltage of a 1200 V / 450 A IGBT module containing "T4" IGBT chips as a function of the collector current for T_C = 25°C

If IGBT – e.g. when impressed onto a short circuit – are turned off even before they reach their static saturation level, the collector current drops particularly steeply, since hardly any minority carriers have to recombine. This results in higher turn-off overvoltages – in particular when Trench IGBT are involved. Figure 5.1.4 demonstrates on the example of a 1200 V-IGBT4 that in the extreme case (high DC link voltage, low temperature) current derating may be necessary if the possibility of extremely short turn-on times (t_p < 5 µs) occurring exists.

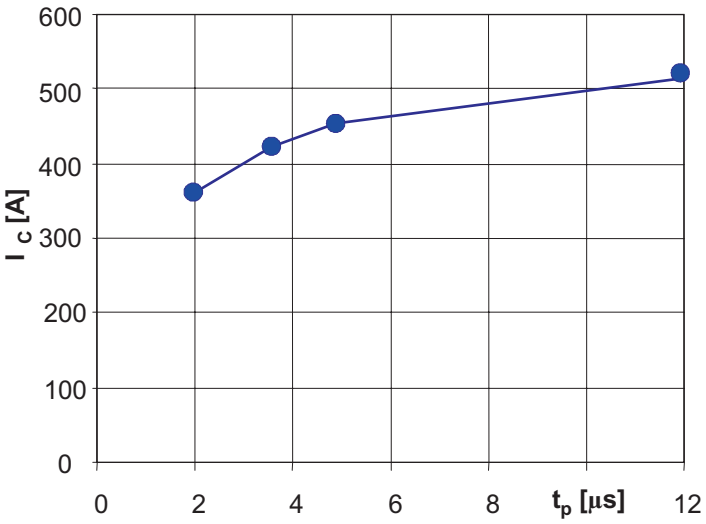


Figure 5.1.4 Necessary current derating to meet $V_{CE(max)}$ for very short turn-on times t_p of a 1200 V-IGBT4 with V_{CC} = 800 V and T_C = 25°C

As demonstrated here, the measurement-based dimensioning requirements for any possible operating condition have become even stricter as a result of the introduction of the IGBT4. This is owing to the fact that the different interaction between application conditions and IGBT properties is far more complex today than for older IGBT generations.

As an additional method of damping overvoltages – especially for DC link voltages > 700 V (for 1200 V-IGBT) and collector currents of some 100 A – we recommend placing suitable foil capacitors near the DC terminals of the module as snubbers (+DC: collector TOP IGBT, -DC: emitter BOT IGBT). Details on their effect and dimensioning are provided in [AN1].

5.1.1.2 Co-ordination of insulation

Co-ordination of insulation brings the voltage stress requirements for electrical insulation in line with the necessary withstand capability. Such co-ordination values, which have been obtained from past experience, have been laid down in standards and must be observed for equipment design.

For this purpose, a distinction is made between high-voltage (> 1000 V) and low-voltage systems (< 1000 V) to start with. For voltages < 1000 V, the (basic) standard EN 60664 (Insulation coordination for equipment within low-voltage systems) is the most crucial. The requirements of this standard are also reflected in product group standards such as EN 50178 (Electronic equipment for use in power installations) or product standards such as EN 61800-5-1 (Adjustable speed electrical power drive systems - Safety requirements). Other standards, e.g. EN 50124-1 (Railway applications - Insulation coordination - Basic requirements), set down even more stringent requirements for certain areas of application. The requirements derived from EN standards differ considerably from those set down in UL standards such as UL 508C (power conversion equipment).

For the purpose of insulation co-ordination, a distinction is made between three hierarchically graded requirements:
- Functional insulation isolates different potentials within a circuit and takes purely functional, but no safety-relevant aspects into account.
- Basic insulation isolates mains supply circuits from earthed exposed parts and is thus vital for safety.
- Reinforced or double (= 2 x basic) insulation isolates mains supply circuits from unearthed exposed parts, on the one hand, and from information technology circuits, on the other hand. This means that no further protection is provided for equipment users, which is the reason why stricter requirements must be in place for insulation.

For power electronics components, such as power modules, this division means the following:
- Functional insulation between the module terminals
- Basic insulation between the module base plate (earthed in the device through the heatsink) and the module terminals
- Reinforced or double insulation between the module terminals and its insulated internal sensors (e.g. for current, voltage, temperature), whose outputs may be connected to the voltage potential of information electronics by the user without any additional measures being taken.

The user must already be aware of the electrical and environmental conditions (cf. chapter 6.2) to be expected when choosing a power module, i.e. at the beginning of the device design stage, since these conditions strongly influence insulation co-ordination.

For this reason, the following requirements must be analysed in addition to selecting the proper voltage class of IGBT or MOSFET in line with the highest peak voltage that will be encountered:

Mains overvoltage category in accordance with EN60664
- Assignment of voltage levels to areas of application, cf. Figure 5.1.5
- Standard: 3 for mains-connected circuits
- Degree of pollution to which the power module is exposed in accordance with EN 60664 or EN 50178,
- depending on application conditions and the cooling concept of the device, for example
- Standard: 2 if condensation is only possible in dead state, otherwise 3

Maximum altitude of application
- The dielectric strength of air is reduced in proportion to the altitude of installation (falling atmospheric pressure) → reducing the insulation capability of clearances in air at the module, cf. chapter 6.2.6.
- Standard: up to 2000 m

Earthing of the supply network
- The earthing type of the supplying network determines the maximum voltage between earth potential and the connection terminals.
- Standard: neutral-earthed TN network

Maximum conductor-to-conductor voltage or highest DC supply voltage
- Is crucial for the selection of the relevant rated voltage
- cf. Figure 5.1.5

Maximum DC link voltage
- It has to be factored in if the DC link voltage can exceed the rectified mains voltage or DC supply voltage, e.g. due to energy feedback, pulse rectifier or inverter operation (e.g. 4Q inverter).

Insulation requirements for sensors and potential isolating spots for isolation from control circuits
- Dependent on the requirements for the circuit to which the sensor is connected
- If the sensor is connected to a mains circuit, functional insulation will be sufficient.
- If connected to a SELV or PELV circuit, the insulation between the load terminals of the module and the sensor must be "reinforced" or "doubled".

Maximum control voltage
- Maximum voltage of the control circuit against earth potential
- Standard: < 50 V

Insulation requirements must be regarded separately for clearances in air, creepage distances and solid insulation. The clearances must be so large that flashover is prevented at all times. The determining factor for this is the highest peak voltage present. For this reason, particular consideration must be given to the overvoltage category of the circuit and its installation height. If this is > 2,000 m above mean sea level, the required clearance in air must be enlarged by an altitude correction factor, cf. Table 6.2.1 in chapter 6.2.6. For reinforced or double insulation, the clearance in air for the next voltage class up is required.

The degree of pollution and the resistance of the materials used with regard to surface currents determine the dimensioning of the creepage distances, which is described by the comparative tracking index (CTI). The more resistant a material is, the shorter the creepage distance may be. What is decisive here is the effective value of the voltage applied, not its peak value. Nevertheless, the creepage distance must be at least as large as the clearance in air. The minimum creepage distances required in standards were usually determined empirically, with only the tracking resistance of PCBs being determined for voltages of up to 1000 V and degrees of pollution 1 and 2 in experimental set-ups and the results adopted as a requirement. This is why the required distances here are much smaller than the CTI of the PCB material would actually require. To attain double or reinforced insulation, the creepage distance assigned to the voltage must be doubled.

Solid insulation is when the insulation distance is not created solely by air or gas. To verify that solid insulation withstands the voltage load, an impulse withstand and partial discharge test is performed. Ideally, the onsetting partial discharge voltage is greater than the maximum peak voltage to be expected (because then partial discharge will never occur) and the intermittent partial discharge voltage is greater than the voltage continuously present. (If the maximum peak voltage is ever exceeded, the partial discharge which now starts must then be safely interrupted again). Some standards require a partial discharge test for reinforced or double insulation only.

In order to ensure that no fault has occurred during the assembly of the module or device, many product or product group standards require a dielectric test. This test does not serve the purpose of verifying that the insulation of the sample has been properly designed.

Maximum value of rated operational voltage to earth (V) a.c. r.m.s. or d.c.	Nominal voltage of the supply system (≤ rated insulation voltage of the equipment)				Preferred values of rated impulse withstand voltages, kV (1.2/50) at 2000 m			
					Overvoltage Category			
					IV	III	II	I
	a.c. r.m.s. (V)	a.c. r.m.s. (V)	a.c. r.m.s. or d.c. (V)	a.c. r.m.s. or d.c. (V)	Origin of installation (service entrance) level	Distribution circuit level	Load (appliance, equipment) level	Specially protected level
50	---	---	12.5, 24, 25, 30, 42, 48	60–30	1.5	0.8	0.5	0.33
100	66/115	66	60	---	2.5	1.5	0.8	0.5
150	120/208 127/220	115, 120, 127	110, 120	220–110, 240–120	4	2.5	1.5	0.8
300	220/380, 230/400, 240/415, 260/440, 277/480	220, 230, 240, 260, 277	220	440–220	6	4	2.5	1.5
600	347/600, 380/660 400/690, 415/720, 480/830	347, 380, 400, 415, 440, 480, 500, 577, 600	480	960–480	8	6	4	2.5
1000	---	660, 690, 720, 830, 1000	1000	---	12	8	6	4

Figure 5.1.5 Insulation test voltages for selected network types, line voltages and overvoltage categories [54]

The above-mentioned standards provide different rating guidelines for the necessary insulation test voltages. Example: Insulation test voltages for basic insulation at a line voltage of 690 V for AC and DC testing according to different standards.

In accordance with EN 50178

Test duration: type test 5 s; routine test 1 s

a) earthed neutral

phase-earth voltage: 690 V/√3 = 398 V: $V_{isol} = 398\ V \cdot 1.5 + 750\ V = 1.35\ kV_{rms}$

b) earthed delta circuit

phase-earth voltage: 690 V $V_{isol} = 690\ V \cdot 1.5 + 750\ V = 1.79\ kV_{rms}$

In accordance with EN 61800-5-1

Test duration: type test 5 s; routine test 1 s

a) earthed neutral

phase-earth voltage: 690 V/√3 = 398 V $V_{isol} = 398\ V + 1200\ V = 1.6\ kV_{rms}$

b) earthed delta circuit

phase-earth voltage: 690 V $V_{isol} = 690\ V + 1200\ V = 1.89\ kV_{rms}$

In accordance with UL 508C

Test duration: 1 min

$V_{isol} = 2 \cdot V_{nominal} + 1000\ V$ $V_{isol} = 2 \cdot 690\ V + 1000\ V = 2.38\ kV_{rms}$

The datasheets for power modules (see, for example, chapters 3.3.1 and 3.4.1, module limit values) specify the **insulation test voltage V_{isol}** - which is tested by means of routine in-production module testing - as the effective value (AC voltage, 50 Hz) between the input terminals / control terminals (all terminals connected) and the insulated module base plate. Test duration varies between 1 s and 1 min. Alternatively, an insulation test can be performed as a DC test for $V_{isol(}DC) = \sqrt{2} \cdot V_{isol}(AC)$. Insulation testing for sensors contained in the module and their environment, as well as for isolation in intelligent modules is done in the same way.

In order to be able to use power modules across multiple applications, manufacturers specify test voltages as high as possible (within the scope of technical feasibility), for example 2.5 kVac/1 min…4 kVac/1 min….4.5 kVac/1 s for 1200 V-IGBT, 4 kVac/1 min…5.6 kV/1 s for 1700 V-IGBT, 6 kV/1 min for 3300 V-IGBT and 10.2 kV/1 min for 6500 V-IGBT. SEMIKRON also tests IGBT and diode modules at 9.5 kV/1 min in line with non-standard customer requirements.

All insulation voltage tests must be performed at an ambient temperature of 15…35°C, a relative humidity of 45…75% and an atmospheric pressure of 860…1060 hPa. The insulation test (dielectric test) is considered passed if no electrical breakdown has occurred, i.e. small leakage currents that occur are irrelevant. Since every insulation test may cause premature damage to the module as a result of partial discharge, the number of tests should be kept low and the test voltage should be no greater than necessary.

Insulation tests under the voltages specified in the datasheets are not to be performed as part of inspections carried out on incoming shipments. Generally speaking, repetitive tests should be dispensed with. If they cannot be avoided, however, a regeneration time of at least 10 minutes must be complied with between 2 tests.

5.1.2 On-state current

The values specified in the datasheets as maximum ratings I_C (collector DC), or I_D (drain DC), at which the maximum rated chip temperature is reached, are formally calculated for a stationary fully controlled transistor according to the following formula:

$$I_C = \frac{T_{j(max)} - T_c}{V_{CE(sat)} \cdot R_{th(j-c)}} \quad \text{(IGBT module)}$$

$$I_D = \sqrt{\frac{T_{j(max)} - T_c}{r_{DS(on)} \cdot R_{th(j-c)}}} \quad \text{(MOSFET module)}$$

at case temperatures T_c = 25°C and 80°C for modules with base plate, or T_s = 25°C and 70°C for modules without base plate; also see the explanations given in the datasheet specifications in chapters 3.3.1 and 3.4. For modules without base plate, T_s substitutes T_c and $R_{th(j-s)}$ substitutes $R_{th(j-c)}$. Values for $R_{DS(on)}$ and $V_{CE(sat)}$ are those that apply at the maximum rated chip temperature $T_{j(max)}$. This information is intended for rough orientation only, since under real operating conditions switching and (low) blocking losses will occur in addition to the forward on-state losses, the case temperature will differ and the static maximum ratings of $R_{DS(on)}$ or $V_{CE(sat)}$ will not be reached during the entire turn-on process.

The IGBT **chip current I_{Cnom}** specified in more recent datasheets is likewise intended for orientation only (rated current of IGBT chips indicated in the chip manufacturer datasheet, multiplied by the number of chips connected in parallel in the module per switch) and is also a DC current (cf. chapter 3.4.1).

The **repetitive peak collector current I_{CRM}** is the maximum rated peak current value present at the collector terminal in pulsed operation, and thus the limit value for maximum current load during periodic switching operation (cf. chapter 3.3.1). I_{CRM} is not dependent on temperature and is limited by the permissible chip current density. In many datasheets I_{CRM} is indicated as $2 \cdot I_{Cnom}$; this corresponds to the former specified limit for collector current I_{CM}. For IGBT4 chips (T4, E4) currently used in SEMIKRON IGBT modules, the chip manufacturer specifies $I_{CRM} = 3 \cdot I_{Cnom}$, but without indicating a permissible pulse width. As shown in relevant tests, repetitive turn-off of such high currents may, however, cause early desaturation of the hottest chips and, consequently, involve high power losses. Therefore, SEMIKRON continues to recommend turning off currents above the permissible value specified with $2 \cdot I_{Cnom}$ within RBSOA as an exception only (e.g. DC link voltage reduction, active clamping, very slow turn-off or turn-off snubber circuit) and retains the previous RBSOA limit of $I_{CRM} = 2 \cdot I_{Cnom}$.

Another on-state current limit is the maximum rated **RMS on-state current value** $I_{t(RMS)}$ of the module structure, averaged over a full cycle of the operating frequency; this is applicable to any current characteristic, conduction angle or cooling conditions. This value is limited by the current carrying capacity of the internal connections and the external terminals of the IGBT module; cf. chapter 3.3.1.

The current limits of freewheeling diodes, i.e. **inverse diode forward current I_F, diode chip current I_{Fnom}** and **peak forward current of the inverse diode I_{FRM}** are defined in the same way as the transistor limit values. The (non-periodic) surge forward current limit I_{FSM} is relevant for the selection of protective measures when operating inverse diodes as line rectifiers. This value defines the forward current surge peak in the form of a 50 Hz sinusoidal half-wave which the diode is able to withstand without being damaged in the event of a malfunction (short-circuit), provided this is does not occur too often during the diode lifetime. The limiting overload characteristics can be used to establish values for different half-wave periods, as well as for several consecutive half sine waves (cf. chapter 3.3.1).

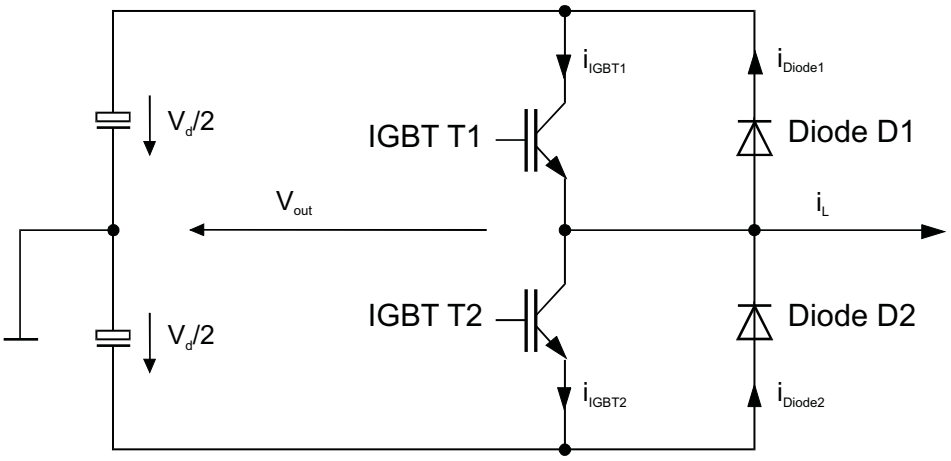
As a rule, the output current of a power electronics circuit that can be gained in field applications is limited by the entire balance of power losses (forward, reverse and switching losses) of the transistors and freewheeling diodes in the power modules and the possible heat dissipation from the chips through the module and the cooling system to the cooling medium:
- There is no stationary or dynamic operating condition (with the exception of short-circuit turn-off which may only be repeated to a limited extent; cf. chapter 3.3.4 "SCSOA"“) where the maximum rated chip temperature of IGBT, diodes or MOSFET may be exceeded.
- The temperature gradients that occur due to load and temperature changes must not result in wear-induced module destruction before the end of the expected module lifetime; cf. chapter 2.7.

Further limits also exist. These include the following:
- the switching capacity of transistors in operation and in the event of overloads up to the maximum current being turned off, i.e. within the limits of the rated transistor operating areas; cf. chapter 3.3.4
- the necessary selectivity of active and passive overcurrent protection measures
- the switching overvoltages that depend on the current being turned off (cf. chapter 5.1.1)

5.1.3 Stress conditions of freewheeling diodes in rectifier and inverter mode

In order to be able to feed energy back to the grid, drive converters are often rated for 4-quadrant operation, which means they consist of 2 topologically identical converters at the line side (LSC: **L**ine **S**ide **C**onverter) and at the machine side (MSC: **M**achine **S**ide **C**onverter). Depending on the direction of current flow (rectifier or inverter mode), the freewheeling diodes of the two converters are under different stresses as regards resultant power dissipation for the same power transmitted.

In inverter mode, the average energy flow is directed from the DC link to the AC side, i.e. the AC side supplies a consumer, e.g. a three-phase motor or a power system. On the other hand, the average energy flow in rectifier mode is directed from the AC side to the DC link. In this case, the converter works as a pulse rectifier connected to an AC mains or generator. Although the power performance in both cases is the same, the power semiconductors are subject to different power losses essentially due to the opposite phase shift between the voltage and current fundamental frequency on the AC side that occurs in rectifier or inverter mode. This can be explained using to the basic circuit in Figure 5.1.6.



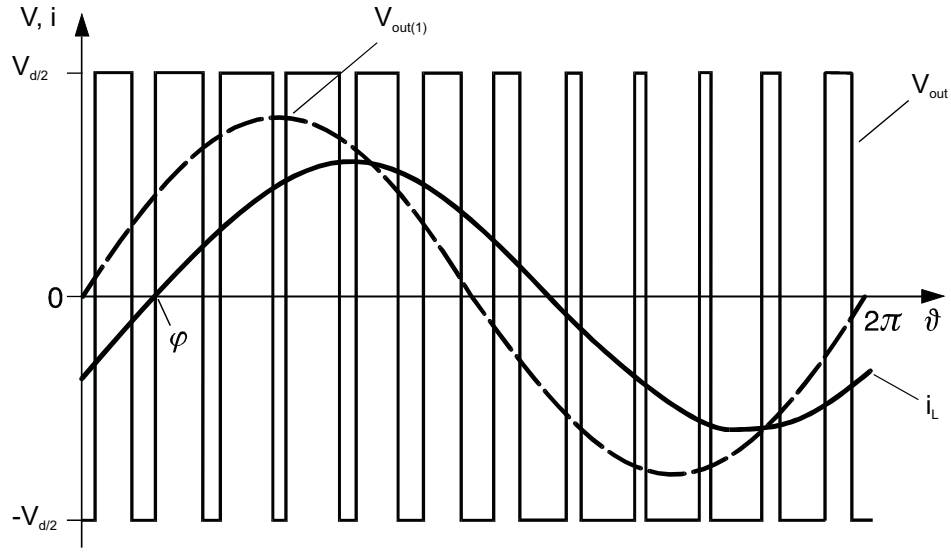


Figure 5.1.6 Basic circuit of a converter phase with IGBT and freewheeling diodes
The following can be seen:
if v_{out} = positive and $i_L > 0$: current flow through IGBT 1
if v_{out} = negative and $i_L > 0$: current flow through diode 2
if v_{out} = positive and $i_L < 0$: current flow through diode 1
if v_{out} = negative and $i_L < 0$: current flow through IGBT 2

Consequently, the IGBT and freewheeling diode on-state power losses occurring at a given RMS current value are dependent on the cos φ between voltage and current fundamental frequency, as well as on the modulation factor m of the converter (this determines duty cycles).

In inverter mode the following applies: $0 \leq m \cdot \cos \varphi \leq 1$. Power dissipation in semiconductors reaches its limits if $m \cdot \cos \varphi = 1$. In this case, maximum on-state losses and, therefore, total losses in the IGBT have been reached, whereas losses in the freewheeling diodes are at their minimum.

In rectifier mode the following applies: $0 \geq m \cdot \cos \varphi \geq -1$. Power dissipation in semiconductors reaches its limits if $m \cdot \cos \varphi = -1$. In this case, minimum on-state losses and, therefore, total losses in the IGBT have been reached, whereas losses in the freewheeling diodes are at their maximum. Applied to the characteristics in Figure 5.1.6, this situation would be given if the pulse rectifier converts pure active power from the line – referred to the fundamental component – and the neutral point of the line is connected to the centre point of the DC link voltage. Figure 5.1.7 graphically illustrates these interrelations in an example.

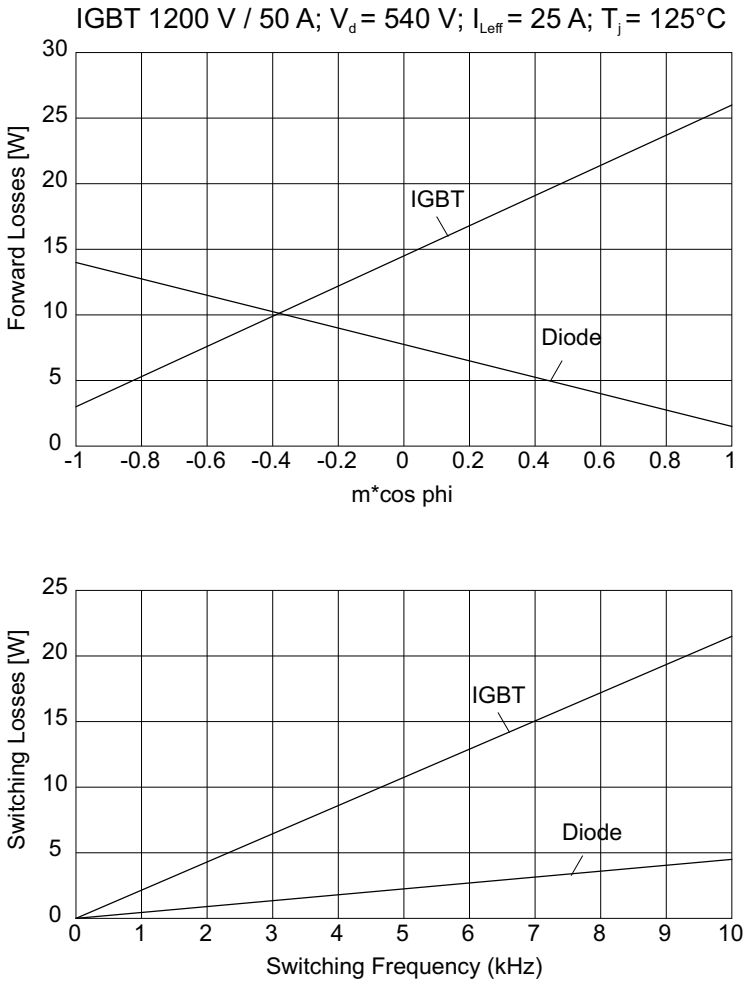


Figure 5.1.7 Switching and forward on-state losses of IGBT and freewheeling diode in a frequency converter

At given DC link voltage and RMS AC current values, the switching losses of the components are merely linearly dependent on the switching frequency (Figure 5.1.7). Most available IGBT and MOSFET modules with integrated freewheeling diodes are dimensioned for use in inverters in reference to the power losses that can be dissipated at rated current (e.g. cos φ = 0.6...1). Due to their reduced on-state and total losses, diodes have been designed for a far lower dissipation of power losses than for IGBT (ratio IGBT : Diode ≈ 2...3:1). When dimensioning a converter for use as a pulse rectifier, the diode load must be taken into particular consideration.

5.1.4 Switching frequency

Figure 5.1.8 shows the measured turn-on and turn-off behaviour of a power MOSFET and an IGBT module for one specific operating point. Apart from the characteristics for v_{DS} or v_{CE} and i_D or i_C, the instantaneous power dissipation values p(t) have been determined by multiplying instantaneous current and voltage values; the integral of p(t) reflects the total MOSFET and IGBT losses over the entire period. The total losses in the power module are composed of the losses of all transistors and freewheeling diodes contained in the module.

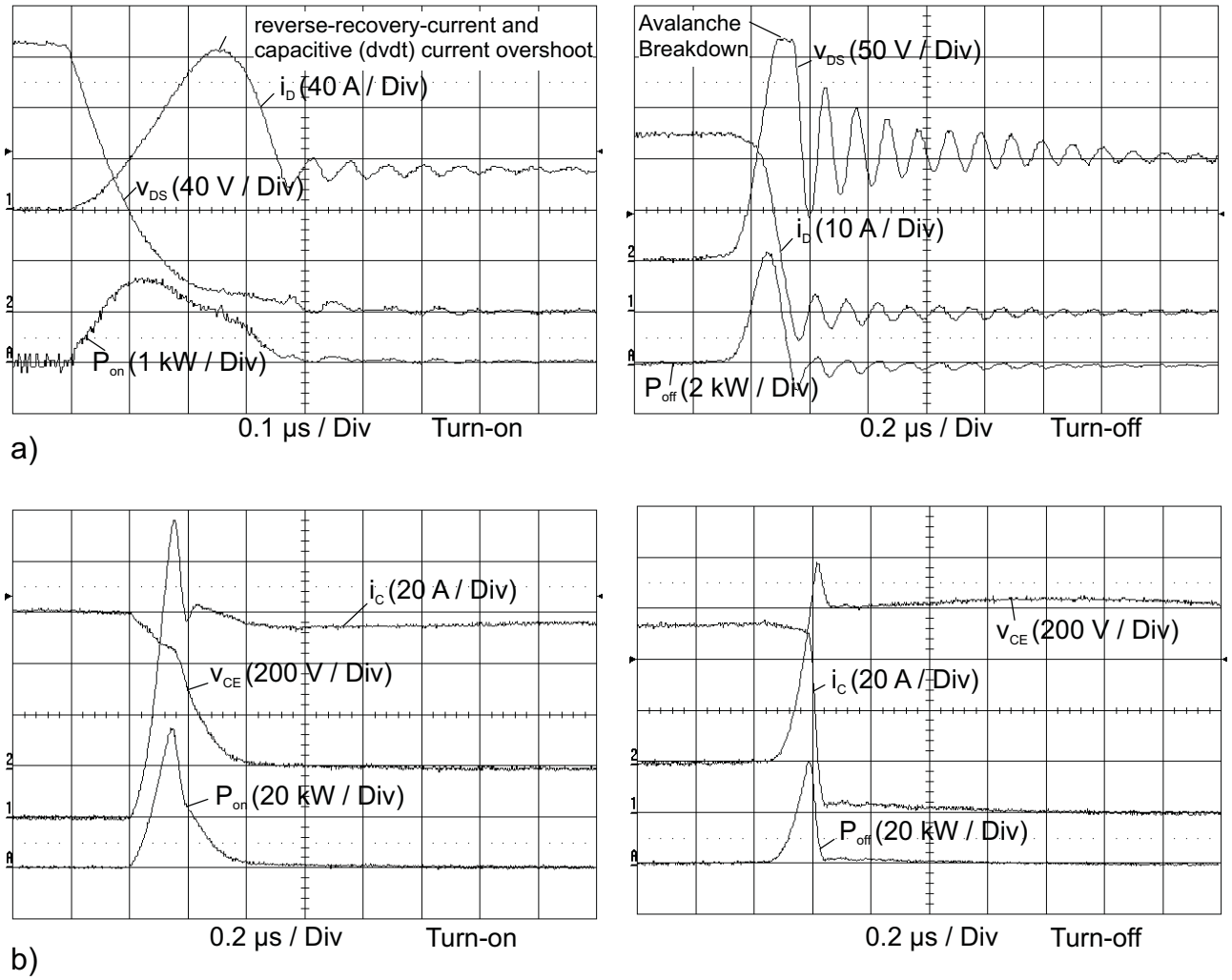


Figure 5.1.8 Measured switching processes (hard turn-on and turn-off under ohmic-inductive load)
a) Power MOSFET module; b) IGBT module

A qualitative explanation of current and voltage characteristics is given in chapters 2.4, 3.3 and 3.4. Since switching losses increase in proportion to the frequency, they limit the switching frequency, although this can still be increased by oversizing the power module.

Other limitations may be set by the transistor turn-on and turn-off delay times $t_{d(on)}$, $t_{d(off)}$, the reverse recovery times of the freewheeling diodes, the driver control power which increases proportionate to the frequency, as well as by the minimum turn-on, turn-off or dead times necessary for driver, interlocking, measuring, protection and monitoring functions. If switching losses are to be shifted to passive networks (snubbers) or overvoltages are to be limited by snubbers, the recharge time of such networks required after low-loss switching has to be considered as deadtime.

Switching times of MOSFET and IGBT power modules are within the range of some ns to some 100 ns. While the switching times of MOSFET and older IGBT can be influenced within relatively wide limits by control parameters, many new Trench IGBT provide this option for turn-on to a limited extent only and for turn-off barely at all (cf. Figure 5.1.9), unless drastic increases in switching losses – owing to very high gate resistances – are accepted.

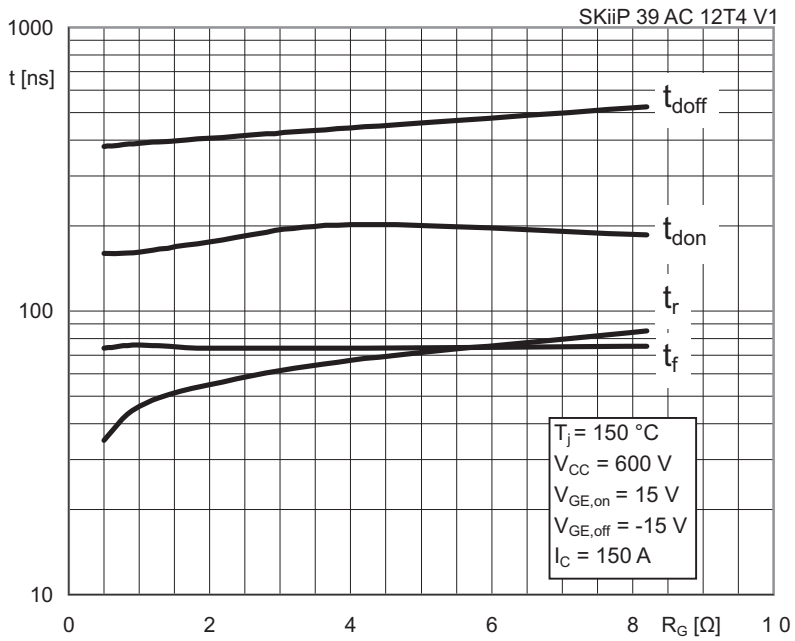


Figure 5.1.9 IGBT4 switching times dependent on the external gate resistance R_G

As transistor switching time decreases, the influence of parasitic inductances and the real properties of the freewheeling diodes (t_{rr}, Q_{rr}) end to become limiting factors for the switching frequency in case of hard switching and higher operating voltages. This is because, for example,
- the turn-off velocity, limited by the permissible switching overvoltage, and
- the turn-on velocity, limited by the permissible peak current (load current + reverse recovery current of the freewheeling diode depending on di/dt)

often determine the maximum values of the feasible switching speed.

Moreover, transistor dv/dt and di/dt values, which are prone to be too steep within the high power range, might cause electromagnetic interference and dv/dt-dependent insulation problems under certain loads (machines). For this reason, an optimum compromise between the requirements resulting from the application (e.g. frequency out of range of audibility), switching times / losses, power dissipation and EMC features has to be looked for when determining switching frequency and (if possible) switching times.

Today, the following guideline values for switching frequencies in standard modules apply:

for hard switching:	MOSFET modules	low-voltage	up to 250 kHz
		high-voltage	up to 100 kHz
	IGBT modules	600 V	up to 30 kHz
		1200 V	up to 20 kHz
		1700 V	up to 10 kHz
		3300 V	up to 3 kHz
for soft switching:	MOSFET modules	low-voltage	up to 500 kHz
		high-voltage	up to 250 kHz
	IGBT modules		up to 150 kHz

5.2 Thermal dimensioning for power transistors

All explanations in this chapter refer to IGBT modules. All of the considerations and calculations can also be applied to MOSFET modules, provided the designation indices are replaced by those for MOSFET. MOSFET do not have a threshold voltage for the on-state characteristic, meaning that these terms are omitted from formulae ($V_{CE0} \rightarrow V_{DS0} = 0$). In reverse mode (freewheeling diode), a differentiation must be made as to whether only the body diode is conductive or whether the MOSFET has also been actively turned on for freewheeling operation in reverse direction. The

following explanations look predominantly at hard-switching converters connected to a DC voltage link. Chapter 5.1 outlines thermal dimensioning processes for rectifier components.

5.2.1 Individual and total losses

In power electronics, both IGBT and diodes are operated as switches, taking on various static and dynamic states in cycles. In any of these states, one power dissipation or energy dissipation component is generated, heating the semiconductor and adding to the total power losses of the switch. Suitable power semiconductor rating and cooling measures must be taken to ensure that the maximum junction temperature specified by the manufacturer is complied with at any standard moment of converter operation. Exceptions to this are short-circuit turn-off and surge current loads where $T_{j(max)}$ is usually exceeded. Such events may, however, happen very seldom only during the entire component lifetime. Following such cases, the components must be allowed sufficient time to cool down.

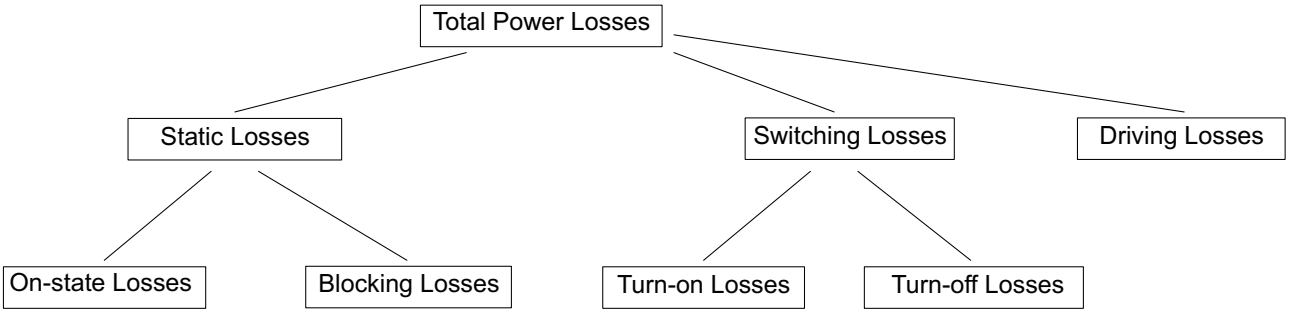


Figure 5.2.1 Individual power losses of power modules used as switches

IGBT

Owing to the fact that forward blocking losses and driver losses account for a small share of the total power dissipation only, they can normally be neglected. In case of high blocking voltages (> 1 kV) and/or high operating temperatures (>= 150°C), blocking losses may gain importance and may even result in thermal runaway owing to the exponentially rising reverse currents. Often, control losses must only be taken into account for low-volt MOSFET applications with very high frequencies.

On-state power dissipation ($P_{cond(T)}$) is dependent on:
- the load current (over output characteristic $V_{CE(sat)} = f(I_C, V_{GE})$)
- the junction temperature
- the duty cycles

At given control parameters (R_G, V_{GG}) and neglecting parasitic effects (L_S, C_{load}), turn-on and turn-off losses (P_{on}, P_{off}) are dependent on:
- the load current and the electric load type (ohmic, inductive, capacitive)
- the DC link voltage
- the junction temperature
- the switching frequency

Total losses are composed as follows:

$$P_{tot(T)} = P_{cond(T)} + P_{on} + P_{off}$$

Freewheeling diode

Since it only accounts for a minor share of the total power dissipation, reverse blocking power dissipation may also be neglected in this case. The same constraints apply as for IGBT. Schottky diodes might be an exception here owing to their high-temperature blocking currents. Turn-on power dissipation is caused by the forward recovery process. As for fast diodes, this share of the losses may be neglected as well.

On-state power dissipation ($P_{cond(D)}$) is dependent on:

- the load current (over output characteristic $V_F = f(I_F)$),
- the junction temperature
- duty cycles.

At given control parameters of the IGBT commutating with the diode, and neglecting parasitic effects (L_S), turn-off losses (P_{rr}) are dependent on:
- the load current
- the DC link voltage
- the junction temperature
- the switching frequency

Total losses are composed as follows:

$$P_{tot(D)} = P_{cond(D)} + P_{rr}$$

The total losses of a module $P_{tot(M)}$ are obtained by multiplying the individual losses with the number of switches n integrated in the module:

$$P_{tot(M)} = n \cdot (P_{tot(T)} + P_{tot(D)})$$

5.2.1.1 DC/DC converters

Owing to the constant duty cycle, DC/DC converter losses can be relatively easily calculated under stationary conditions. Values for switching losses at rated conditions / reference values, as well as IGBT and diode forward voltage drops are specified in the datasheets. They must be converted to the operating point in the circuit. The two basic circuits - step-down converter and boost converter - are the basic elements of numerous, more complex applications.

Step-down converter

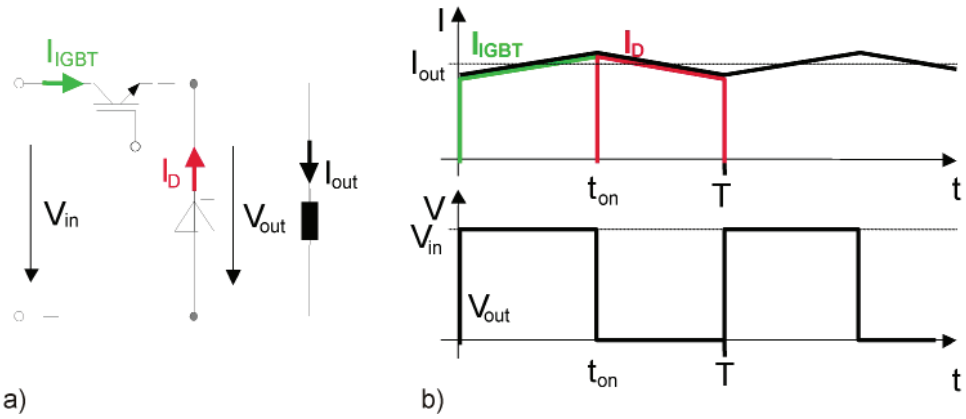


Figure 5.2.2 Step-down converter with ohmic-inductive load, a) Circuit; b) Current and voltage curve

Figure 5.2.2 shows a circuit diagram of a step-down converter with characteristics generated under ohmic inductive load. A high input voltage V_{in} is converted to a low mean output voltage V_{out}. During steady circuit state, the IGBT losses at a given operating point can be calculated as follows:

On-state power dissipation: $$P_{cond(T)} = \frac{1}{T}\int_0^{t_1} i_C(t) \cdot v_{CE}(t)\, dt$$

Neglecting the load current ripple and mapping the on-state characteristic using an equivalent straight line from V_{CE0} and r_{CE} will result in:

$$P_{cond(T)} = (I_{out} \cdot (V_{CE0(25°C)} + TC_V \cdot (T_j - 25°C)) + I_{out}^2 \cdot (r_{CE(25°C)} + TC_r \cdot (T_j - 25°C)))\, DC_{(T)}$$

Switching losses: $P_{sw} = f_{sw} \cdot (E_{on}(V_{in}, I_{out}, T_j) + E_{off}(V_{in}, I_{out}, T_j))$

$$P_{sw(T)} = f_{sw} \cdot E_{on+off} \cdot \left(\frac{I_{out}}{I_{ref}}\right)^{Ki} \cdot \left(\frac{V_{in}}{V_{ref}}\right)^{Kv} \cdot (1 + TC_{Esw} \cdot (T_j - T_{ref}))$$

where

I_{out}:	Average load current
$DC_{(T)}$:	Transistor duty cycle (duty cycle = $t_{on}/T = V_{out}/V_{in}$);
f_{sw}:	Switching frequency
TC_V, TC_r	Temperature coefficients of the on-state characteristic
I_{ref}, V_{ref}, T_{ref}:	Reference values of the switching loss measurements taken from the datasheet
K_i:	Exponents for the current dependency of switching losses ~1
K_v:	Exponents for the voltage dependency of switching losses ~1.3...1.4
TC_{Esw}:	Temperature coefficients of the switching losses ~ 0.003 1/K.

Temperature coefficients of the on-state characteristic can be calculated from 25°C and the hot values of the datasheet characteristic, e.g. for TC_V applies:

$$TC_V = \frac{V_{CE0(125°C)} - V_{CE0(25°C)}}{125°C - 25°C}$$

Similarly, the following applies to the diode:

On-state power dissipation: $P_{cond(D)} = \frac{1}{T}\int_{t_1}^{T} v_F(t) \cdot i_F(t)\, dt$

$$P_{cond(D)} = (I_{out} \cdot (V_{F0(25°C)} + TC_v \cdot (T_j - 25°C)) + I_{out}^{\,2} \cdot (r_{F(25°C)} + TC_r \cdot (T_j - 25°C)))DC_{(D)}$$

Turn-off power dissipation: $P_{rr} = f_{sw} \cdot E_{rr}\,(V_{in}, I_{out}, T_j)$

$$P_{sw(D)} = f_{sw} \cdot E_{rr} \cdot \left(\frac{I_{out}}{I_{ref}}\right)^{Ki} \cdot \left(\frac{V_{in}}{V_{ref}}\right)^{Kv} \cdot (1 + TC_{Err} \cdot (T_j - T_{ref}))$$

where

$DC_{(D)}$:	Diode duty cycle (duty cycle for continuous current = $(T\text{-}t_{on})/T$)
K_i:	Exponents for the current dependency of switching losses ~0.6
K_v:	Exponents for the voltage dependency of switching losses ~0.6
TC_{Err}:	Temperature coefficients of the diode switching losses ~ 0.006 1/K.

The calculation of IGBT and diode on-state power dissipation is based on an ideal duty cycle (neglecting the share the switching time contributes to the total cycle duration).

Boost converter

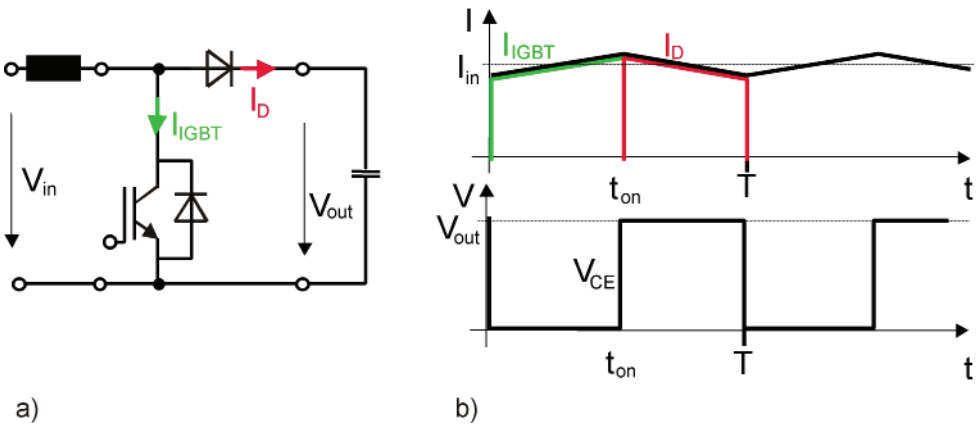


Figure 5.2.3 Boost converter with capacitive load, a) Circuit; b) Current and voltage curve

A boost converter (Figure 5.2.3, Booster) converts a low input voltage V_{in} to a higher output voltage V_{out}. Power dissipation can be calculated along similar lines to those for the step-down converter. The current flowing through the components is now the input current of the circuit, and switching operations are carried out against the high output voltage V_{out}.

$$P_{cond(T)} = (I_{in} \cdot (V_{CE0(25°C)} + TC_v \cdot (T_j - 25°C)) + I_{in}^2 \cdot (r_{CE(25°C)} + TC_r \cdot (T_j - 25°C)))DC_{(T)}$$

$$P_{sw(T)} = f_{sw} \cdot E_{on+off} \cdot \left(\frac{I_{in}}{I_{ref}}\right)^{Ki} \cdot \left(\frac{V_{out}}{V_{ref}}\right)^{Kv} \cdot (1 + TC_{Esw} \cdot (T_j - T_{ref}))$$

$$P_{cond(D)} = (I_{in} \cdot (V_{F0(25°C)} + TC_v \cdot (T_j - 25°C)) + I_{on}^2 \cdot (r_{F(25°C)} + TC_r \cdot (T_j - 25°C)))DC_{(D)}$$

$$P_{sw(D)} = f_{sw} \cdot E_{rr} \cdot \left(\frac{I_{in}}{I_{ref}}\right)^{Ki} \cdot \left(\frac{V_{out}}{V_{ref}}\right)^{Kv} \cdot (1 + TC_{Err} \cdot (T_j - T_{ref}))$$

where

$DC_{(T)}$: Transistor duty cycle (duty cycle = $t_{on}/T = 1\text{-}V_{in}/V_{out}$);

$DC_{(D)}$: $1\text{-}DC_{(T)}$

5.2.1.2 PWM voltage inverter

Figure 5.2.4 shows ideal characteristics of an inverter phase for a sinusoidal pulse width modulation (PWM).

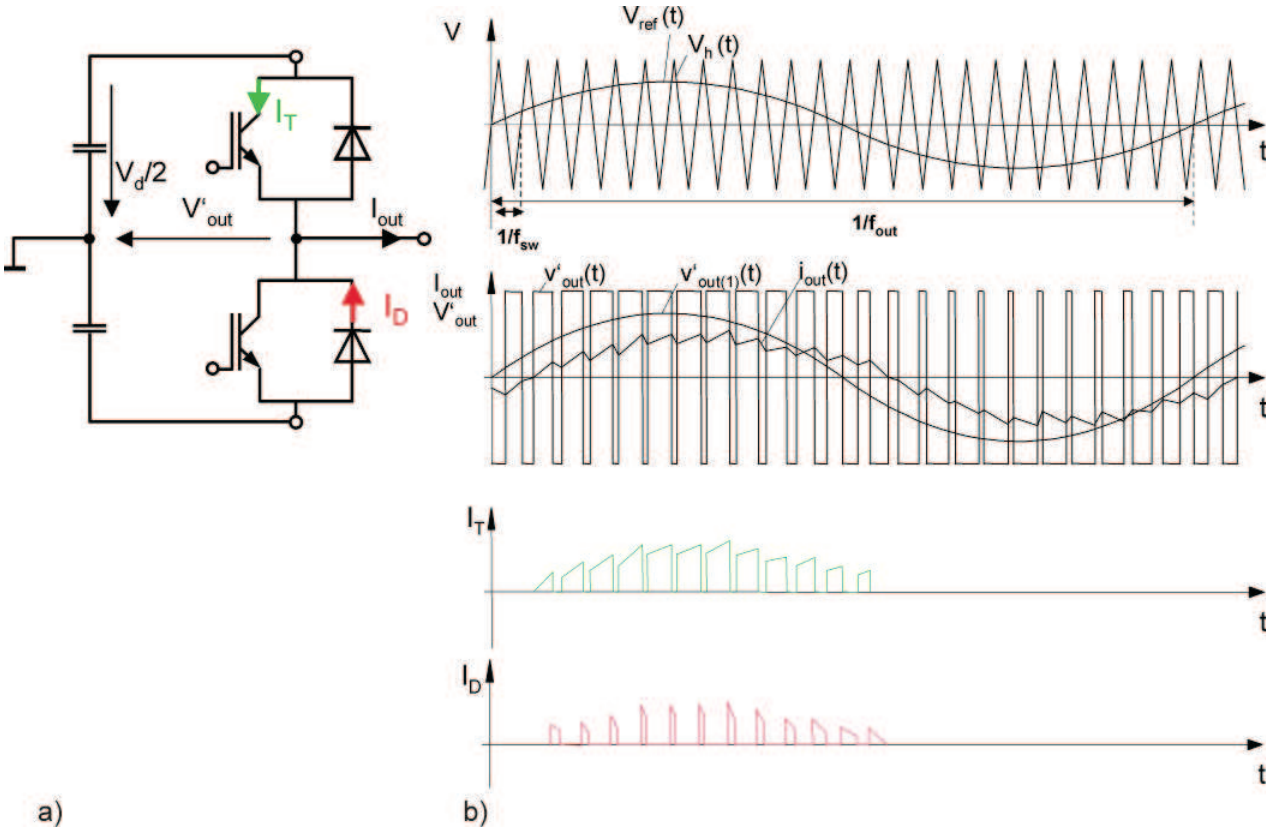


Figure 5.2.4 a) Phase module of a PWM inverter, b) Pulse pattern generation by means of sine/delta comparison, output voltages and currents

According to the conventional approach, the pulse pattern is generated by comparing a sinusoidal reference voltage V_{ref} to a delta-shaped auxiliary control voltage V_h (Figure 5.2.4). The reference voltage sets the fundamental frequency of the AC parameters f_{out} and the auxiliary control voltage the switching or pulse frequency of the switches f_{sw}. The intersections of reference and auxiliary control voltage are the basis for switching times in the converter phase. Amplitude V_{ref} determines

the voltage utilisation or the degree of converter modulation. Up to a ratio of $V_{ref} = V_h$, this is called linear modulation, where the modulation factor m <= 1. The modulation factor refers to the virtual neutral point of the load (phase-neutral) and a virtual centre point of the DC link voltage. It expresses the ratio between the fundamental amplitude of the AC voltage and 50% of the DC link voltage.

$$m = \frac{\hat{V}_{out(1)}}{\frac{V_d}{2}}$$

$\hat{V}_{out(1)}$ is the amplitude of the fundamental harmonic of the phase voltage to neutral

The phase shift between the fundamental harmonics of AC current and voltage is described by the angle φ. In inverter mode (energy flow from DC to AC) $\cos(\varphi) > 0$ applies; in rectifier mode (energy flow from AC to DC) $\cos(\varphi) < 0$ applies, i.e. it is negative.

The current and voltage characteristics for IGBT and diodes will turn out to be identical yet time-shifted due to the symmetrical structure of the inverter circuit. It is therefore enough to consider just one IGBT and one diode with regard to loss evaluations. Inverter losses can then be determined by multiplying the result by the corresponding number of IGBT/diodes (4 - single-phase or 6 - three-phase). In contrast to the calculations made in chapter 5.2.1.1, duty cycle, load current and junction temperature are not constant under static circuit conditions, but vary depending on the fundamental frequency of the AC side (e.g. 50/60 Hz). This means that the switching losses and on-state power dissipation of IGBT and diodes vary in time and call for a more in-depth analysis of system power losses. Precise results can thus only be expected insofar as the simplifications made are applicable, or deviations are still acceptable [55].

The following simplifications are assumed:
- transistor and diode switching times are neglected
- junction temperatures are temporally constant (permissible f_{out} = ~ 50 Hz)
- linear modulation
- the switching frequency ripple of the AC current (sinusoidal current) is neglected
- $f_{sw} >> f_{out}$

In a pure sine/delta comparison, the switching interlock time t_d with $f_{sw} \cdot t_d * V_{CC}/2$ at the voltage-time area of the output voltage would be missing. An upstream regulator would balance the missing voltage by lengthening the control pulses, so that the voltage required to obtain the desired current value is also present at the inverter output. The calculation of the modulation factor m from the output voltage allows for t_d to be omitted as a source of error.

Conventional PWM will switch at the maximum number of possible commutation points in time, thus causing a maximum of switching losses. Other control methods, such as vector control, omit selected switching operations, thus showing lower switching losses than calculated using the formulae below. The linearisation of the IGBT output characteristic using an equivalent straight line results in the following expression for the temporal correlation of the saturation voltage v_{CEsat}:

$$v_{CEsat}(t) = V_{CE0} + r_{CE} \cdot i_C(t) = V_{CE0} + r_{CE} \cdot \hat{I}_1 \sin \omega t$$

Considering the sinusoidal dependency of duty cycles versus time, the on-state power dissipation of the IGBT may be calculated according to

$$P_{cond(T)} = \left(\frac{1}{2\pi} + \frac{m \cdot \cos(\varphi)}{8} \right) \cdot V_{CE0}(T_j) \cdot \hat{I}_1 + \left(\frac{1}{8} + \frac{m \cdot \cos(\varphi)}{3\pi} \right) \cdot r_{CE}(T_j) \cdot \hat{I}_1^2$$

Provided that the energy dissipation during switching is linearly dependent on the collector current, the total switching loss of an IGBT may be calculated with

$$P_{sw(T)} = f_{sw} \cdot E_{on+off} \cdot \frac{\sqrt{2}}{\pi} \cdot \frac{I_{out}}{I_{ref}} \cdot \left(\frac{V_{cc}}{V_{ref}}\right)^{K_V} \cdot \left(1 + TC_{Esw} \cdot (T_j - T_{ref})\right)$$

where

$\hat{I}_1$:	Amplitude of the inverter output current =1.41×I_{out}
$V_{ce0}(T_j)$:	Temperature-dependent threshold voltage of the on-state characteristic
$r_{ce}(T_j)$:	Temperature-dependent bulk resistance of the on-state characteristic
I_{ref}, V_{ref}, T_{ref}:	Reference values of the switching loss measurements taken from the datasheet
K_v:	Exponents for the voltage dependency of switching losses ~1.3...1.4
TC_{Esw}:	Temperature coefficients of the switching losses ~ 0.003 1/K.

This is actually based on the assumption that the IGBT switching losses generated during one sine half-wave of the current are approximately identical to the switching losses generated if an equivalent direct current is applied, which would correspond to the average value of the sine half-wave.

Accordingly, the following applies to the diode:

$$v_F(t) = V_{F0} + r_F \cdot i_F(t) = V_{F0} + r_F \cdot \hat{i}_1 \sin \omega t$$

Considering the sinusoidal dependency of duty cycles versus time, the on-state power dissipation of diode D2 may be calculated according to

$$P_{cond(D)} = \left(\frac{1}{2\pi} - \frac{m \cdot \cos(\varphi)}{8}\right) \cdot V_{F0}(T_j) \cdot \hat{I}_1 + \left(\frac{1}{8} - \frac{m \cdot \cos(\varphi)}{3\pi}\right) \cdot r_F(T_j) \cdot \hat{I}_1^{\,2}$$

Diode switching losses are approximated as follows:

$$P_{sw(D)} = f_{sw} \cdot E_{rr} \cdot \left(\frac{\sqrt{2}}{\pi} \cdot \frac{I_1}{I_{ref}}\right)^{K_i} \cdot \left(\frac{V_{cc}}{V_{ref}}\right)^{K_V} \cdot \left(1 + TC_{Err}(T_j - T_{ref})\right)$$

$V_{F0}(T_j)$:	Temperature-dependent threshold voltage of the on-state characteristic
$r_F(T_j)$:	Temperature-dependent bulk resistance of the on-state characteristic
Kv:	Exponents for the voltage dependency of switching losses ~0.6
K_i:	Exponents for the current dependency of switching losses ~0.6
TC_{Err}:	Temperature coefficients of the switching losses ~ 0.006 1/K.

The formula for diode switching losses expresses an approximate only, since switching losses are not a linear function of the current ($K_i \neq 1$). For this reason, the diode switching losses during a sine half-wave are no longer identical to the switching losses of an equivalent direct current which corresponds to the average of the sine half-wave. The results rendered by the simplified calculation above are sufficient for estimating the expected power dissipation during converter operation mode in practice. The decisive advantage that is offered to the user is that all necessary parameters can be taken directly from the module datasheets.

5.2.2 Junction temperature calculation

5.2.2.1 Thermal equivalent circuit diagrams

The terms 'thermal resistance' and 'thermal impedance' have already been explained in chapter 2.5.2.2; this section deals with the types of modelling only. The calculation of junction temperatures is based on simplified thermal equivalent circuit diagrams (Figure 5.2.5) in which three-dimensional structures are mapped to one-dimensional models. This will inevitably result in errors, since thermal connections between different components inside one housing or on one heatsink are dependent on time as well as on the electric operating point of the components (e.g. distribution of losses between diode and IGBT). More complex models with a matrix composed of coupling elements are impractical and difficult to parameterise [37]. If such effects have to be considered more closely, FEM simulations are preferred to the analytical approaches presented here.

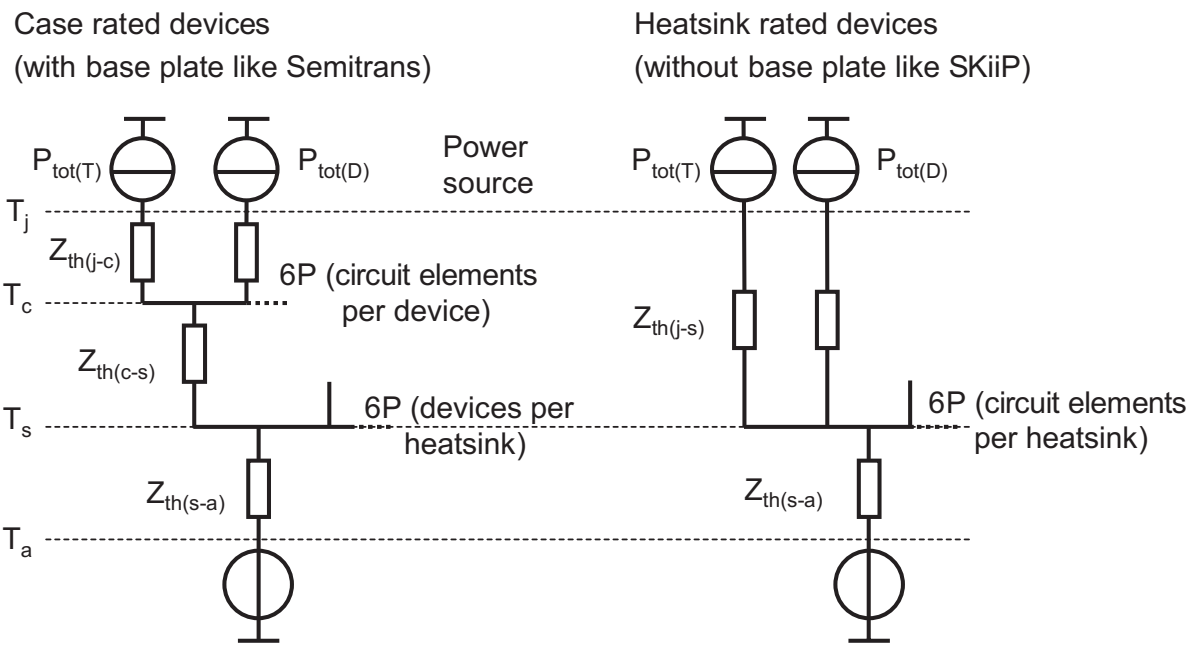


Figure 5.2.5 Simplified thermal equivalent circuit diagram of IGBT and freewheeling diode in a power module: for module with copper base plate (l); for module without base plate (r).

To obtain thermal equivalent circuit diagrams, electrical analogies to thermal parameters are used. The sources of power dissipation $P_{tot(T/D)}$ correspond to current sources, constant temperature levels are represented by voltage sources and RC elements are used to represent the thermal impedances $Z_{th(x-y)}$. In power modules with base plate, the transistor and inverse diode are soldered onto a common copper substrate, thus being thermally coupled. For the purpose of simplification, we may assume a common case temperature. The energy losses of all internal components in the module must be dissipated through the thermal impedance $Z_{th(c-s)}$ (Figure 5.2.5, left). IGBT losses will heat the base plate and thus the diode, too, even if the diode itself does not produce any losses. Several modules on one heatsink will all contribute to heat build-up, meaning that we may also assume a uniform heatsink temperature in this case.

Modules without base plate only demonstrate low thermal coupling in the module, which only exists at all if there are very small clearances between the heat sources. For the purpose of simplification, we may assume a common heatsink temperature (Figure 5.2.5, right). Component losses are directly dissipated to the heatsink, meaning that, together, all of the components heat up the heatsink.

Two equivalent circuit diagrams are quite common when mapping thermal impedance: the ladder-type "physical" equivalent circuit diagram (Figure 5.2.7, left, "Cauer network") and the chain-type "mathematical" equivalent circuit diagram (Figure 5.2.7, right, "Foster network"). At first glance, both types are equally useful. If a step-function response in a black box were "measured", it wouldn't be possible to determine which of the equivalent circuit diagrams was used (Figure 5.2.6).

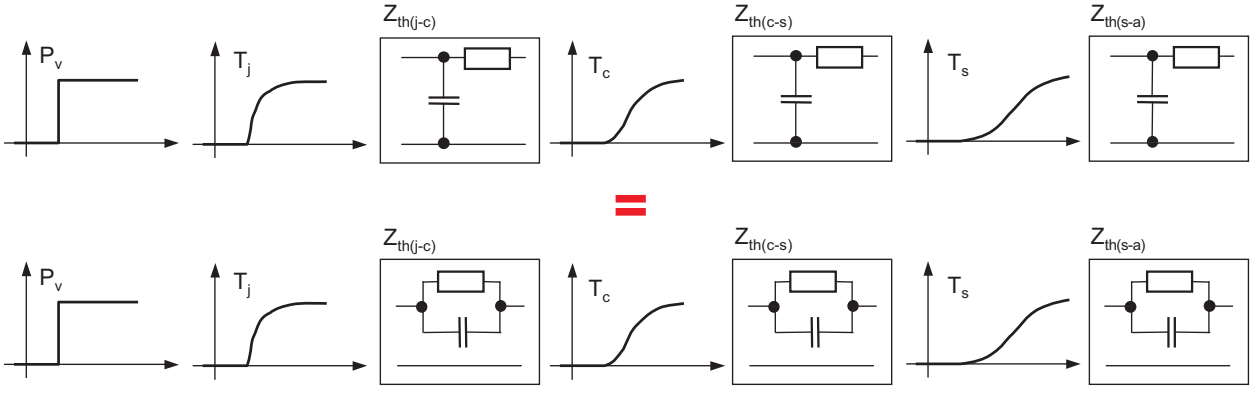


Figure 5.2.6 Mapping thermal impedance with the aid of equivalent circuit diagrams

The smallest error is produced in subsequent calculations if the entire system is measured as a closed system. The time-dependent temperature differences of T_j, T_c, T_s and T_a can be used to determine the blocks for thermal impedances $Z_{th(j-c)}$, $Z_{th(c-s)}$ and $Z_{th(s-a)}$, which are represented as four poles. To obtain a ladder-type equivalent circuit diagram, the geometrical dimensions and material properties are employed. For each layer in the structure at least one "ring" is necessary. Subsequent adjustments are often necessary in order to adapt the calculated functions to the measured results. In this way, the physical relation gets somewhat lost. To obtain the chain-type equivalent circuit diagram, the factors and time constants for the exponential function are determined by means of formula manipulation.

$$Z_{th(x-y)} = R_{th1} \cdot \left(1 - e^{\frac{-t}{\tau_{th1}}}\right) + R_{th2} \cdot \left(1 - e^{\frac{-t}{\tau_{th2}}}\right) + \cdots = \sum_{\nu=1}^{n} R_{th\nu} \cdot \left(1 - e^{\frac{-t}{\tau_{th\nu}}}\right)$$

2 to 3 exponential terms are often sufficient for mapping. The main advantage of the exponential function is that it can be easily used for subsequent temperature calculation. SEMIKRON specifies the power module parameters for $Z_{th(j-c)}\backslash Z_{th(j-s)}$ in the form of 2 to 6 RC elements in the data book for computer-aided simulations of the time curve of the junction temperature.

It is possible for both equivalent circuits to line up the sub-blocks determined in the overall system and determine the intermediate temperatures T_c, T_s. Where things go wrong, however, is when one block from the chain of thermal impedances is to be replaced by another. Heat spreading produces feedback to the preceding blocks. For example, this is the case if parameterisation has been done on a very good water cooler and in the real application the component is mounted on a poor air cooler. Nevertheless, to simplify matters, often only $Z_{th(s-a)}$ is replaced.

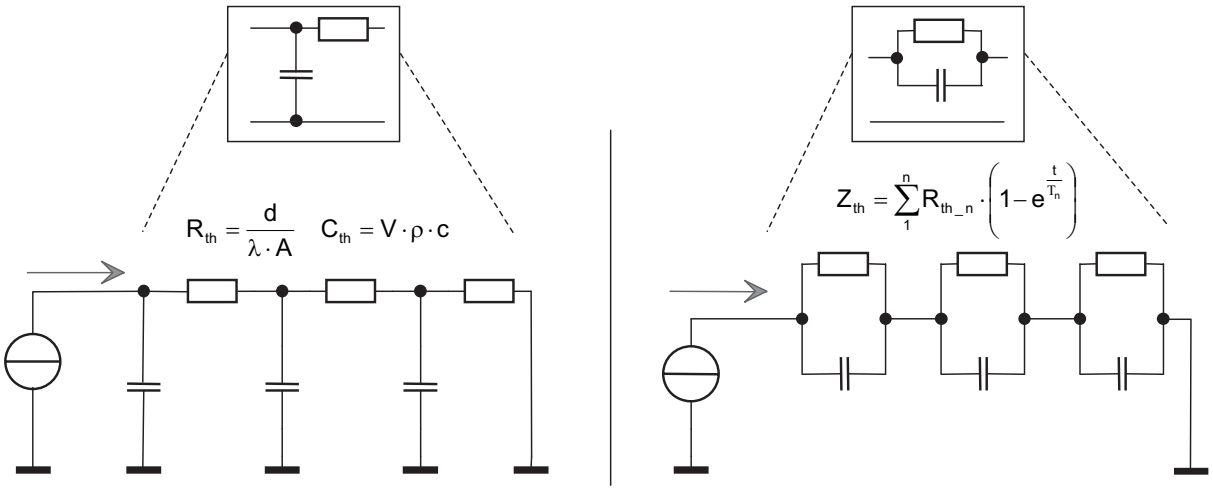


Figure 5.2.7 Mapping of the Z_{th} four-pole blocks by means of thermal equivalent circuit diagrams; left: conductor-type "physical" equivalent circuit diagram (Cauer network); right: chain-type "mathematical" equivalent circuit diagram (Foster network)

Notes on the use of the Foster network:
- The intermediate points within a block (Figure 5.2.7, right) do not represent system temperatures.
- The R and C elements cannot be assigned to any physical components.
- The sequence of the RC elements within a block can be interchanged.
- They cannot be connected in series with a resistance.

It is often only the average junction temperatures and their ripples that are decisive for the thermal layout of converters. Examples of calculations for typical loads are shown in the subsequent chapters.

5.2.2.2 Junction temperature during stationary operation (mean-value analysis)

After losses have been calculated, temperatures during stationary operation can be calculated with the aid of the thermal resistances R_{th} (= final value of the Z_{th} curves). Temperature calculation is performed starting with the ambient temperature from the outside to the inside (cf. example Figure 5.2.8).

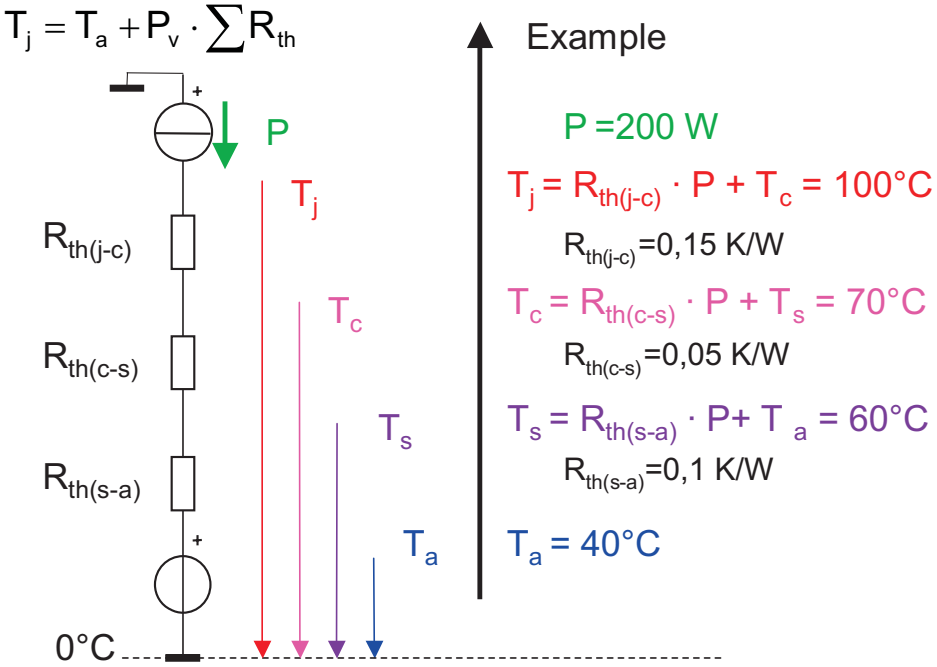


Figure 5.2.8 Temperature calculation under stationary conditions

If there is more than one source of power loss on a heatsink, the individual losses of all n_1 components are added up (e.g. 6 IGBT and 6 freewheeling diodes of a 3-phase inverter); this total loss is used to calculate the heatsink temperature.

$$T_s = n_1 \cdot \left(P_{tot(T)} + P_{tot(D)}\right) \cdot R_{th(s-a)} + T_a$$

Modules with base plate show good thermal coupling between their components, the thermal resistance $R_{th(c-s)}$ is specified for the entire module, which is why all sources of power loss n_2 in the module are added up to calculate the case temperature (e.g. 2 IGBT and 2 freewheeling diodes in a half-bridge module):

$$T_c = n_2 \cdot \left(P_{tot(T)} + P_{tot(D)}\right) \cdot R_{th(c-s)} + T_s$$

In some examples, this modelling will result in excessive temperatures if just one IGBT and its spatially divided freewheeling diode is used in a half-bridge module, or if IGBT and parallel inverse diode produce time-shifted losses in inverter mode. If $R_{th(c-s)}$ is only specified for a single component (e.g. the IGBT), the thermal coupling of the copper base plate with the inverse diode is neglected. In this case, modelling in combination with simultaneous losses in IGBT and diode will produce an error with temperatures that are too low.

The junction temperature is finally calculated from the losses of the single component and its thermal resistance to the case for modules with base plate, or to the heatsink for modules without base plate. For IGBT this is, for example,

$$T_{j(T)} = P_{tot(T)} \cdot R_{th(j-c)} + T_c$$

or

$$T_{j(T)} = P_{tot(T)} \cdot R_{th(j-s)} + T_s$$

All semiconductor losses are temperature-dependent, meaning that chip temperature and losses are coupled. In the simplest case, losses are calculated at the maximum junction temperature. This will ensure that you are on the safe side, since most losses increase in line with temperature. In an improved procedure, losses are determined iteratively at the calculated junction temperature. For this loop that can easily be programmed, the starting value is the power dissipation at ambient temperature (Figure 5.2.9). This value allows for an initial approximation of the junction temperature. At this temperature, a new, more precise loss value is produced. After 3 to 4 iterative loops, the final value will have been reached in most cases.

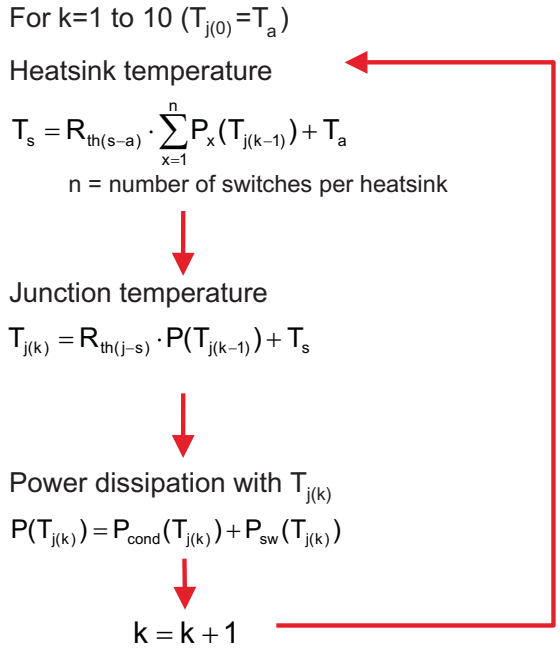


Figure 5.2.9 Loop used to calculate temperature-dependent semiconductor losses for a module without base plate

5.2.2.3 Junction temperature during short-time operation

Higher current loads are permitted during short-time operation of the power semiconductors than specified in the datasheets for continuous operation. What must be ensured here, however, is that the maximum junction temperature that develops under the defined conditions does not exceed the limit value for $T_{j(max)}$. T_j is calculated with the aid of the thermal impedance Z_{th}. For pulses in the millisecond range, it is sufficient for $Z_{th(j-c)}$ to be considered at a constant case temperature T_c. In the range up to 1 s, it is possible to work with the module impedance $Z_{th(j-s)} = Z_{th(j-c)} + Z_{th(c-s)}$ and constant heatsink temperature. In longer pulse sequences, the total impedance $Z_{th(j-a)} = Z_{th(j-s)} + Z_{th(s-a)}$ should be used.

Single pulse

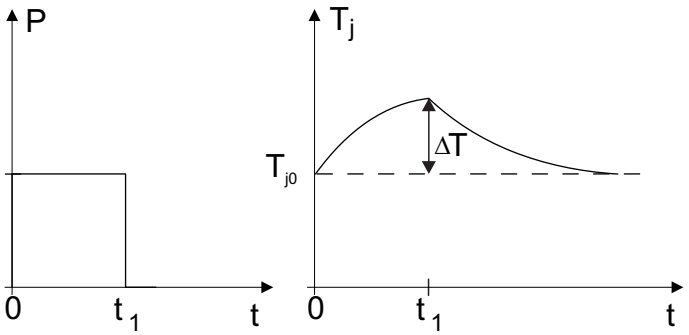


Figure 5.2.10 Time curve of power dissipation and junction temperature in the event of a single power dissipation pulse

The junction temperature change at the moment t_1, following a single power dissipation pulse, is calculated using the following formula:

$$\Delta T_j = P \cdot \sum_{\nu=1}^{n} R_{th\nu} \cdot \left(1 - e^{\frac{-t_1}{\tau_{th\nu}}} \right)$$

The following applies to the junction temperature curve during the cooling phase:

$$\Delta T_j \left(t > t_1 \right) = P \cdot \sum_{\nu=1}^{n} R_{th\nu} \cdot \left(1 - e^{\frac{-t}{\tau_{th\nu}}} \right) - P \cdot \sum_{\nu=1}^{n} R_{th\nu} \cdot \left(1 - e^{\frac{-(t-t_1)}{\tau_{th\nu}}} \right)$$

The formulae assume a fixed reference temperature.

One-time sequence of m power dissipation pulses

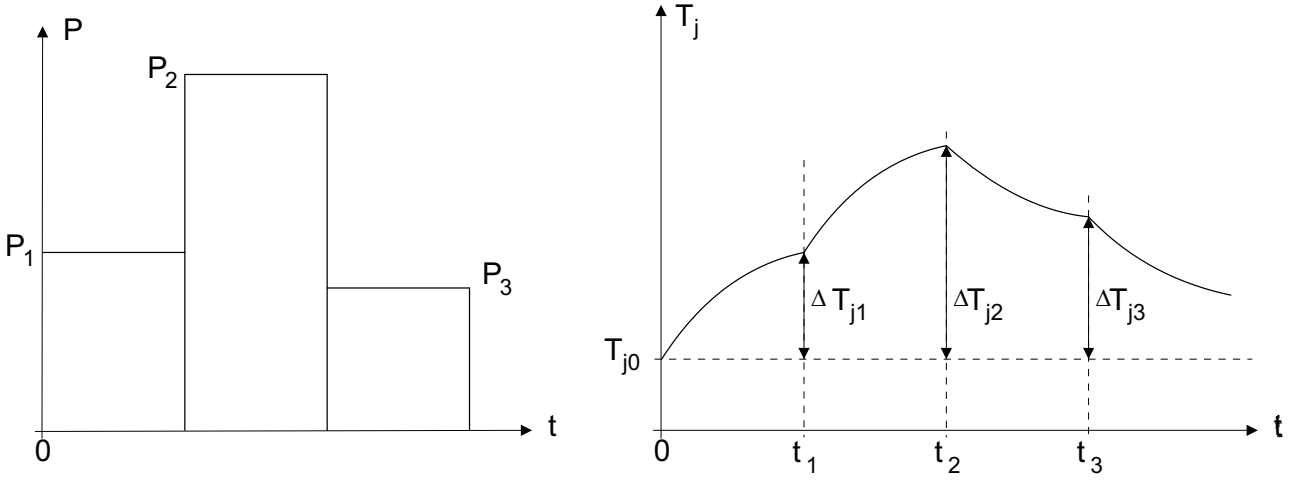


Figure 5.2.11 Time curve of power dissipation and junction temperature in the event of a one-off sequence of m power dissipation pulses

The junction temperature change at the moment t_1 is to be calculated in the same way as for the single pulse. For a junction temperature change at the moment t_2, the following applies:

$$\Delta T_j(t_2) = P_1 \cdot \sum_{\nu=1}^{n} R_{th\nu} \cdot \left(1 - e^{\frac{-t_2}{\tau_{th\nu}}} \right) + (P_2 - P_1) \cdot \sum_{\nu=1}^{n} R_{th\nu} \cdot \left(1 - e^{\frac{-(t_2 - t_1)}{\tau_{th\nu}}} \right)$$

Junction temperature change at the moment t_m:

$$\Delta T_j(t_m) = \sum_{\mu=1}^{m} (P_\mu - P_{\mu-1}) \cdot \sum_{\nu=1}^{n} R_{th\nu} \cdot \left(1 - e^{\frac{-(t_m - t_{\mu-1})}{\tau_{th\nu}}} \right)$$

These formulae also assume a fixed reference temperature. This formula enables the discretisation of any time curve, meaning a time-dependent calculation of the temperature curve of complex load cycles can be programmed.

Junction temperature at constant pulse sequence

In order to calculate the mean and maximum junction temperature for periodically recurring power dissipation loads, the $Z_{th(j-c)}$ curve of transistor and diode in periodic pulse operation can be used as specified in the datasheets.

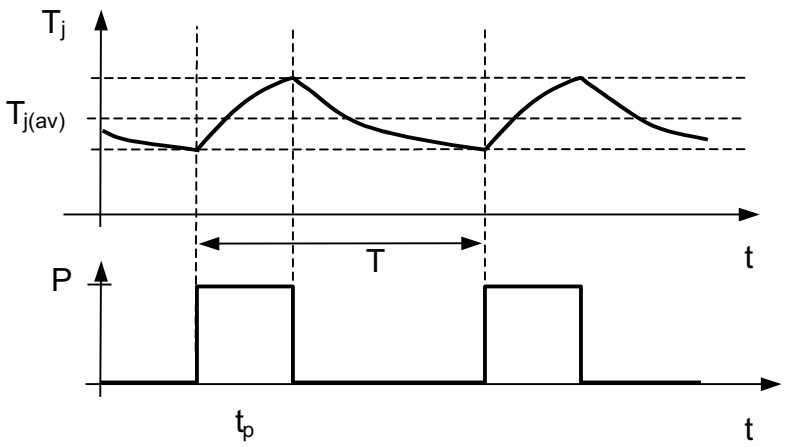


Figure 5.2.12 Temperature curve for periodic pulse load

The average junction temperature $T_{j(av)}$ results from the product of stationary heat resistance R_{th} and the average total loss P_{av}. This value is obtained by averaging the loss energies per pulse over the entire length of a period T. The maximum junction temperature at the end of the loss pulse $P(t_p)$ results from

$$\Delta T_j(t_p) = P \cdot \sum_{\nu=1}^{n} R_{th\nu} \cdot \left(\frac{1 - e^{\frac{-t_p}{\tau_{th\nu}}}}{1 - e^{\frac{-T}{\tau_{th\nu}}}} \right)$$

For pulse durations in the millisecond range, significant temperature swings occur. After some 100 ms, a strong stationary temperature difference will already have developed between chip and case.

5.2.2.4 Junction temperature at fundamental frequency

The calculation of the junction temperature determined by the fundamental frequency of the converter output current is only efficient if performed using computer-aided methods. Both thermal system and electrical system per pulse duration have to be calculated in detail in order to integrate the IGBT and diode junction temperature over a sine half-wave. The thermal model essentially corresponds to Figure 5.2.5 simulating the thermal impedances by means of exponential functions.

Switching losses per pulse may be calculated based on stored characteristics, if the current converter parameters such as DC link voltage and instantaneous load current are given. The instantaneous junction temperature is entered into the calculation via the temperature coefficients. Figure 5.2.13 shows the time characteristic of the power dissipation and the average power dissipation in an IGBT, as well as the resulting junction temperature characteristics for different fundamental output frequencies as the result of a simulation.

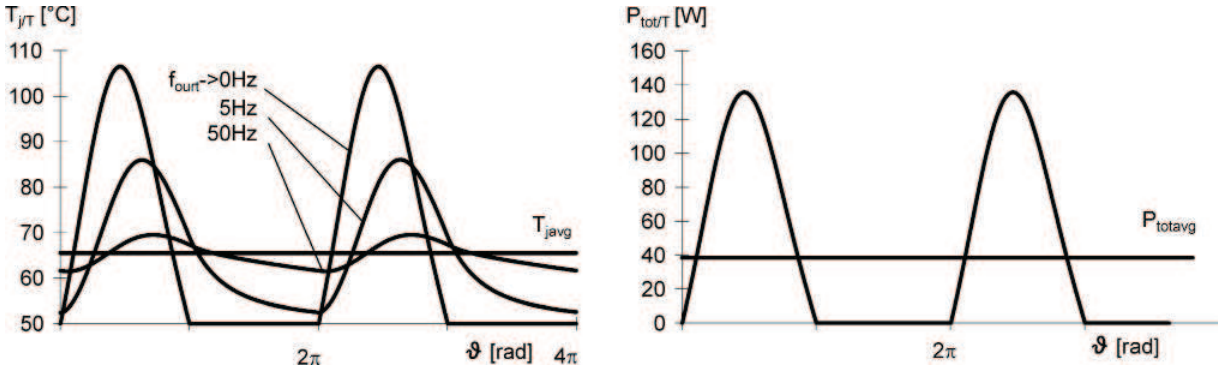


Figure 5.2.13 Simulated junction temperature and power dissipation characteristics of a 1200 V / 50 A-IGBT in inverter mode for different fundamental output frequencies; [37] v_d = 540 V; i_{1eff} = 25 A, f_s = 8 kHz; cos φ = 0.8; m = 0.8; T_h = 50°C

In this example, the maximum junction temperature exceeds the average value by just about 4-5 K at a frequency of 50 Hz. For low frequencies the average junction temperature is no longer permitted to determine the thermal layout of the system because of its far higher maximum value. Therefore, the minimum frequency at rated power output is a critical parameter for inverters besides overcurrent. When the frequency decreases, the maximum temperature will rise despite constant mean losses. An explanation for this is the fact that the thermal time constants of power semiconductors are below one second and thus within the range of normal inverter output frequencies. When frequencies are high, the thermal capacitances of the semiconductor (case) still average the temperature characteristic. When frequencies are low (<2...5 Hz), the junction temperature follows the power dissipation. This results in high temperature fluctuations around the mean temperature. Consequently, the permissible output current RMS value for a defined power module will decrease at a given heatsink temperature and switching frequency.

A particularly critical case with regards to the thermal stress of power modules is the voltage- and frequency-controlled starting process of a three-phase motor drive supplied by an inverter. Figure 5.3.14 shows a suitable simulation example.

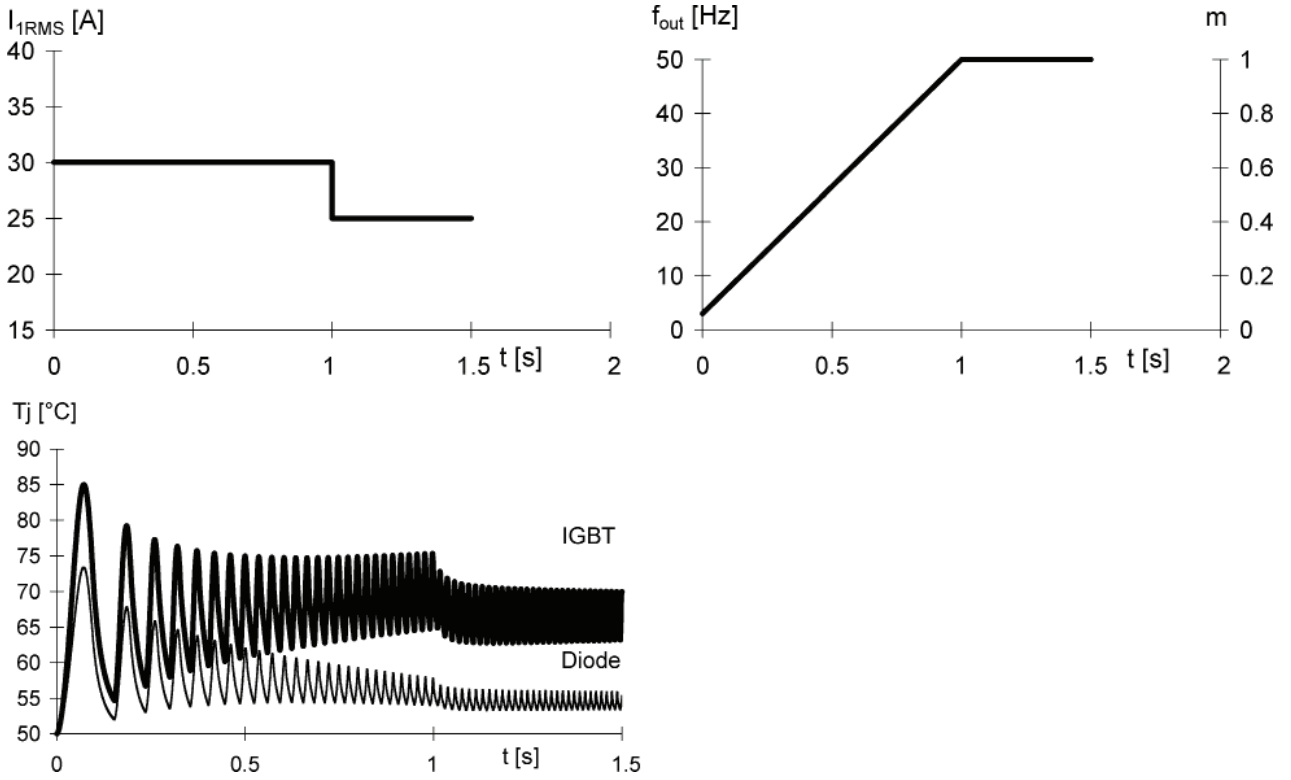


Figure 5.2.14 Starting process of a three-phase motor drive (parameters as in Figure 5.2.13), [37]

If you do not use a circuit simulation but rather the formulae given in chapter 55.2.1.2, inverter operation at an output frequency of f_{out} = 0 Hz is a limiting case. If mean values of a period are used for calculations, the period will be infinite at f = 0 Hz. "Infinite" applies if the dwell time in this condition is far greater than the thermal time constants of the system. Besides the marginality of the formula definition, it is extremely problematic to generally assume an even distribution of losses on the heatsink, whereas in this case it is only one of the 6 switches that produces the major part of the losses. Theoretically, one switch might switch a direct current at the very moment when the current and losses reach their maximum. It is therefore the better choice to calculate this operating condition with the aid of a chopper circuit (step-down converter).

Starting an electric motor from a standstill does not begin at 0 Hz in the mathematical sense of the formulae used in chapter 5.2.1.2. The first half-wave ends after a finite period of time, in the example given in Figure 5.2.15 this is no more than 200 ms, which – in purely mathematical terms for semiconductor losses – corresponds with a starting frequency of 2.5 Hz.

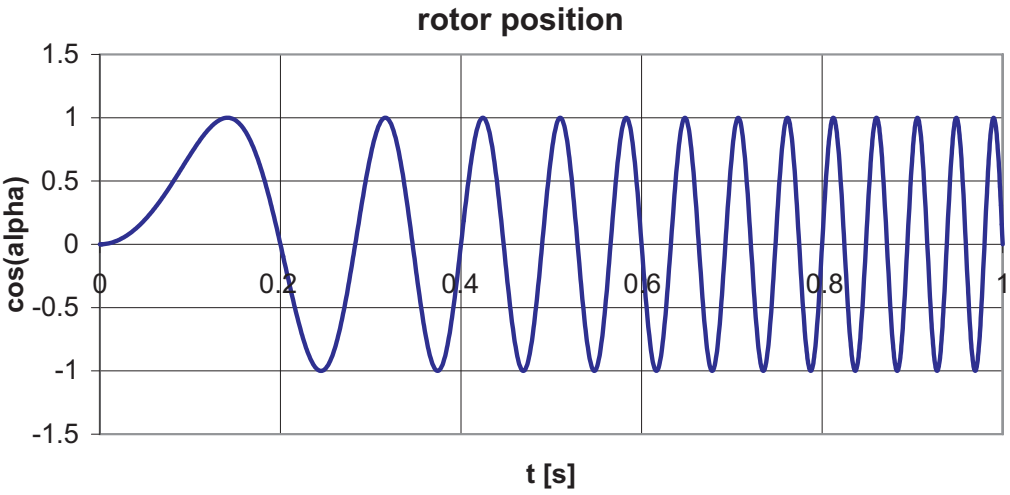


Figure 5.2.15 Rotor position at motor start

5.2.3 Calculation of power dissipation and temperature using SemiSel

General information on the areas of application and their potential is given in chapter 7. This book is based on SemiSel version 3.1.

5.2.3.1 Possible solution for temperature and power dissipation calculation

How much work does a tool such as this do to be able to produce results so fast? At first, the program converts the circuit parameters entered into values for the individual components. Components are characterised by simple correlations, e.g. an equation of the straight line for the on-state characteristic (V_0 – zero-point voltage + r_f – bulk resistance) or simple exponential interrelations for switching loss dependencies. SemiSel employs an analytical approach to calculate power dissipation. This approach is based on the solution for the integral of voltage and current present in a component. The equations presented in chapter 5.2.1 are used. These provide the mean losses for the component. With the aid of the thermal resistances defined for each reference point (j – junction, c – case, s – heatsink or a – ambient), the mean junction temperature T_j is calculated:

$$T_j = P_{(av)} \cdot R_{th(j-s)} + R_{th(s-a)} \cdot \sum_n P_n + T_a$$

Where P_n represents the individual component losses on a common heatsink. Most component parameters used for loss calculation are temperature-dependent, which is why the software determines the real losses iteratively by considering component self-heating.

Calculating losses and maximum temperatures under special load conditions is of particular interest. For most circuits, the most important overload parameter that must be defined is an overcurrent (referred to the rated current) for a certain period of time. Higher load simply results from increased power dissipation and consequently a higher junction temperature. The only thing that is different in the calculation as compared to rated conditions, is the fact that calculations are performed with a thermal impedance rather than thermal resistances.

$$T_j(t) = P_v(t) \cdot Z_{th(j-s)}(t) + Z_{th(s-a)}(t) \cdot \sum_n P_{v\_n}(t) + T_a$$

The program breaks down the overload pulse into time-discrete points and calculates the temperature characteristic up to the n-th point in a second iteration loop, always starting from t = 0. The result is time-dependent temperature characteristics for the component. As mentioned above, the minimum frequency is also a critical parameter for inverters besides overcurrent (chapter 5.2.2.4). Here, SemiSel converts the mean losses obtained into a sinusoidal half-wave and uses this source of power dissipation together with the thermal impedance to calculate the maximum T_j.

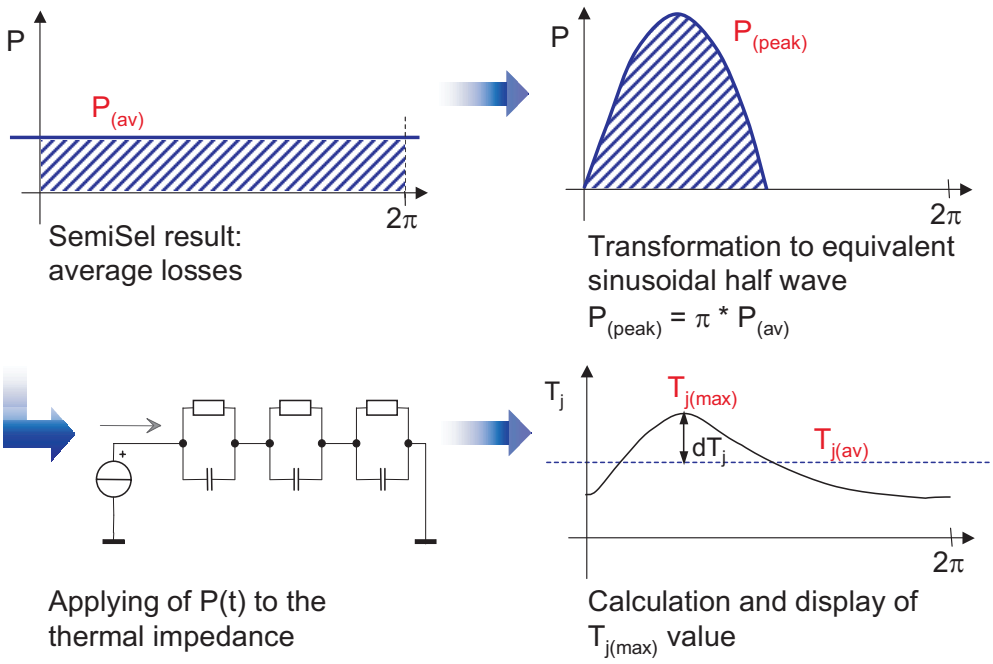


Figure 5.2.16 Calculation of the junction temperature fluctuation as a function of the inverter's output frequency using SemiSel

5.2.3.2 Circuit selection

The following description refers to the program element used most frequently: "Step by Step". In this part as well as in the "Device proposal" part, the first step is to select the circuit type. This loads the circuit-specific templates and formulas. For transistor components you can choose between DC/DC converters and inverter circuits (AC/DC).

5.2.3.3 Electrical operating conditions

Electrical parameters must be specified as the first part of the input values for the calculation. The user has to define - besides the rated conditions - the overload conditions relevant to component dimensioning. This may be an overload current for a limited period of time or, in the case of inverters, operation at a low output frequency. The selected component must be rated for these cases so as to provide a sufficient reserve to the maximum temperature $T_{j(max)}$.

circuit parameter			
input voltage	$V_{(d)}$	600	V
output voltage	V_{out}	400	V
cosinus phi	cos_{phi}	0.85	
output power	P_{out}	80	kW
output current	I_{out}	136	A
switching frequency	f_{sw}	8	kHz
output frequency	f_{out}	50	Hz
load and overload parameter			
factor		2	
duration		10	s
user defined load cycle		☑	
min. output frequency	$f_{min\ out}$	2	Hz
min. output voltage	$V_{min\ out}$	54	V

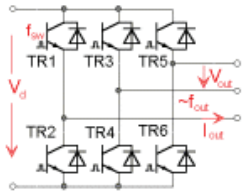
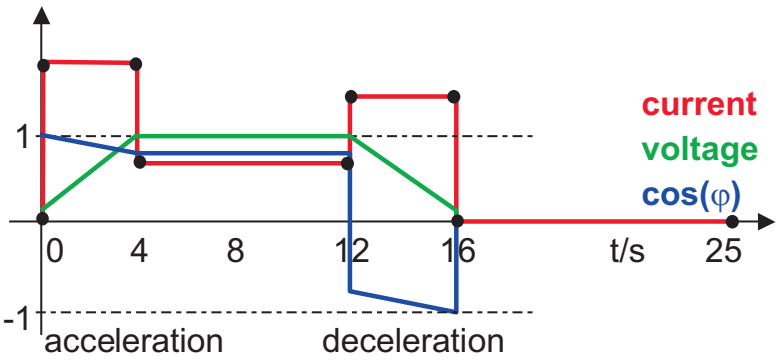


Figure 5.2.17 Entering the electrical ratings and overload conditions

Another aspect that limits service life is the load and temperature cycles. For these cases, SemiSel provides an option for entering and calculating typical load cycles. What is relevant for this kind

of load is the temperature difference between operation under full load and idling rather than the maximum temperature. This leads to ageing signs in the power module (cf. chapter 2.7) and must therefore be included in the lifetime evaluation of the converter. Figure 5.2.18 shows an example of an operating cycle of a drive incl. the 4 operating states: start, constant speed, braking, standstill. The load cycle values are entered in a table with reference points. Between these points, the program performs a linear interpolation. The calculations of temperature and power dissipation are done in a similar way as for the overload current. During the acceleration and braking phase, an overcurrent flows and the switching frequency was reduced. A particularity of braking is that the direction of energy flow is changed. The phase angle cos(φ) becomes negative – the inverter works as a rectifier and feeds back energy.



t [s]	I/Iout	V/ Vout	cos (φ)	fout [Hz]	fsw [kHz]
0	0	0	0	0	6
0.1	2	0,1	1	5	4
4	2	1	0.85	50	4
4.1	0.7	1	0.85	50	6
12	0.7	1	0.85	50	6
12.1	1.5	1	-0.85	50	4
16	1.5	0.1	-1	5	4
16.1	0	0	0	5	6
25	0	0	0	0	6

Figure 5.2.18 Definition of a load cycle in SemiSel

5.2.3.4 Component selection

The second set of input quantities which is required is the component parameters. These are loaded from a database by selecting the component name (Figure 5.2.19). Here, users have to have an idea of which product they could possibly use. This refers to the case type as well as the various chip technologies. As an initial starting point that does not factor in overload, the user can request a product suggestion in the "Device proposal" program section.

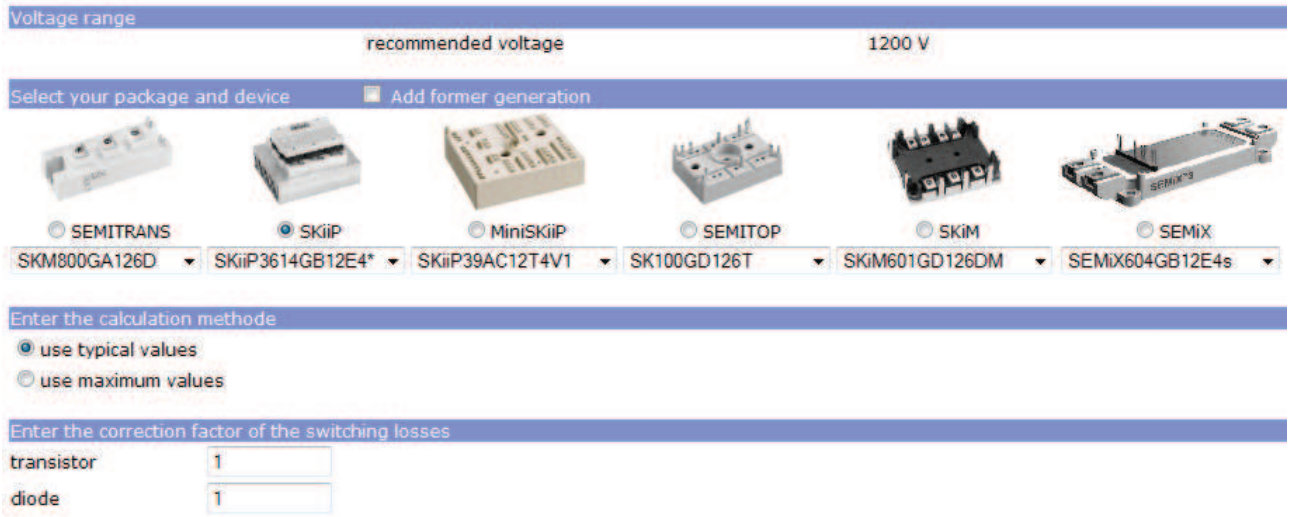


Figure 5.2.19 Component selection

To influence component parameters, users can choose between typical and maximum on-state parameters. Apart from that, switching losses can be modified with the aid of a correction factor. This may, for example, be necessary when the driver parameters deviate from the datasheet ratings, or when "soft switching" is performed. The correction factor is established by setting the switching losses at the nominal operating point in relation to the switching losses in the application (Figure 5.2.20). For modified driver parameters, the characteristic $E_{sw} = f(R_G)$ from the datasheet is to be used.

$$K_{E_{sw}} = \frac{E_{on+off}(R_g)}{E_{on+off}(R_{g\_ref})}$$

Data sheet value at $R_{g\_ref} = 7\ \Omega$:

$E_{on+off} = 33$ mJ

$E_{rr} = 8$ mJ

Switching losses at $R_g = 20\ \Omega$:

$E_{on+off} = 57$ mJ

$E_{rr} = 5{,}5$ mJ

Correction factor:

transistor $K_{E_{sw}\_IGBT} = 1{,}72$

diode $K_{E_{sw}\_D} = 0{,}69$

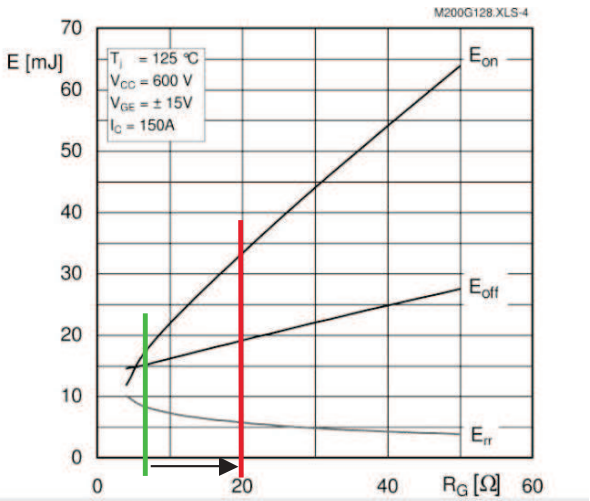


Fig. 4 Typ. turn-on /-off energy = f (R_G)

Figure 5.2.20 Establishing the correction factor for switching losses for modified driver parameters

5.2.3.5 Thermal operating conditions

The last parameter to be specified is the cooling conditions. In the simplest case, losses and chip temperature can be calculated at a constant heatsink temperature. Afterwards, the required thermal heatsink resistance may be calculated from the maximum ambient temperature, defined heatsink temperature and calculated total losses.

$$R_{th(s-a)} = \frac{T_s - T_a}{P_{tot}}$$

Should a heatsink have already been specified, the ambient temperature has to be entered. Here, ambient temperature is to be understood in the sense of the coolant temperature (water, air). This needn't necessarily correspond to the temperature inside the control cabinet. Users can define a thermal impedance as a function of τ_ν and $R_{th\nu}$ with up to 6 elements as heatsink model. Alternatively, users may choose from selected Semikron heatsinks featuring natural convection, forced air cooling or water cooling. These heatsinks are assigned to the product groups (disk cells, modules with base plate, SKiiP...), but there is no verification of whether the case dimensions and number of modules reasonably match the heatsink dimensions.

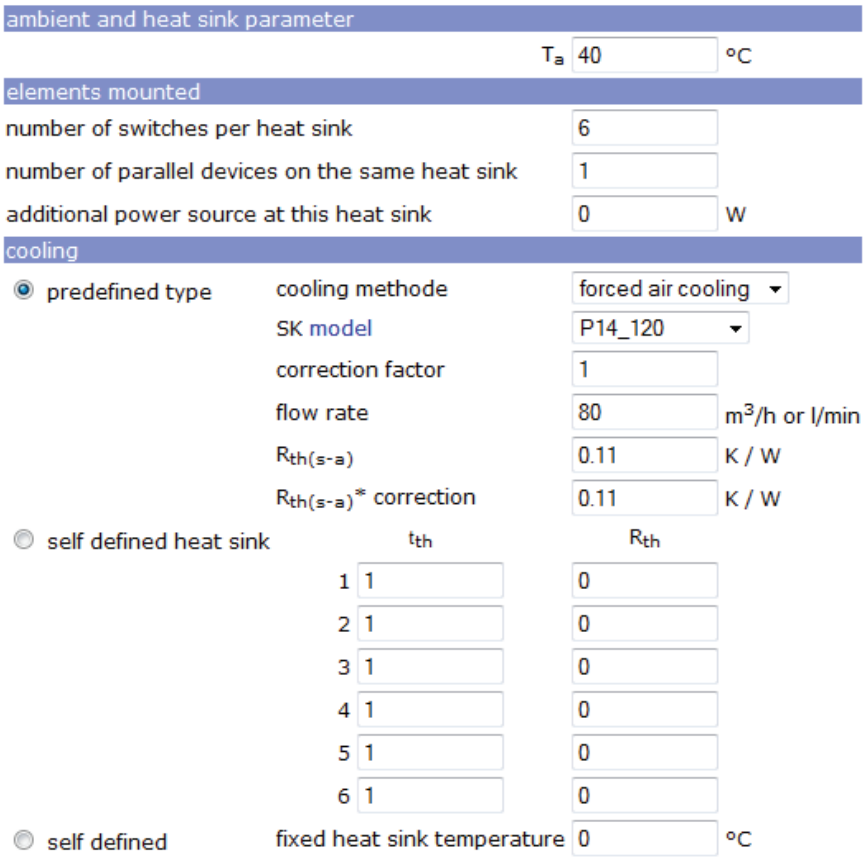


Figure 5.2.21 Defining cooling conditions in SemiSel

Specifying cooling conditions requires engineering expertise which the software cannot provide. The influence of the component size, the number of components, and the distribution of heat sources to the thermal resistance of the heatsink $R_{th(s-a)}$ have to be considered. Heatsink thermal resistances are often given by the manufacturers to indicate evenly spread heat spread. In case of sporadic impression R_{th} is increased. Some parameters are given in chapter 55.3 as a guideline; for some SEMIKRON heatsinks, dependencies are specified in terms of component size and quantity. To be able to influence $R_{th(s-a)}$, the user is offered a correction factor. This factor is multiplied by the database value for the selected heatsink to enable adjustment to the above-mentioned influences. The correction factor can also be used to adjust R_{th} of an actual heatsink to the value for a heatsink provided in the program. Their size and weight should, however, be similar. The new value is displayed as $R_{th(s-a)*}$. $R_{th(s-a)}$ is also dependent on the coolant volumetric flow rate. This may be varied for the pre-defined heatsinks within certain limits.

When calculating T_s it is important that the number of heat sources n is specified. These are universally defined as switches. A three-phase IGBT inverter consists of 6 switches; 1 IGBT and the relevant inverse diode make up one switch. A switch may also consist of a parallel connection of several chosen components. This must also be defined. The upper image in Figure 5.2.22 shows a three-phase inverter comprising 3 half-bridge modules (GB). 6 switches are mounted on the heatsink; there is no parallel connection. In the other two examples, there is a parallel connection. The example in the middle shows one phase with 2 switches per heatsink, while in the example at the bottom, all of the 6 switches reside on one heatsink once again, but every switch consists of 2 modules connected in parallel. The total power dissipation on the heatsink adds up to

$$P_{tot} = n_s \cdot n_p \cdot \left(P_{tot(T)} + P_{tot(D)}\right)$$

n_s = number of switches on the heatsink
n_p = number of components connected in parallel in the switch

In a parallel connection, the inverter current is ideally divided between the number of parallel components.

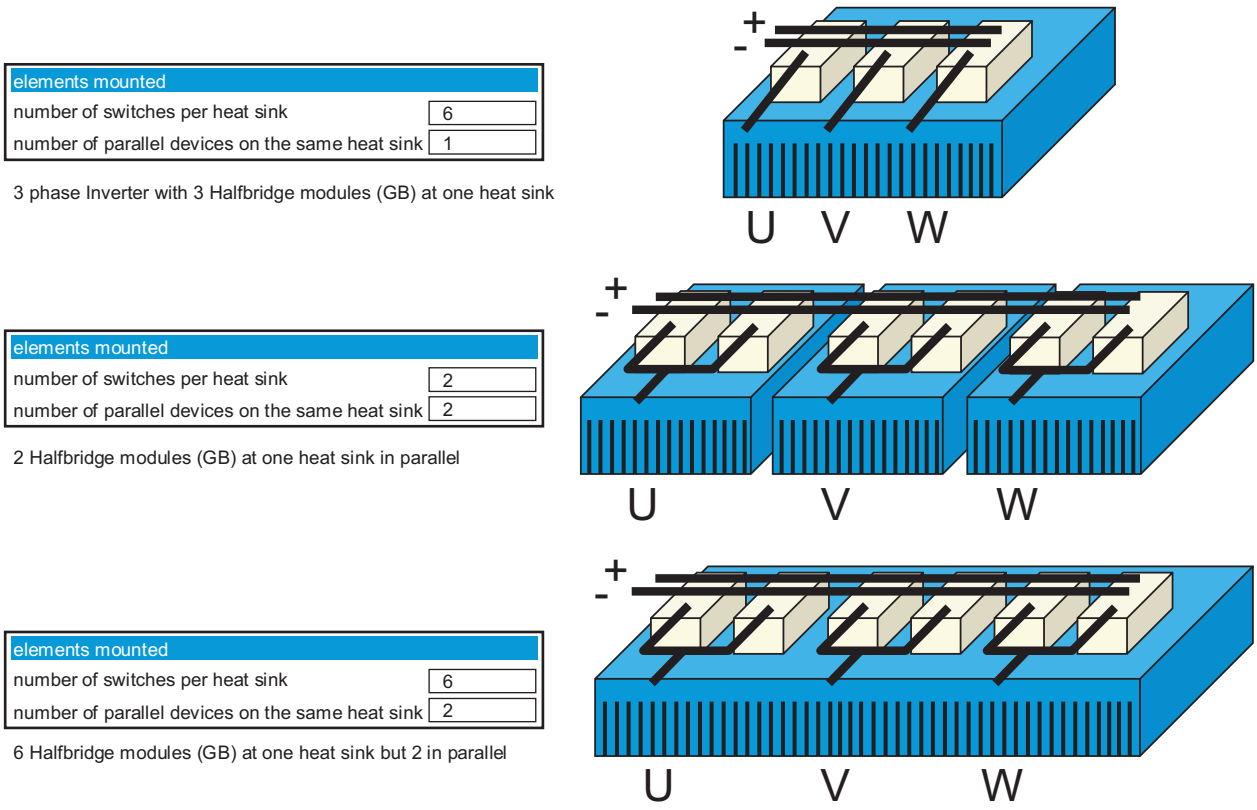


Figure 5.2.22 Examples of the definition of switches and parallel components per heatsink

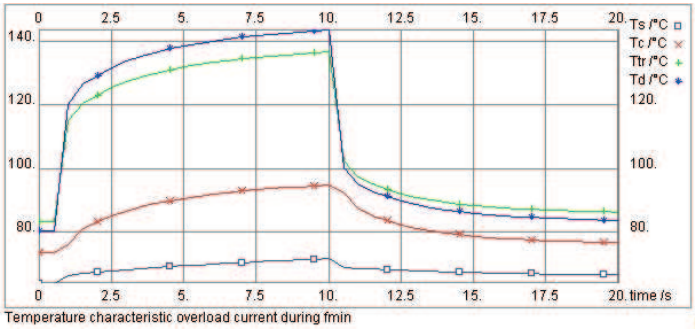
The last option for input prior to the calculation of results is to impress additional losses into the heatsink. This is necessary, for instance, if input rectifier and inverter heat up the heat sink at the same time. These rectifier losses can be established in a second calculation and can then also be factored in as an additional source of power dissipation.

5.2.3.6 Results

The results page first presents a summary of all parameters entered for the electrical operating point and the cooling condition, as well as a list of the semiconductor parameters used for the calculation. This is followed by a list of the switching and conducting losses of IGBT and diode under rated conditions, for the overload current and for operation at minimum frequency. The chip temperatures $T_{j(T)}$ and $T_{j(D)}$, as well as the case and heatsink temperatures T_c and T_s are given as averages for the rated current and the overload current and as peak values for the operating point "minimum frequency + overload". All information on losses and temperatures is presented in tabular form and for the operating point with the highest temperature, the temperature characteristic of $T_{j(T)}$, $T_{j(D)}$, T_c and T_s is presented as a graph (Figure 5.2.23). Finally, the temperatures are evaluated. We recommend a safety margin of 25°C below $T_{j(max)}$ for IGBT modules.

Calculated losses and temperatures with rated current, at overload and at $f_{min\ out}$:

	Rated Current	Overload	f_{min} and Overload
$P_{cond\ tr}$	43 W	117 W	73 W
$P_{sw\ tr}$	52 W	118 W	118 W
P_{tr}	95 W	234 W	191 W
$P_{cond\ d}$	8.32 W	19 W	66 W
$P_{sw\ d}$	26 W	51 W	55 W
P_d	34 W	69 W	122 W
P_{tot}	774 W	1824 W	1876 W
	Average Values	Average Values	Maximum Values
T_s	64 °C	72 °C	72 °C
T_c	74 °C	94 °C	95 °C
T_{tr}	81 °C	111 °C	137 °C
T_d	79 °C	104 °C	144 °C



Temperature characteristic overload current during fmin

Evaluation:

This configuration works fine.

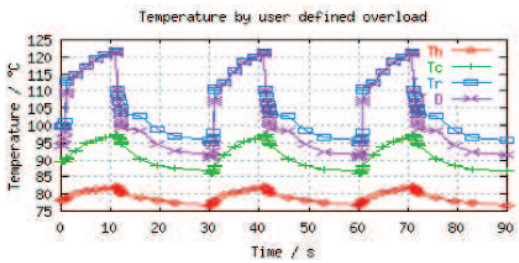
Figure 5.2.23 SemiSel representation of results for losses and temperatures

If necessary the results gained from overload conditions enable the definition of certain constraints for the purpose of cost optimisation in the design process (e.g. maximum ambient temperature, reduced bias, or reduced overload). This will ensure that the given requirements can be met with the desired assembly. The user-friendly, high-performance program allows for parameters to be "played around with" in order to reach the ideal compromise between design goals. The user can return to any of the input pages and then repeat his calculation(s) using the modified parameters. If a detailed load cycle has been defined, results are provided both as numerical values for minimum and maximum losses and temperatures, and graphs of the time functions of all parameters (Figure 5.2.24). An extensive help function offers users assistance where needed.

Calculated losses and temperatures with user defined load cycle:

Temperatures			
$T_{h\ max}$	82 °C	$T_{h\ min}$	77 °C
$T_{c\ max}$	97 °C	$T_{c\ min}$	86 °C
$T_{tr\ max}$	122 °C	$T_{tr\ min}$	95 °C
$T_{d\ max}$	122 °C	$T_{d\ min}$	91 °C

Power Losses			
$P_{tr\ av}$	113 W	$P_{d\ av}$	38 W
$Pv_{Tr\ max}$	138 W	$Pv_{Tr\ min}$	99 W
$Pv_{D\ max}$	64 W	$Pv_{D\ min}$	23 W



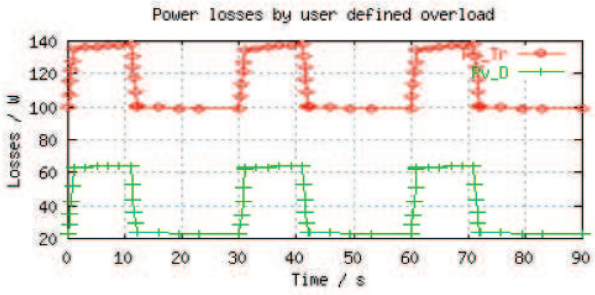


Figure 5.2.24 Presentation of results for temperatures and losses for a user-defined load cycle

5.3 Cooling power modules

Here, the main focus will be on forced air cooling and water cooling, since these types of cooling cover 95% of all power module applications. Other cooling methods, such as evaporative cooling and spray cooling, and natural air cooling, too, will be mentioned. However, these are still of minor importance for IGBT and MOSFET power modules. Details on natural air cooling and cooling plates are explained in chapter 4.2 in the context of (discrete) rectifiers.

The extensive heat build-up in power modules caused by forward, switching and blocking losses has to be dissipated by means of heatsinks; these heatsinks provide an expanded surface for convection and radiation, spreading the heat flow as well as reducing the intensity of transient thermal processes. Due to their internal insulation, all of the power modules in a system can be mounted onto one common heatsink, which may also take on some function in the design construction, too (case, chassis etc.). Heat dissipation through a heatsink works on the principle that the heat is dissipated to the coolant either by direct heat conduction or via a heat carrier. Coolants may be air, water or aqueous mixtures, or (less frequently) insulation oil, which is circulated by the effect of gravity or using fans or pumps.

5.3.1 Thermal model of the cooling system

The thermal equation of the heatsink is as follows:

$Q = \alpha \cdot A \cdot \Delta T = P_{tot}$

This result in the definition of the thermal resistance:

$$R_{th(s-a)} = \frac{\Delta T_{(s-a)}}{P_{tot}} = \frac{1}{\alpha \cdot A}$$

(Q - dissipated heat quantity, α - heat-transfer coefficient, A - heat transfer area)

Since T_s was measured at a certain point in order to determine $\Delta T_{(s-a)}$, the value for $R_{th(s-a)}$ only applies to this measuring point of ambient temperature (see chapter 5.3.2.4). Other measuring points will result in different values. To simplify analysis, a uniform heatsink temperature for all components is often assumed in other layouts containing several modules. Losses occurring in all of the heat sources on the heatsink are dissipated through the common $R_{th(s-a)}$.

The equation above for R_{th} shows that a high number of fins makes sense in order to increase the dissipation area. What must be ensured, however, is that the flow conditions are set in a way which will not excessively reduce the flow speed and hence the heat-transfer coefficient α. This explains, for example, why there are different optimisation criteria for heatsinks with natural and forced air cooling. In line with better heat penetration on the heatsinks as a result of higher power dissipation, homogenous heat distribution or more even heat spread, the effective heat exchange area A_{eff} increases and the efficiency of the heatsink increases or $R_{th(s-a)}$ decreases. Swirling the coolant as much as possible greatly increases the value of α, which also contributes to the reduction of $R_{th(s-a)}$.

In the explanation of power modules' thermal characteristics in chapter 5.2, the heatsink was initially described in the thermal equivalent circuit diagram by one "RC element" only ($R_{th/(s-a)}$, $Z_{th(s-a)}$). However, with a sudden increase in power dissipation at t = 0 from P = 0 to P = Pm, the transient thermal impedance characteristic of the heatsink $Z_{th(s-a)}$ versus time t is split up into several time constants, as shown in Figure 5.3.6. From this, the total thermal impedance characteristic $Z_{th(j-a)}$ of the assembly may be determined by adding the thermal impedance characteristics of the power module and the heat transfer to the heatsink. The Z_{th} curves can be described as the sum of n exponential functions using the following equations:

$$\Delta T_{(s-a)}(t) = P_m \cdot \sum_{\nu=1}^{n} R_{th\nu} \cdot \left(1 - e^{\frac{-t}{\tau_{th\nu}}}\right)$$

$$Z_{th(s-a)}(t) = \frac{\Delta T_{(s-a)}(t)}{P_m}$$

It thus follows that

$$Z_{th(s-a)}(t) = \sum_{\nu=1}^{n} R_{th\nu} \cdot \left(1 - e^{\frac{-t}{\tau_{th\nu}}}\right)$$

The number ν of summands and the values for R_{thn} and τ_ν are chosen such that a sufficient approximation of the curve shape can be produced with a reasonable amount of calculations involved, irrespective of the physical structure. The basis for determining values of R_{th} and τ_{th} is the existing Z_{th} curve. Mathematical programs and spreadsheets such as Excel (→ Solver) are able to solve equation systems with a large number of unknown elements by setting the sum of error squares to zero (0) for a large number of interpolation nodes, as shown in the following equation.

$$\left(Z_{th(s\text{-}a)}(t_n) - \sum R_{th\nu} \cdot \left(1 - e^{\frac{-t_n}{\tau_{th\nu}}}\right)\right)^2 = 0$$

In order to rule out absurd solutions, a constraint must define R_{th} and $\tau_{th} > 0$ sind. The number of R_{th}/τ_{th} pairs can be increased until the desired accuracy has been achieved. In most cases, 3...5 pairs are sufficient.

5.3.2 Factors influencing thermal resistance

5.3.2.1 Number of heat sources

The number of heat sources spread across the heatsink has a crucial impact on $R_{th(s\text{-}a)}$. Unless explicitly specified otherwise, the values given by heatsink manufacturers apply to a large-area heat impression across the entire mounting surface. The closer we approach this ideal case with a large number of distributed heat sources, the better this theoretical R_{th} value can be reached. Measurements are complex and time-consuming and manufacturer data on different configurations is hard to come by. FEM simulations could be a solution, since these simulations are especially meaningful whenever relative comparisons are to be made with known parameters. Figure 5.3.1 depicts simulations [56] of the same heatsink comprising 1 x (right) and 3 x 62 mm IGBT module(s) (left). For 3 modules the following applies:

$$R_{th(s-a)} = \frac{120°C - 40°C}{1800\ W} = 0{,}034\ K/W$$

The R_{th} of the same heatsink for identical ambient conditions will increase to the following value if just one module is mounted.

$$R_{th(s-a)} = \frac{74°C - 40°C}{600\ W} = 0{,}0566\ K/W$$

This is equivalent to a 65% increase. For some of their heatsinks, SEMIKRON specifies R_{th} in dependence of the number of modules and module size (Figure 5.3.2). Unless thermal impedances have been given for different layouts, they can be adjusted by weighing $R_{th\nu}$ with a correction factor gained from the ratio of thermal resistances. The time constants of the thermal impedances will remain the same.

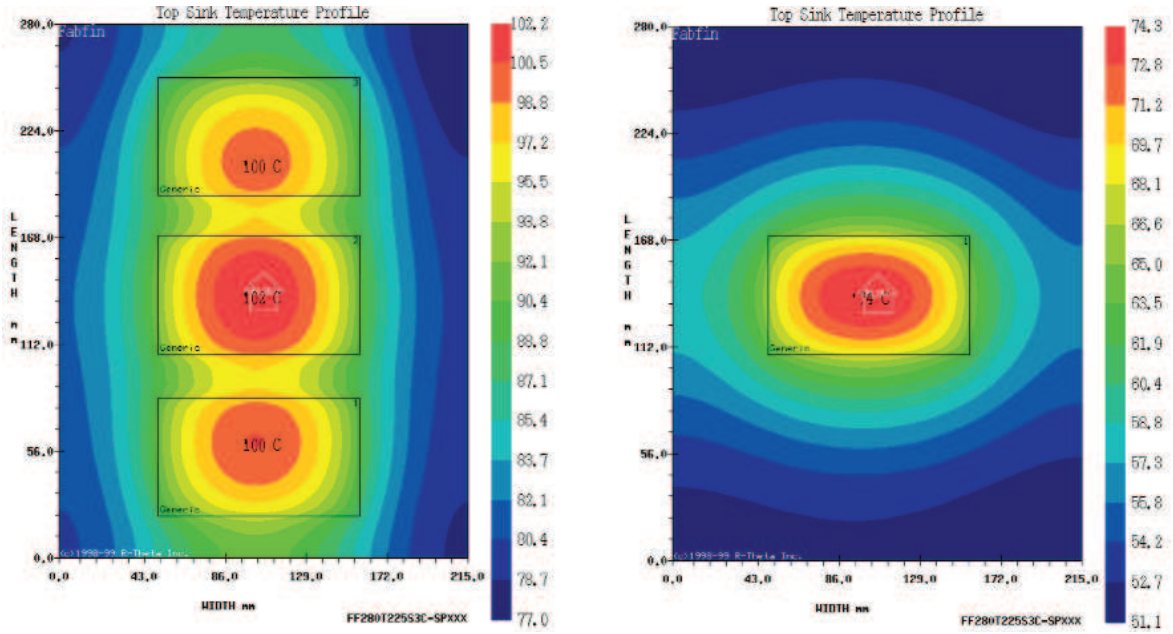
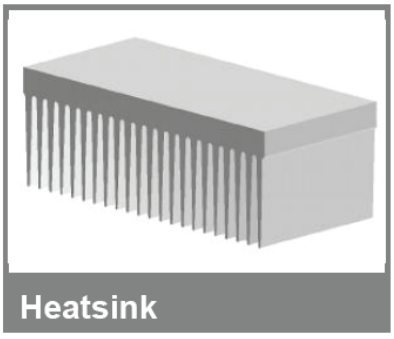


Figure 5.3.1 Simulation of heatsink performance for different numbers of components

P 16



Standard lengths	n	b / d Ø mm	R_{thha} K/W	R_{thha} with fan SKF 16B-230-01 K/W	w kg
P 16/170	3	20		0,05	4
P 16/200	3	20		0,046	4,7
	6	20		0,039	
	3	34		0,038	
	2	50		0,04	
	3	50		0,033	
P 16/300	6	34		0,036	7
	6	50		0,024	

Figure 5.3.2 Example of $R_{th(s-a)}$ as a function of quantity n and size b of the heat sources, given for an air cooler

5.3.2.2 Heat spreading

Heat spreading can be obtained either with good material heat conductivity, thick material layers or by using heat pipes (see chapter 5.3.6) in the heatsink itself. It can also be improved by spreading the heat sources evenly across the entire mounting area. This involves finding a compromise between compact design and good heat distribution. In the thermal simulation depicted in Figure 5.3.3, the thermal resistance $R_{th(s-a)}$ is reduced by 11% when the spacing between modules is increased from 0 mm to just 18 mm. The number and size of the sources of power dissipation are the same. Power dissipation amounts to 600 W per module and the ambient temperature is T_a = 40°C.

$$R_{th(s-a)} = \frac{120°C - 40°C}{1800\ W} = 0{,}034\ K/W$$

$$R_{th(s-a)} = \frac{74°C - 40°C}{600\ W} = 0{,}0566\ K/W$$

From a thermal point of view, a clearance of up to 3 cm would be desirable on an air cooler; this, however, would require a larger heatsink (→ $R_{th(s-a)}$ = 0.266 (-17%)). On a water cooler, this effect is less noticeable owing to its better heat dissipation. Here, a clearance of more than 1 to 2 cm will barely improve the situation.

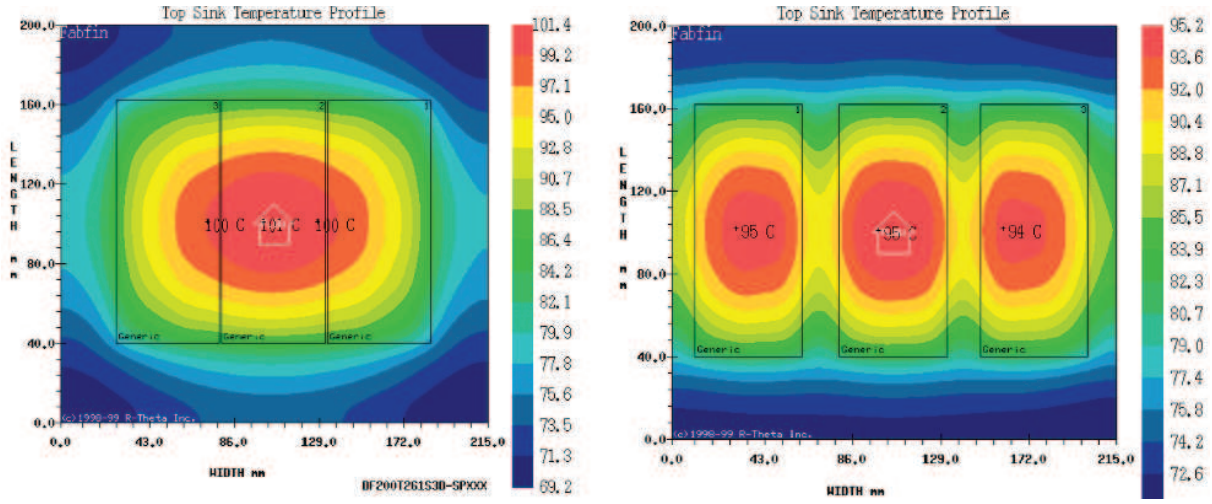


Figure 5.3.3 Effect of better distribution of heat sources across the heatsink surface, temperature simulation on the heatsink surface

5.3.2.3 Position of heat sources in relation to direction of cooling flow

Besides the number and distribution of heat sources on the heatsink, $R_{th(s-a)}$ also depends on the flow direction of the coolant. Figure 5.3.4 shall demonstrate this relationship with the example of a specific layout. The position on the edge of the heatsink is particularly unfavourable, since heat spreading in the direction of coolant flow is stronger than in the opposite direction.

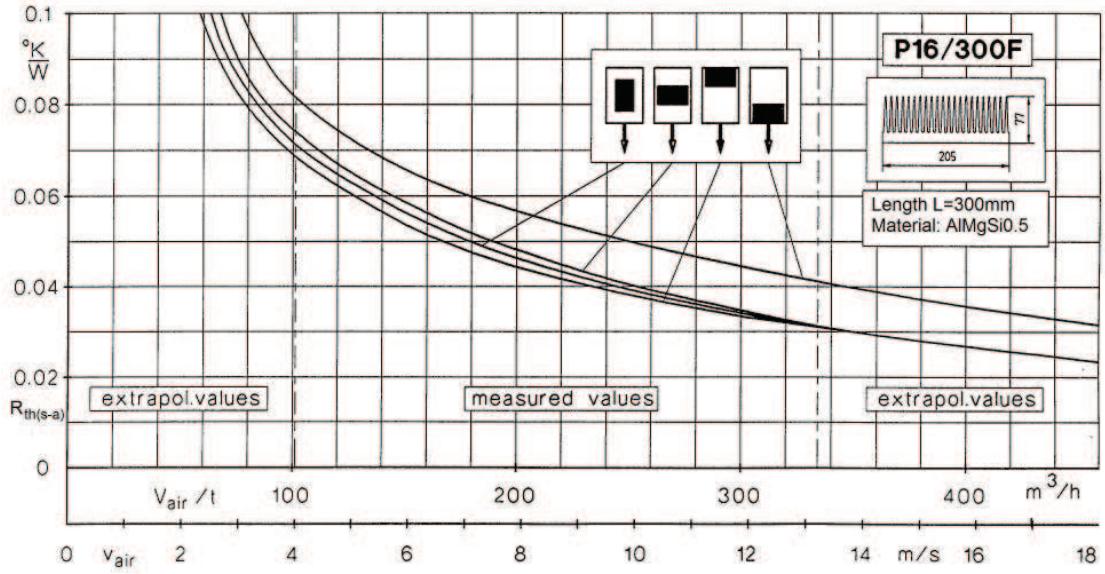


Figure 5.3.4 Thermal heatsink resistance $R_{th(s-a)}$ of a SKiiP assembly versus air flow and position of the SKiiP on the heatsink

5.3.2.4 Measuring points for determining R_{th}

In addition to all of the design influences, $R_{th(s-a)}$ also depends on the measuring point of the heatsink temperature. As you can see in Figure 5.3.3, for example, the heatsink surface may well display temperature differences of 30 K. In principle, T_s must be measured at the same point for which the value of $R_{th(c-s)}$ or $R_{th(j-s)}$ of the semiconductor modules was specified; otherwise the chain from the junction to its ambient area would be interrupted. Unfortunately, such reference points vary between (semiconductor) manufacturers (Figure 5.3.5) and there are also different reference points for the various SEMIKRON product groups. The measuring points most frequently used are those beside the module at chip position level or underneath the module in a borehole of up to 2 mm into the heatsink surface.

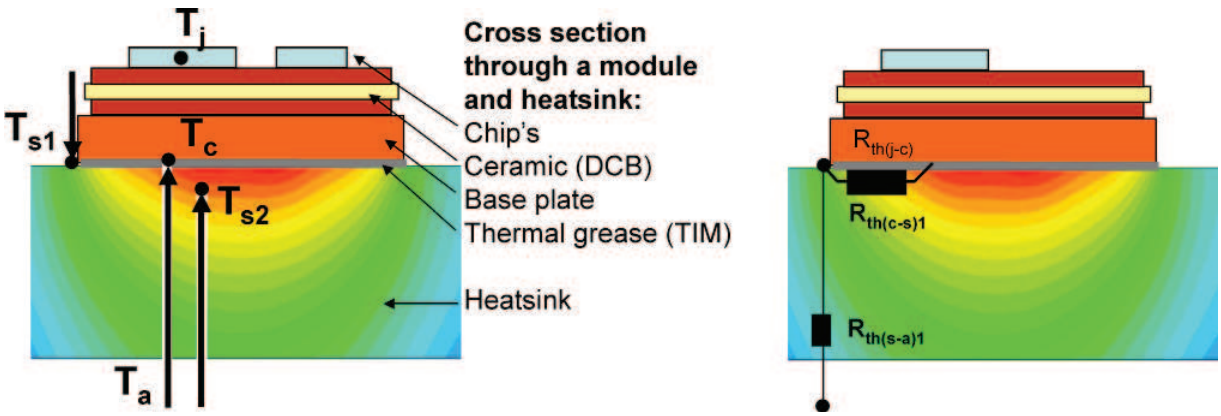


Figure 5.3.5 Measuring points T_{s1} and T_{s2} to determine $R_{th(c-s)}$ and $R_{th(s-a)}$

For all modules with base plate, SEMIKRON specifies $R_{th(c-s)}$ for a measuring point beside the module at its longitudinal side (ca. 1/3 away from the module corner). At this spot T_{s1}, the heatsink is far cooler than underneath the module. As a result, the temperature difference $\Delta T_{(c-s)}$ is high and $\Delta T_{(s-a)}$ is low. This results in a higher resistance $R_{th(c-s)1}$ and a lower $R_{th(s-a)1}$ compared to the other method where the heatsink temperature T_{s2} is taken underneath the module ($R_{th(c-s)2}$; $R_{th(s-a)2}$). The better the heatsink dissipates the heat, the greater the difference (water cooling ↔ air cooling). The advantage of method 1 - "next to the module" - is the better accessibility to the measuring point the the layout. A specially prepared heatsink is not required. Its disadvantage is the dependency of $R_{th(c-s)}$ on the heat spreading in the heatsink. Please note that you should always use the same reference point for comparative calculations in modules supplied by different manufacturers. As an approximation, we may assume $R_{th(c-s)1} \approx 2 \cdot R_{th(c-s)2}$. For modules without base plate, SEMIKRON specifies $R_{th(j-s)}$ for a spot underneath the chip. For this reason, method 2 ("underneath the module") must be chosen when heatsink measurements are taken for modules without base plate.

5.3.3 Natural air cooling (free convection)

Natural air cooling is used in low-power applications up to 50 W and even high-power applications if the use of fans is not possible or if extremely large cooling surfaces are available in the device. Since the thermal transient resistance of the heatsinks usually exceeds the internal thermal resistance of the power modules in the case of free convection, the temperature difference between chip (125°C) and cooling air (45°C) mainly decreases over the heatsink. Near the modules, the heatsink temperature is usually higher than with forced air cooling, for example 90...100°C. Because power losses are usually low with natural air cooling, heatsink root and fins do not have to be very thick, since heat conductivity has only a minor influence on the thermal features. The fin clearances have to be sufficiently large to obtain a favourable ratio between air uplift (drop of temperature / density) and air friction. A black coating on the heatsink will improve its radiation characteristics, and thus $R_{th(s-a)}$ by up to 25% as a function of the temperature difference between mounting area and ambient air. For more details, please refer to chapter 5.2.

5.3.4 Forced air cooling

In contrast to natural air cooling, forced air cooling can reduce the thermal heatsink resistance to 1/5...1/15. Figure 5.3.6 compares the $Z_{th(s-a)}$ characteristics of natural and forced air cooling up to the final $R_{th(s-a)}$ value using the example of a SEMIKRON P16 heatsink in different lengths.

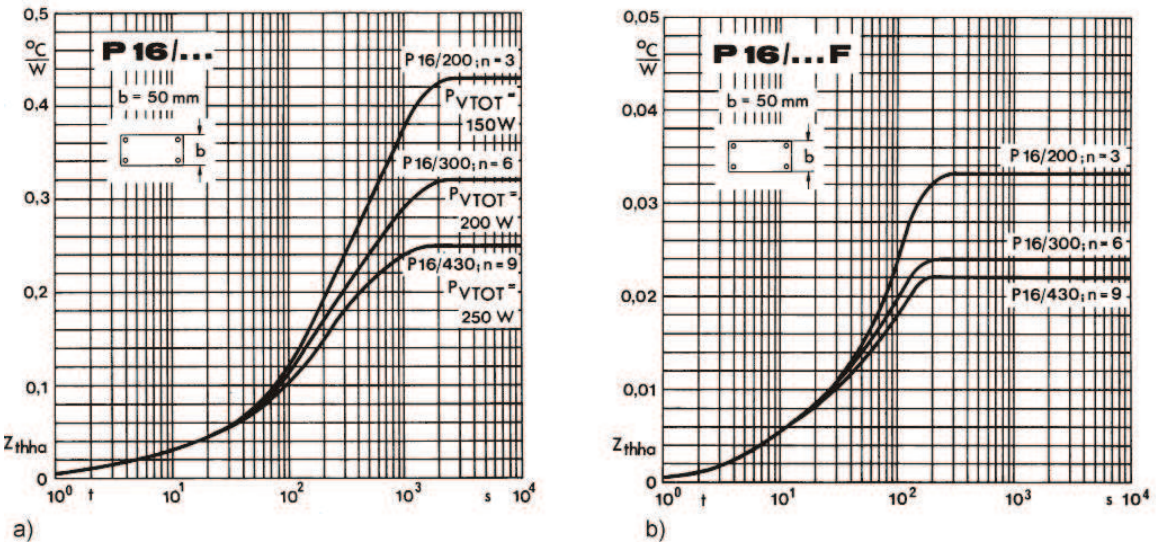


Figure 5.3.6 $Z_{th(s-a)}$(t) characteristics for different P16 heatsink lengths/length in [mm], number of heat sources n; a) in case of free convection with different power dissipation values; b) for forced air cooling

α is much higher with forced air cooling than with free convection. The rated surface temperature of forced air-cooled heatsinks should not exceed 80...90°C at a supply air temperature of 35°C (condition for datasheet ratings). Since convection is mainly responsible for the dissipation of heat, coating the heatsink black will have virtually no effect in the case of forced air cooling.

5.3.4.1 Cooling profiles

The heatsink material must display optimum heat conductivity and heat spreading (high coefficient of thermal conductivity λ) at reasonable material and processing costs. For this reason, aluminium is often preferred (λ = 247 W/K·m for pure Al), but copper is also used to meet particularly high requirements (λ = 398 W/K·m). The dependence of heat spreading on the production process and the alloy used is remarkable; in practice, heatsinks display λ values of between 150 W/K·m (Al-die cast alloy) and 220 W/K·m (AlMgSi extruded material). Heat spreading in the material has a considerable influence on the thermal efficiency of the heatsink. Therefore, optimised dimensioning is important for root thickness, number of fins, fin height and fin thickness:

- The *root* of a heatsink is the unfinned part of the mounting surface for the power modules where the heat is spread.
- The *fins* of an air heatsink are used to dissipate the majority of the heat to the environment by convection.

To determine optimised conditions for forced air-cooled heatsink profiles, heat conduction and convection can also be integrated by way of the fin height layout, which will result in the following formula on condition of some simplifications:

$$R_{th(s-a)} = \frac{1}{n \cdot \sqrt{\alpha \cdot U \cdot \lambda \cdot A} \cdot \left[\frac{1}{1+e^{-2\kappa}} - \frac{1}{1+e^{2\kappa}} \right]}$$

where $\kappa = h \cdot \sqrt{\frac{\alpha \cdot U}{\lambda \cdot A}}$

(α: heat-transfer coefficient, U: fin circumference, λ: coefficient of thermal conductivity of heatsink material,
A: cross-section of fins, h: fin height)

Table 5.3.1 provides a rough overview of the design features of various types of heatsink.

	
Thin root	Thick root
Many fins	Few fins
Lower $R_{th(s-a)}$	Higher $R_{th(s-a)}$
But:	
Low overload capacity (e.g. for pumps)	High overload capacity (e.g. for lifts)
Short time constants	Long time constants
Little heat spread	Good heat spread
High pressure drop – less air	Low pressure drop – more air
Sensitive to dirt	Less sensitive to dirt

Table 5.3.1 Properties and selection criteria for different heatsink profiles

5.3.4.2 Pressure drop and air volume

$R_{th(s-a)}$ continues to be mainly determined by the rate of air flow per time V_{air}/t depending on the average cooling air velocity v_{air} and the transfer cross section A:

$V_{air}/t = v_{air} \cdot A$

Instead of the assumed laminar air flow, air swirling on the fin surfaces will induce turbulent flow conditions which will improve heat dissipation to air, provided the fin surfaces are set out accordingly. Of course, it is not just the static, but also the transient thermal resistance (thermal impedance) Z_{th} which is reduced by forced air cooling. Figure 5.3.6 shows $Z_{th(s-a)}$ characteristics up to the final $R_{th(s-a)}$ value for natural and forced air cooling in a SEMIKRON P16 heatsink. Time behaviour also changes by a power of ten. While for natural air cooling the static end value will only have been reached after 2,000…3,000 s, in the case of forced air cooling this process is completed after just 200...300 s.

Increasing the number of fins and fin width will reduce the transfer cross section of the heatsink. As with increased heatsink length, the pressure drop in the cooling air Δp rises and the volumetric flow rate decreases. This is a counter-effect to extending the cooling surface. For this reason, each fan has an optimum with regard to flow cross section, heatsink length and volumetric flow rate. Heat dissipation is dependent on the fan properties, which are described in the fan characteristic $\Delta p = f(V_{air}/t)$ (Figure 5.3.7).

The intersection of the characteristic fan curve and the pressure drop curves for the heatsinks $\Delta p = f(V_{air}/t, L)$ enables the volumetric flow rate at the operating point to be determined according to Figure 5.3.7. When integrating the fan characteristic, the permissible operating voltage fluctuation (e.g. 230 V +/- 10%) must also be taken into account. Sufficient cooling has to be ensured even when a minimum voltage is applied, i.e. when there is less air flow. The heat transfer resistance $R_{th(s-a)}$ of the heatsink layout (Figure 5.3.8) is a function of the determined volumetric flow rate.

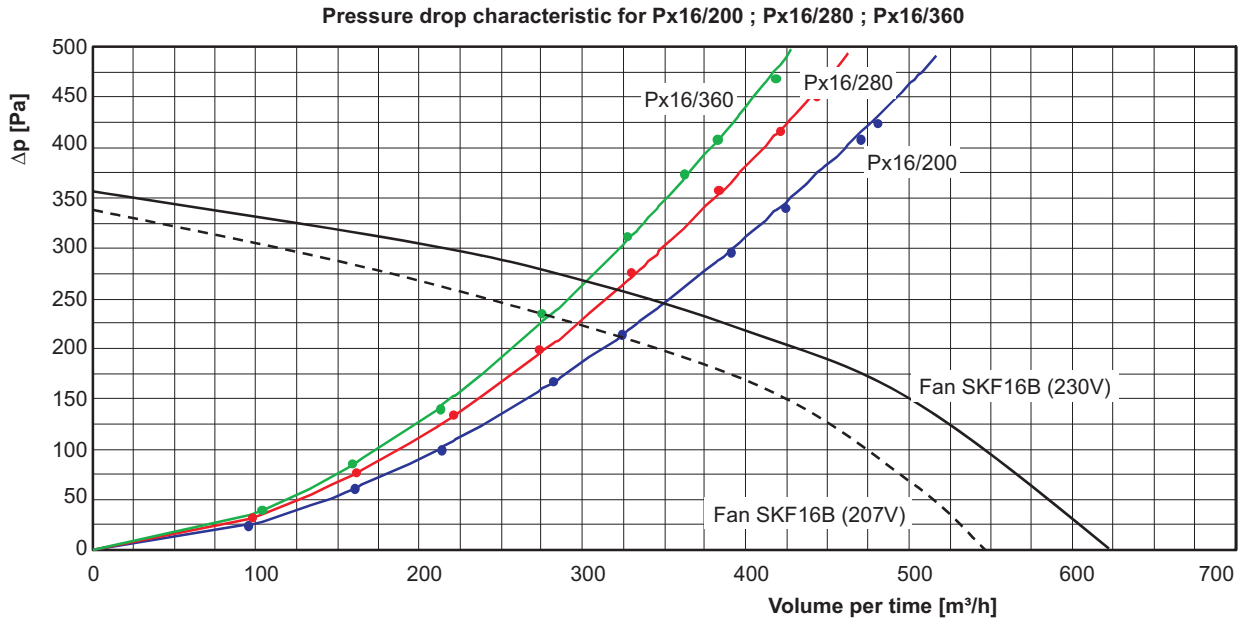


Figure 5.3.7 Cooling air flow of a Px 16/... heatsink profile for various heatsink lengths and fan characteristics

Nearby a known operating point, $R_{th(s-a)}$ can be determined as a function of the volumetric flow rate according to the following equation:

$$R_{th(s-a)2} = R_{th(s-a)1} \cdot \left(\frac{\dot{V}_1}{\dot{V}_2} \right)^K$$

where K = 0.7…0.9

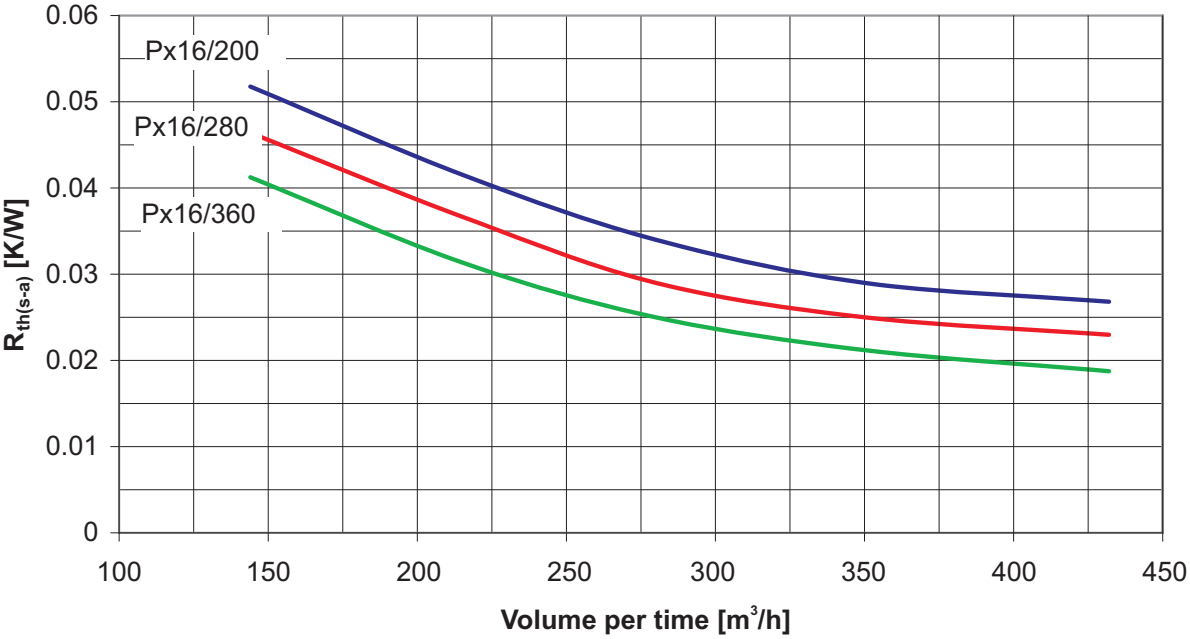


Figure 5.3.8 Characteristic curve of the Px16 heatsink as a function of the volumetric flow rate

5.3.4.3 Fans (ventilators, blowers)

Fans produce the air flow required for air cooling. Depending on the kind of heatsink and application, different fan types are used (Figure 5.3.9):

Axial-flow fans

The spin axis of the axial rotor runs parallel to the air flow. The air is moved through the axial rotor which acts similar to an airscrew. The advantages of axial-flow fans are their relatively small

dimensions in relation to the high air flow rate handled. Their disadvantage is the increase in pressure compared to radial-flow fans.

Radial-flow fans or centrifugal fans

Radial-flow fans (Figure 5.3.10) are used whenever, unlike axial-flow fans, a higher pressure increase for the same amount of air is important. The air is sucked in parallel or axial to the drive axis of the radial-flow fan, and deflected by 90° as a result of the rotation of the radial rotor and blown out in a radial direction. In order to minimise pressure losses due to the high exit velocity of air out of the radial-flow fan, care must be taken to continue the air chanelling, e.g. by using a diffuser.

Tangential or cross-flow fan

Cross-flow fans have an intake and blow-out slot across their entire length. Air is sucked into the interior of the rotor through the intake slot, where it is swirled, deflected and blown out highly homogenously. Cross-flow fans provide a high air flow rate even at low speeds and can therefore be constructed to emit relatively low noise. The rotor length and the outlet slot are matched to the heatsink width.

Figure 5.3.9 a) Axial-flow fan, b) Radial-flow fan, c) Cross-flow fan

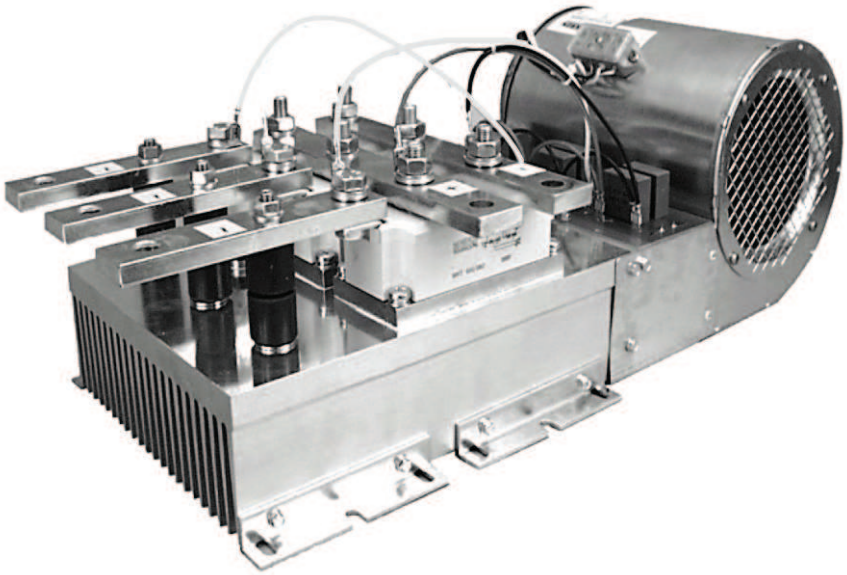


Figure 5.3.10 Set of 3 diode-half-bridge modules in a three-phase rectifier circuit on a cooling profile with radial-flow fan

5.3.4.4 Operating height

The amount of heat to be dissipated depends on the atmospheric pressure and the density of the cooling air. Air density, and hence cooling efficiency, decreases as the operating height increases. Decreasing air density deteriorates heat dissipation. Heatsink efficiency also deteriorates. To fac-

tor this in, it is necessary to reduce the inverter power, or to multiply R_{th} for thermal rating by a correction factor in accordance with Table 5.3.2 [57].

Height [m / ft]	Performance reduction	Correction factor for $R_{th(s-a)}$
0 / sea level	1	1
1000 / 3000	0.95	1.05
1500 / 5000	0.90	1.11
2000 / 7000	0.86	1.16
3000 / 10000	0.8	1.25
3500 / 12000	0.75	1.33

Table 5.3.2 Impact of operating height above sea level on thermal resistance

These performance constraints also apply to water coolers if the cooling water temperature is regulated by means of an air-cooled heat exchanger.

5.3.5 Water cooling

Water cooling in power modules can be used for very high power inverters (MW range) as well as for low-power devices which already have a water cycle for operating reasons (e.g. car drives, galvanic installations, inductive heating). In most cases, the admission temperature of the coolant values is as much as 50...70°C when the heat of the coolant is directly dissipated to the atmosphere; in industrial plants with active heat exchangers, the temperature is about 15...25°C. The temperature difference between heatsink surface and coolant, which is lower than for air cooling, may be utilised in two ways:

- increased power density, but with high dynamic ΔT_j of chip temperature per load cycle (for limits for module life see chapter 2.7), or
- low chip temperature, long module life.

Figure 5.3.11 shows an example of water cooling of a 6-fold SKiiP on a water-cooled heatsink.

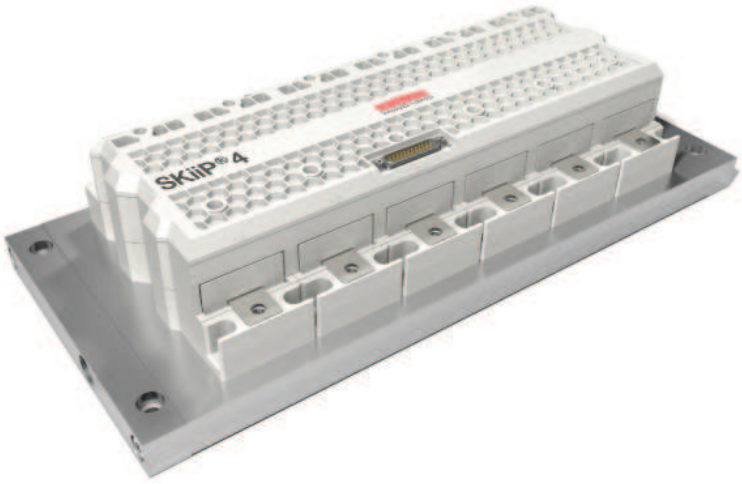


Figure 5.3.11 SKiiP4 layout with water-cooled heatsink

The following factors influence the thermal resistance in a liquid cooler:

- the contact area to the coolant (e.g. number of cooling channels)
- the volumetric flow rate as a function of the pressure drop (chapter 5.3.5.1)
- the heat storage capability of the coolant (chapter 5.3.5.2)
- turbulence in the water flow
- heat conduction and spreading in the heatsink (heatsink material)
- the coolant temperature (depending on viscosity and density)

Enlarging the contact area of heatsink / coolant will result in improved heat transfer. The traditional cooler is subject to limitations with regard to the number of cooling channels. The pin-fin cooler features little columns protruding into the coolant, which enlarges the contact area and also ensures sufficient turbulence (Figure 5.3.12).

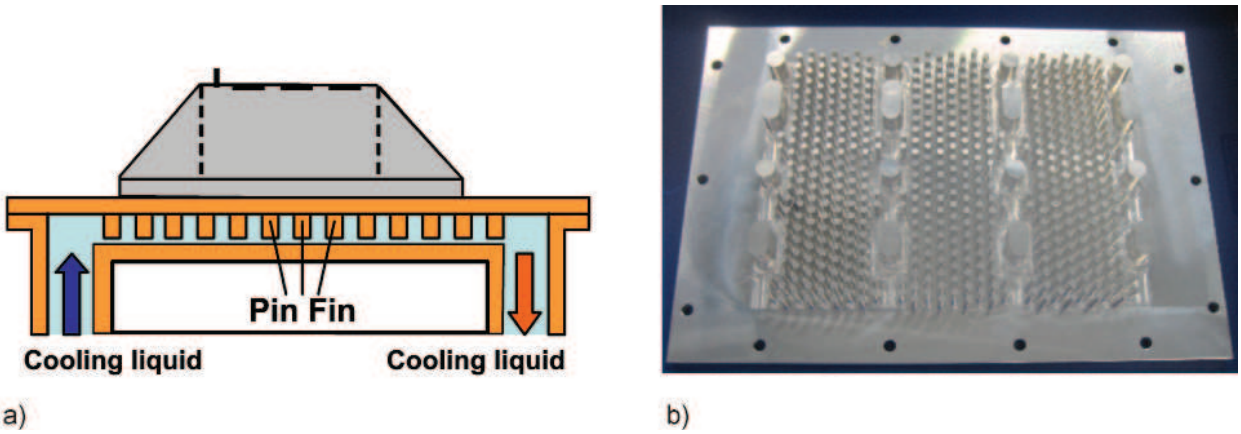


Figure 5.3.12 Pin-fin-liquid cooler to enlarge the heat transfer area; a) Schematic drawing; b) Photograph of the cooling side

The particular shape of the liquid cooler and a sufficiently high flow velocity creates a turbulent flow which substantially reduces the heat transfer resistance between heatsink and liquid (also see the spiral-shaped inserts in Figure 5.3.16). Without turbulence, a liquid film is created on the cooler surface which impairs heat transfer.

Even more so than with air coolers, an even distribution of heat sources across the heatsink surface is important for low thermal resistance. Due to the high heat-transfer coefficient of some 1000 W/(m²*K), the heat flow is dissipated to the cooling liquid with only minor cross-conduction. This means that essentially only those areas on which power semiconductor modules are mounted are used for cooling. Copper rather than aluminium as heatsink material will reduce the volume resistance, increase cross-conduction, thus also increasing the effective cooling area. A cooler made of copper allows for a reduction in $R_{th(j-a)}$ by approx. 20% for a standard IGBT module.

Especially in water-glycol mixtures, $R_{th(s-a)}$ depends on the coolant temperature. This is due the glycol viscosity, as well as the changing density of the coolant, albeit to a lesser extent. For a mixture of 50% glycol and 50% water in the temperature range of 10°C to 70°C, it was found that $R_{th(r-a)}$ was reduced by ca. 25% between the temperature sensor and coolant (Figure 5.3.13).

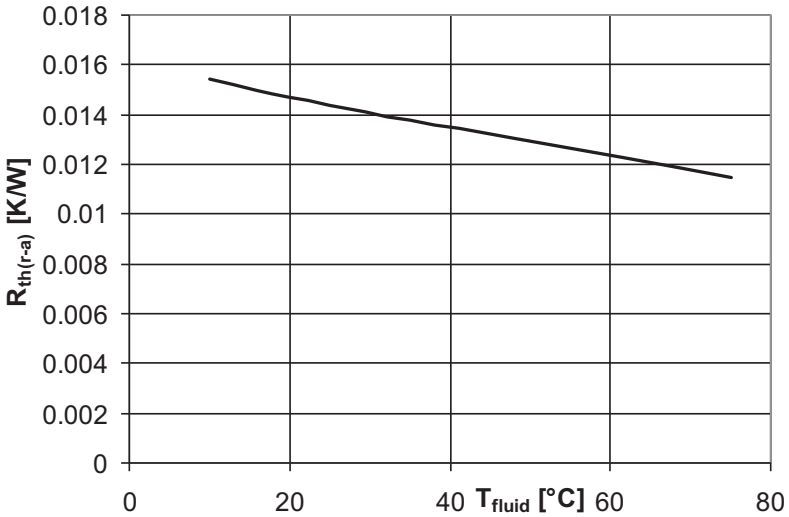


Figure 5.3.13 Dependency of the heatsink resistance on the coolant inlet temperature (NHC152 + SKiM-459GD12E4 temperature sensor)

5.3.5.1 Pressure drop and water volume, test pressure

In a closed cycle, liquid flow from the heat source and back can be generated by gravity (the heated liquid has a lower density, thus rising upwards to the heat exchanger, the cooled water sinks down to the heat source again; thermosyphon cooling). In most cases, however, a pump is used to circulate the liquid. This means that the available pumping power can be used to set the required water volume. Increasing water volume causes the thermal resistance to drop, but the pressure drop across the cooling unit also increases.

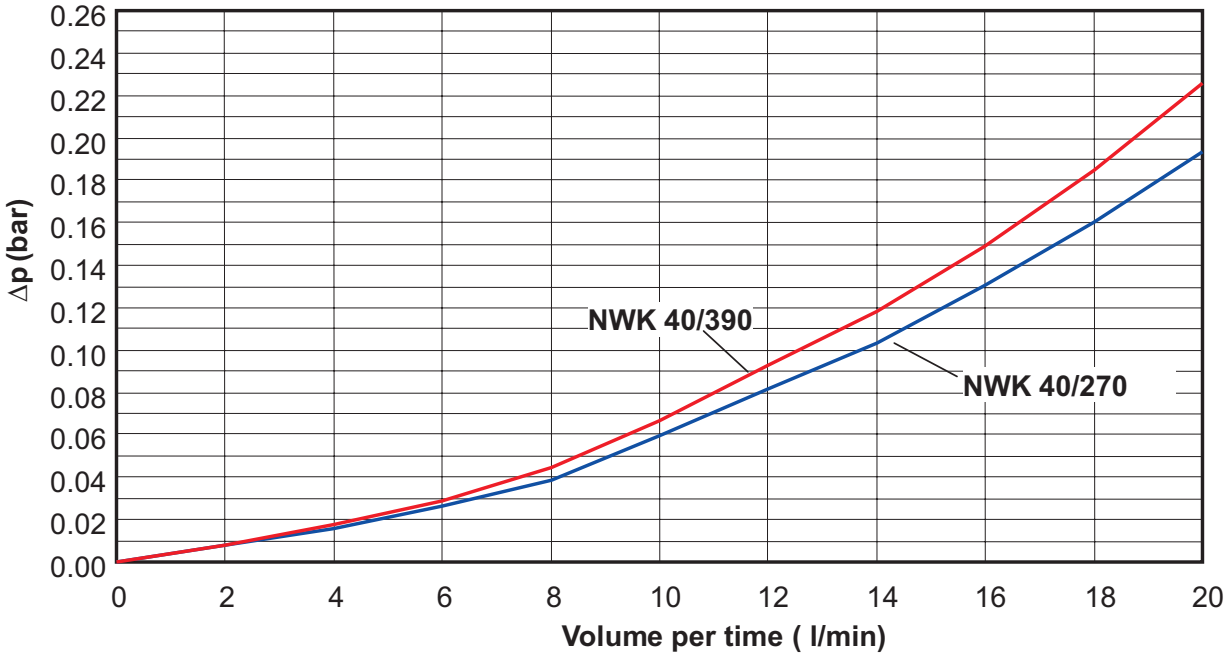


Figure 5.3.14 Pressure drop across a SEMIKRON water cooler (SKiiP3 – NWK40) for 2 different lengths (incl. 90 mm end pieces) dependent on the volumetric flow rate (water-glycol mixture 50%:50%, diagonally opposite inlet / outlet, T_a= 55°C)

The length data in Figure 5.3.14 applies to a water-cooled heatsink profile including 90 mm end pieces, e.g. …/390 means 300 mm heatsink profile + 90 mm end piece. This image also shows that an elongation of the profile by 66% from 180 mm to 300 mm will only increase the pressure drop by around 15%. It thus follows that the major part of the pressure drop is caused by the end pieces. This is not surprising, since there is narrowing in the cross section at the connection pieces, a surface for water distribution and 4 changes in direction which are responsible for the pressure drop. If a greater volume of water is to be pumped through the cooling circuit with reasonable pumping power, large pipe diameters are needed. In addition, care should be taken to ensure the following for the cooling cycle:

- no narrowing in the cross-section,
- no slam-shut valves,
- as few directional changes (elbows) as possible

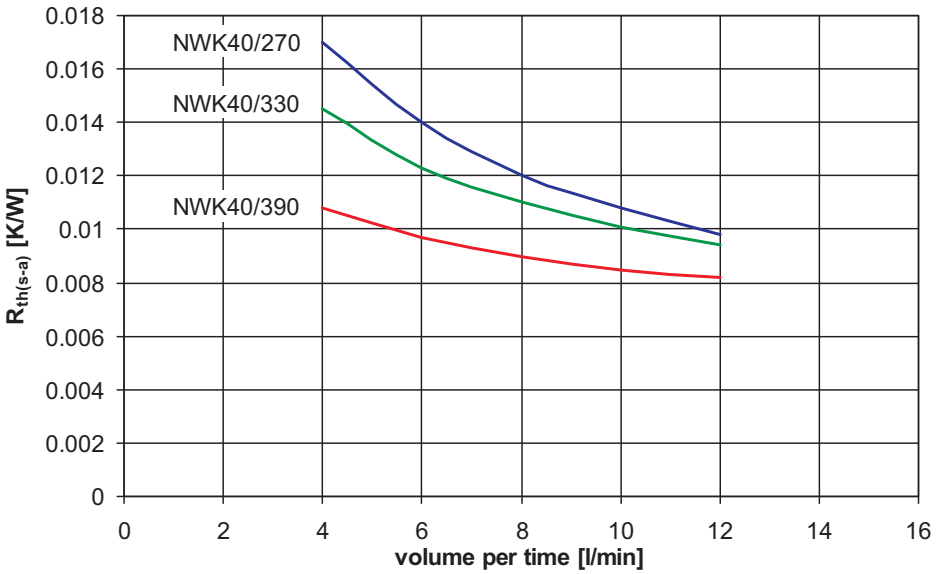


Figure 5.3.15 Thermal resistance as a function of the volumetric flow rate of the NWK40 with SKiiP3 for various lengths and a 50:50 water / glycol mixture

The SKiiP systems with water-cooler supplied by SEMIKRON are subjected to a leak test at a test pressure of 6 bar. The recommended operating pressure is 2 bar. Nearby a known operating point, $R_{th(s-a)}$ can be determined as a function of the volumetric flow rate according to the following equation:

$$R_{th(s-a)2} = R_{th(s-a)1} \cdot \left(\frac{\dot{V}_1}{\dot{V}_2} \right)^K$$

where K = 0.3…0.5

5.3.5.2 Coolant, cooling cycle and chemical requirements

The typical heat transfer medium to be used for liquid cooling is often water or a glycol/water solution (anti-freeze). More rarely, deionised water or insulation oil (fluorocarbons and PAO = synthetical hydrocarbons) is used. Due to its high heat retention capability (specific heat capacity c_p = 4.187 kJ/kg·K), water is generally preferred to oil or glycol for heat dissipation. Water can either form a closed circuit and be air-cooled by means of a heat exchanger, or fresh water is used which runs off after flowing through the cooling unit. Deionised water, which is characterised by low electric conductivity, can be used in closed circuits (cf. chapter 5.3.5.2). From the outset, fresh water is noticeably conductive, but this is of minor importance for semiconductor components with internal insulation, since the cooling water remains de-energized in contrast to non-insulated components.

It is important to choose a liquid that is compatible with the cooling circuit and provides either corrosion protection or a minimum risk of corrosion. To ensure corrosion protection in SEMIKRON water-cooled aluminium heatsinks, the glycol content must amount to at least 10%. Manufacturers of antifreeze mixtures even call for a higher minimum glycol content to avoid undercutting the necessary concentration of corrosion inhibitors for non-ferrous metals. The hardness degree of the cooling water must not exceed 6. At least for coolant temperatures above 60°C we recommend using a closed cooling circuit. Some of the explanations and tables below dealing with coolants originate from an application manual by Lytron Inc. [58]. Table 5.3.3 provides recommendations regarding which metals and liquids are compatible in the cooling circuit.

	Water	Glycol mixtures	Deionised water	Non-conductive liquids (Fluoro-inert, PAO)
Copper	X	X		X
Aluminium		X		X
Stainless steel	X	X	X	X

Table 5.3.3 Materials and compatibility of liquids [58]

Fresh water

Water is the most effective cooling liquid due to its high thermal capacity. We recommend using a closed circuit. Depending on its chemical composition, fresh water or tap water may cause rust formation in metals. Chloride, for example, which can usually be found in tap water is corrosive. Fresh water should not be used for a liquid cooling circuit if it contains more than 25 ppm of chloride or sulphates. The proportion of calcium and magnesium in water must also be observed, since both minerals cause limescale on metal surfaces, thus reducing the thermal performance of the heatsinks (Figure 5.3.16).

Minerals	Recommended limit
Calcium	< 50 ppm
Magnesium	< 50 ppm
Chloride	< 25 ppm
Sulphates	< 25 ppm

Table 5.3.4 Recommended upper limits for ions in cooling water [58]

a) b)

Figure 5.3.16 Cooling channels and turbulators (spirals); a) New; b) After extended use with unsuitable cooling liquid and heavy limescale

Deionised water

Deionised water was freed from ions such as natrium, calcium, iron, copper, chloride and bromide. The deionisation process removes harmful minerals, salts and other impurities which may cause corrosion or limescale. Compared to tap water and most other liquids, deionised water has a high electric resistance and is an excellent insulator. But it easily turns acid when it comes into contact with air. Carbon dioxide in air dissolves in water, thus resulting in an acid pH-value of approximately 5.0. Pressure compensation vessels must therefore be separated from air by means of a membrane. This limits the maximum fluctuation of the temperature range for the coolant. It may be necessary to use anticorrosives in applications with deionised water. Connection pieces should be nickel-coated. Copper leads are incompatible with the use of deionised water for cooling plates or heat exchangers. Leads made of stainless steel are recommended.

Inhibited glycol and aqueous solutions

Due to the corrosive effect of water and the often necessary frost-resistance, open or closed circuits with pure water are hardly ever used. **E**thylene **G**lycol **W**ater (EWG) and **P**ropylene **G**lycol **W**ater (PWG) are the two most frequently used solutions in liquid cooling applications. Ethylene glycol has positive thermal properties such as a high boiling point, low freezing point, stability across a wide temperature range, a relatively high specific heat capacity and thermal conductivity. It also features low viscosity, meaning the piping requirements are less strict. PGW is used for applications where toxicity might be a problem. The glycol used in cars should not, however, be used in a cooling system or heat exchanger, since it contains a silicate-based rust inhibitor. These preventives may turn solid and cause deposits to form on the surfaces of heat exchangers, in doing so impairing their efficiency. Glycol solutions should contain an anticorrosion agent.

By adding glycol, for example, the heat retention capability of the coolant will diminish (e.g. 3.4 J/(kg*(kg·K) for an addition of 50% glycol and a coolant temperature of 40°C). Since the viscosity and specific weight of the coolant will increase, the thermal resistance from heatsink to coolant $R_{th(s-a)}$ will increase substantially together in line with the percentage of glycol. Compared to pure water, 10% glycol will cause an increase in R_{th} of around 15%, while adding 50% glycol will cause an increase of 50...60%. If the glycol content is increased to as much as 90%, R_{th} will double. Please note that these statements also depend on the flow conditions in the heatsink and the coolant temperature.

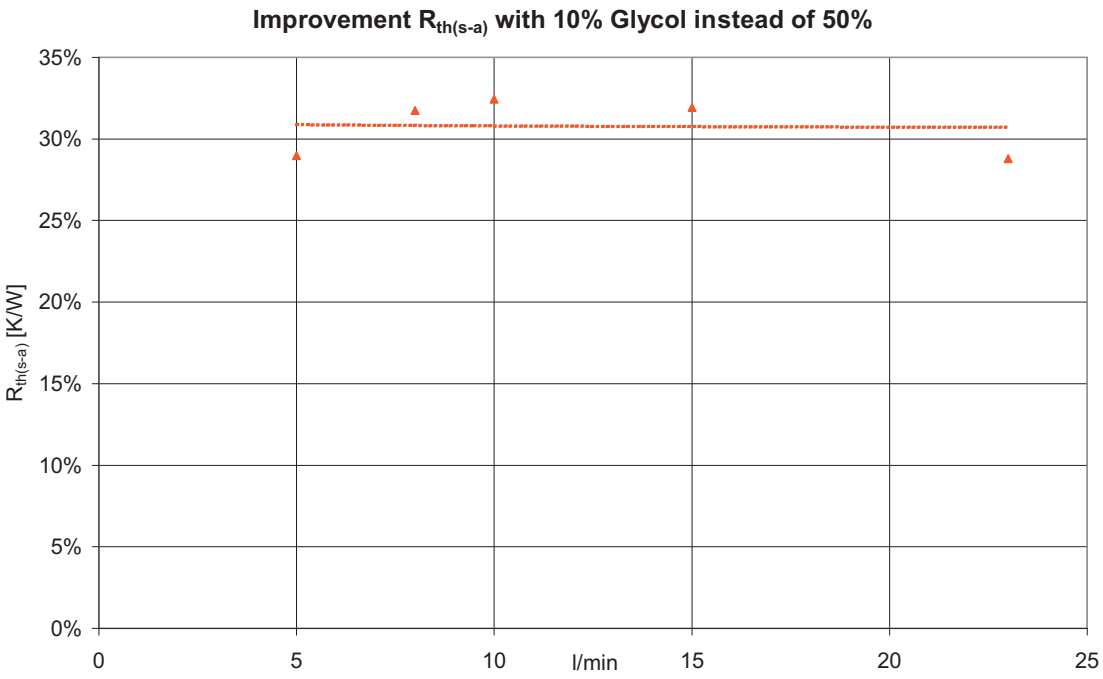


Figure 5.3.17 Influence of water-glycol mixture ratio on $R_{th(s-a)}$ for different flow rates

5.3.5.3 Mounting direction and venting

When setting up the cooling circuit, care must be taken that cooling is not blocked by air bubble build-up. The best mounting set-up therefore consists of vertical channels, while the worst is horizontal channels on top of each another, since the top channel accumulates the air bubbles (Figure 5.3.18).

The preferred flow direction is upwards with the inlet at the bottom and the outlet at the top in the control cabinet. Loops in the water flow, i.e. an "up and down" arrangement in the cabinet is disadvantageous. In that case, vent valves would be required in the cooling circuit above the power semiconductors. After the cooling unit has been filled, a test run with the highest flow rate should be performed for an extended period of time (> 0.5 h) without exposing the unit to normal electrical operation. A high flow rate (l/min) may remove existing air bubbles that might have been generated when the unit was first set up.

When designing parallel cooling circuits, steps must be taken to ensure that the pressure drop is the same in all parallel channels (same number and length of heatsinks, tubes, number of directional changes). The inertia of water in the direction of flow must be observed, since this is responsible for straight water flow, even if equally long parallel paths turn off sideways. Baffles to feed water into the branching channels must be used.

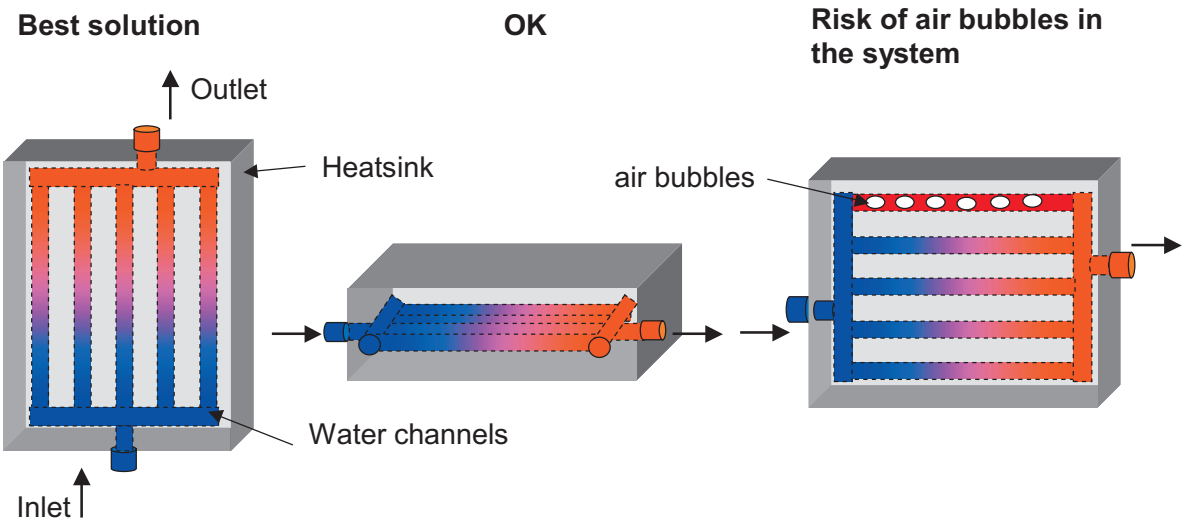


Figure 5.3.18 Tips on how to arrange water coolers

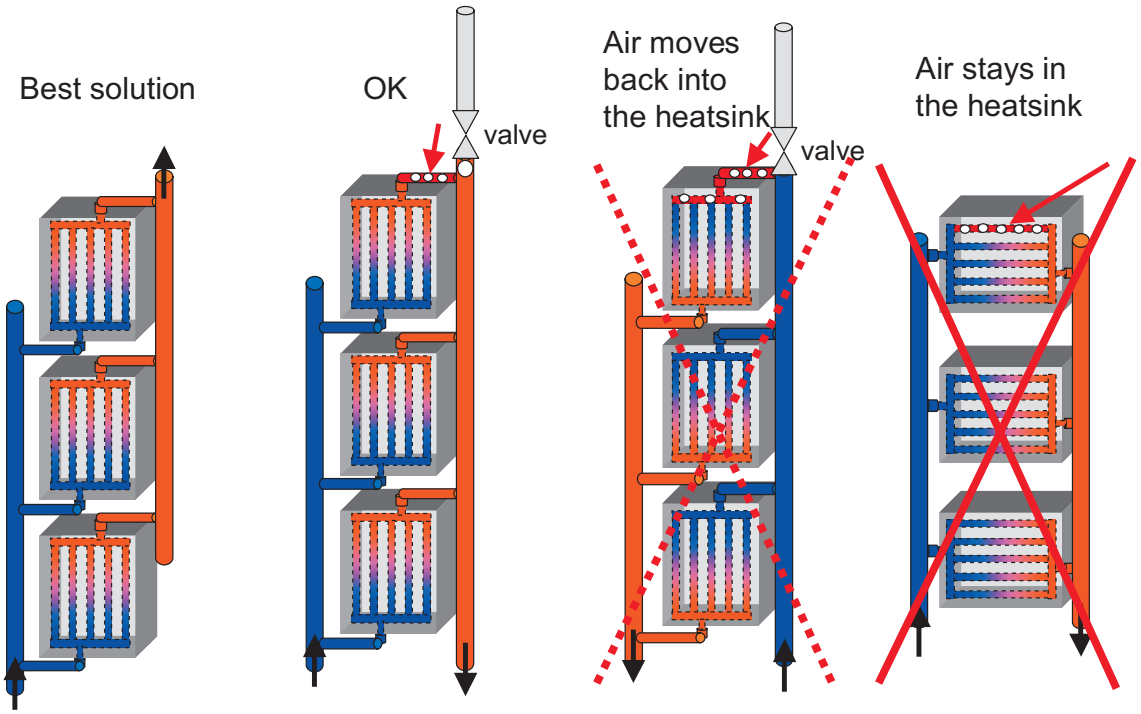


Figure 5.3.19 Setting up the water circuit

5.3.5.4 Other liquid cooling possibilities

Microchannels

Microchannel coolers are a special type of liquid cooler (Figure 5.3.20). In the DBC process, the microchannel cooler is furnished with several copper foils that are inserted between two DBC layers. These foils are punctured such that the holes are offset against each other. In the ceramic substrate of the bottom DBC layer there is a liquid inlet and outlet. Due to the offset bores in the sheet copper stack, a turbulent flow is created even at a low coolant flow rate, which ensures good heat transfer from the component being cooled to the cooling liquid. In this way, a very good cooling effect can be achieved with a relatively low pressure drop and little coolant. A disadvantage is

the high risk that channels might get clogged up by dirt or scaling or the steep temperature gradient within a module due to the low water quantity.

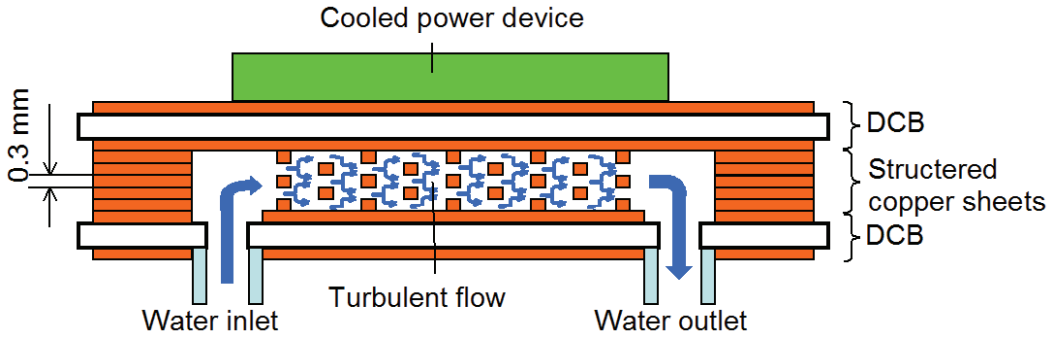


Figure 5.3.20 Diagram showing cross-section of a microchannel cooler

Phase transformation cooling

Phase transformation cooling utilises the fact that a given heat quantity (evaporation heat) - the amount of heat depends on the liquid - is required to evaporate a liquid in order to transform the liquid heat carrier into a gaseous state. If the gas condenses, this heat quantity will then be dissipated again. If you manage to keep this cycle of evaporating and condensing going in a closed vessel, large heat quantities may be transported from the point of evaporation to the point of condensation. Gravity and capillary forces will be sufficient to keep the heat carrier moving; pumps are not necessary. Various kinds of cooling equipment use phase transformation for heat transport.

Evaporative cooling

The coolant evaporates at the hot spots, e.g. a power module, gas bubbles will rise and condense on the colder case or separate condenser (Figure 5.3.21).

CAUTION: If the heat flow density is too high, a compact layer of vapour may be created at the heat source. This interrupts the thermal contact between heat source and liquid, meaning that cooling will be abruptly stopped (Leidenfrost effect).

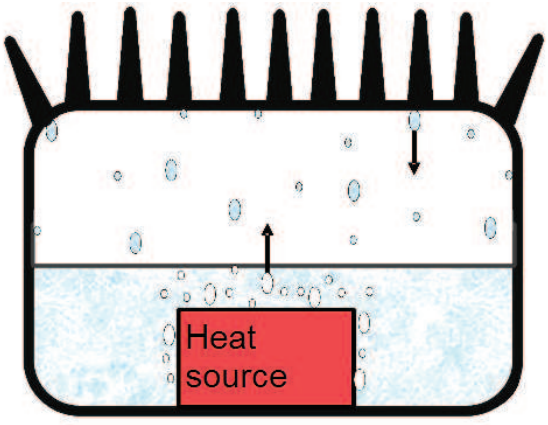


Figure 5.3.21 Diagram showing evaporative cooling

Spray cooling, jet cooling

These cooling methods use the principle of spraying the liquid coolant onto the surface either as droplets or jet (Figure 5.3.22). To some extent, the heat of evaporation is utilised here, too. Cooling may be applied from one side or both sides. The coolant evaporates at the spot where it hits the surface and condenses at colder spots. Typical coolants are often inert liquids, such as fluorinated hydrocarbons which are available with a wide range of boiling points. Water cannot be used for direct spraying onto chips, because its electric conductivity gets too high even after short use, and this would cause shorting at the chip edges.

It is advantageous if the coolant hits the chip directly, since this will result in optimum cooling directly at the point of heat generation and the exchange of coolant at the spot which is to be cooled

occurs rapidly. The disadvantages of spray and jet cooling are the low amounts of evaporation heat produced by the fluorinated hydrocarbons, the complexity of the cooling arrangement, the high pressure of 3 to 15 bar prevailing in the entire cooling system and the risk of nozzle clogging (Ø some 0.1 mm). Another problem is the densely packed bond wires lying side by side which often obstruct direct spraying of the chips.

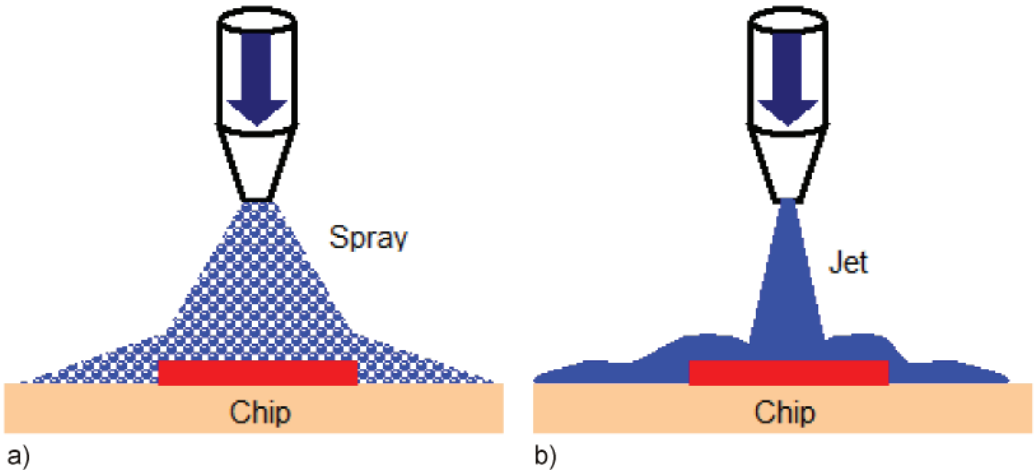


Figure 5.3.22 Principle behind spray cooling (a) and jet cooling (b)

Direct base plate cooling

This cooling method eliminates the thermal resistance of heatsink and thermal paste layer between the module and the cooling liquid by directly mounting the module and its base plate over an opening in the heatsink. The necessary sealing is ensured by an O-ring. $R_{th(j-a)}$ can be reduced by ca. 25% with this method. Two different types can be implemented. With the first type, the module base plate has a structured surface (pin fins) which is immersed into the cooling liquid contained in a trough. For the second variant, the company Danfoss has coined the term "ShowerPower®" [59]. Here, a plastic insert with many parallel holes in the heatsink opening creates a turbulent and vertical flow which ensures good and even cooling (Figure 5.3.23). The advantage of the latter solution is the low-cost manufacture of the plastic inserts as compared to structured base plates, while its disadvantage is the reduced contact area and the high pressure drop.

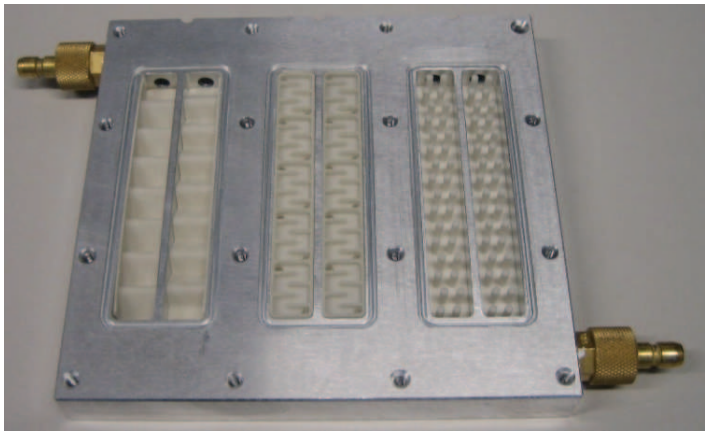


Figure 5.3.23 Test cooling plate with various inserts for direct base plate cooling

5.3.6 Heatpipes

The advantages of heatpipes are:
- their extremely high heat transport capacity (100 times, other sources say 1000 times higher than copper) with small temperature gradient
- no mechanically moved parts, i.e. no maintenance required
- they can be produced in almost any shape.

Heatpipes are used in order to transport heat effectively from the heat source to a remote location where the heat is dissipated to a cooling unit (cooling profile, heat exchanger). Alternatively, heatpipes are integrated into the root of the cooling profile to increase heat spreading inside a heatsink, thus reducing the thermal resistance $R_{th(s-a)}$.

Heatpipes consist of a hermetically sealed copper pipe that is filled with a liquid under reduced pressure. The inner wall of the heatpipe is clad with a capillary structure (wick). At the hot end the liquid will evaporate absorbing heat of evaporation; the vapour transports the heat to the cooler end where it condenses and dissipates the heat of evaporation to a heatsink or heat exchanger again. The liquid flows back to the hot end, which is supported by the capillary structure (Figure 5.3.24).

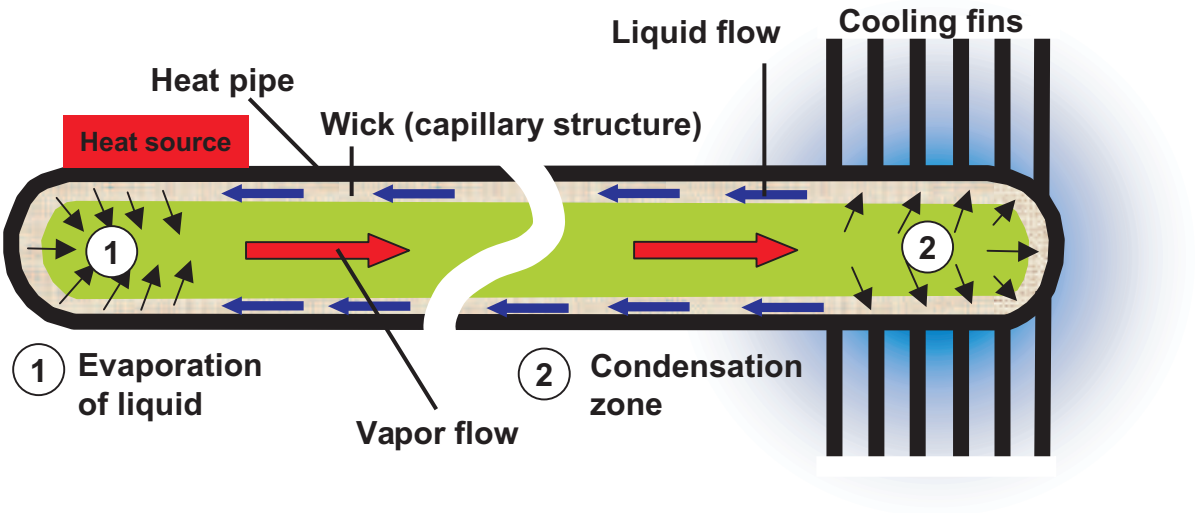


Figure 5.3.24 Principle behind a heatpipe. Since gas and liquid are almost in a balance in (1) and (2) and the same pressure is present, the temperatures in (1) and (2) are almost identical.

The capillary structure at the inside of the pipe wall (wick) is a porous structure which supports the capillary effect. It is made of metal foam or carbon fibre, for example. A variety of designs are common:
- sintered powder (highest cooling effect)
- enlarged surface at the inside pipe wall (weak capillary effect only)
- grid or mesh structure (most frequently used).

The function of the heatpipe depends on its position. The heatpipe can only work against gravity (i.e. evaporating at the top pipe end, condensing at the bottom end) if it has a sintered capillary structure. Different media are used as heat transport media, depending on the intended operating temperature range. The temperature range is generally limited: towards low temperatures by the freezing point of the heat transport medium; upwards by the critical point when a distinction between liquid and gaseous state of matter is no longer possible. Frequently used media in heatpipes are water (cannot be used below 0°C), acetone, alcohol, ammonia and fluorinated hydrocarbons.

5.3.7 Thermal stacking

When thermally stacking several heatsinks, in particular in combination with larger power electronics assemblies, the reduction in coolant flow rate resulting from the increased pressure drop and pre-heating of the coolant for the "backward" units has to be considered in the calculations (Figure 5.3.25b).

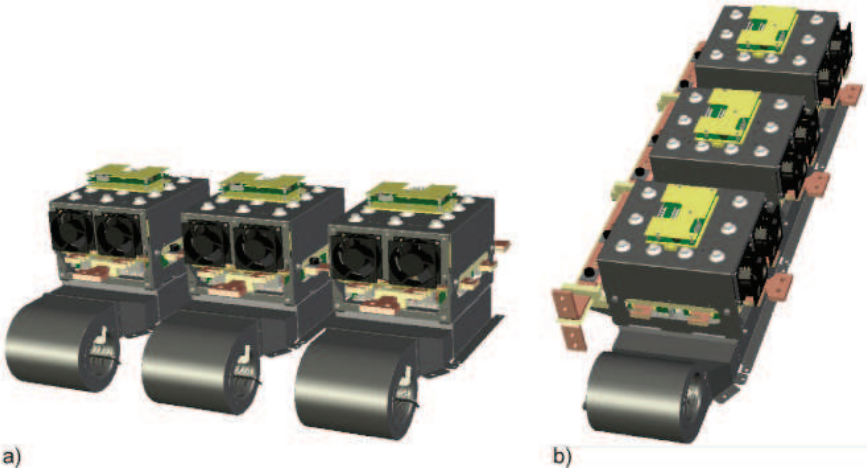


Figure 5.3.25 a) Individual cooling; b) "Thermal stacking" of 3 SEMIKUBEs with forced air cooling

The following two methods are suitable for calculating pre-heating.
a) Determining a thermal impedance $Z_{th(a\text{-}a')}$ between measuring points at the heatsink 1, 2 and 3
b) Calculating coolant pre-heating; the coolant outlet temperature from the first module is the inlet temperature at the second one etc.

5.3.7.1 Determining an additional thermal impedance

Pre-heating is determined by total power dissipation $P_{tot(n)}$ of the heat source, the stationary thermal resistance $R_{th(a\text{-}a^*)}$ or the transient thermal impedance $Z_{th(a\text{-}a^*)}$ between two adjacent heatsinks (Figure 5.3.25b). To this end, the temperature differences between the heatsink temperatures must be determined at a given power dissipation. As time passes, the second and any other heatsink will get warmer than the unit directly in front. This temperature difference divided by the component power dissipation results in $Z_{th(a\text{-}a^*)}$. For this part of the transient thermal impedances, 1 R/Tau element is sufficient in most cases. The following known correlation applies to component 1 in the direction of coolant flow:

$$Z_{th(s\text{-}a)1} = \sum_{\nu=1}^{n} R_\nu \cdot \left(1 - e^{\frac{-t}{\tau_{th\nu}}}\right)$$

To cater for component 2, an additional element for the temperature difference between heatsink 1 ("a") and 2 ("a*") is introduced. This pre-heating depends on the losses of component 1, which is why all of the losses must be weighted. If the losses of all heat sources are identical, this may be omitted:

$$Z_{th(s\text{-}a)2} = \sum_{\nu=1}^{4} R_\nu \cdot \left(1 - e^{\frac{-t}{\tau_{th\nu}}}\right) + \frac{P_{tot1}}{P_{tot2}} \cdot R_{th(a\text{-}a^*)} \cdot \left(1 - e^{\frac{-t}{\tau_{th(a-a^*)}}}\right)$$

For component 3 and any additional one, this applies by analogy:

$$Z_{th(s\text{-}a)3} = \sum_{\nu=1}^{4} R_\nu \cdot \left(1 - e^{\frac{-t}{\tau_{th\nu}}}\right) + \frac{P_{tot1} + P_{tot2}}{P_{tot3}} \cdot R_{th(a\text{-}a^{**})} \cdot \left(1 - e^{\frac{-t}{\tau_{th(a-a^{**})}}}\right)$$

5.3.7.2 Calculating pre-heating for air cooling

The basic idea behind this method is to retain the well proven basic equations of temperature calculation and re-determine the coolant inlet temperature for the "n-th" element only: This can easily be done using the heat retention capability of the coolant, if even through-heating is assumed. This can easily be done using the heat retention capability of the coolant, if even through-heating is assumed. Both the specific weight and the heat retention capability are temperature-dependent, which is why there is a temperature coefficient for pre-heating.

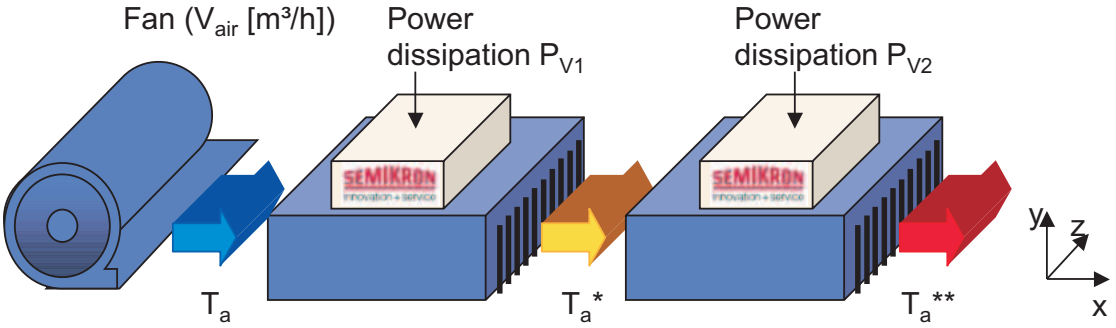


Figure 5.3.26 Thermally stacked, air-cooled layout, split into sectors with different air pre-heating

The general formula is:

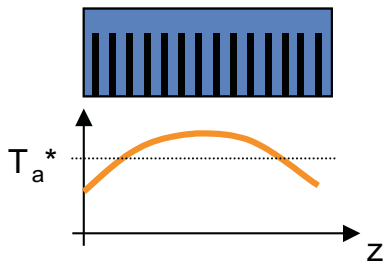
$$T_a^* = T_a + \left(\frac{1}{c_p \cdot \rho} + TC_c \cdot T_a \right) \cdot \frac{P_{tot1}}{V_{air}}$$

c_p:	Specific heat capacity of air [kJ/K/kg]
ρ:	Density of air [kg/m³]
TC_c:	Temperature coefficient of the specific heat capacity
T_a*:	Coolant temperature for the second heat source
P_{tot1}:	Power dissipation of heat source 1

Adapted to an average atmospheric pressure of 1 bar, a basic temperature of 0°C and the conversion to a specification for the volumetric flow rate in [m³/h], the following results:

$$T_a^* = T_a + \left(\frac{3{,}6}{1{,}006 \cdot 1{,}275} + 0{,}01\,°C^{-1} \cdot T_a \right) \frac{°C \cdot m^3}{W \cdot h} \cdot \frac{P_{tot1}}{V_{air}} \cdot K_{Ing}$$

P_{tot1} [W]:	Power dissipation of heat source 1
V_{air} [m³/h]	Volumetric flow rate through the heatsink
K_{ing}:	Correction factor for uneven heat profile at the outlet of heatsink 1



K_{Ing}=1...1,25 to consider average air temperature at the section

Figure 5.3.27 Uneven temperature profile of the exiting air over the fan cross section if heat sources are arranged centrally

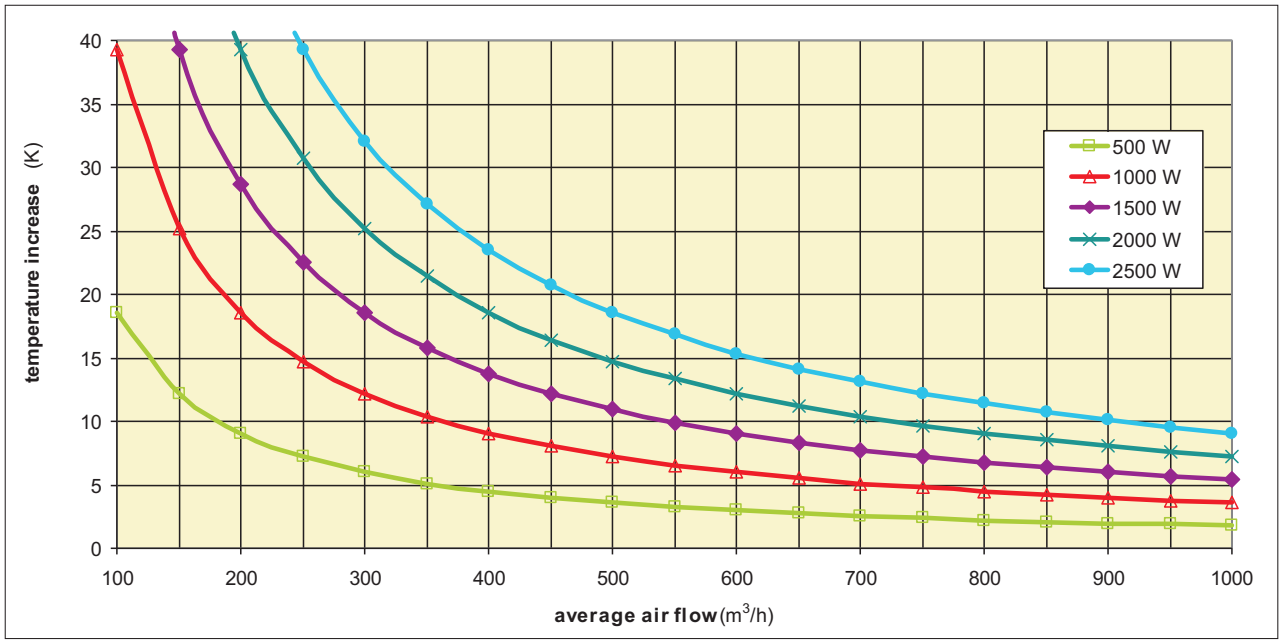


Figure 5.3.28 Temperature difference between incoming and outgoing air as a function of power dissipation P_{V1} (W) and the volumetric flow rate, T_a = 40°C

5.3.7.3 Calculating pre-heating for water cooling

In principle, the same basic equation applies to thermal stacking for liquid cooling as for air cooling: However, it must be borne in mind that the dynamic viscosity changes as a function of the temperature. The heat retention characteristic for a 50:50 water/glycol mixture and a conversion to the volumetric flow rate in [l/min] results in:

$$T_a^* = T_a + (0{,}0174 - 0{,}000013 \cdot °C^{-1} \cdot T_a) \cdot \frac{°C \cdot l}{W \cdot min} \cdot \frac{P_{tot1}}{V_{H2O}}$$

For pure water, the specific heat capacity and the temperature coefficient will change to:

$$T_a^* = T_a + (0{,}0133 - 0{,}000008 \cdot °C^{-1} \cdot T_a) \cdot \frac{°C \cdot l}{W \cdot min} \cdot \frac{P_{tot1}}{V_{H2O}}$$

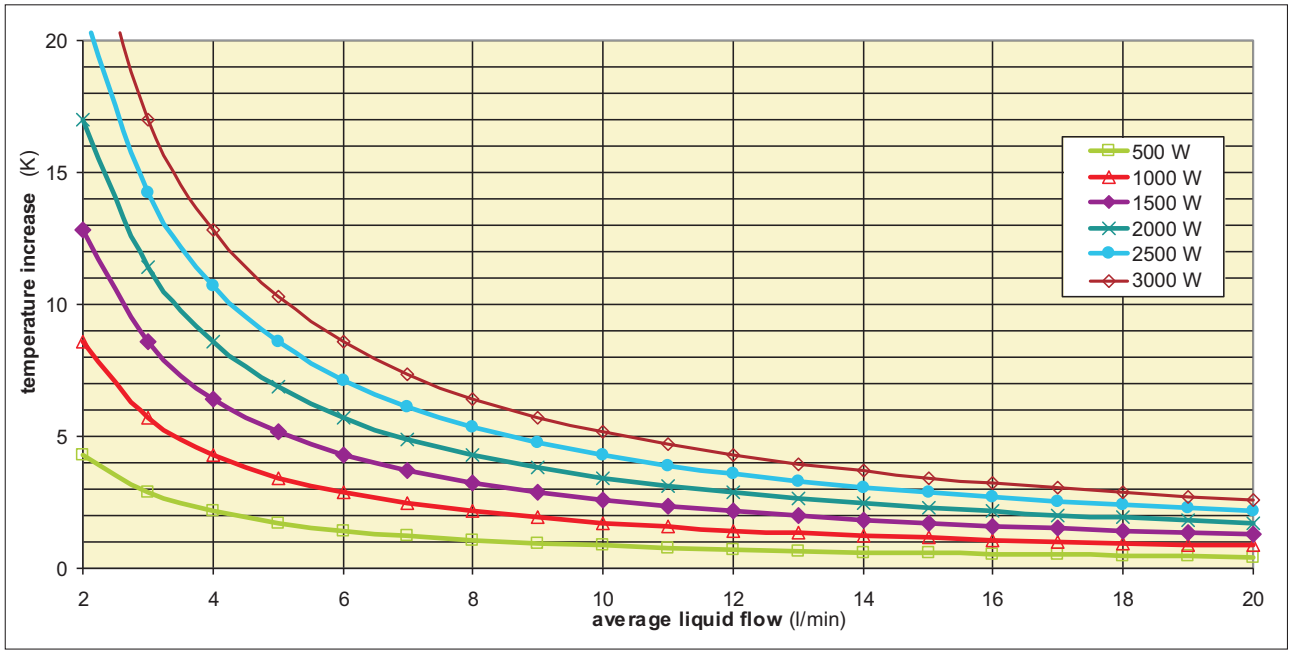


Figure 5.3.29 Temperature difference between water/glycol mixture flowing in/out as a function of the power dissipation and the volumetric flow rate, T_a = 25°C, 50% glycol

5.4 Power design, parasitic elements, EMC

Power circuits used to connect power semiconductors and passive components (L, C etc.) are designed in printed circuit board technology, or by means of cables or solid copper or aluminium bars, depending on the currents and voltages to be switched.

Apart from the general specifications to be met, for example with regard to creepage and clearance distances, current density or heat dissipation, the short switching times within the nano to microsecond range call for a power design which also lives up to the requirements related to high-frequency applications. In this context, commutation circuits are of particular importance, because their parasitic inductive and capacitive characteristics have a crucial influence on the overall system behaviour.

5.4.1 Parasitic inductances and capacitances

To analyse the individual effects of parasitic inductances and capacitances and their interdependence in converters, it suffices to examine one commutation circuit.

Figure 5.4.1 shows the commutation circuit of an IGBT converter with parasitic elements, consisting of DC link voltage V_d (corresponds to commutation voltage V_K) and two IGBT switches with driver and antiparallel freewheeling diodes. The commutation voltage is impressed by the DC link capacitance C_d. The impressed current i_L flows out of the commutation circuit.

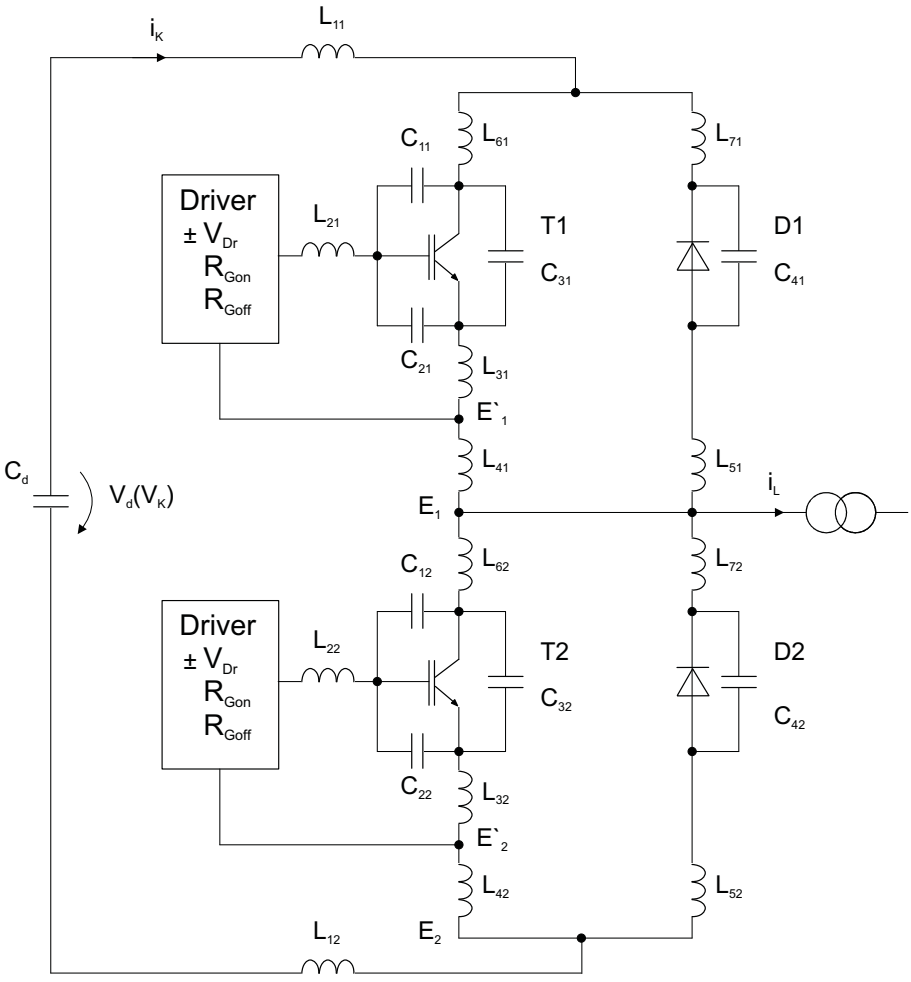


Figure 5.4.1 Commutation circuit with parasitic inductive and capacitive elements

The effects of parasitic elements/counter-measures

Total commutation circuit inductance

In the commutation circuit with T1 and D2, the sum of L_{11}, L_{61}, L_{31}, L_{41}, L_{72}, L_{52} and L_{12}. Similarly, the sum of L_{11}, L_{71}, L_{51}, L_{62}, L_{32}, L_{42} and L_{12} is effective in the commutation circuit with D1 and T2. During active turn-on of T1 or T2, the total commutation inductance becomes effective as turn-on relief, which will reduce turn-on power dissipation in T1 or T2 (cf. chapter 5.9).
However, during active turn-off of T1 and T2, as well as during reverse-recovery di/dt of D1 and D2, switching overvoltages are generated in the transistors and diodes due to high di/dt caused by the commutation circuit inductances. This increases turn-off power dissipation and voltage stress in the power semiconductors.
This effect is especially critical with regards to short circuits and overload (cf. chapter 5.7). Moreover, undesired high-frequency oscillations in the range of some MHz may be generated in connection with parasitic capacitances.
In hard-switching converters, it is therefore vital that inductances in the commutation circuit be reduced to a minimum. With the exception of L_{11} and L_{12}, all inductances are generated within the modules and cannot be influenced by the user. In this respect, it is up to the manufacturers of power modules to keep on working on the minimisation of internal inductances by improving module assembly technologies (cf. chapter 2.4.).

SEMIKRON datasheets indicate the internal inductances effective at the module output terminals (Example: SKM300GB12T4: L_{CE} = typ. 15 nH; Example: SEMiX252GB126HDs: L_{CE} = typ. 18 nH).

In the case of single-switch modules (1 IGBT/MOSFET + 1 inverse diode), the connection of both modules has to be as low-inductive as possible in a converter phase or commutation circuit.

Particularly important here is that the DC link busbars are low-inductive. This applies to the busbars between the DC link capacitors, as well as to the connection of the power modules to the DC link. In relation to this, laminated busbar systems (tightly parallelled plate systems) adapted to the specific converter layout have become widely accepted in practice, achieving busbar inductances of up to 20...50 nH.

The effect of the remaining inductances L_{11}+L_{12} on the power semiconductors can still be reduced by connecting C-, RC- or RCD-circuits directly to the DC link terminals of the power modules [AN1]. In most cases, a simple C-circuit with film capacitors within the range of 0.1...2 µF is connected. In low-voltage high-current applications, attenuated RC-circuits are preferred.

Emitter / source inductances

The elements L_{31} or L_{32} of the emitter / source inductances are effective in the power circuit, as well as in the driver circuit of the transistors. Due to the fast di/dt of the transistor current, voltages will be induced that will have the effect of inverse feedback in the driver circuit (emitter / source inverse feedback). This, however, will decelerate the charging process of the gate-emitter capacitance during turn-on or the discharging process of the gate-emitter capacitance during turn-off, resulting in increased switching times and switching losses. The inverse feedback effect of the emitter may be utilised to limit the collector current di/dt in the case of short circuits near the modules. To minimise the inductances L_{31} and L_{32}, power modules are equipped with separate emitter control terminals.

If several BOTTOM driver stages of a converter are supplied by a common operating voltage with negative DC link reference, the parasitic inductances between the ground connectors of the drivers and the negative potential of the DC link may cause undesired oscillations in the ground loops. This problem can be solved by way of HF stabilisation of the driver operating voltage near to the output stage or, in high-power converters, by way of separate supply voltage potentials for the BOTTOM driver stages.

Inductances L_{21} and L_{22}

The inductances L_{21} or L_{22} designate the inductance of the supply line between driver and transistor. Apart from increasing the impedance of the driver circuit, they may cause unwelcome oscil-

lations with the input capacitance of the transistor. This may be remedied by using a short, low-inductance connection between driver and transistor. Increasing the gate series resistance may dampen oscillations; this, however, will unintentionally cause an increase in transistor switching losses at the same time. For more details refer to [AN3].

Capacitances

The capacitances C_{xx} in Figure 5.4.1 stand for the intrinsic capacitances in the power semiconductors (voltage-dependent, non-linear) and cannot be influenced by the user. They indicate the minimum value for commutation capacitance C_K and, generally speaking, cause a reduction in power dissipation during turn-off (cf. chapter 1 and chapter 5.9.).
Additional power dissipation is generated during active turn-on due to the recharge process of the commutation capacitances; in high-frequency MOSFET applications (...>100 kHz...), in particular, these losses must be taken into account.
C_{11} and C_{12} result in the Miller effect, as well as dynamic dv/dt-feedback to the gate that slows down the switching process.
The circuit must be designed such as to prevent strong capacitive coupling between the inductive supply leads to gate and collector / drain as well as to gate and emitter / source outside the module, which is likely to cause additional high-frequency parasitic oscillations. This aspect is becoming increasingly important in fast high-voltage power MOSFET applications.

5.4.2 EMI and mains feedback

5.4.2.1 Energy processes in converters

The processes that take place in a converter system will always produce unwelcome interference due to the switching of the power semiconductors, on the one hand (Figure 5.4.2), and welcome energy transmission with corresponding signal processing, on the other hand.

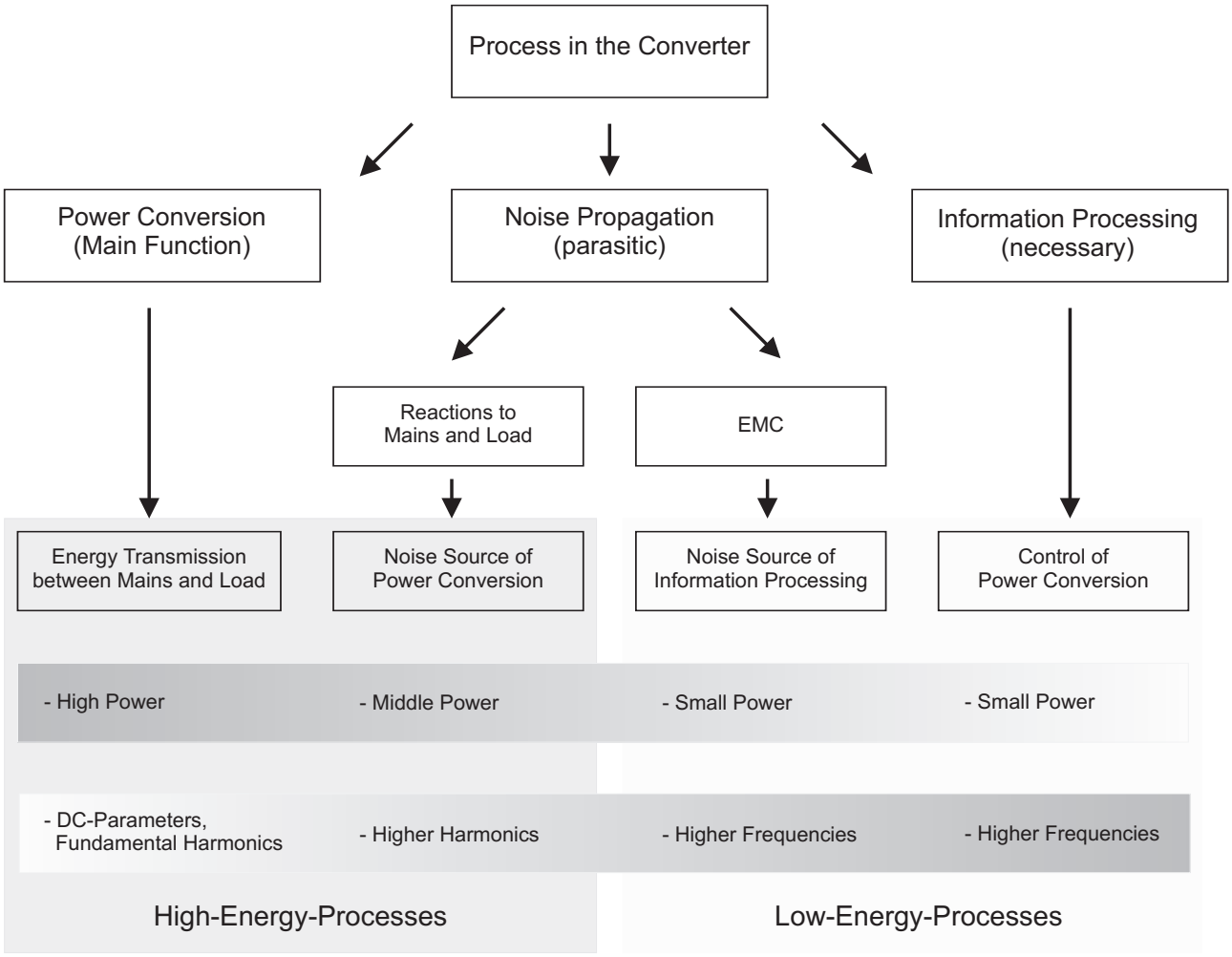


Figure 5.4.2 Energy processes in converters [60]

These processes can be divided up into high-energy processes, which may cause interference in the mains and the load within a frequency range between fundamental frequency and about 9 kHz, and low-energy-processes above 9 kHz up to about 30 MHz, where noise emission and, consequently, non-conducted current flow will start to be propagated. In the low-frequency range, these effects are called converter mains feedback, which are normally characterised by discrete harmonic current oscillations up to about 2 kHz. At higher frequencies, these oscillations are called radio interference voltages or radio interference and are given as interference voltage spectra in dB/mV for reasons of selective measurement. Terms such as zero current, leakage current or asymmetrical interference voltage only differ with respect to their assignment to different frequency ranges and with regards to the frequency dependency of the switching parameters. Since this frequency dependency is continuous, as is the transition to radio interference, the frequency transition range is inevitably very wide.

5.4.2.2 Causes of interference currents

Electromagnetic interference is caused mainly by the switching operation mode of power semiconductors. Causes of interference may be explained by the equivalent commutation circuit in Figure 5.4.3.

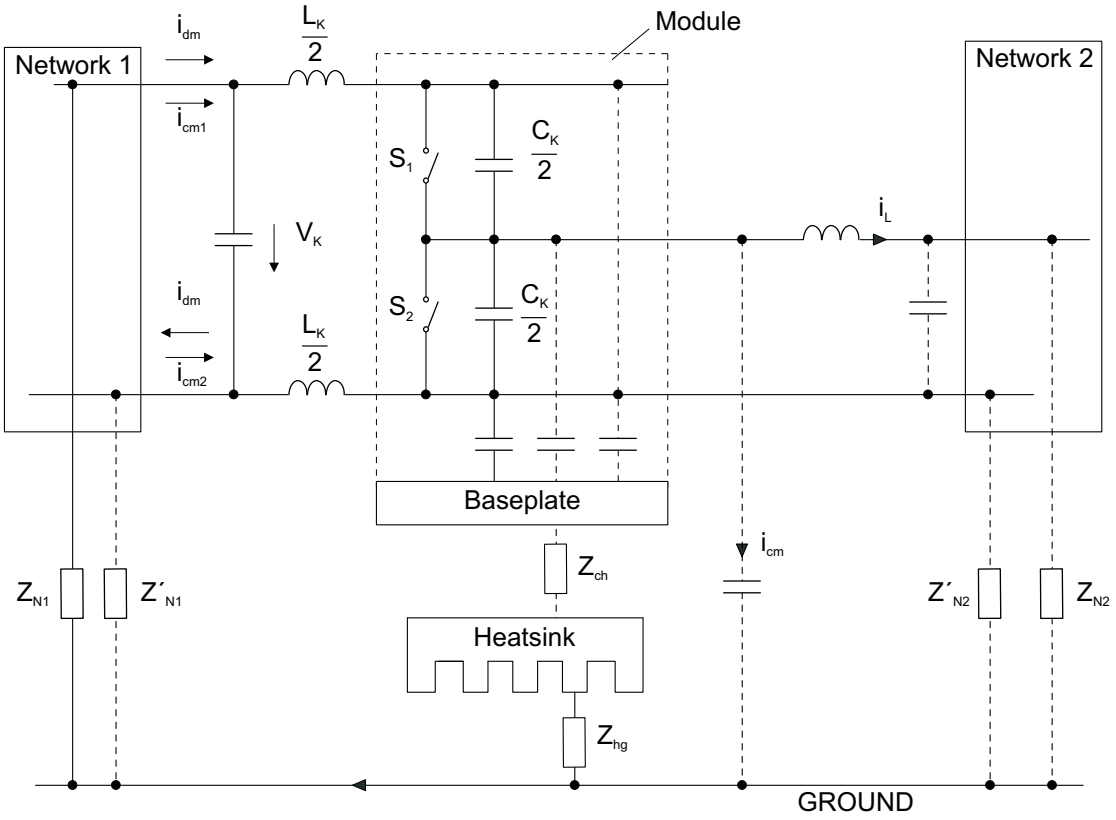


Figure 5.4.3 Equivalent commutation circuit with noise propagation paths [60]

In the case of inductive commutation, switch S1 will switch over to conducting switch S2. In a hard switching process ($L_K = L_{Kmin}$, $C_K = C_{Kmin}$), the current is initially commutated with a di/dt that is given by the semiconductor characteristics of switch 1. Commutation is finalised by the reverse-recovery di/dt of switch 2, which determines voltage commutation and, consequently, dv/dt along with the current-carrying inductance and the effective capacitances C_K. The effective capacitances comprise all capacitances C_Σ which are effective towards the neutral potential. In addition to the impedances of the commutation voltage connections to the neutral potential, parallel impedances of the commutation capacitances will become effective. At the beginning of the commutation process, the di/dt of switch 1 will cause a symmetrical current flow i_{dm} (differential mode) within the commutation voltage capacitance and the parallel network 1. The dv/dt at the end of the commutation process caused by the reverse-recovery di/dt of switch 2 and the inductance L, which serves as a supply current, conducts the currents i_{cm} (common mode) asymmetrically via the ground line through the parallel lines to the commutation capacitances C_K.
Transition to soft turn-on induced by an increase in L_K (ZCS, chapter 5.9) reduces the di/dt, thus minimising symmetrical current interference. At the same time, the increased inductances L_K are effective in the asymmetrical interference current circuit. At the beginning of the commutation process, dv/dt is determined by the switching characteristics of S1. The voltage leap at the end of the commutation process is determined by the reverse recovery current behaviour of switch S2. Transition to soft switching in ZCS mode reduces symmetrical current interference and changes the frequency range of asymmetrical currents, without reducing them considerably; also see chapter 5.9.

The capacitive commutation process is begun by active turn-off of switch S1.
In hard switching processes ($C_K = C_{Kmin}$), the asymmetrical interference current is determined by the impedances towards the neutral potential which are effective parallel to the commutation capacitances, and by the semiconductor characteristics of switch S1. The current commutation which is triggered after voltage commutation, and, consequently, the symmetrical interference current is determined by the turn-off behaviour of S1 and the turn-on behaviour of S2.

An increase in C_K calls for the use of a zero-voltage switch with soft turn-off behaviour (chapter 5.9). The turn-off process starts with the first stage of current commutation at a di/dt determined

by switch S1 at a reduced voltage. The delayed dv/dt will reduce the asymmetrical currents during voltage commutation. Passive turn-on of S2 determines the di/dt during the second stage of current commutation. Asymmetrical current interference will be reduced by soft switching in ZVS mode without changing symmetrical currents noticeably. Nevertheless, the increased capacitances C_K will diminish the symmetrical interference current in network 1 in relation to the capacitive current divider. Soft switching converter circuits (resonant, quasi-resonant) with turn-on or turn-off phase-shift control will reduce asymmetrical and symmetrical interference currents when using zero-voltage switches or zero-current switches. In converter circuits with auxiliary commutation arms, where ZVS and ZCS are switched alternately, interference currents will not be reduced considerably in comparison to hard switching circuits, since both high di/dt and dv/dt are involved in the total system within one switching cycle; see chapter 5.9.

5.4.2.3 Propagation paths

In order to detect conducted radio interference voltages, selective measurements of voltage fluctuations at the mains connections for inverter to ground are taken. The potential fluctuations refer to a defined point of ground, which is determined in standard measurements by connecting a line impedance stabilisation network. Regarding symmetrical and asymmetrical interference currents within the frequency range of EMI, all simple low-frequency switching elements are equipped with additional inductances, resistances and capacitances, which will render a clearer simulation of their frequency dependency.

Figure 5.4.4 shows an example of a simple step-down converter circuit, where network 1 is represented by the line impedance stabilisation network (LISN) and network 2 by the applied load in contrast to Figure 5.4.3.

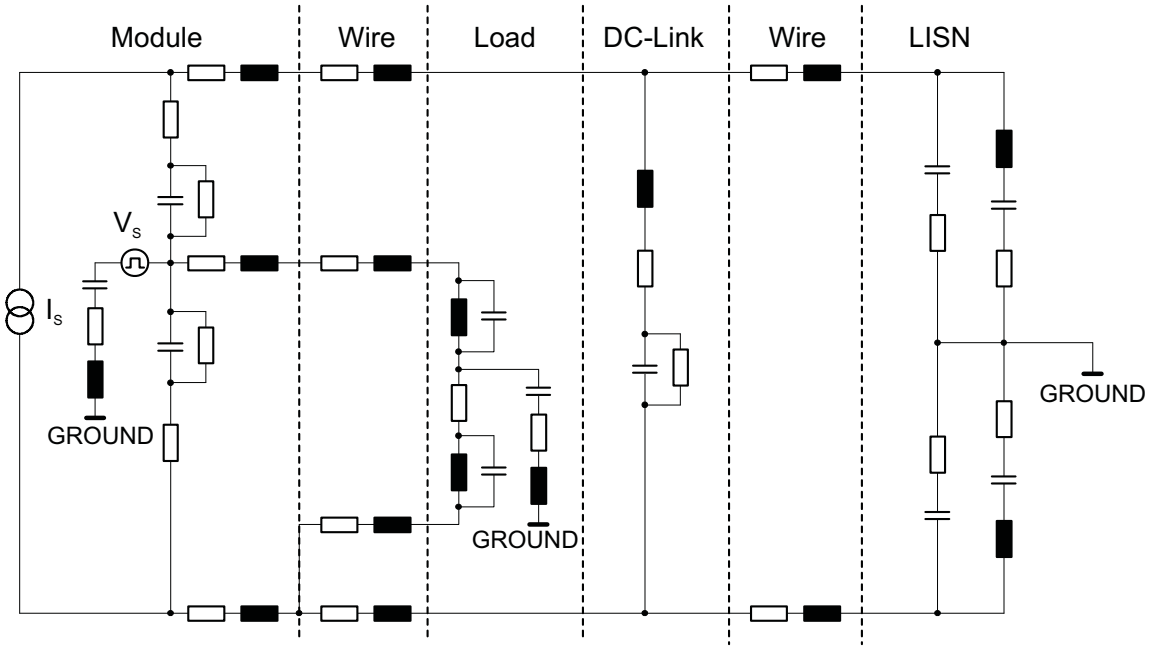


Figure 5.4.4 EMI equivalent circuit of a step-down converter [38]

The module simulates switches S1 and S2, including the commutation circuit inductances and capacitances. The aforementioned origins of interference currents are illustrated in a simplified way, namely as current source I_S for symmetrical interference currents and as voltage source V_S causing asymmetrical interference currents. In both sources, the measured semiconductor characteristics are included as a function of time (Figure 5.4.5).

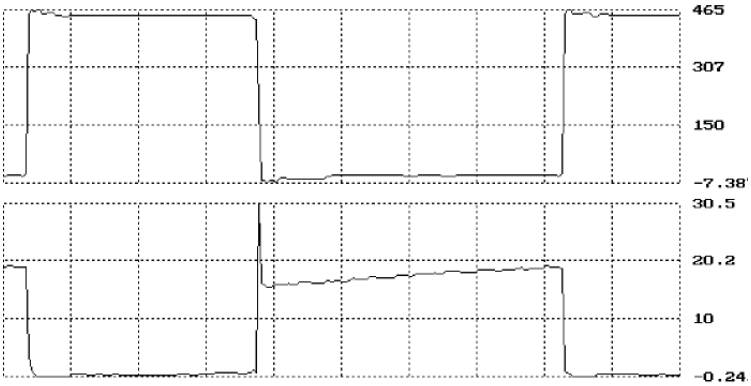


Figure 5.4.5 Typical voltage and current characteristics of an IGBT switch (top characteristic in V, bottom in A) [38]

Figure 5.4.6 shows simulated results with the example taken from [38] based on the model shown in Figure 5.4.4; these results concur largely with the actual measurements taken.

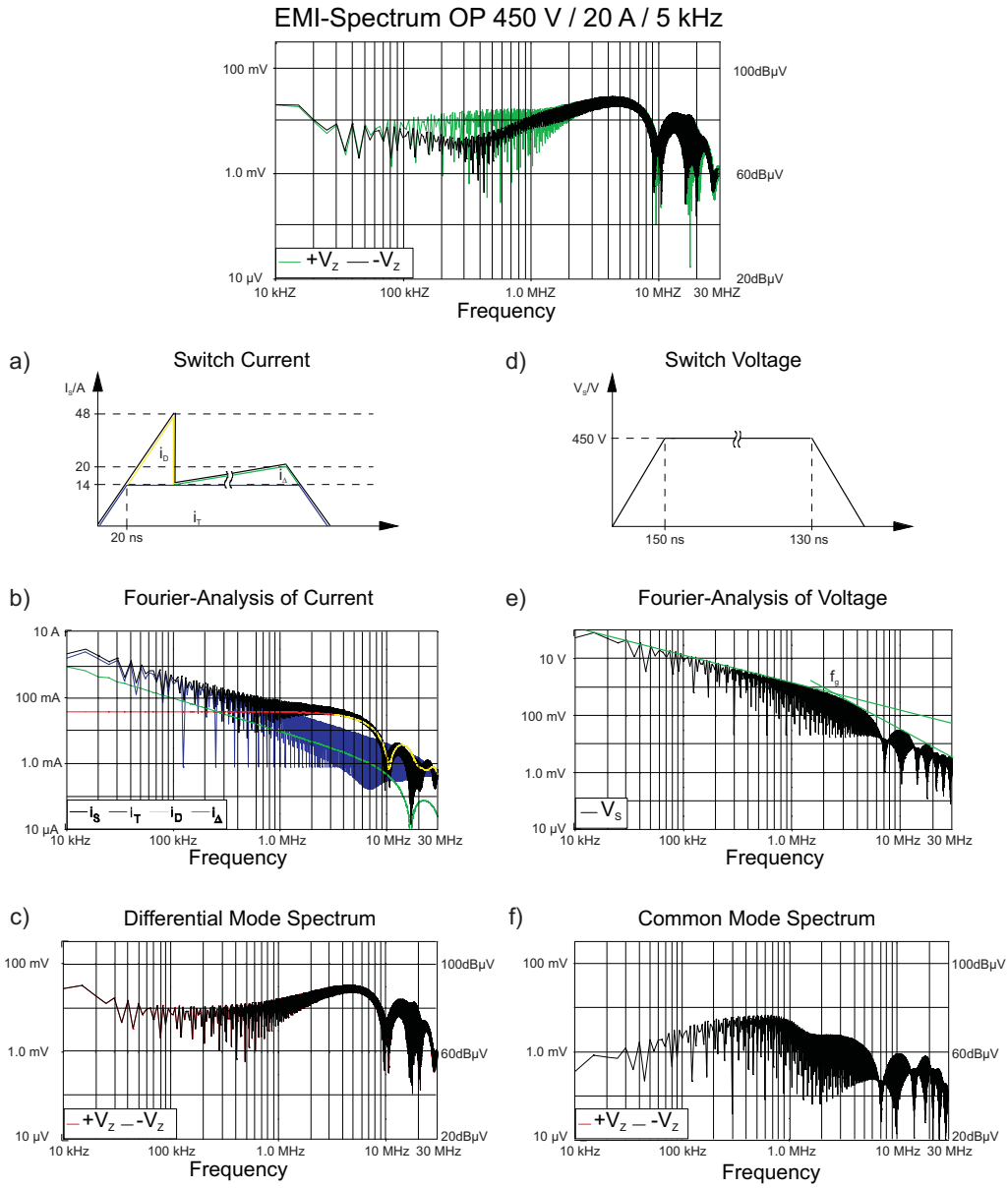


Figure 5.4.6 Simulation results for a 1200 V / 50 A NPT IGBT dual module
Operation parameters: DC link voltage V_Z = 450 V; Load current = 20 A
Pulse frequency = 5 kHz

The influence of additional propagation paths via energy and information transmission lines of the driver circuits were also examined in [60].

5.4.2.4 Other causes of electromagnetic interference (EMI)

The cyclic operating mode of power semiconductors with steep switching edges, as well as the current and voltage frequency shares involved here are discussed as one of the main causes of electromagnetic interference in chapter 5.4.2.2. This, however, by no means constitutes a detailed description of the the EMI behaviour of power electronic systems.
In [17], for example, further component-related oscillation effects are identified as reasons for electromagnetic interference beyond the circuit-related effects (parasitic frequencies in the range of 100 Hz - 30 MHz), which can be summarised as follows:

LC oscillations

(1) Oscillations that occur when switching individual power semiconductors (IGBT, MOSFET, diode)

Cause: excitation of resonant circuits consisting of the non-linear intrinsic semiconductor capacitances and the parasitic circuit environment (L,C)
Interference frequency range: 10 - 100 MHz
Counter-measure: circuit layout optimisation, reduction of switching speed, limitation by external circuits

(2) Oscillations in paralleled or series-connected IGBT / MOSFET or diode chips in modules or press-packs:
Cause: variations in parameter tolerances among the chips; asymmetries in the parallel / series circuit layout (also applicable to series or parallel connection of discrete components and modules)
Interference frequency range: 10 - 30 MHz
Counter-measure: circuit layout optimisation (balancing), use of suitable gate series resistors, chip optimisation, reduction of switching speed, limitation by external circuits

Oscillations during charge carrier transit time

(1) PETT oscillations (**P**lasma **E**xtraction **T**ransit **T**ime)
Cause: occur in the tail current phase of the turn-off process of bipolar components (IGBT, soft-recovery diode); the space charge zone collides with a pile of (free) charge carriers which form the tail current; PETT oscillations occur in the form of radiated electromagnetic interference frequency range: 200 - 800 MHz
Counter-measure: avoid LC circuits with resonant frequencies in the PETT oscillation range in the module design

(2) IMPATT oscillations (**Imp**act Ionisation (**A**valanche) **T**ransit **T**ime)
Cause: dynamic process during diode turn-off; the electrical field encounters the residual pile of (free) charge carriers; the diode changes dynamically to avalanche state (electron impact ionisation), IMPATT oscillations occur in the form high-energy radiated electromagnetic interference
Interference frequency range: 200 - 900 MHz
Counter-measure: optimisation of chip design

5.4.2.5 EMI suppression measures

Conventional conducted interference suppression is based on the use of customised filters or standard filter topologies which are attached to the mains and load side of the device. According to the set limit characteristics for a certain type of device or application (defined in terms of radiation and immunity by national and international standards for conducted and radiated EMI), various filters are used by means of line impedance stabilisation network and standardised test assemblies, until the limit values are complied with in all frequency ranges.

In this largely empirical approach, the filters are used are often both complex and costly. Whether the use of a simulation tool for optimising the overall EMC system layout makes sense or not, should be verified individually for each application, since model generation and the parameterisa-

tion processes involved are rather time-consuming. Basically, it is effective to design and construct a circuit that takes into account the effects of electromagnetic interference and the optimisation of propagation paths with respect to their origins and available measuring points at the beginning of the development processes already. Optimisation means either producing high-resistance propagation paths for interference currents by applying selective blocking circuits or creating low-resistance short circuit paths for interference currents by using selective suction filter circuits.
The selected measures are explained below with regard to Figure 5.4.3.

Symmetrical interference current circuits will be closed via the capacitance of the commutation voltage source. Ideal capacitance connected to switches 1 and 2 without the influence of any line impedances would be required for the creation of a short circuit path for interference currents. Measurable radio interference voltages will then be generated via the capacitive voltage ripple, effecting current flow over the parallel effective circuits. Therefore, all measures that may be taken to reduce symmetrical interference currents aim at the positioning of suitably connected suction filter circuits parallel to the connection lines of the commutation voltage. The closer the ideal capacitances (low intrinsic and ohmic inductance) and active suction filter circuits can be connected to the switch connection points, the less effort is involved for EMI suppression.

Essentially, asymmetrical interference currents are propagated via the ground line. In the context of interference suppression, extremely high-resistance impedances seem to be important at all switching points with steep potential increases versus ground potential, limiting the jumping potential to the non-avoidable switch connection points at the same time. In the example of the equivalent circuit in Figure 5.4.3, interference suppression was initially implemented by using reduced parasitic coupling capacitances of the potential-isolating components of the drivers and capacitances effective via the module base plate and the heatsink. If the drivers are not supplied with switching information or auxiliary energy by the neutral potential, displacement currents are not conducted via the earth line, i.e. the circuit is closed inside the device. There will be no flow of asymmetrical interference currents. Interference currents propagating across the base plate can be reduced by optimising the module layout and materials [38]. EMI suppression measures implemented close to the power semiconductor chips may considerably reduce interference currents, as shown in Figure 5.4.7 on the example of a modified IGBT module [38].

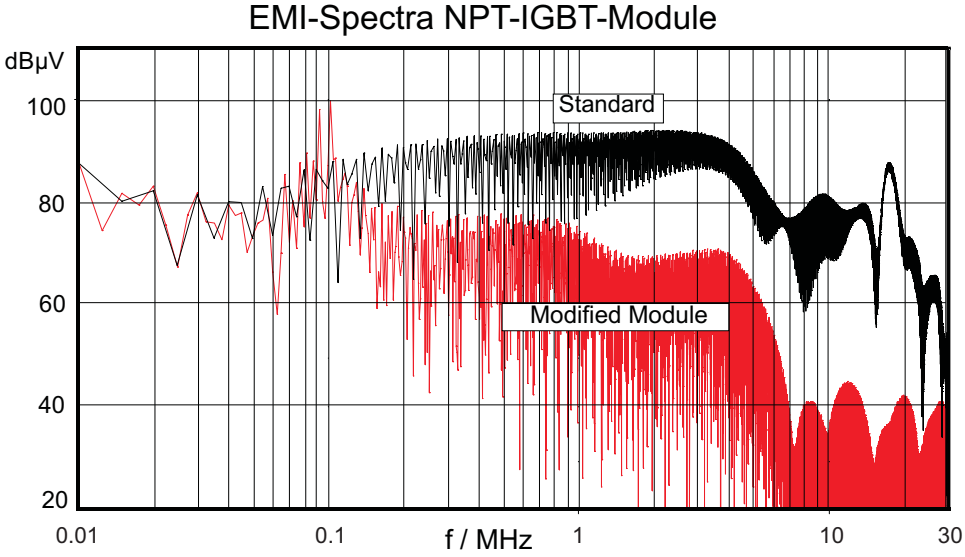


Figure 5.4.7 Interference spectra of a standard IGBT module compared to an EMI-optimised IGBT module [38];
Operation parameters: DC link voltage = 450 V; Load current = 20 A
Pulse frequency = 5 kHz

The connection to network 2 via the choke coil depicted in Figure 5.4.3 remains unaffected. A reduction in the coupling capacitance can only be achieved by reducing the connection line to a minimum. Ideally, an L/C filter should be connected directly to the the jumping potential: thanks

to the filter inductance, potential jumps are attenuated to such an extent that all other coupling capacitances in network 2 will be unable to noticeably contribute to the asymmetrical interference current. Should network 2 serve as the mains supply point where the LISN standard measurement takes place, this step is an absolute must, i.e. the L/C filter must be part of the EMI filter.

In addition to the use of EMI filters, additional measures with respect to earthing and shielding are performed in practice in order to improve EMI behaviour.

5.5 Solutions

5.5.1 Definition of the term "solutions"

The terms "solution“ and "SEMISTACK“ are used to designate fully assembled converter power sections such as

- line-commutated converter circuits, e.g. B2…B6U/HK/C/CF, W1…W3C, EU
- power output stages with IGBT modules, e.g. SEMITRANS, SEMiX, SKiM or SKiiP in customised circuit configurations, e.g. B2CI, B6CI, 2xB6CI, step-up and step-down converters as well as combinations thereof.

The functional design usually includes the power semiconductors interconnected in a chassis or case and mounted on heatsinks, the customer interfaces (control and power terminals) and, for IGBT stacks, DC link and snubber capacitors, as well as driver circuits and the necessary potential isolation features. Optionally, fans, temperature and current sensors, protective circuits and semiconductor fusing may be added. Each fully assembled solution undergoes final testing, documented with a test report in some cases.

5.5.2 Platforms

Cost-effective production of solutions is the key to creating competitive advantages for our customers. To achieve this goal, SEMIKRON has developed a number of platforms based on a modular design concept and the use of identical components where possible. This strategy is crucial in order to achieve short development and qualification times and make optimum use of competences. The high-volume effects for components bring about substantial cost advantages for series production as compared with customer-specific solutions, enabling short delivery times and an efficient spare part service at the same time. For this reason, platforms should always be kept in mind when implementing customer projects.

Existing SEMIKRON platforms:

Platform	Basic components		
	Power Semiconductors	**DC link**	**Cooling**
SEMIKUBE	SEMITRANS, SEMIPACK	Elyt or foil C	air*
SEMiXBOX	SEMiX	Elyt or foil C	air*
SKiiPSTACK	SKiiP	Elyt or foil C	air*, water
SEMISTACK Px120	SEMIPACK	-	air*
SEMISTACK P3	SEMIPACK	-	air**
SEMISTACK P16	SEMIPACK	-	air*
SEMISTACK Px308[x)]	SEMIPACK	-	air*
SEMISTACK P1	Threaded stud diodes/thyristors	-	air**
SEMISTACK P 17/18/19, N4	Capsule diodes/thyristors	-	air*
SEMISTACK P11, U3	Capsule diodes/thyristors		air***

x) Structure identical to SEMIKUBE
air*: forced air cooling
air**: forced or natural air cooling
air***: natural air cooling

Table 5.5.1 SEMIKRON platforms for solutions

The current Solutions/SEMISTACK product range for the most important platform products (including datasheets) can be found at www.semikron.com/products. Details on the type designation system and datasheet content is provided in the "Technical Explanations", likewise accessible online.

5.5.2.1 Platforms with IGBT standard modules

SEMIKUBE

SEMIKUBE B6CI is a flexible platform for 90...900 kW inverters in B2CI (half-bridge) or B6CI (three-phase inverter) configuration with an optional rectifier using standard 62-mm IGBT modules. Figure 5.5.1 shows the functions included and principle layout of a SEMIKUBE module.

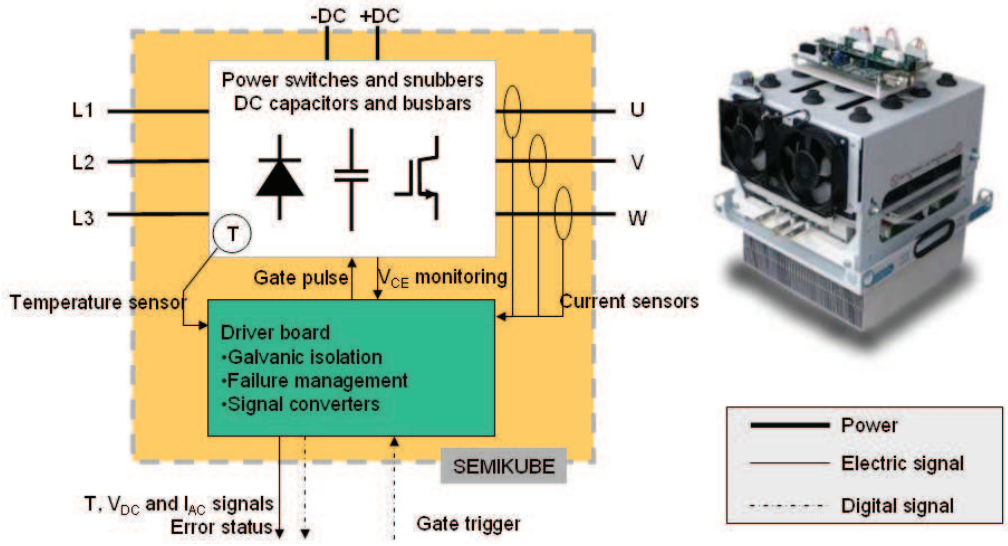
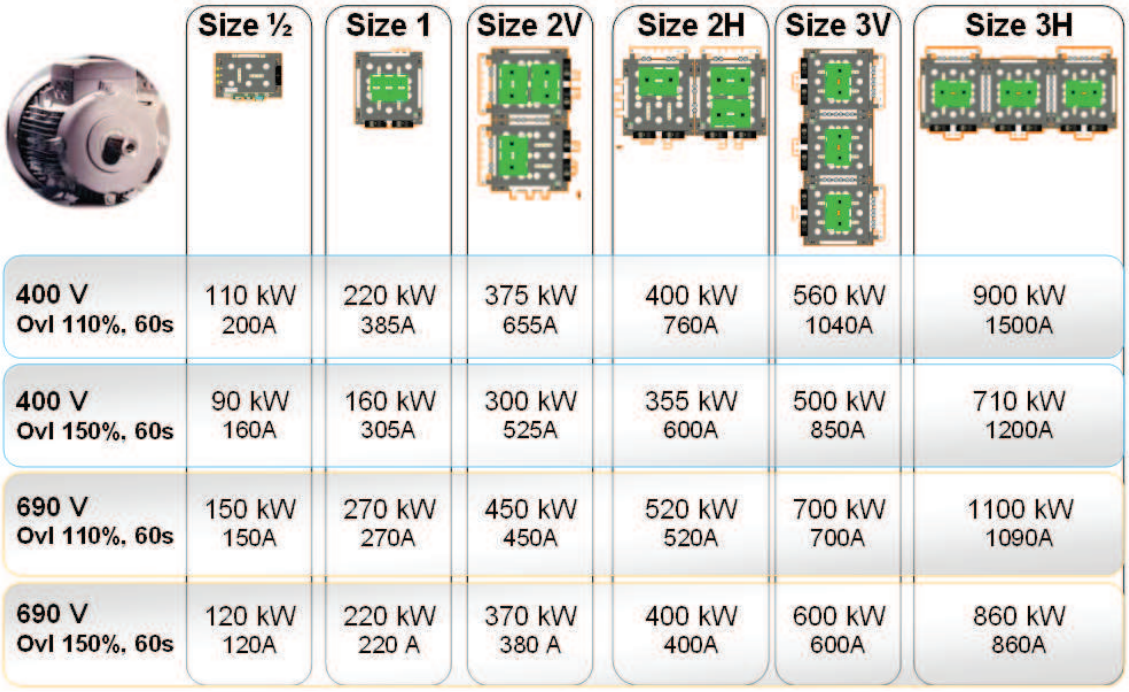


Figure 5.5.1 Functions and principle layout of a SEMIKUBE

The SEMIKUBE platforms shown are produced in either inverter, inverter / rectifier or inverter / bridge arm topology and may be configured for even more powerful inverters by varying interconnections (Figure 5.5.2).



	Size ½	Size 1	Size 2V	Size 2H	Size 3V	Size 3H
400 V Ovl 110%, 60s	110 kW 200A	220 kW 385A	375 kW 655A	400 kW 760A	560 kW 1040A	900 kW 1500A
400 V Ovl 150%, 60s	90 kW 160A	160 kW 305A	300 kW 525A	355 kW 600A	500 kW 850A	710 kW 1200A
690 V Ovl 110%, 60s	150 kW 150A	270 kW 270A	450 kW 450A	520 kW 520A	700 kW 700A	1100 kW 1090A
690 V Ovl 150%, 60s	120 kW 120A	220 kW 220 A	370 kW 380 A	400 kW 400A	600 kW 600A	860 kW 860A

Figure 5.5.2 SEMIKUBE modular system

Figure 5.5.3 shows SEMIKUBE1 and SEMIKUBE3H assemblies with optional radial fans.

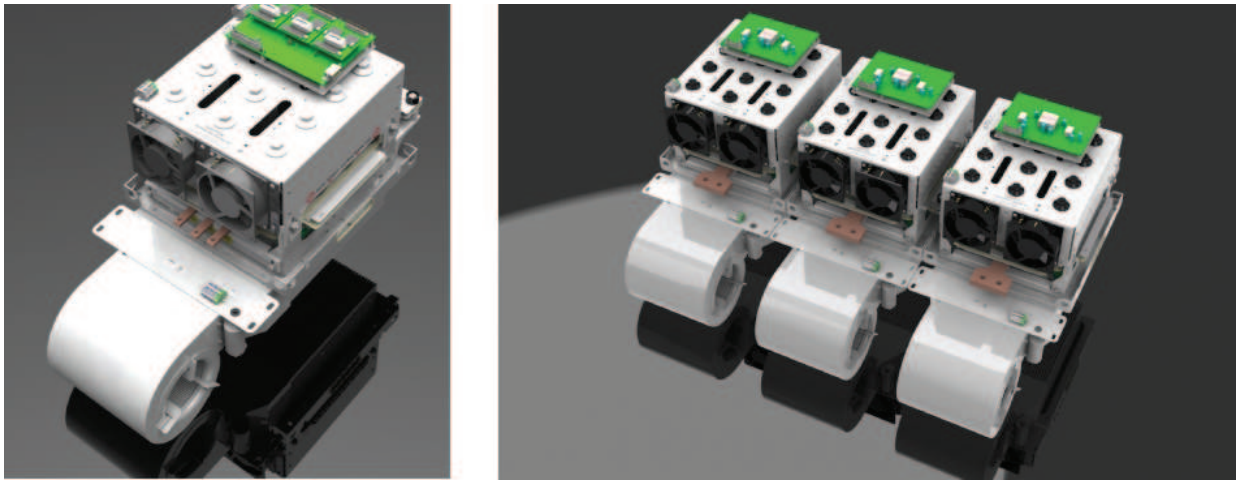


Figure 5.5.3 SEMIKUBE1 and SEMIKUBE3H with optional radial fans

Datasheets and detailed information on the application of SEMIKUBE platforms may be downloaded at www.semikron.com/products (e.g. [AN2].

SEMiXBOX

SEMiXBOX is a new platform product made by SEMIKRON based on SEMiX IGBT modules featuring converter power outputs of 10-90 kW with similar functions to SEMIKUBE.

Figure 5.5.4 shows the main dimensions and module integration options of the 2 different cell sizes (cell3, cell2). As the cells can be connected as desired and cooled using a common fan system, inverter bridges, rectifiers and chopper circuits can be implemented using SEMiX IGBT, thyristor and diode modules.

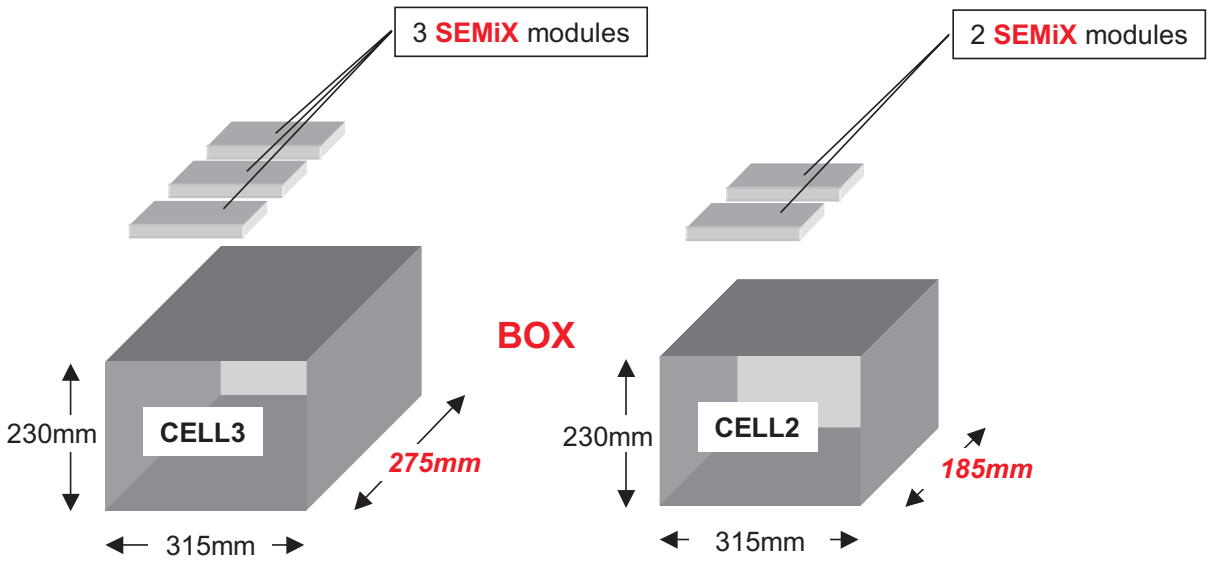


Figure 5.5.4 Main dimensions and module integration options for different SEMiXBOX cells

Motor ratings of approx. 51 kW for cell2 and 100 kW for cell3 can be achieved at a frequency of 50 Hz with modern SEMiX phase and full bridge modules, provided T_a = 40°C, V_N = 400 V, f_{sw} = 3 kHz, overload 150% / 60 s.

5.5.2.2 SKiiPSTACK platforms

The most powerful IGBT STACKs are based on SKiiP power modules and cover a power range of between 100 kW and approx. 1 MW. Connected in parallel, even higher powers can be achieved. 5.4.2.2 shows a standard SKiiPSTACK platform.

Figure 5.5.5 SKiiPSTACK (standard platform)

Predominantly for use in renewable energy applications such as wind power and photovoltaics, the standard SKiiPSTACK platform range is currently being further developed for grid-side voltage levels of 400 / 480 V (SKiiP 1200 V) and 690 V (SKiiP 1700 V). Compared to standard platforms, these power output stages, which are optimised for wind and solar power converters, result in cost reductions and more compact systems.

Both the air-cooled and water-cooled versions of the SKiiPSTACK platform use the same mechanical topology. Currently, SKiiP3 solutions cover the power output range 450 kW…2.5 MW (in parallel connection). The basic inverter unit configured in B6CI topology (three-phase inverter) used forced air or water cooling. Figure 5.5.6 shows a 4Q inverter consisting of 2 air-cooled basic units, suitable for integration into a standard 600 x 600 mm (w x d) cabinet.

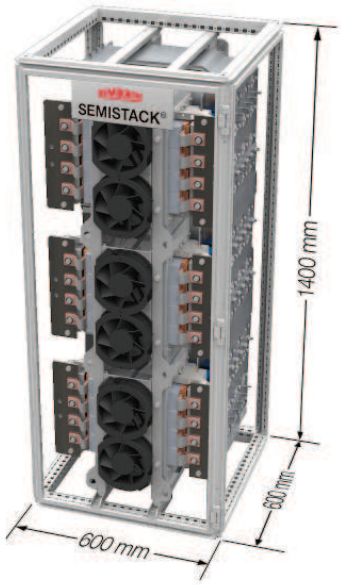
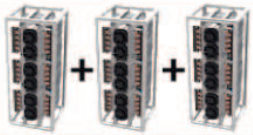
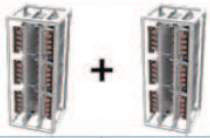


Figure 5.5.6 Air-cooled 4Q inverter

Equipped with four-fold SKiiP, the mounting height is 1400 mm, enabling the complete assembly to fit into a standard 2000 mm cabinet with sufficient space for other components, e.g. filter chokes. The basic units may also accommodate three-fold or two-fold SKiiPs. Based on the example of SKiiP3, Figure 5.5.7 shows the current and system output ratings achievable with different combinations of SKiiP components and parallelling.

		Air-cooled solution				Water-cooled solution			
Wind generator		1.5 MW		2.5 MW		1.5 MW		2.5 MW	
	DFIG Double-Fed Induction Generator								
		N° SKiiPs in //	I_{out} (A)	N° SKiiPs in //	I_{out} (A)	N° SKiiPs in //	I_{out} (A)	N° SKiiPs in //	I_{out} (A)
	Rectifier	1	600	2	1100	1	470	1	950
	Inverter	1	420	1	720	1	525	1	820
	SG Synchronous Generator								
	Rectifier	2	1440	3	2160	1	1350	2	2400
	Inverter	2	1500	3	2250	1	1350	2	2400
	T_a 40°C, T_w 40°C DFIG 1.5 overload 20 s, Inverter: 1100 V_{dc} / 690 V_{ac} / 2 kHz / 50 Hz / cos φ 1, Rectifier: 1100 V_{dc} / 690 V_{ac} / 2 kHz / 50 Hz / cos φ 0,95 f_{min} 3Hz								

		450 kW		900 kW		650 kW		1,3 MW	
Solar	Inverter								
		N° SKiiPs in //	I_{out} (A)	N° SKiiPs in //	I_{out} (A)	N° SKiiPs in //	I_{out} (A)	N° SKiiPs in //	I_{out} (A)
	1200 V SKiiP®	1	1100	2	2200	1	1350	2	2700
	1700 V SKiiP®	1	650	2	1300	1	950	2	1900
	T_a 40°C, T_w 40°C 3 kHz / 50 Hz / cos φ 1, 1200 V: 600 V_{dc} / 300 V_{ac} 1700 V: 1100 V_{dc} / 600 V_{ac}								

Figure 5.5.7 Current and power output ratings achievable with SKiiPSTACK platforms based on SKiiP3

5.5.2.3 Examples of platform solutions for line-commutated circuits using thyristors or diodes

Different platforms for thyristor and diode modules, as well as for threaded stud and capsule thyristors and diodes are available in combination with a variety of standard SEMIKRON heatsinks. The platforms are different in terms of power and heat dissipation properties (natural convection or forced-air cooling), the possibilities for using different component families, and in terms of geometry. Examples of these platforms are given in Figure 5.5.8.

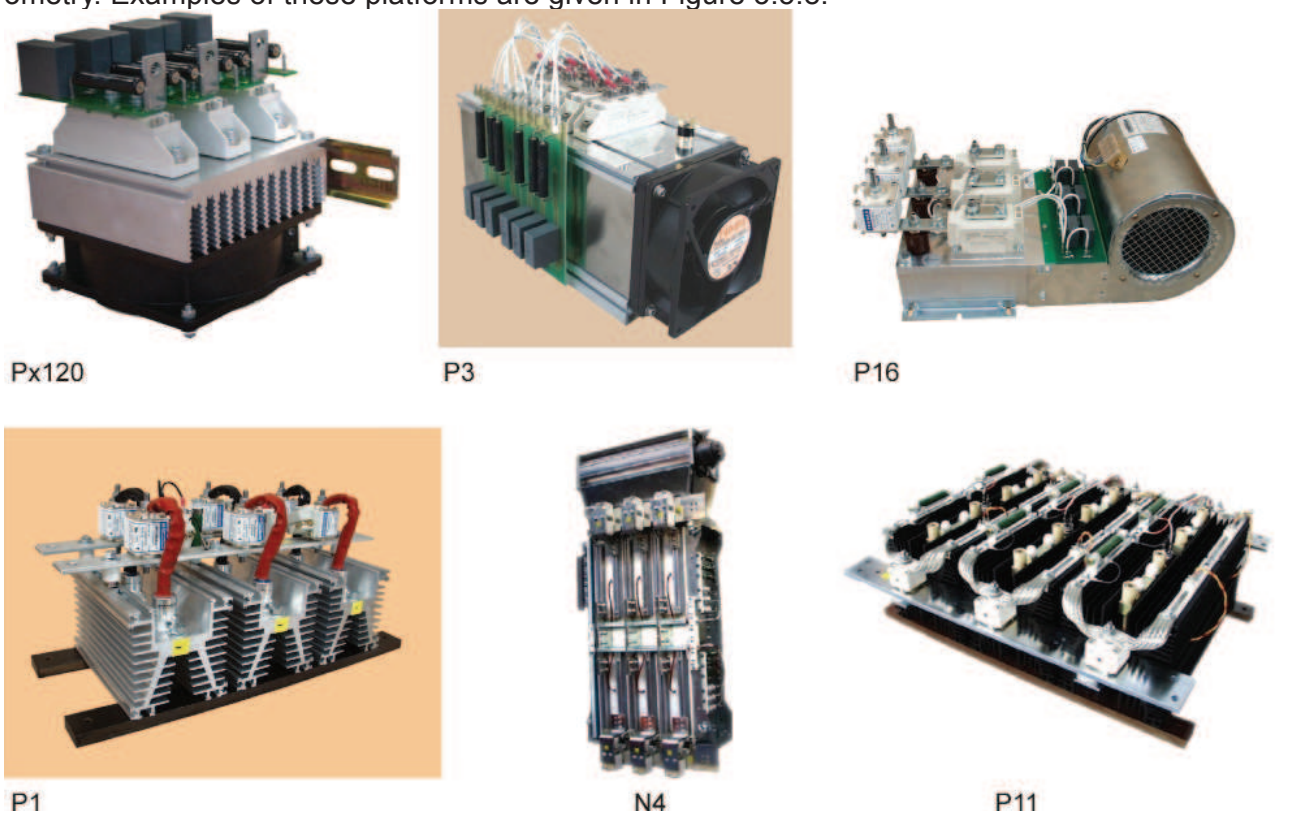


Figure 5.5.8 Examples of platforms for line-commutated circuits with thyristors and diodes

SEMISTACK datasheets and explanations on the code designation system for line-commutated circuits are detailed in the /SEMISTACK® DATASHEETS Basic Explanation Guide/ at www.semikron.com. A checklist for specifying the requirements of a platform solution can also be found here. The checklist includes the following technical aspects:

- Area of application, power flow direction(s), circuit structure, required functions
- Mounting dimensions (size, weight), other non-standard requirements (vibration, shock load, etc.)
- Input (mains, generator, battery,etc.), input voltage range, cos φ, specifics relating to mains feedback: fundamental frequency, pulse frequency, DC link voltage
- Output (mains, transformer, DC motor, AC motor, reluctance motor, etc.), output voltage range, output current, cos φ, overload (value/duration/frequency), fundamental frequency (min./max.), current at min. fundamental frequency, pulse frequency, load cycles (current, voltage, frequency, cos φ as a function of time)
- DC link (electrolytic or polypropylene capacitors), rated voltage, min./max. capacitance, max. DC link voltage, ambient DC link temperature
- Isolation test voltages, type of protection
- Driver, driver interface (transformer, optical), options (sensors for current, temperature, DC link voltage)
- Cooling: ambient temperature / coolant temperature min./max; for natural air cooling: max. air volume, permissible noise level
- For liquid cooling: cooling medium (antifreeze, volume, rate of flow)
- Storage temperature, other climate-related requirements, extreme assembly height above MSL
- Required module service life (power modules, DC link capacitors)

Furthermore, the simulation software SemiSel, which offers access to the key solutions and standard heatsinks, is provided on the SEMIKRON website as a tool for dimensioning platforms.

5.5.3 SKAI: System assemblies for vehicle applications

System assemblies offer an even higher level of integration compared to components and solutions, enabling the customer to control the system with his own software via an implemented controller or an integrated slot. SEMIKRON has developed a range of such module families in the form of power modules featuring assembly and packaging technology that has been tailored specifically to meet the requirements of automotive applications. One of these assembly families is called **SKAI** (**S**EMI**K**RON **A**dvanced **I**ntegration). The functions included here is given in Figure 5.5.9.

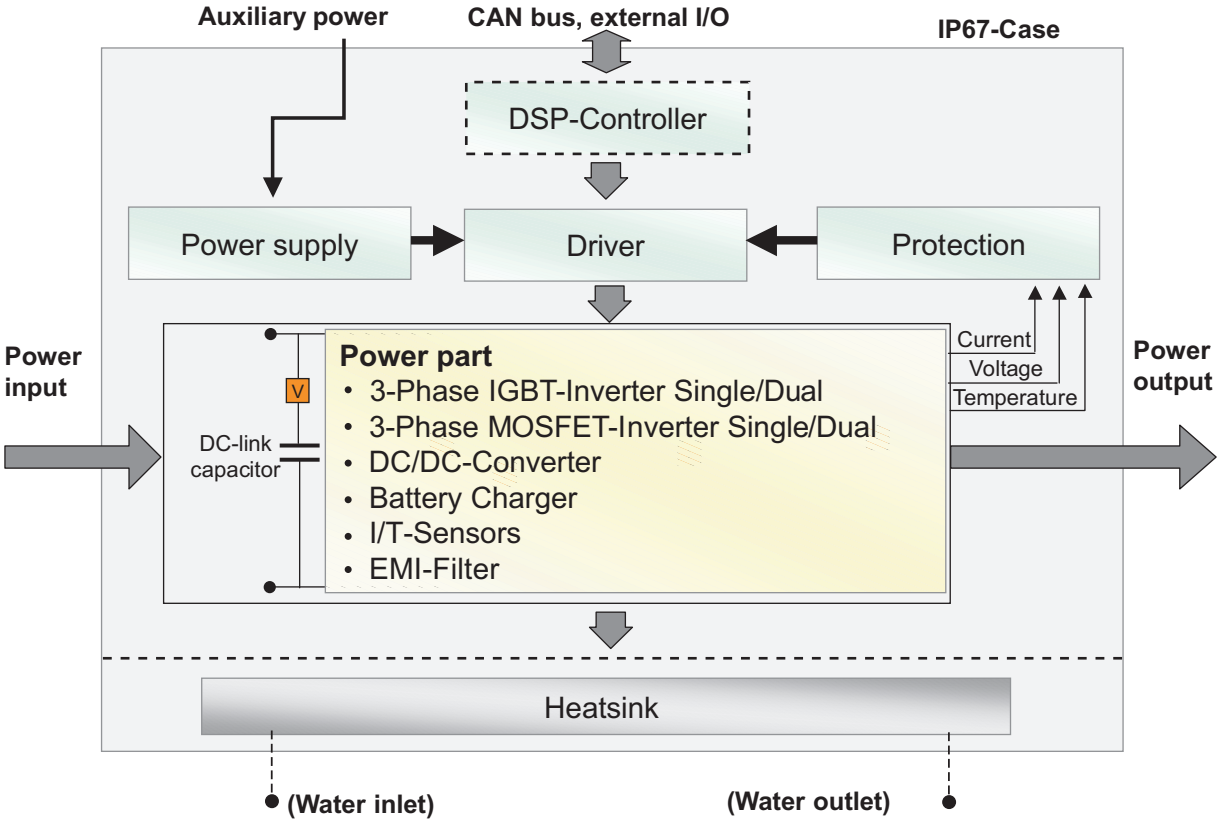


Figure 5.5.9 SKAI functions

High-voltage SKAI modules feature 600 V or 1200 V IGBT and are dimensioned for motor outputs of 100 kW or 150 kW. Low-voltage SKAI modules for power ratings in the range of some 10 kW work with power MOSFET. Thanks to their design, as well as assembly and packaging technology, SKAI vehicle power systems meet the multiple requirements of the broad automotive market, such as high temperature cycling capability, high vibration resistance, long service life and compact design. Figure 5.5.10 shows examples of the latest systems made by Semikron.

	MOSFET-System	IGBT - System	Multi-Converter Box
			
Application	Fork lifts, Electric vehicle	Full electric cars, Hybrid cars	Auxiliary drives for Industrial trucks
Typical output power	< 55kVA	< 250kVA	< 40kVA
DC-link voltage	24V - 160V	150V - 850V	450V - 850V
Topology	3-Phase Single/Dual-Inverter	3-Phase-Inverter	Active Front End, Inverter and DC/DC-Converter

Figure 5.5.10 Examples of SKAI systems

5.6 Driver

5.6.1 Gate current and gate voltage characteristics

Driving process

As already described in chapters 2.4.2.2 and 2.4.2.3, the switching behaviour of MOSFET and IGBT modules can be largely controlled by the gate capacitance recharge speed (i.e., in this case: gate capacitance = input capacitance C_{GE}+ C_{CG}).

In theoretical borderline cases, the gate capacitance recharge may be controlled by resistance, voltage or current (Figure 5.6.1).

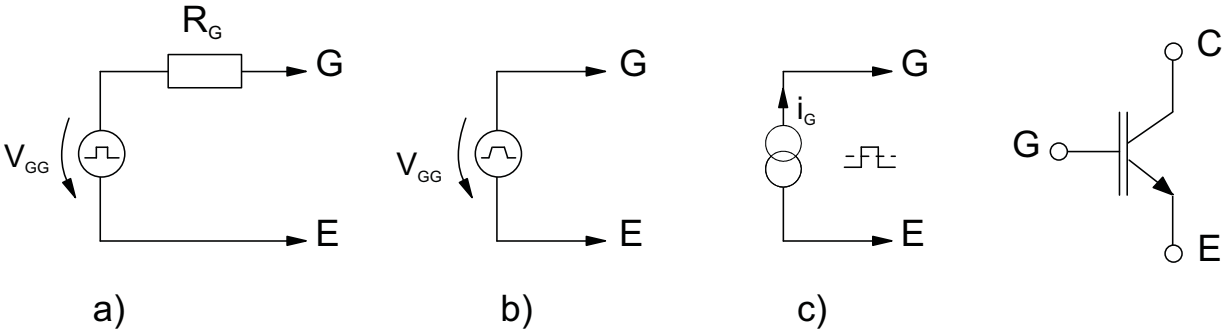


Figure 5.6.1 Gate driving process for IGBT [37] (MOSFET analogue)
a) Control by resistance, b) Control by voltage, c) Control by current

The most commonly used approach is to drive the system via a gate resistor (or two separate resistors for turn-on and turn-off) according to Figure 5.6.1a, since this is the most practical way of implementing the circuit. Characteristic here is the Miller plateau in the gate-source or gate-emitter voltage (Figure 5.6.2). Both switching speed and time are adjusted by R_G at a continuous supply voltage V_{GG}; the smaller the resistance R_G, the shorter the switching times. In applications using modern IGBT technologies (e.g. IGBT4), it may be observed within a defined range of the gate series resistance that, contrary to expectations, the di/dt during IGBT turn-off rises in line with the increasing R_G. This aspect must be considered when dimensioning the driver circuit (cf. [AN4]). The disadvantage of resistance-based control is that the gate capacitance tolerances of the MOSFET or IGBT will have a direct influence on switching times and switching losses; beyond that, the

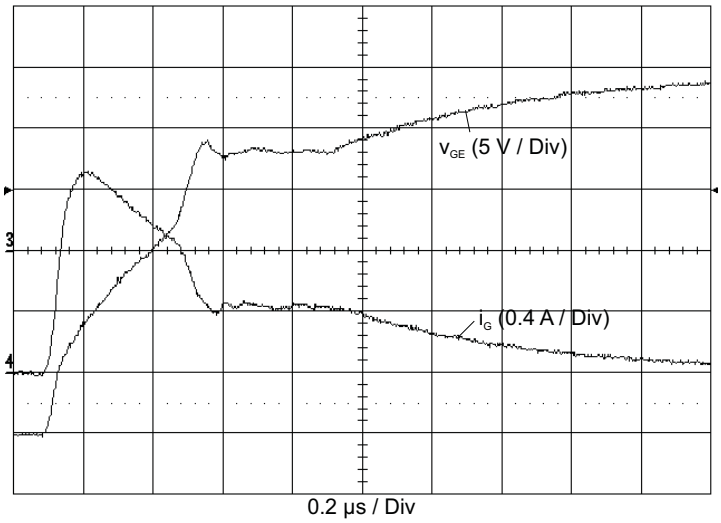
maximum values for the di/dt and du/dt during switching are not fully controllable in applications that use modern IGBT technologies.

Impressed voltage at the transistor gate driven according to Figure 5.6.1b will eliminate this influence; the switching speed of the transistor is directly determined by the defined impressed gate dv/dt. Thanks to this voltage, the gate voltage characteristic does not show a Miller plateau at all or, if so, it will be minimum only. This requires sufficient driver current and voltage capacity throughout the entire switching process. Driver topologies required for voltage-controlled circuits are definitely more complex and costly in comparison to resistance-based control. A possible compromise would be to combine resistance and voltage control, for example state-dependent switching of the gate series resistors, or dynamic gate control driver technologies.

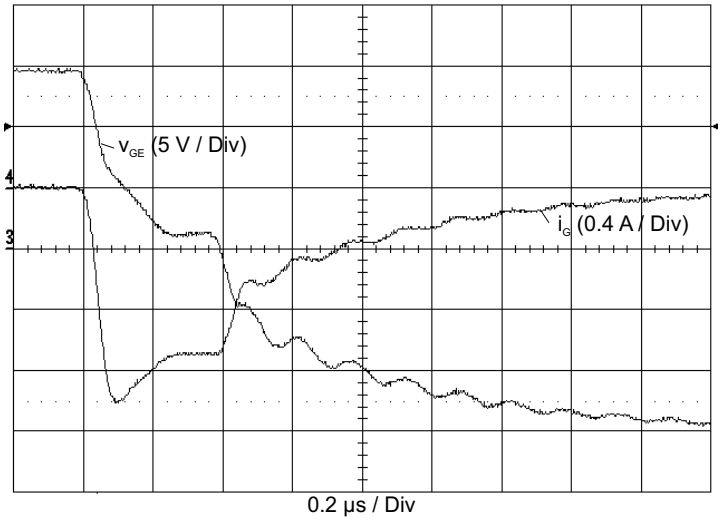
Current control using a "positive" and "negative" gate current generator, as shown in Figure 5.6.1c, determines the gate charge characteristics (cf. Figure 2.4.7) and is comparable to resistance control with respect to gate voltage characteristics. In practice, current control is also used for controlled, one-off slow turn-off due to overcurrent or short circuit.

Control voltage ratings

Figure 5.6.2 shows the characteristics for gate current i_G and gate-emitter voltage v_{GE} in a resistance-controlled circuit.



a)



b)

Figure 5.6.2 Gate current and voltage characteristics during turn-on and turn-off
a) Turn-on, b) Turn-off

The absolute maximum control voltage V_{GG} for both polarities must be dimensioned according to the electrical strength of the gate isolation; in datasheets, this value is usually specified at 20 V

for modern power MOSFET and IGBT. This value may not be exceeded - not even transiently; this may mean that additional measures have to be taken during turn-off; see chapter 5.6.2 and chapter 5.7.3.

On the other hand, $R_{DS(on)}$ and V_{CEsat} decrease as the gate voltage increases. It is therefore recommended that a positive control voltage is applied, delivering a gate voltage of

V_{GS} = +10 V for power MOSFET modules or
V_{GE} = +15 V for IGBT modules

during stationary on-state. Most datasheet ratings are based on these measurement parameters. For logic-level MOSFET a positive control voltage of +5 V is sufficient.

As demonstrated in Figure 5.6.2, the gate voltage for IGBT should be negative to the emitter potential during turn-off and OFF-state; the recommended values are -5...-8...-15 V.

Throughout the entire turn-off process (even if V_{GE} approaches $V_{GE(th)}$) this will maintain a negative gate current that is high enough to result in short switching times.

Another, more serious disadvantage of blocking the IGBT of a bridge circuit with V_{GE} = 0 V will occur during the reverse-recovery of the parallel inverse diode of the transistor that has been turned off because of the dv_{CE}/dt (Figure 5.6.3).

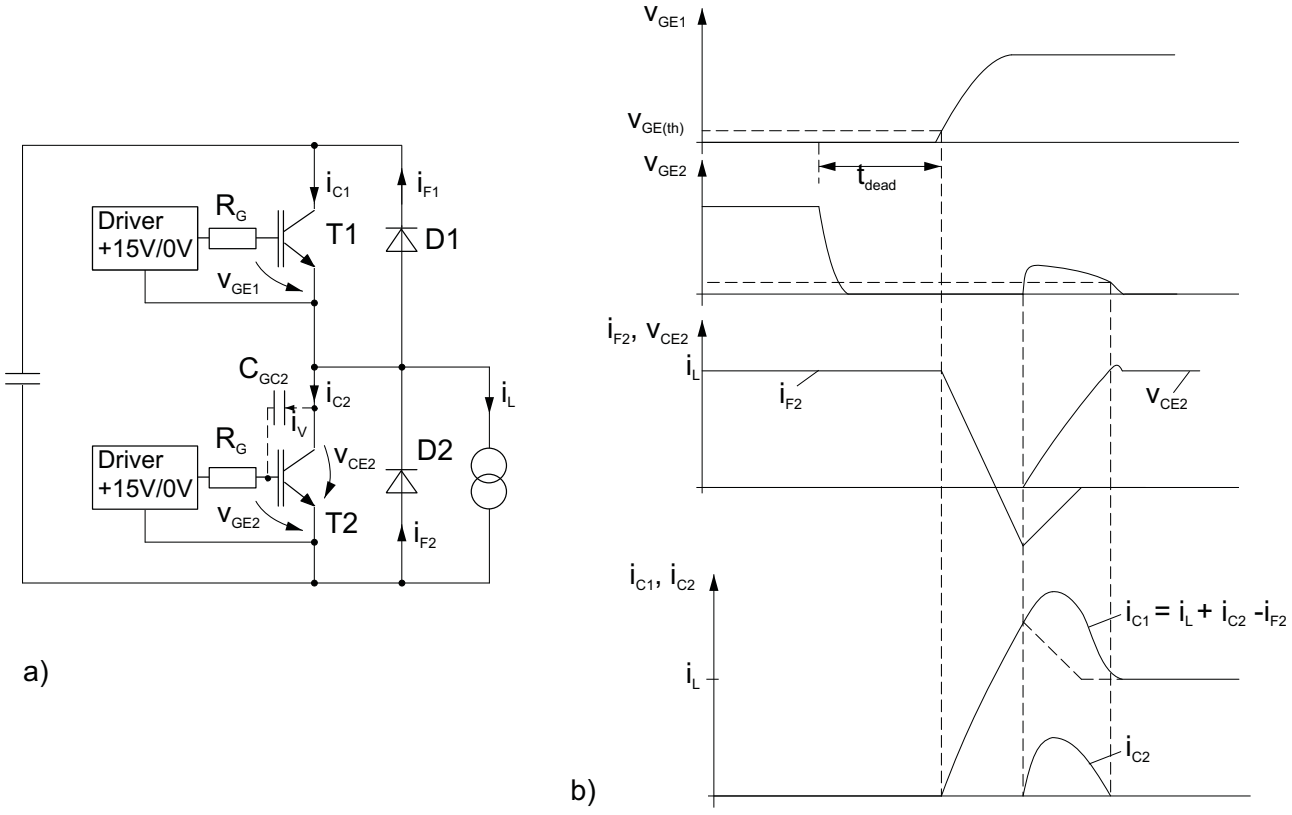


Figure 5.6.3 Cross current in an IGBT bridge arm due to turn-on by dv_{CE}/dt feedback of T2
a) Circuit diagram, b) Current and voltage characteristics

The high dv_{CE}/dt of the collector-emitter voltage v_{CE2} during the reverse-recovery di/dt of D_2 will effect a displacement current i_V through the gate-collector capacitance C_{GC2}, cf. chapter 2.4.2.2.

$i_V = C_{GC} \cdot dv_{CE}/dt$,

This displacement current will cause a voltage drop across the resistance R_G (or $R_{GE/RG}$). If this causes v_{GE} to rise and exceed the threshold voltage $V_{GE(th)}$, T2 will be driven to its active region during the reverse-recovery di/dt (cross current, additional power dissipation in T1 and T2).

Other than with IGBT, the application of a static negative gate-source voltage during off-state is not recommended to drive power MOSFET. Parasitic turn-on with all of the consequences described above happens within the MOSFET too; at the same time, however, it will protect the transistor /

diode structure of the MOSFET, whose dv/dt resistance is limited. The equivalent circuit of a power MOSFET (Figure 2.4.16) demonstrates the displacement current through C_{DS} to the base of the parasitic npn-bipolar transistor as a result of dv_{DS}/dt. If the voltage drop at the lateral p-well resistor R_W reaches threshold voltage level, the bipolar transistor will be turned on parasitically, which may lead to destruction of the MOSFET as a result of power dissipation during periodic operation.

Parasitic turn-on of the MOSFET channel at V_{GS} = 0 V over C_{GD} will reduce dv_{DS}/dt during blocking state and will weaken the unwelcome effect of bipolar transistor turn-on (cf. Figure 5.6.3).

Furthermore, parasitic turn-on of the MOSFET channel will reduce dv/dt at the moment of the body diode's turn-off during reverse recovery, thus avoiding failure of the diode as a consequence of its restricted dynamic ruggedness.

In field applications, MOSFET driver circuits are known which switch towards 0 V during the body diode's commutation process and apply a negative gate voltage during static off-state of the switch.

Control current ratings, driving power

The total driving power P_{Gavg} to be delivered by the driver circuit can be determined from the gate charge Q_{Gtot} (cf. Figure 2.4.7):

$$P_{Gavg} = \left(V_{GG+} + \left|V_{GG-}\right|\right) \cdot Q_{Gtot} \cdot f_s \qquad \text{where } Q_{Gtot} = C_{ERSATZ} \cdot \left(V_{GG+} + \left|V_{GG-}\right|\right)$$

Peak gate current values are calculated as follows:

$$I_{GMon} = \left(V_{GG+} + \left|V_{GG-}\right|\right) / R_{Gon} \qquad \text{(ideal)}$$

$$I_{GMoff} = \left(V_{GG+} + \left|V_{GG-}\right|\right) / R_{Goff} \qquad \text{(ideal)}$$

The ideal calculation method neither considers the internal resistance effective in the driver output stage, nor does it take account of the dynamically effective wave impedance resulting from the driver circuit inductance and input capacitance of the IGBT / MOSFET. The smaller the external gate series resistance, the bigger the difference between ideal and real gate peak current.

Driver power per channel is calculated as follows:

$$P\left(V_{GG+}\right) = V_{GG+} \cdot Q_{Gtot} \cdot f_s \qquad f_s \text{ = switching frequency}$$

$$P\left(V_{GG-}\right) = \left|V_{GG-}\right| \cdot Q_{Gtot} \cdot f_s$$

Example: V_{GG+} = 15 V, V_{GG-} = -15 V, R_{Gint} = 2.5 Ω, $R_{Gon} = R_{Goff}$ = 1.5 Ω
Q_{Gtot} = 2.4 µC (SKM300GB12E4)
f_s = 10 kHz, V_{DC} = 600 V

Resulting in:

$$I_{GMon} = \left|I_{GMoff}\right| = 7{,}5\ \text{A} \qquad \text{(ideal)}$$

$$P_{Gav} = 0{,}72\ \text{W}$$

$$P(V_{GG+}) = P(V_{GG-}) = 0{,}36\ \text{W}$$

$$I(V_{GG+}) = I(V_{GG-}) = 24\ \text{mA} \qquad \text{(average)}$$

5.6.2 Driver parameters and switching properties

As mentioned, important features of driven power MOSFET or IGBT are dependent on V_{GG+}, V_{GG-} and R_G ratings. The table below provides an initial overview of these(<: increases, >: decreases, -: remains unaffected):

Rating/ characteristic	V_{GG+} <	$\|V_{GG-}\|$ <	R_G <
$R_{DS(on)}$, V_{CEsat}	>	-	-
t_{on}	>	<	<
E_{on}	>	-	<
t_{off}	<	>	<
E_{off}	-	>	<
Transistor turn-on peak current*)	<	-	>
Diode turn-off peak current*)	<	-	>
Transistor turn-off peak voltage*)	-	<	>
di/dt	<	<	>**)
dv/dt	<	<	>
Actively limited I_D, I_C	<	-	-
Ruggedness towards load short circuit	>	-	<

*) during hard switching under ohmic-inductive load
**) not constant throughout the R_G spectrum during turn-off

Forward characteristics ($R_{DS(on)}$, V_{CEsat})

The dependencies of the power MOSFET and IGBT forward characteristics on the drive parameters can be derived from their output characteristics (cf. chapters 2.4.2.1 and 2.4.2.3). In Figure 5.6.4 this is explained by way of an example each for SEMITRANS MOSFET and IGBT modules using the data given in the datasheets.

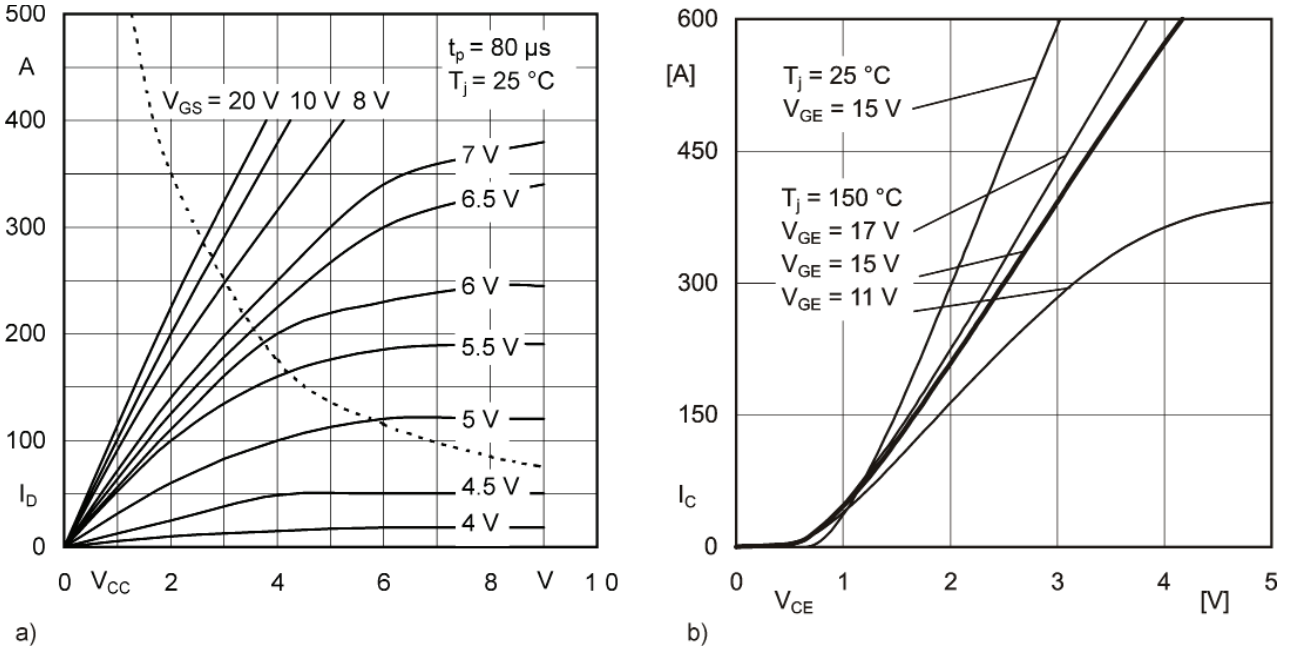


Figure 5.6.4 Forward characteristics versus control voltage V_{GG+}
a) Power MOSFET module b) IGBT module

In SEMIKRON power module datasheets, the recommended maximum ratings and characteristic values mentioned in chapter 5.6.1 are indicated with V_{GG+} = 10 V for power MOSFET modules and

V_{GG+} = 15 V for IGBT modules, which is an acceptable compromise in conventional applications between power dissipation, turn-on peak current and short circuit behaviour.

Switching times, energy dissipation (t_{on}, t_{off}, E_{on}, E_{off})

Control voltages and gate resistances affect the various components of turn-on time $t_{on} = t_{d(on)} + t_r$, turn-off time $t_{off} = t_{d(off)} + t_f$ and tail time t_t of the IGBT.

Due to the gate capacitance amounting to absolute ratings of V_{GG+} and V_{GG-} before switching, the recharge time between switching will decrease (turn-on delay time $t_{d(on)}$, turn-off delay time $t_{d(off)}$) in proportion to the decreasing gate series resistance.

On the other hand, switching times t_r and t_f, consequently, a large part of the switching losses E_{on} and E_{off} are greatly affected by the switching control voltages V_{GG+} or V_{GG-} and the gate resistor R_G.

IGBT datasheets include diagrams showing the dependencies of switching times and energy dissipation on R_G; in most cases given for rated current values and on condition of hard switching under ohmic-inductive load (Figure 5.6.5).

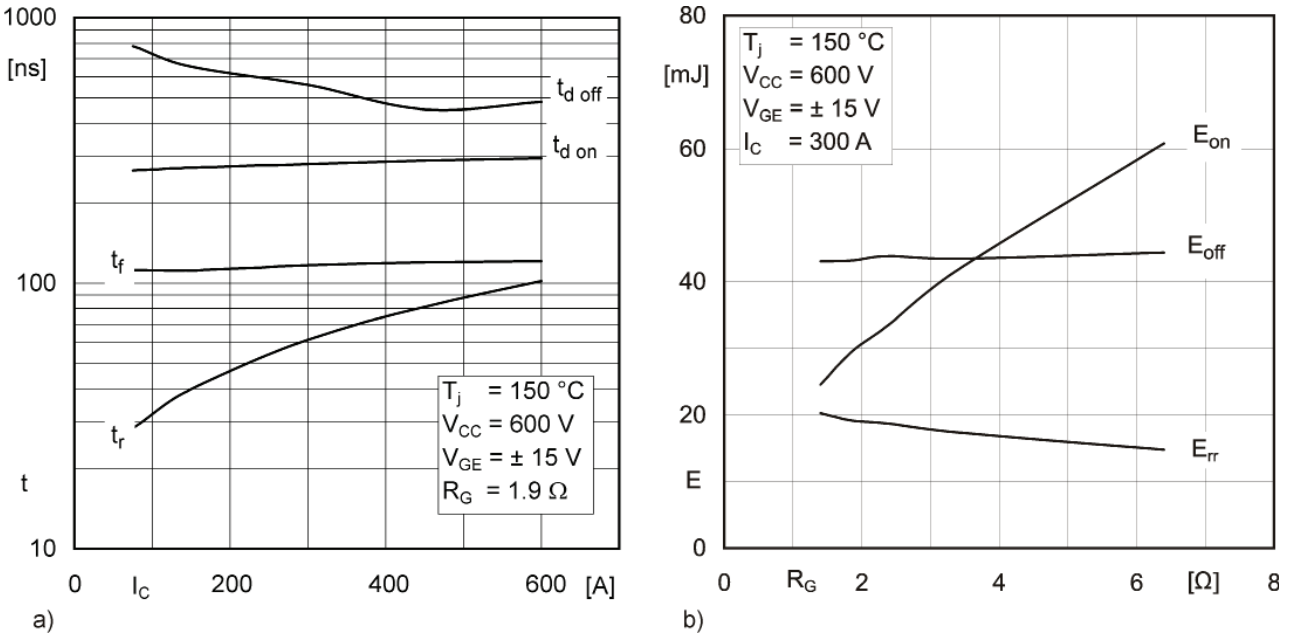


Figure 5.6.5 IGBT switching times (a) and switching losses (b) versus gate series resistance R_G; here at T_j = 125°C, V_{CE} = 600 V, I_C = 75 A, V_{GE} = ± 15 V and on condition of hard switching under ohmic-inductive load

Dynamic turn-off behaviour of the free-wheeling diode (reverse recovery) and turn-on peak current of the transistor

The IGBT turn-on losses indicated in Figure 5.6.5b already includes the influence of the turn-off behaviour of the integrated free-wheeling diode on turn-on peak current and turn-on losses; see chapters 2.3.3.2 and 3.3.3.

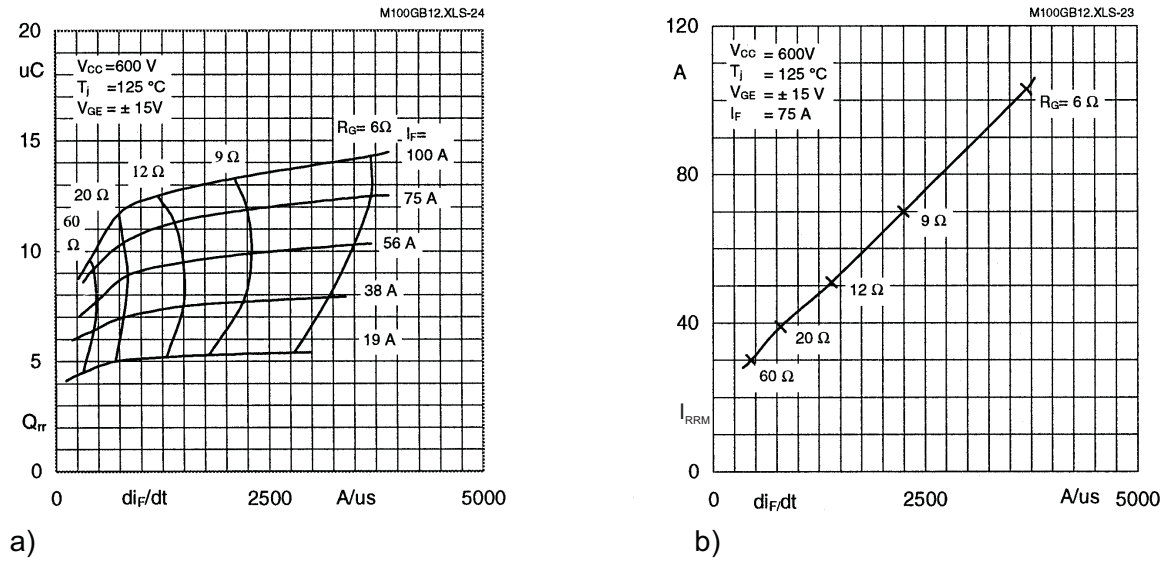


Figure 5.6.6 Recovered charge Q_{rr} (a) and peak reverse recovery current I_{RRM} (b) of the free-wheeling diodes in an IGBT module (e.g. SKM100GB123D) versus commutation speed $-di_F/dt$ of the diode current

The drain or collector current (i_D, i_C) rise time t_r will decrease as the gate current rises (higher V_{GG+} or smaller R_G). This in turn will increase the current commutation speed $-di_F/dt$ in the free-wheeling diode which the recovered charge Q_{rr} and peak reverse recovery current I_{RRM} depend on.

These dependencies are depicted in the datasheets for the fast free-wheeling diodes used in IGBT modules (Figure 5.6.6 and Figure 5.6.7).

An increase in Q_{rr} and I_{RRM} will cause higher turn-off losses in the internal free-wheeling diode.

Since a higher $-di_F/dt$ results in a higher Q_{rr} and I_{RRM} and, since the load current is increased by I_{RRM} within the collector or drain current, the turn-on peak current and turn-on switching losses of the transistor will increase in line with its turn-on speed (Figure 5.6.5).

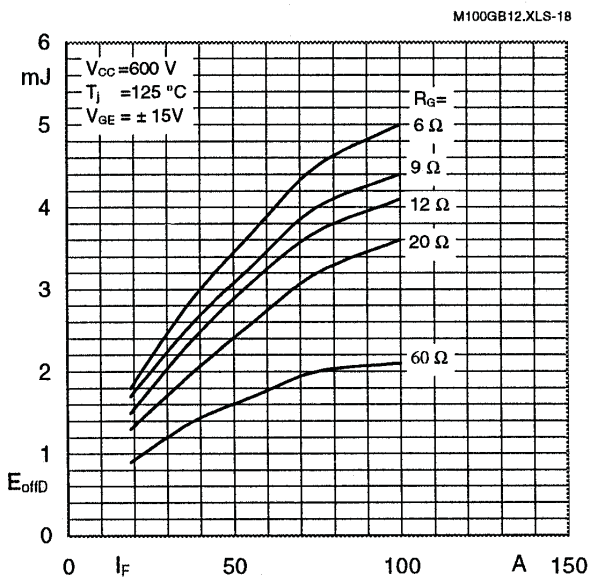


Figure 5.6.7 Free-wheeling diode turn-off losses E_{offD} versus R_G of the transistor during turn-on

Turn-off peak voltage

If V_{GG-} increases or R_G decreases, the turn-off gate current of the transistor being turned on will rise. As shown in Figure 5.6.5a, the drain or collector-current fall time t_f decreases, i.e. $-di_D/dt$ or

$-di_C/dt$ increases. The voltage $\Delta u = -L_\sigma \cdot di/dt$ induced during di/dt over the parasitic commutation circuit inductance L_σ increases in proportion to di/dt.

Further technical information on the dimensioning of IGBT drivers and gate resistance is provided in [AN3], [AN5], [AN6].

5.6.3 Driver circuit structures

Figure 5.6.8 shows the basic structure of a high-performance driver circuit for a MOSFET or IGBT bridge arm which, in addition to the basic gate driver function, includes TOP / BOTTOM interlock, protection and monitoring functions, as well as pulse shapers.

The driver depicted features TOP and BOTTOM switches of the central logic and control units (microprocessor, DSP, FPGA) separated by potential isolation for control signals, driving energy, as well as state and error feedback signals. In less complex driver circuits such as used in low-cost applications, these potential isolations may either be combined (common energy and signal transmission) or have no electrical isolation (e.g. bootstrap circuits for TOP voltage supply; level shifter for signal transmission to the TOP switch). Low-voltage switches, especially those used in applications with low converter voltages or low-side choppers (only BOTTOM switch is active), require a very simple driver structure only, since individual driver functions can be easily implemented or even dispensed with (e.g. interlock and dead-time functions).

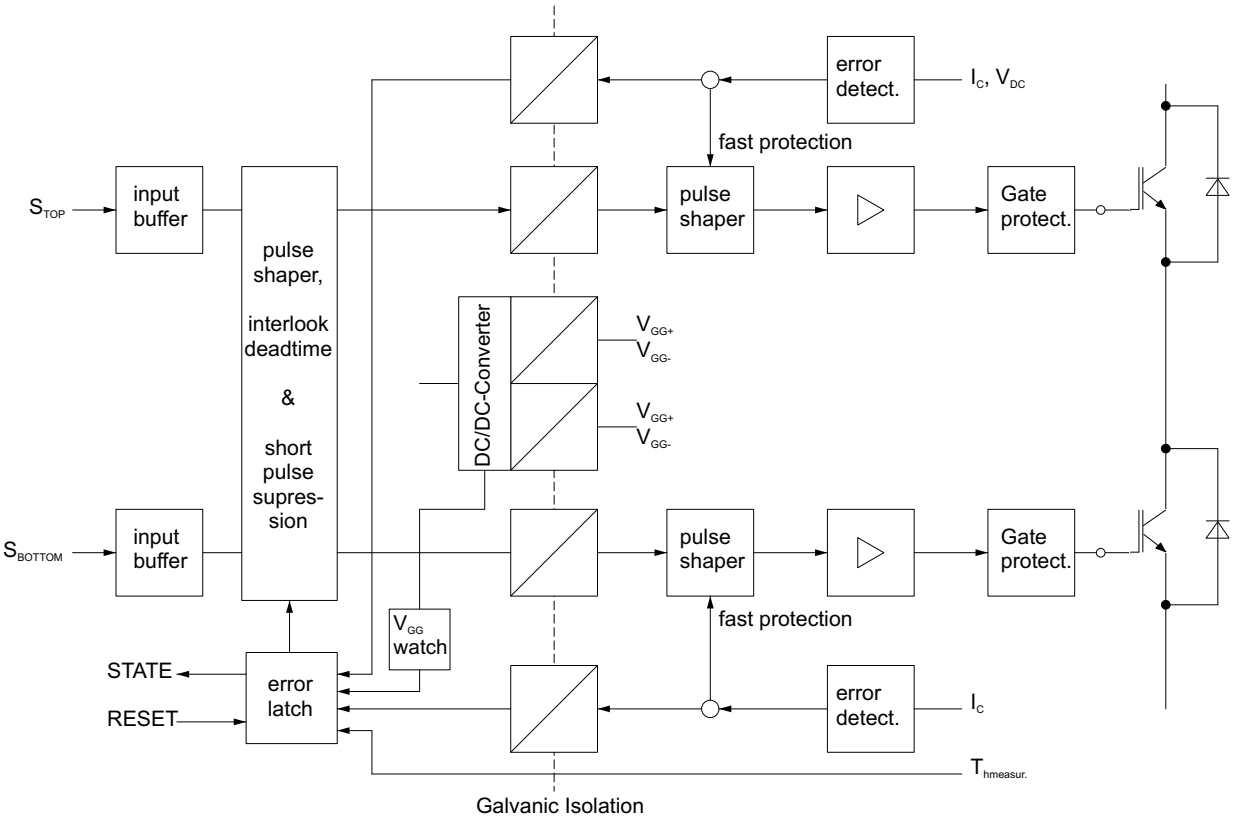


Figure 5.6.8 Block diagram of a high-performance IGBT bridge arm driver circuit with TOP/BOTTOM interlock, protection and monitoring functions

The gate unit is the core part of the driver circuit and consists of (mainly) primary-side time control stages for delay, interlock and minimum on and off times (cf. chapter 5.6.4), potential isolation (with pulse shapers, if necessary) and a generator for positive / negative gate control voltage. Overvoltage protection, sometimes also combined with active clamping for v_{DS} or v_{CE}, may be connected directly at the power transistor gate (cf. chapter 5.7).

Figure 5.6.9 shows the principle behind a driver output stage for positive and negative gate control voltage (designed for IGBT with negative gate-emitter voltage).

Besides the complementary stage with low-power MOSFET (or bipolar transistors), totem-pole drivers (push-pull output stage) with MOSFET or bipolar transistors and emitter followers are also commonly used.

Other types of driver circuits are detailed in chapter 5.6.6.

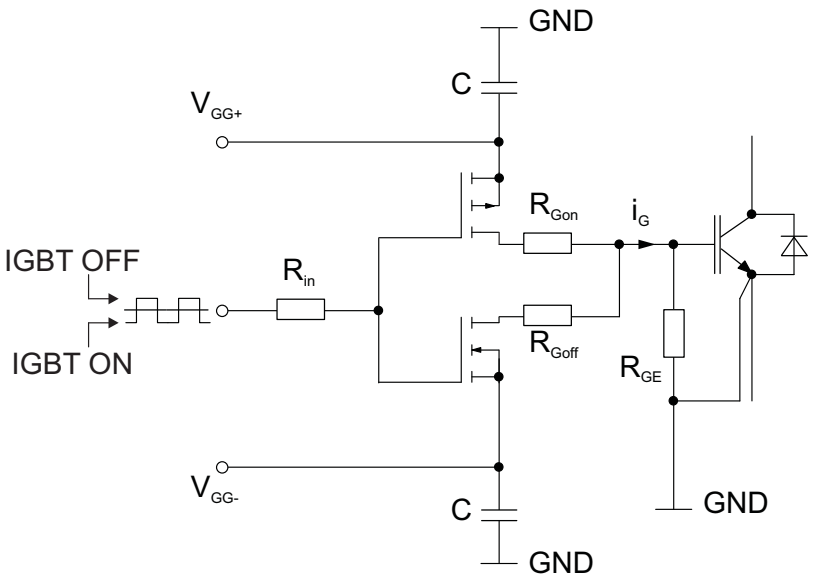


Figure 5.6.9 Driver output stage for gate control voltage turn-on and turn-off

The gate resistance R_G in Figure 5.6.9 is split up into two resistances R_{Gon} and R_{Goff} for turn-on and turn-off, respectively. Thus, cross current conducted from V_{GG+} to V_{GG-}, which is almost inevitably generated during switching of the driver MOSFET, can be limited. The main advantage offered by this solution, however, is that the turn-on and turn-off processes can be optimised individually with regard to all dynamic parameters (cf. chapter 5.6.2) and the switch is fully controllable in the event of malfunction or error (chapter 5.7.3). If only one output is available for R_G, this function can also be maintained by equivalent circuits such as parallelling R_{Gon} and R_{Goff} with the diodes connected in series to the resistors arranged such that the cathode is directed towards the IGBT gate for R_{Gon} and the anode is directed towards the IGBT gate for R_{Goff} (cf. [AN5]).

The gate-emitter resistance R_{GE} (10... 100 kΩ) should not be omitted in any application, since it prevents unintentional charging of the gate capacitance even under driver operating conditions with highly resistive output levels (switching, off-state and driver supply voltage breakdown). This resistor must be positioned next to the transistor control terminals.

The low-inductive capacitors C serve as a buffer for V_{GG+} and V_{GG-} near the driver output and - in connection with the sufficiently low-resistive driver circuit - have provide a minimum dynamic internal driver resistance. The capacitors provide the gate peak currents required for fast switching. They are also important in the process of passive gate-voltage clamping of the driver supply voltages (gate overvoltage limitation) by means of Schottky diodes.

In addition, the following aspects are to be borne in mind for the driver output stage layout:
- minimum parasitic inductances in the gate circuit, e.g. short (<< 10 cm), twisted connection lines between driver and gate/driver and emitter (source); minimum circuit area in accordance with Figure 5.6.9
- elimination of load current feedback to the gate voltage caused by the parasitic emitter / source inductance in the power module
- avoidance of ground loops

- avoidance of transformatory and capacitive coupling between gate and collector circuit (oscillation tendency)

For low-pass filters, pulse shapers and pulse-width-triggered flip-flops integrated into the signal transmission paths for interference suppression, their delay times must be able to accommodate the permissible minimum pulse duration and the necessary response times in the event of malfunction / error.

Additional information is provided in [AN3].

5.6.4 Protection and monitoring functions

To protect MOSFET or IGBT modules in the event of malfunction/errors, the use of different efficient, quick-response protection functions in the driver is recommended, for example overcurrent and short circuit protection, protection from excessive drain-source or collector-emitter voltage, gate overvoltage protection, overtemperature protection and monitoring of the gate control voltages V_{GG+} and V_{GG-}.

With reference to Figure 5.6.8, the integration of protective functions in the driver is explained below. Realization and dimensioning aspects are dealt with in chapter 5.7.

Overcurrent and short circuit protection

The current signal can be generated as an analogue signal (measured via e.g. shunt, current probe, $R_{DS(on)}$ of the driven power MOSFET or sense-source / sense-emitter cells) or maximum rating exceeding (desaturation of the IGBT). As soon as an error has been detected by comparing the actual value to a defined maximum rating, an error memory is set (ERROR status) either on switch potential already or - in the case of potential-isolated sensors - in the primary circuit of the driver, which will block the power transistors until the RESET signal is triggered.

If the error memory is integrated on the secondary side, the error memory status signal will be transmitted to the primary side by a potential-isolated unit. If potential-isolating, high-precision current sensors are used (as for example in SKiiP), their output signal may serve as the actual value for control loops.

Gate overvoltage protection

In contrast to the protection functions described so far, the gate protection might have to limit the gate voltage periodically without the presence of an actual error that would require the power transistors to be turned off. For this reason, there is no connection to the error memory. More details are given in chapter 5.7.3.

Protection from excessive drain-source or collector-emitter voltage

Voltage limitation at the main terminals of a power transistor can be performed by the transistor itself (avalanche-proof MOSFET), by passive networks or by an active circuit, which implements a defined partial turn-on of the transistor in case of overvoltage (cf. chapter 5.7.3).

Optional (option "U") basic protection - although this is not able to detect switching peak voltages and other fast overvoltage peaks - which is integrated into the SKiiP driver as static DC bus voltage monitoring is also available. A "quasi"-potential-isolated sensor will indicate the actual DC bus voltage value, transmit it to the main control circuit in the form of an analogue actual value and set the error memory to ERROR as soon as the limiting value is exceeded. In addition, a brake chopper buffer may be used to protect the DC link capacitors from active feedback loads.

Overtemperature protection

The temperature of the power transistor chips, the temperature around the chips and the heatsink temperature can be determined using the calculation methods described in chapter 5.7.3. If the sensor is isolated, the temperature signal (e.g. voltage) may also be transmitted to a main control circuit. A threshold switch on the primary side will set the error memory to ERROR as soon as a limiting value is exceeded.

Supply undervoltage protection for the gate control voltages V_{GG+} and V_{GG-}

If the gate control voltage drops considerably, the secondary control, protection and transmission functions may fail. Moreover, this will also mean that the power transistors can no longer be fully controlled or blocked.

In order to detect this critical state in time, either one of the control voltages or the internal driver power supply has to be monitored. In the event of an error or malfunction, the error memory is set to ERROR.

5.6.5 Time constants and interlock functions

Short-pulse suppression

When pulse transformers or opto-couplers are used to isolate the control signal potential, it is particularly important to ensure that the driver is protected from control pulses (interference pulses) which are too low or too short and might cause the driver to malfunction.

Schmitt triggers, for example, can be connected in series to the potential isolation, suppressing all turn-on or turn-off signals lower than logic level (CMOS, TTL) or < 0.2...0.5 ms. A similar solution may be applied to the secondary side of opto-couplers.

Dead-time for bridge arm control and bridge arm short-circuit interlock

To avoid a bridge arm short circuit, MOSFET and IGBT in the same bridge arm must not be switched on at the same time in voltage source circuits.

In the static state, this may be avoided by interlock of both drivers even if the driver input signals are affected by interference (not suitable for current source circuits, because overlapping operation of the drivers would be required).

Depending on the type of transistor, specific application and driver, the dead time has to total up to t_{dead} = 2...8 µs.

The blanking time of short circuit protection featuring measurement of drain or collector current and drain-source or collector-emitter voltage

If the transistors have to be turned off because one of the limiting values of the given measurement parameters has been exceeded, the turn-on peak current has to be gated from the measurement. When monitoring the desaturation process of an IGBT, the dynamic saturation voltage characteristic has to be considered, too. During the initial microseconds of the turn-on time, $V_{CEsatdyn}$ is far higher than its final value V_{CEsat} (in the static state in accordance with the static forward characteristic) (Figure 5.6.10). For this reason, short circuit protection must be deactivated during transistor turn-on for a minimum blanking time t_{min} (also referred to as t_{bl}) (cf. Figure 5.6.10).

For the sake of safe short circuit suppression (SC-SOA), the blanking time must not exceed the maximum short-circuit time the transistor may be exposed to (typ. 5...10 µs) (cf. chapter 5.7).

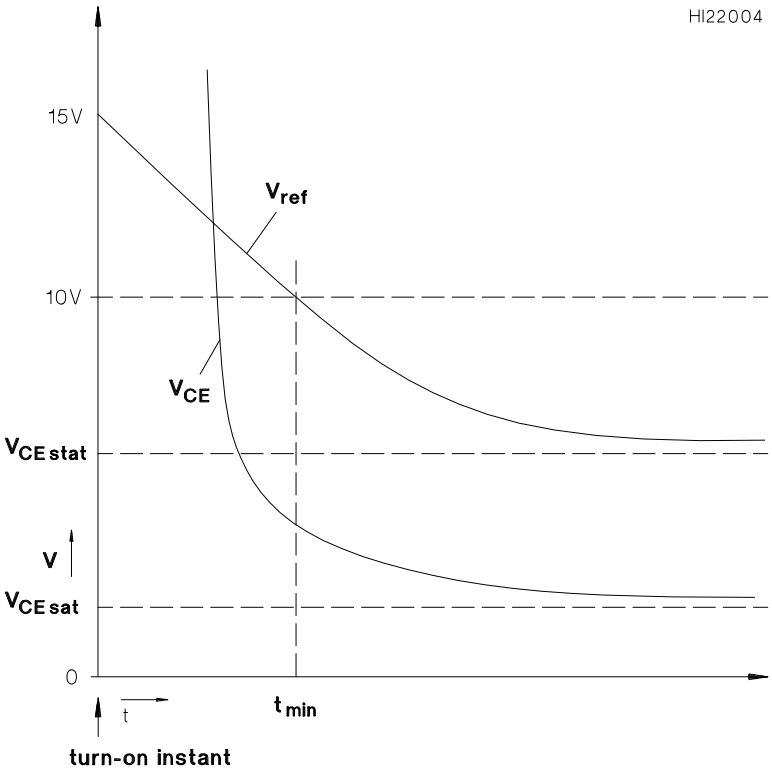
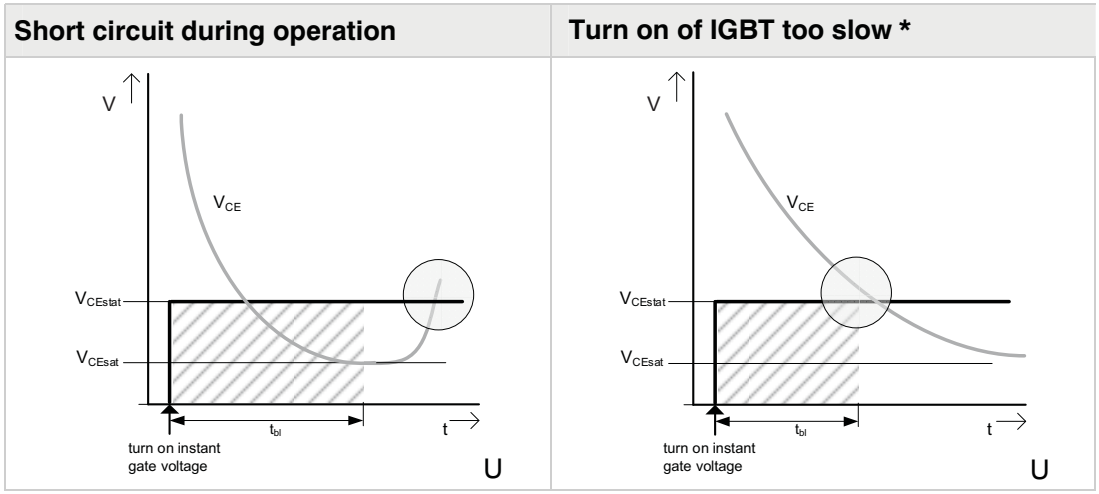


Figure 5.6.10 Dynamic saturation voltage characteristic of an IGBT and possible protection level



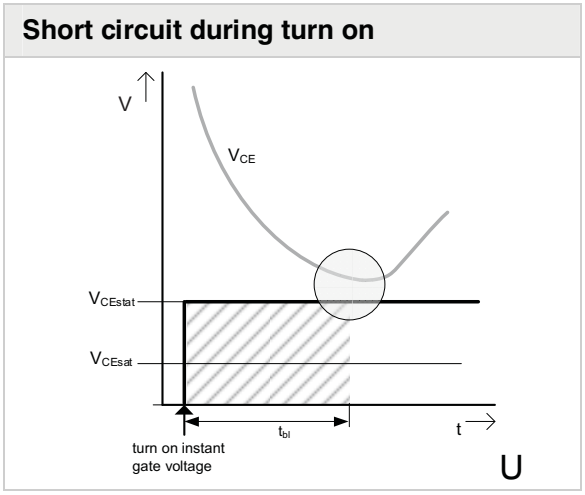


Figure 5.6.11 Possible scenarios for saturation voltage control triggering

5.6.6 Transmission of driver signal and driving energy

Control signals from the control unit to the driver stage, reversely transmitted status and error signals, where applicable analogue measurement values (current, temperature, DC link voltage (optional)) as well as the driving energy have to be transmitted to the driver on separate potentials.

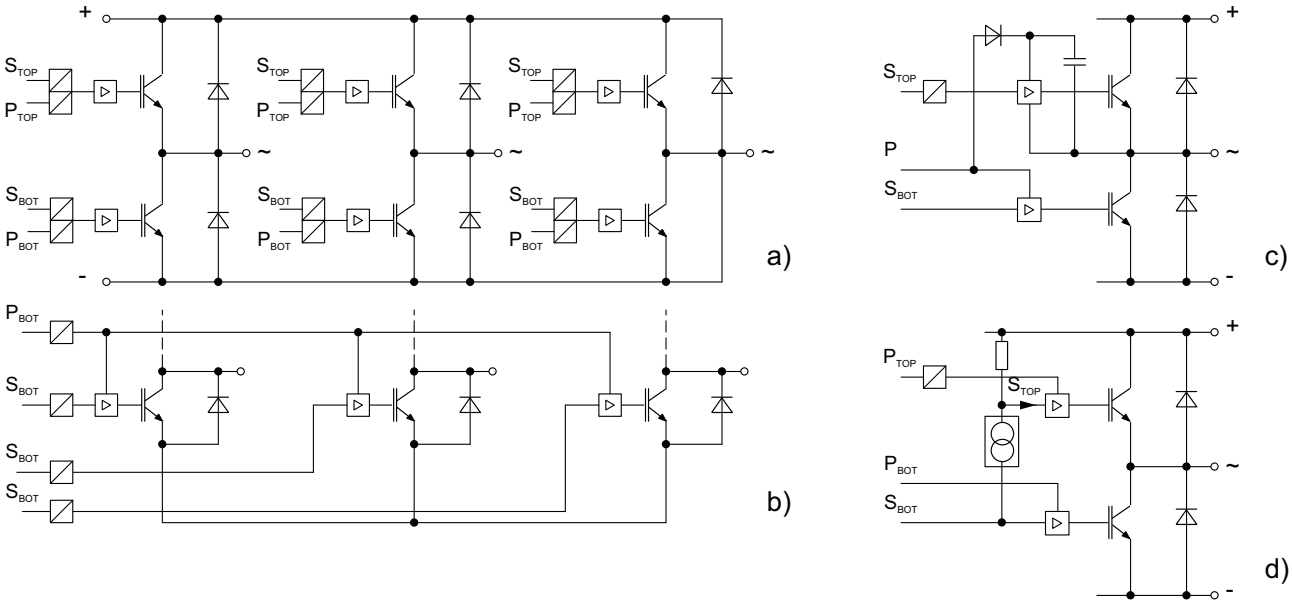


Figure 5.6.12 Selected signal and energy transmission principles
STOP, SBOT: control signal for TOP / BOTTOM switch
PTOP, PBOT: driving energy for TOP / BOTTOM switch
a) Maximum variant, b) Common energy supply for BOTTOM drivers
c) Bootstrap principle, d) Level-shifter principle

In most applications, signals are transmitted via optical or transformatory (magnetic) potential isolation or via "quasi"-potential isolation such as bootstrap circuits (for the driving energy) or level-shifters (for the driver signal).

Figure 5.6.12 shows a diagram of the key basic configurations of signal and energy transmission.

Figure 5.6.12a shows the most common configuration with potential isolation for control signal (S) and driving energy (P), one for each driver circuit. This configuration is preferred (except for low-cost applications) because of its high degree of interference immunity and minimum mutual influence of the switches.

Variant b) contains separate potential isolation circuits for the control signal of all BOTTOM drivers, but only one common potential isolation for the driving energy of the BOTTOM drivers. This is used mainly in low-power applications and is often the preferred solution in IPMs.

The principle behind a bootstrap circuit to supply energy to the TOP switch without "proper" potential isolation is depicted in Figure 5.6.12c. Figure 5.6.12d shows a diagram of a level-shifter, where the control signal S_{TOP} transmitted without galvanic isolation via a high-voltage current source. Usually, level-shifters are used in monolithic driver ICs.

The most important requirements applicable to potential isolation are sufficient static isolation strength (2.5...4.5... kV_{eff}, as defined in the applicable standards; partial discharge test, if required) and sufficient application-specific dv/dt ruggedness (15...100 kV/µs).

High dv/dt-ruggedness can be achieved by using small coupling capacitances (within 1..10 pF range) between the primary and secondary sides of the potential isolation. This will minimise or even avoid signal transmission interference caused by displacement currents during switching (Figure 5.6.12).

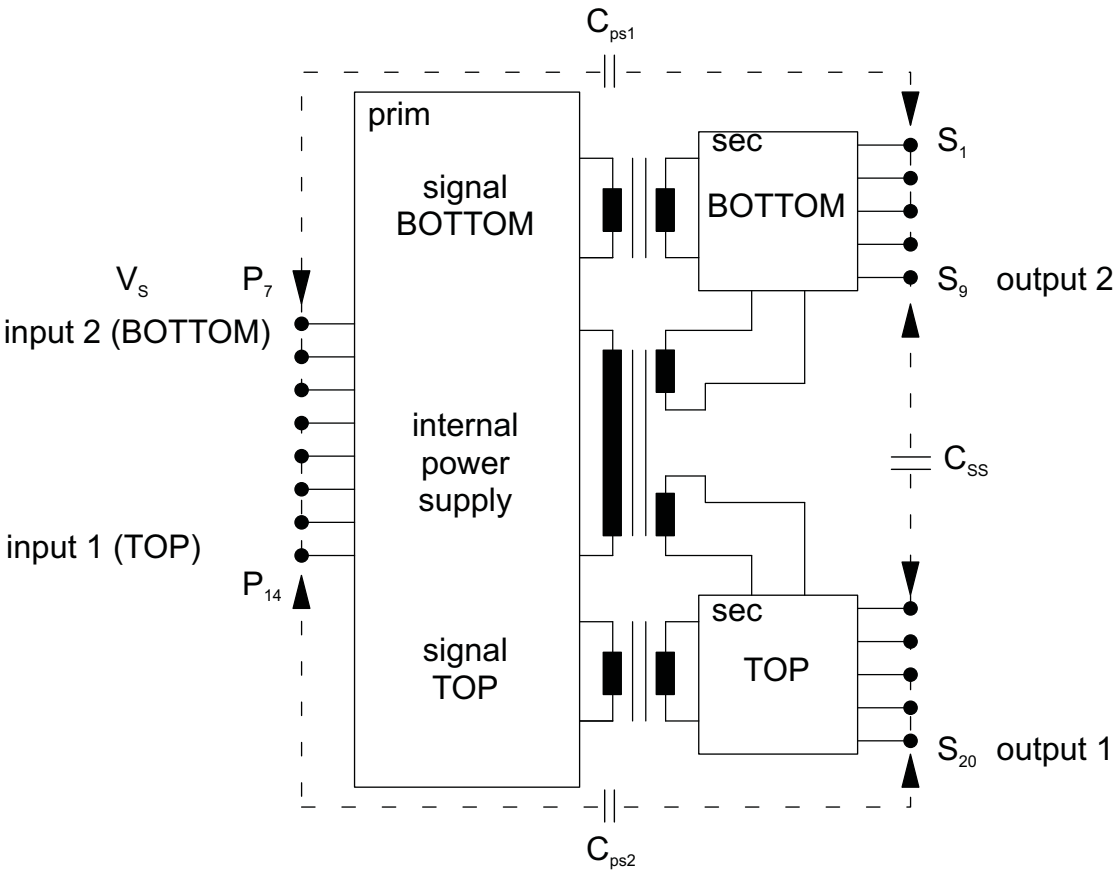


Figure 5.6.13 Diagram of equivalent coupling capacitances in a half-bridge driver with potential isolation
C_{ps1}: Capacitance between primary and BOTTOM secondary side
C_{ps2}: Capacitance between primary and TOP secondary side
C_{ss}: Capacitance between secondary side TOP and BOTTOM

5.6.6.1 Driver control and feedback signals

Table 5.6.1 contains the most common transmission principles used today for driver control and feedback signals with and without potential isolation and the key features of the given principles.

System	Conventional pulse transformer (with magnetic core) Coreless pulse transformer	Opto-coupler	Fibre optic link
Principle behind potential isolation	magnetic	optical/ opto-coupler	optical/ fibre optic link
Galvanic isolation	yes	yes	yes
Transmission directions	bi-directional	uni-directional	uni-directional
Inherent delay time tolerances	low	high	high
Reaction to magnetic field influence	+	-	-
Reaction to electrical field influence	-	-	-
dv/dt immunity (data taken from datasheet examples)	35..50..100 kV/µs	15..25 kV/µs	n/a
System	Giant Magnetic Resistance (GMR) transformer	capacitive transformer	Level shifter
Principle behind potential isolation	magnetic	capacitive	current source
Galvanic isolation	yes	yes	no
Transmission directions	uni-directional	uni-directional	uni-directional
Inherent delay time tolerances	low	low	low
Reaction to magnetic field influence	+	-	-
Reaction to electrical field influence	-	+	-
dv/dt immunity (data taken from datasheet examples)	..30.. kV/µs	25..50 kV/µs	35..50 kV/µs

Table 5.6.1 Principles behind energy and signal transmission

Analogue output signals may be fed back from the driver to the main control unit in a pulse-width modulated state via potential isolations.

5.6.6.2 Driving energy

Table 5.6.2 gives an overview of the most common solutions used for potential-isolated transmission of driving energy to the driver:

System	Mains transformer 50 Hz power supply	primary-side	DC link side	Bootstrap
		power supply unit		
Principle behind potential isolation	transformer-coupled (magnetic)			blocking pn-junction
Galvanic isolation	yes	yes	yes	no
Supplied by	auxiliary voltage or mains voltage	auxiliary voltage	DC link	operating voltage on BOTTOM side
AC frequency	low	very high	medium	medium (pulse fr.)
Smoothing requirements	high	very low	low	low
Output voltage	positive and negative	positive and negative		positive only
Duty cycle limitation	no	no	no	yes
Costs	-	-	+	- -

Table 5.6.2 Principles behind potential-isolated transmission of driving energy

5.6.7 Monolithic and hybrid driver ICs

In most cases, modern drivers are equipped with monolithical driver ICs which come in a wide variety of single, half-bridge, full-bridge and three-phase bridge driver topologies.

These circuits normally comprise the following functions:
- gate voltage generator;
- input for V_{CEsat}- or $V_{DS(on)}$ monitoring; where applicable input for shunt or sense-emitter, too;
- supply undervoltage monitoring;
- error memory and error feedback output;
- variable dead time generation;
- gate control pulse generation
- bootstrap power supply for TOP driver;
- shut down input;
- integrated level shifters for transmission of TOP driver signals.

Modern monolithical driver ICs are manufactured in latch-up free SOI technology and are characterised by their robust level-shifter structures. On the one hand, this results in a considerable improvement in dv/dt-ruggedness. On the other hand, it strengthens the resistance to transient negative voltages and the TOP and BOTTOM driver ground outputs (especially at the TOP-side emitter/source output).

Another possible way to implement an IGBT or MOSFET driver is to combine fast opto-couplers with downstream power driver output stages. Here, to achieve low-cost driver units, all that is needs to be added is a DC/DC converter (or bootstrap circuit) to supply the driving energy, and a few passive components.

With the growing variety of functions and protection mechanisms in driver circuits, the components used in the obligatory primary-side assemblies have to meet ever increasing requirements; these assemblies include, for example, input signal logic, short-pulse suppression, dead time generation, error memory and error evaluation, control for DC/DC converter, and pulse transformer control.

To be able to produce reliable, low-cost driver circuits, these functions have been combined, for instance in control ASICs developed by SEMIKRON.

5.6.8 SEMIDRIVER

SEMIDRIVER are user-friendly, plug-in driver stages for IGBT and MOSFET power modules that differ in the number of driver channels (1, 2, 3, 6 or 7 channels).

By dimensioning the external circuits accordingly, users can adapt the driver parameters, signal interfaces, as well as the protection levels to the given application.

Table 5.6.3 provides an overview of the key parameters of the available driver stages.

Type	V_{CE} [V]	$V_{G(on)}$ [V]	$V_{G(off)}$ [V]	$I_{outpeak}$ [A]	$Q_{out/pulse}$ [µC]
SKHI10/12 R	1200	15	-8	8	9.6
SKHI10/17 R	1700	15	-8	8	9.6
SKHI21 A R	1200	15	0	8	4
SKHI22 A/B H4 R	1700	15	-7	8	4
SKHI22 A/B R	1200	15	-7	8	4
SKHI23/12 R	1200	15	-8	8	4.8
SKHI23/17 R	1700	15	-8	8	4.8
SKHI24 R	1700	15	-8	15	5
SKYPER 32 PRO R	1700	15	-7	15	6.3
SKYPER 32 R	1700	15	-7	15	2.5
SKYPER 52 R	1700	15	-15	50	100
SKHI61 R	900	14.9	-6.5	2	1
SKHI71 R	900	14.9	-6.5	2	1

Type	f_{max} [kHz]	V_{iso} [V]	dv/dt [kV/µs]	Number of channels	Supply voltage [V]	Input logic level [V]
SKHI10/12 R	100	2500	75	1	15	5 or 15
SKHI10/17 R	100	4000	75	1	15	5 or 15
SKHI21 A R	50	2500	50	2	15	15
SKHI22 A/B H4 R	50	4000	50	2	15	15(A), 5(B)
SKHI22 A/B R	50	2500	50	2	15	15(A), 5(B)
SKHI23/12 R	100	2500	75	2	15	5 or 15
SKHI23/17 R	100	4000	75	2	15	5 or 15
SKHI24 R	50	4000	50	2	15	5
SKYPER 32 PRO R	50	4000	50	2	15	15
SKYPER 32 R	50	4000	50	2	15	15
SKYPER 52 R	100	4000	100	2	24	3.3 or 5
SKHI61 R	50	2500	15	6	15	5 or 15
SKHI71 R	50	2500	15	7	15	5 or 15

Table 5.6.3 SEMIDRIVER main parameters

Every SEMIDRIVER includes the following features and functions:
- Power supply +15 V on input control signal potential; integrated SMPS with potential isolation
- 15 V CMOS and/or 5 V TTL compatible control signal inputs; integrated magnetic pulse trans-

formers for potential isolation
- Short circuit protection on the basis of V_{CEsat} monitoring (reference value at 13 V)
- Driver supply voltage control
- Error memory with error feedback and RESET function
- Variable dead time (arm interlock time) between driver TOP and BOTTOM for drivers with 2 or more channels
- Short-pulse suppression

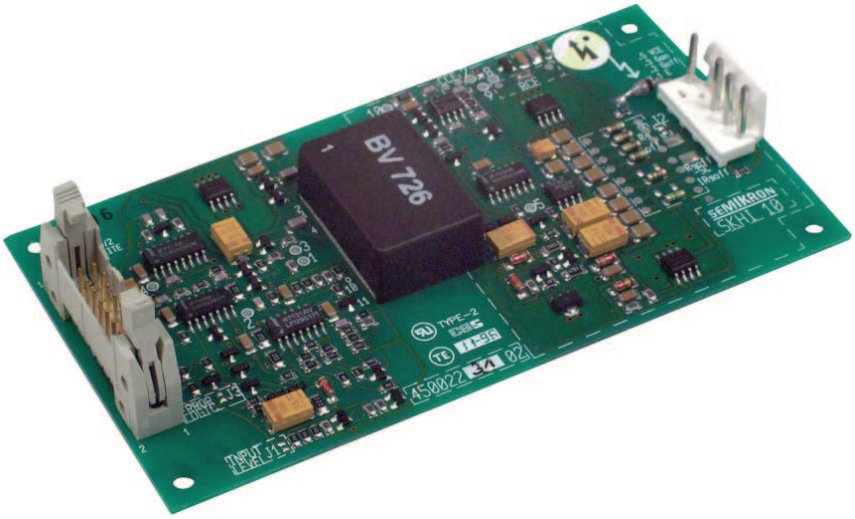


Figure 5.6.14 PCB of a SKHI10 driver stage

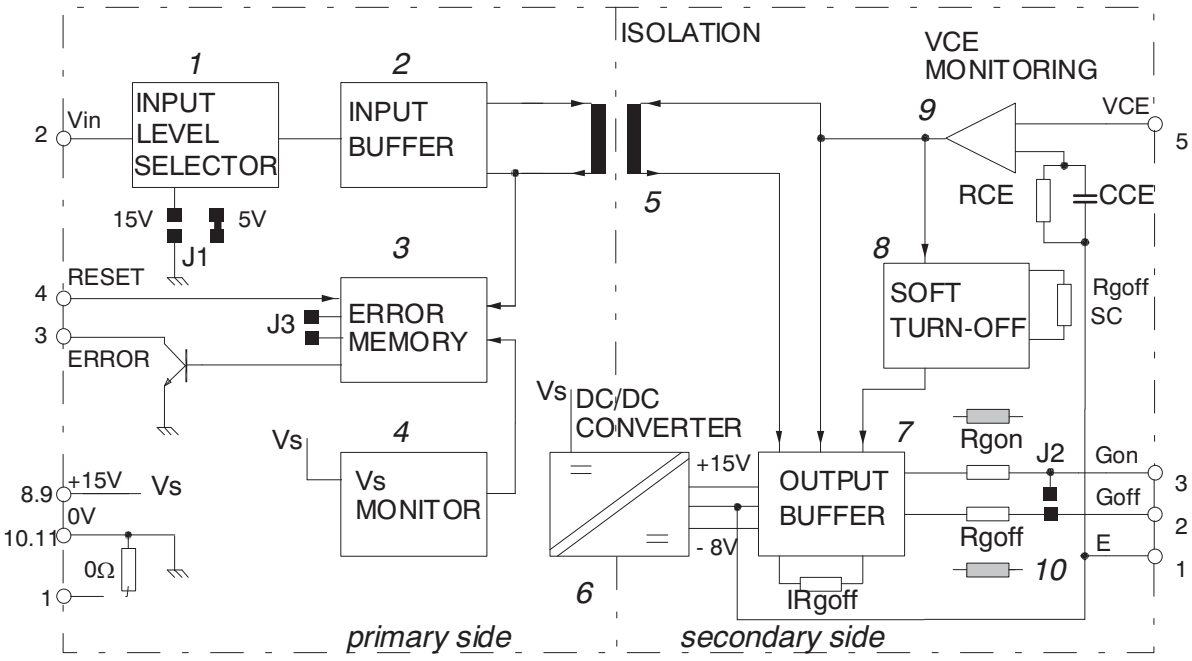


Figure 5.6.15 Block diagram of a SKHI10 driver stage

SKYPER 32, SKYPER 32 PRO and SKYPER 52 IGBT drivers feature, among others, the following functions:
- internal magnetic pulse transformers for potential isolation of control and status signals
- internal potential-isolated SMPS for driver supply
- Short circuit protection on the basis of V_{CEsat} monitoring
- Driver supply voltage control
- Dead time (arm interlock time) between driver TOP and BOTTOM (not adjustable in SKYPER 32)
- Short-pulse suppression
- Error management, error inputs and outputs

SKYPER 32 PRO includes the following additional functions:
- driver undervoltage protection on primary and secondary side
- HALT logic signal
- digital parameter setting for arm interlock time
- external error input
- user-definable soft turn-off function in the event of error/malfunction
- PCB with protective coating

SKYPER 52 features the following additional functions:
- fully digital signal processing
- driver undervoltage protection on primary and secondary side
- HALT logic signal
- common shut down signal
- potential-free transmission of temperature signals from TOP to primary side
- gate voltage clamping
- suppression of input control signal frequencies > 100 kHz
- multi-state/progressive turn-off to optimise switching times and switching overvoltages
- soft turn-off in the event of error/malfunction
- status LEDs
- PCB with protective coating

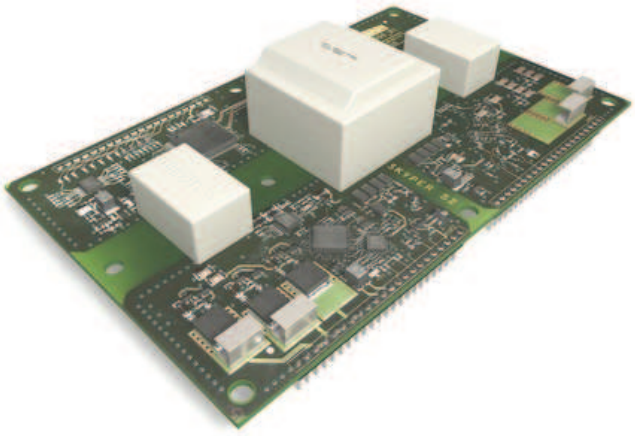


Figure 5.6.16 SKYPER 52 R driver stage PCB

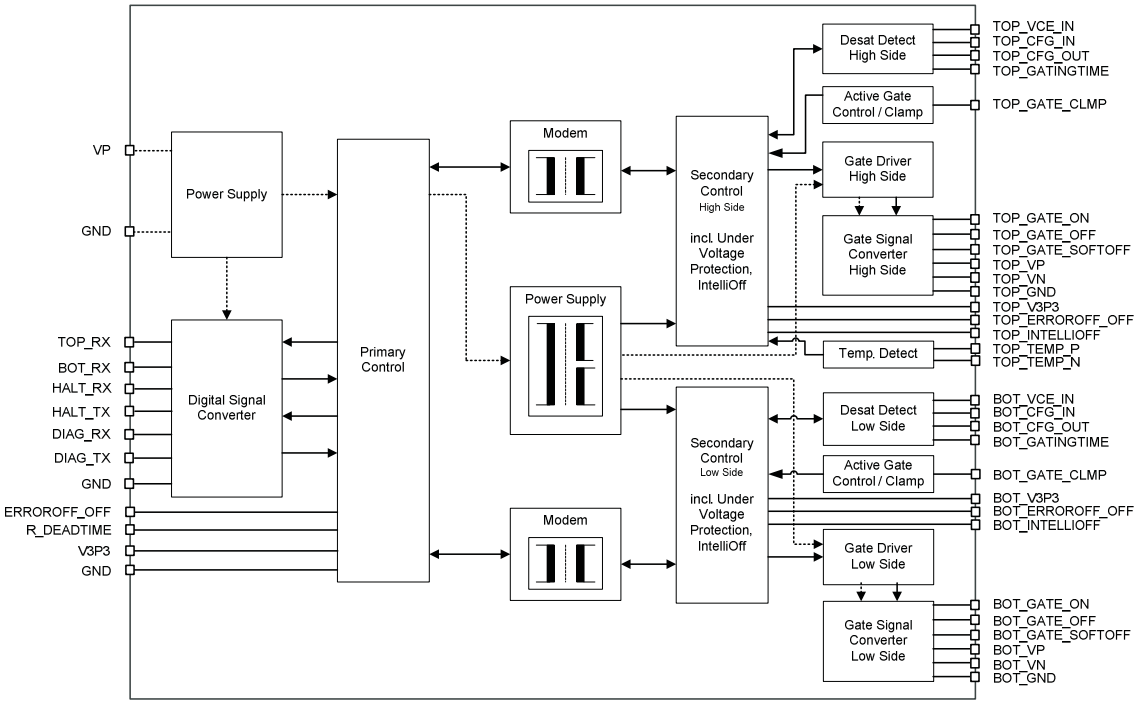


Figure 5.6.17 SKYPER 52 R driver stage block diagram

The "Driver Select Tool“ provided by the simulation and dimensioning software "Semisel“ under www.semikron.com provides the user with a user-friendly aid for selecting the most suitable driver for his application.

5.7 Error behaviour and protection

5.7.1 Types of faults/errors

Power semiconductors have to be protected from non-permissible stress in every operational state.
Leaving SOAs leads to damage and, therefore, reduces component life. In the worst case scenario, the component will be immediately destroyed.
This is why it is important to detect critical states and faults and respond to them with suitable measures.
The explanations in this chapter refer mainly to IGBT, but may also be applied to power MOSFET in the same manner. Any matters relevant to MOSFET in particular will be pointed out separately.

Fault currents

Fault currents are collector / drain currents that exceed standard operating values of a certain application due to control or load errors.
They might lead to damage to the power semiconductors due to the following mechanisms:
- thermal destruction caused by high power dissipation
- dynamic avalanche
- static or dynamic latch-up
- overvoltages that occur in connection with fault currents

A distinction is made between the following fault currents:

Overcurrent

Features:
- usually relatively low collector current di/dt (depending on load inductance and driving voltage)
- fault current is conducted through the DC link
- transistor does not desaturate

Causes:
- reduced load impedance
- converter control error

Short-circuit current

Features:
- very steep collector current di/dt
- fault current is conducted through the DC link
- transistor is desaturated

Causes:
- arm short circuit (case 1 in Figure 5.7.1)
  + by defective switch
  + by faulty driver pulses for the switches
- load short circuit (case 2 in Figure 5.7.1)
  + by faulty isolation
  + human errors (wrong connection wiring etc.)

earth fault current (case 3 in Figure 5.7.1)

Features:
- collector current di/dt is dependent on earth inductance and driving voltage
- earth fault circuit is not closed over DC link
- desaturation of the transistor is dependent on fault current value

Causes:
- connection between a live conductor and earth potential (caused by faulty isolation or human error)

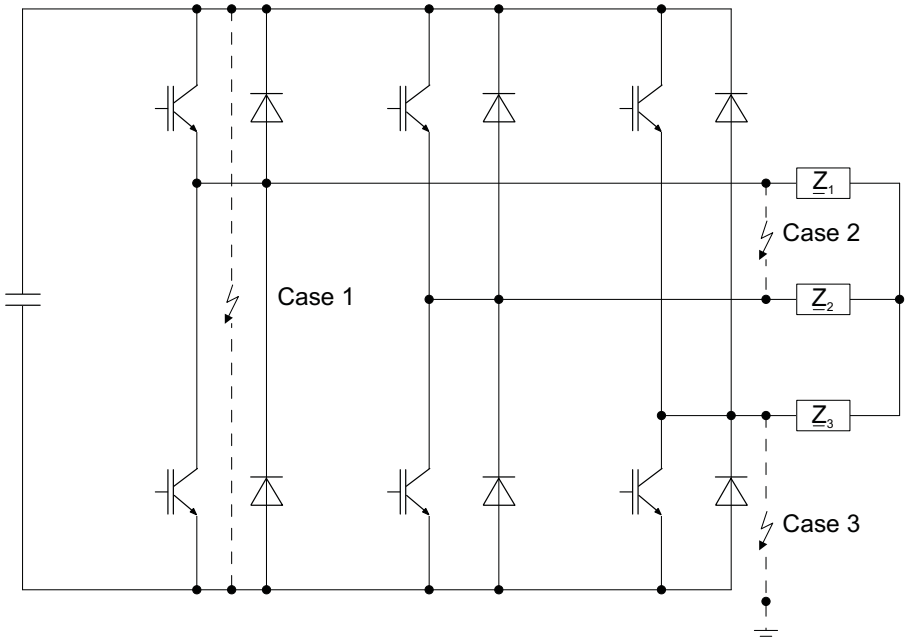


Figure 5.7.1 Causes of fault currents

Overvoltages

Dangerous overvoltages occur if the break-down voltages of power semiconductors are exceeded. This applies to both transistors and diodes. With respect to IGBT and MOSFET, overvoltages may occur between collector and emitter (or drain and source) - i.e. between the main terminals - as well as between gate and emitter (or gate and source) - i.e. between the control terminals.

Causes of overvoltages between main terminals

Figure 5.7.2 shows basic types of overvoltages between the main terminals of power semiconductors on the example of a commutation circuit.

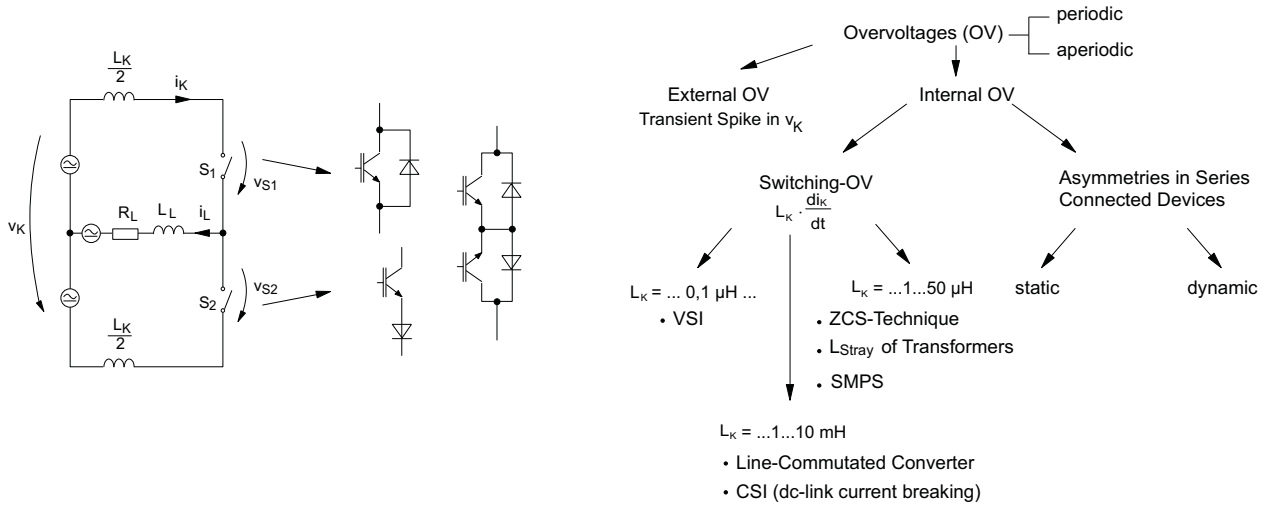


Figure 5.7.2 Types of overvoltages

Generally speaking, in commutation circuits a distinction is made between external and internal overvoltages. In connection with this, an "external overvoltage" is to be seen as a transient increase in the impressed commutation voltage v_K. This may happen, for example, in the DC voltage mains in electric traction power circuits or in any power supply system. Increased DC link voltages are to be seen in the same way (caused e.g. by active feedback loads or control errors in pulse rectifiers).

"Internal overvoltages" are generated, for example, if the power electronic switch is turned off against the commutation circuit inductance L_K ($\Delta v = L_K \cdot di_K/dt$) or if oscillations occur due to switching procedures. The following cases are typical examples of the generation of switching overvoltages:

- Active turn-off of load current i_L by the active elements of switches S_1 and S_2 during normal converter operation:
  In many SMPS applications (Switch-Mode Power Supply), the inductance L_K is generated as a result of the stray inductance of transformers, which may be as much as 1-100 µH.
- Reverse recovery di/dt during passive turn-off of fast diodes in hard switching converters or ZCS converters:
  Owing to their operating principle, ZCS converters may also show an increased commutation inductance within the range of 10 µH (cf. chapter 5.9).
- High di/dt (...10 kA/µs...) in the event of short circuits and during turn-off of short circuit currents in converters with DC voltage link
- Active interruption of DC link currents in CSI topologies (failure).

Furthermore, overvoltages in power electronic devices may be generated by static or dynamic asymmetries in switches connected in series (cf. chapter 5.8). Overvoltages during normal operation of converters and converter fault operation may appear as periodic (...Hz...kHz...) or aperiodic overvoltages.

Causes of overvoltages between control terminals:

Overvoltages between control terminals of IGBT and MOSFET can be due to:

- supply voltage error in the driver stage
- dv/dt feedback (displacement current to the gate) via Miller capacitance (e.g. short circuit II, see chapter 5.7.2),
- emitter / source di/dt feedback (cf. chapter 5.4.1),
- increase in gate voltage during active clamping (cf chapter 5.7.3.2)
- parasitic oscillations in the gate circuit (e.g. connection to collector/drain, transient oscillations between gate circuits of parallelled transistors etc.).

Overtemperature

Dangerous overtemperatures occur if the maximum junction temperature specified by the device manufacturer is exceeded (e.g. T_{jmax} = 150°C...175 °C for silicon devices).

During converter operation, overtemperatures might be generated by:
- an increase in energy dissipation caused by fault currents
- an increase in energy dissipation caused by defective drivers
- failure or malfunction of the cooling system

5.7.2 Behaviour in the event of overload or short circuit

Overload

Essentially, the switching and on-state behaviour under overload does not differ from "standard operation" under rated conditions. In order not to exceed the maximum junction temperature and to ensure safe operation, the overload range has to be restricted, since increased load current may cause increased power dissipation in the device or destruction of components such as diodes due to dynamic failure mode effects.

Here, limits are set by the absolute value of the junction temperature as well as by overload temperature cycles.

These limits are specified in the datasheet SOA diagrams (Safe Operating Area).

5.7.3 shows the example of an IGBT.

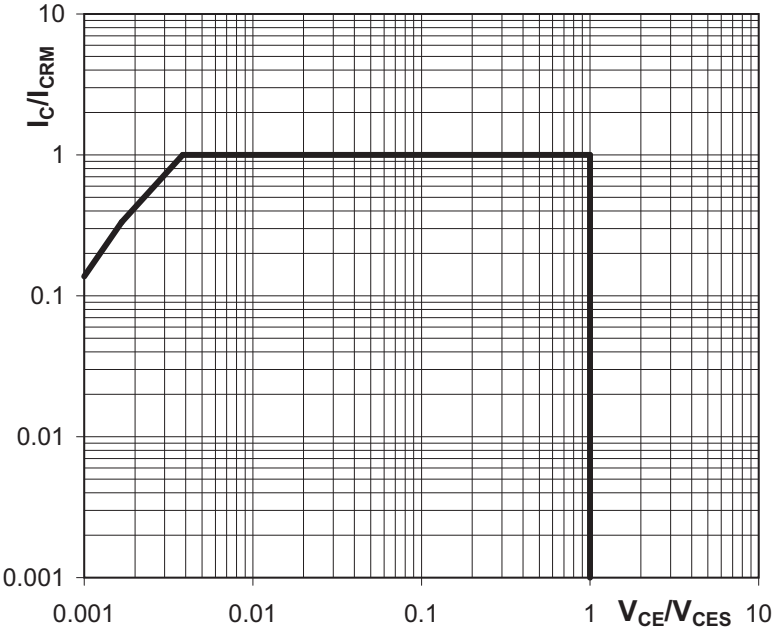


Figure 5.7.3 SOA diagram for an IGBT

Short circuit

Essentially, IGBT and MOSFET are short-circuit proof, i.e. they may be subjected to short circuits under certain given conditions and actively turn these off without damaging the power semiconductors.

Two different types of short circuit must be distinguished between (on the the example of an IGBT).

Short circuit I (SC I)

With SC I, the transistor is turned on when a load or bridge short circuit already exists, i.e. the full DC link voltage is applied to the transistor before the short circuit even occurs. The di/dt of the short-circuit current is determined by the driver parameters (driver voltage, gate resistor) and the transfer characteristic of the transistor. This transistor current increase will induce a voltage drop

over the parasitic inductance of the short circuit, which is manifest as a decrease in the collector-emitter voltage characteristic (Figure 5.7.4).

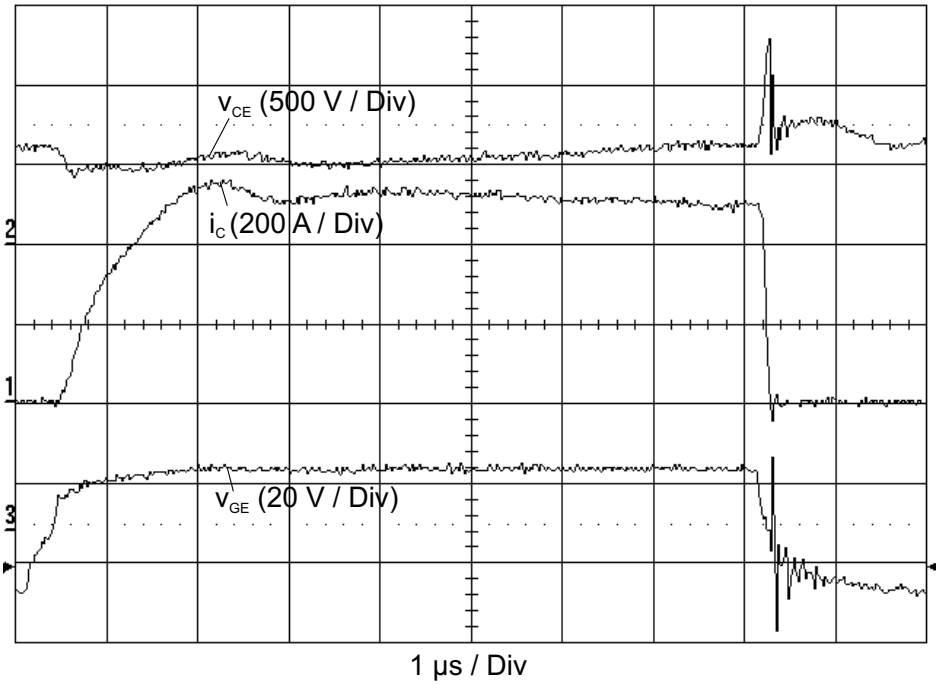


Figure 5.7.4 SC I characteristics of an IGBT

The static short-circuit current adjusts itself to a value determined by the output characteristic of the transistor. Typical values for IGBT of different technologies are as much as 6...10 fold the rated current (cf. Figure 5.7.7b).

Short circuit II (SC II)

In this case, the transistor is already turned on before the short circuit occurs. Compared to SC I, this case is much more critical with respect to transistor stress.

Figure 5.7.5 shows an equivalent circuit and principle characteristic to explain the SC II procedures.

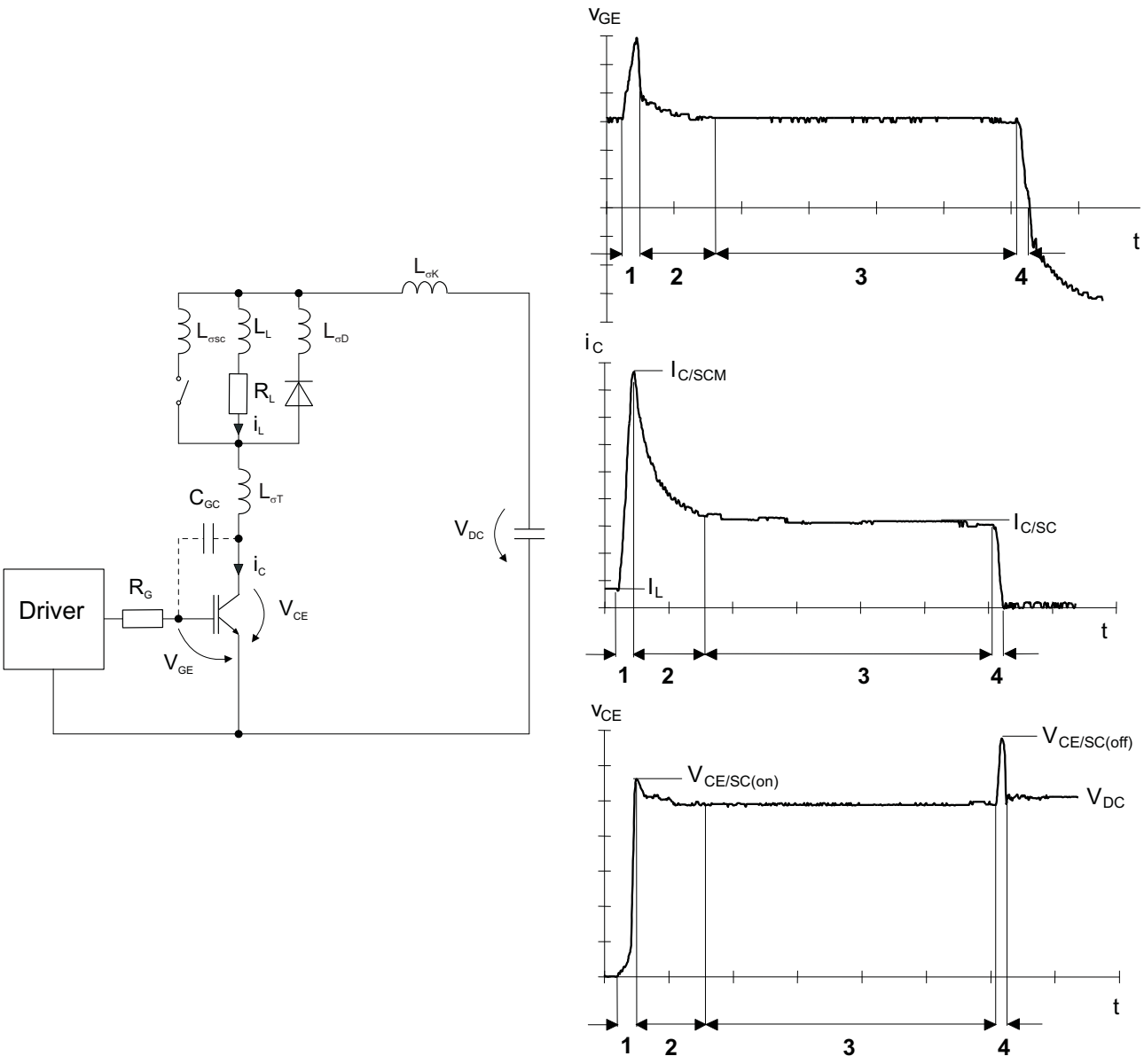


Figure 5.7.5 Equivalent circuit and principle characteristics of SC II, [37]

As soon as the short circuit has occurred, the collector current will increase very steeply, the di/dt is determined mainly by the DC link voltage V_{DC} and the inductance of the short-circuit loop.

During time interval 1, the IGBT is desaturated. The resultant high dv/dt of the collector-emitter voltage will cause a displacement current to flow through the gate-collector capacitance which will increase the gate-emitter voltage. This in turn will cause a dynamic short-circuit peak current $I_{C/SCM}$.

Once the desaturation phase is complete, the short-circuit current will drop to its static value $I_{C/SC}$ (time interval 2). During this procedure, a voltage will be induced over the parasitic inductances which becomes effective as overvoltage in the IGBT.

The stationary short-circuit phase (time interval 3) is followed by turn-off of the short-circuit current towards the commutation circuit inductance L_K, which will in turn induce an overvoltage in the IGBT (time interval 4).
The transistor overvoltages induced during a short circuit may be several times higher than the normal operating values.

The processes that occur during the stationary short-circuit and turn-off phase are identical for SC I and II.

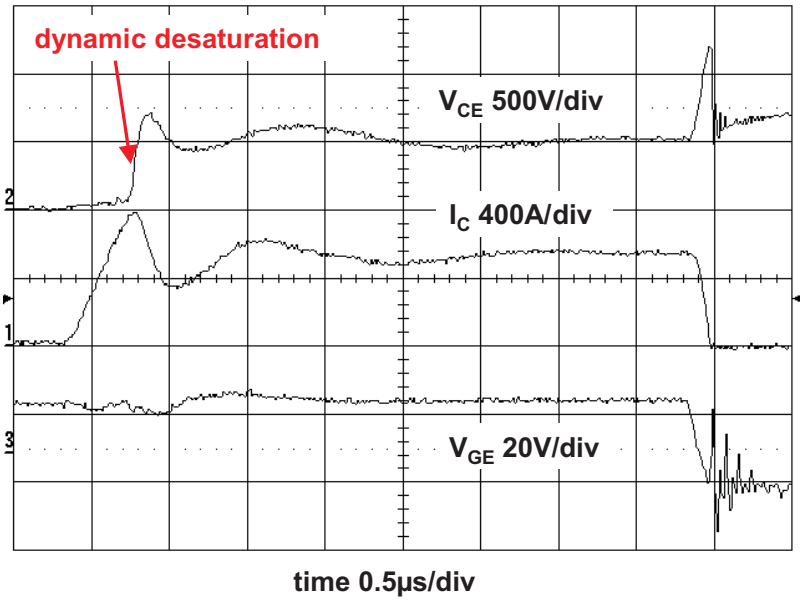


Figure 5.7.6 SC II characteristics of an IGBT with external dynamic gate voltage limitation

The SCSOA diagram (SC = short circuit) for short circuit, as shown in the IGBT datasheets or technical explanations, displays the limits for safe control of a short circuit (Figure 5.7.7a).

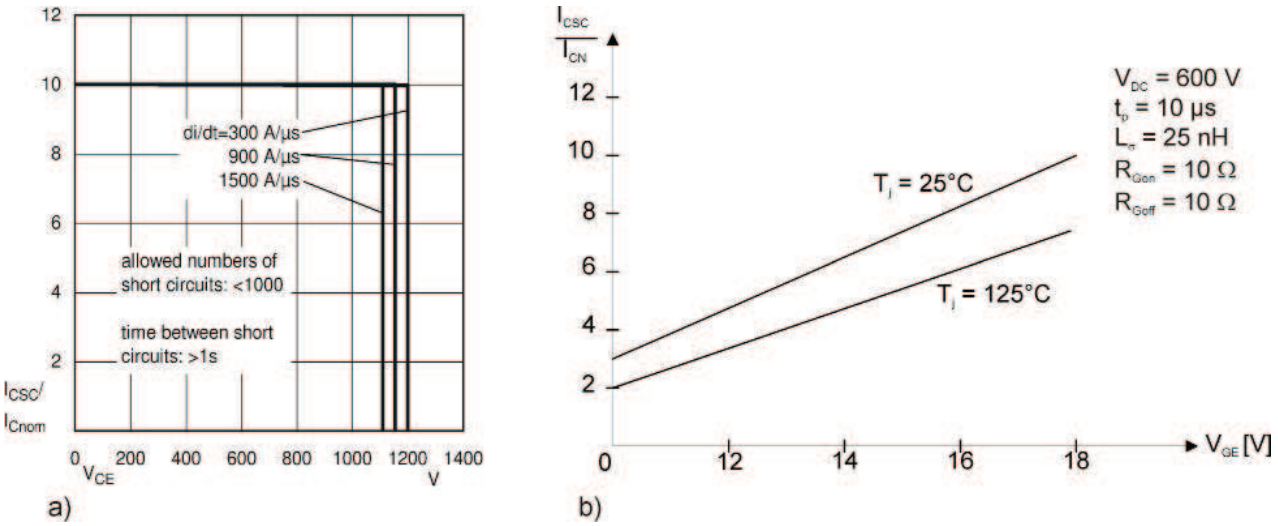


Figure 5.7.7 Short circuit specifications of an IGBT
a) SCSOA; non-periodic, parameters: t_{sc_max}, inductance in the commutation circuit, V_{GE}, T_{jmax}
b) short-circuit current normalised to rated current level as a function of the gate-emitter voltage

The following important conditions must be complied with in order to guarantee safe operation under short-circuit conditions:

- The short circuit has to be detected and turned off within a defined maximum period of time (typically t_{sc_max} = 10 µs for many technologies).
- The time between two short circuits must be within a defined range (typical value for many technologies: 1 s).
- The IGBT must not be subjected to more than a specified maximum number of short circuits during its entire operating time (typical value for many technologies: 1,000).

Figure 5.7.7b shows the influence of gate-emitter voltage and junction temperature on the static short-circuit current.
Short circuit I and II cause high losses in the transistor which increase the junction temperature. In such case, the negative temperature coefficient of the static short-circuit current, also depicted in the IGBT and MOSFET output characteristic, proves its benefits (cf. Figure 5.7.7b).

With respect to the turn-off overvoltages involved, a static short circuit is often not the most critical consequence, especially in applications that use modern IGBT technologies. Tests have shown that maximum overvoltages are induced by turning the IGBT off exactly at its desaturation limit. This case must always be considered when verifying the selected drive and protection concept.

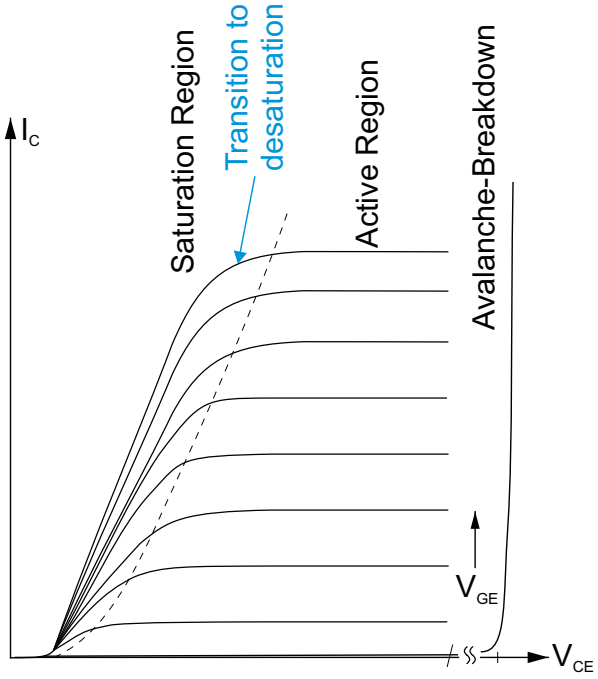


Figure 5.7.8 IGBT desaturation limit

Reliable methods of detecting fault currents and limiting resultant overvoltages are given in chapter Figure 5.7.3.

5.7.3 Fault detection and protection

Errors in converter circuits may be detected at various points. The responses to detected errors, however, may be very different.
The term fast protection is used, if an error signal is detected in the switch or in close vicinity to the switch and the respective switch is turned off immediately by the driver stage. The total response time of the switch may even be just a few 10 nanoseconds.

For error detection outside the switches, an error signal is initially transmitted to the control board, where a response to the error is triggered. This can be referred to as slow protection. Alternatively, the processes that occur may be assigned to converter control (e.g. the system's reaction to overload).
Modern converters mostly combine slow and fast protection processes, depending on the specific application and design philosophy.

5.7.3.1 Detection and reduction of fault currents

Detection of fault currents

Figure 5.7.9 shows a voltage source inverter circuit. Here, the measuring points at which fault currents can be detected are marked.

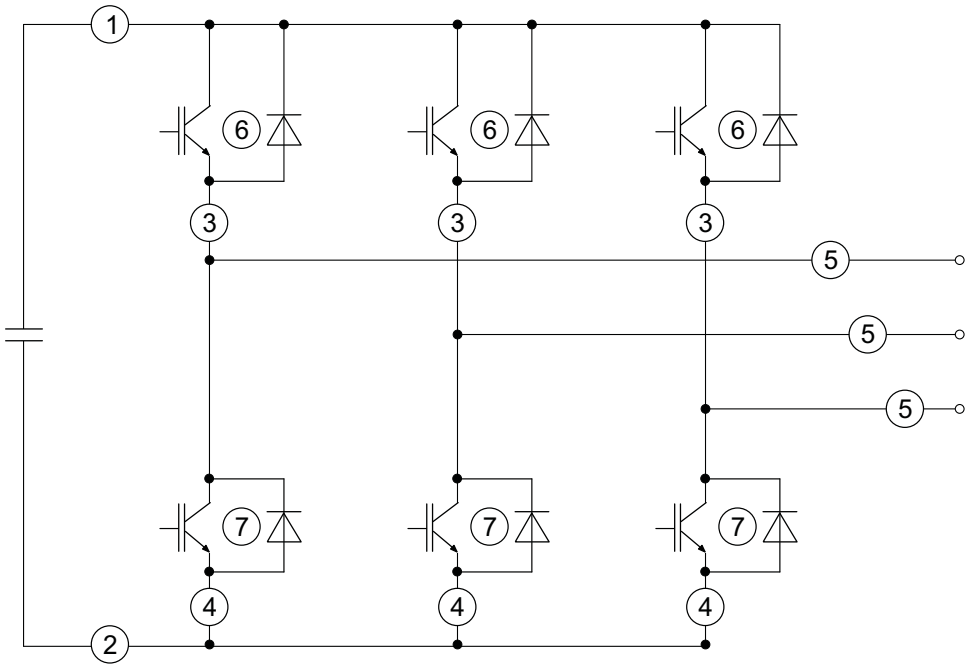


Figure 5.7.9 Voltage source inverter (VSI) with detection points for fault currents

Fault currents can be classified as follows:

Overcurrent:	detectable at points 1-7
Arm short circuit:	detectable at points 1-4 and 6-7
Load short circuit:	detectable at points 1-7
Ground short circuit:	detectable at points 1, 3, 5, 6 or by calculating the difference between 1 and 2

In general, to control short-circuit currents fast protection measures with direct control of the driver output stage are needed, since the transistor has to be switched off (with reduced switching speed, active control provided) within t_{sc_max} (typ. 10 µs). To do so, fault currents may be detected at points 3, 4, 5, 6 and 7.

Measurements at points 1-5 may be taken using measuring shunts or inductive measuring current transformers (frequently used at point 5).

Measuring shunt:
- simple measuring method
- low-resistance (1...100 mΩ), low-inductance power shunts needed
- measuring signal is highly sensitive to interference
- measuring values are not available with potential isolation

Current sensors:
- far more expensive than measuring shunt
- measuring signal is less susceptible to interference than measuring shunt
- measuring values are available with potential isolation

At points 6 and 7, fault currents are detected directly at the IGBT / MOSFET terminals. Here, protection is provided by way of v_{CEsat} or $v_{DS(on)}$ monitoring (indirect measuring method) and current sensing if a sense IGBT / sense MOSFET is used (direct measuring method). Figure 5.7.10 shows the principle circuits.

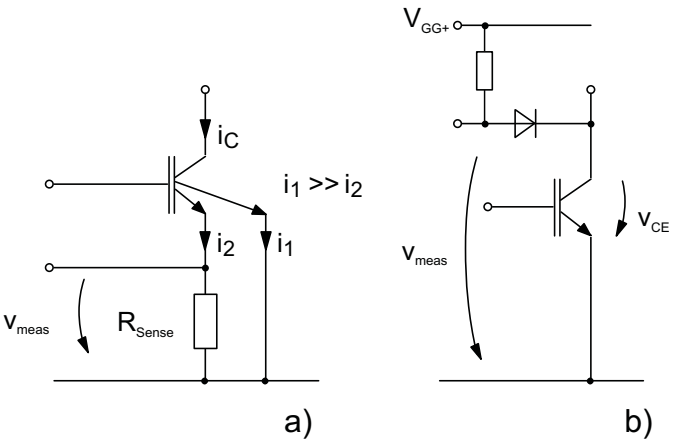


Figure 5.7.10 Fault current detection using a) current sensing and b) v_{CEsat} monitoring

Current sensing with sense IGBT

In a sense IGBT, a few cells are combined to create a sense-emitter, generating two parallel current arms. Information is given by the conducted collector current as soon as it passes the measuring resistor R_{Sense}. At R_{Sense} = 0 the current division ratio between both emitters is ideal, corresponding to the ratio of the number of sense-cells to the total number of cells. If R_{Sense} is increased, the current conducted in the measuring circuit will be reduced by feedback of the measuring signal.
For this reason, resistance R_{Sense} should be within a range of 1...5 Ω to obtain a sufficiently accurate measurement result for the collector current.
If the turn-off current threshold value is only slightly higher than the transistor rated current, the current monitoring has to be made ineffective during IGBT turn-on because of the reverse-recovery current peak of the free-wheeling diode.
For very high sense-resistances ($R_{Sense} \rightarrow \infty$), the measuring voltage corresponds to the collector-emitter saturation voltage, meaning that the current sensing acts as v_{CEsat} monitoring.

v_{CEsat} monitoring

v_{CEsat} monitoring makes use of the relationship between collector current and collector-emitter voltage (forward voltage, output characteristic) indicated in the transistor datasheets.
The collector-emitter voltage is detected by a fast high-voltage diode and compared with a reference value. If the reference value is exceeded, the error memory is set and the transistor turned off. The fast desaturation process in the transistor means that short circuits are quickly detected. If the transistor is not desaturated in the event of a fault (e.g. if slowly increasing ground fault currents and overcurrents are involved), the use of v_{CEsat} monitoring for fault detection is restricted.
To guarantee safe turn-on of the IGBT during normal operation, v_{CEsat} monitoring has to be blanked out long enough for the collector-emitter voltage to fallen below the reference voltage (cf. chapter 5.6.4). Since no short-circuit protection exists during this period, the blanking time must not exceed t_{sc_max}.
Temperature dependency of the output characteristic as well as parameter tolerances have negative effects on v_{CEsat} monitoring. However, the main advantage over current sensing using a sense IGBT is that this protection concept is applicable to every standard IGBT or MOSFET.

Fault current reduction

A better way to protect the transistor switch is to reduce or limit high fault currents, especially with regard to short circuits and low-impedance ground fault circuits.

As explained in chapter 5.7.2, a short circuit of type II will generate a dynamic short-circuit overcurrent due to the increase in the gate-emitter voltage as a result of high dv_{CE}/dt.
The amplitude of the short-circuit current may be reduced by clamping the gate-emitter voltage. Suitable circuit variants are given in chapter 5.7.3.2.
Besides limiting dynamic short-circuit overcurrents, static short-circuit currents may also be decreased by reducing the gate-emitter voltage (cf. Figure 5.7.7 in chapter Figure 5.7.2). This will reduce transistor power losses during the short-circuit phase. At the same time, overvoltage is

decreased, since the short circuit current has to be turned off at a lower level. This principle is shown in Figure 5.7.11.

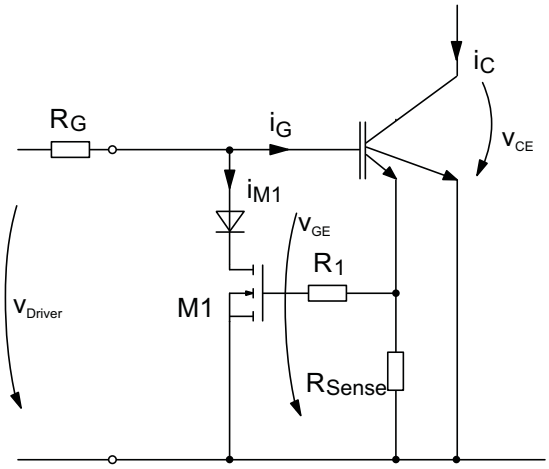


Figure 5.7.11 Short-circuit current limitation by reducing gate-emitter voltage [37]

This protection method limits the static short-circuit current to about 2.5...3 times the rated current in given applications in practice.

5.7.3.2 Overvoltage limitation

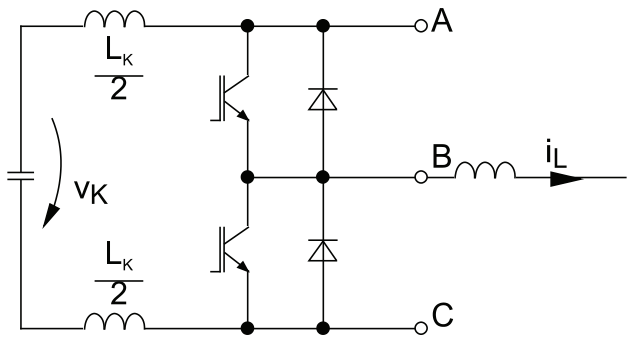
Overvoltage limitation between main terminals [72]

Measures to limit overvoltages between main terminals (collector-emitter voltage, DC link voltage) can be divided into passive snubber-networks, active clamping and dynamic gate control. Irrespective of the type of overvoltage limitation, the avalanche operation mode of MOSFET can be utilised, if applicable. The limiting values given in the datasheets must be strictly adhered to. In addition, the suitability of avalanche operation for the intended application should be confirmed by the manufacturer.

Passive snubber networks

Passive networks (snubbers) are combinations of passive elements such as R, L, C, suppressor diodes, diodes, varistors etc. Figure 5.7.12 shows basic and frequently used circuits.

Basic Circuit



Snubber Variants

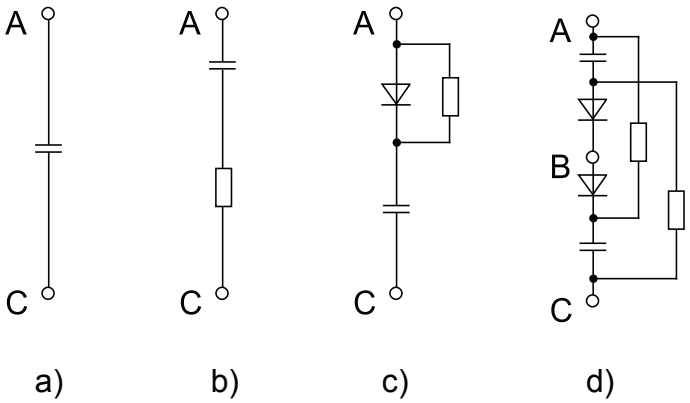


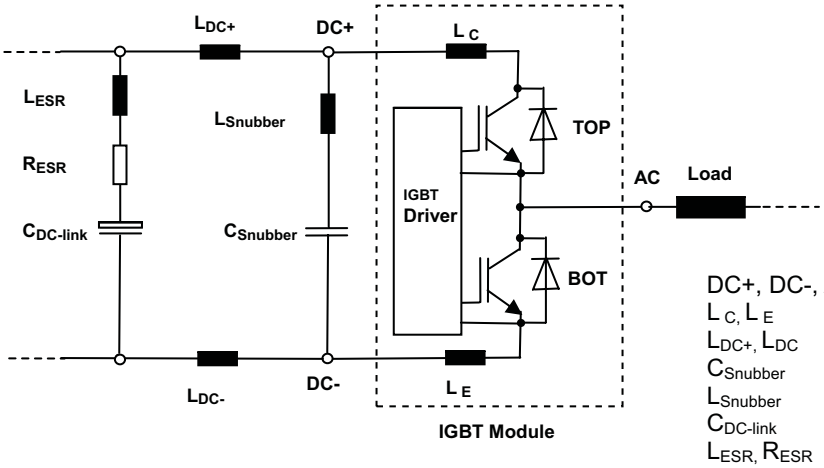
Figure 5.7.12 Passive overvoltage limitation networks (snubbers)

Passive snubber networks prevent dangerous overvoltages from being induced by the inductances of the commutation circuit L_K by attaching a capacitor which absorbs the energy stored in L_K ($E = L_K/2 \cdot i^2$). To ensure that the circuit continues to work effectively, the absorbed energy has to be discharged again between two charging processes. With simple snubbers, this task is performed by heat conversion in the snubber resistors or by feedback to the DC link capacitor.

The simplest method is to clamp the DC link voltage directly to the power module terminals by means of a capacitor (such as a film capacitor). This measure is sufficient for many VSI applications. In this case, the capacitance value lies in the region of 0.1...2 µF (Figure 5.7.12a).

The following parameters must be considered when dimensioning the capacitor:
- DC voltage class of the capacitor (e.g. 1000 V, 1250 V, 1600 V)
- Capacitance and minimum parasitic internal inductance
- Pulse current capability
- Effective capacitor voltage and current (power losses!)
- Service life

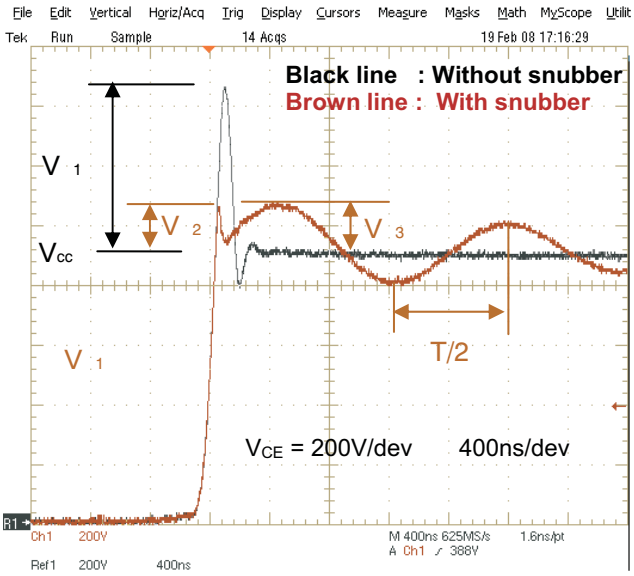
Figure 5.7.13 shows a simplified equivalent DC link circuit with typical, concentrated parasitic inductances.



DC+, DC-, AC	IGBT module terminals
L_{C}, L_{E}	IGBT module parasitic inductance
L_{DC+}, L_{DC-}	Bus bar parasitic inductance
$C_{Snubber}$	Snubber capacitor capacitance
$L_{Snubber}$	Snubber capacitor series inductance
$C_{DC-link}$	DC-link capacitor capacitance
L_{ESR}, R_{ESR}	DC-link capacitor parasitics

Figure 5.7.13 Simplified equivalent DC link circuit with typical, concentrated parasitic inductances

Figure 5.7.14 shows the typical voltage characteristics of an IGBT turn-off process with and without snubber and compiles simplified equations for dimensioning the snubber circuit.



$$\Delta V_1 = \Sigma L \cdot di_c / dt$$

$$\Delta V_2 = (L_C + L_E + L_{Snubber}) \cdot di_c / dt$$

$$\Delta V_3 \leq \sqrt{\frac{L_{DC\text{-}Link} \cdot i_c^2}{C_{Snubber}}}$$

$$f = \frac{1}{T} = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{DC-Link} \cdot C_{Snubber}}}$$

$$\Sigma L = L_C + L_E + L_{DC+} + L_{DC-} + L_{ESR}$$

$$L_{DC-Link} = L_{DC+} + L_{DC-} + L_{ESR}$$

Figure 5.7.14 IGBT turn-off process: typical voltage characteristics with and without snubber; simplified equations for snubber circuit dimensioning

Further technical information is provided in [AN1].

To absorb parasitic oscillations between C and L, voltage clamping may be implemented using an RC element (Figure 5.7.12b). This measure is often taken for low-voltage / high-current applications (e.g. MOSFET converters) to avoid parasitic oscillations in the DC link voltage at the module terminals when switching high currents.
Figure 5.7.12c and d show RCD networks. The integrated fast diodes should display low forward turn-on overvoltage and soft reverse-recovery behaviour.
The design of the snubber network itself and the power module terminals (A,B,C) must be as low-inductive as possible.
An advantage of passive networks besides their simple topologies is that they do not require active components.
A disadvantage of this, however, is that the overvoltage limit value varies depending on the operating point of the converter. For this reason, dimensioning has to be based on the worst case scenario (overcurrent, short circuit, high di/dt).

Active clamping [37], [73]

Active clamping of MOS-controlled transistors refers to direct feedback of the collector / drain potential to the gate via a Zener element. Figure 5.7.15 shows the basic principle and variants produced with the example of an IGBT-switch.

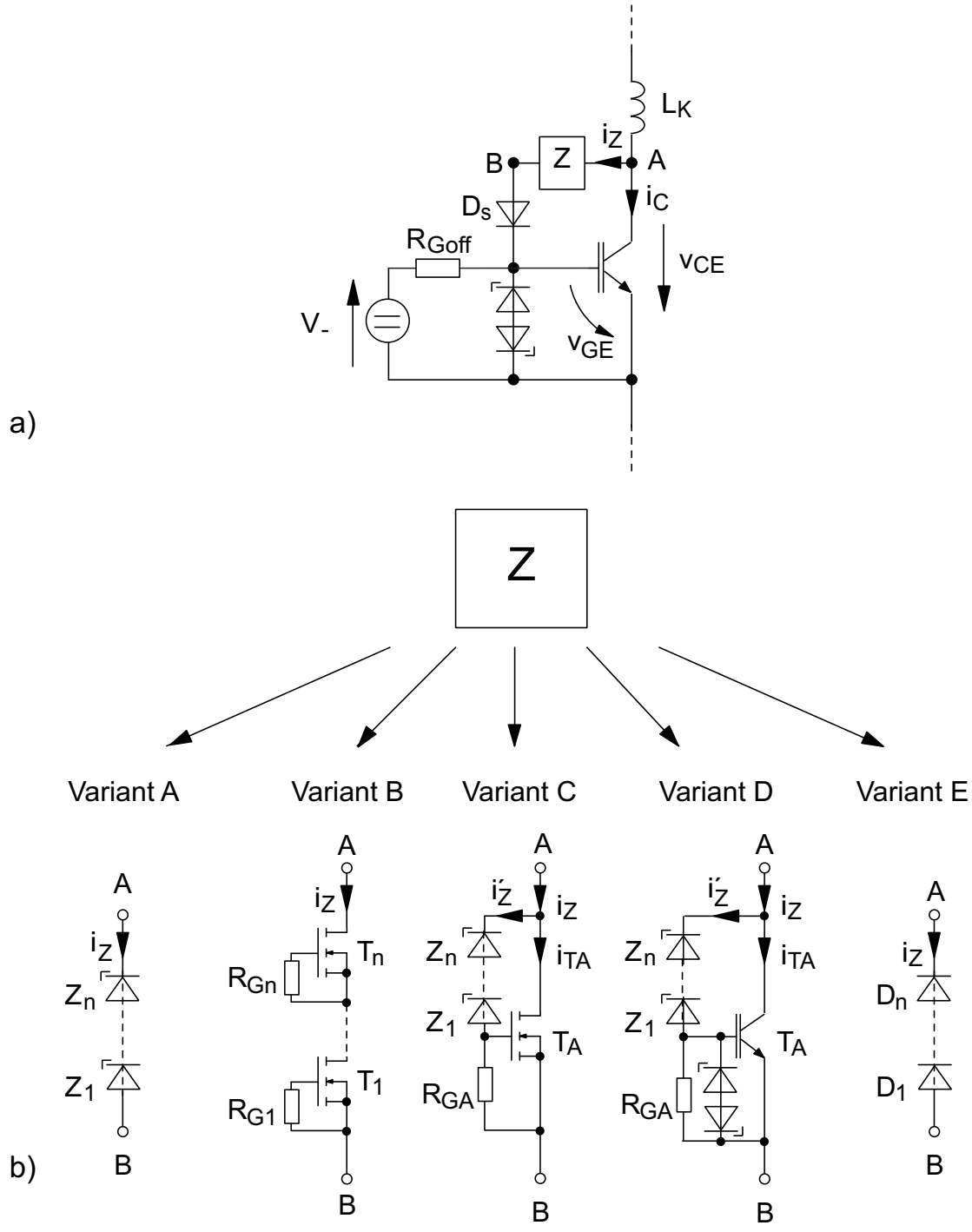


Figure 5.7.15 Basic principle and types of active clamping

The feedback arm consists of a Zener element Z and a series-connected diode D_s, which will stop current flow from driver to collector when the IGBT is turned on.
If the collector-emitter voltage passes the avalanche breakdown voltage of the Zener element, a current will be conducted to the IGBT gate via feedback coupling which will raise the gate potential to a value given by the IGBT transfer and output characteristic ($i_c = f(v_{CE},v_{GE})$) (Figure 5.7.16).
The clamping process lasts as long as current is impressed by the series inductance. The voltage applied to the transistor is determined by the current-voltage characteristic of the Zener element.

The transistor operates in the active area of its output characteristic (!!safe operating area!!) and converts the energy stored in L_K (often also referred to as stray inductance L_S) to heat (Figure 5.7.16). Figure 5.7.16 explains these correlations by way of a simplified equivalent circuit and typical characteristics.

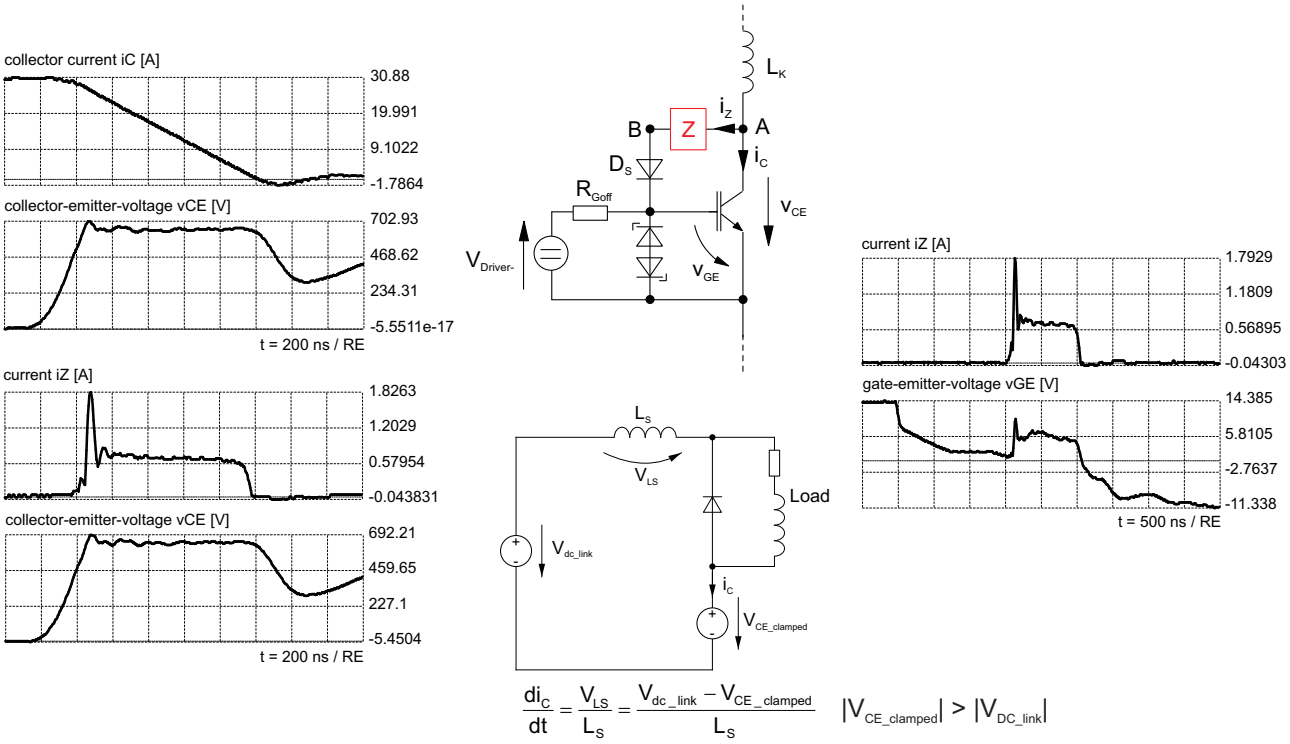


Figure 5.7.16 Simplified equivalent circuit and typical current and voltage characteristics during active clamping of an IGBT (variant A)
Example: V_{dc_link} = 400 V, $V_{CE\_clamped}$ = 640 V, i_{C0} = 30 A, L_S = 10 mH, T_{j0} = 30°C, V_{GE_off} = -15 V

The switching energy processed in the transistor switch during active clamping can be calculated using a simplified equation:

$$E_{clamp} = \frac{L_S}{2} \cdot i_{C0}^{\ 2} \cdot \frac{V_{CE\_clamped}}{V_{CE\_clamped} - V_{DC\_link}}$$

The gate charge peak current needed to increase the gate-emitter voltage at the beginning of the clamping process is clearly shown in Figure 5.7.16.

The clamping circuit may be effective either directly at the gate or at the driver output stage.

The choice of clamping channel depends on the average power dissipation in the Zener element. The following principle applies: the higher the voltage difference between commutation voltage (DC link voltage) and clamping voltage, the lower the losses in the clamping circuit.
Other possible selection criteria are the dynamic response of the circuit and the rate of rise of the Zener characteristic (Figure 5.7.17).

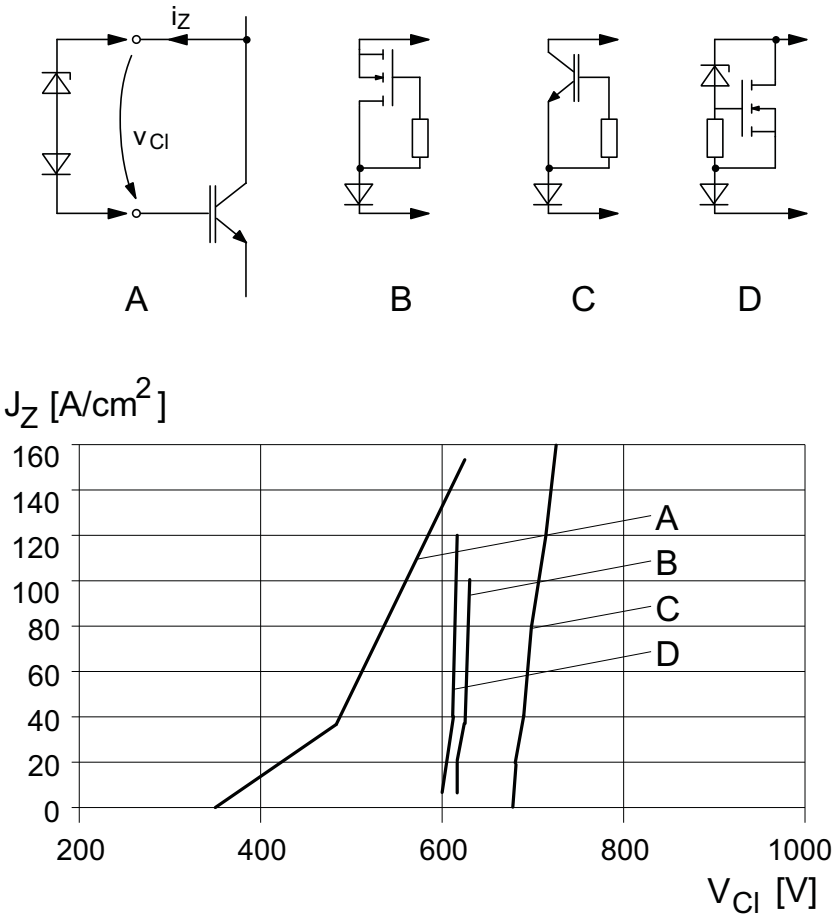


Figure 5.7.17 Static characteristics of selected Zener elements

A: Suppressor diode B: MOSFET during avalanche breakdown

C: IGBT during avalanche breakdown D: Suppressor diode + MOSFET as amplifiers

Version A shown in Figure 5.7.17 can be achieved rather easily and may be used in low clamping energy applications (e.g. in aperiodic processes in voltage source inverters). The MOSFET and diodes in versions B and E are operated in avalanche mode. This mode of operation is to be specified explicitly in the datasheet and must be approved by the manufacturer. In versions C and D, the MOSFET/IGBT serves as to amplify the Zener current; version D boasts particularly high ruggedness.

Active clamping involves the following features:
- simple circuit arrangement
- the transistor to be protected is part of the protection itself and converts the main share of energy stored in the inductance during the clamping process
- there is no need for power resistors and snubber capacitors
- steep clamping characteristic
- the switch voltage to be limited does not depend on the operating point of the converter
- no separate power supply is needed
- conventional drivers may be used
- overvoltages during reverse-recovery di/dt of the inverse diodes are limited inherently
- option to equip either every single transistor switch with a clamping circuit or to attach one central clamper for one or several pairs of switches

The principle of active clamping is applicable to both aperiodic (e.g. short-circuit turn-off) and periodic (e.g. in certain ZCS-topologies) clamping processes and has to be dimensioned accordingly.

Dynamic gate control [74], [75]

In the process of dynamic gate control, the di/dt and dv/dt of MOSFET and IGBT and the resultant induced overvoltages are directly determined by the driver. Simple dynamic gate control includes soft turn-off of IGBT and MOSFET in the event of overcurrents or short circuit; soft turn-off here is achieved either by applying higher gate series resistances (e.g. driver SKHI23, SKYPER52) or by implementing turn-off with a defined small gate current (current source control). (Figure 5.7.18).

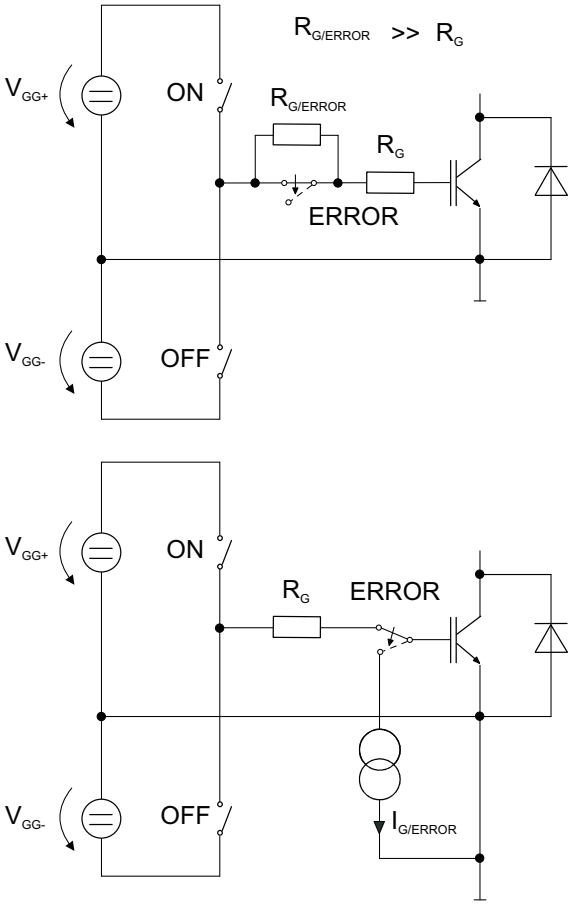


Figure 5.7.18 Possible IGBT soft turn-off processes in the event of malfunction (extremely simplified diagram)
a) Increased R_{Goff} b) Current source control

In more complex driver circuits, the gate series resistors are switched consecutively even during standard-mode converter operation in order to optimise switching times, switching losses and switching overvoltages (e.g. "intelligent turn-off" function in SKYPER52 driver).

In a number of drivers known from technical literature and real applications, the IGBT / MOSFET di/dt and dv/dt are detected passively and fed back dynamically to the gate or the driver output stage (Figure 5.7.19).

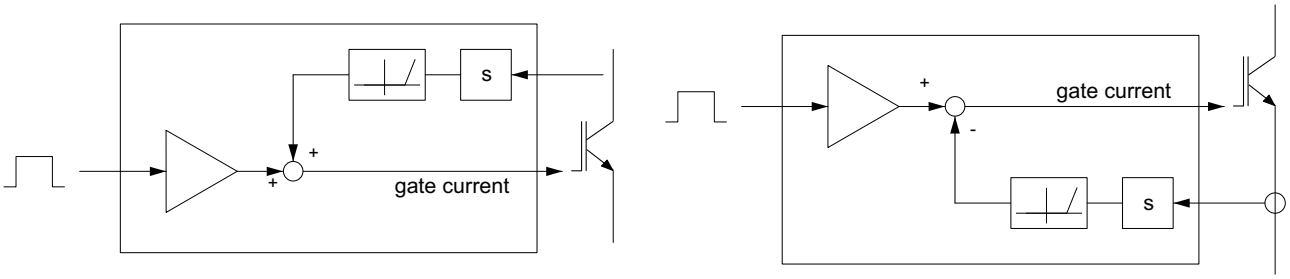


Figure 5.7.19 Direct dynamic dv/dt and di/dt feedback (extremely simplified diagram)

Here, the information on di/dt or dv/dt is obtained by inductance at the emitter or by capacitance at the collector.

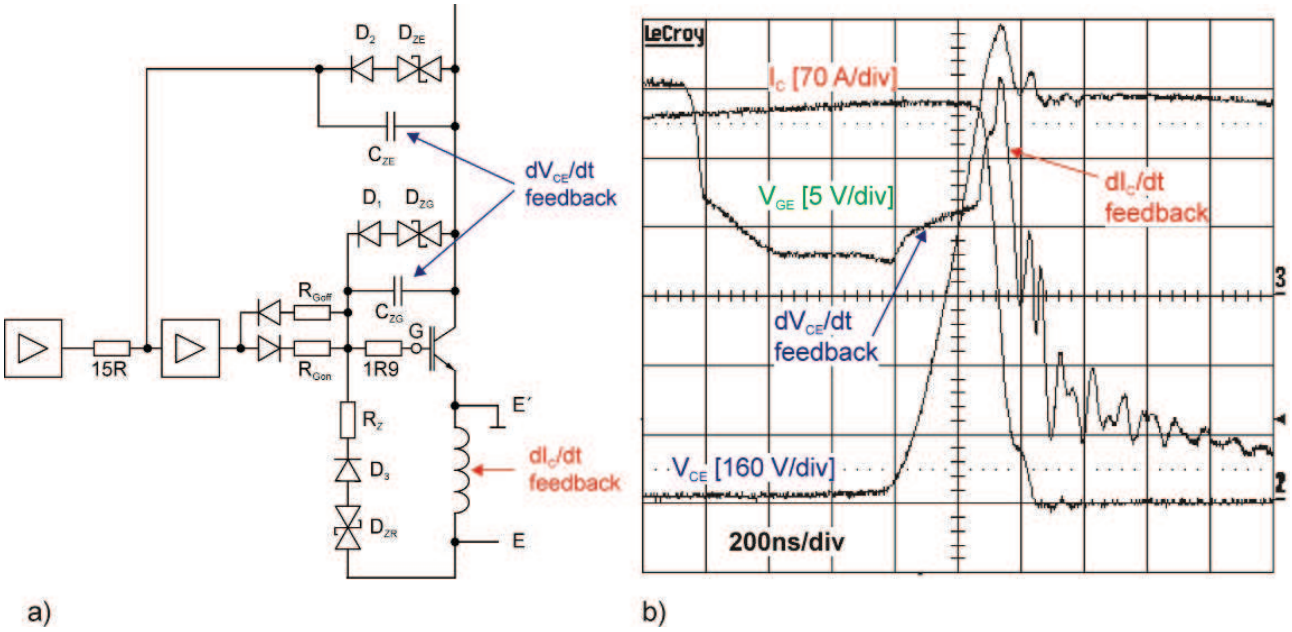


Figure 5.7.20 a) Overvoltage protection by means of combined active clamping and dynamic feedback
b) Oscillogram of a 1200 V Trench-Field-Stop IGBT turning off from overcurrent level at high DC link voltage with optimised dynamic feedback (V_D=900 V, I_C=400 A, V_{CE_peak}=1100 V)

The protective circuit depicted in Figure 5.7.20 uses a combination of active clamping and dynamic feedback. Active clamping and dv/dt feedback are executed consecutively, i.e. both gate and driver output stage are directly affected by protection. The dynamic behaviour may be controlled by suitable dimensioning of D_{ZE}, D_{ZG}, C_{ZE} and C_{ZG}. Feedback from di/dt is implemented by a small inductance (...nH...); the response threshold can be set via parameter D_{ZR}.

Overvoltage limitation between control terminals

Overvoltage limitation between control terminals is required to maintain the maximum gate-emitter / gate-source voltage, on the one hand, and limit the dynamic short-circuit current amplitude, on the other hand .
Figure 5.7.21 provides an overview of simplified passive circuits. To optimise efficiency, the limitation circuits should be designed for low inductance and be positioned as close to the gate as possible.
The use of fast Schottky diodes to clamp the gate voltage to the driver supply voltages has proven particularly efficient in switching applications.

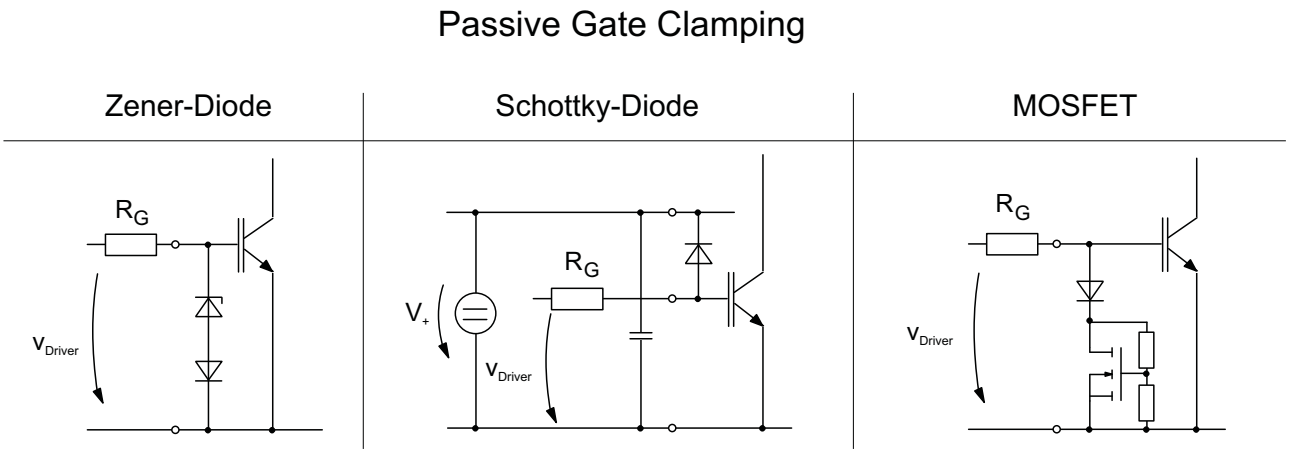


Figure 5.7.21 Simple passive gate voltage limitation circuits (passive gate clamping)

5.7.3.3 Overtemperature detection

Direct measurement of the junction temperature is only possible if the temperature sensor is positioned very close to the semiconductor component (e.g. by monolithic integration or by connecting the temperature sensor and the power semiconductor chip).
Frequently, temperature is detected by evaluating the temperature-dependent blocking current of a diode, thus serving as a temperature sensor. Technologies of this kind are used in smart-power components, for example.

In transistor power module applications, temperatures are measured either outside the module at the heatsink or inside the module using temperature-dependent resistors positioned close to the power semiconductor chips on the DBC substrate.
Owing to the given thermal time constants, this measurement provides filtered information on the temperature change only (highly dynamic temperature measurement is not possible).

5.8 Parallel and Series Connections

The chapters below are designated for IGBT with freewheeling diode. They may also, however, be applied to MOSFET, provided the connection/terminal designations are modified accordingly.

5.8.1 Parallel connection

Parallel connections are always needed when the performance of an individual component is insufficient. Paralleling begins at the microscopic level with some hundred thousands of individual IGBT cells, continues on the module level in the parallel chip connections and on the circuit level in the parallel connection of modules and entire inverter units.

5.8.1.1 Problems involved with current balancing

Maximum utilisation of the switch generated by parallel connection is only achieved in the case of ideal static (i.e. in conducting mode) and dynamic (i.e. at the moment of switching) current balancing. The cause of different distribution is either different output voltage in the parallel inverter phases or different branch impedance. This in turn is caused by differences in:
- power semiconductor on-state voltage;
- power semiconductor switching times and speeds;
- the signal propagation times of the driver outputs;
- DC link voltages;
- cooling conditions (e.g. due to thermal series connection in air-cooled applications);
- AC impedance (cable length or position) or
- DC impedance (DC link connection).

The larger the modules and assemblies, the more difficult it will be to achieve symmetry. The increased power and spatial expansion results in

- non-symmetrical current paths
- greater and, more importantly, unequal parasitic elements (stray inductances)
- greater interference fields
- steep current and voltage edges (especially di/dt) and
- varying temperatures in the semiconductor elements.

For this reason, in real applications with parallel module connection, great care must be taken when designing and optimising symmetrical layouts.

	Static symmetry	Dynamic symmetry
Semiconductors		
On-state voltage $V_{CEsat} = f(i_C, V_{GE}, T_j)$; $V_F = f(i_F, T_j)$;	x	
Transfer characteristic $I_C = f(V_{GE}, T_j)$ g_{fs}; $V_{GE(th)}$		x
Current path		
Impedance in the output circuit	(x)	x
Stray inductance in the commutation circuit L_s (inside the module + outside the module)		x
DC link voltage $V_{out} = f(V_{CC})$	(x)	
Driver circuit		
Output impedance driver (incl. gate series resistance)		x
Gate voltage characteristic $i_C = f(V_{GE}(t))$		x
Inductance L_E carrying emitter current inside the driver circuit		x

Table 5.8.1 Key factors influencing current distribution among parallel modules; (x) = quasi static

Static current distribution: influence of on-state voltage

The on-state voltage induced during stationary forward on-state is the same for both parallel components. Current distribution is dependent on the tolerances of the output characteristics. Figure 5.8.1 shows the distribution of the total load current to two parallel IGBT with different output characteristics.

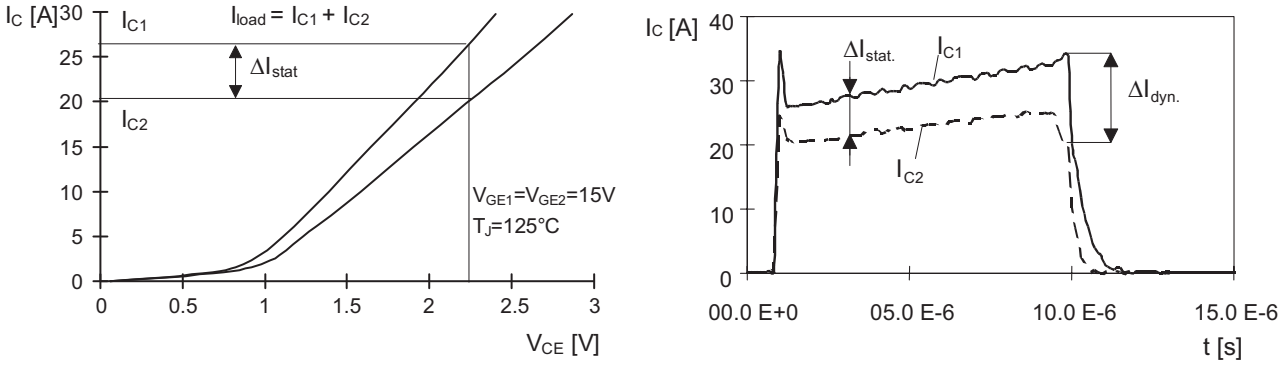


Figure 5.8.1 Stationary current distribution in two parallel IGBT with different output characteristics.

In the beginning, the major current share is conducted by the transistor with the lower on-state voltage, which is therefore subject to higher conducting losses, causing the junction temperature to increase rapidly. At this point, the temperature coefficient (TC) of the saturation voltage is of crucial importance. If the TC is positive, i.e. if the saturation voltage rises in line with increasing temperature, the current will be shifted to the transistor which had initially carried the smallest cur-

rent share. As a result, the current will (ideally) be evenly distributed across the parallel transistors. Power semiconductors with a positive TC are therefore the preferred choice for parallel connections. With a few exceptions, available IGBT technologies (NPT, SPT, Trench) all display a positive TC above around 10…15% of the rated current range. The same applies to the MOSFET R_{DSon}, which essentially has a high positive TC.

Freewheeling diodes, by way of contrast, have a negative TC across virtually the entire range up to rated current (Figure 5.8.2). An extremely negative temperature coefficient (> 2 mV/K) involves the risk of thermal overload for parallel connection of diodes, which always display a certain spread in on-state voltage owing to production processes. Take care that the variation in on-state voltage is as small as possible. In the case of considerable variation, selection may be necessary. Connection in parallel does not require any additional snubber circuit.

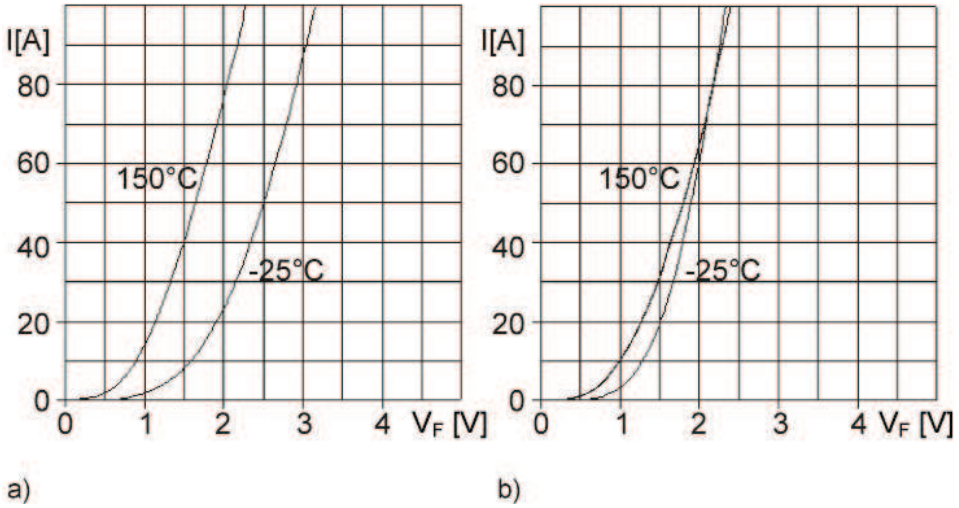


Figure 5.8.2 Temperature dependency of the on-state voltage for different types of diodes
a) highly negative temperature coefficient; b) positive temperature coefficient from rated current on (75 A)

The on-state characteristic of power semiconductors varies considerably from datasheet parameters. In relation to these values, a drastic limitation of the total current would result for parallel connection of one component at the lower specification limit (LSL) and a higher number of components at the upper specification limit (USL). This combination would be the worst case scenario, as the "good" diode has to conduct the biggest share of the current alone, while the many "poor" diodes barely conduct at all.

What can be verified, however, is that under static conditions, a case such as this would never occur [61]. The more parallel elements there are, the less probable the combination of a component from the lower specification limit with n-1 components from the upper specification limit is. Combinations of typical components would alleviate this problem and relieve the component with the smallest on-state voltage. Figure 5.8.3 shows an example of the static V_F distribution of 125,000 diode chips (a) and the probability of a combination of the diodes at the specification limits (b). The probability drops for 4 components below 10^{-20} already and, technically speaking, is no longer relevant.

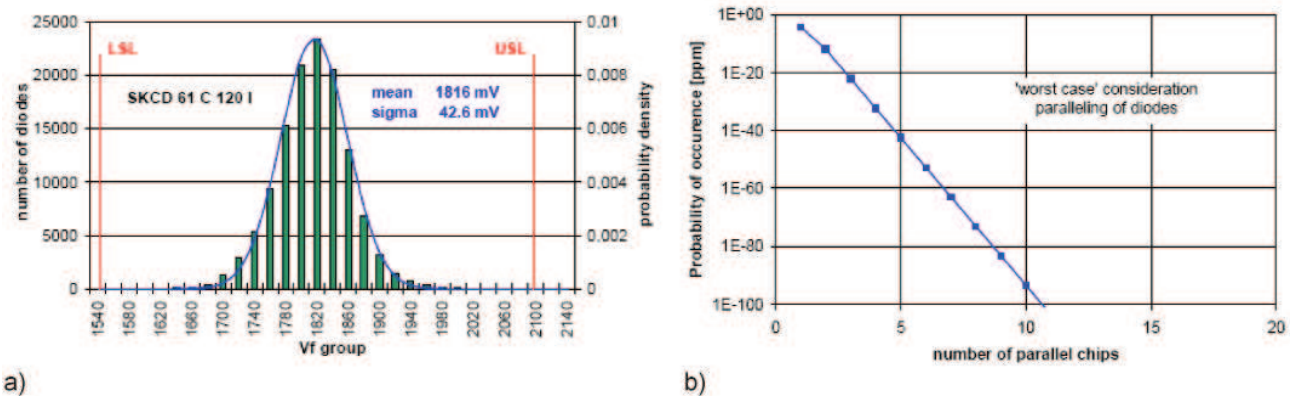


Figure 5.8.3 a) Statistic distribution of diode voltage Vf @ 50 A for 125,000 diode chips;
b) Probability of combination 1 x LSL and (n-1) x USL chips for n parallel chips

Paralleling is therefore no longer a problem in pure technical terms, but is rather a statistical and commercial problem, i.e. "What probability level is still acceptable?" Assuming an acceptable probability of 1:1 m (1 ppm), V_F limits can be calculated as follows: What diode combinations of 1 x LSL and (n-1) x USL of the V_F spectrum have a probability occurrence of 1 ppm? While for 2 diodes with upper distribution the variation is still 270 mV, the variation for 5 diodes is as little as 130 mV (Figure 5.8.4a). This conclusion also means that it is possible to calculate that, in order to consider the maximum load caused by the static asymmetrical current induced by the semiconductor, a current reduction of 10% is sufficient (red characteristic in Figure 5.8.4b). On the basis of the maximum current that a single USL diode can conduct, even bigger currents are possible for a greater number of parallel diodes, since the on-state voltage of the diodes will increasingly approach the statistical mean value.

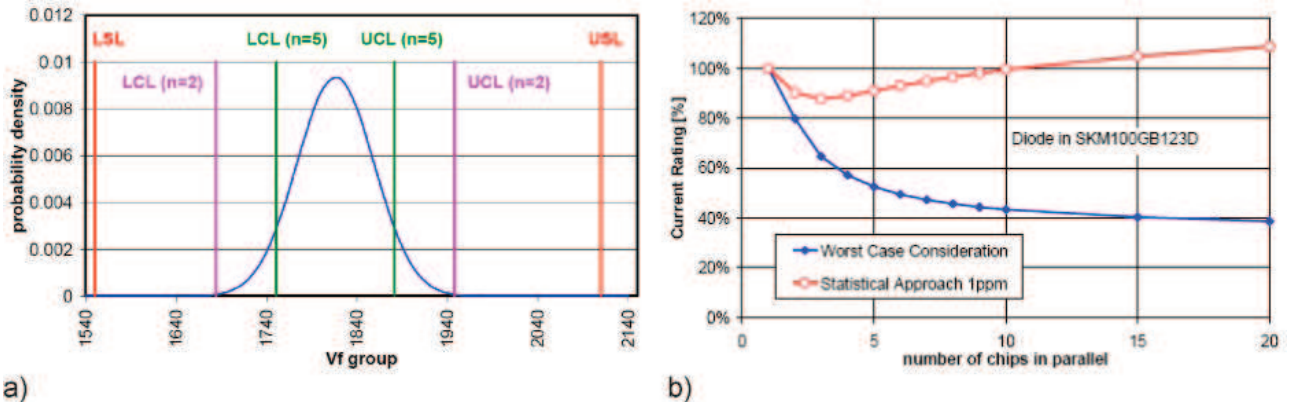


Figure 5.8.4 a) Occurrence of diode combinations of one diode from the LCL with n-1 components from the UCL with a probability of 1 ppm; b) comparison between possible current utilisation under "worst case scenario" conditions with the USL / LSL and current from a statistical point of view

Dynamic current distribution 1: Capacitances and transfer characteristic

A parallel circuit test was performed to examine the influence of the semiconductor capacitances. The variation for a random selection of components can be seen in Figure 5.8.5a. Statistic distribution resulting from production tests do not exist. The maximum deviation is +/- 5%. No differences in the switching properties of the parasitic components were ascertained. For this reason, in a further test 4.7 nF was connected externally between the gate and emitter of one of the parallel IGBT (=C_{GE} + 20%). The differences recorded were still minimal. The conclusion that can be drawn from this is that differences in the low-signal capacitances have a minor impact only on current symmetry during switching.

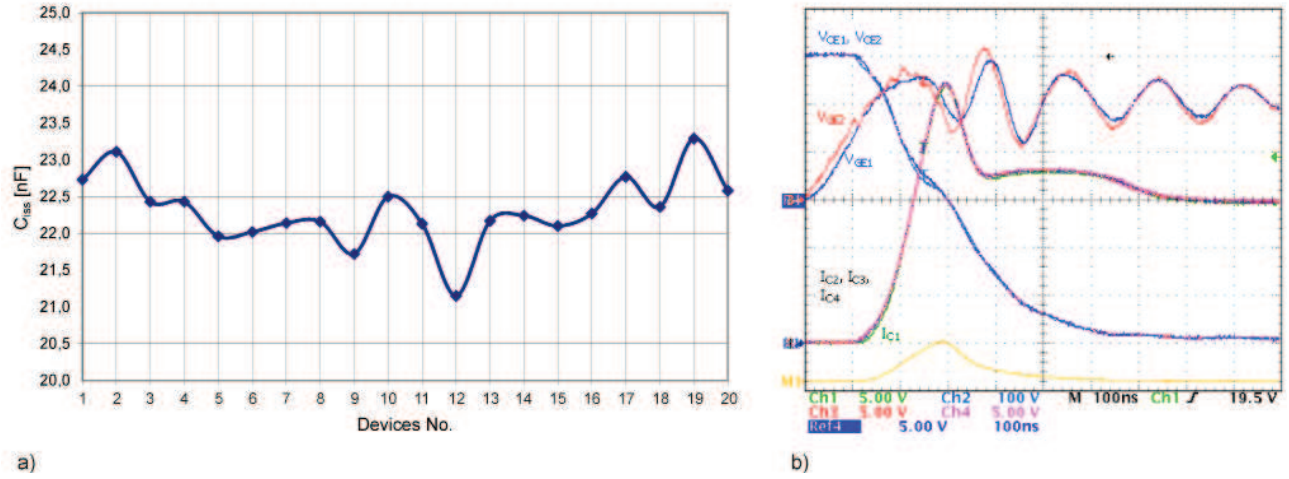


Figure 5.8.5 a) Variation recorded for input capacitance C_{ies} of a selection of 450 A Trench2 IGBT modules; b) Switching test with 4 parallel modules (turn-on) with an additional 4.7 nF external capacitance between module gate and emitter

In contrast, differences in the transfer characteristics lead to dynamic asymmetry in the moment of switching and thus to different switching losses. IGBT of the latest generations display relatively low variations in transfer characteristics (Figure 5.8.6). For hard parallel connection of the gates and the resultant common gate voltage, residual differences cause the IGBT with the steeper transfer characteristic to take up the biggest current during the Miller phase, meaning this IGBT also has the biggest switching losses. The threshold voltage $V_{GE(th)}$ has a negative temperature coefficient TC, while the slope of the characteristic g_{fs} has a positive TC. Depending on the operating point, this can result in a positive feedback or negative feedback effect with the junction temperature. Decisive for current asymmetry during switching is the plateau voltage $V_{GE(pl)}$ which is induced during the switching process as a horizontal line of the gate voltage.

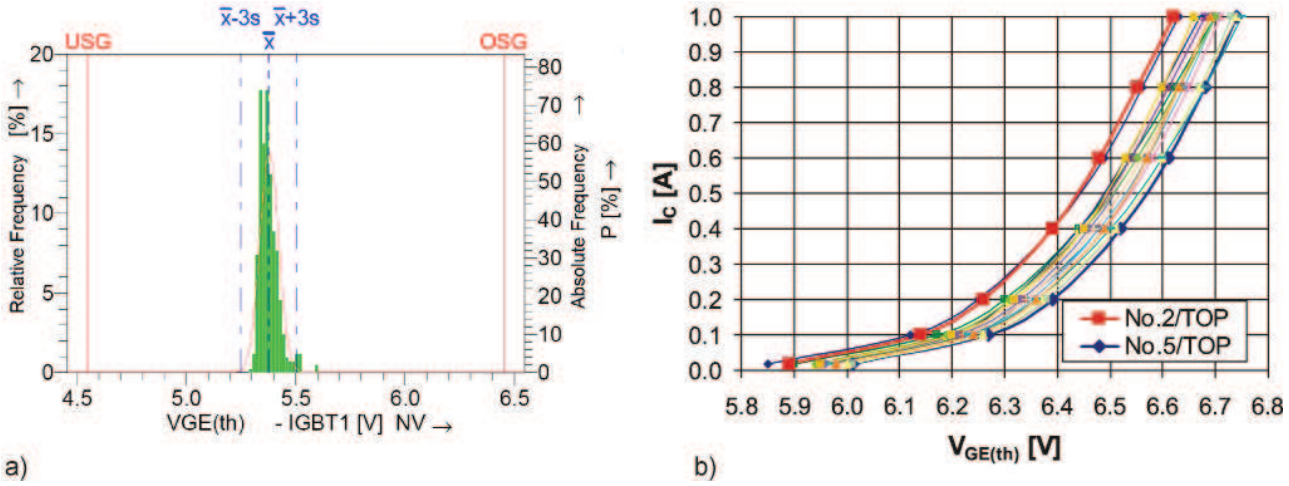


Figure 5.8.6 a) Distribution of the threshold voltage of 800 Chips (@ 4 mA, 25°C) with the specification limits (LSL and USL); b) Measurement of the transfer characteristic of various modules in the threshold voltage range for the extreme value selection for parallel switching tests

In a switching test [62] with 6 parallel SEMIX modules, the influence of the different transfer characteristics was examined. For this purpose, the two components with the biggest variation in plateau voltage were placed at the outside of the configuration (Figure 5.8.7: Pos. 1 + Pos. 6; $V_{GE(pl)}$ +/- 100 mV) and typical components in the centre (Pos. 2-5). The circuit is driven by a common driver unit; to the front right in the image. The IGBT modules are all dynamically "decoupled" by their own gate and auxiliary emitter resistances, as explained below. This induces values for $V_{GE(pl)}$ in the modules that are relatively independent of one another. For this test. the AC terminal is symmetrical and fed back to the DC circuit centrally between modules 3 and 4 (green arrow) beneath

the entire set-up. In comparison to this, the following paragraph looks at the influence of an asymmetrical AC cable connection.

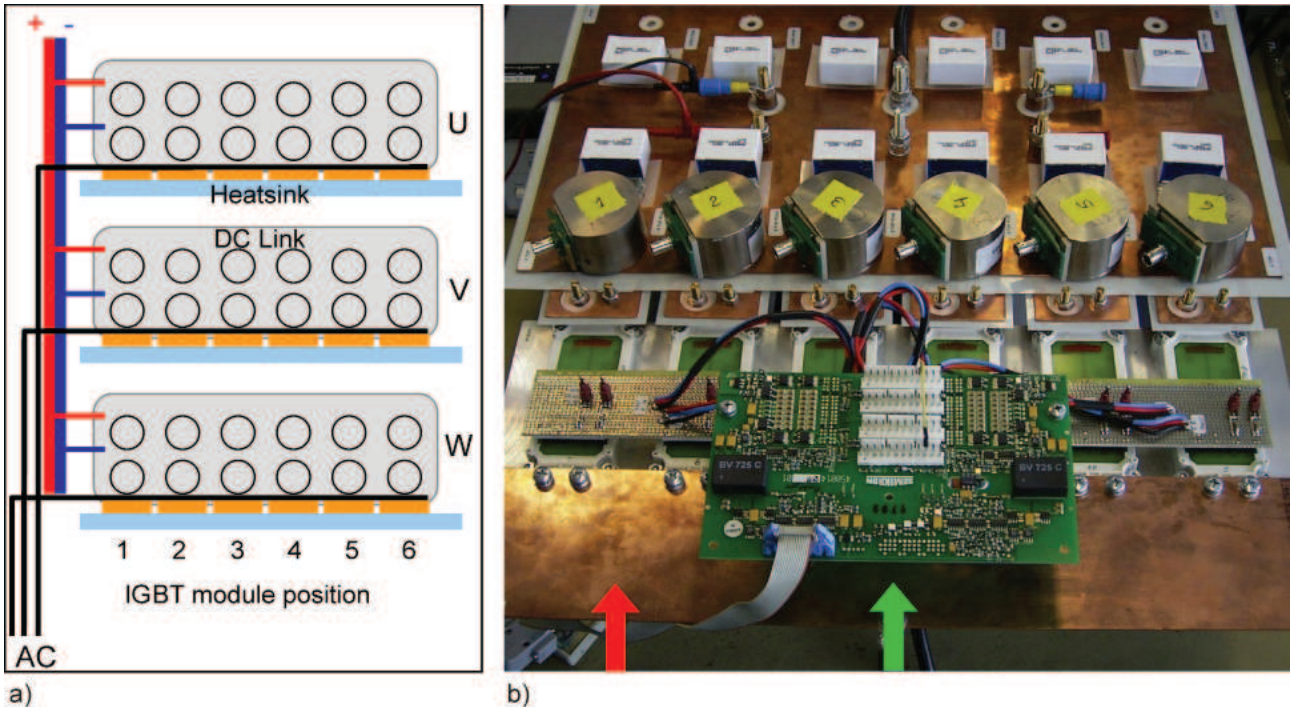


Figure 5.8.7 a) Diagram showing an inverter set-up with 6 parallel modules per phase and asymmetrical AC terminal position; b) Test set-up with 6 x 450 A SEMiX modules (driver unit can be seen at the fore; in the background the DC link circuit featuring Pearson converters for current measurements and snubber capacitors)

In the switching test, the measured peak currents during turn-on are compared in order to provide a yardstick for the differences in percentage in turn-on losses. Theoretically, the IGBT in the centre should conduct the biggest current, since they have the lowest impedance to the AC interface (green arrow). But in fact, the component in position 1 that displays the lowest plateau voltage has the biggest current. The maximum deviation is +10%-12% in relation to the mean value. A similar situation occurs during turn-off: the component with the lowest plateau voltage switches last and takes up the current from the other components. Consequently, here too the switching losses of this component are highest.

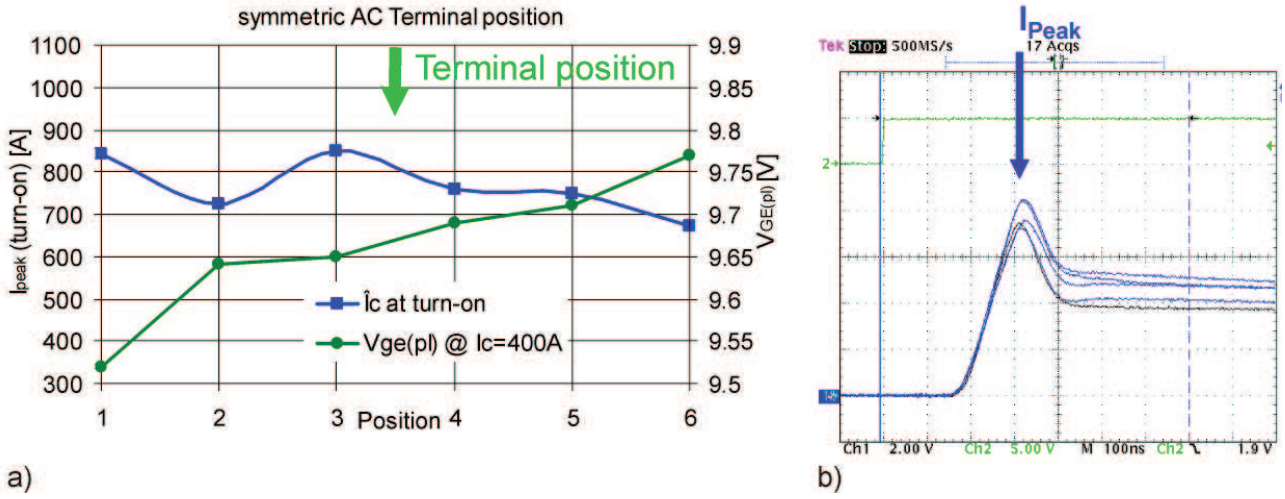


Figure 5.8.8 a) Current peaks for symmetrical AC terminal position (blue, left Y-axis) and plateau voltage of the modules (green, right Y axis); b) measured turn-on current peaks in double pulse with inductive load and 400 A per module (200 A/Div)

Dynamic current distribution 2: Loop or branch impedance

The aforementioned test set-up used to investigate the influences of the plateau voltage was adapted and the AC terminal is asymmetric and attached at the side (Figure 5.8.7 red arrow). The rest of the test set-up remained unchanged.

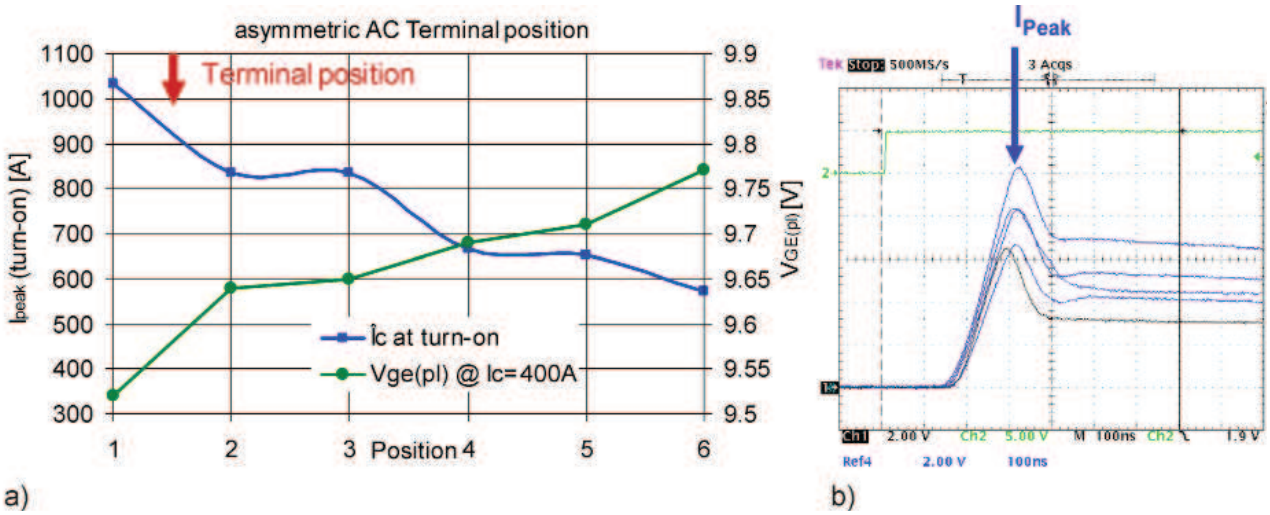


Figure 5.8.9 a) Current peaks for asymmetrical AC terminal (blue, left Y-axis) and plateau voltage of the modules (green, right Y-axis); b) measured turn-on current peaks in double pulse with inductive load and 400 A per module (200 A/Div)

The differences in the turn-on peak currents starkly increase. The deviation from mean value is +34% / - 24%. This is three times higher than can be accounted for by the different transfer characteristics. The influence of the terminal position dominates. The problem for the user is that even a centre cable connection which runs sideways away from the modules has the same effect as a cable positioned laterally. Cables fed from the centre outwards are often difficult to access for maintenance and repairs. Differences in branch impedance result in different output currents in the inverter phases, even in quasi static conditions.

Dynamic current distribution 3: Impedance in the driver circuit

Existing deviations will lead to non-simultaneous switching and will contribute to unbalanced distribution of switching losses. In combination with transistor input capacitances, the driver circuit loop inductance can generate heavy oscillations, which might even spread between parallel transistors. Fast changes in the emitter current ~ I_C during switching will induce voltages across the driver circuit inductance L_{E1}, where the main current is conducted. These can be counteractive to (negative emitter feedback) or boost (positive feedback) the gate charge or discharge process. This is one of the most critical effects on dynamic current distribution. Even just 1 nH will cause a voltage difference of 1 V for 1 kA/µs.

For modules with auxiliary emitter, L_{E1} is inside the case, meaning it cannot be influenced by the user. The main and driver circuit are largely decoupled. For IGBT with smaller rated currents without additional external auxiliary emitter the user can improve symmetry during switching by using symmetric negative feedback in the emitter current path to balance the switching speeds. When dimensioning, what should be taken into consideration is that the resultant deceleration of the switching process produces greater switching losses. In Figure 5.8.10 the voltage conditions are shown for different track arrangements during turn-on.

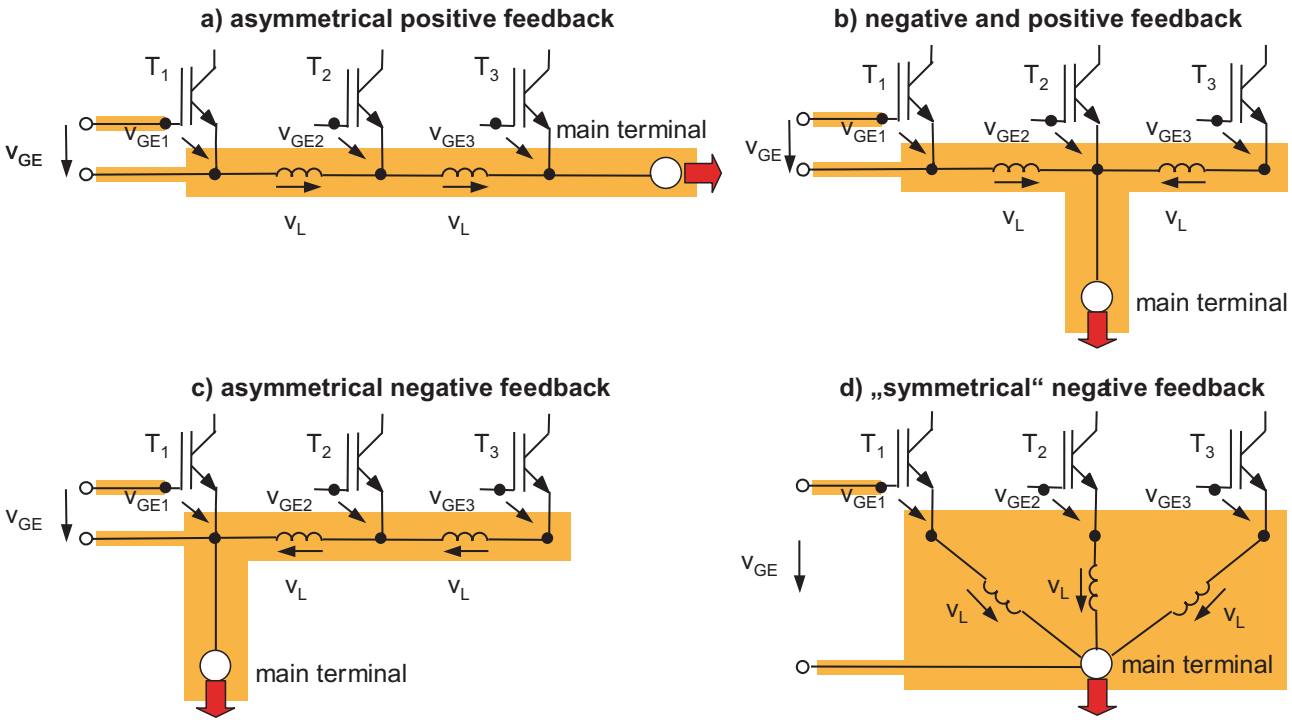


Figure 5.8.10 Examples of positive and negative main current feedback in the driver circuit

Example a) shows different degrees of positive feedback, causing transistor T_3 to turn on **more quickly** than $T_1 \cdot v_{GE3} = v_{GE} + 2 \cdot v_L > v_{GE1}=v_{GE}$.
In example b) T_2 has positive feedback and T_3 negative feedback
$v_{GE2} = v_{GE} + v_L > v_{GE1} = v_{GE} > v_{GE3} = v_{GE} - v_L$.
In example c) different degrees of negative feedback occur, causing transistor T_3 to turn on **more slowly** than $T_1 \cdot v_{GE3} = v_{GE} - 2 \cdot v_L < v_{GE1}=v_{GE}$.
In example d) all of the transistors have approximately the same amount of negative feedback amounting to $v_{GE1} = v_{GE2} = v_{GE3} = v_{GE} - v_L$; as a result, they will switch largely **synchronously**.

Dynamic current distribution 4: Commutation inductance

As explained in chapter 5.4 (power layout), commutation circuit inductance L_s affects the semiconductor turn-on losses (turn-on loss reduction) and turn-off losses (generating switching overvoltage). The commutation circuit basically includes the inductances between the semiconductors and the DC link capacitors. If commutation circuits are subject to different loop inductances, the switching speeds of fast power semiconductors may be different, resulting in dynamic asymmetry which has more impact than variations in semiconductor parameters. Even slight differences in this inductance might lead to asymmetrical distribution of switching losses and oscillations between the semiconductors. For this reason, the commutation circuit layout must be as symmetric as possible (current paths must identical in length and enclose the same areas).

Different switching speeds cause loop currents in the conductor loops from the short circuited auxiliary emitter and main emitter. They result in a rapid change in the emitter potential of individual switches and might, under certain circumstances, overload the thin auxiliary emitter terminal.

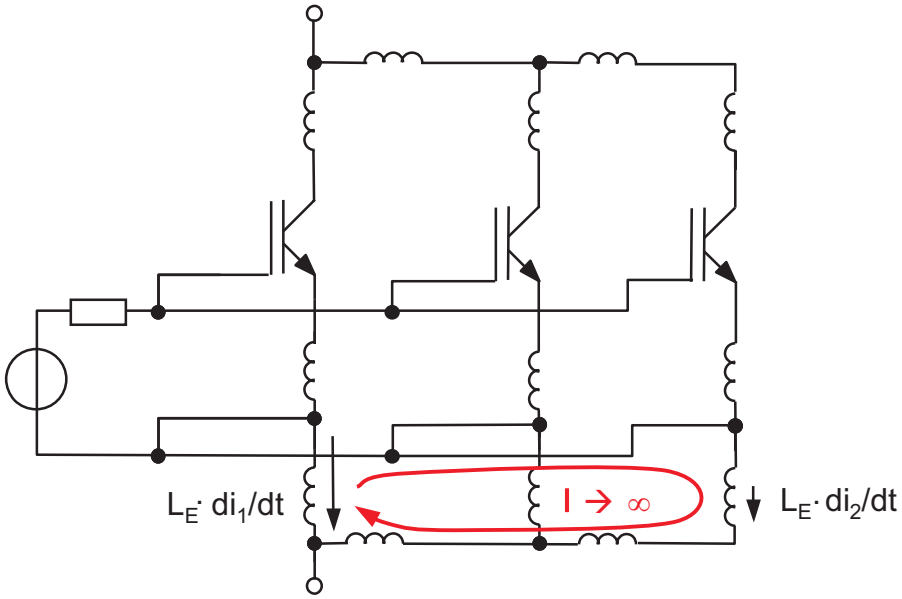


Figure 5.8.11 Different di/dt caused by differences in commutation inductances and the resultant high induced current loop

5.8.1.2 Ways of improving current symmetry

The following driver and layout tips for parallel IGBT and MOSFET configurations can be derived from chapter 5.8.1.1:

Driver

Figure 5.8.12 contains a possible driver set-up for parallel IGBT connections. The circuit is driven by a single, common driver unit. Twisted pairs that are identical in length or identical-length PCB tracks and minimum tolerance for the gate resistances (1%) are needed.

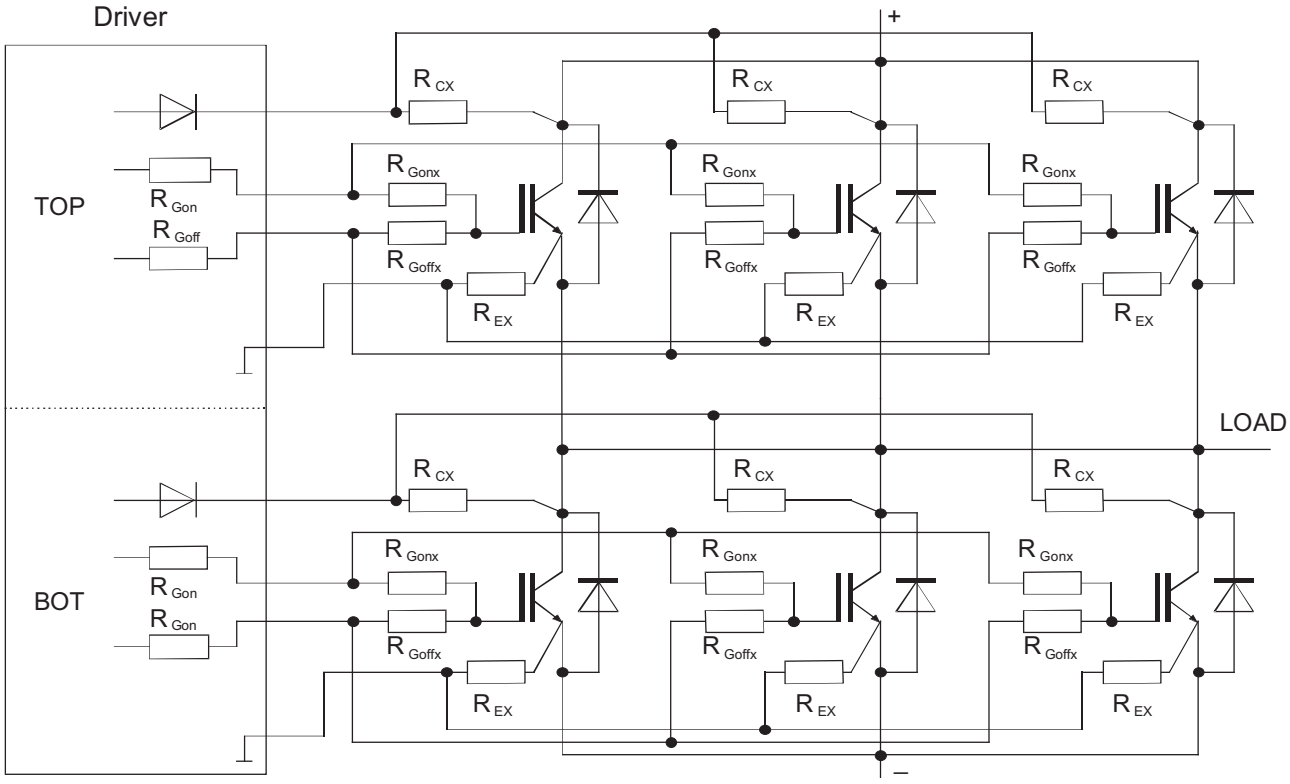


Figure 5.8.12 Parallel connection of IGBT modules

In addition to the common gate series resistances R_{Gon} and R_{Goff} integrated into the driver, the individual circuitry per transistor / module with the resistances R_{Gonx} and R_{Goffx} attenuate parasitic oscillations between the gate-emitter circuits. More importantly, however, they reduce the effects of different gradients in the transfer characteristic. The individual gate resistances may result in different plateau voltages at the moment of switching (Figure 5.8.13). As a result, one component with a flatter transfer characteristic turns on only with a slight delay of Δt_1. In a hard clamped gate, the component with the lower $V_{GE(pl)}$ would first have to turn on fully and V_{GE} rise to the point when the component with the higher plateau voltage can turn on (Δt_2).

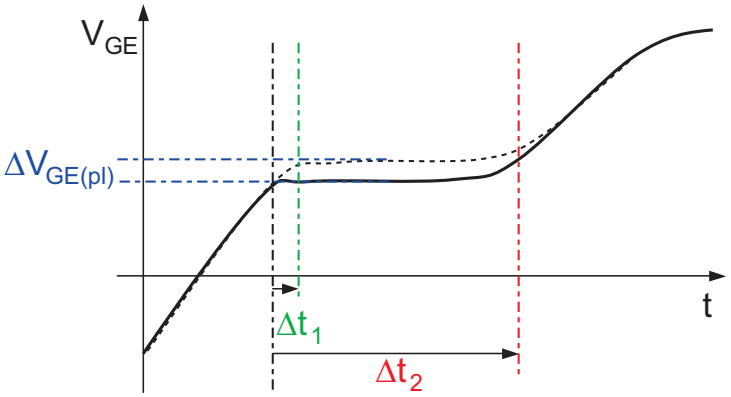


Figure 5.8.13 Gate voltage characteristic for parallel components with individual gate series resistances

Resistances R_{Gonx} and R_{Goffx} should be at least 50% of the gate resistance. Resistances R_{Ex} suppress loop currents across the auxiliary emitters. These are to be dimensioned with approx. 0.5 Ω. The voltage drop across the resistors works against current edges with different slopes (Figure 5.8.14). A higher induced voltage (black) across the emitter inductance of the fast IGBT ensures that a loop current flows through across the auxiliary / main connection. During turn-on, the voltage drop V_{Rex1} (green) induces a reduction in gate voltage in the fast IGBT $v_{GE1}=v_{GE}-v_{Rex1}$. In the slow IGBT, the gate voltage (blue) increases $v_{GE2}=v_{GE}+v_{Rex2}$. The switching speeds of the two IGBT consequently level up. This measure produces symmetry at the edges only; it does not balance the diverging of the currents during the plateau phase.

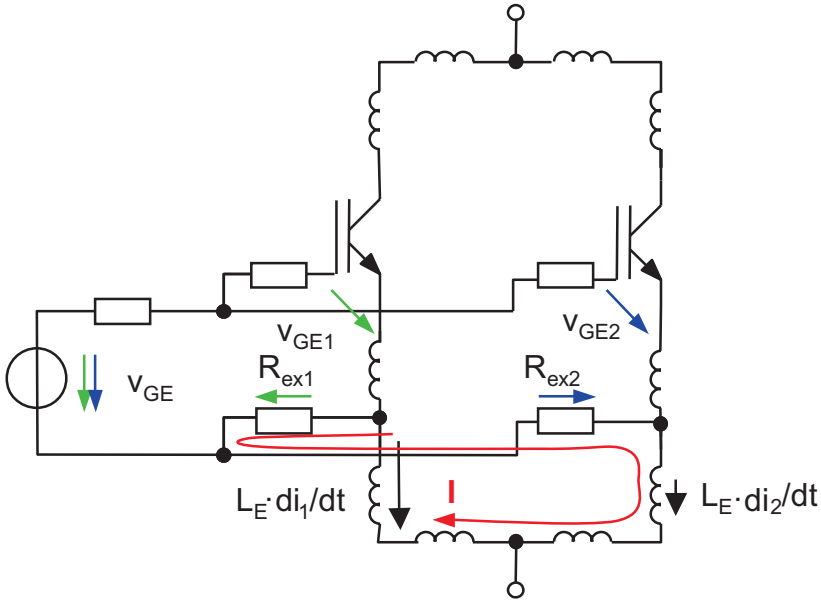


Figure 5.8.14 Balancing effect of R_{ex}; voltage drop across emitter inductance L_E causes loop current

The effective total gate resistances of the individual switch is calculated, for example for turn-on, as follows:

$$R_G = n \cdot R_{Gon} + R_{Gonx} + R_{Gint} + R_{ex}$$

n: Number of parallel components; R_{Gint}: Internal gate resistance

If overcurrent and short circuit protection is implemented on the basis of V_{CEsat} evaluation, the resistances R_{Cx} are used to determine the actual value for V_{CE}. These resistances are to be dimensioned with approximately 47 Ω. Often it is enough to take a measurement from one switch only.

Owing to the different signal propagation times, we do not recommend driving parallel transistors using separate driver circuits. A jitter-free driver does not exist, since output-stage transistors have a variation of 10 ns in the switching times. On top of this, differences exist in signal propagation times in the cables, as well as in the potential isolation. The advantage of a solution like this is the separation of the induction loops at the emitter, meaning that R_{ex} is no longer necessary. If this should still be necessary, however, measures such as those described in chapter 5.8.1.4 for SKiiP are to be implemented.

Module selection

In terms of semiconductor parameters, module selection is not necessary. However, several parameters influence current symmetry and can amount to a considerable cumulative effect, meaning that each individual factor should be reduced to a minimum. Thus, for larger assemblies it might make sense to select on the basis of the on-state voltage of the freewheeling diodes. Here, non-standard variants with purpose-selected diodes with a variation in V_F of 150…200 mV are needed.

Circuit layout

All power and driver circuits within the parallel circuit have to be laid out with minimum parasitic loop inductance and strictly symmetrical wiring. The need for symmetry applies not only to the length of the connection to the common AC terminal (branch impedance) but also to the current path from the semiconductor to the DC link capacitors (commutation inductance). Small capacitors with identical number per module and the same clearances between module and capacitor connections are needed for this. The emitter inductances are to be kept small, since they ensure rapid potential change in the driver voltages during switching.

Cooling conditions

Good thermal coupling between parallel modules must be ensured. In modules with internal parallel layouts, coupling is achieved by way of the substrate or the base plate and in parallel modules via the heat sink. Modules are therefore to be mounted close to one another on a common heatsink with good thermal coupling properties (also for reasons of symmetry of the inverse and freewheeling diodes). In large parallel systems with several heat sinks - especially air-cooled systems - thermal stacking is to be avoided. (see chapter 5.3). A temperature difference of 10°C means as much as 20 mV difference in on-state voltage for identical diodes. The hotter diode takes up even more current, further increasing the temperature difference.

Symmetry in DC link voltages

To avoid differences in the DC voltages of parallel capacitor banks (→ different output voltage despite identical switching times), these should be connected hard. Take care that during switching no oscillations between the capacitors occur (LC circuit). In large systems (MW), DC fuses ought to be used between the capacitor banks in order to limit the energy that flows into the short-circuit point in the event of a short circuit. Parallel systems have to be identical in terms of design; in addition, same-type and same-rating capacitors must be used.

5.8.1.3 Derating

Ideal static and dynamic symmetry is not feasible - even for optimum module selection, driver and layout conditions. That is why, with regard to the total rated load current of the switches, derating has to be factored in. On the basis of practical experience across a wealth of applications, as well as the aforementioned factors influencing static and dynamic semiconductor parameters, a minimum derating of 10 % is recommended. A semiconductor that can conduct 100 A as a single component should therefore be rated for a current of 90 A in parallel configurations. In asymmetric assemblies, the differences in the current of parallel components may be much greater. In some cases, balancing inductances will be necessary (see the section below on SKiiP).

5.8.1.4 Specifics of parallel connections for SKiiP modules

With regard to symmetry, cooling conditions and derating, the statements made above likewise apply to SKiiP. One difference in SKiiP modules is that the semiconductors and the driver circuits are integrated into a single case. Synchronous switching using one common gate signal cannot be guaranteed owing to the different driver signal propagation times. To be able to implement SKiiP parallel connections, the following conditions must be met on the driver side:

- synchronous setting of the switching signals including external locking time, where necessary controlled delay of switching commands as active current balancing measure;
- common error management for all connected systems with a common OFF signal;
- separate monitoring of the sensor signals for current and temperature;
- common auxiliary current supply for all connected systems.

The user can influence symmetry by way of the power layout (inductances, cooling system) . In addition, active current balancing via the switching signals is recommended. To ensure that parallel SKiiP modules are not subject to thermal overload, the effects of the existing differences could be reduced to a minimum by way of sufficiently large external inductances between the AC terminals of the parallel SKiiP modules. Nonetheless, we still recommend derating for the theoretical converter power. This is necessary because, regardless of what steps are taken, current asymmetry is unavoidable. The 10% derating value recommended above is intended as a guideline only and should be monitored by analysing the current sensor signals.

Signal propagation times and switching speeds

Here, current diverging at the moment of switching and extremely different switching losses are prevented thanks to external inductances (Figure 5.8.15). As soon as one of the two IGBT switches, the DC link voltage will be applied over the parallel connection for a moment (t_1-t_2) until the second IGBT has switched, too. The external inductance prevents commutation of the entire output current I_{out} to the "slower" SKiiP, as well as oscillations between the SKiiPs. As regards driver signal jitter, one can assume that for one period of output frequency, the switching occasions are evenly distributed. This means there is no need to be concerned about any influence on the effective output current, at least over the long term. Loop currents are caused by permanently displaced driver signals or semiconductor switching times (phase shift of fundamental frequency of output voltages). Once again, limiting is achieved by way of the inductance. To limit the current divergence, for example to 50 A for a max. jitter of 125 ns (SKiiP3) and a DC link voltage of 1200 V, the following inductance would be needed:

$$2 \cdot L_{min} = \frac{1200\ V \cdot 125\ ns}{50\ A} = 3\ \mu H\ ,$$

In other words, approx. 1.5 µH per SKiiP.

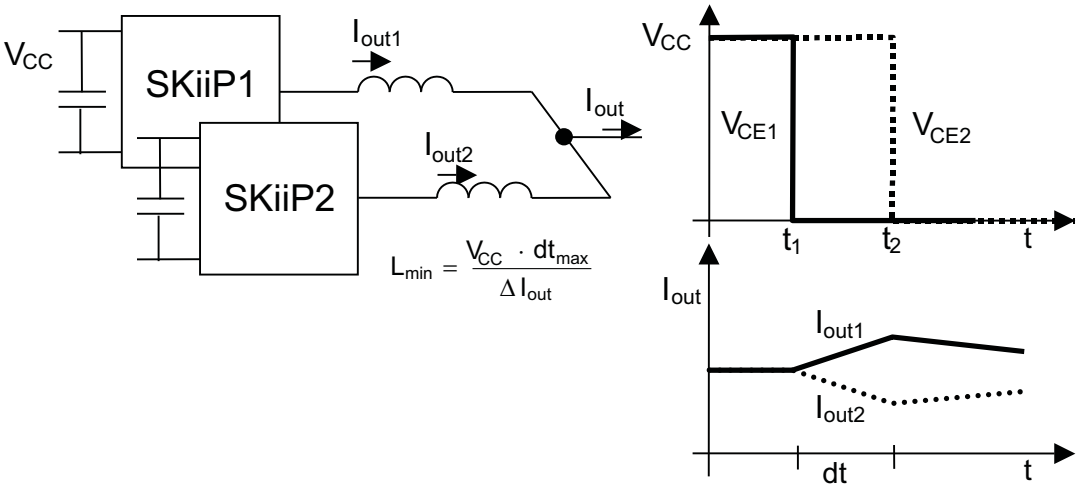


Figure 5.8.15 Dynamic decoupling of parallel individual modules using inductances in the load terminal paths

Branch impedance and on-state voltage of the semiconductors

Differences in the effective current are caused mainly by the branch impedance in the inverter phases. For identical output voltage (voltage-time area), the currents are distributed in inverse proportion to the branch impedance (Figure 5.8.16). For typical SKiiP IGBT on-state resistances of 1 mΩ, 100 µΩ difference in branch impedance means 10% current displacement. All of the IGBT used in SKiiP modules have a positive temperature coefficient of the on-state voltage. As a result of chip temperature coupling, this means that current asymmetry is "automatically" limited. The diodes used have a negative temperature coefficient, but are produced with very low tolerances in order to limit current asymmetry. For SKiiP3 and SKiiP4 modules, selection in groups of similar forward voltage is not needed. Existing current asymmetry can be reduced using an AC choke and their ohmic shares (choke and cable resistance). Low-frequency applications (< 5 Hz) are particularly difficult , however, since the inductive share is ineffective in practice.

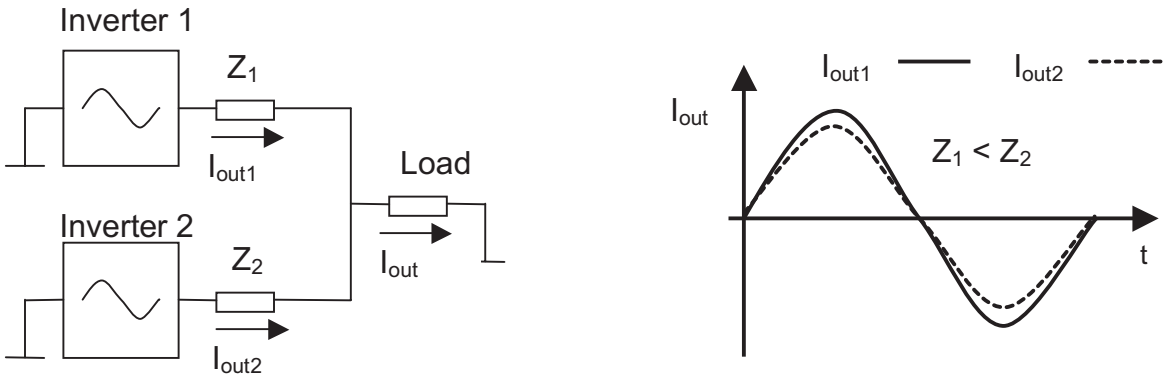


Figure 5.8.16 Abstract single-phase circuit diagram of 2 parallel inverter phases as a voltage source with branch impedance $Z_{1/2}$ and current asymmetry caused by differences in impedance

5.8.2 Series connection

Power semiconductors connected in series are uncommon without avalanche effect. Owing to
- additional losses caused by the n-fold diffusion voltage (on-state voltage);
- losses in the parallel resistor;
- the substantial charge that has to be taken up by the transistor during switching;
- the degree of complexity with regard to the components needed for the circuitry

series connections are seldom used for power semiconductors if a component specified for the higher voltage is available. One exception here might be cases where the on-state power losses do not play a major role and one is reliant on the short switching time and low switching losses in semiconductors of the lower voltage class. Far more common are circuits which in themselves work on a voltage level which is not critical for the individual semiconductor. Examples here are multi-level inverters with clamping diodes, flying capacitors or cascaded inverters. Provided clearances, creepage distances and dielectric strength in relation to ground are considered, these can be seen as individual switches with no series connections.

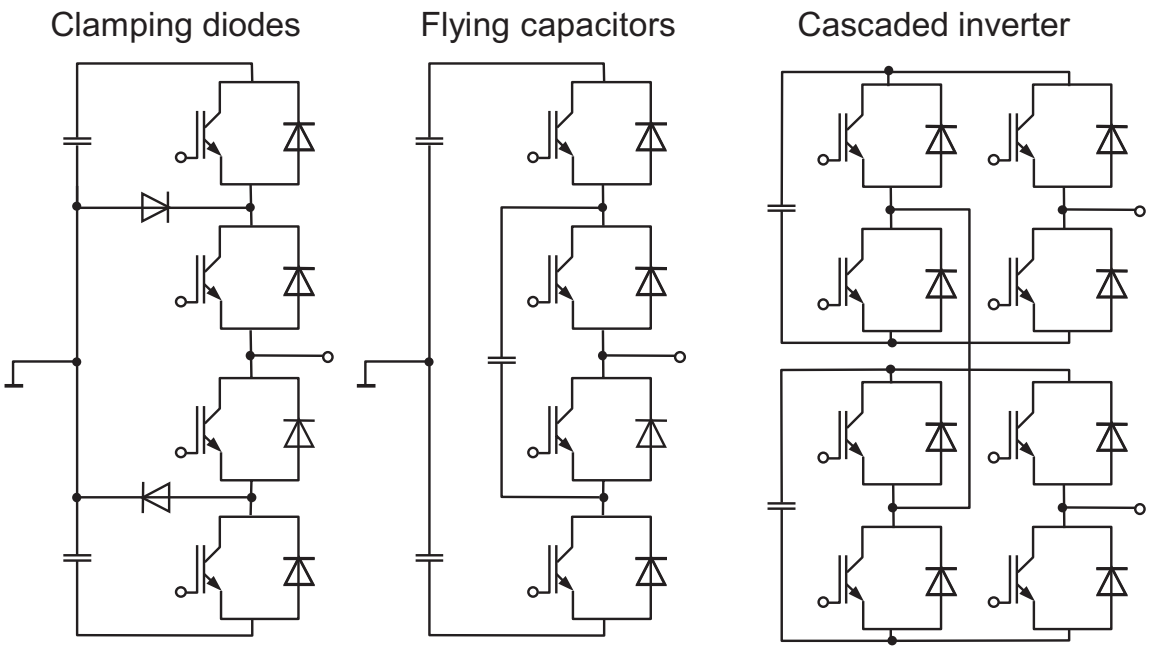


Figure 5.8.17 Examples of IGBT series connection without critical voltage distribution

5.8.2.1 The importance of voltage symmetry

To increase the blocking voltage of power electronic switches, IGBT modules may be connected in series. In module applications, series connection applies to both the transistors and the corresponding inverse and freewheeling diodes.

Maximum utilisation of the switch generated by series connection is only achieved in the case of ideal static (i.e. in blocking mode) and dynamic (i.e. at the moment of switching) voltage balancing among the individual modules. This is why, in real applications where series connection is used, it is crucial that symmetry be optimised.

	Static symmetry	**Dynamic symmetry**
Semiconductors		
Blocking current $i_{CES} = f(V_{CE}, T_j)$	x	
Transfer characteristic $I_C = f(V_{GE}, T_j)$ g_{fs}; $V_{GE(th)}$		x
Current path		
Total loop inductance (inside module + external)		x
Driver circuit		
Output impedance driver (incl. gate series resistances)		x
Gate voltage characteristic $V_{CE} = f(V_{GE}(t), T_j)$		x
Inductance L_E carrying emitter current inside the driver circuit		x

Table 5.8.2 Main factors influencing voltage symmetry in series-connected IGBT

Cause of static asymmetry

During stationary off-state, symmetry is determined by the blocking characteristic of the series-connected semiconductors. The bigger the blocking current or the lower the blocking resistance, the lower the voltage taken up by the series-connected semiconductor. The blocking current in-

creases exponentially to the increasing temperature. In stationary off-state, the variation in blocking current due to production processes will drive the components with the lowest blocking current into the region of breakthrough voltage. As long as the avalanche stability of the components can be relied on, no resistors will have to be connected. If, however, components with a blocking capability of > 1200 V are connected in series, it is common practice to use a parallel resistor.

Reasons for dynamic asymmetry

The factors influencing dynamic symmetry as described in Table 5.8.2 will all ultimately result in different switching times for the components connected in series. The factors influencing dynamic symmetry as described in will all finally result in different switching times for the components connected in series. The transistor that turns off first and the one that turns on last will be burdened with the highest voltage and, consequently, the highest switching losses. To prevent the maximum permissible semiconductor voltage from being exceeded, the countermeasures discussed in the following section must be taken. Essentially, dynamic voltage distribution may differ from static voltage distribution. If one of the pn-junctions connected in series is free of charge carriers earlier than the others, this will take up voltage earlier, too.

5.8.2.2 Ways of improving voltage symmetry

Optimum symmetry is essentially achieved by ensuring minor variations in the parameters of the modules in the series connection; for dynamic symmetry minimum differences in the signal propagation times for the driver stages are the key. Different types of modules or modules produced by different manufacturers should not be connected in series. The layout of power and driver circuits is basically to be done with a view to achieving minimum parasitic inductance and strictly symmetrical arrangements.

Static symmetry

To achieve optimum static symmetry, the influence of different blocking currents has to be decreased by using parallel-connected resistors. This resistor has to be dimensioned with respect to the fact that voltage distribution is always determined by the parallel resistance. If the blocking current is accepted as independent of the voltage and if resistance tolerances are neglected, the simplified rule for dimensioning the resistance for series connection of n diodes is as follows:

$$R < \frac{n \cdot V_r - V_m}{(n-1) \cdot \Delta I_r}$$

where

V_m: maximum voltage occurring across the entire series connection

V_r: maximum voltage which is to drop across a single semiconductor

ΔI_r: the maximum variation in blocking/leakage current

This is based on the maximum operating temperature. V_r is to be selected such that sufficient safety margin to the maximum reverse voltage of the component exists (e.g. < 66% V_{CES}). As regards ΔI_r, the following assumption can be made with a sufficient degree of certainty:

$\Delta I_r = 0.85\ I_{rm}$

where I_{rm} is specified in the datasheet. The series connection can now be optimised for n and R. Experience shows that for state-of-the-art power semiconductors it is sufficient to dimension the resistor such that at maximum voltage, it will carry current three times the maximum leakage current. However, even then considerable power losses are generated within the resistor. For IGBT modules with integrated antiparallel diode, the total leakage current of both components is to be given as I_{CES}. Here, too, the current conducted through the parallel resistor may be rated to about 3-5 times the transistor blocking current.

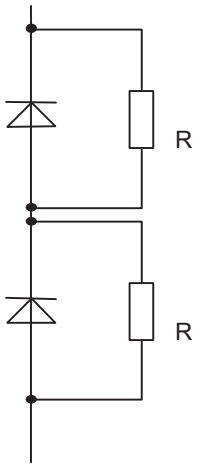


Figure 5.8.18 Resistor circuitry for static voltage symmetry of diodes in series connection

Cooling conditions

The semiconductors have to be mounted on a common heatsink close to each other to guarantee optimal thermal coupling. In large systems with several heat sinks - especially air-cooled systems - thermal stacking is to be avoided (see chapter 5.3). A 10°C temperature difference means 1.5…2.5-fold blocking current of identical IGBT, diodes or thyristors. The hotter semiconductor, however, takes up less voltage, which alleviates the temperature difference somewhat.

Dynamic symmetry using passive networks

To achieve dynamic symmetry, RC or RCD networks may be used (cf. Figure 5.8.19). These networks reduce and thus balance dv/dt speeds during switching (compensation of non-linear component junction capacitances). However, the high degree of reliability achieved using RC or RCD networks goes hand in hand with the need for more passive power components, which have to be designed for high voltages. Snubber networks are responsible for generating what in some cases are considerable additional losses. Furthermore, one disadvantage is the fact that the quantitative effect depends on the circuit operating point. That said, an important advantage is the fact that no additional control components are needed and standard driver stages can be used. If capacitor tolerances are neglected, a simple dimensioning rule can be used for this capacitor for series connection of n diodes of a specified reverse voltage $V_{r:}$

$$C > \frac{(n-1)\cdot \Delta Q_{RR}}{n\cdot V_r - V_m}$$

Here, ΔQ_{RR} is the maximum variation in diode storage charge. The following can be assumed with relative certainty:

$\Delta Q_{RR} = 0.3\ Q_{RR}$

provided diodes from one production batch are used. Q_{RR} is specified by the semiconductor manufacturer. When the freewheeling diode is turned off, the charge stored in this capacitor is generated in addition to the storage charge and also has to be taken up by the IGBT during turn-on. Based on these dimensioning rules, the resultant charge will be as much as twice the storage charge of a single diode.

If passive networks are combined with active balancing technologies, they may be dimensioned smaller in terms of parameters. In [63] and [64], a combination of active balancing and a passive RC network is shown. Here, the RC networks have R = 3.3 Ω and C = 15 nF at a DC link voltage of 2.4 kV for four series-connected 1200 V / 600 A IGBT switches.

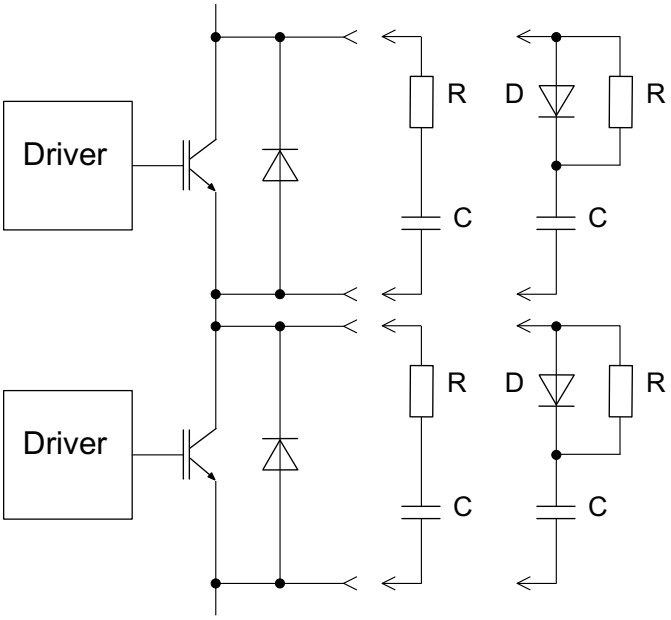


Figure 5.8.19 Passive networks for dynamic voltage symmetry

Active balancing measures; switching time correction

Figure 5.8.20 shows a possible way of achieving dynamic voltage symmetry using the principle of switching time correction based on delay time control [65]. No additional passive power components are needed for this process. No additional losses occur in the IGBT / MOSFET either.

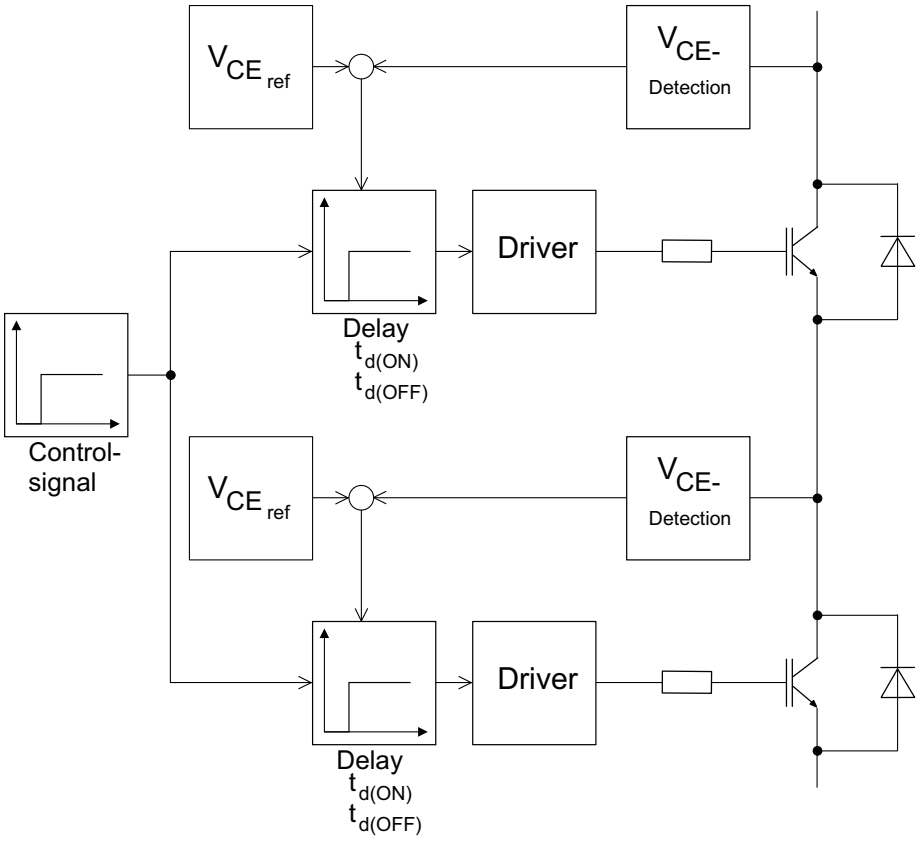


Figure 5.8.20 Principle behind switching time correction

Dynamic symmetry by way of dv/dt, di/dt control

In dv/dt control (Figure 5.8.21), reference value for the dv/dt speed of single modules during switching is compared to the actual values by the driver and the difference transmitted to the driver output stage. One problem here is the precise and reproducible capacitive coupling or feedback

of the actual dv/dt values. If the dv/dt reference value is lower than the "natural" dv/dt during hard switching, additional losses will be generated in the power transistors. Consequently, the driver layout has to be more sophisticated, and standard drivers may no longer be used. Similarly, di/dt control with inductive feedback of the di/dt speed of IGBT / MOSFET may be implemented [66], [67].

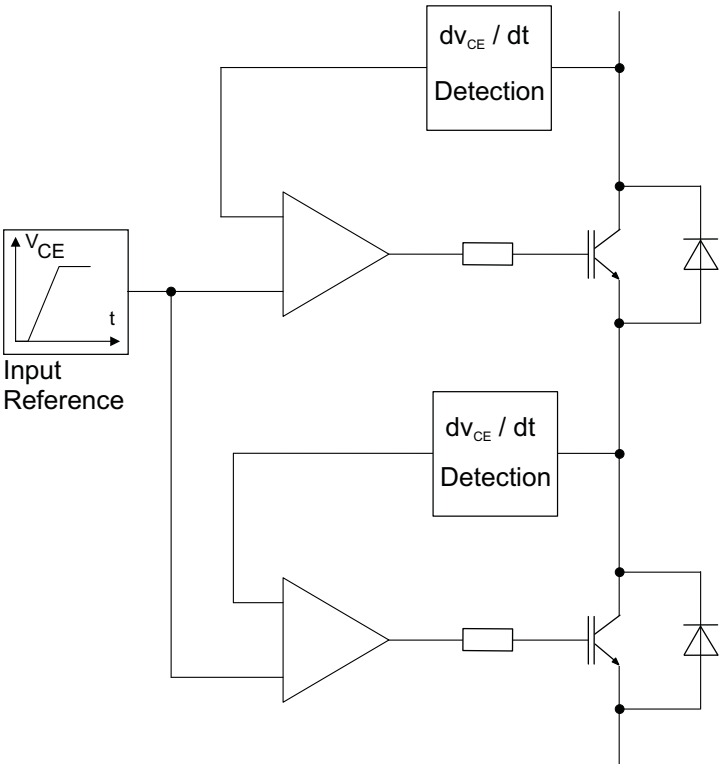


Figure 5.8.21 Dynamic voltage symmetry using dv/dt control

Active voltage limitation / active clamping

In the process of active clamping [64], [68], [69], [70] the collector-emitter voltage or drain-source voltage is measured and fed back to the gate via a Zener element (cf. chapter 5.7 "Active Clamping", Figure 5.8.22). If the transistor voltage exceeds the given maximum voltage, the gate voltage will be increased to such an extent that the operating point is shifted to the active region of the output characteristic in accordance with the collector/drain current that is flowing.

The additional losses generated in the transistor during active clamping are relatively low. Active clamping has no influence on the symmetry of the switching edges. This method works without time delays, the limitation voltage value being independent of the operating point of the inverter. A further advantage is the fact that almost any standard driver may be equipped with the clamping device and that active clamping will be performed automatically for antiparallel diode turn-off, too. Protection is guaranteed even in the case of driver supply voltage failure.

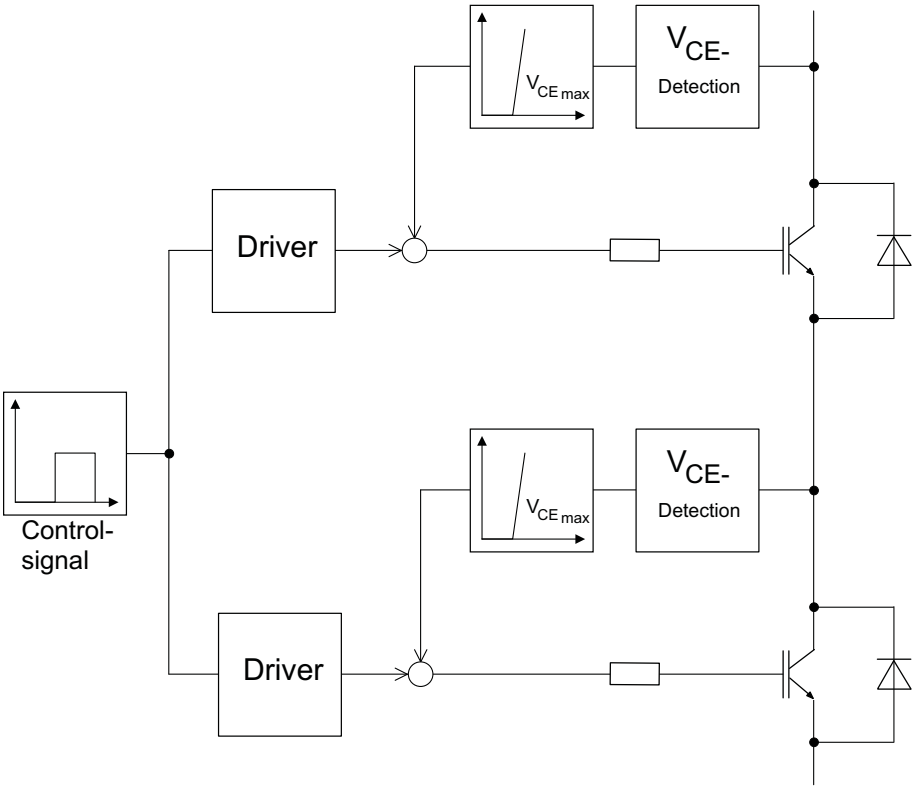


Figure 5.8.22 Active voltage limitation / active clamping

Master slave concepts

An adaptation of the commonly known master / slave principle, which originates from thyristor technology [71], can also be used to achieve dynamic voltage symmetry (Figure 5.8.23). Only the bottom switch (master) is equipped with a complete driver circuit with auxiliary power supply and potential-separated control pulse input. This is the major advantage of the principle. The driver circuit of the top switch (slave) integrates nothing but the output stage. The decoupling between master and slave is done by a high blocking diode. The slave will be turned on as soon as its emitter potential has dropped to a point where the decoupling diode is able to turn on, i.e. with a slight time delay. The slave is turned off by blocking the decoupling diode. In principle, several slaves may be connected in cascade. While this concept is able to achieve turn-off symmetry rather well, turn-on symmetry is very limited. For this reason, a combination of the master / slave concept and active clamping is recommended. The disadvantage of limited turn-on symmetry can be ignored in ZVS applications.

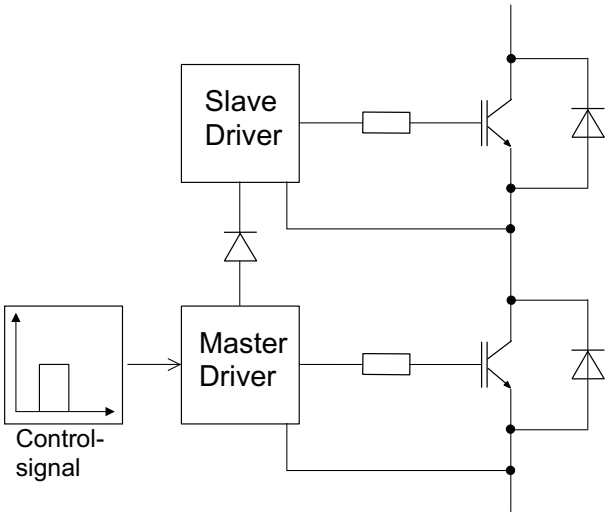


Figure 5.8.23 Basic principle behind the master / slave concept

5.8.2.3 Conclusions

In addition to the high-resistance parallel resistors for static symmetry, passive and/or active measures to achieve dynamic symmetry must be taken when IGBT or MOSFET modules are connected in series.

With the exception of active clamping, the methods shown here will protect the transistors only, meaning that additional passive networks will be needed to protect the inverse diodes.

5.9 Soft switching as ZVS or ZCS / switching loss reduction networks (snubbers)

5.9.1 Aims and areas of application

Industrial power electronic circuit engineering in the medium and upper power class range is dominated by topologies related to impressed direct voltages. In these circuits, IGBT and MOSFET are operated almost exclusively in hard switching mode, i.e. they are subject to high switching losses and power dissipation peaks, resulting in typical switching frequencies between 1 kHz and 30 kHz (IGBT) or 50 - 100 kHz (MOSFET).

Increasing the switching frequency will generally lead to reduction in size and weight of passive energy storage components (chokes, capacitors, transformers, filters), which is of interest, for example, with respect to the integration of transformers into converter systems.

Typical areas of application:
- Battery charging,
- UPS with potential-isolated DC-DC converter,
- electronic power supply units (switch-mode power supply) for general applications,
- PFC circuits,
- industrial power supply systems (welding, electroplating, inductive heating, x-ray, plasma, etc.).

If the required switching frequencies cannot be obtained in a hard-switch application, either interleaved technologies have to be used or the resulting switching losses have to be reduced. Basically, there are two ways of reducing switching losses:

1. Implementation of additional switching loss reduction networks, whilst keeping the basic circuitry (snubber circuit)
2. Soft switching as ZVS (**Z**ero **V**oltage **S**witch) or ZCS (**Z**ero **C**urrent **S**witch).

5.9.2 Switching loss reduction networks / snubber circuits

Power-electronic switches with conventional thyristors or GTOs require snubber circuits in order to guarantee operation within the safe operating area, i.e. these networks are indispensable if the components are to live up to their basic functions during switching. In contrast to this, the SOA characteristics of modern IGBT and MOSFET allow operation without the use of networks, meaning that additional networks may only serve to reduce switching losses or perform symmetry tasks in the case of cascading.

Figure 5.9.1 shows a conventional buck converter with IGBT and basic networks for turn-on and turn-off relief (reduction of switching losses).

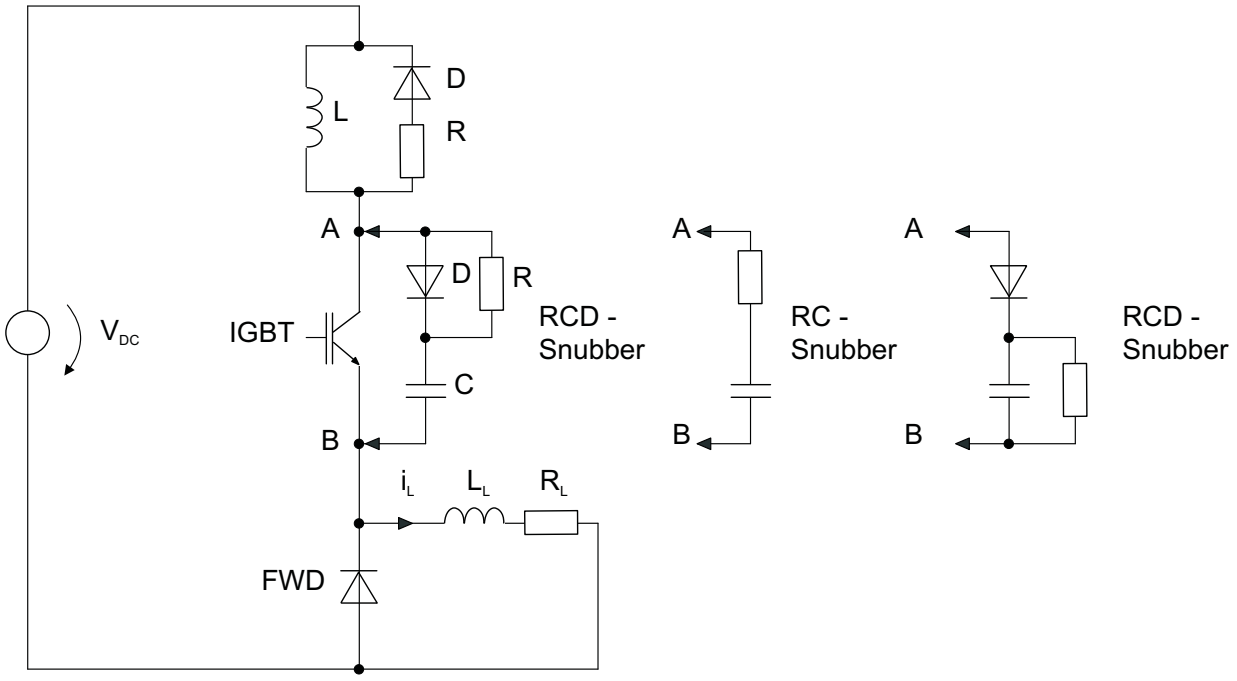


Figure 5.9.1 Buck converter with IGBT and basic switching loss reduction networks

Reduction of turn-on losses (RLD network)

To begin with, the IGBT is in off-state ($v_{CE} \approx v_{DC}$), and the load current is flowing in the freewheeling circuit.
Commutation from the freewheeling diode to the IGBT is started by active IGBT turn-on. As soon as the snubber inductance L has reached a certain value, it will take up the commutation voltage almost completely (this corresponds to the input DC voltage of the converter) when the collector current rises, meaning that the collector-emitter voltage is quickly reduced to a very low level. At the same time, the network inductance will bring about a reduction in the current commutation speed.
Together, these two factors lead to a substantial decrease in IGBT turn-on losses.
The characteristics of collector current and collector-emitter voltage correspond to soft switching as explained in chapter 1.
In chapter 5.9.3 it will be shown that the use of inductances with just some microhenry are sufficient to effectively reduce IGBT and MOSFET power losses.
In addition to the reduction of IGBT turn-on losses, the turn-off losses of the freewheeling diode will also be decreased during commutation, since the reduced current commutation speed will lead to low-level reverse recovery peak currents.
The combination of R-D will create a freewheeling circuit for the network inductance, which will limit IGBT and FWD overvoltages during turn-off.

Recommendations for dimensioning:

1. The network inductance should not to be dimensioned any bigger than needed for loss reduction,
2. Reduce the inherent (internal) capacitance of the snubber inductor to a minimum,
3. R and L form the time constants (t = L/R) necessary for internal energy discharge in the inductor. This results in a minimum IGBT static off-time (duty cycle limitation) to achieve efficient reduction of turn-on power losses (no residual current in L). On the one hand, increasing R will reduce the minimum IGBT static off-time; on the other hand, however, it will lead to a higher voltage and, consequently, higher power dissipation in the power semiconductors that are turning off.

Reduction of turn-off losses (RCD snubbers)

To begin with, the IGBT is in on-state and conducts the load current.
Commutation from the IGBT to the freewheeling diode is started by active IGBT turn-off.

The load current quickly commutates from the IGBT to the parallel D-C branch, causing the collector current and the collector-emitter dv/dt to decrease at the same time.
This leads to a reduction in the IGBT turn-off losses. The characteristics for collector current and collector-emitter voltage correspond to soft switching as explained in chapter 1.
Chapter 5.9.3 shows that the loss reduction that can be achieved with a certain capacitance strongly depends on the given transistor technology. At the end of voltage commutation, the freewheeling diode will turn on with low losses and take up the snubber capacitance current. As of the next time the IGBT turns on, the energy stored in the snubber network capacitor will be mainly converted to heat by resistor R.

Recommendations for dimensioning:

1. The snubber inductance should not to be dimensioned any bigger than needed for loss reduction
2. Use fast network diode with lower turn-on overvoltage (forward recovery)
3. Use pulse-proof capacitors (film capacitors or similar) with low internal inductance
4. Reduce loop inductance in the snubber network to a minimum
5. R and C form the time constants (t = R*C) necessary for internal energy discharge in the capacitor. This results in a minimum IGBT static off-time (duty cycle limitation) to achieve efficient reduction of turn-off power losses (no residual voltage in C). On the one hand, decreasing R will reduce the minimum IGBT static on-time; on the other hand, however, it will lead to a higher current and, consequently, greater losses when the transistor is turned on.

Note that bigger inductive and capacitive snubber elements will always lead to longer commutation times!

In applications that use simple snubber networks, as described above, the total energy stored is converted to heat mainly in the network resistor but also partially in the transistor (dissipative snubber). Thus, the overall efficiency of the circuit will not be improved - irrespective of the reduced losses in the switches. All this measure does is move the losses from the semiconductor to the snubber resistor, thus allowing higher switching frequencies.
Furthermore, numerous low-loss snubber networks (non or low-dissipative snubbers), where the energy is stored in resonant circuits or fed back to the DC link, are well-known from relevant literature. However, circuit designs such as these are often very complicated to dimension, and the layout and circuitry requirements are very challenging, too. [72].

5.9.3 Soft switching

5.9.3.1 Load on power semiconductors

Soft switching is another possible way of reducing losses in power electronic switches.
The expression "soft switching" actually refers to the operation of power electronic switches as zero-voltage switches (ZVS) or zero-current switches (ZCS) (cf. chapter 1).
The many different converter circuits that working according to these principles are generally assigned to resonance or quasi-resonance technology.

ZVS (Figure 5.9.3):
- The commutation process is started by active turn-off, switching losses are reduced thanks to parallel connection of commutation capacitance C_K,
- the commutation process is completed by passive, low-loss turn-on at a switch voltage $v_s \approx 0$,
- before next commutation, the direction of current flow changes in the switch that is turned on with impressed di/dt,
- Inductance in commutation circuit L_K should be at the minimum.

ZCS (Figure 5.9.5):
- The commutation process is started by active turn-on, switching losses are reduced thanks to series connection of commutation inductance L_K,
- the commutation process is completed by passive, low-loss turn-off at a switch current $i_s \approx 0$,
- before next commutation, the voltage direction changes in the switch that is turned on with im-

pressed di/dt,
- Capacitance in commutation circuit C_K should be at the minimum.

Continuous soft switching is based on the condition that only one kind of commutation process - either inductive commutation / ZCS or capacitive commutation / ZVS – takes place in the commutation circuit of the converter. Owing to this restriction, the loss of one control possibility as compared with hard switching has to be accepted.
This is only achieved if the polarities of the driving commutation voltage v_K or the commutated output current i_L are reversed between two identical commutation processes.

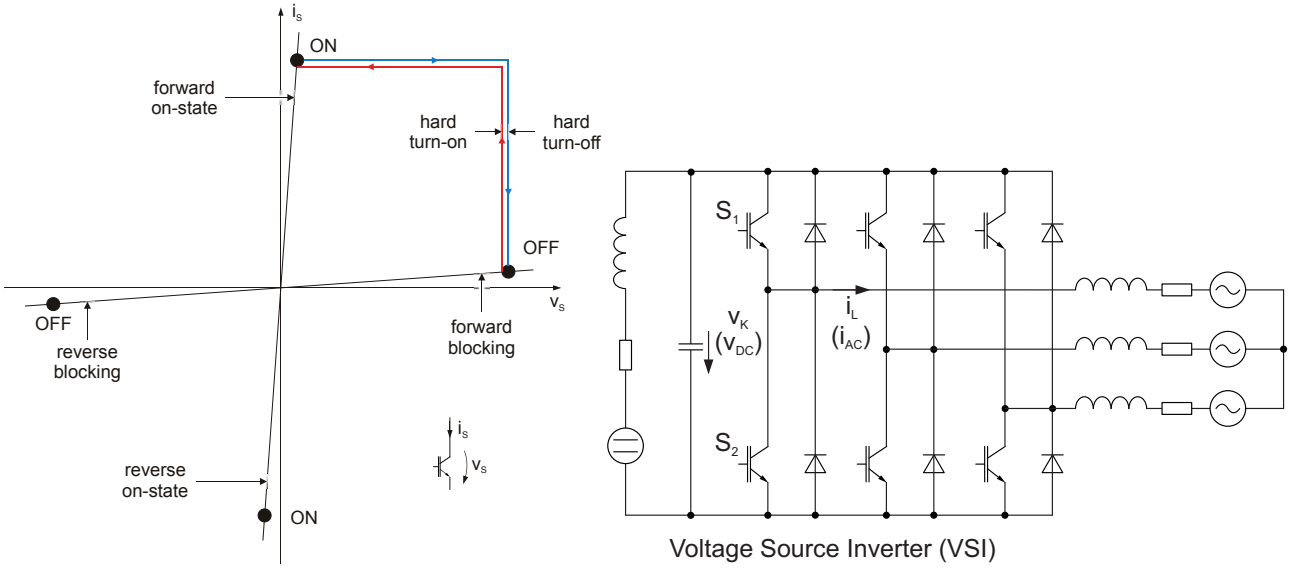


Figure 5.9.2 Operating point characteristic of switch current and voltage for hard switching (IGBT, MOSFET) and typical circuit diagram for voltage source inverter

The IGBT, MOSFET and diodes available today were developed and optimised almost exclusively for hard switch applications and display comparable features for this area of application (Figure 5.9.2).
Extensive investigations over the past few years, however, ([74], [76], [77]) have demonstrated that the different component structures and technologies behave very differently during soft switching (cf. chapter 5.9.3.3.).

And yet the datasheets available at the moment do not make these differences apparent to the user.

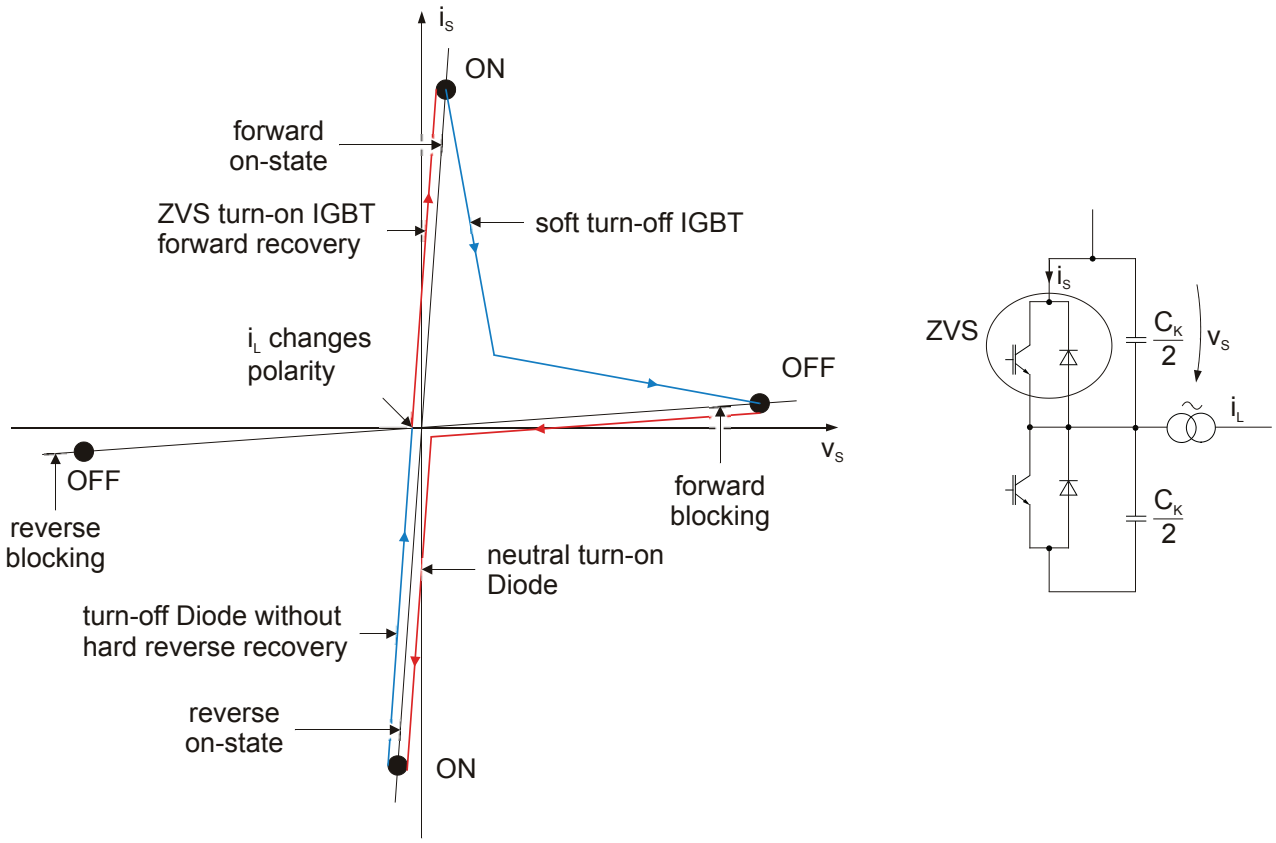


Figure 5.9.3 Operating point characteristic of switch current and voltage during soft / resonant switching as ZVS

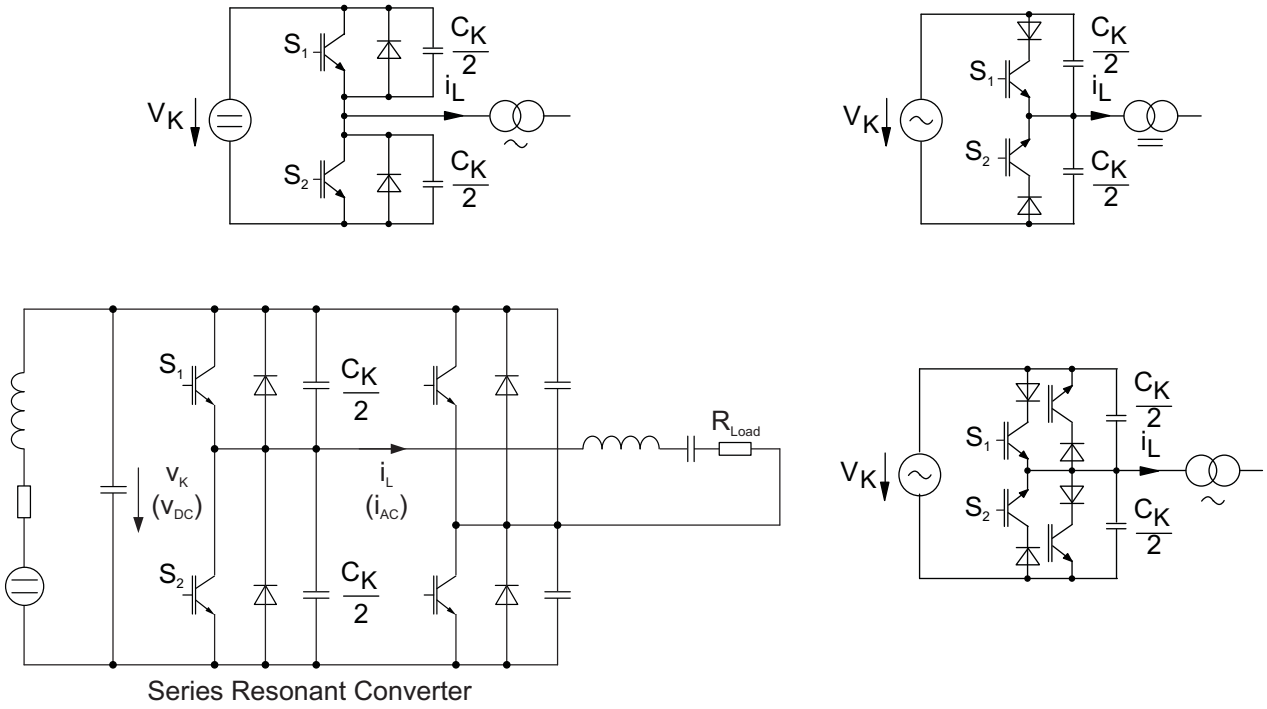


Figure 5.9.4 Sample circuit diagrams for commutation circuits with ZVS and a series resonant converter

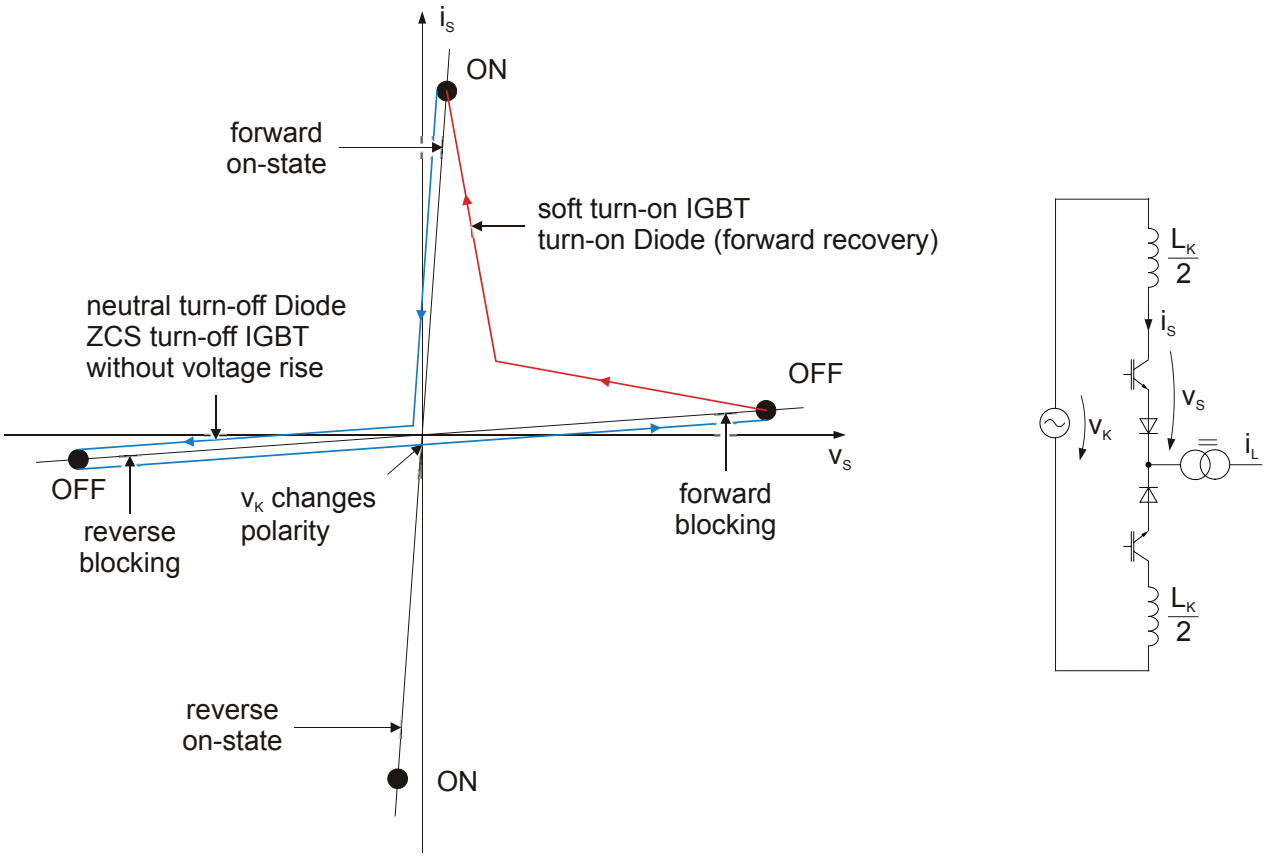
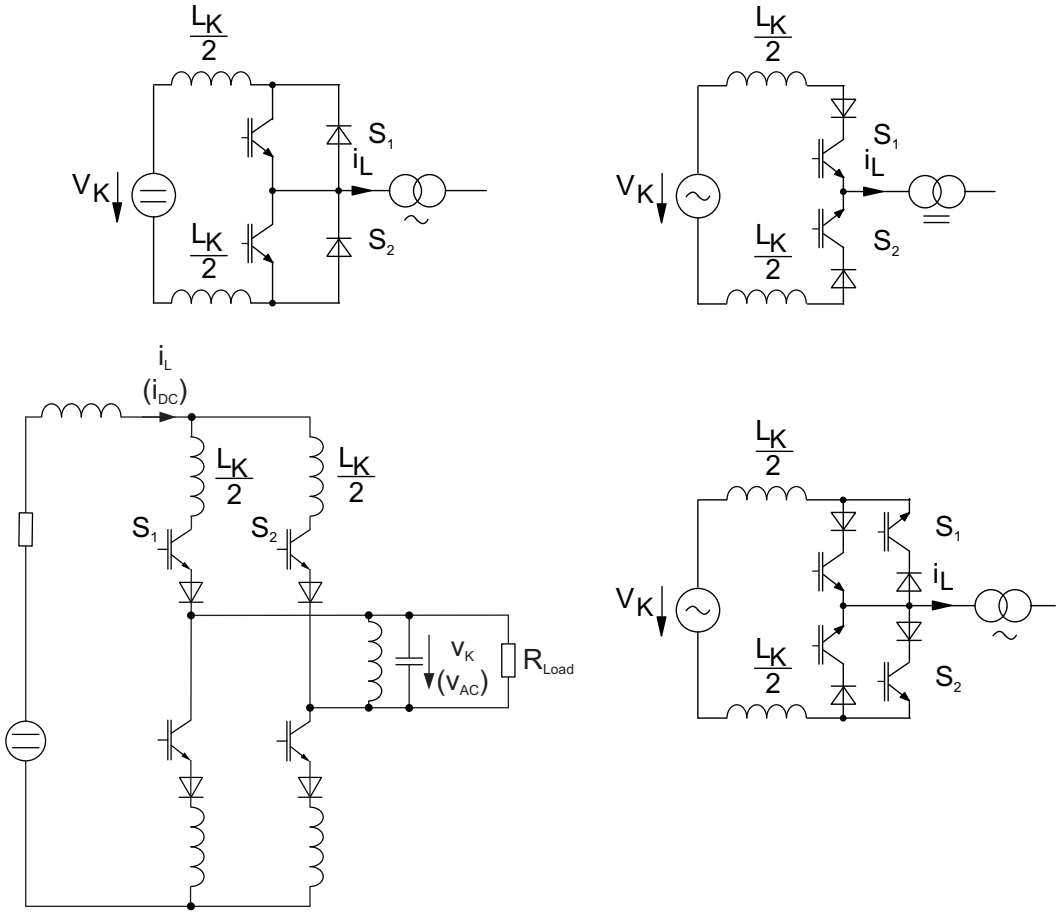


Figure 5.9.5 Operating point characteristic of switch current and voltage during soft / resonant switching as ZCS



Parallel Resonant Converter

Figure 5.9.6 Sample circuit diagrams for commutation circuits with ZCS and a parallel resonant converter

A comparison of the track of the operating points in figures 5.9.2, 5.9.3 and 5.9.5 shows that the area encircled by the track is different in size. The area is a relative measure of the power losses that occur during switching. During hard switching (Figure 5.9.2) the area is at its maximum. In the case of ideal resonant switching, the track of the operating point would go along the axes of the coordinate system. In real resonant or quasi-resonant switching and commutation processes, the resulting path will lie somewhere between the two aforementioned ideal conditions (Figures 5.9.3 and 5.9.5).

5.9.3.2 Semiconductor and driver requirements

ZVS

Power semiconductors
- have to feature active turn-off and demonstrate good power-loss reduction behaviour during turn-off
- For IGBT: + short charge carrier lifetime and low tail charge
  + low dependence of tail charge and charge carrier lifetime on the junction temperature
  + low forward turn-on overvoltage during conductivity modulation during zero-voltage turn-on with impressed di/dt
- Since ZVS-diodes do not turn off with reverse-recovery di/dt and take on reverse voltage at the same time, the requirements for reverse-recovery behaviour are not as strict as for hard switching topologies.

Driver circuit:

The driver circuit has to comply with the following minimum requirements:
- active IGBT / MOSFET turn-off and
- switch voltage monitoring and passive turn-on of ZVS at $v_S \approx 0$ V.

Modified ZVS mode:

The duration of a capacitive commutation process can be approximated as follows:

$$t_{Kc} \approx (C_K \cdot v_K)/i_L$$

Where: C_K: Commutation capacitance (power loss reduction capacitance)
v_K: Commutation voltage
i_L: Load current to be commutated

With low load currents, the commutation process in power converters may last an undesirably long time, impairing circuit function. This can be avoided by using modified zero voltage switches, which will abruptly end the commutation process after a variable maximum commutation time by active turn-on towards the not yet fully recharged commutation capacitance. This can, however, result in increased switching losses.

Figure 5.9.7 shows the principle behind a modified ZVS.

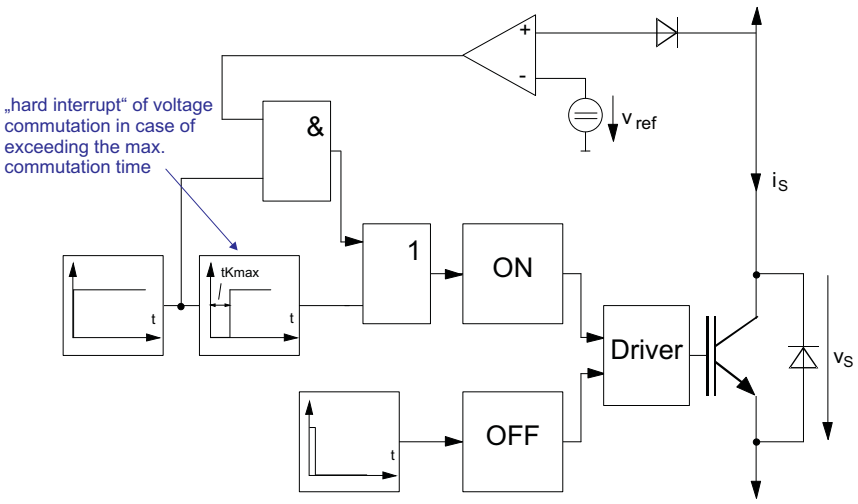


Figure 5.9.7 Modified ZVS: basic principle

ZCS

Power semiconductors
- have to feature active turn-on and demonstrate good power-loss reduction behaviour during turn-on,
- should have low internal capacitance,
- For IGBT: + short charge carrier lifetime
  + low dependence of storage charge and tail charge on the junction temperature
  + short dynamic saturation phase during turn-on
- Diodes: Low reverse recovery charge (Q_{RR}, t_{RR})

Driver circuit:

The driver circuit has to comply with the following minimum requirements:
- active IGBT / MOSFET turn-on and
- switch current monitoring and passive turn-off of ZCS at $i_S \approx 0$ A.

Modified ZCS mode:
The duration of an inductive commutation process can be approximated as follows:

$t_{Ki} \approx (L_K \cdot i_L)/v_K$.

Where: L_K: Inductance in the commutation circuit (power loss reduction inductance)
vK: Commutation voltage
i_L: Load current to be commutated

At low commutation voltages or high load currents, the commutation process in power converters may last an undesirably long time, impairing circuit function. This can be avoided by using modified zero current switches, which will abruptly end the commutation process after a variable maximum commutation time by active turn-off towards the live commutation inductance. This can, however, result in increased switching losses. In connection with this, please note that in many applications zero current switches have to feature overvoltage protection.

Figure 5.9.8 shows the principle behind a modified ZCS.

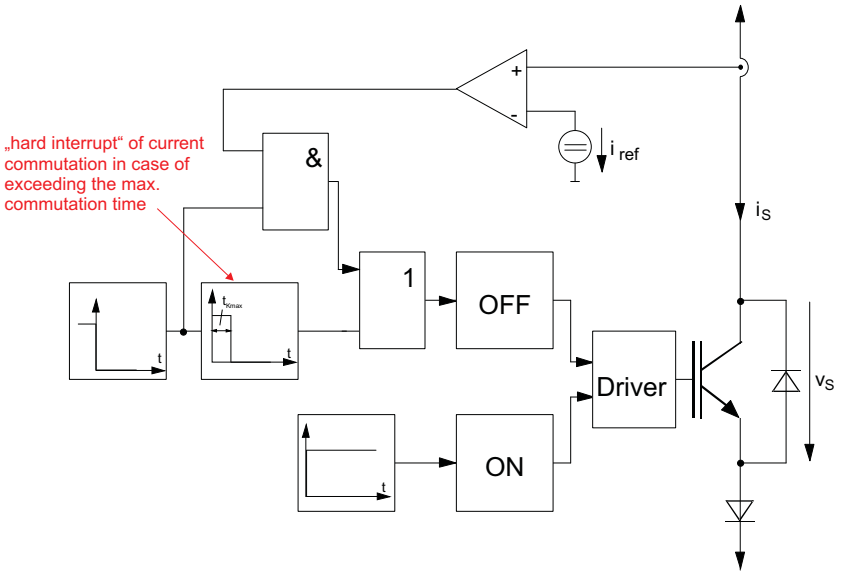


Figure 5.9.8 Modified ZCS: basic principle

5.9.3.3 Switching properties

ZVS with PT and NPT IGBT [74], [76], [78]

during zero-voltage turn-on with impressed di/dt

Before the IGBT is able to conduct a current, it has to be turned on by the driver. Since conductivity modulation within the n^- base will not have taken place before the current is taken up, the IGBT will react to the di/dt-impression with a transient increase in on-state voltage and, consequently, increased on-state losses for this time interval (forward recovery). Dynamic overvoltage, the duration of conductivity modulation and, hence, power dissipation depend mainly on the basic doping of the n^- base, emitter efficiency, charge carrier lifetime, di/dt, final switch current value (load current) and temperature.
NPT IGBT, which are characterised by low emitter efficiency and long charge carrier lifetime, will respond with relatively low forward voltage peaks (Figure 5.9.9a). The procedure, however, may take more than 10 µs. By contrast, the transient forward voltage peaks of PT structures exceed the stationary forward voltage by 30 to 40 times (high emitter efficiency, short charge carrier lifetime). In this case, however, the procedure will take some 100 ns only (Figure 5.9.9b). The conflicting tendency of voltage peak and process duration will cause the power losses in the NPT and PT IGBT ZVS, which can make up a significant share of the total power losses, especially in high-switching-frequency applications, to line up somewhat (Figure 5.9.10a and b).

If the ZVS short-circuit protection is based on v_{CE} measurement and evaluation, this protection has to be blanked out during di/dt impression to prevent the converter from being turned off due to the error message.

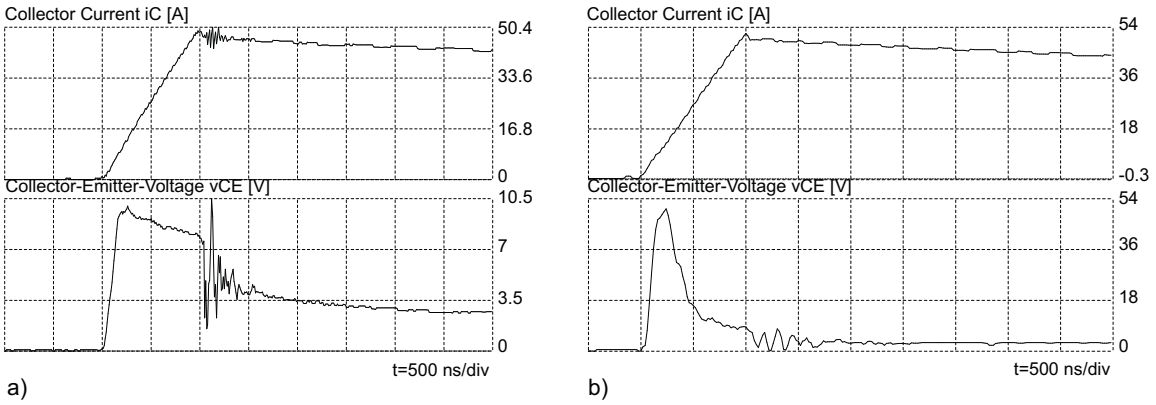


Figure 5.9.9 a) di/dt-impression in a 1200 V / 50 A-NPT-IGBT (di/dt = 50 A/µs; i_L = 50 A)
b) di/dt-impression in a 1200 V / 50 A-PT-IGBT (di/dt = 50 A/µs; i_L = 50 A)

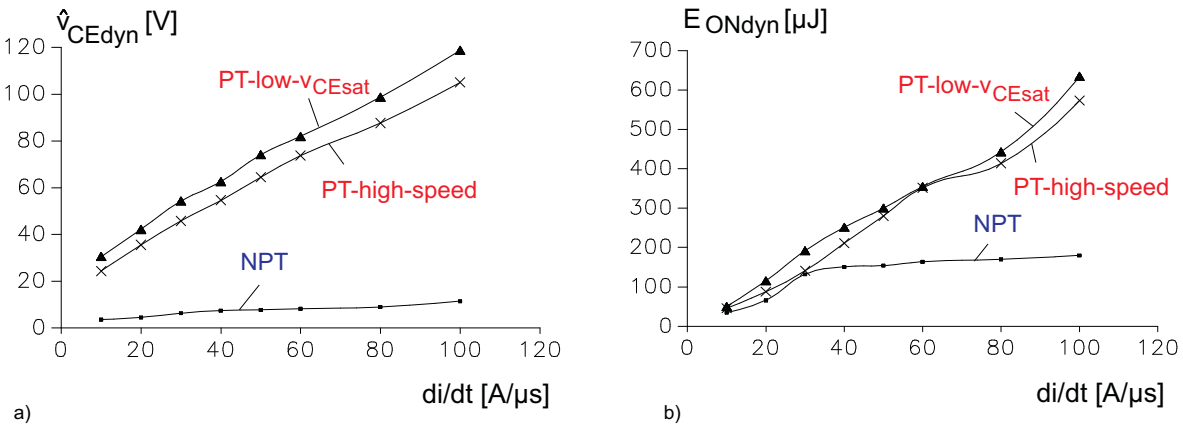


Figure 5.9.10 a) Dynamic on-state voltage amplitude of 1200 V / 50 A NPT and PT IGBT as a function of impressed di/dt (i_L = 30 A)
b) Losses during di/dt impression of 1200 V / 50 A NPT and PT IGBT as a function of impressed di/dt (i_L = 30 A)

Active, soft turn-off (cf. Figure 1.1.2 in chapter 1.1)

During active soft IGBT turn-off, current can commutate directly to the parallel capacitance C_K with reduced collector-emitter dv/dt, resulting in reduced switching losses. The tail current characteristic, i.e. the discharge of charge stored in the IGBT after MOSFET channel blocking, is determined substantially by the collector-emitter dv/dt. Increasing the commutation capacitance will lower the initial tail current value (comparable to a capacitive current divider between IGBT and snubber capacitor). At the same time, the tail current will be prolonged, impairing the reduction of turn-off losses. For NPT structures with long charge carrier lifetime, this will lead to unsatisfactory switching loss reduction (Figure 5.9.11a, Figure 5.9.12). In contrast, the oscillogram in Figure 5.9.11b shows that with PT structures the tail current may already have dropped to zero before the collector-emitter voltage has reached the level of the outer commutation voltage. The result of tests using 1200 V / 50 A PT IGBT modules showed that for a commutation capacitance C_K = 30 nF, the turn-off switching losses may be reduced by 50 % compared to hard switching (Figure 5.9.12). With comparable NPT IGBT, the switching losses were reduced by only around 20 %.

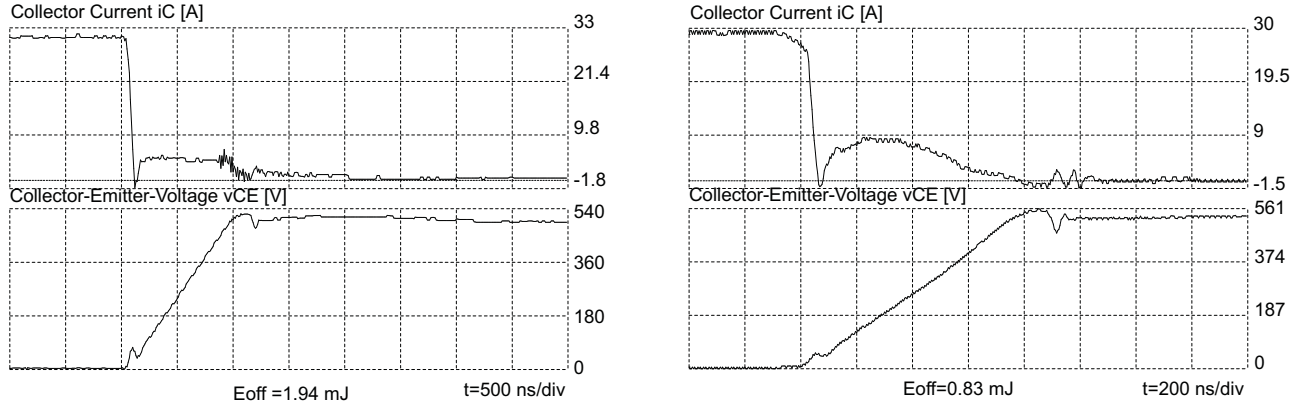


Figure 5.9.11 a) Soft turn-off of a 1200 V / 50 A NPT IGBT at C_K = 47 nF
b) Soft turn-off of 1200 V / 50 A PT IGBT at C_K = 30 nF

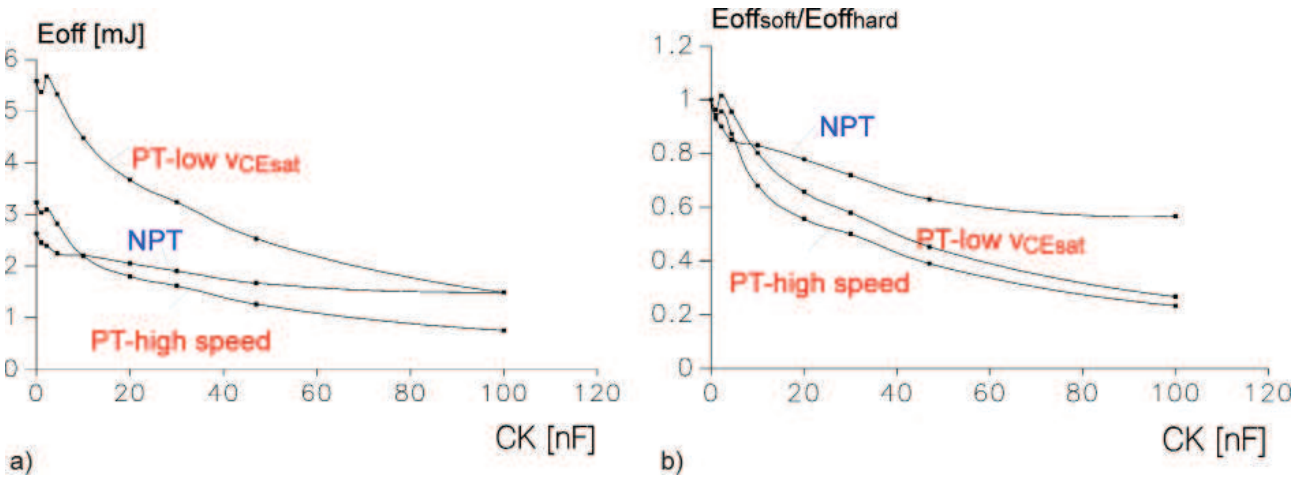


Figure 5.9.12 a) Turn-off losses of 1200 V / 50 A IGBT as a function of the commutation capacitance C_K (v_K = 500 V; i_L = 50 A)
b) Turn-off losses in relation to hard switching of 1200 V / 50 A IGBT as a function of the commutation capacitance C_K (v_K = 500 V; i_L = 50 A)

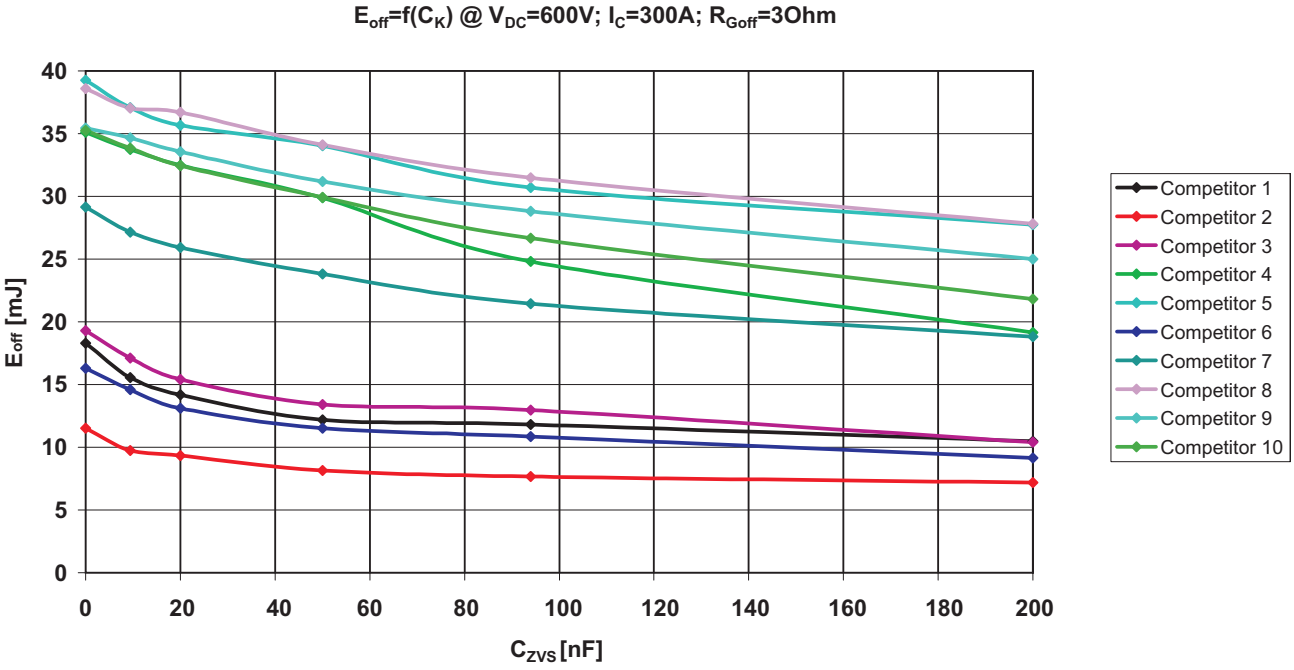


Figure 5.9.13 Comparison of turn-off losses and power loss reduction of the IGBT technology available on the market today (1200 V / 300 A modules); operating point V_{DC}=600 V, I_C=300 A under comparable driver conditions

Figure 5.9.13 demonstrates the clear differences in suitability of existing IGBT technologies for soft turn-off as ZVS at high switching frequencies. At this point, a careful choice must be made for the individual application with a view to optimising efficiency.

[75] shows that in ZVS applications, state-of-the-art field-stop technologies are able to compete with fast NPT and PT technologies.

ZVS with MOSFET [77]

MOSFET are unipolar devices that must not be charged or discharged with any storage charge. This results in the following specifics for use in ZVS applications:

- There is no dynamic forward overvoltage during zero-voltage turn-on with impressed di/dt.
- Within the same device rating class, the comparison with IGBT shows that turn-off switching losses in MOSFET with commutation capacitances of some nF are virtually non-existent. The relatively high output capacitance of MOSFET supports the turn-off loss reduction.
- The process where the off-state transistor is subject to high dv_{DS}/dt is critical for MOSFET; in ZVS

mode this process does not exist (cf. chapter 5.6). That is why, in principle, MOSFET may be driven by negative gate-source voltage in this case.

Fast diodes in ZVS

In ZVS operation, diodes will not turn off with reverse-recovery di/dt and take up reverse blocking voltage at the same time. The reverse-recovery behaviour of fast diodes is therefore negligible compared to hard switching.

Having said that, optimum dynamic turn-on is still required in ZVS applications. In relation to this, CAL diodes offer particular advantages.

ZCS with PT and NPT IGBT [75], [78], [79]

Active, soft turn-on (cf. 1.1.2 in chapter 1)

Figure 5.9.14 shows the oscillogram of soft turn-on of a 1200 V / 50 A NPT IGBT, as well as the dependence of turn-on losses of different IGBT technologies on the commutation inductance L_K.

The power loss reduction during turn-on is very good. Power losses in the IGBT compared here are identical for a series commutation inductance greater than 3 µH. For IGBT, the losses amount to as little as around 15 % of those for hard switching.

Unlike turn-off in ZVS mode, the turn-on loss reduction for PT and NPT IGBT is equally good.

In [75], experimental investigations verify that combining state-of-the-art field stop technology and fast diodes results in minimum-loss ZCS solutions. In ZCS applications, the right choice of switch diode is particularly important.

Power losses that occur during IGBT turn-on in ZCS mode are caused by the processes that take place during dynamic saturation.

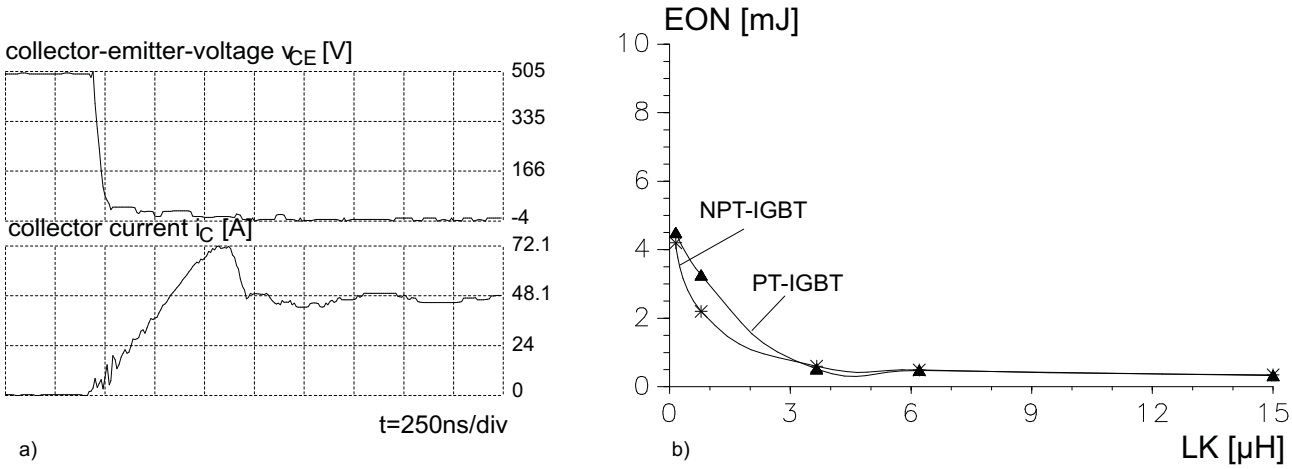


Figure 5.9.14 a) Low-loss turn-on of an NPT IGBT (L_K = 3.6 µH)
b) Turn-on losses of ZCS as a function of the commutation inductance L_K (v_K = 500 V, i_L = 30 A)

In ZCS circuits with high frequencies, i.e. short switching duration, the losses might be dominant during dynamic saturation (conductivity modulation). This is owing to fact that the stationary forward on-state of the IGBT is not reached.
In [79] a driver concept is introduced which feeds an additional gate current into the IGBT during dynamic saturation, causing a reduction in energy losses of around 50% during this period. The time point for gate current feed is determined by the start of the Miller plateau phase.

Voltage reversal in off-state ZCS with removal of residual IGBT storage charge

Figure 5.9.15 shows the processes involved in passive turn-off of IGBT ZCS (IGBT with series and antiparallel diode) with subsequent switch voltage polarity reversal.

What can be clearly seen is that, in the case of PT structures, the residual charge to be removed Q_S is low (short charge carrier lifetime) when the IGBT takes up forward blocking voltage after the hold-off time t_H, leading to lower losses during this dynamic process.

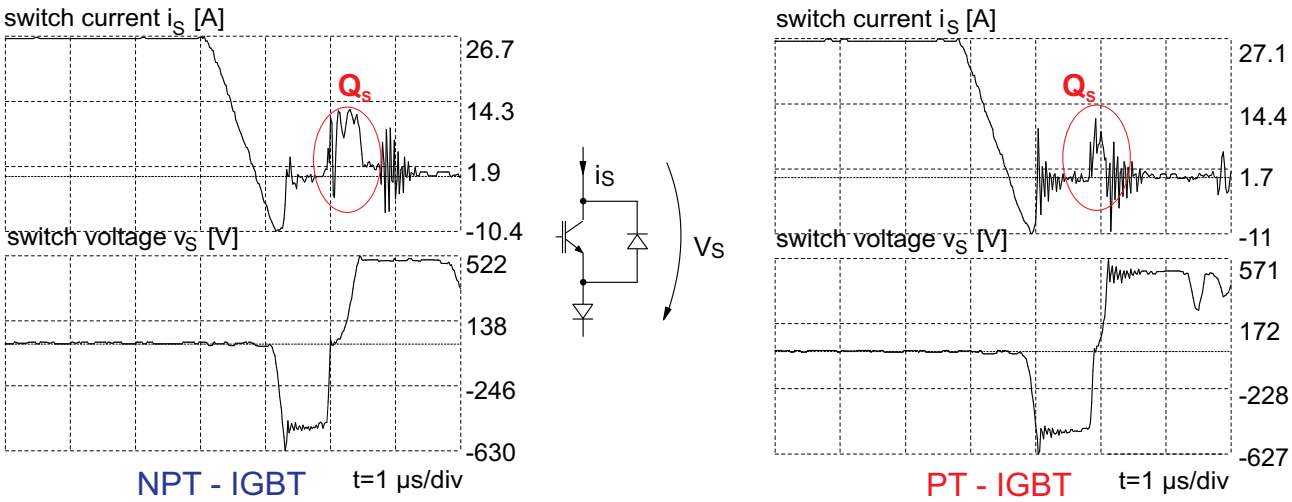


Figure 5.9.15 Turn-off characteristics of 1200 V / 50 A NPT and PT IGBT at the same operating point (t_H = 1.3 µs, L_K = 10 µH)

The dependence of residual storage charge on the hold-off time is shown in Figure 5.9.16a. Here, the advantages of PT structures are illustrated very clearly. By way of contrast, storage charge of PT structures is more temperature-dependent, which restricts the maximum permissible switching frequency due to the risk of thermal instability (thermal runaway), especially for short hold-off times (Figure 5.9.16b).

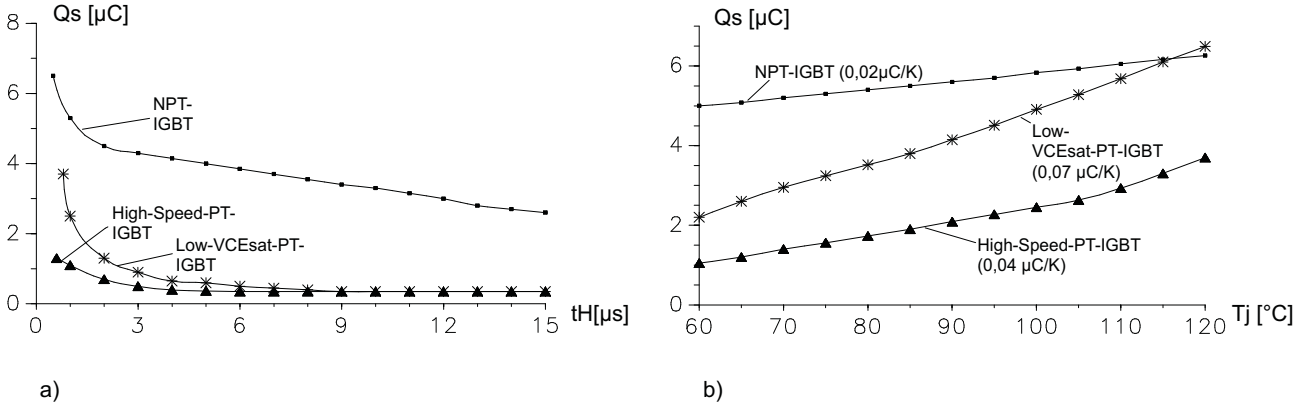


Figure 5.9.16 a) Residual storage charge of PT and NPT IGBT ZCS as a function of hold-off time (v_K = 400 V, i_L = 30 A, L_K = 10 µH)
b) Storage charge of PT and NPT IGBT ZCS as a function of the junction temperature of the transistor (v_K = 400 V, i_L = 30 A, L_K = 10 µH, t_H = 1.3 µs)

In [78] an IGBT ZCS driver stage is presented that involves an additional collector current being fed to the IGBT by the driver during hold-off time in order to remove the storage charge. This step enabled the drastic reduction of the losses during blocking voltage uptake especially for hold-off times t_H > 2 µs.

ZCS with MOSFET

Since MOSFET do not feature dynamic saturation, MOSFET with very small (...1 µH...) series soft switch inductances can almost be fully relieved of turn-on losses.
The high output capacitance of MOSFET, however, has a negative impact on the turn-on losses. If high switching frequencies are used (> 50 kHz), the resulting share of power losses has to be factored in to the total power losses.
Due to the unipolarity of MOSFET there will be no removal of residual storage charge during change of polarity of the switch voltage at the end of hold-off time. The relatively high output capacitance, in contrast, has to be recharged.

Fast diodes in ZCS

In ZCS mode, diodes turn off with reverse-recovery di/dt and take up reverse blocking voltage at the same time. Due to the existing commutation inductances, current will be commutated in the diodes at a lower speed than in hard-switching converters (lower reverse current peak, reduced turn-off losses). Nevertheless, the need for very good dynamic turn-off behaviour hand in hand with low turn-off losses prevails.

In addition, the use of fast diodes as series diodes of IGBT or MOSFET in ZCS mode calls for very good dynamic turn-on behaviour of the diodes (forward recovery).

5.9.3.4 Conclusion

The behaviour of power semiconductors during hard switching is not applicable to soft switching. In principle, components with a shorter charge carrier lifetime are more suitable for soft-switching applications due to the aforementioned dynamic processes. Generally speaking, the information on power electronic components specified in existing datasheets is not suitable for evaluating dynamic behaviour in ZVS and ZCS topologies.

Owing to the great variety of low-loss converter topologies with their own specific switch requirements, a general conclusion on the limitation of frequencies of IGBT and MOSFET switches cannot be drawn.

6 Handling instructions and environmental conditions

This chapter provides an overview of the most important requirements for transportation, storage, mounting and operation of discrete power semiconductors and power modules. The requirements for transportation and storage also apply to modules integrated in devices in order to ensure reliable operation throughout the device's service life.

6.1 Sensitivity to ESD and measures for protection

All IGBT or MOSFET power modules are sensitive to ESD (**E**lectro **S**tatic **D**ischarge) due to the thickness of their gate isolation (gate oxide layer), which amounts to some ten nanometers only. This is why they are classified as ESD (**E**lectrostactic **S**ensitive **D**evices) in accordance with EN 61340-5-1 and EN 61340-2-3 – i.e. devices which are prone to damage by electrostatic fields or electrostatic discharge during routine handling, testing and transportation. IGBT and power MOSFET with big chip areas are characterized by high input capacitances and, compared to small-signal devices, are classified as minor sensitive components according to procedure 3015.6 of the MIL-STD 883C standard.

When handling IGBT or MOSFET power modules, the regulations set down in the aforementioned MIL standard, as well as those of DIN VDE 0843 T2, which is identical to IEC 801-2, must be adhered to. Inspection and further processing must always be carried out by suitably clothed staff (antistatic overalls, wrist strap, if available). Before ESD-sensitive components are processed, all transportation and assembly equipment, as well as PCBs must be adjusted to the potential of the ESD-sensitive components, and electrostatic re-charge must be prevented. For identification purposes, a warning label as specified in IEC 60417, reg. no. 5134 must be attached to packaging of electrostatic sensitive devices (Figure 6.1.1).

Figure 6.1.1 Warning label for ESD packaging

The power modules are supplied with gate and emitter / source terminals short-circuited by suitable conductive packaging, packaging lined with conductive foam or rubber mats, self-sealing metal foils, with annular rivets on the terminals or caps on the connectors. If possible, this short circuit should not be removed until connecting the gate.

6.2 Ambient conditions for storage, transportation and operation

This sections refers to the classification and description of environmental conditions according to EN 50178 and EN 60721-3 (IEC 721-3) including standard sections EN 60721-3-1 (storage), EN 60721-3-2 (transportation) and EN 60721-3-3 (stationary use at weather-protected locations). Other parts not referred to in this section describe the conditions of stationary use at non-weather-protected locations (EN 60721-3-4), ground vehicle installations (EN 60721-3-5), ship environment (EN 60721-3-6) and portable, non-stationary installations.

As illustrated in Figure 6.2.1, devices are exposed to many different kinds of environmental stress, which are summarised accordingly in the environmental conditions stipulated in EN 60721-3. Environmental conditions which can be then expected to occur in the field application must be factored in during the development and construction of electronic devices already. This also includes the selection of suitable power semiconductors, as well as semiconductor cooling and assembly.

Consequently, in order to comply with the environmental provisions determined by application specifics, operating location, the conditions of storage and transportation to the final place of use, as well as conditions during down-time, the selection of components on the basis of environmental conditions is to be iteratively combined with design measures for protection from environmental impacts.

The best compromise between the component, circuitry and design complexity must be found during the development process already, while taking into consideration existing semiconductor-specific or component-specific limits such as moisture absorption of the soft mould of IGBT.

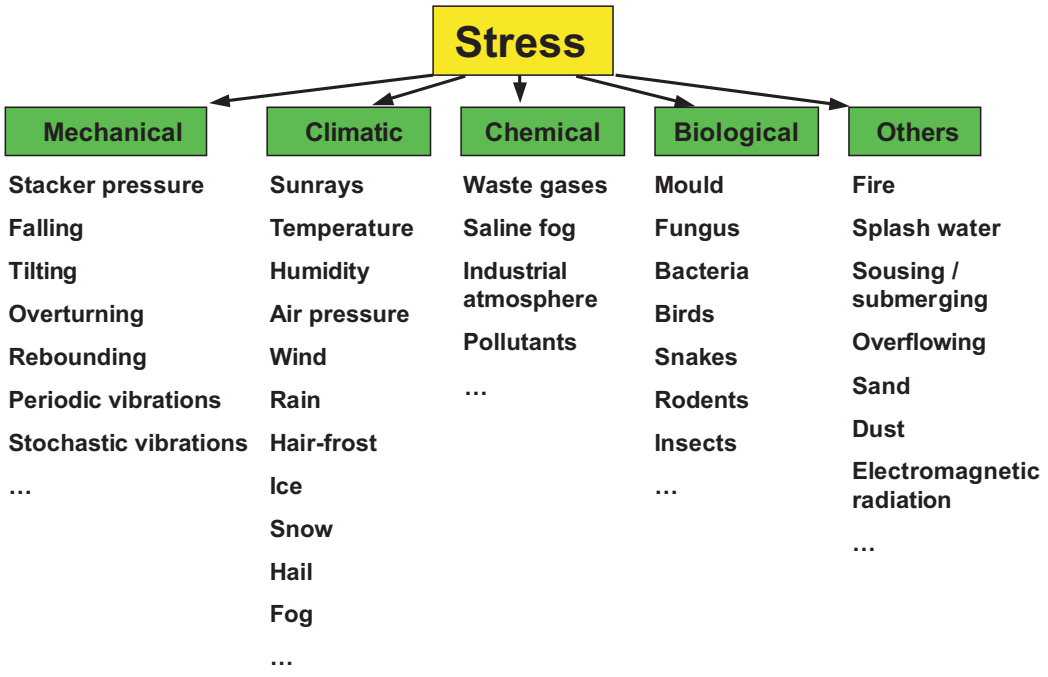


Figure 6.2.1 Environmental stress factors during transportation, storage and operation as per DIN-EN 60721-3

EN 60721-3, environmental conditions are categorised according to the "nAxY" environmental classification code:

The first digit (n) identifies the area of application that the requirements defined by the subsequent digits apply to.

n: 1: Storage 2: Transportation 3: Operation

The first capital letter (A) determines the type of environmental quantity the limits refer to.

A: K: Climatic; M: Mechanical; B: Biological; C: Chemically active substances; S: Mechanically active substances; Z: Other climatic conditions

The third digit (x) determines the limits of the environmental quantity under A

x: Numbering (in ascending order by degree of severity)

Y: Additional capital letter for further specification

In most cases, higher degree classes include the requirements of lower degree classes. In addition, assembly, maintenance and repair conditions are to be taken into account, insofar as these are likely to deviate from the storage and operating conditions. Furthermore, 7 standardized combinations of the environmental conditions above (designated with "IExx“) are defined in the aforementioned EN standard, providing a thorough classification description for 4 standard cases of environmental conditions with respective application examples.

Compliance with the specified environmental requirements is proven by inspection and testing of sample products under simulated environmental conditions. To do so, the products are subjected to environmental tests that are set down in the IEC 60068-x-x and IEC 60749 standards. To select suitable test procedures and the degree of severity, the "Guide on the correlation and transformation of environmental condition classes of IEC 60721-x to the environmental tests of IEC 60068" (draft standard DIN 40046-721-x, separate documentation for storage (-1), transportation (-2), stationary use at weather-protected locations (-3), etc.) may be referred to.

The following sections will provide a rough characterization of the most important environmental classes using the example of the operating conditions for electric appliances in stationary use at

weather-protected locations according to EN 60721-3-3. Detailed information on specific limits is provided in EN 60721-3-3. Please refer to this for a more thorough understanding of the classification system.

6.2.1 Climatic conditions

Climatic conditions include air temperature, absolute and relative air humidity, condensation, rate of temperature change, barometric pressure, solar and thermal radiation, air movement, wind-driven rain, water (except for rainfall) and ice formation.

Climatic conditions are classified into 11 categories designated by codes 3K1....3K11, which are sorted in ascending order with reference to their degree of climatic impact. The most important climate classes are:

- 3K1: Fully air-conditioned locations. Locations with permanent air humidity and temperature regulation.
- 3K2: Closed locations with permanent air temperature regulation, non-regulated air humidity, condensation ruled out.
- 3K3: Closed locations with air temperature regulation, non-regulated air humidity, condensation ruled out.
- 3K4: Closed locations with air temperature regulation and a wide range of possible relative humidity (non-regulated air humidity). Products are able to withstand condensation and water (except for rainfall) impact.
- 3K5: Closed locations without air temperature or humidity regulation. Heating may be used if the climate class conditions differ greatly from the open-air climate. Products are able to withstand ice formation.
- 3K6, 3K7, 3K8: Weather-protected locations with optional openings to the open air, i.e. locations may only be partly closed.

Products (except for class 3K7L products) may be exposed to solar radiation of varying intensity. Impact from wind-driven precipitation (including snowfall) is permitted to a limited extent only. With the exception of class 3K1, the climate classes correlate with the open-air climate types as per EN 60721-2-1:

- extremely cold climate (except for the Antarctic)
- cold climate
- moderate climate
- moderately dry climate
- dry-hot climate
- extremely dry-hot climate
- moist-hot climate
- moderately moist-hot climate

The climate class applicable to the individual open-air climates and operating conditions may therefore be determined using appendix A of the EN 60721-3-3 standard and the climatograms provided in the standard (also refer to the example in chapter 6.2.7).

6.2.2 Mechanical environmental conditions

Figure 6.2.2 illustrates the various types of mechanical stress listed in the environmental conditions in accordance with EN 60721-3-3.

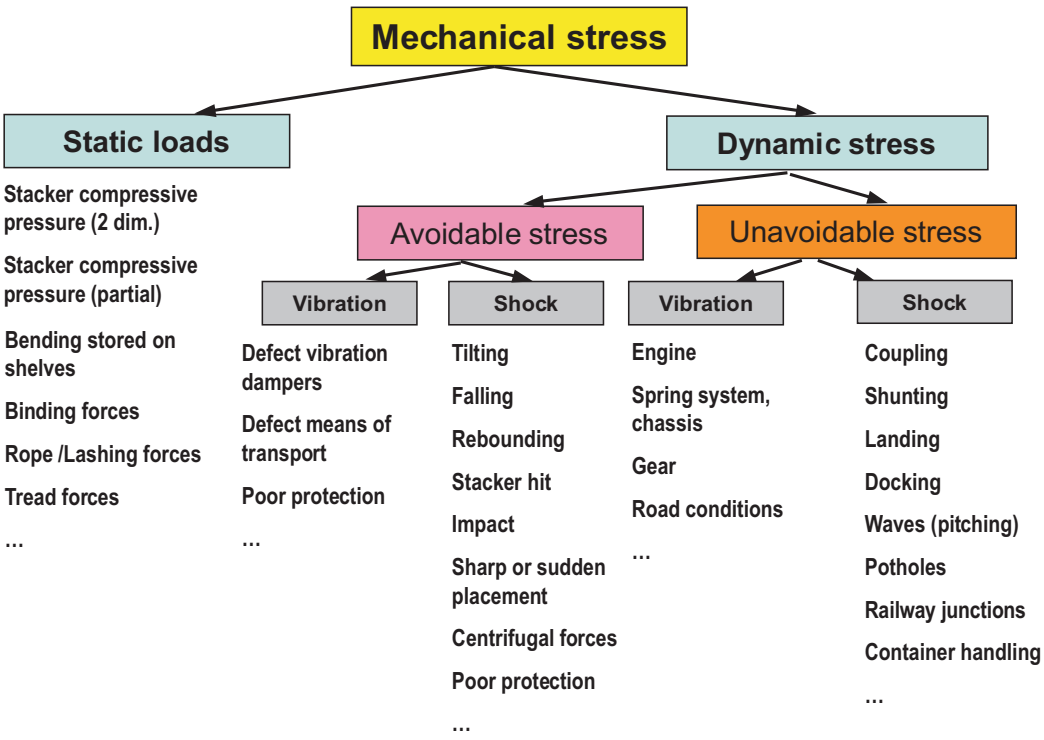


Figure 6.2.2 Types of mechanical stress according to the environmental conditions listed in EN 60721-3-3

Mechanical environmental conditions are specified by the limit values for the following variables:
- Vibrations: Displacement or acceleration amplitude and frequency range for sinusoidal vibrations, acceleration spectral density, roll-off and frequency range for vibration noise
- Shocks: Total shock response spectrum, peak acceleration, impact duration, directions of impact and number of impacts per direction

Mechanical environmental conditions are classified by 8 categories sorted in ascending order with reference to their degree of mechanical impact:
- 3M1: Locations not affected by vibrations and shocks
- 3M2: Locations subject to minor vibrations
- 3M3: Locations that are not or only minorly affected by vibrations, but with a risk of low-energy shocks, triggered e.g. by local blasting or pile-driving operation, slamming of doors etc.
- 3M4: Locations exposed to significant vibrations and shocks, e.g. due to running machines or passing vehicles
- 3M5: Locations exposed to significant high-energy vibrations and shocks, e.g. due to running heavy machinery, conveyors etc.
- 3M6: Locations exposed to high vibration levels and high-energy shocks, e.g. next to heavy machinery
- 3M7: Locations exposed to very high vibration levels and high-energy shocks, e.g. in places where devices are directly attached to machinery
- 3M8: Locations exposed to extremely high vibration levels and high-energy shocks, e.g. if devices are attached to hammer mills

In addition to the vibration level and the shock energy content, the determination of the appropriate mechanical stress class depends on the type of device and its fixture (rigid, flexible, on vibration dampers).

The required mechanical environmental class may be determined using the maximum rating tables included in appendix A of standard EN 60721-3-3.

6.2.3 Biological environmental conditions

Biological environmental conditions are classified by 3 categories sorted in ascending order according to the degree of contamination by mould / fungus formation, rodents and other animal pests:
- 3B1: Locations not explicitly exposed to detrimental biological impact; mould formation or detriment due to animal pests, for example, are unlikely
- 3B2: Locations with a risk of mould formation and infestation by animal pests (with the exception of termites)
- 3B3: Locations with a risk of mould formation and infestation by animal pests, including termites

The required biological environmental class may be determined using the maximum rating tables included in appendix A of standard EN 60721-3-3.

6.2.4 Environmental impact due to chemically active substances

Impact caused by chemically active substances such as sea salt / road salt, sulphur dioxide, hydrogen sulphide, chlorine, hydrogen chloride, hydrogen fluoride, ammonia, ozone and nitrous gases are classified according to 6 categories arranged in ascending order with reference to their degree of environmental impact.
- 3C1R: Locations with thorough atmosphere control and monitoring (cleanroom category)
- 3C1L: Locations with continuous atmospheric control
- 3C1: Locations with little industry and moderate traffic density; higher risk of air pollution in more densely populated areas in winter due to heating; risk of salt spray in coastal regions and at non-fully-enclosed locations at sea
- 3C2: Locations with air pollution levels typical of more densely populated areas with industrial facilities and high traffic volumes
- 3C3: Locations in the direct vicinity of industrial facilities with chemical emissions
- 3C4: Locations within industrial facilities where emissions containing high concentrations of chemical pollutants are permissible.

The standard does not take into account chemically active liquids and other existing chemically active solids. The required chemical environmental class can be determined from the tables of maximum ratings included in appendix A of standard EN 60721-3-3.

6.2.5 Environmental impact caused by mechanically active substances

Impact caused by mechanically active substances such as sand particles in the air and dust particles in air or precipitation are classified into 4 categories arranged in ascending order with reference to their degree of environmental impact:
- 3S1: Locations with minimum dust formation; sand ingression is prevented
- 3S2: Locations where no particular measures are taken to minimise dust formation or sand ingression, but which are not situated near to dust or sand sources
- 3S3: Locations where no particular measures are taken to minimise dust formation or sand ingression and which are situated near to dust or sand sources
- 3S4: Locations subject to sand or dust due to technical processes or situated in geographic regions with a permissible naturally high sand or dust concentration in the air

The required mechanical environmental class can be determined from the tables of maximum ratings included in appendix A of standard EN 60721-3-3.

6.2.6 Notes on operation at high altitudes

Depending on the particular circuit design, it might be necessary to limit the operating area when operating systems at heights greater than 2,000 m above sea level.

- Reduction of the output power or maximum operating temperature of air-cooled systems due to the low atmospheric density and barometric pressure, which adversely affects the cooling system; cf. chapter 5.3
- Reduction of the insulation capacity, because the dielectric strength of the air decreases in line with the increase in assembly height (decreasing barometric pressure)

Most SEMIKRON power modules comply with EN 50178 as far as insulation distances (clearances and creepage distances) are concerned. For assembly heights higher than 2000 m above sea level, however, stricter clearance requirements apply. In this case, clearances should be increased by a correction factor or, if this is not feasible, upstream transformers could be used, for example, to reduce the line voltage. The particular correction factors are stipulated below according to IEC 60664-1, Table A.2.

Operating height (in metres) above sea level	Barometric pressure in kPa	Correction factor
2,000	82	1.00
2,500	76	1.075
3,000	70	1.14
4,000	62	1.29
5,000	50	1.48

Table 6.2.1 Effect of operating height on insulation distances

Example SKiiP3, 1700 V:

For appliances supplied with V_N = 690 V_{eff} phase-to-phase voltage with grounded neutral point, the minimum clearance for safe insulation up to 2,000 m above sea level is 8 mm (EN 50178, Table 3). At operating heights above 2,000 m, this clearance must be multiplied by the respective correction factor. As the clearance is 9 mm for SKiiP3 (= 1.125 x 8 mm), the component may be operated at heights of up to 2,880 m (correction factor approximated between 2,500 m and 3,000 m).

Influence of cosmic radiation on the failure rate

Cosmic radiation is high-energy particle radiation from outer space. Primary radiation consists mainly of electrons and fully ionised atoms penetrating the Earth's atmosphere. Primary radiation is emitted mainly by supernovas and by the sun as well. The Earth's outer atmosphere is exposed to around 1,000 particles per square meter and second, but only a very small portion of this reaches the Earth's surface directly, since most primary particles collide with the gas molecules of the Earth's atmosphere (O_2, N_2). The secondary particles generated in this process once again collide with gas molecules in the Earth's atmosphere, causing them to disintegrate into a vast number of even smaller particles (pions, muons and neutrons), also referred to as cosmic ray shower, cf. Figure 6.2.3).

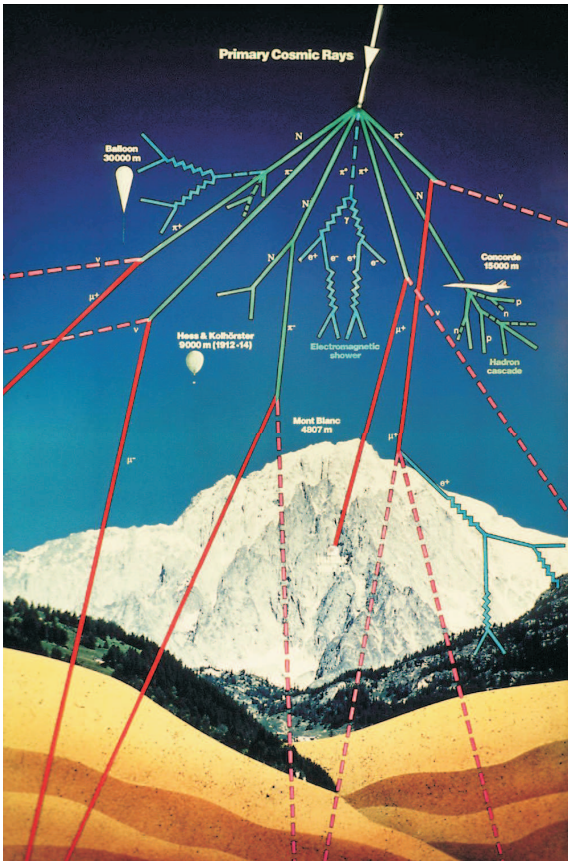


Figure 6.2.3 Diagram showing cosmic radiation [80]

Although semiconductors remain unaffected by most of these particles, some of the particles - mainly neutrons - are able to destroy a power semiconductor due to a local breakdown in the bulk of the semiconductor material, triggered within nanoseconds without prior indication of failure or wear. Failure rates are dependent on the operating height, voltage and chip temperature and are controllable, at least to a certain extent, by adapting the power semiconductor design, cf. [80]. ABB provides the following parameterised model equation for their HIPak IGBT power modules where V_{CES} = 1700 V….6500 V:

$$\lambda(V_{DC}, T_{vj}, h) = \underbrace{C_3 \cdot \exp\left(\frac{C_2}{C_1 - V_{DC}}\right)}_{1} \cdot \underbrace{\exp\left(\frac{25 - T_{vj}}{47.6}\right)}_{2} \cdot \underbrace{\exp\left(\frac{1 - \left(1 - \frac{h}{44300}\right)^{5.26}}{0.143}\right)}_{3}$$

λ: FIT rate (failures in 10^9 h)
C1, C_2, C_3: type-specific model parameters
h: Operating height in m
Term 1: Voltage dependency of the FIT rate
Term 2: Temperature dependency of the FIT rate
Term 3: Dependence of the FIT rate on the operating height

As a rule of thumb, the FIT rate doubles every 1,000 m in height. Voltage V_{DC} in term 1 represents the voltage actually applied between collector and emitter, i.e. the FIT rate should be determined separately for different operating states (including turn-off) and added (weighted by duration).

6.2.7 Air humidity limits and condensation protection

Silicone-based single-layer coating and encapsulation systems have become increasingly used to provide electrical insulation on the surface of DBC substrates. This is done for numerous reasons, e.g. polluting environment in production, recyclability, minimisation of mechanical stress, weight reduction.

Different humidity levels are balanced in both directions within these encapsulating systems. Thus, the speed of diffusion of water ions in the silicone gel amounts to 0.04 mm/s at 18°C, increasing up to 1 mm/s at 100°C. For silicon layers of approx. 5 mm in thickness, the saturation state is reached within 5 hours.

Example SKiiP3:

A time constant of τ = 8 h, the residual moisture left in the silicone gel after 4 hours of drying time is 40%.

Basically, the accumulation of water ions induces changes in the field line patterns in the barrier layers between semiconductor and casting compound, as well as in the fotoimide insulation layer of the chips. Electrolytic processes may be involved as well. Most SEMIKRON power modules conform to climate class 3K3 as per EN 60721-3-3 in compliance with EN 50178 and, with regard to clearances and creepage distances, may be operated under pollution degree 2 conditions stipulated by EN 50178 and EN 61800-5-1.

Accordingly, operation is not permitted in places of operation or installation where dripping or condensation water impacts on the power modules for example. Condensation is admissible occasionally only, and on provision that the system is not under voltage. Under no circumstances may condensation residue resulting from occasional condensation be allowed to accumulate due to frequent condensation / drying cycles.

To prevent power semiconductor failure due to condensation, applications must comply with the component-specific climatic requirements. For operation, additional anti-condensation measures such as standstill heating, air conditioning, continuous duty, cooling water temperature control etc., must be taken. According to climate class 3K3, operation must take place in shielded locations which must not be exposed to weather and which have a maximum relative air humidity of 85% and an absolute air humidity of 26 g/m³. Interpreting the climatogram in Figure 6.2.4, this means that at an air temperature of 40°C, for example, the relative air humidity must not exceed 50%.

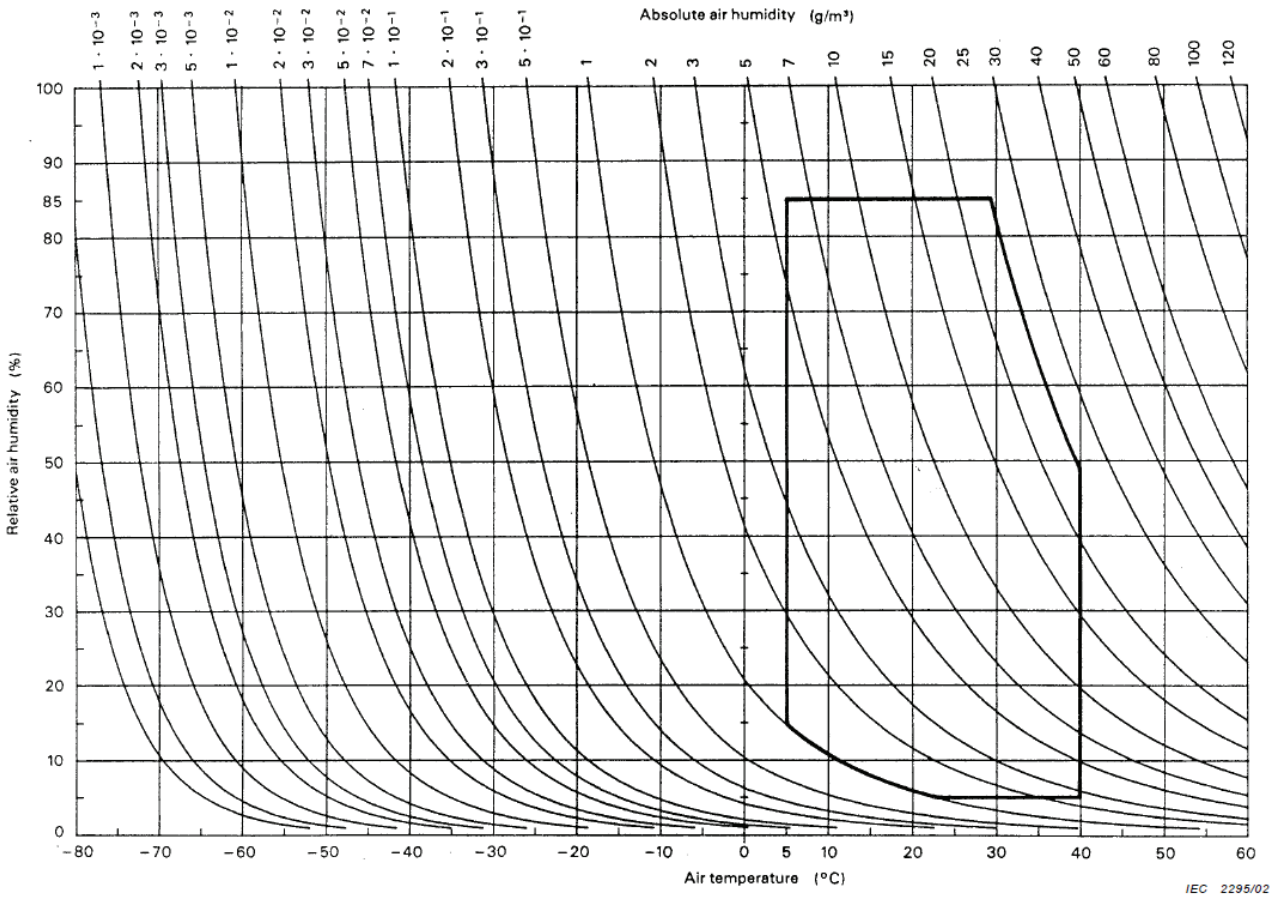


Figure 6.2.4 Climatogram with parameters temperature, relative air humidity and absolute air humidity; the outlined area corresponds to climate class 3K3 (Figure B.3 of EN 60721-3-3, similar to Figure A.7 of EN 50178)

The absolute air humidity changes by barely more than 1 g/m³ within 24 hours (major changes are only noticeable following rainfall). Unless and until devices are hermetically sealed, air is exchanged with the environment. Consequently, the absolute air humidity inside and outside the device is theoretically the same. In practice, however, there are differences due to local temperature variations, since the parameters temperature, absolute air humidity and relative air humidity interact according to the rules of the climatogram.

Example:

At an air temperature of 40°C and a relative air humidity of 20%, the absolute air humidity amounts to 10 g/m³ (the characteristic passing through the intersection of 40°C and 20% relative air humidity is marked accordingly at the top of the diagram). In areas where the air is cooled to 20°C, the relative air humidity will rise to 58% (point at which the 10 g/m³ characteristic intersects the 20°C curve). In order to stay within the tolerances of climate class 3K3, the ambient temperature of the specific module must not fall below 13°C, e.g. by cooling measures (intersection of the 10 g/m³ characteristic with the 85% relative air humidity curve). The condensation process starts as soon as the temperature falls below 11°C (intersection of the 10 g/m³ characteristic with the 100% air humidity curve).

6.2.8 Ramifications for design process

Air humidity is likely to condense at all parts of a device if the device temperature differs from the air temperature to a certain extent; in extreme cases, condensation causes the generation and accumulation of water droplets which might be drawn to moisture-sensitive components such as power semiconductors. Anti-condensation design requirements to avoid moisture-induced failure depend on the application-specific climatic conditions which the device is developed for. Examples of anti-condensation measures are as follows:

a) Case with separate internal air circulation
   - closed system (min. protection degree IP65) with an air-to-air or water-to-air heat exchanger
   - closed system with internal air conditioning (air temperature and air humidity regulation)
   - open system with in-case forced ventilation

   Power semiconductors integrated in such systems are usually liquid-cooled or cooled by heat sinks located outside the case and separated by a seal.

b) Heat sink temperature control using cooling-air intake control
   (fan speed or fan duty cycle)

c) Internal temperature control using interior heating

The diagram in Figure 6.2.5 illustrates the relevant design features with the example of a switchgear cabinet with integrated SKiiP power modules.

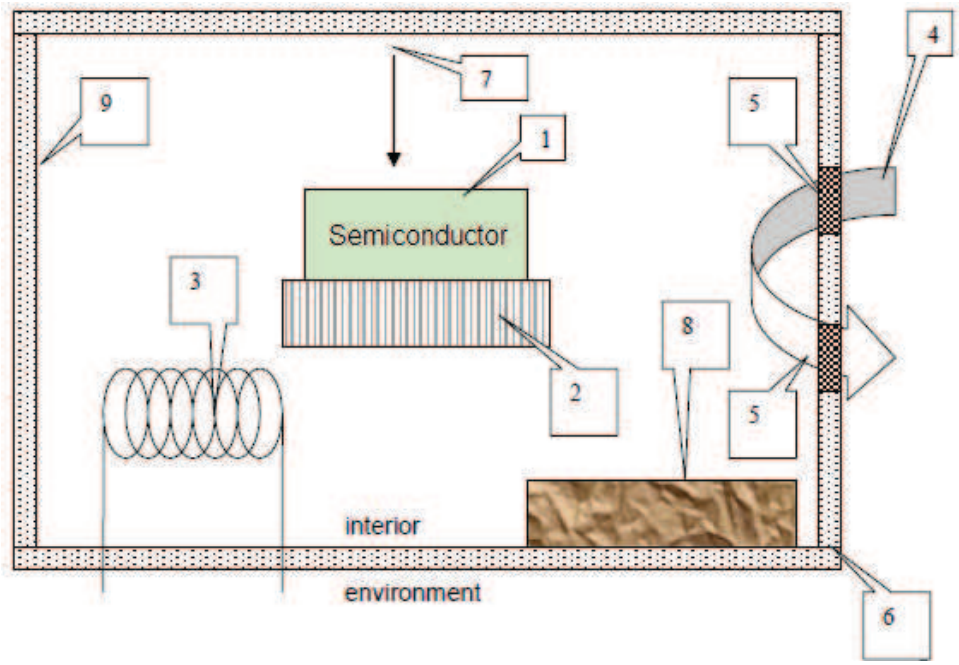


Figure 6.2.5 Design details of a power electronic switchgear cabinet

1. Power module to be protected from moisture
2. Critical zone: Heat sink, heat sink temperature T1, e.g. adjustable with a two-step controller to T1 ≥ T2 → Risk of condensation, if T1 < T2
3. Heating: Interior temperature is adjusted to T2 within the admissible operating temperature range of the components
4. Cooling-air intake to the switchgear cabinet (air flow and air humidity control)
5. Air intake and outlet: Possible chimney effects must be attenuated by way of air channelling to make sure that the cooling air is evenly distributed
6. Case with IP54 protection min.
7. Deflection of water droplets from the case top
8. Optional: Water-absorbing granulate for passive air humidity control
9. Critical zones: Cabinet side panels

In a closed case, surfaces that are colder than the interior air temperature are likely to be affected by condensation or even ice formation. Condensation water is typically generated if the temperature of the interior environment drops to a point where the relative air humidity reaches 100%. The air humidity will then condensate on surfaces with temperatures below the interior temperature (e.g. air intake and outlet, case panels, heat sink). The requirements for ventilation inside the device depend on the respective climatic conditions of use.

The air inside closed interior systems without active air humidity control may absorb water up to saturation state. The absorbable amount of liquid is limited by the interior air volume. If the temperature changes, this process will either continue or be reversed, i.e. water condenses from the air. In such systems, water-absorbing granulate might be used to avoid condensation.

A change in temperature will cause air pressure compensation. Ventilation valves with a defined humidity compensation capability (e.g. Gore Prevent) may be installed in order to prevent moisture from penetrating the closed system as a result of temperature fluctuations.

Heat sink temperature control is recommended for closed systems. To avoid damage due to failure in the sealing system, the air humidity inside the system should be monitored. Systems used in tropical or other high humidity environments should be equipped with active air humidity control system.

Inside switchgear cabinets without closed interiors, areas of condensation exist as a result of the constant supply of fresh air. Provisions must be made to shift these areas to places where condensation, ice formation or water droplets do not have detrimental effects on the system. The temperature of critical live components (such as heat sink, power semiconductors, PC boards etc.) must always exceed the environment temperature. This can be achieved, for example, by way of suitable preheating, interior ventilation and air distribution measures. Condensation water must be collected and suitably deflected from critical components.

When controlling the heat sink temperature, transition states such as low-load operation and standby to operating mode switchover also have to be taken into account, since in such states the above-mentioned requirements can only be fulfilled by reducing the cooling temperature. In standby mode it might make sense to maintain the supply of auxiliary voltage and, if necessary, induce additional heating of the heat sinks and the interior to keep the temperature at a reasonable level.

6.3 Power module assembly

6.3.1 Quality of the heat sink mounting surface

To meet the requirements for thermal contact and thermal transient resistances specified in the datasheets, the heat sink mounting surface must be clean and free of dust and must comply with the specifications as illustrated in the example in Figure 6.3.1:

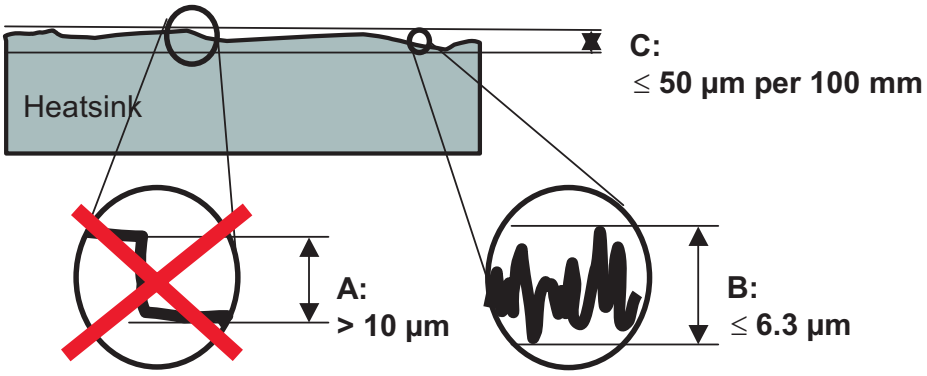


Figure 6.3.1 Mechanical specifications for power module mounting surface (example)

	Unevenness per 10 cm	Roughness R_z	Steps
	(DIN EN ISO 1101) A	(DIN EN ISO 4287) B	(DIN EN ISO 4287) C
Baseplate modules			
SEMITRANS	≤ 50 µm	≤ 10 µm	≤ 10 µm
SEMIPACK, SEMiX, SEMIPONT…4	≤ 50 µm	≤ 10 µm	≤ 10 µm
Modules without baseplate			
MiniSKiiP, SEMIPONT 5/6, SKiM4/5	≤ 50 µm	≤ 6.3 µm	≤ 10 µm
SKiM63/93	≤ 50 µm	≤ 10 µm	≤ 10 µm
SEMITOP	≤ 50 µm	≤ 6.3 µm	no steps

Table 6.3.1 Requirements applicable to heat sink / mounting surface for Semikron modules

6.3.2 Thermal coupling between module and heat sink by means of thermal interface material (TIM)

Due to the unevenness of the mounting surfaces, a gap is left between module and heat sink when mounting a power module onto a cooling surface. With a specific thermal conductivity of $\lambda_{air} \approx 0.03$ W/m·K, air is a poor conductor of heat. The gap therefore has to be filled with another, more effective thermal conductor; cf. Figure 6.3.2.

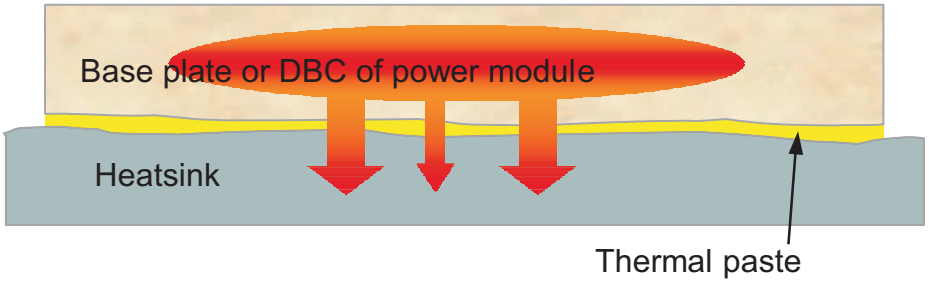


Figure 6.3.2 Heat dissipation from power module to heat sink via a thermal interface material

Different thermally conductive materials are available for this purpose, managing a specific thermal conductivity within the range of $\lambda_{paste} \approx 0.5$ - 6 W/m·K, thus exceeding the thermal conductivity of air by 20 to 200 times.

These materials can be roughly assigned to the following basic types:
- pastes, e.g. thermal pastes with Al_2O_3 or boron nitride (BN) compounds,
- phase change interface materials based on the principle of phase transition (e.g. low-melting metallic compounds) or variation of viscosity (e.g. HiFlow™),
- foils, electrically non-insulating (e.g. SoftfaceTM, glass-fibre reinforced graphite foil, aluminium foil with graphite coating) and electrically insulating (e.g. foil filled with BN or Al_2O_3),
- combined systems such as wax-coated graphite or aluminium foils.

Most commonly used are inexpensive paste systems made up of a flowable compound (e.g. silicone oil) filled with fine, thermally conductive powder.

The following table provides an overview of the specific thermal conductivity of the components of a power module and illustrates the effects the thermal paste conductivity has on the overall system. Thermal paste P12 manufactured by Wacker Chemie AG serves as an example. The R_{th} values indicated depend on the module-specific heat spreading.

Material	Specific thermal conductivity λ [W/(m·K)]	Thickness [µm]	Proportion of R_{th} for SKiM modules
Chip	106	120	2.92%
Chip solder	57	70	3.65%
DBC (copper)	394	300	1.94%
DBC (Al_2O_3)	24	380	32.91%
DBC (copper)	394	300	1.31%
Thermal paste (P12 from WACKER)	0.81	30	57.26%

Table 6.3.2 SKiM module design: material properties and thermal resistance share

As Table 6.3.2 demonstrates, the thermal conductivity of thermal paste does not rate particularly well compared to other components of a power module. The contribution of thermal paste to the overall thermal resistance $R_{th(j-s)}$ of the module amounts to approx. 20-65%, depending on the particular assembly. For this reason, the thermal paste layer has to be as thin as possible and as thick as necessary (Figure 6.3.3).

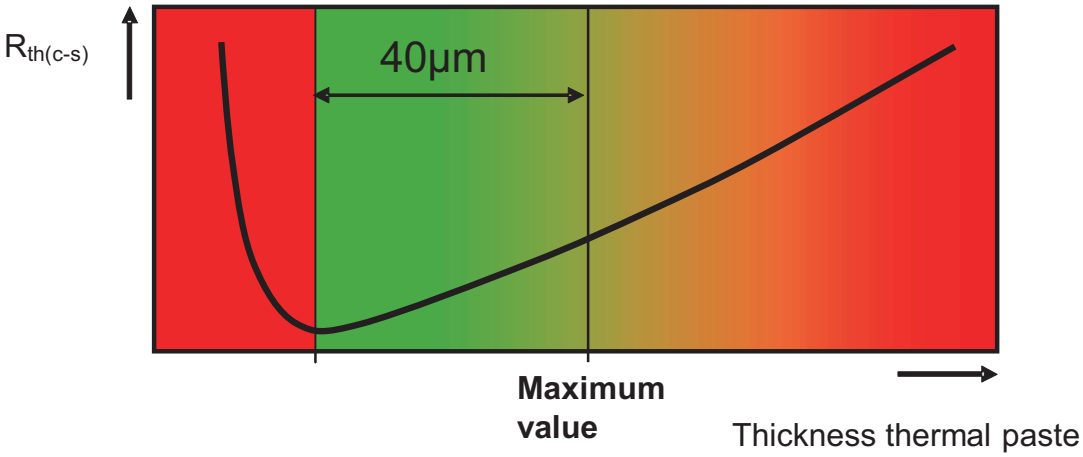


Figure 6.3.3 Dependency of thermal resistance on thermal paste layer thickness

Too thin a thermal paste layer results in air inclusions between the underside of the module and the top of the heat sink, causing a high thermal resistance $R_{th(c-s)}$ or $R_{th(j-s)}$. Beyond the optimum thickness, the thermal resistance $R_{th(c-s)}$ or $R_{th(j-s)}$ increases again in line with the increase in thermal paste layer thickness. This is due to the fact that the specific thermal conductivity λ of the thermal interface material is very low compared to other materials in a power semiconductor module. The minimum value (module on heat sink) is different in each system and has to be determined in suitable tests.

The thermal paste layer thickness, as well as the requirements for heat sink surface quality are given for different module types in the respective mounting instructions.

Recommended thermal paste thickness for SEMIKRON modules with thermal paste P12 (Wacker Chemie AG, silicone-based) and HTC (ELECTROLUBE, silicone-free):

Baseplate modules					
SEMIPACK approx. 50 µm	SEMITRANS approx. 50 µm	SEMiX50… approx. 100 µm	SEMIPONT4 approx. 50 µm		
Modules without baseplate					
MiniSKiiP0 25…40 µm	MiniSKiiP1 35…50 µm	MiniSKiiP2 65…85 µm	MiniSKiiP3 45…65 µm	SEMIPONT5/6 50…55 µm	
SKiM4/5 40...60 µm	SKiM63/93 30…50 µm	SEMITOP1 20…25 µm	SEMITOP1 30…35 µm	SEMITOP3 50…55 µm	SEMITOP4 50…55 µm

Table 6.3.3 Recommended thermal paste layer thicknesses for Semikron modules

The specific thermal conductivity λ of P12 thermal paste recommended by SEMIKRON is at the lower end of the scale. The use of this particular thermal paste is recommended for the following reasons:

- R_{th} test series have proven that the thermal conductivity of a thermal paste in actual application depends not only on its thermal conductivity λ, but also on its specific composition. The larger the filler particles in a thermal paste, the higher the specific thermal conductivity. The particle size of the filler determines the minimum thermal layer thickness. In other words, the thermal paste layer applied cannot be thinner than the largest particles in the paste. After several temperature cycles, a paste with small particles (e.g. P12: particle size 0.04…4 µm) provides almost metal-to-metal contact at points where the contact pressure is particularly high, usually resulting in a substantial reduction in $R_{th(c-s)}$ or $R_{th(j-s)}$.
- The paste is highly resistant to "bleeding" and "drying out".

The following table illustrates the properties of the most important thermal interface materials which have undergone testing at SEMIKRON.

Product name; manufacturer	**Description**	**Containing silicone**	**Conductive**	**Methods of application**	**Applicable thickness of TIM in µm**	**Thermal resistance**	**Specific thermal conductivity λ W/(m*K) (datasheet)**
P12, Wacker	Paste, filler: Al_2O_3	Yes	No	Rolling, screen / stencil printing	10-100	+	0.81
HTC, Electrolube	Paste, filler: Al_2O_3	No	No	Rolling, screen / stencil printing	10-100	+	0.9
PSX-P8, Hala Contec GmbH	Phase changer, filler: aluminium powder	No	No	Rolling, screen / stencil printing	10-100	+	3.4
Keratherm 86/50; Kerafoil	Foil, filler: boron nitride	Yes	No	Manually	120	-	2.9
Q2 Pad; Bergquist	Aluminium foil with graphite coating	Yes	Yes	Manually	152	-	2.5

Product name; manufacturer	Description	Containing silicone	Conductive	Methods of application	Applicable thickness of TIM in µm	Thermal resistance	Specific thermal conductivity λ W/(m*K) (datasheet)
TIC 1000 A, Bergquist	Paste, filler: Al_2O_3	Yes	Yes	Rolling, screen / stencil printing	15-100	O	1.5
TIC 4000, Bergquist	Paste, filler: fluid metal	Yes	yes	Rolling, screen / stencil printing	approx. 100	+	4.0
KU ALC-5, Kunze	Phase-change aluminium foil with wax coating	No	Yes	Manually	approx. 76	O	220
KU ALF; Kunze	Phase-change aluminium foil with wax and graphite coating	No	Yes	Manually	approx. 76	+	220

Table 6.3.4 Types and properties of TIMs (thermal pastes and others)

Methods of thermal paste application

In addition to compliance with the recommended layer thicknesses, care must also be taken to ensure that the thermal paste is applied evenly and homogeneously across the module underside or heat sink surface. Non-homogeneity of the thermal paste layer (in extreme cases: application of one or more thermal paste blobs) may either cause cracks in the DBC substrate or lead to local overheating at spots where air inclusions remain between module underside and heat sink surface. This is particularly true when mounting modules with no baseplate, since, in such cases, the heat sink serves almost exclusively as thermal capacitance to manage transient thermal loads.

Application using a rubber roller

Applying thermal paste with a rubber roller may lead to sufficient results, provided the procedure is carried out by experienced professional and suitably trained staff. This process, however, involves shortcomings such as non-homogeneity, poor reproducibility and risk of contamination. An ultrathin layer of thermal paste must be applied homogeneously either to the module or the heat sink contact surface using a hard rubber roller. Layer thicknesses for the different SEMIKRON product groups are specified in the table above.

Stencil and screen printing

In stencil printing, a stainless steel stencil and stainless steel scraper are normally used to print the thermal interface material on the module or heat sink. The "effective" thermal paste layer thickness is determined by the ratio of filled area to non-filled area, as well as by the height of the dots applied, which in turn is determined by the thickness of the stencil itself.

In screen printing, Monolen PET meshes and a polyurethane scraper with a shore hardness of 75 are commonly used. The thickness of the yarn and the number of yarns per unit of length determine the thickness of the thermal paste layer.

In stencil and screen printing, far better results can be achieved than in the roller process, provided the printing is done automatically. Performing this process manually can lead to substantial process fluctuations.

Control check on thermal paste layer thickness

The thickness of a thermal paste layer can be measured directly or indirectly. An indirect way of measuring the thickness is, for example, to weigh the thermal paste by performing a Tara weight measurement using suitable scales. An example of a direct contact-free measurement of the thermal paste layer is a measurement using an optical profilometer such as the µSCAN from Nano Focus. Other measurement equipment that can be used to measure the thermal paste layer directly includes, for example, thickness gauges such as wet film combs or wet film wheels; the downside of these, however, is that they may destroy the layer in places.

The edges of the wet film comb (e.g. ZND 2050-2054 from Zehntner) have support teeth and measurement teeth which have a defined distance to the surface. The comb is held perpendicular to the surface and run across the surface horizontally (Figure 6.3.4); when this is done, some paste residue will be left on the teeth of the comb that are beneath the surface of the paste layer.

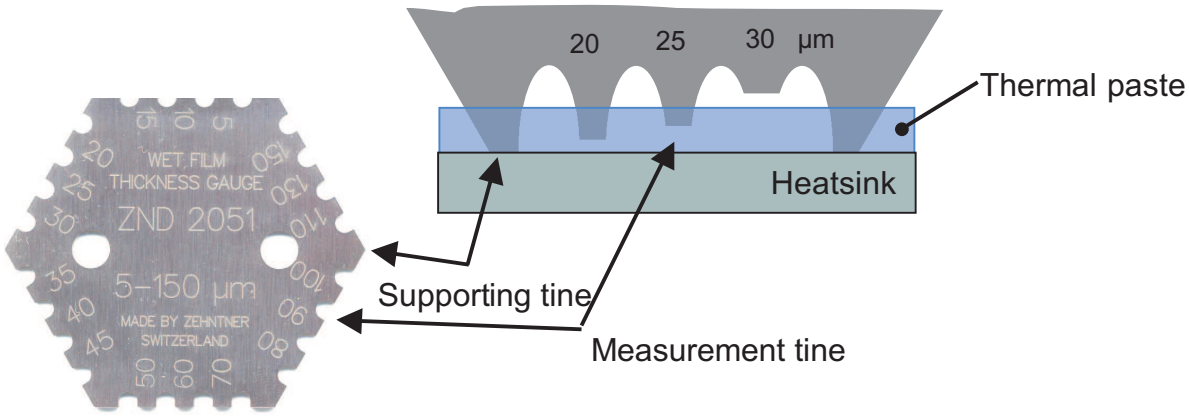


Figure 6.3.4 Measuring the thermal paste layer using wet film comb ZND 2050 – 2054

A wet film wheel (e.g. ZWW 2100-2108 from Zehntner, see Figure 6.3.5) produces more accurate results in thermal paste layer thickness tests than a wet film comb. The wet film wheel consists of two support discs which are positioned at the outer edges, and one measurement disc located between the support discs. The measurement wheel is rolled across the surface that has been coated with thermal paste. The thermal paste layer thickness can be read from the scale taken from the end of the wet segment of the middle measurement disc.

Figure 6.3.5 Wet film wheel ZWW 2100-2108

Thermal paste applied by the manufacturer

Starting with the MiniSKiiP product range, SEMIKRON now offers selected product types with pre-applied thermal paste on request (Figure 6.3.6). This process is currently qualified for thermal paste P12 (Wacker Chemie AG, silicone-based) and HTC (ELECTROLUBE, silicone-free).

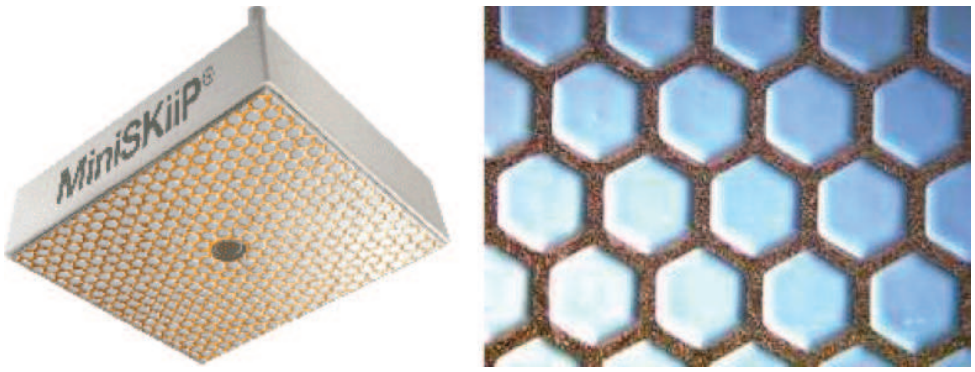


Figure 6.3.6 MiniSKiiP supplied with thermal paste layer

Thanks to special blister packaging (Figure 6.3.7),the coated components are transportable in compliance with ESD requirements and the thermal paste layer is not at risk of being damaged. In this blister packaging, the modules are storable up to 18 months at temperatures of between -25…+60°C and at an air humidity of 10…95%. Further processing on the MiniSKiiPs can be done directly from the blisters.

Figure 6.3.7 Transportation and storage packaging for coated MiniSKiiP modules

6.3.3 Mounting power modules onto heat sink

We recommend the use of steel DIN screws (strength class 4.8) with washers / spring washers or combined screw-and-washer assemblies to secure the modules. The torque range M_s specified in the datasheets must be complied with. The screws must be tightened evenly and diagonally to the torque M_s in several steps. For modules with baseplate, it may be of advantage to wait for some hours and then re-tighten the screws with the indicated torque. This may be necessary since the contact pressure may cause some of the thermal paste to ooze out.

Details on the mechanical dimensions of the fasteners, tightening sequences and torques are provided in the given "Mounting Instructions" and "Technical Explanations" retrievable under www.semikron.com in the product-specific datasheet menu.

In the case of power modules without baseplate, the consequences of non-compliance with mounting instructions are far more serious than for modules with baseplate. For this reason, for some of these modules the mounting screws are tightened in two steps, as specified in the "Mounting Instructions". Automated screwdrivers (if used) should have a maximum rotation speed of 250 min^{-1} and soft torque limitation (no torque peaks, such as with pneumatic screwdrivers). The loosening torque applicable to the mounted assembly will be much lower than the original tightening torque due to relaxation of the case and thermal coupling medium flow. The fixing screws of modules without baseplate, however, must not be re-tightened (non-permissible step!).

6.3.4 Electrical connections

Safe electrical connection of pressure-contact power modules without baseplate (MiniSKiiP, SKiM) at the customer's site may be guaranteed only after the modules have been fixed properly with the specified tightening torques. The same applies to disc-type cells. Furthermore, the electrical terminals must not be subjected to mechanical stress before the module is mounted onto the heat sink (SKiM) or until the module is being mounted on the heat sink (MiniSKiiP).

Screw-in depth limits and permissible tightening torques M_t specified in the datasheets for power modules with screw terminals must be observed. Details on connection elements and further instructions are provided in the given "Mounting Instructions" and "Technical Explanations" retrievable under These also include the maximum permissible forces effective at the electrical terminals and are given for each product group in the three dimensions of the coordinate system (Figure 6.3.8).

Moreover, SKiiP and SKiM pressure contact IGBT modules run the risk of inadmissible relief of the pressure contacts if the effective forces are exceeded due to unsuitable connections.

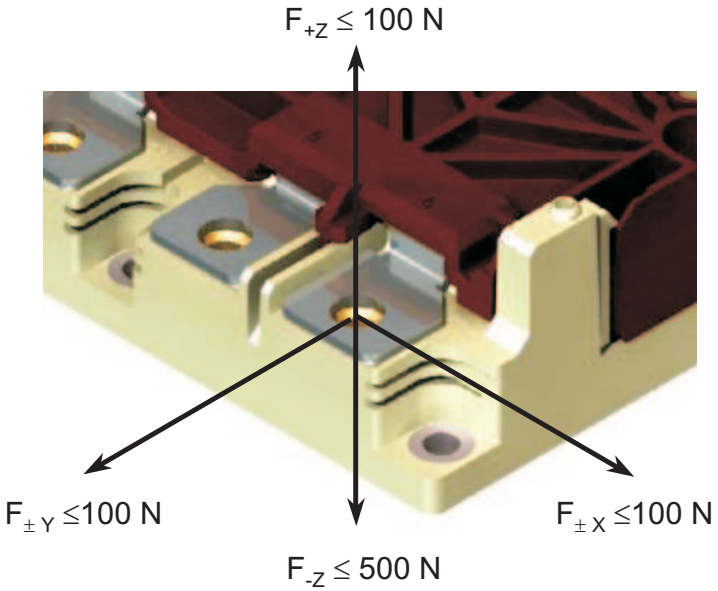


Figure 6.3.8 Maximum permissible forces effective at the terminals of a SKiM63/93 module

The DC-side power connection of IGBT and MOSFET modules should be realized using symmetrically arranged DC-link busbars to ensure minimum stray inductance, thus minimising switching overload. To avoid parasitic oscillations, pulse-proof low-inductance film capacitors are attached to the DC terminals in most applications (e.g. collector TOP-IGBT / emitter BOT-IGBT); cf. chapter 5.4.

Principally, the connection path between driver terminals and driver circuit must be as short as possible to minimise stray inductances, electromagnetic interferences and oscillations. This is particularly important in IGBT and MOSFET modules. Cable connections (e.g. gate and emitter connection cables) are to be twisted where possible; parallel arrangement of driver cabling and power busbars must be avoided at all cost.

Connection of MiniSKiiP, SEMiX and SKiM contact springs

All power (MiniSKiiP) or driver terminals (SEMiX, SKiM) are connected to the PCB using contact springs. Consequently, electrical load (also for testing purposes) must be applied to these power modules only after proper connection to the PCB. Details on PCB mounting and the relevant mounting material are provided in the "Mounting Instructions". Information on screw diameters, screw-in depths and tightening torques is provided in the product-specific datasheets as well.

The following key requirements apply to PCBs (also refer to the particular "Technical Explanations" and "Mounting Instructions"):

- PCB material, e.g. FR4
- Conductor thickness in compliance with IEC 326-3
- Tried and tested PCB surface finishes for the conductors pads: electroless nickel immersion gold (Ni Au) with > 5 µm Ni, hot air levelling tin (HAL Sn), chemical tin (chem.I Sn), tin / lead (Sn Pb)
- Due to the intrinsic instability of passivated finishes, SEMIKRON does not recommend the use of PCBs with organic solderability preservatives coating (OSP) finish for the conduction pads.
- Overall low-inductive layout (where possible +/- coplanar conductor paths with maximum Cu surface, gate and emitter conductor paths in parallel and as close to each other as possible)
- Conductor pads with no vias
- No inadmissible tin bulges which might neutralize the spring effect (if required, a cover should be used during flow soldering process)
- Conductor pads free of solder resists, solder flux, contamination, oil or other substances (if a no-clean flux is used, PCB cleaning can be omitted).
- Compliance with EN 50178 - A7.1.8.5, e.g. use of press-in bushes to connect the power terminals to the PCB in order to avoid contact problems due to PCB material flow

Requirements for solder connections

All SEMIKRON power modules with solder connectors are suitable for wave soldering.

The soldering instructions provided in the datasheets and the "Mounting Instructions" must be adhered to. The soldering temperature in the manual soldering process of tab terminals (soldering tool must be grounded!) must not exceed

T_{solder} = 235 ± 5°C / ≤ 5 s.

For SEMIPONT 5 or 6 and SEMITOP power modules, as well as for SEMiX 33c auxiliary terminals the maximum permissible soldering temperature is T_{solder} = 260°C / ≤ 10 s zulässig. For machine soldering, SEMIKRON specifies the soldering profile illustrated in Figure 6.3.9. The maximum preheating temperature has to be kept under or equal to the maximum storage temperature. The maximum soldering temperature is 260°C for 10 s max.

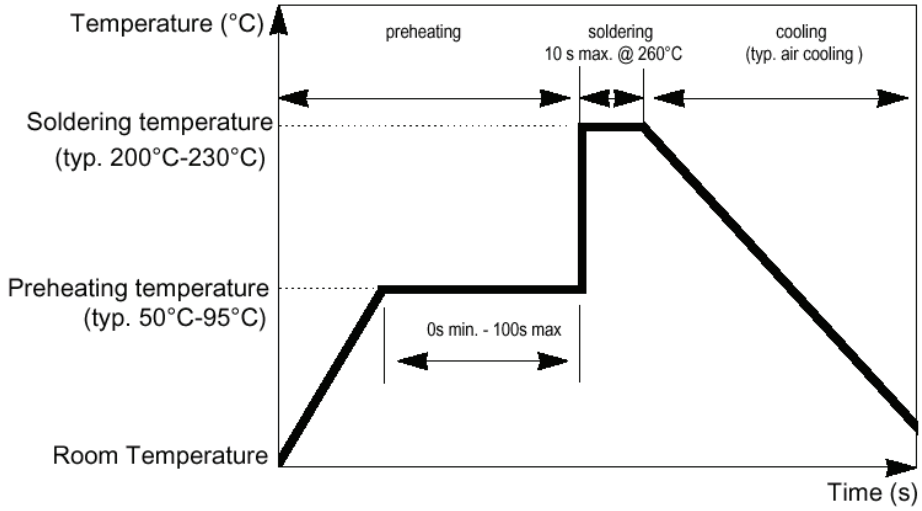


Figure 6.3.9 Wave soldering profile for SEMIKRON power modules

6.4 Mounting of capsule diodes and thyristors (disc cells)

Disc cell housings possess two thermal contact surfaces. For maximum current capacity yields, double-sided cooling (DSC) is usually used. For this purpose, the cell is clamped between two heat sinks using a clamping fixture as described below; in lower load applications, single-sided cooling (SSC) is used as a standard practice as well.

The electrical contact between component and heat sink is established for disc cells, as well as components with screw-in housings via the thermal contact surfaces. This means that contact

surfaces have to be able to fulfil both thermal and electrical requirements. They must be even and smooth (maximum permissible unevenness 10 µm, maximum surface roughness 6.3 µm). Individual nicks, notches or scratches are acceptable, provided no flash protrudes. The surfaces must be free of impurities and dust.

Within just a few minutes of exposure to air, an oxide layer will form on aluminium. Due to this oxide layer, the electrical contact resistance will increase many times over, which may lead to contact corrosion after extended periods of current passage. For this reason, the contact surfaces of non-zinc-plated aluminium heat sink areas have to be mechanically cleaned directly before the disc cell is mounted. A fine wire brush immersed in thermal paste or an abrasive sponge will be suitable for this purpose (e.g. "Scotchbrite" from 3MCompany). Abrasive residues have to be removed thoroughly from the treated surfaces; immediately afterwards, an ultrathin layer of thermal paste without (insulating) powder fillers, e.g. ELECTROLUBE GX, must be applied to the contact surfaces.

The clamping fixture must be designed such that one of the two heat sinks can move freely during mounting. For this purpose, one of the two mounting clamps forms a pivoting bearing (contact between spherical and flat surface). The second mounting clamp should be attached to the respective heat sink in such a way that it does not deform when the screws are tightened.

The heat sink which forms the pivoting bearing with the clamping fixture must be able to move freely. This means that no rigid mechanical connections to other heat sinks or support elements are mounted on this heat sink. The electrical connection between this heat sink and the corresponding busbar must be established with a flexible lead.

Figure 6.4.1 shows a diagram of a clamping fixture.

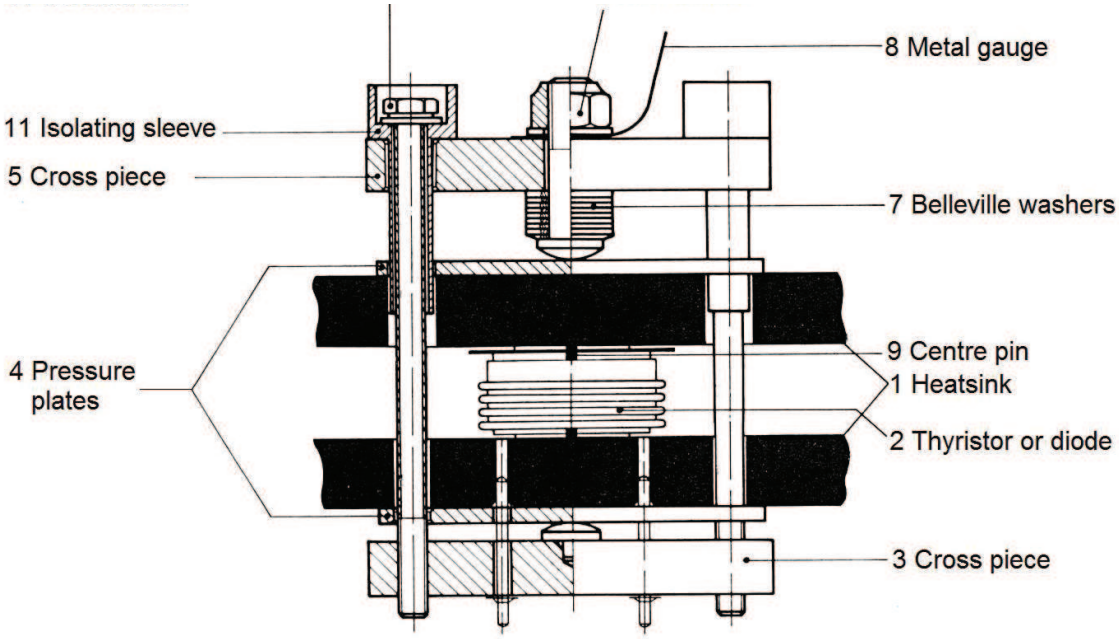


Figure 6.4.1 Capsule thyristor / diode mounted with "MC" clamping fixture

The following mounting instructions apply to "MC" clamping fixtures available at SEMIKRON as an accessory to some of their capsule diodes and thyristors:

The clamping fixture must be able to establish the contact pressure specified in the capsule datasheet. Firstly, the heat sink contact surfaces for the component and the power supply must undergo thorough pre-treatment, as described above. Thorough cleaning with a solvent will do for plated surfaces. Both surfaces are then coated with a thin layer of thermal paste, e.g. using a rubber roller. The contact surface of the capsule diode / thyristor should now be firmly pressed onto the mating surface of the respective heat sink by hand, turning it back and forth whilst doing so. The centre pins (9) must be placed in position before. When the diode / thyristor is removed from the heat sink, the mating surfaces must be uniformly coated with thermal paste. If this is not the case, the surfaces must be recoated with a thin layer of thermal paste.

The clamping fixture is then positioned such that the cross piece (5) and pressure plate (4) with the tension bolts (10) is at the top. The cross piece (3) and pressure plate (4) is inserted from below, and the two tension bolts (10) are tightened alternately until a slight resistance is felt. Now check that both cross pieces (3) and (5) are parallel. To do so, it is sufficient to measure the lengths of the ends of the bolts protruding from the bottom of the two cross pieces (3). The bolt ends must be equal in length. The two tension bolts (10) should now be tightened alternately up to the point where the metal gauge (8) can be easily moved. Under no circumstances should the tension bolts be tightened beyond this point, as doing so would mean that the permissible mounting force has been exceeded. For the same reason, the pre-set nut (6) of the Belleville washer assembly (7) should never be adjusted. The metal gauge (8) is secured to prevent it from falling out.

As an alternative to such clamping fixtures, which may be installed by the customer, more simple mechanical clamping systems are used for the SEMISTACK product range (see chapter 5.5), which must be mounted in presses using force measuring devices only. These clamping systems are not suitable for changing disc cells on the part of the customer.

7 Software tool as a dimensioning aid

7.1 SemiSel

As an additional service to aid customers with product selection and loss and temperature calculations SEMIKRON has introduced the extensive free software program SEMISEL to its homepage to enable customers to perform numerous simulations with power-electronic switches under a wide range of operating conditions. This program went live in 2001 and has since been continually expanded and improved on. The description below refers to the functions included in version 3.1 of the program. The calculation possibilities that the tool offers range from simple product suggestions for one nominal operating point to driver and heatsink specifications and complex calculations for complete load cycles. One of the main criteria when developing this program was to have a very simple user interface that would enable users to quickly familiarize themselves with the program and produce quick "estimations" on the required component application at the same time.

This tool is suitable for the following:
- selecting power semiconductors when designing new converters;
- specifying the necessary cooling measures;
- calculating efficiency rates;
- calculating maximum temperatures and thermal cycles for module life time calculations;
- comparing products with different semiconductor technologies and of different generations;
- selecting the optimum price-to-performance-to-size ratio by comparing existing degrees of freedom in the system design (switching frequency, cooling measures, overload capability);
- risk assessments as regards variation in both components and electric circuit parameters.

Some of the pros and cons of this type of calculation and simulation tool in comparison to commercial circuit simulators are listed in the table below.

Advantages	**Disadvantages**
High-level availability thanks to ready access via the Internet	Limited to certain key application areas, e.g. PWM inverters, which is why its suitability for new developments in the field of circuit technology and niche applications is somewhat limited
High-speed thanks to analytical calculations for cycle duration and the use of mean value models	Time functions of current and voltage cannot be calculated (switching edges); instead mean values over periodic functions only
Product database continuously updated and maintained by manufacturer	Simplified modelling, e.g. of the on-state characteristic as a linear equation or simplified thermal equivalent circuits
Application engineers' expertise in the area of power semiconductors made available to a broad range of users	User has no influence on the calculation algorithms used, but has to assume they are suitable for his purpose

Table 7.1.1 Pros and cons of online simulation tools for loss and temperature calculations

7.1.1 Program functions

The program offers the user 4 different tools to aid him in the semiconductor configuration and design process. An overview of these is given in the table below.

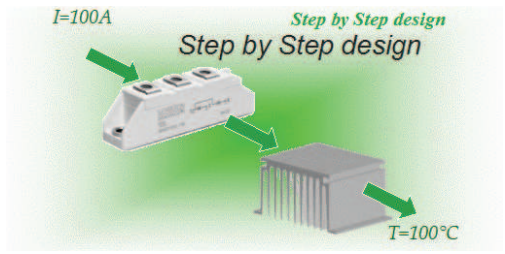
In "Step by Step" design, the power electronic circuit is specified step by step in accordance with the user's requirements and the thermal calculations then performed. This tool offers the greatest freedom and flexibility, as well as scope of influence on the calculations.	
The “Device Proposal” option gives the user a number of suitable components for a single chosen nominal operating point.	
DriverSel is used to select a suitable SEMIKRON IGBT driver. The switching frequency, gate charge, peak and mean driver current values, and IGBT reverse voltage are taken into account in the selection.	
The "Stacksel" function is used to test the suitability of pre-fabricated stacks comprising power semiconductors and heatsink from the SEMIKRON Solution Centres.	

Table 7.1.2 SemiSel program functions

7.1.2 Using SemiSel

The process steps involved in the most commonly used "step by step" circuit design tool are shown in Figure 7.1.1.

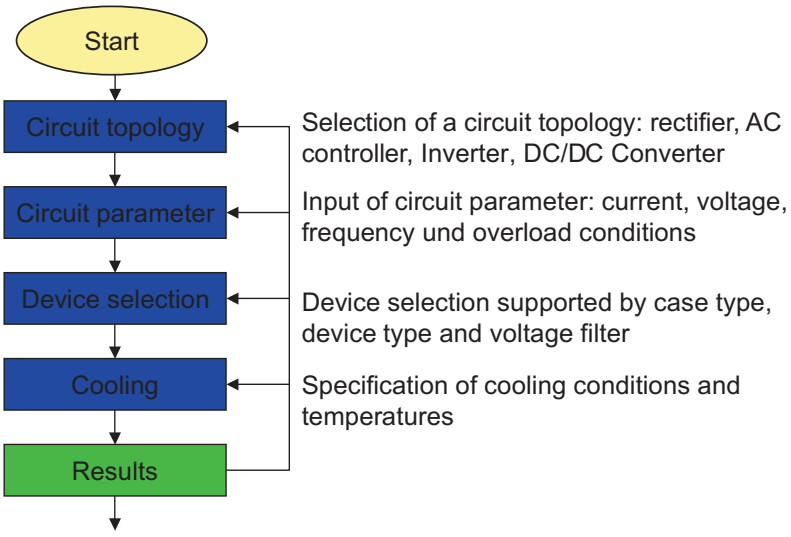


Figure 7.1.1 Program steps in "step by step" dimensioning

The user can choose between 14 different topologies to find the circuit most suited to his requirements. Diagrams showing the circuit topology facilitate selection. In the next steps, the electric parameters for the circuit are entered, a suitable component is selected and the cooling conditions specified. The losses and chip temperatures occurring under these conditions in the chosen component are then calculated. If changes have to be made, the user can easily return to the parameter fields, make the desired changes and re-calculate on this basis.

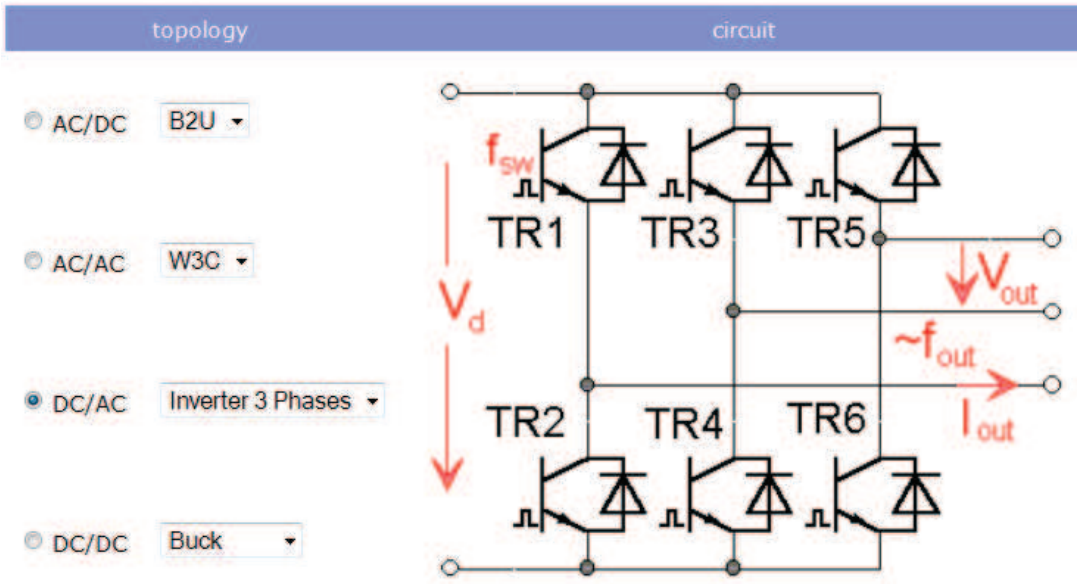


Figure 7.1.2 Selecting circuit topology – three-phase inverter in this case

With the exception of driver selection, the other program parts are similar in structure; one difference is that in the other parts, some of the entry fields do not exist owing to pre-defined entries and simplifications, meaning the calculation can be performed immediately. The program features an extensive user help function. Further application tips and details on loss and temperature calculations for individual circuits are provided in the previous chapters on design and configuration of power transistors (chapter 5.2) and rectifier components (chapter 4.1).

7.2 Semiconductor models

This section looks at semiconductor models used in electric circuit simulation. Before starting to look for suitable models, the following question must always be answered: What properties does my model have to have to meet the simulation task at hand?

- Analysis of the circuit operating principle: Ideal switch models
- Determination of losses and temperatures: Static models and state models
- Examination of individual switching processes: Physical model of semiconductor and behaviour models

7.2.1 Static models

Static models are switch models to which a static characteristic can be assigned. Triggering is done via logic signals. These models are suitable for analysing circuit operating principles and calculating losses in low-frequency circuits (e.g. line rectifiers). The forward characteristic of a semiconductor is typically:

- Line approximation
- Exponential function (with series resistance)
- Quadratic function
- Tables with deposited measuring points

7.2.2 State models

The online simulation tool SemiSel can be used to perform simple power dissipation and temperature calculations. If necessary, however, state models can simply be generated using the data provided in the datasheets. These models use static characteristics and equations or "look-up tables" for switching losses and switching times. They are suitable for all simulation tools that are compatible with state graphs [81], [82], [83]. On request, SEMIKRON can provide assistance creating the datasets for these models. These models are not suitable for examining switching processes; they have ideal switching edges, which is why no parasitic inductances may be factored into the simulation circuit.

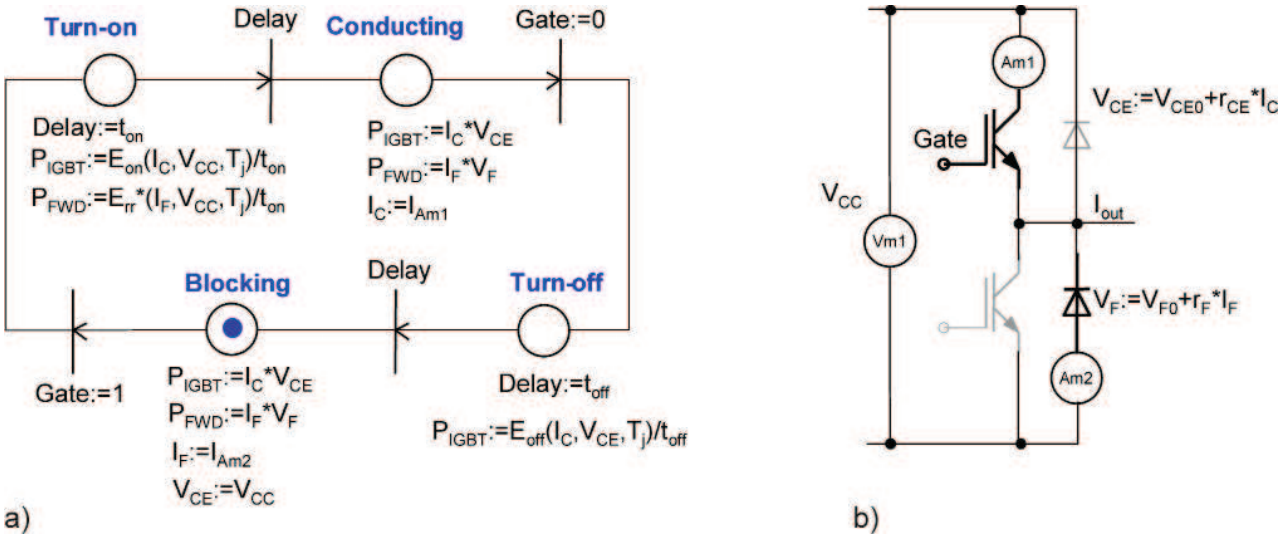


Figure 7.2.1 Semiconductor modelling using state models; a) State description; b) Electric equivalent circuit

A model such as this comprises an "ideal" switch with a logic drive signal ("Gate"=1/0 in Figure 7.2.1), for which the power dissipation is calculated in 4 different states. In the example shown, the states (shown as circles) are given as IGBT switching states. If a transition (line) applies, e.g. if the signal "Gate = 1" is set, the marked, active state moves to the next state. In the example here, the marker would move from "Blocking" to "Turn-on". During this state, switching losses are caused; here, turn-on losses for the IGBT and turn-off losses for the diode. After a delay time t_{on}, the marker moves to the next state - "Conducting"- where conducting losses occur. These losses are continuously calculated from the circuit current and the on-state voltage of the IGBT. The on-state voltage can be stored in the form of a characteristic or using a line approximation, or assigned to the component. If the driver signal is set to "0", the component goes over to "Turn-off" state, in which turn-off losses occur. After a delay time t_{off}, the IGBT goes back to the original state - "Blocking" - where the conducting losses of the diode are calculated. This completes the switching cycle. The switching losses can likewise be stored as a characteristic and read out for the current switching parameters. For simple cases, the equations for switching energies given in chapter 5.2.1 are used, since the junction temperature and DC link voltage dependencies are not available in the datasheet as characteristics.

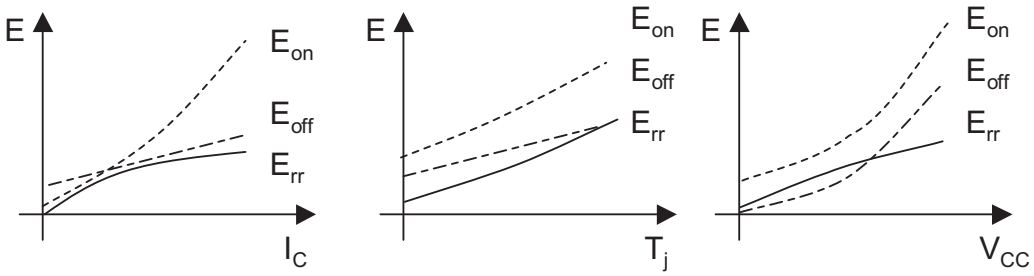


Figure 7.2.2 Example of dependency of switching losses on I_c,T_j and V_{CC}

Current sources in the thermal equivalent circuits can then be fed with the calculated losses (Figure 7.2.3). The resistances correspond with the R_{th} values of the thermal impedances. The capacitances are calculated from $C_{th} = t/R_{th}$. The temperature is then fed back to the switching parameters and affects the switching losses and on-state voltage of the models. For the PWM inverter, it suffices to calculate the losses and temperatures for one IGBT and one diode; this is owing to the symmetry here.

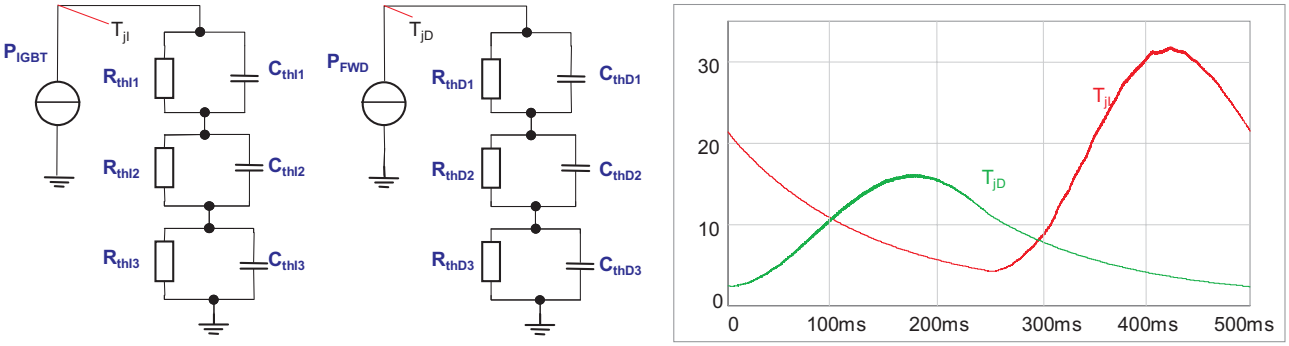


Figure 7.2.3 Thermal equivalent circuit and example of calculated temperature characteristic of a PWM inverter with 2 Hz output frequency

7.2.3 Physical models of semiconductor and behaviour models

Both model types claim to provide a realistic picture of the switching behaviour in dependence of the driver and load conditions. They are highly suitable for investigating individual switching processes. Owing to the differences in time scale (some 10^{-9} s for a single switching process ↔ heating in 100 s), these models are not suitable for simulating heat build-up. Even just a few periods of a converter output frequency require substantial calculation time.

While physical models draw upon equations used in semiconductor physics, behaviour models describe the semiconductors more like a blackbox would. Combined forms are feasible for use in any increments. For the physics-based semiconductor models, the main problem lies in the fact that the parameters are difficult to obtain, meaning that these models are ultimately not very practical for users. They do, however, offer the advantage that they provide valid results across a broad operating range. Behaviour models are more easily parameterised with datasheet values and measured switching processes; one shortcoming here, however, is that they are often applicable to a limited range only. Both models, however, confirm that switching behaviour is essentially determined by parasitic elements (L_S) in the semiconductor environment. The merit of the given model can therefore only be assessed on the basis of how easily elements of the packaging can be included in the model.

An example of a behaviour model is shown in Figure 7.2.4 [84]. The static behaviour is simulated using two characteristics: saturation characteristic and the transfer characteristic. The saturation characteristic is assigned to diode D1 and causes the voltage drop $V_{CE}=f(I_C)$. The transfer characteristic controls the current source parallel to D2 in dependence of the applied gate voltage. The current in the IGBT rises and falls in line with the charge and discharge of the gate-emitter capacitance C_{GE} via the gate. The most important element when modelling the dynamic behaviour is the non-linear Miller capacitance which ensures feedback of the collector-emitter voltage to the gate.

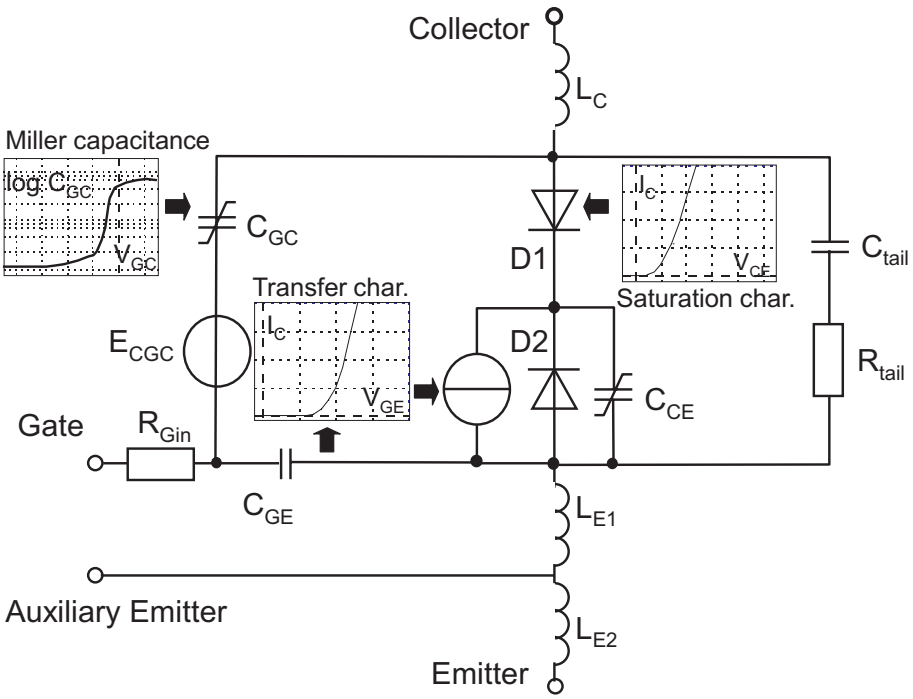


Figure 7.2.4 Example of an IGBT behaviour model with equivalent circuit elements [84]

The models can be optimised for certain operating points to ensure that they correctly model switching times and losses. They do not, however, sufficiently describe the switching properties for any given switching condition to malfunction/failure, meaning that the amount of time and work that goes into producing these models is by no means justified. What is more, no adapted models exist for latest-generation Trench IGBT, despite the fact that the switching behaviour of these components differs greatly from that of the predecessor NPT-IGBT generation. This is why, at present, SEMIKRON is not offering semiconductor models for circuit simulation.

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Abbreviations used in SEMIKRON Datasheets

Acronym	English	German
$(di/dt)_{cr}$	Critical rate of rise of on-state current	Kritische Stromsteilheit
$(dv/dt)_{cr}$	Critical rate of rise of off-state voltage	Kritische Spannungssteilheit
$\int$ vdt	Voltage-time integral at no load	Spannungs-Zeit-Fläche bei Leerlauf
a	Maximum acceleration under vibration	Zulässige Beschleunigung beim Schalten
b	Width of the module base	Breite des Modulbodens
B2	Two-pulse bridge connection	Zweipuls-Brückenschaltung
B25/85	Exponent of temperature sensor equation	Exponent für Temperatursensor Gleichung
B6	Six-pulse bridge connection	Sechspuls-Brückenschaltung
$BW_{Ioutsens}$	Bandwith of output current sensing	Bandbreite der Strommessung
BW_{TBsens}	Bandwith of temperatur sensing on driver board	Bandbreite der Temperatur-Messelektronik
$BW_{TCSsens}$	Bandwith of temperatur sensing on ceramic-substrate	Bandbreite des Temperatursensors
$BW_{VDCsens}$	Bandwith of DC-link-voltage sensing	Bandbreite der Zwischenkreisspannungserfassung
C_{CHC}	Capacitance chip-case (baseplate)	Kapazität Chip-Gehäuse (Grundplatte)
C_{DC}	Capacitance of DC-link capacitor bank	Kapazität des Zwischenkreiskondensators
C_{eqvl}	Equivalent capacitance of a DC-link capacitor bank	Ersatzkapazität einer Zwischenkreiskondensatorbank
C_{ies}	Input capacitance, output short-circuited (IGBT)	Eingangskapazität, Ausgang kurzgeschlossen (IGBT)
C_{IN}	Input capacitance	Input capacitance
C_{iss}	Input capacitance, output short-circuited (MOS)	Eingangskapazität, Ausgang kurzgeschlossen (MOSFET)
C_j	Junction capacitance	Sperrschichtkapazität
C_L	Load capacitor	Lastkondensator
C_{max}	Maximum value of reservoir capacitor	Größter Ladekondensator (bei größerem C Strom verringern)
C_{oes}	Output capacitance, input short-circuited (IGBT)	Ausgangskapazität, Eingang kurzgeschlossen (IGBT)
C_{oss}	Output capacitance, input short-circuited (MOSFET)	Ausgangskapazität, Eingang kurzgeschlossen (MOSFET)

C_{ps}	Coupling capacitance, primary to secondary winding	Koppelkapazität zwischen Primär- und Sekundärwicklung
C_{res}	Reverse transfer capacitance (Miller capacitance) (IGBT)	Rückwirkkapazität (Miller-Kapazität) (IGBT)
C_{rss}	Reverse transfer capacitance (Miller capacitance) (MOSFET)	Rückwirkkapazität (Miller-Kapazität) (MOSFET)
D	Duty cycle. D =f · tp	Tastverhältnis D=f · tp
di/dt	change of current per time	Stromänderung pro Zeiteinheit
di_D/dt	Rate of fall ot the drain current (MOSFET)	Abklingsteilheit des Drainstroms (MOSFET)
di_F/dt	Rate of rise of the forward current (Diode)	Anstiegssteilheit des Durchlassstromes (Diode)
di_F/dt	Rate of fall of the forward current (Diode)	Abklingsteilheit des Durchlassstromes (Diode)
di_G/dt	Rate of rise of gate current	Anstiegssteilheit des Durchlassstromes (Thyr.)
di_T/dt	Rate of rise of Thyristor current	Anstiegssteilheit des Steuerstroms
di_T/dt	Rate of fall of Thyristor current	Abklingsteilheit des Durchlassstromes (Thyr.)
DSC	Double sided cooling	Beidseitige Kühlung
d_{tp}	thickness of thermal paste	Dicke der Wärmeleitpaste
dv/dt	change of voltage per time	Spannungsänderung pro Zeiteinheit
dV/dt	Volume flow	Volumenstrom
E_{cond}	Energy dissipation during conduction time	Verlustenergie während der Stromflusszeit
ED	Intermittend duty	Relative Einschaltdauer (Aussetzbetrieb) = te/tsp
E_{off}	Energy dissipation during turn-off	Verlustenergie während der Abschaltzeit
E_{on}	Energy dissipation during turn-on	Verlustenergie während der Einschaltzeit
E_P	Maximum permissible non-repetitive peak pulse energy (rectangular pulse 2 ms)	Höchstzulässiger nichtperiodischer Impulsenergie Spitzenwert (Rechteckpuls 2 ms)
E_{rr}	Energy dissipation during reverse recovery (diode)	Verlustenergie während der Sperrverzögerungszeit
E_{RSM}	Non repetitive peak reverse avalanche energy	Einmalig zulässige Avalanche Energie
E_{tp}	dielectric strength of thermal paste	Durchschlagsfestigkeit der Wärmeleitpaste
f	Operating frequency	Betriebsfrequenz
F	Mounting force	Montagekraft
f_{Fan}	AC voltage frequency for fan operation	Frequenz der Lüfterspannung
f_{max}	Maximum frequency	Maximale Frequenz

f_{out}	Output requency of a circuit	Ausgangsfrequenz einer Schaltung
f_{sw}	Switching frequency	Puls-, Schaltfrequenz
Fu	Recommended fuse (fast acting)	Empfohlene Sicherung (flink bzw. überflink)
g_{fs}	Forward transconductance	Übertragungssteilheit
g_{tp} (γ)	specific gravity of thermal paste	Spezifisches Gewicht der Wärmeleitpaste
HIN	PWM signal input high side switch	Eingang PWM Signal TOP Schalter
l	Length of the heatsink profile	Länge des Kühlprofils
i^2t	i2t value	Grenzlastintegral
$I_{AC\text{-}terminal}$	AC-Terminal current	Wechselstrom-Anschluss Strom
$I_{analogOUT}$	Current sensor refference value (SKiiP)	Nennstrom der Stromsensor-auswertung (SKiiP)
I_C	Continuous collector current	Kollektor-Gleichstrom
I_{CES}	Collector-emitter cut-off current with gate-emitter short-circuited	Kollektor-Emitter-Leckstrom, Gate-Emitter kurzgeschlossen
I_{Cnom}	Nominal collector current	Kollektor Nennstrom
I_{CRM}	Repetitive peak collector current	Periodischer Kollektor Spitzenstrom
I_{CSM}	Non-repetitive peak collector current	Nichtperiodischer Kollektor-Spitzenstrom
I_D	Direct output current (of a rectifier connection)	Ausgangsgleichstrom (einer Gleichrichterschaltung)
I_D	Continuous drain current (MOSFET)	Drain-Dauergleichstrom (MOSFET)
$I_{D(CL)}$	Direct output current with capacitive load (limiting value)	Ausgangsgleichstrom bei C-Last (Grenzwert)
I_{DD}	Forward off-state current (Thyristor)	Gleichsperrstrom (in Vorwärtsrichtung)
I_{DM}	Peak value drain current	Spitzenwert Drainstrom
I_{DR}	Continuous reverse drain current (inverse diode forward current)	Drain-Gleichstrom in Rückwärtsrichtung (Durchlassstrom der Inversdiode)
I_{DRM}	Peak value of reverse drain current, (inverse diode forward current)	Spitzenwert des Drainstroms in Rückwärtsrichtung (Durchlassstrom der Inversdiode)
I_{DSS}	Drain-Source cut-off current with gate source short-circuited	Drain-Source-Leckstrom, Gate-Source kurzgeschlossen
I_E	Continuous emitter current	Emitter-Gleichstrom
i_F	Forward current (actual value)	Durchlassstrom (Augenblickswert)
$I_{F(CL)}$	Mean forward current with capacitive load	Dauergrenzstrom bei kapazitiver Last

$I_{F(OV)}$	Overload forward current	Überlast-Durchlassstrom
I_{Fan}	Current for fan operation	Lüfterstrom
I_{FAV}	Mean forward current	Mean forward current
I_{FM}	Peak forward current	Durchlassstrom-Spitzenwert
I_{FN}	Recommended mean forward current	Empfohlener Durchlassstrom-Mittelwert
I_{FRM}	Repetitive peak forward current	Periodischer Spitzenstrom
I_{FRMS}	RMS forward current	Durchlassstrom-Effektivwert
I_{FSM}	Surge forward current	Stoßstrom-Grenzwert
I_{G}	Gate current	Gatestrom
I_{GD}	Gate non-trigger current	höchster nichtzündender Gatestrom
I_{GES}	Gate-emitter leakage current, collector emitter short-circuited	Gate-Emitter-Leckstrom, Kollektor-Emitter kurzgeschlossen
I_{Goff}	max. turn-off output current (driver)	Max. Ausgangs-Abschaltspitzenstrom (Treiber)
I_{Gon}	max. turn-on output current (driver)	Max. Ausgangs-Einschaltspitzenstrom (Treiber)
I_{GSS}	Gate-source leakage current, drain-source short-circuited	Gate-Source-Leckstrom, Kollektor-Emittler kurzgeschlossen
I_{GT}	Minimum guaranteed gate trigger current	Mindestzündstrom für sicheres Einschalten
I_{H}	Hold current	Haltestrom
I_{iH}	Input signal current (High)	Eingangssignalstrom (High)
I_{L}	Latching current	Einraststrom
I_{M}	Highest peak current obtainable at a rise time lower than 1 µs (pulse transformers)	Höchster bei einer Anstiegszeit unter 1µs erreichbarer Spitzenstrom (Impulsübertrager)
$I_{max(EO)}$	Maximum Error Output Current	Maximaler Strom des Fehlerausgangs
I_{N}	Nominal current	Empfohlener Gleichstrom
$I_{N(CL)}$	Recommended direct output current with capacitive load	Empfohlener Gleichstrom bei C-Last
I_{nom}	Nominal current	Nennstrom
I_{Omax}	Max. output current (driver)	Max. Ausgangsstrom (Treiber)
I_{out}	Output current of a circuit	Ausgangsstrom einer Schaltung
I_{outAV}	Output average current (driver)	Ausgangsstrommittelwert (Treiber)
$I_{outPEAK}$	Output peak current (driver)	Ausgangsstromspitzenwert (Treiber)
$I_{outsens}$	AC sensing range	Wechselstrom Messbereich
$I_{outtrip}$	AC over current trip level	Überstrom-Fehler Grenzwert

$I_{overload}$	Overload current for a specified time	Überlaststrom für eine bestimmte Zeit
$I_{peak(1)}$	magnitude of the first hamonic of a current	Amplitude der ersten Harmonischen eines Stromes
I_R	Reverse current	Off-state current
I_{RD}	Direct reverse current (Thyristor)	Gleichsperrstrom in Rückwärtsrichtung (Thyristor)
I_{RMS}	Maximum r.m.s current of a complete AC-controller circuit	Maximaler Effektivstrom eines Wechselspannungsstellers
I_{rr}	Reverse recovery current (measuring condition for t_f and t_{rr})	Sperrverzögerungsstrom (Messbedingung für t_f und t_{rr})
I_{RRM}	Peak reverse recovery current	Rückstromspitze
I_{RSM}	Maximum non-repetitive peak reverse current (avalanche diodes)	Höchstzulässiger nichtperiodischer Stoßspitzensperrstrom (Avalanche-Dioden)
I_S	Supply current primary side	Versorgungsstrom primärseitig (Treiber)
I_{S0}	Supply current primary side (driver) at no load	Versorgungsstrom prim. Leerlauf (Treiber)
i_T	On-State current (instantaneous value)	Durchlassstrom (Augenblickswert)
I_T	(Direct) on-state current	Durchlass(gleich)strom
$I_{T(OV)}$	Overload on-state current	Durchlass-Überstrom
I_{TAV}	Mean on-state current	Mean forward current
I_{TM}	Peak on-state current	Durchlassstrom-Spitzenwert
ITRIP	Comperator input for current measurement	Komperatorschwellwert für Strommess-Eingang
I_{TRIPLG}	Ground fault current trip level (SKiiP)	Erdschlussfehler Stromgrenzwert (SKiiP)
I_{TRIPSC}	Over current trip level (SKiiP)	Überstrom-Fehler Grenzwert (SKiiP)
I_{TRMS}	RMS on-state current	Durchlassstrom-Effektivwert
I_{TSM}	Surge on-state curren	Stoßstrom-Grenzwert
I_z	Tail current (IGBT)	Schweifstrom (IGBT)
L	inductance	Induktivität
L_{CE}	Parasitic collector-emitter inductance	Parasitäre Kollektor-Emitter-Induktivität
L_{DS}	Parasitic drain-source inductance	Parasitäre Drain-Source-Induktivität
L_{ext}	External circuit inductance (short circuit)	Externe Schaltungsinduktivität (im Kurzschluss)
LIN	PWM singnal input low side switch	Eingang PWM Signal BOTTOM Schalter
L_p	Inductance of the primary winding at 1 kHz	Induktivität der Primärwicklung bei 1 kHz

L_s	Stray inductance	Streuinduktivität
L_{ss}	Parasitic stray inductance (Transformer secundary side)	Streuinduktivität (Sekundärseite Übertrager)
l_{tp} (λ)	thermal conductivity of thermal paste	Wärmeleitfähigkeit der Wärmeleitpaste
M	Mounting torque	Anzugsdrehmoment bei der Montage
M_1	Torque for mounting the semiconductor to the heatsink	Anzugsdrehmoment für die Montage des Bauelements auf dem Kühlkörper
M_2	Torque for mounting the busbars to the semiconductor	Anzugsdrehmoment für die Montage der Stromschienen auf dem Bauelement
M_{ac}	Mounting torque for AC terminals	Anzugsdrehmoment für AC - Anschluss
M_{dc}	Mounting torque for DC terminals	Anzugsdrehmoment für DC - Anschluss
M_s	Mounting torque on heat sink	Anzugsdrehmoment für Montage auf Kühlkörper
M_t	Mounting torque for terminals	Anzugsdrehmoment für Anschlüsse
n	specified number	Anzahl von…
N	Maximum number of serie connected silicon elements	Höchstzahl der Siliziumelemente in Reihenschaltung
N_p/N_s	Ratio of winding primary to secondary	Übersetzungsverhältnis Windungszahl prim/sec.
Ø d	Contact diameter of capsule devices	Kontaktdurchmesser bei Scheibenzellen
P_{AV}	Maximum permissible average power dissipation	Hochzulässige Dauerverlustleistung Mittelwert
$p_{coolant}$	pressure of coolant	Druckabfall Kühlflüssigkeit
P_D	Power dissipation of one component	Verlustleistung eines Bauelements
P_{Fan}	Power consumption of fan	Leistungsaufnahme des Lüfters
P_{FAV}	Mean forward power dissipation	Mittlere Durchlassverlustleistung
P_{FM}	Peak forward power dissipation	Spitzenwert der Durchlassverlustleistung
P_G	Peak gate power dissipation	Spitzenwert der Steuerverlustleistung
P_R	Reverse power dissipation	Sperrverlustleistung
P_{RAV}	Mean reverse power dissipation	Mittlere Sperrverlustleistung
P_{RRM}	Peak repetitive reverse power dissipatiom	Periodischer Spitzen-Sperrverlustleistung
P_{RSM}	Non-repetitive peak reverse power dissipation	Stoßspitzen-Sperrverlustleistung

P_{TAV}	Mean on-state power dissipation (Thyristor)	Mittlere Durchlass-Verlustleistung (Thyristor)
P_{tot}	Total power dissipation	Gesamt-Verlustleistung
P_W	Water pressure	Wasserdruck
P_{ZSM}	Non repetitive peak power dissipation (Zener diodes)	Stoßspitzen-Verlustleistung (Zener Dioden)
Q_f	Charge recovered during the reverse current fall time	Ladung, die während der Rückstrom-Fallzeit abfließt
Q_G	Gate charge (IGBT; MOSFET)	Gate-Ladung (IGBT; MOSFET)
Qout/pulse	Output charge per pulse (Driver)	Ausgangsladung pro pulse (Treiber)
Q_{rr}	Reverse recovery charge	Sperrverzögerungsladung
$R_{CC'+EE'}$	Resistance of the interconnections between terminals and die	Kompletter Anschlusswiderstand Terminal-Chip-Terminal
r_{CE}	On-State slope resistance (IGBT)	Bahnwiderstand IGBT
R_{CE}	Resistor for V_{CE} monitoring	Widerstand für V_{CE}-Überwachung (Treiber)
$r_{DS(on)}$	Drain-source on-resistance (MOSFET)	Drain-Source-Einschaltwiderstand (On-Widerstand) MOSFET
rec.	Rectangular current waveform	Rechteckförmiger Stromverlauf
rec. 120	Rectangular current pulse, 120° conduction angle	Rechteck-Strompuls, 120° Stromflusswinkel
R_{EX}	Auxiliary emitter series resistor (parallel IGBT)	Widerstand vor Hilfsemitter (für parallelgeschaltete IGBT)
r_F	On-state slope resistance, forward slope resistance (Diode)	Durchlass- Ersatzwiderstand (Diode)
R_G	Gate circuit resistance	Externer Gate Widerstand
R_{Gint}	Internal gate resistance	Interner Gate Widerstand
R_{Goff}	External gate series resistor at switch-off (MOSFET, IGBT)	Gatevorwiderstand zum Abschalten
$R_{Goffmin}$	Minimum value of an external switch-off gate resistor (Driver)	Minimalwert für einen Externen Ausschalt-Gatewiderstand
R_{gon}	External gate series resistor at switch-on (MOSFET, IGBT)	Gatevorwiderstand zum Einschalten
R_{Gonmin}	Minimum value of an external switch-on gate resistor (Driver)	Minimalwert für einen Externen Einschalt-Gatewiderstand
R_{GS}	Gate-source resistance (MOSFET)	Gate-Source-Widerstand (MOSFET)
$RH_{storage}$	storage humidity	Luftfeuchte bei Lagerung
R_{IN}	Input resistance	Eingangswiderstand
R_{iso}	Insulation resistance	Isolationswiderstand
R_L	Load resistance	Lastwiderstand

$R_{min(CL)}$	Minimum series resistor für capacitive load	Minimaler Schutzwiderstand bei C-Last
R_P	Recommended parallel resistor for a series connection of demiconductors	Empfohlener Parallelwiderstand bei Reihenschaltung von Halbleitern
R_p	D.C. resistance of the primary winding	Gleichstromwiderstand der Primärwicklung
R_s	D.C. resistance of each secondary winding	Gleichstromwiderstand jeder Sekundärwicklung
$R_{softcharge}$	Recommendet DC-Link charge resistor	Empfohlener Ladewiderstand für kapazitiven Zwischenkreis
r_T	On-state slope resistance, forward slope resistance (Thyristor)	Durchlass-Ersatzwiderstand (Thyristor)
RTD	Resistor for interlock dead time (Driver)	Beschaltungswiderstand für Verriegelungstotzeit (Treiber)
$R_{th(c-a)}$	Thermal resistance case to ambient	Thermischer Widerstand Gehäuse-Umgebung
$R_{th(c-s)}$	thermal resistance case to heat sink	Thermischer Widerstand Gehäuse-Kühlkörper
$R_{th(j-a)}$	Thermal resistance junction to ambient	Thermischer Widerstand Sperrschicht-Umgebung
$R_{th(j-c)}$	Thermal resistance junction to case	Thermischer Widerstand Sperrschicht-Gehäuse
$R_{th(j-c)D}$	Thermal resistance junction to case inverse diode	Thermischer Widerstand Sperrschicht-Gehäuse Inverse-Diode
$R_{th(j-c)FD}$	Thermal resistance junction to case free wheeling diode	Thermischer Widerstand Sperrschicht-Gehäuse Freilaufdiode
$R_{th(j-r)}$	Thermal resistance junction to reference point (temperature sensor)	Thermischer Widerstand Sperrschicht-Bezugspunkt (Temperatur Sensor)
$R_{th(j-s)}$	Thermal resistance junction to sink	Thermischer Widerstand Sperrschicht-Kühlkörper
$R_{th(j-s)}D$	Thermal resistance junction to sink (Diode)	Thermischer Widerstand Sperrschicht-Kühlkörper (Diode)
$R_{th(j-s)}I$	Thermal resistance junction to sink (IGBT)	Thermischer Widerstand Sperrschicht-Kühlkörper (IGBT)
$R_{th(j-T)}$	Thermal resistance junction to terminal	Thermischer Widerstand Sperrschicht-Anschluss
$R_{th(r-w)}$	Thermal resistance thermal trip-cooling water	Thermischer Widerstand Thermostat Kühlwasser
$R_{th(s-a)}$	Thermal resistance heat sink to ambient	Thermischer Widerstand Kühlkörper-Umgebung
R_{tp}	resistivity of thermal paste	Elektrischer Widerstand der Wärmeleitpaste

R_{TS}	resistance of a temperature sensor	Widerstand des Temperatursensors
sin.	Sinusoidal current waveform	Sinusförmiger Stromverlauf
sin. 180	Half sinewaves, 180° conduction angle	Sinus-Halbschwingungen, 180° Stromflusswinkel
SSC	Single sided cooling	Einseitige Kühlung
T_a	Ambient temperature	Umgebungs-, Kühlmitteltemperatur
T_c	Case temperature	Gehäusetemperatur
tcond	Conducting time	Einschaltdauer, Stromführungszeit
$T_{coolant}$	Coolant temperature	Temperatur des Kühlmediums
T_{cop}	Case operating temperature	Gehäusetemperatur im Betrieb
t_d	Delay time	Verzögerungszeit
$t_{d(err)}$	Propagation delay time on ERROR	Fehlersignalverzögerungszeit
$t_{d(err)io}$	ERROR input-output propagation delay time (driver)	Fehlereingang-Ausgangsverzögerungszeit (Treiber)
$t_{d(off)}$	Turn-off delay time	Abschalt-Verzögerungszeit
$t_{d(off)io}$	Input-output turn-off propagation delay time (driver)	Eingangs-Ausgangs-Abschaltverzögerungszeit (Treiber)
$t_{d(on)}$	Turn-on delay time	Einschalt-Verzögerungszeit
$t_{d(on)io}$	Input-output turn-on propagation delay time (driver)	Eingangs-Ausgangs-Einschaltverzögerungszeit (Treiber)
T_{err}	Max. temperature for setting ERROR	Max. Grenztemperatur für Fehlersignale
t_f	Fall time	Abfallzeit
t_{fr}	Forward recovery time	Durchlass-Verzögerungszeit
t_{gd}	Gate controlled delay time	Zündverzögerungszeit
t_{gr}	Gate controlled rise time	Durchschaltzeit
T_j	Junction temperature	Sperrschichttemperatur
t_{off}	Turn-off time	Abschaltzeit
t_{on}	Turn-on time	Einschaltzeit
T_{op}	Operating temperature range	Operating temperature range
t_p	Pulse duration	Impulsdauer
t_{pRESET}	Min. pulse width ERROR memory RESET time	Min. Fehlerspeicher Rücksetzzeit
t_q	Circuit commutated turn-off time (thyristor)	Freiwerdezeit
t_r	Rise time	Anstiegzeit

t_R	Reverse blocking time: $t_R = t_c - t_p$	Zeit, während der Sperrspannung anliegt: $t_R = t_c - t_p$
T_r	Reference point temperature (temperature sensor)	Bezugspunkttemperatur (Temperatur Sensor)
t_{rr}	Reverse recovery time	Sperrverzögerungszeit
T_s	Heatsink temperature	Kühlkörper-Temperatur
t_{SC}	Short circuit time	Kurzschlusszeit
T_{sold}	Solder temperature	Löttemperatur
T_{stg}	Storage temperature	Lagerungs-Temperatur
t_{stg}	storage time	Lagerzeit
t_{TD}	Interlock time	Verriegelungszeit
T_{Trip}	Trip level of over temperature protection (SKiiP)	Ansprechschwelle für Übertemperaturschutz (SKiiP)
T_{vj}	(Virtual) junction temperature	Ersatzsperrschichttemperatur
T_w	Water temperature	Wassertemperatur
t_z	Tail time (IGBT)	Schweifzeit (IGBT)
$V_{(BR)}$	Avalanche breakdown voltage	Durchbruchspannung (Avalanche-Spannung)
$V_{(BR)CES}$	Collector-emitter breakdown voltage, gate-emitter short circuited	Kollektor-Emitter-Durchbruchspannung, Gate-Emitter kurzgeschlossen
$V_{(BR)DSS}$	Drain-source breakdown voltage, gate-source short circuited	Drain-Source-Durchbruchspannung, Gate-Source kurzgeschlossen
$V_{(TO)}$	Threshold voltage Thyristor	Schleusenspannung Thyristor
v_{air}	Air velocity	Luftgeschwindigkeit
V_{air}	Air volume	Luftmenge
V_{air}/t	Air flow	Luftdurchsatz
V_{CC}	Collector-emitter supply voltage	Kollektor-Emitter-Versorgungsspannung
V_{CE}	Collector-emitter voltage	Kollektor-Emitter-Spannung
$V_{CE(clamp)}$	Collector-emitter clamping voltage during turn-off	Begrenzte Kollektor-Emitter-Spannung beim Abschalten
V_{CE0}	Collector-emitter threshold voltage (static)	Kollektor-Emitter-Schleusenspannung (statisch)
V_{CEdyn}	Dynamic threshold voltage for collector-emitter voltage monitoring (driver)	dyn. V_{CE}-Überwachungsschwellspannung
V_{CES}	Collector-emitter voltage with gate-emitter short circuited	Kollektor-Emitter-Spannung bei kurzgeschlossenen Gate-Emitter-Anschlüssen
V_{CEsat}	Collector-emitter saturation voltage	Kollektor-Emitter-Sättigungsspannung

V_{CEstat}	Static threshold voltage for collector-emitter voltage monitoring (driver)	stat. V_{CE}-Überwachungsschwellspannung
$V_{ChopperError}$	Chopper error voltage level	Chopper Fehlermeldungsspannung
$V_{ChopperOff}$	Chopper deactivation voltage level	Chopper Deaktivierungsspannung
$V_{ChopperOn}$	Chopper activation voltage level	Chopper Aktivierungsspannung
V_D	Direct output voltage (bridge rectifier)	Gleichgerichtete Spannung (Brückengleichrichter)
V_{DCTRIP}	Trip level of DC link voltage monitoring (SKiiP)	Schwellspannung der Zwischenkreisüberwachung (SKiiP)
V_{DD}	Direct off-state voltage (thyristor)	Gleichsperrspannung in Vorwärtsrichtung (Thyristor)
V_{DD}	Drain-source supply voltage (MOSFET)	Drain-Source-Versorgungsspannung (MOSFET)
V_{DGR}	Drain-gate voltage with specified input resistance	Drain-Gate-Spannung bei angegebenem Eingangswiderstand
V_{DRM}	Repetitive peak off-state voltage	Periodische Spitzensperrspannung (in Vorwärtsrichtung)
V_{DS}	Drain-source voltage	Drain-Source Spannung
V_{DSS}	Drain-source voltage with gate-source short circuited	Drain-Source Spannung bei kurzgeschlossenen Gate-Source-Anschlüssen
V_{EC}	Emitter-Collector voltage	Emitter-Kollektor Spannung
V_{EE}	Emitter supply voltage	Emitter-Betriebsspannung
v_F	Forward voltage (instantaneos value)	Durchlassspannung (Augenblickswert)
V_F	Forward voltage	On-state voltage
V_{F0}	Forward threshold voltage (Diode)	Schleusenspannung Diode
V_{Fan}	Operating voltage fan	Lüfter-Betriebsspannung
V_G	Gate voltage	Gaterspannung
$V_{G(off)}$	Turn-off gate voltage level (driver)	Gateabschaltspannung (Treiber)
$V_{G(on)}$	Turn-on gate voltage level (driver)	Gateeinschaltspannung (Treiber)
V_{GD}	Gate non-trigger voltage	Untere Zündspannung (höchste nichtzündende Spannung)
V_{GE}	Gate-emitter voltage	Gate-Emitter-Spannung
$V_{GE(th)}$	Gate-emitter threshold voltage	Gate-Emitter Schwellenspannung
V_{GES}	Gate-emitter voltage, collector-emitter short-circuited	Gate-Emitter-Spannung, Kollektor-Emitter kurzgeschlossen

V_{GS}	Gate-source voltage	Gate-Source Spannung
$V_{GS(th)}$	Gate-source threshold voltage	Gate-Schwellenspannung
V_{GSS}	Gate-source voltage, drain-source short circuited	Gate-Source Spannung, Drain-Source kurzgeschlossen
V_{GT}	Gate trigger voltage	Zündspannung
V_{iH}	Input signal voltage (HIGH) max.	Eingangssignalspannung (HIGH) max.
V_{in}	Input voltage	Eingangsspannung
Visol	Insulation test voltage (r.m.s.)	Isolations-Prüfspannung (Effektivwert)
$V_{isol(12)}$	Isolation test voltage (r.m.s. /1 min.) output 1 - output 2 (driver)	Isolations-Prüfspannung (eff. 1 min.) Ausgang 1 - Ausgang 2
$V_{isol(IO)}$	Isolation test voltage (r.m.s. /1 min.) input-output (driver)	Isolations-Prüfspannung (eff. 1 min.) Eingang-Ausgang
V_{isolPD}	Partial discharge extinction voltage	Teilentladungsaussetzspannung
V_{iT-}	Input threshold voltage (LOW) max.	Maximale Eingangssignalsschwellspannung (LOW)
V_{iT+}	Input threshold voltage (HIGH) min.	Minimale Eingangssignalsschwellspannung (HIGH)
V_{M}	Peak pulse voltage	Impuls-Spitzenspannung
V_{oH}	Logic HIGH output voltage (driver)	Signalausgangsspannung (HIGH) (Treiber)
V_{oL}	Logic LOW output voltage (driver)	Signalausgangsspannung (LOW) (Treiber)
V_{out}	Output voltage	Output voltage
V_{R}	(Direct) reverse voltage	Sperr(gleich)spannung (in Rückwärtsrichtung)
V_{RD}	Direct reverse voltage	Gleichsperrspannung (in Rückwärtsrichtung)
V_{RGM}	Peak reverse gate voltage	Rückwärts-Spitzensteuerspannung
V_{RGO}	No-load reverse gate voltage	Rückwärts-Steuerspannung im Leerlauf
V_{RRM}	Repetitive peak reverse voltage	Periodische Spitzensperrspannung (in Rückwärtsrichtung)
V_{RSM}	Non-repetitive peak reverse voltage	Stoßspitzensperrspannung in Rückwärtsrichtung
V_{S}	Supply voltage primary (for gate driver)	Versorgungsspannung
V_{S1}	Supply voltage stabilized	stabilisierte Versorgungsspannung
V_{S2}	Supply voltage non stabilized	nicht stabilisierte Versorgungsspannung
V_{SD}	Negative source-drain voltage (inverse diode forward voltage)	Source-Drain-Spannung in Rückwärtsrichtung

v_T	On-state voltage (instantaneous value)	Durchlassspannung (Augenblickswert)
V_T	On-state voltage (Thyristor)	Durchlassspannung (Thyristor)
V_{VRMS}	Alternating input voltage (r.m.s. value)	Eingangswechselspannung (Effektivwert)
V_w	Water volume per unit time	Wassermenge in der Zeiteinheit
V_w	Water volume	Wassermenge (Volumen)
V_{WW}	Maximum alternating working voltage between windings (r.m.s. value) (pulse transformer)	Höchstzulässige Betriebswechselspannung zwischen den Wicklungen (Effektivwert)
w	Weight	Gewicht
W1	Single phase a.c. controller connection	Einphasige Wechselwegschaltung (antiparallel)
W3	Three phase a.c. controller connection	Dreiphasige Wechselwegschaltung (antiparallel)
Z_{th}	Transient thermal impedance	Thermische Impedanz
$Z_{th(c-a)}$	Transient thermal impedance case to ambient	Thermische Impedanz Gehäuse-Umgebung
$Z_{th(j-c)}$	Transient thermal impedance junction to case	Thermische Impedanz Sperrschicht-Gehäuse
$Z_{th(j-c)FD}$	Transient thermal impedance junction to case of the freewheeling diode	Thermische Impedanz Sperrschicht-Gehäuse der Freilaufdiode
$Z_{th(j-r)}D$	Transient thermal impedance junction to reference (sensor) inverse Diode	Thermische Impedanz Sperrschicht-Temperatursensor der Freilaufdiode
$Z_{th(j-r)}I$	Transient thermal impedance junction to reference (sensor) IGBT	Thermische Impedanz Sperrschicht-Temperatursensor der IGBT
$Z_{th(j-s)}$	Transient thermal impedance junction to heat sink	Thermische Impedanz Sperrschicht-Kühlkörper
$Z_{th(r-a)}$	Transient thermal impedance reference (sensor) to ambient	Thermische Impedanz Temperatursensor - Umgebung
$Z_{th(s-a)}$	Transient thermal impedance heat sink to ambient	Thermische Impedanz Kühlkörper - Umgebung
Z_{thp}	Transient thermal impedance under pulse conditions	Pulswärmewiderstand
Δp	Pressure drop	Druckdifferenz
Θ	Conduction angle	Stromflusswinkel

Application Manual Power Semiconductors

Today, IGBT and power MOSFET modules are instrumental in power electronic systems and are increasingly gaining ground in new fields. This goes hand in hand with the ever increasing need for rectifier diodes and thyristors as cost-efficient means of connecting to the power supply grid. This application manual is intended to assist users with component selection and application. This manual contains basic explanations and background information on semiconductor physics where needed to provide a better understanding of the application possibilities and limits. A larger section of the manual contains descriptions of different packaging technologies, examining the different impacts on module properties and ratings in field applications. This section is rounded off with statements on component reliability and service life, as well as the relevant test procedures.

The manual also explains the structure of data sheets and provides useful tips on how to interpret data sheet specifications. An important focus of the manual is the examination of application-specific aspects which must be taken into account in component selection and application. This includes, for example, electric circuits for the most important operating scenarios, driver technology and component protection, thermal dimensioning and heat sink solutions, notes on parallel and series circuits, notes on optimum power layouts with regard to parasitic elements, as well as requirements associated with certain ambient conditions.

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