A Practical Approach to Thermal Modeling and Validation of 3D ICs

Miroslav Cupak[1], Herman Oprins[1], Geert Van der Plas[1], Pol Marchal[1], Bart Vandevelde[1], Adi Srinivasan[2], and Edmund Cheng[2]

[1] *IMEC vzw, Leuven, BELGIUM*

[2] *Gradient Design Automation Inc., Santa Clara, CA, USA*

Notice of Copyright

ARTICLE: Thermal Modeling and 3D

A Practical Approach to Thermal Modeling and Validation of 3D ICs

Miroslav Cupak[1], Herman Oprins[1], Geert Van der Plas[1], Pol Marchal[1], Bart Vandevelde[1], Adi Srinivasan[2], and Edmund Cheng[2]

[1] *IMEC vzw, Leuven, BELGIUM*
[2] *Gradient Design Automation Inc., Santa Clara, CA, USA*

Abstract— 3D stacking of dies is an enabler for further miniaturization and increase of functionality. Individual dies are thinned down aggressively – down to approximately 20 um – and glued on top of each other. With such 3D ICs, the same power dissipation will lead to higher temperatures in a stacked-die package compared to a single-die package. Hence, there is a need to perform detailed thermal analysis in various phases of 3D IC design. Thermal analysis should be included in the design loop to assess the thermal consequences of design iterations and verify the final design before signoff. From a new methodology characterization point of view, for layouts consisting mainly of test structures, thermal analysis plays an important role in final chip verification. This article presents a practical approach to perform detailed thermal analysis of stacked-die packages, interconnections between the dies, and the complete electrical design layout. The methodology is demonstrated on a two stacked die structure in a BGA package.

Index Terms— Thermal modeling, thermal-aware design, 3D stacked ICs, experimental validation, thermal test chip.

I. INTRODUCTION

3D stacking of dies is an enabler for further miniaturization and increase of functionality. Individual dies are thinned down aggressively – down to approximately 20 µm – and are glued on top of each other. With such 3D ICs, the same power dissipation will lead to higher temperatures in a stacked-die package compared to a single-die package. As a consequence, detailed thermal analysis must be performed in various phases of 3D IC design. Thermal analysis should be included in the design loop to assess the thermal consequences of design iterations and verify the final design before signoff [1]. From a new methodology characterization point of view, for layouts consisting mainly of test structures, thermal analysis plays an important role in final chip verification [2].

This article presents a practical approach to detailed thermal analysis of stacked-die packages, interconnections between the dies, and the complete electrical design layout. The approach is primarily intended for final layout verification, with aspects of the methodology also applicable in the high-level design flow (see Figure 1). Section 2 explains the general approach. Section 3 demonstrates the approach on a test case whose structure consists of two stacked dies in a ball grid array (BGA) package.

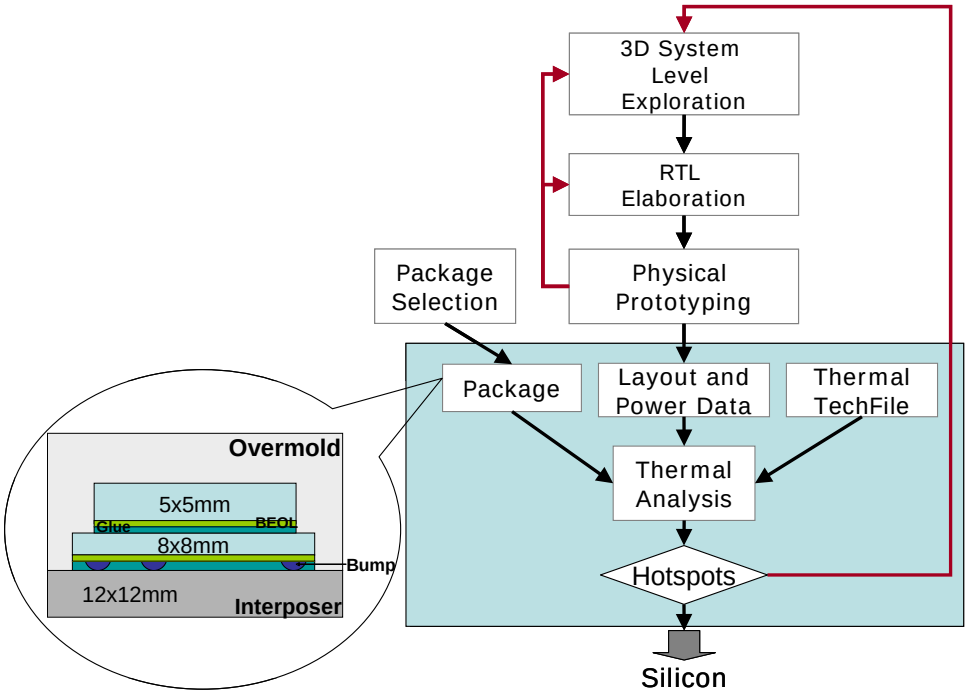

Figure 1: Positioning of our thermal analysis approach (shaded area) in the high-level design flow.

II. THERMAL SIMULATION METHODOLOGY

Our methodology for detailed thermal analysis of full chip design consists of several steps (see Figure 2).

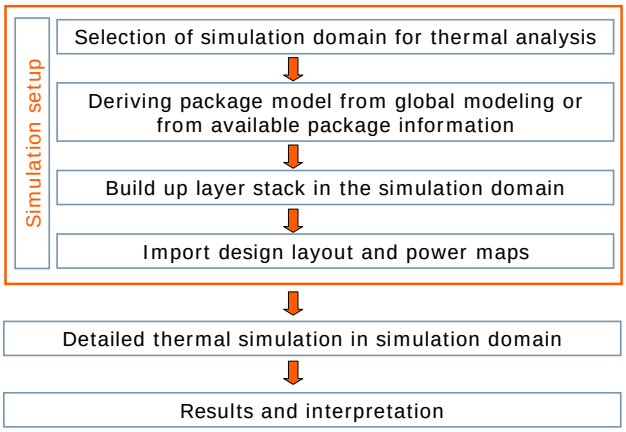

Figure 2: Flow for detailed thermal modeling of a stacked-die structure.

1) In the first step, the region of interest for thermal analysis is selected. There is a significant difference between the submicron length scales of heat sources (and heat transport paths) within the die, and the cm length scales of the package and board objects. Accurate computation of the temperature within the 3D die-stack requires thermal-modeling of the submicron layout features. Therefore, the system is partitioned as follows. The die stack including interface layers, which is the region of interest, is modeled in detail and numerically solved. The thermal effects of the package and board are represented as boundary conditions of the die stack, using what is termed a *package model*.
2) The second step is to represent the package (overmold, interposer, etc.), solder balls, PCB and ambient environment as boundary conditions for the detailed simulation. This may be done using thermal package properties from a data sheet or by extracting the information from a system-(board-) level simulation to estimate the heat flow at each boundary surface of the die-stack. In this case, steady-state or transient boundary conditions are derived from a system-level simulation, and are represented as thermal RC networks in a package model. For the finite element analysis the software tool Msc.Marc is used. From this thermal model the heat flow through each of the faces of the simulation domain can be obtained and converted to boundary conditions in the form of RC thermal networks, to be used in the detailed model.
3) The third step is to construct a *thermal technology-file* describing the thicknesses and thermal properties of all materials in the die stack and interface layers. The temperature dependence of these material properties is also expressed. This enables the construction of a 3D simulation model from the design's layout database.
4) The fourth step is to define the layout geometries and power distribution in the die-stack. Figure 3 shows how the design data for the individual dies are used to prepare the 3D stacked die data for thermal analysis. The 3D die stack is represented in Cadence Virtuoso, and then in GDSII, as a series of layout layers, with unique names for the layers on the top and bottom dies. Layout geometries are also used to define where interface materials such as overmold are present. Scripts were written to prepare geometries defining the extents of power sources in 3D, and defining the power dissipated within each power source. Named monitors, or regions within which the temperature is reported, are also defined.

5) Given the material descriptions, layout database, and package model described above, the fifth step is to model and compute temperature within the simulation domain using the thermal simulation tool FireBolt. FireBolt [3] solves the heat diffusion equation, which in steady state is $\nabla \cdot [k(\mathbf{r},T)\nabla T(\mathbf{r})] + P_v(\mathbf{r}) = 0$ where $\mathbf{r} \equiv (x, y, z)$ in (m), T is the temperature (K), k is the thermal conductivity (W/(mK)), and P_V is the power density (W/m^3). In this case, P_V is invariant with temperature. Boundary conditions specifying temperature or heat flux are expressed at the surfaces which define the interface between the 3D die stack and its package (or surroundings). In this case, the 3D IC is modeled as a cuboid with six faces, on which boundary conditions are specified. In FireBolt, the 3D IC chip is modeled at the length scales of its layout geometries, as needed to meet specified spatial and thermal error tolerances.

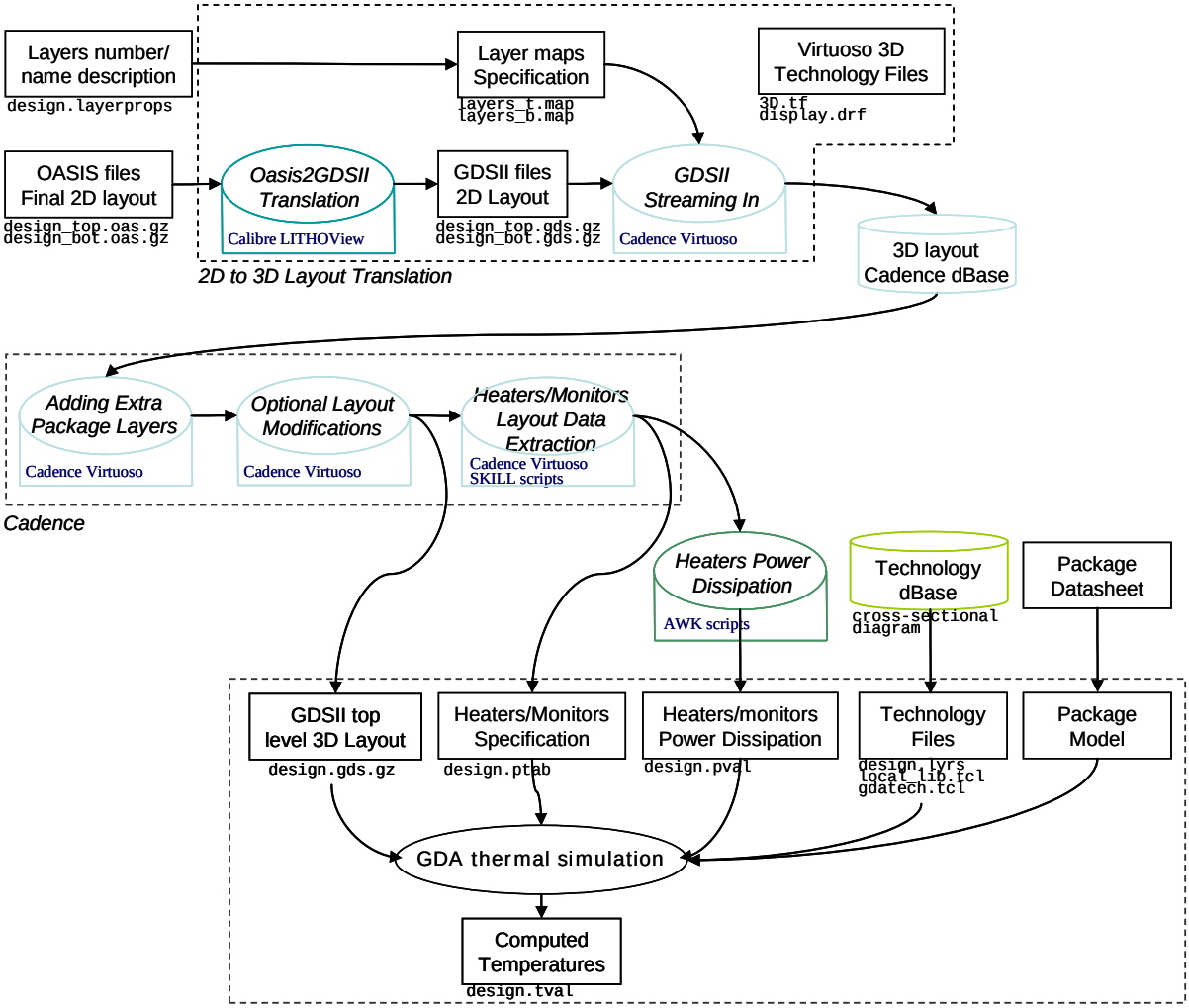

Figure 3: Flow for preparation of layout, power, thermal properties, and package for thermal simulation of the 3D die stack.

III. THERMAL SIMULATION RESULTS

The test case consists of a two-die, face-to-back (F2B) stacked structure in a BGA package. The BGA package is soldered to a PCB, and the whole structure is considered to be in an ambient environment of still air at 300K. The top die is 25 µm thick and 5x5 mm^2 in size. The active region of the top die is connected to the bottom die by means of Cu through-Si vias (TSVs) through the top die. These vias have a diameter of 5µm. Several pitches of the TSVs are considered to study the effect of the TSV on the thermal behavior or the stack. The bottom die is an 8x8 mm^2 die with a thickness of 250µm. Figure 4 gives a schematic overview (not to scale) of the material layers and their respective thickness in the die stack, Figure 5 shows the 3D design for this stack of a smaller die on top of a larger bottom die. In the figure the location of six heat sources in indicated, with a total of 2100 power source elements. Heat sources are implemented as (resistive) meanders in the *metal2* layer of the top die (see Figure 6). The figure also illustrates positions of five monitoring diodes for characterization of hot spots. Located on both the top and bottom die, they are used for study of vertical heat conduction in the stack.

Finally, Figure 7 shows the temperature distribution in the *metal2* layer of the top die. This is the layer where the power is dissipated. A sharp temperature peak can be observed at the location of the hot spots. The thermal modeling results are experimentally validated with temperature data from integrated diodes as depicted in Figure 8.

As can be noted, the experimental results are obtained on a simplified version of the packaged die stack. A thinned top die is bounded to a full thickness landing wafer and such a structure is mounted on a chuck and kept in place by vacuum. The temperature of chuck is controlled to provide isothermal boundary to the bottom of the stack. Probes were used to connect heaters and monitoring diodes. The aim of such an experimental setup is to evaluate thermal modeling early in the development of the 3D integration including TSV, without the necessity of having the stack packaged. Future work will involve application of our approach to fully packaged die stack, with die test structures designed to improve inter-tier thermal characterization.

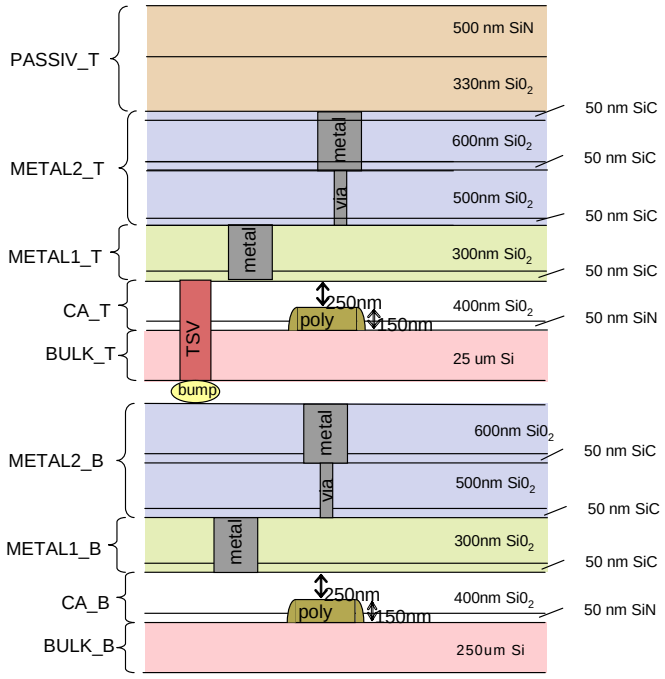

Figure 4: Cross section of the die stack, with the BEOL structure of the top (_T) and bottom (_B) die.

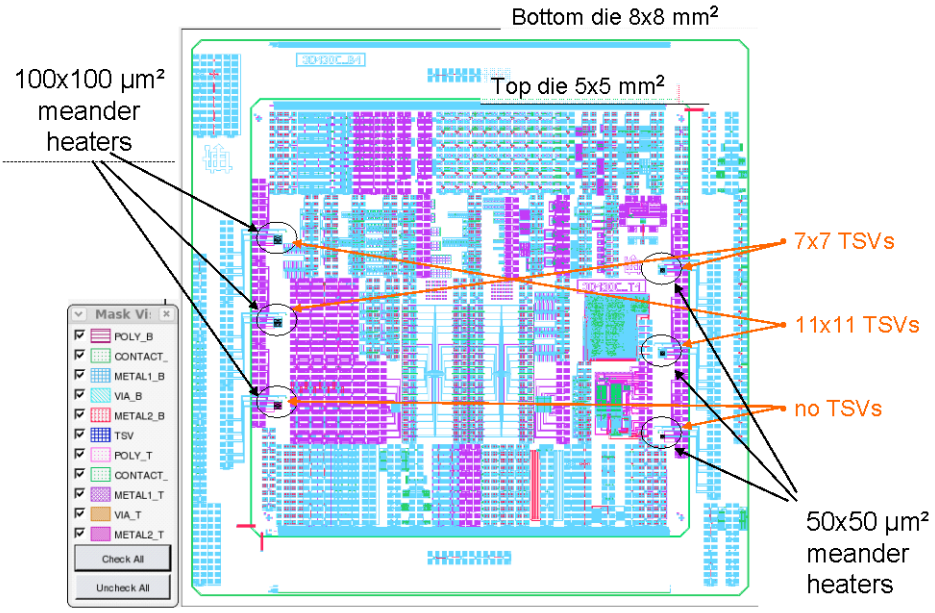

Figure 5: Combined view of the layout of the top die on top of the bottom die including the heating structures and the TSVs through the top die.

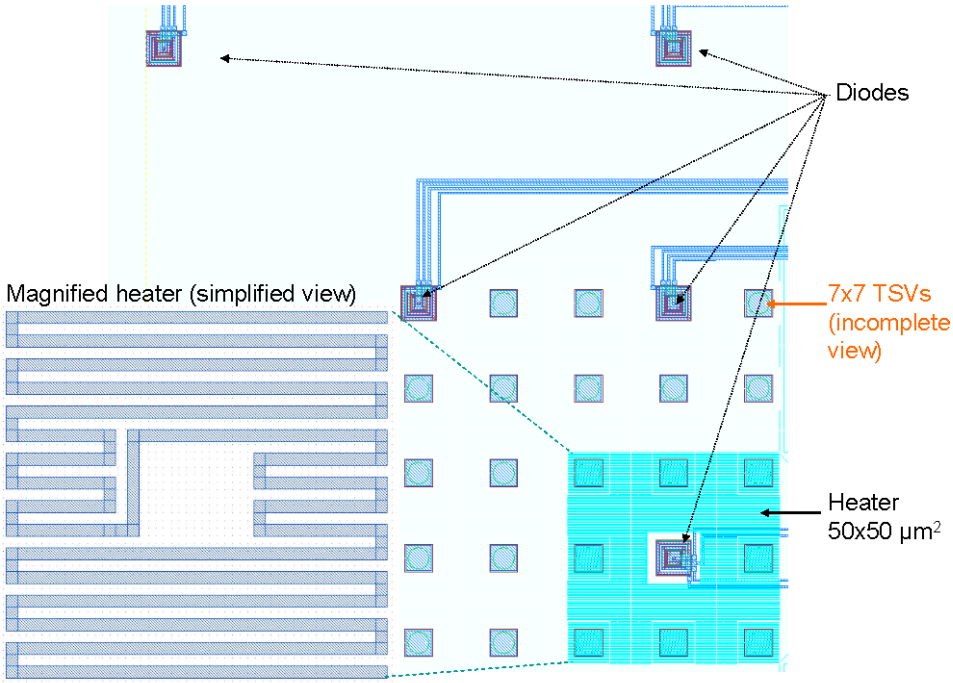

Figure 6: Detail of the heater/monitors structure showing the position of monitoring diodes, TSV array, heater and magnified meander heater structure (simplified view).

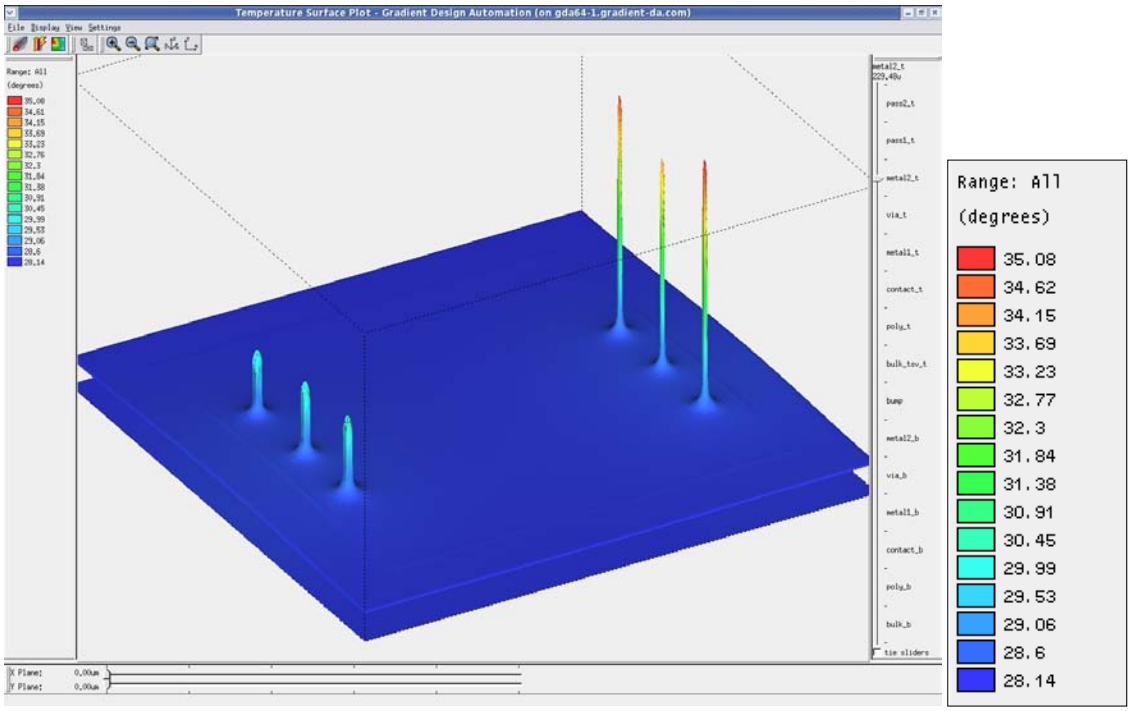

Figure 7: Surface plot of the temperature distribution (°C) in the metal2 layer of the top die for a power of 10mW dissipated in the heat sources with an array of 100x100 µm^2 heaters on the left side and 50x50 µm^2 heaters on the right side.

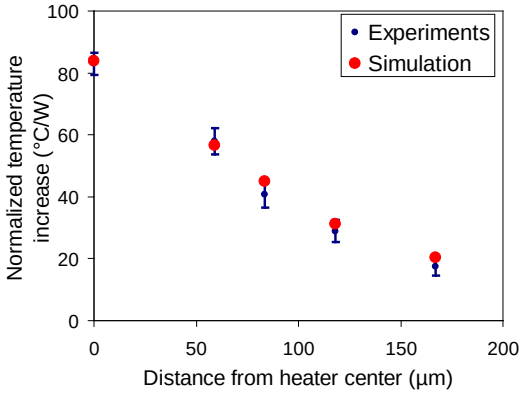

Figure 8: Comparison of the simulation results (red dots) with the experimental temperature measurements (blue dots and error bars) for a 100x100 µm^2 meander heater.

IV.CONCLUSION

A methodology has been presented to perform a detailed thermal analysis of stacked-die packages including the complete back end of line (BEOL) structure, interconnections between the dies, and the complete electrical design layout of all the stacked dies.

The methodology has been demonstrated on a two stacked-die structure in a BGA package. A 3D field solver computes the detailed temperature profiles, given the power profiles and detailed layout of all the dies in the stack. The effect on temperature of varied power-source dimensions (i.e., power density) and TSV density is shown.

REFERENCES

[[1] S. Melamed, T. Thorolfsson, A. Srinivasan, E. Cheng, P. Franzon and R. Davis. Junction-level Thermal Extraction and Simulation of 3DICs. *IEEE International 3D Systems Integration Conference*, Sep. 2009.

[2] H. Oprins, M. Cupak, G. Van der Plas, B. Vandevelde, P. Marchal, A. Srinivasan and E. Cheng. Fine grain thermal modeling of 3D stacked structures. *15th International Workshop on Thermal investigations of ICs and Systems (THERMINIC* , pages 45-49, Oct. 2009, Leuven, Belgium.

[3] FireBolt (Nanoscale Full-Chip Thermal Simulator), Gradient Design Automation, Inc, http://www.gradient-da.com/.