

# Display Technologies for Intel<sup>®</sup> Graphics

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Intel Corporation

**GVCS001**

# Agenda

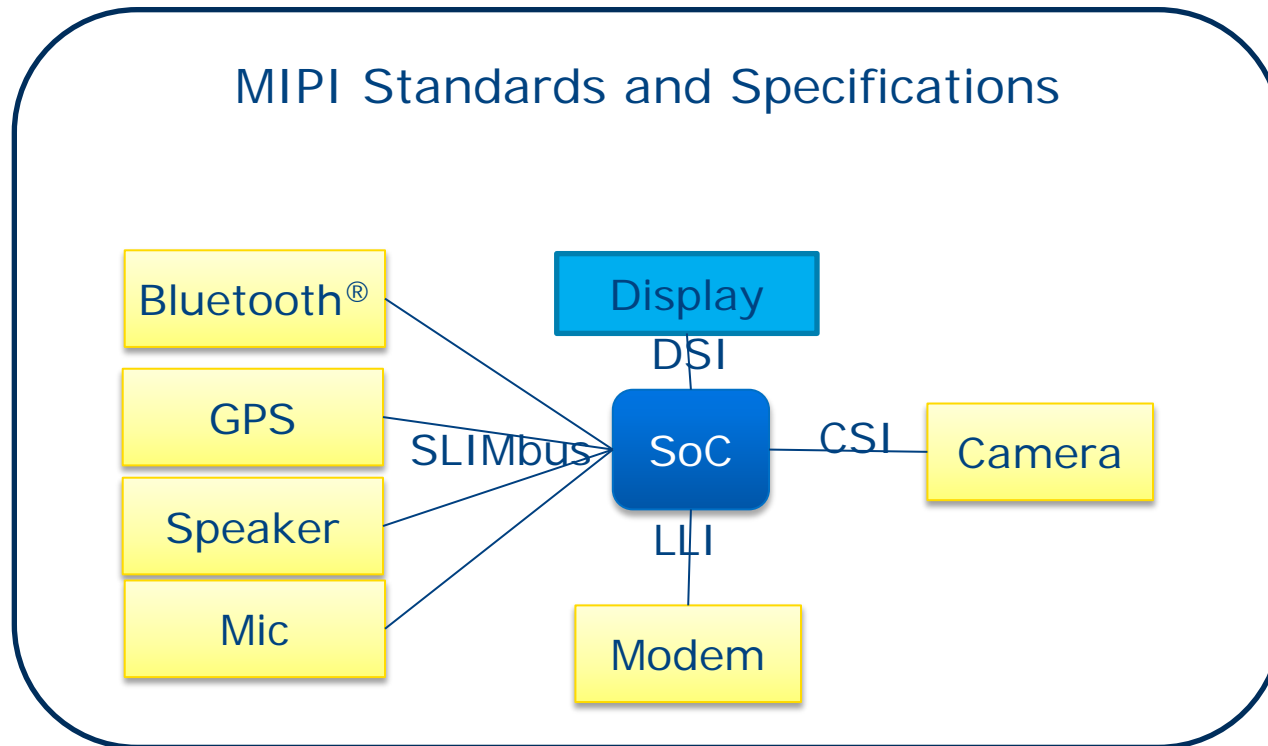


- Mobile Industry Processor Interface (MIPI\*) Based Displays
  - Overview
  - Enabling considerations
  - Scalable model for fast time to market
- Display Power Savings
  - Display power consumption
  - Display power savings features
- Miracast\* Wireless Display Demo

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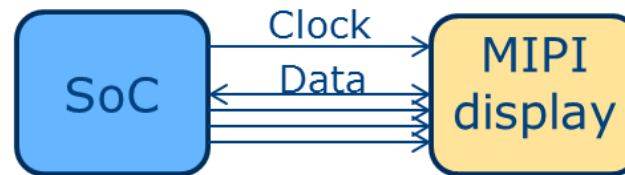
- MIPI\* – DSI Based Displays
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# MIPI \* Display Overview



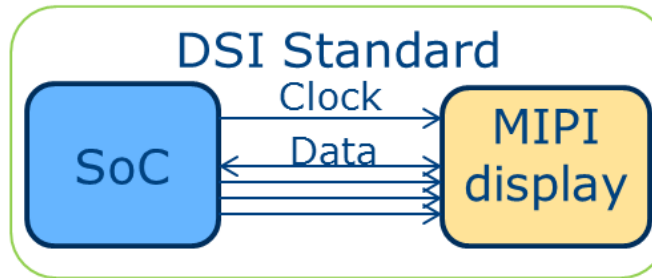
# MIPI\* Display Overview - DSI

DSI Clock and Data



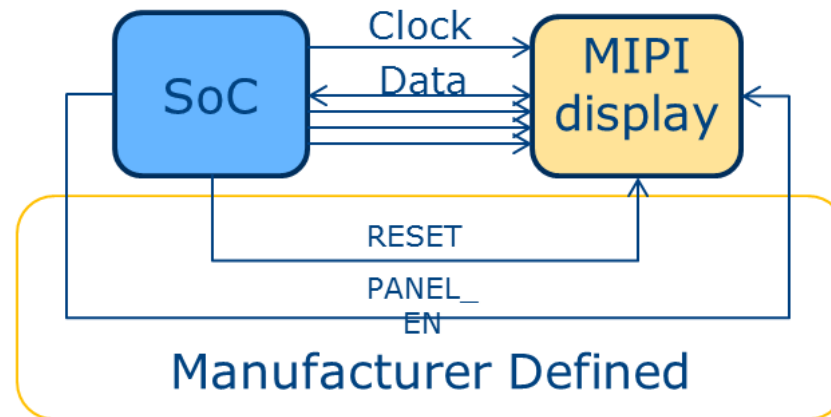
# MIPI\* Display Overview - DSI

## DSI Clock and Data



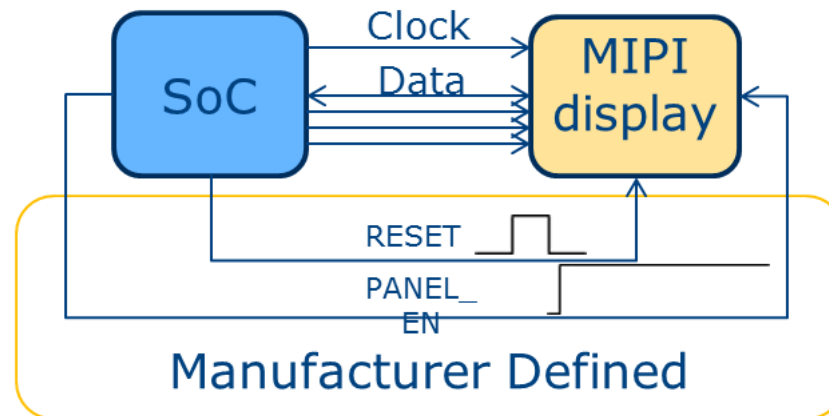
# MIPI\* Display Overview - DSI

## Manufacturer Defined Pins



# MIPI\* Display Overview - DSI

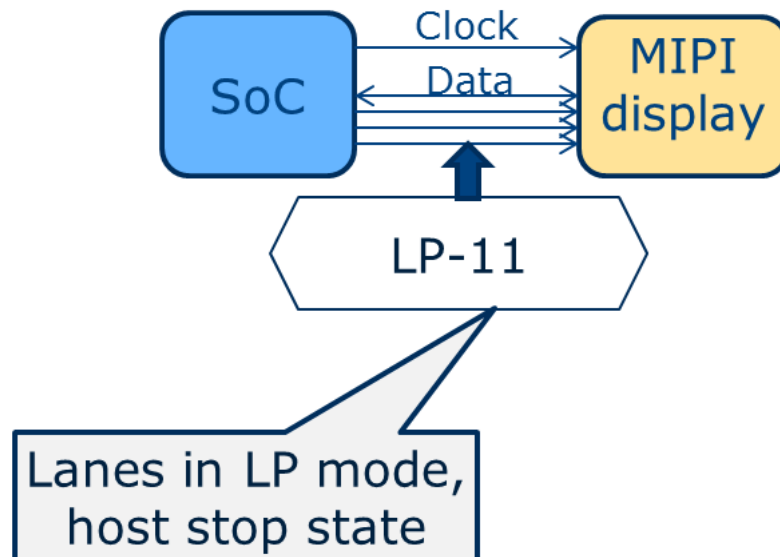
## Panel Power-up Sequence





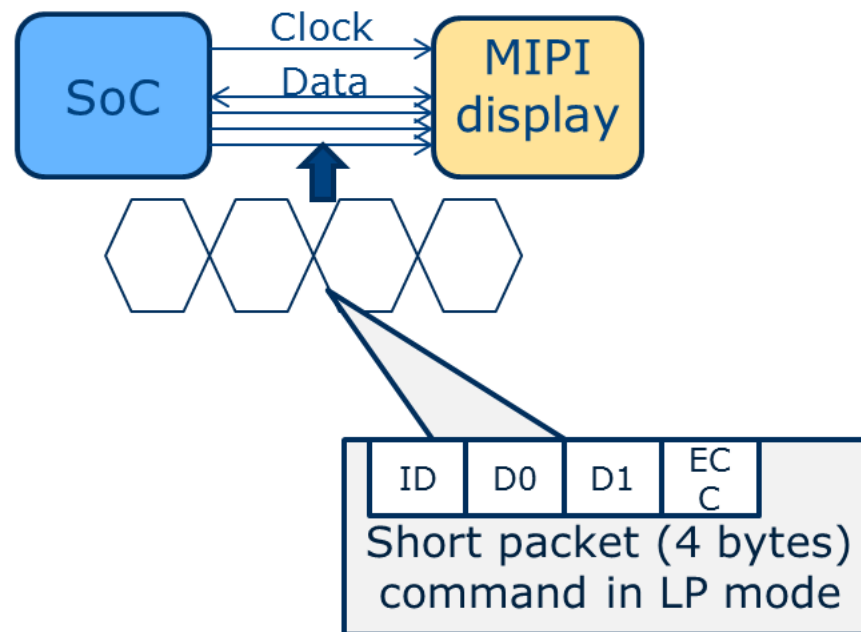
# MIPI\* Display Overview - DSI

## Lane State On Power-up



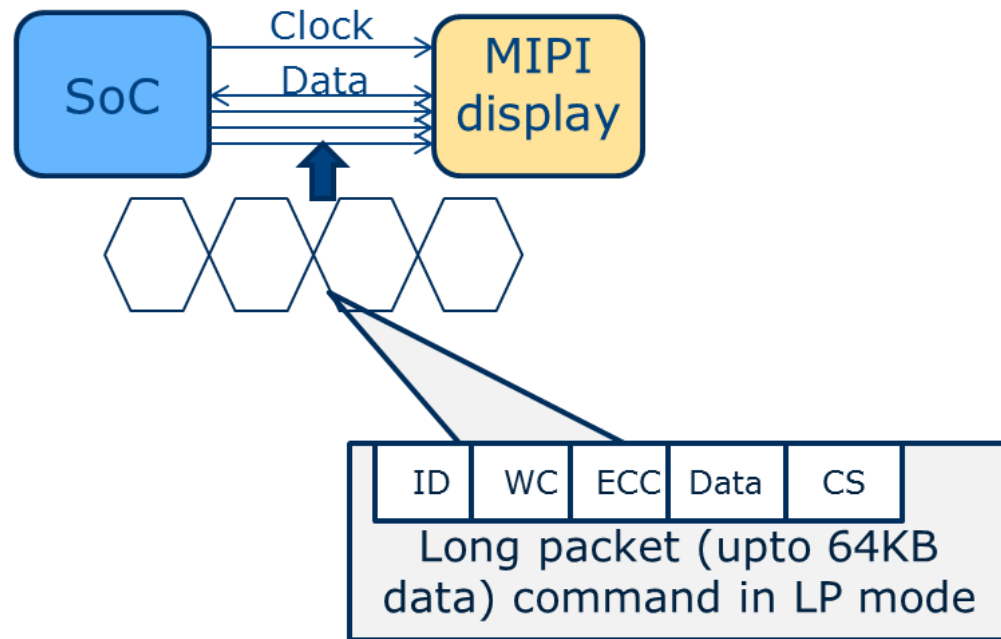
# MIPI\* Display Overview - DSI

## Manufacturer Defined Panel Start-up Commands



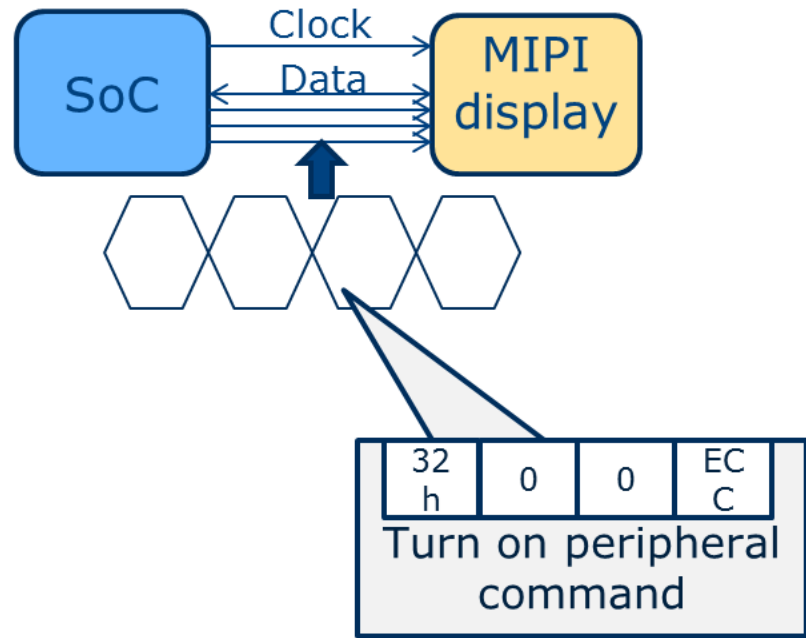
# MIPI\* Display Overview - DSI

## Manufacturer Defined Panel Start-up Commands



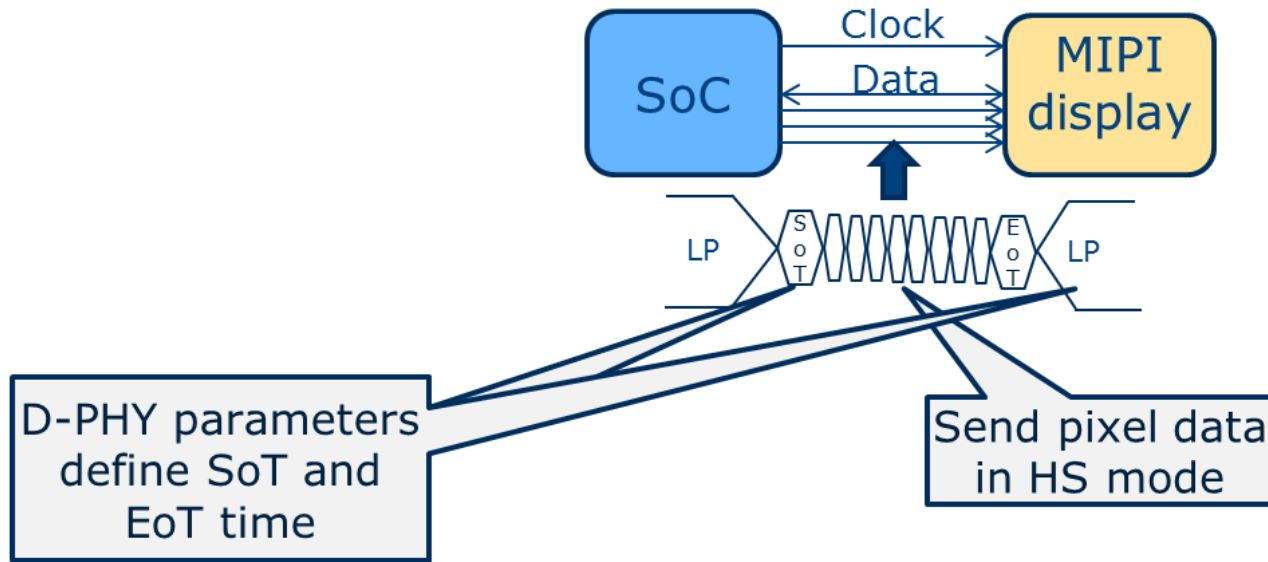
# MIPI\* Display Overview - DSI

Video Mode: Send Turn On Command



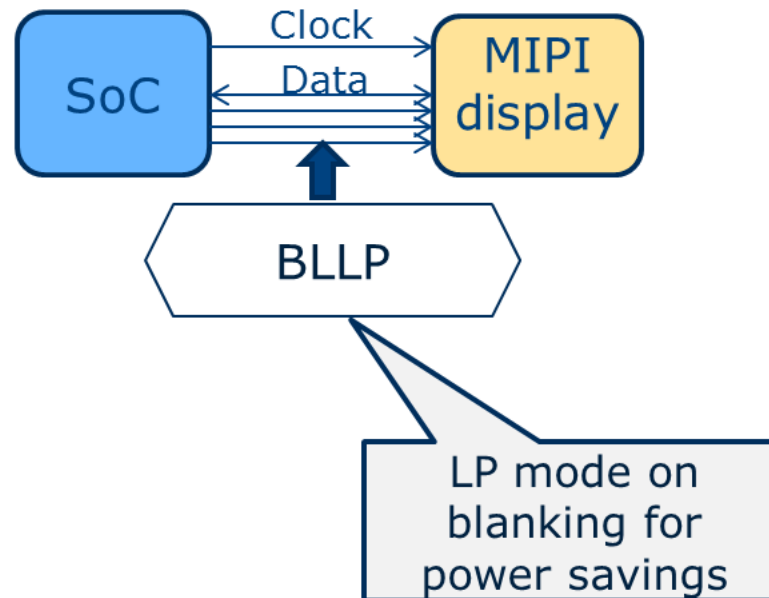
# MIPI\* Display Overview - DSI

Video Mode: Pixel Data Transmission



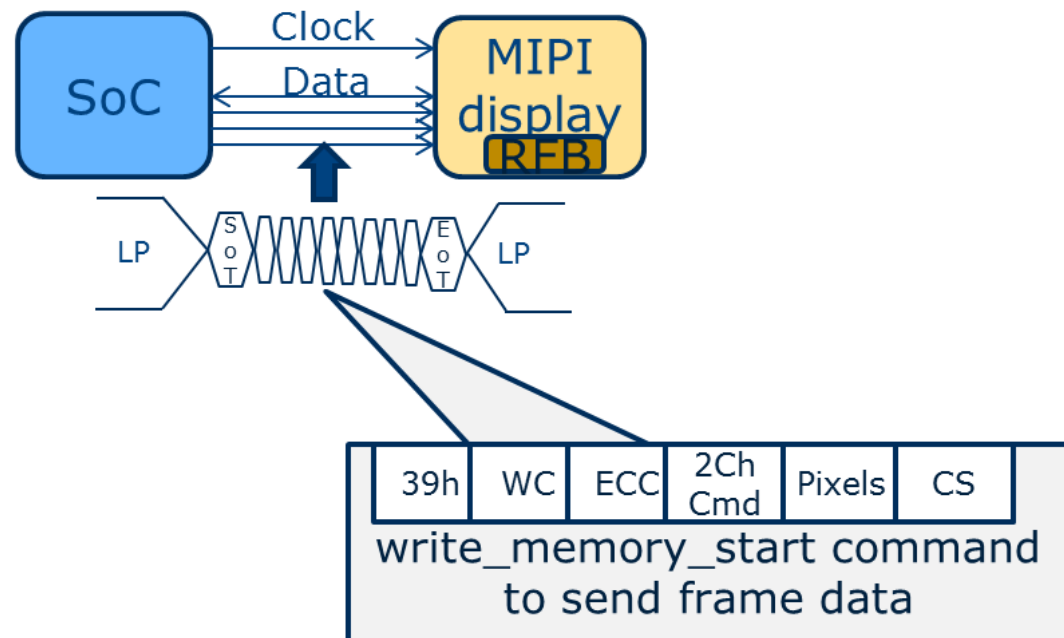
# MIPI\* Display Overview - DSI

Video Mode: Blanking



# MIPI\* Display Overview - DSI

Command Mode: Update Panel Frame Buffer



# MIPI \* Display Support on Intel Platforms



**Intel Atom processor  
Z2760  
MIPI DSI 1.01  
4 lanes  
1366x768**

**MIPI to LVDS  
bridge +  
11" LVDS  
Panels**

**11" Native  
MIPI**

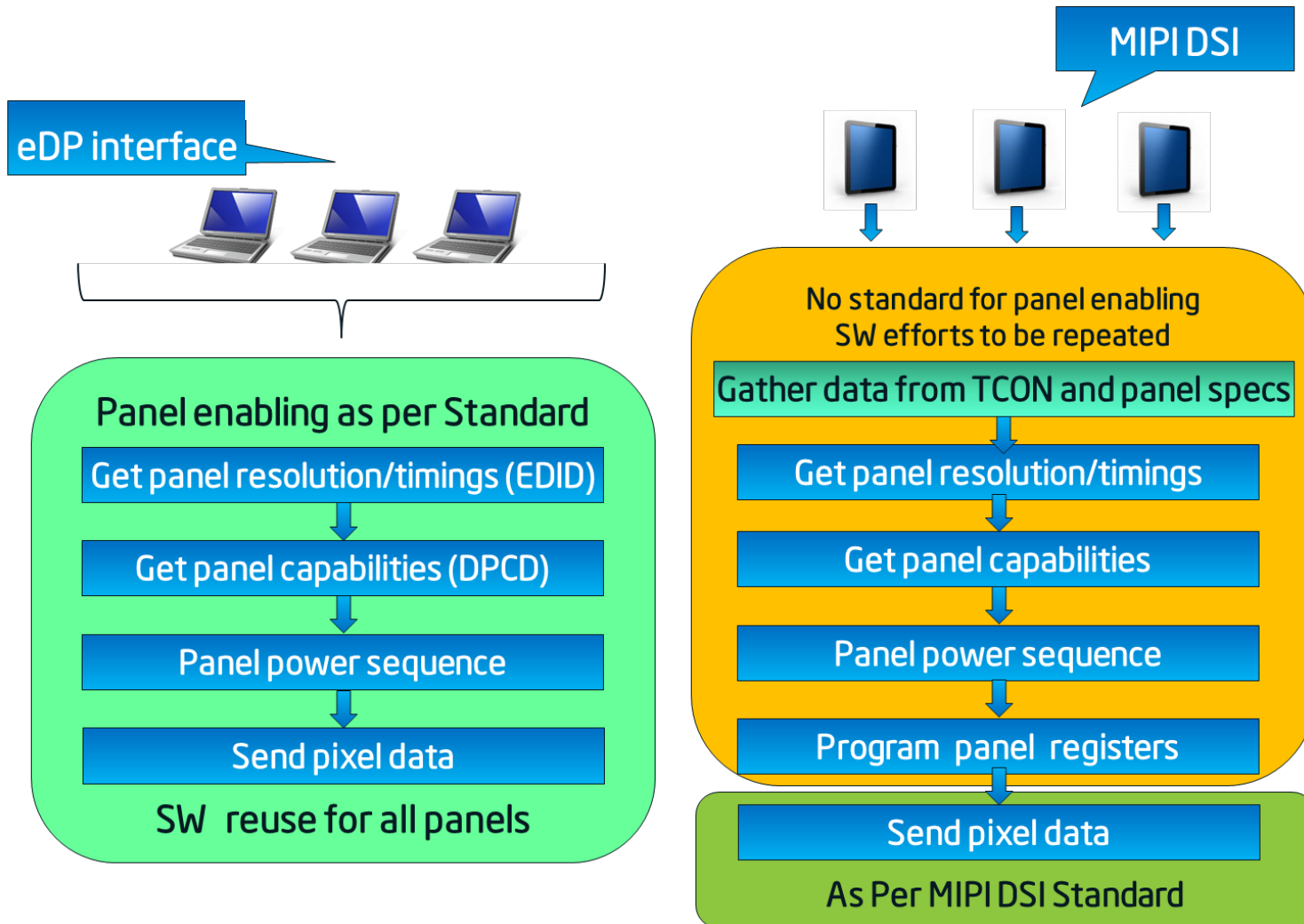
**Intel® Atom™ processor  
based Bay Trail platform**

**MIPI DSI 1.01  
2x4 lanes (Dual-link)  
Single-link -1920x1200  
Dual-link – 2560x1600**

**~ 10" native MIPI**



# MIPI\* vs. eDP\* Panel Enabling



# MIPI\* -DSI Panel Interface considerations

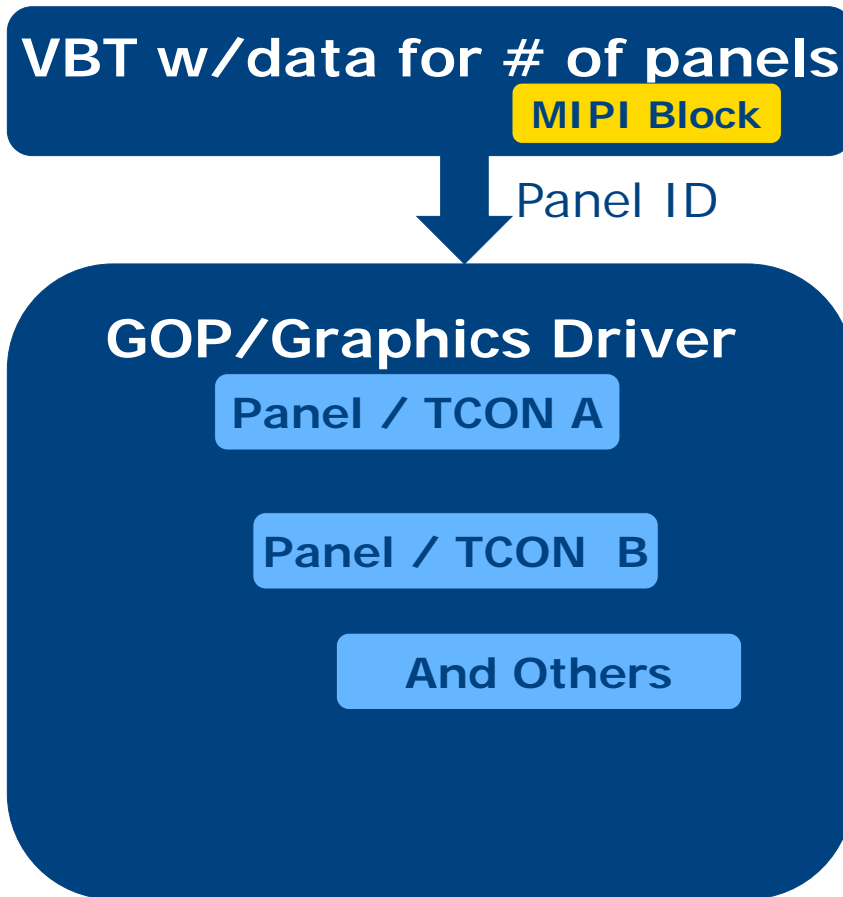
- Panel Variations: Command Mode / Video Mode: W & w/o burst mode; sync events or sync pulses; preferred operating mode
- EDID support is not uniform or consistent
- Panel resolution and timing parameters
- Number of DSI lanes needed / used
- Pixel formats supported by the panel / recommended format
- Recommended data rate/Data frequency
- Panel power up sequence, signals and delays
- LP to HS and HS to LP switching time requirements
- Recommended values for DPHY parameters THS-PREPARE, THS-TRAIL, TCLK-TRAIL, THS-ZERO, EOT packet
- Register programming (EPROM based or by host) during power up/down; programming sequence; default values
- Panel backlight control (external PWM?)
- CABC support and register programming sequence
- Other value-add features supported on the panel; its enabling

**Too many Configuration Items!**

# MIPI \* Panel Enabling Implications

Panel Implementations	Hardware/Software Impact
No EDID	Software: EDID should be configured in VBT
Variance in panel capability (lane count, command/video mode, etc.)	Software: The panel parameters must be configured and read from VBT
Panel power sequence (pin controls and delays)	Software: Driver code addition for panel power sequence
No internal EPROM for panel register initialization	Software: Driver code addition of command sequence for panel register initialization
Non-standard pin assignment, cable, connector	Hardware: Add-on card and cable design according variance in panel pins for Reference Hardware platform

# Current Driver Model for MIPI\*



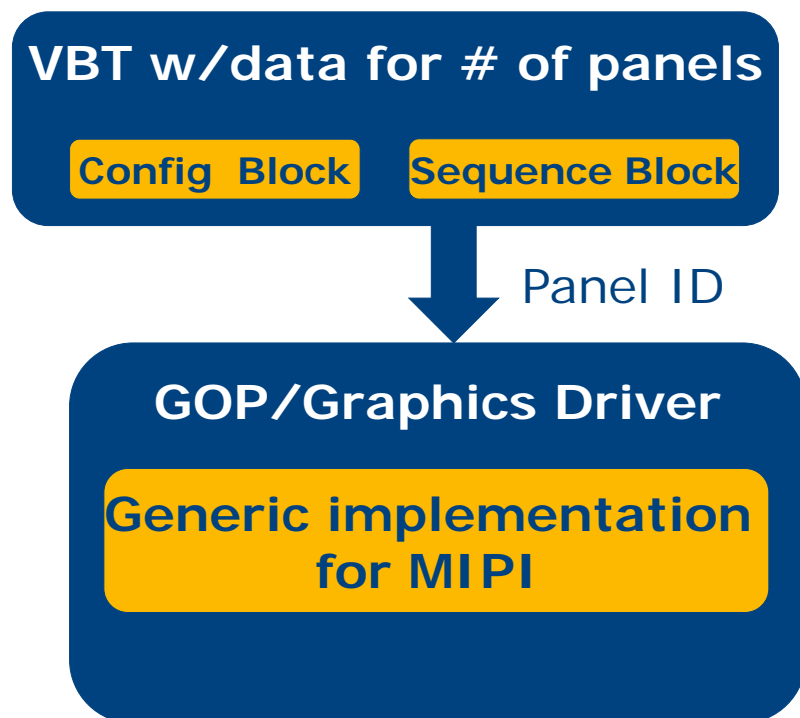
MIPI block in firmware with basic config data used in existing platforms



MIPI\* panel enabling sequence hard coded in driver for each panel

# Towards a Generic Model

- Goals:
  - No driver code changes
  - Support in both GOP and driver
  - Extends to all types of MIPI\* panels/TCON:
  - Scalable for future features / specs / platforms



■ Changes in new implementation

# BMP<sup>1</sup> Settings for Configuration Block

The screenshot displays the configuration interface for the MIPI Display Settings. On the left, a tree view shows the navigation path: Windows Graphics > Display Configuration > LFP 1 > Display Configuration > LFP Panel configuration > Panel #1 > MIPI Display Settings. The main area is titled "MIPI Display Settings" and contains two sections of configuration parameters.

**MIPI DSI Controller Configuration Settings**

Panel Identifier:	MIPI DSI Panel-1
Packet Sequence For Video Mode:	Non-burst with sync events
Colour Format In Video Mode:	RGB888
Dual Link Support:	Dual Link Not Supported
Number Of Data Lanes:	4
Escape Clock:	20 MHz
EoT Packet Transmission:	Enable
HS Transmission Time Out Counter:	0x003FFFFFF
LP Transmission Time Out Counter:	0x0000FFFF
Bus Turn Around Time Out Counter:	0x00000014
Device Reset Time Out Counter:	0x000000FF
DSI Host Controller Initialization Time Out Counter:	0x000007D0
TClkPrepare:	50
TClkTrail:	70
TClkPrepareTClkZero:	310
THsPrepare:	50
THsTrail:	60
THsPrepareTHsZero:	200

**MIPI DSI Panel Power On/Off Sequence(delays)**

PowerUpDelay:	10000
DataTurnOnToPanelBacklightEnableDelay:	200000
BacklightOffToDataTurnOffDelay:	200000
PowerDownDelay:	10000
PowerCycleDelay:	500000

# MIPI\* Sequences Programming

- MIPI\* Sequences
  - Reset assert/de-assert sequence
  - Programming panel OTP by sending DCS commands
  - Display ON/OFF sequence
  - Backlight ON/OFF sequence
- Sequence Operations
  - Delay
  - Send MIPI packets
  - GPIO programming
  - MMIO programming

The screenshot shows the MIPISeqTool application window. The title bar reads "MIPISeqTool". The main interface is titled "Options" and contains several controls:

- Selection Block:** A dropdown menu for "Choose Action" is set to "Add New Sequence".
- Input File (.bin or .xml):** A text field with a browse button (folder icon).
- Choose Sequence:** A dropdown menu set to "MIPI SEQUENCE RESET".
- Element:** A dropdown menu set to "SEND PACKET".
- Byte (hex):** Four input boxes, each containing the value "0".
- Payload:** A large empty text area.
- Data Type, Flags, Word Count:** A section with a light gray background, currently empty.
- Buttons:** "Save Element", "Save Sequence", and "Save Sequence To File" are located at the bottom right.

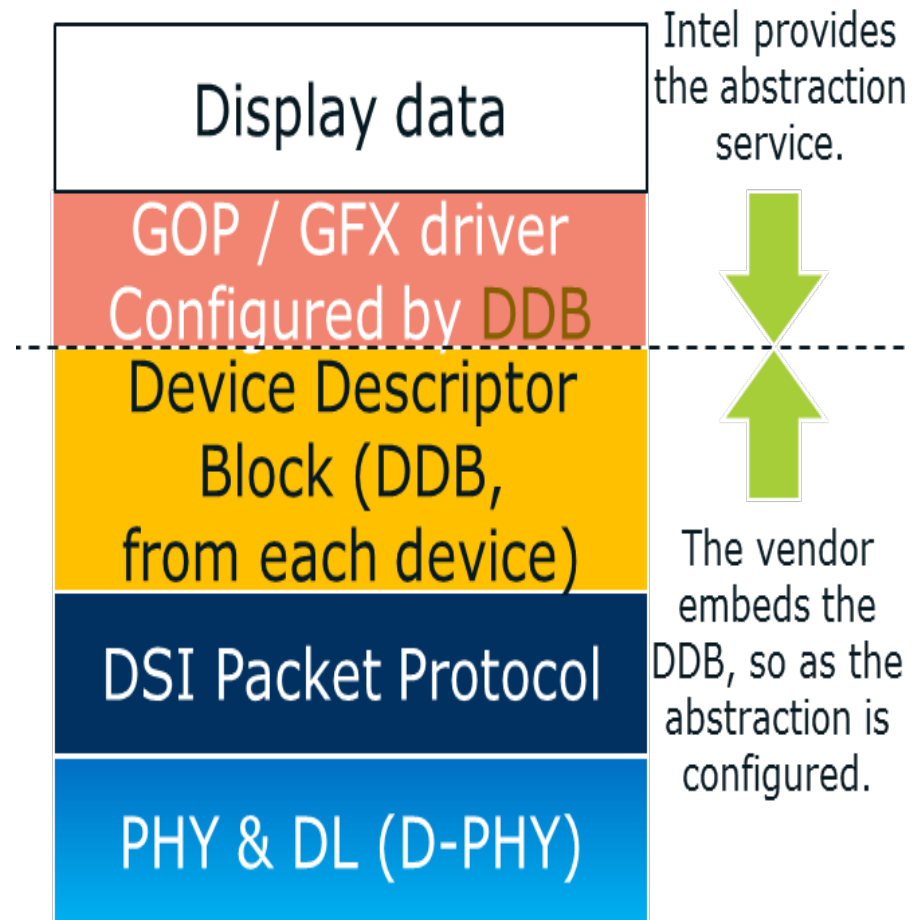
# Generic MIPI\* Design Advantages

Existing model for MIPI* in driver	Generic MIPI support in driver
Updates and rebuild GOP/Gfx driver per panel	No panel specific GOP/Gfx driver changes
Panels, AIC needed w/driver developers	Easy panel enabling w/ just VBT modification (more virtual developers, i.e., AE, OEM)
Requires more panel enabling time	Saves panel enabling effort
Driver update for TCON issues (post-launch issues will need driver updates)	No driver updates fixing TCON specific issues (post-launch issues will need driver updates)
Not scalable for newer features/ Panels/ platforms	Easily scalable for supporting newer features/ panels/ platforms
Supports both Android* & Windows*	Supports both Android & Windows



# Towards Further Standardization

- Intel working to define a standard MIPI\* panel descriptor
- Goal is to implement the standard descriptor among panel TCONs
- Driver would read the panel descriptor from the panel and take the enabling actions
- Next steps / Call to action
  - TCON vendor collaboration for common DDB format



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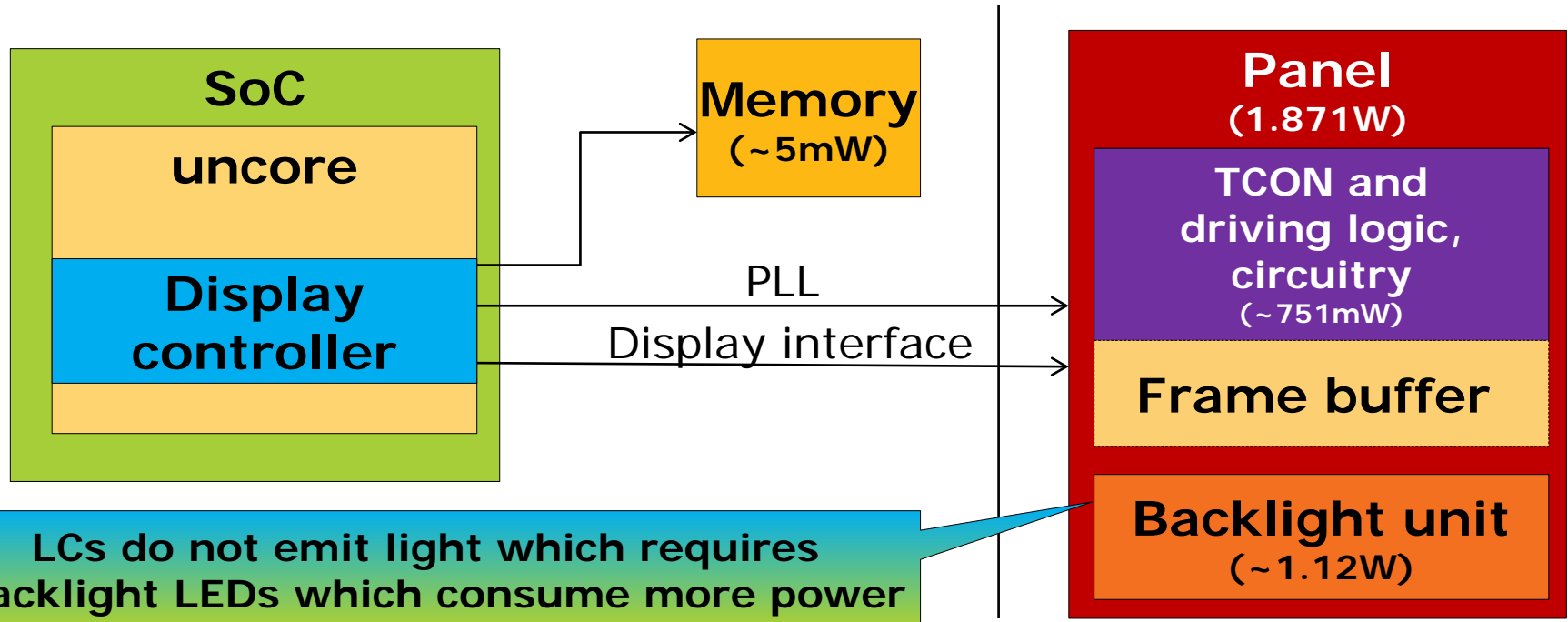
# Display Power Savings

## Agenda

- Display power consumption
- Display power saving features
  - Backlight control
  - Intel® Display Power Saving Technology (Intel® DPST)
  - Content Adaptive Backlight Control (CABC)
  - DPST vs. CABC backlight power comparison
  - Windows\* 8 adaptive brightness control
  - MIPI\* display self refresh
  - Embedded DisplayPort\* (eDP) panel self refresh
  - Other power saving options
  - Co-existence of display power savings features

# Display Power Consumption

Display sub-components that consume power



LCs do not emit light which requires backlight LEDs which consume more power

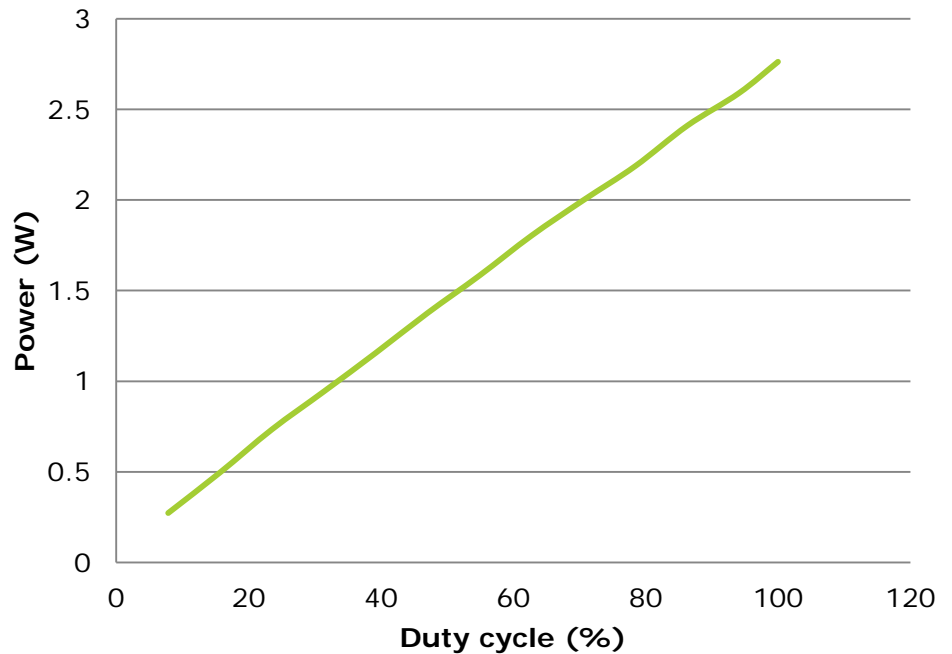
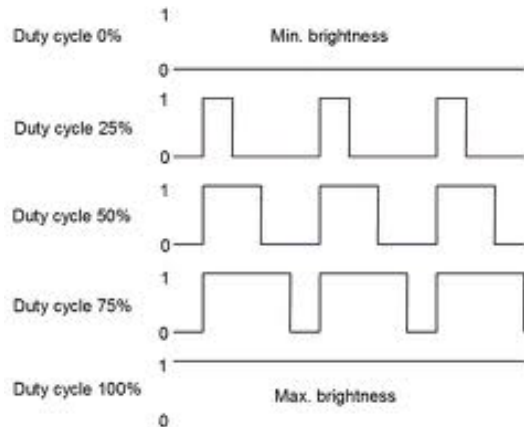
- On a sub 3W tablet platform, display consumes about 50-70% of power
- Backlight power – about 60-75% of panel power

- Intel® Atom™ Processor Z2760 platform power data
- MIPI\* to LVDS + 11.6" panel
- Web browsing scenario power

# Display Power Saving Features

# Backlight Control

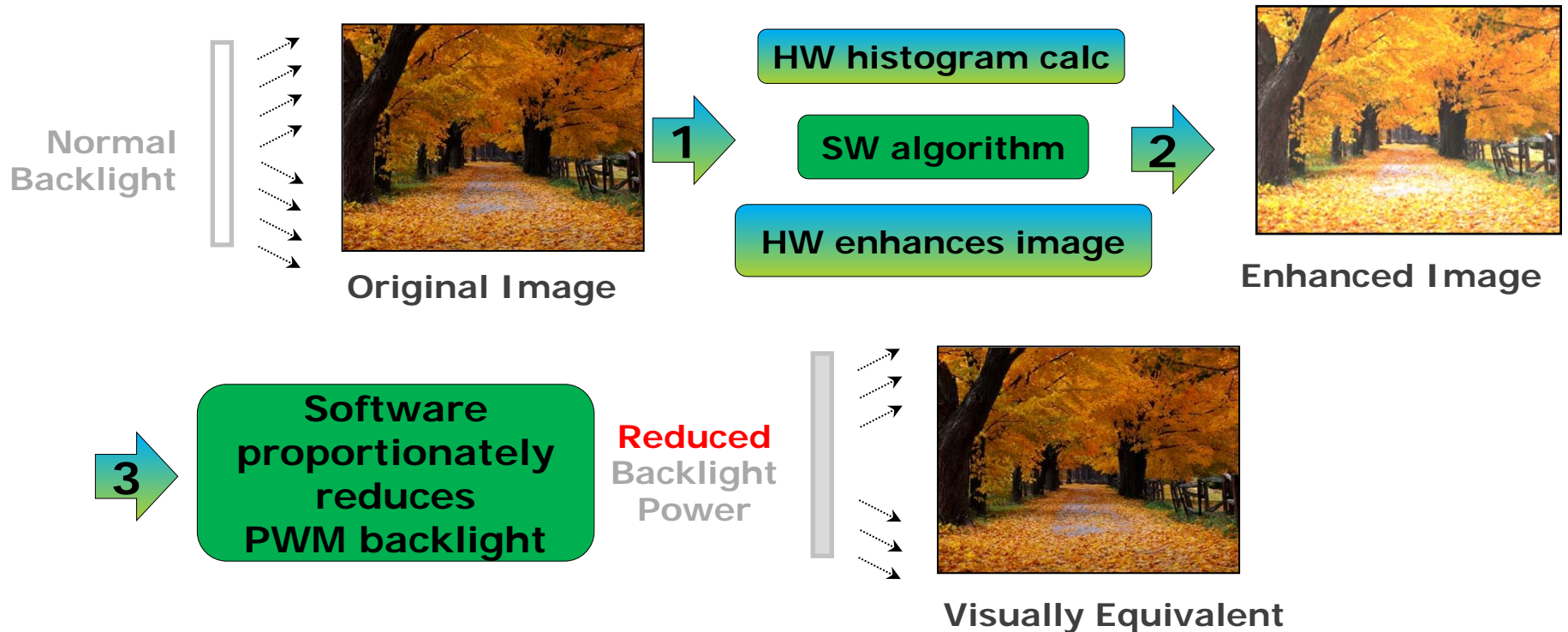
- PWM signals control backlight intensity and power
- OS reduces backlight on
  - User inactivity
  - Ambient light change
- User backlight adjustment



***Controlling backlight intensity linearly impacts power***

# Intel® Display Power Saving Technology (Intel® DPST)

- A power savings technology that reduces backlight power
- Increases pixel luminance and reduces backlight with minimum visual impact



*For DVD workloads, Intel DPST 6.0 reduces backlight power by about 70%*

# Content Adaptive Backlight Control (CABC)

- Similar concept as Intel® Display Power Saving Technology (Intel® DPST), reduces backlight power
- Implementation is on the panel and proprietary to vendor
- Supported on MIPI\* panels/bridges
- Controlled through MCS packets on MIPI
- Intel DPST and CABC cannot be enabled together

*CABC on Intel® Atom™ Z2760 processor reduces backlight power by about 33% on video playback scenarios*

*In general for command mode MIPI panels CABC is preferred*



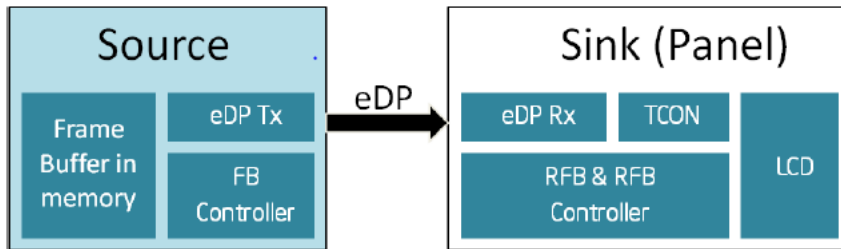
# Windows\* 8 Adaptive Brightness Control

- OS policy for backlight control algorithms
- Requires a balance between power and user experience
- OS controls DPST/CABC
- OS enables CABC based on scenario
- Enabled in battery power and disabled on AC power
- Lower aggressiveness with desktop, browsing, photos, static content
- Higher aggressiveness with dynamic content like video

# MIPI\* Display Self Refresh

- Supported on MIPI\* command mode panels
- Pixels are sent to panel only on demand
- Display engine is active only when pixels are fetched
- DSI PLL can be power gated when OS detects idleness
- Display memory bandwidth is not consumed when display is idle

# Embedded DisplayPort\* (eDP) Panel Self Refresh (PSR)



- Similar to MIPI\* DSR, utilizes panel frame buffer
- Supported on eDP 1.3 with PSR panels
- Hardware detects idle display and enters PSR active
- Display engine clock gated on PSR active
- Software needs to exit PSR on user activity

*PSR and DSR save power on display engine,  
memory panel power on I/O,  
but panel frame buffer will consume power  
SoC+memory+panel savings could save ~17%*

# Other Power Saving Options

- Max FIFO
  - Combine display FIFO in single display
  - Reduces internal clock activity and memory I/O
  - Saves power on display engine and memory I/O
- Dynamic Voltage Frequency Scaling
  - Set Core Display clock according to the max resolution
  - Display vnn scales according to CD clock
  - Saves power on display engine

# Coexistence of Display Power Savings Features

	eDP PSR	MIPI DSR	DPST	CABC	DVFS	Max FIFO	Backlight control
eDP PSR		NA	Yes	NA	Yes	Yes	Yes
MIPI * DSR			Yes	Yes	Yes	Yes	Yes
DPST				NA	Yes	Yes	Yes
CABC					Yes	Yes	Yes
DVFS						Yes	Yes
Max FIFO							Yes
Backlight control							

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# Miracast\* Wireless Display Demo



# Summary

- MIPI\*-DSI Displays
  - Intel scalable model is imperative for time to market
  - Need OxM, Panel, TCON support for success
  - Further standardization opportunities need industry support
- Display Power Management
  - Several techniques exist to fine tune design for optimal power performance
    - Screen size, resolution; Panel type, capability – will drive right power optimization schemes



# Next Steps

- MIPI\* – DSI Displays
  - Needs Industry Collaboration – Panel, TCON, OxM, IHV to drive efficient design and robust enabling

# Additional Sources of Information

PDF of this presentation is available is available from our Technical Session Catalog:

[www.intel.com/idfsessionsSF](http://www.intel.com/idfsessionsSF). The URL is on top of Session Agenda Pages in Pocket Guide.

Additional info on the web – **[www.mipi.org](http://www.mipi.org)**

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