

# A 30-MHz–2.4-GHz CMOS Receiver With Integrated RF Filter and Dynamic-Range-Scalable Energy Detector for Cognitive Radio Systems

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**Abstract**—A 30-MHz–2.4-GHz complementary metal oxide semiconductor (CMOS) receiver with an integrated tunable RF filter and a dynamic-range-scalable energy detector for both white-space and interference-level sensing in cognitive radio systems is reported. The second-order RF filter has only two stacked transistors, and its use, in combination with a subsequent harmonic rejection mixer, results in wideband interference rejection. The energy detector with programmable rectifiers provides dynamic-range (DR) scalability, enabling shared use for white-space/interference-level detection and automatic gain control. A prototype chip, fabricated using 90-nm CMOS technology, achieved over 42-dB harmonic rejection including 7th-order component without any external device, a 67-dB gain, a 5–8-dB noise figure, a  $-11$ -dBm in-band third-order intercept point, and a  $+38$ -dBm second-order intercept point while drawing only 25–37 mA from a 1.2-V power supply. Multi-resolution DR-scalable spectrum sensing with a 0.2–30-MHz detection bandwidth,  $-83$ -dBm minimum sensitivity, and a 29–48-dB DR was demonstrated.

**Index Terms**—Cognitive radio, energy detector, harmonic rejection mixer, RF filter, RSSI, spectrum sensing, tunable filter, wide-band receiver.

## I. INTRODUCTION

**D**EMAND for efficient operation of radio frequency (RF) devices when the resources available, such as the frequency spectrum and electrical supply, are limited is increasing as a variety of wireless applications rapidly become more pervasive. A promising solution to the problem of a limited frequency spectrum is the use of cognitive radio (CR) devices, which sense the radio environment, identify the vacant bands, change their operating parameters accordingly, and make use of these available bands in an opportunistic manner. Their use also helps solve the problem of a limited electrical supply because they improve transmission efficiency by using unoccupied spectrum with favorable propagation properties and reduce retransmission necessitated by data collisions and signal interference.

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An intensely investigated potential application area of CR devices is broadband cellular systems. Cellular networks have recently transitioned from simply providing mobile telephony with limited data services to supporting universal mobile broadband services with extensive data services. Such services require a large data transmission capacity that cannot be supported by the spectrum resources typically allocated to cellular systems. There are, however, many unused spectrum resources at particular times and specific geographic locations, and regulatory agencies, service providers, vendors, and academia have been discussing a new paradigm for spectrum allocation that would enable more dynamic and flexible use of those resources [1]. One approach, based on CR technology, would enable a cellular system to use spectrum resources already allocated to another system as long as doing so would not interfere with the primary system.

Another potential area for CR application is wireless sensor network (WSN) systems, which have attracted much attention for a wide range of wireless communications applications, such as environmental surveillance, agriculture, health care, and intelligent buildings [2]. A current-waveform sensor capable of RF transmission with energy harvesting from AC power lines was recently reported as a key component of home/building energy management systems [3]. A large number of such wireless sensors will likely be used in future WSN systems. Implementing CR technology in those sensors would enable them to dynamically sense the frequency spectrum, find the available spectrum bands in the target spectral range, and then transmit immediately without introducing intra-sensor interference [4]. This would result in more efficient energy use by the RF devices, which would extend the system lifetime.

CR systems have been developed on the basis of the IEEE 802.22 standard [5], [6], but they cover only the 54–862-MHz bandwidth. The main problem in achieving a wider-band CR system is the need to use power-hungry and/or area-inefficient RF filters for interference rejection including rejection of the 7th-order harmonic component [7]. To address this problem, we have developed a wideband complementary metal oxide semiconductor (CMOS) receiver that uses a low-power tunable RF filter. The power used can be further reduced by reconfiguring the receiver parameters in accordance with the interference levels observed with a dynamic-range (DR) scalable energy detector, which is also applicable to white-space sensing.

This paper is organized as follows. Section II describes the approach we took to developing a wideband CMOS receiver and

its architecture. Section III describes the circuit design for each building block of the receiver, including the tunable RF filter and DR-scalable energy detector. The measured performances are discussed in Section IV. Finally, Section V summarizes the key points.

## II. RECEIVER ARCHITECTURE

### A. Design Approach

Our target was an integrated CR-receiver circuit covering TV broadcast and cellular bands from 30 MHz to 2.4 GHz. In such a wideband receiver, harmonic mixing is a serious concern. Up to the 80th harmonic order must be considered whereas a radio targeting 900 MHz to 5 GHz (cellular to WLAN bands) may have to deal with harmonics only up to the 5th or 6th order. Although a harmonic rejection mixer (HRM) can suppress the 3rd- and 5th-order harmonics of local oscillator (LO) signals, amplitude and phase mismatches limit the achievable harmonic rejection ratio (HRR) to typically 30–40 dB [8]. Furthermore, HRMs are much more complex if the 7th- and higher-order LO harmonics must be rejected [9].

One way to achieve wideband harmonic rejection is to use an RF filter before the HRM. The bandwidth of the filter must be tunable to support a wide range of radio frequencies. Although passive filters, such as surface acoustic wave (SAW) and inductor-capacitor (LC) ones, have high linearity and consume no power, tuning their frequency characteristics is difficult. In terms of tunability, which is essential for achieving a low-cost and small-area receiver, active filters, such as active resistance-capacitance (RC) and transconductance-capacitance (Gm-C) ones, are preferable. Since an active-RC-based RF filter has higher power consumption due to its power-hungry wideband operational amplifiers, a Gm-C-based one is a better choice in spite of its poor linearity. The linearity requirements can be relaxed by also using an HRM because an HRM enables the use of a lower-order filter, which is generally linear compared with a higher-order filter having very high impedance internal nodes. To reduce the power consumption of the receiver, we propose switching off and bypassing the RF filter when there is no interference or the interference is negligible. This can be easily accomplished by using the spectrum-sensing function of a CR receiver.

### B. Architecture

Fig. 1 shows a block diagram of the CR-receiver IC we designed. It consists of a wideband low-noise amplifier (LNA), attenuator, tunable RF filter, HRM, tunable baseband low-pass filter (BB LPF), programmable gain amplifier (PGA), and DR-scalable energy detector. The receiver parameters, such as the gain and bandwidth, are controllable via a serial peripheral interface (SPI). These building blocks are commonly used for both receiving communication signals and sensing radio environments.

The two-stage LNA with multiple feedback loops provides wideband impedance matching and a flat gain covering up to the 3-GHz band without the need for area-inefficient inductors [10]. The CMOS-inverter-based configuration reduces power consumption through the reuse of the bias currents and improves

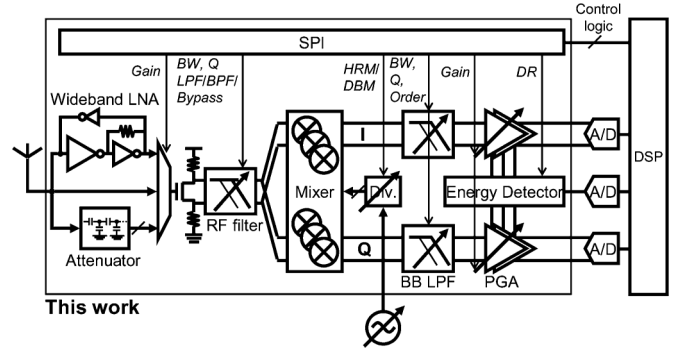


Fig. 1. Block diagram of wideband receiver.

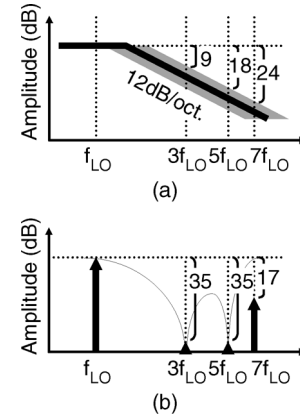


Fig. 2. Typical responses of (a) RF filter and (b) harmonic rejection mixer.

linearity through the cancellation of the even-order distortions. The CMOS-inverter cells do not have AC-coupling capacitors; that is, the p- and n-channel MOS (PMOS and NMOS) transistors are self-biased at the same gate voltage. This enables support of a low-frequency band (down to 30 MHz) with little size overhead. When there is strong interference, the capacitive attenuator or bypass path is used instead of the LNA. The LNA/attenuator output is AC coupled and drives a linear active balun. The use of the subsequent second-order tunable RF filter in combination with the HRM results in an HRR of over 40 dB for all odd-order harmonics without the use of external filters or complicated calibrations, as shown in Fig. 2. The cut-off frequency of the RF filter was roughly adjusted to about 1.4 times that of the carrier frequency, which is equal to the LO frequency  $f_{LO}$  in a direct-conversion receiver, to prevent losing the desired signal while at the same time suppressing the harmonics even with possible parameter variations. The lack of a higher-order RF filter enables low-power, highly linear, and low-noise operation.

The RF signal is down-converted to in-phase and quadrature-phase (I/Q) baseband signals, for which the bandwidths are limited by the following BB LPF, and the signal intensities are observed by the energy detector integrated with the PGA. Wideband spectrum sensing with resolution tunability and DR scalability is possible by sweeping the LO frequency. Although a frequency synthesizer was not implemented in this prototype chip, LO signals covering twice the frequency range, e.g., 5–10 GHz, can be generated by using two or three voltage-controlled oscillators, and lower frequency signals can be easily obtained

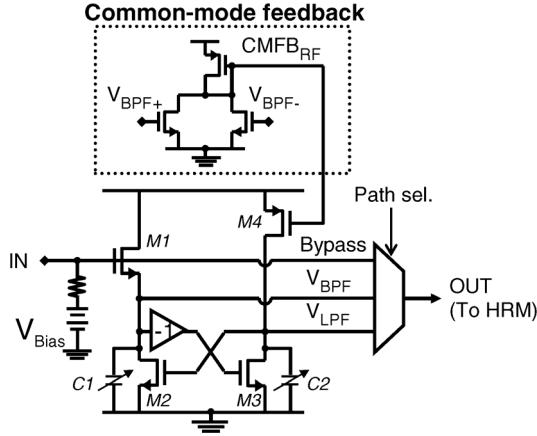


Fig. 3. Circuit diagram of single-ended RF filter.

by using a subsequent divider chain [11]. A divider circuit for four- and eight-phase LO clock generation, whose mismatches crucially affect the harmonic rejection, is integrated on the chip.

### III. CIRCUIT DESIGN

#### A. RF Filter

A schematic of our proposed source-follower-based tunable RF filter with two stacked transistors is shown in Fig. 3. Only single-ended circuits are depicted for simplicity. An inverting function is obtained by cross-coupling the differential lines. This RF filter can provide both low-pass and bandpass functions. It functions as a LPF when the carrier frequency is from 30 to 343 MHz and as a bandpass filter (BPF) when it is from 343 to 800 MHz. Even in LPF mode, low-frequency interference is suppressed because the subsequent passive mixer with load capacitors described below provides low impedance outside the desired frequency band. When the carrier frequency is above 800 MHz, the filter can be bypassed and shut down because the third-order LO harmonic component is outside the band. When the carrier frequency is below 800 MHz, the filter can still be bypassed and shut down if there is no strong interference in related bands, thereby reducing power usage.

The transfer functions of the BPF and LPF are expressed as

$$H_{\text{BPF}}(s) = \frac{V_{\text{BPF}}}{V_{\text{in}}} = \frac{s \frac{g_{m1}}{C_1}}{s^2 + s \frac{g_{m1}}{C_1} + \frac{g_{m2}g_{m3}}{C_1C_2}} \quad (1)$$

and

$$H_{\text{LPF}}(s) = \frac{V_{\text{LPF}}}{V_{\text{in}}} = \frac{\frac{g_{m1}g_{m3}}{C_1C_2}}{s^2 + s \frac{g_{m1}}{C_1} + \frac{g_{m2}g_{m3}}{C_1C_2}}, \quad (2)$$

respectively, where  $g_{mi}$  is the transconductance gain of transistor  $M_i$ . The cut-off (or center) frequency and quality factor are respectively written as

$$\omega_c = \sqrt{\frac{g_{m2}g_{m3}}{C_1C_2}} \quad (3)$$

and

$$Q = \frac{\sqrt{g_{m2}g_{m3}}}{g_{m1}} \sqrt{\frac{C_1}{C_2}}. \quad (4)$$

Since transistors M1–M3 are the same size and operate under the same bias condition in this design, i.e.,  $g_{m1} = g_{m2} = g_{m3} = g_m$ ,  $\omega_c$  and  $Q$  are given by

$$\omega_c = \frac{g_m}{\sqrt{C_1C_2}} \quad (5)$$

and

$$Q = \sqrt{\frac{C_1}{C_2}}. \quad (6)$$

They can thus be tuned by adjusting  $g_m$  and/or  $C_{1,2}$ .

The proposed RF filter achieves low-power wideband interference rejection for several reasons. The source-follower input transistor (M1) with capacitive load  $C_1$  functions as a highly linear first-order filter. The even-order distortions of transistors M2 and M3, which form part of a gyrator, are canceled by the inverse nonlinearity of M1 and by the squared current from transistor M4, respectively. The common mode signals are rejected by M4, unlike a reported low-power LPF [12]. This simple configuration creating a second-order filter with only three core transistors (M1–M3) enables high-frequency and low-noise operation. It also enables the use of relatively large gates for M1–M3, which reduces statistical process variations. Furthermore, the operation of M1–M3 under the same bias condition improves tolerance, especially during low-voltage operation.

Fig. 4(a) shows a schematic of the circuit in balanced configuration that has half-size dummy transistors (MDMY1 and MDMY5) for cancelling feedthrough via the gate-source capacitances of M1 and M5. For further common-mode rejection and stabilization, a cross-coupled nMOS pair and a diode-connected one are added to each node of  $V_{\text{LPF}}$  and  $V_{\text{BPF}}$  (Fig. 4(b)). This circuit provides low impedance for a common-mode signal in contrast to high impedance for a differential one.

To enable a wide tuning range (30 to 800 MHz) to be covered, 4-bit binary-weighted load-capacitor arrays are used to vary the filter characteristics. In addition, transconductance gain  $g_m$  is controlled by tuning the gate bias voltage of M1. Fig. 5 shows simulated frequency characteristics for different capacitor values (solid lines) and gate bias voltages (dotted lines). Here, the capacitances of  $C_1$  and  $C_2$  are equal, meaning that  $Q$  is 1 from (6). The highly linear performance corresponding to the 18-dBm in-band third-order input intercept point (IIP3) with a 1.2-V power supply, as shown in Fig. 6, suppresses intermodulation distortion caused by strong interference. The current consumption of this RF filter is as low as 10 mA.

#### B. Down-Conversion Mixer and Baseband Filter

The HRM (Fig. 7) consists of three passive mixers driven by 25% duty-cycle  $-45^\circ/0^\circ/45^\circ$  LO clocks plus the weighted adder merged with the BB filter. Only a single-ended circuit for the I-signal path is shown. The HRM suppresses the 3rd- and 5th-order LO harmonics by adding three-phase BB signals with a ratio of approximately  $1 : \sqrt{2} : 1$ ; as a result, it achieves, in combination with the RF filter, an HRR of over 40 dB. The 25% duty-cycle passive mixers with capacitive loads provide additional out-of-band interference attenuation due to the pole shift

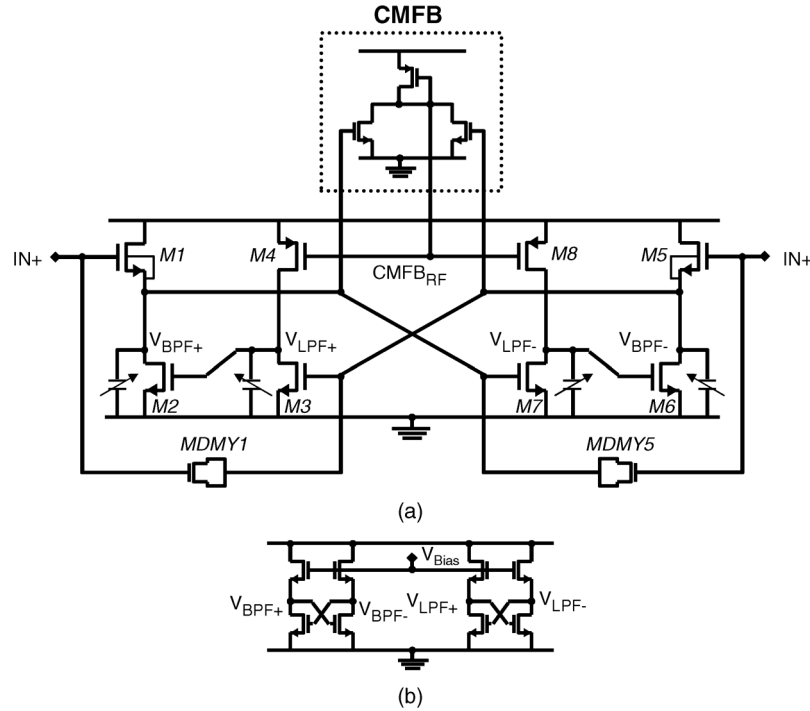


Fig. 4. (a) Circuit diagram of differential RF filter and (b) common-mode rejection/stabilization circuit.

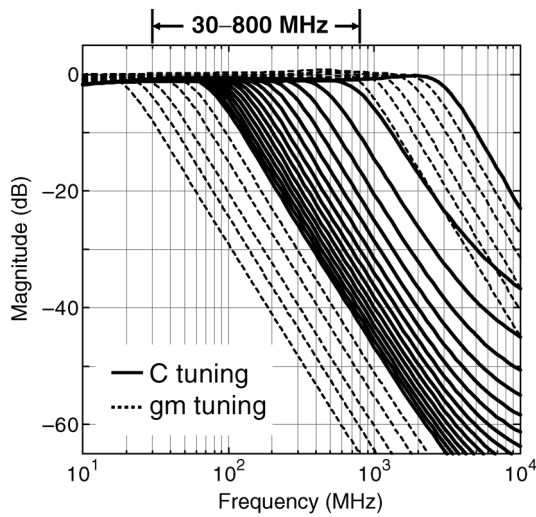


Fig. 5. Simulated frequency characteristics of RF filter.

of the input impedance from the BB to the RF band [13]–[15]. These capacitors also contribute to minimizing the effect of the voltage-dependent gate capacitances.

When the third-order LO harmonic component is out of band, the HRM can be made to operate as a double-balanced mixer (DBM) by setting the LO phases to  $-90^\circ/0^\circ/0^\circ$ . This  $-90^\circ/0^\circ/0^\circ$ -DBM has a conversion gain closer to that of the HRM than does the  $0^\circ/0^\circ/0^\circ$  DBM as Fig. 8 shows. In addition, this approach is area-efficient compared with that having an additional DBM in parallel with the HRM [6].

To enable a simple connection to the down-conversion mixer, four-phase or eight-phase LO clocks are generated by a shared

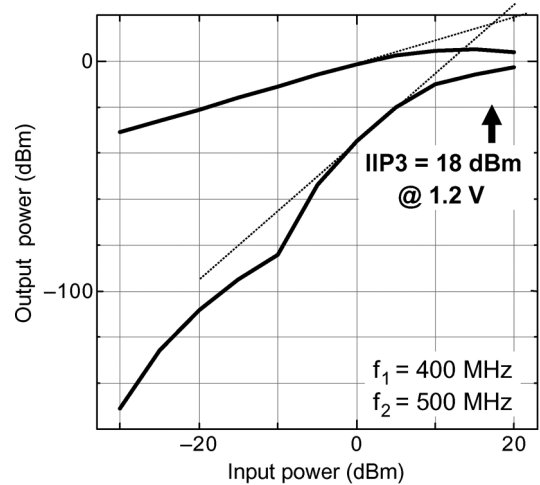


Fig. 6. Simulation results for two-tone test of LPF.

divider circuit that consists of four D-latches, L1–L4, as illustrated in Fig. 9. Although only a single LO clock path is depicted, a differential configuration based on current-mode logic was used in the prototype chip. The divider ratio is changed by using a one-bit control signal, CTL. When CTL is high, this circuit is a simple divide-by-four circuit, as shown in Fig. 10(a), and generates an eight-phase 50% duty-cycle clock. When CTL is low, it is a divide-by-two circuit, as shown in Fig. 10(b), and provides a four-phase clock because latches L2 and L4 pass the input data directly to the next stage with some delay. If the delay is shorter than 1/8 the LO signal's period, the mixer operation is not harmfully affected. This condition can easily be met because the delay time is about 20 ps with 90-nm CMOS technology, whereas 1/8 the LO period is about 50 ps at the highest

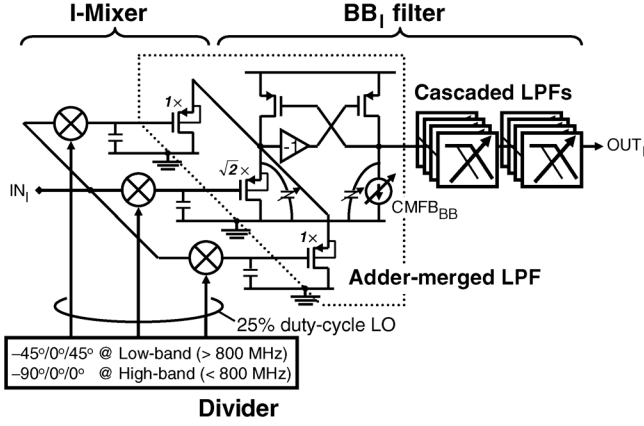


Fig. 7. Circuit diagram of harmonic rejection mixer followed by baseband filter.

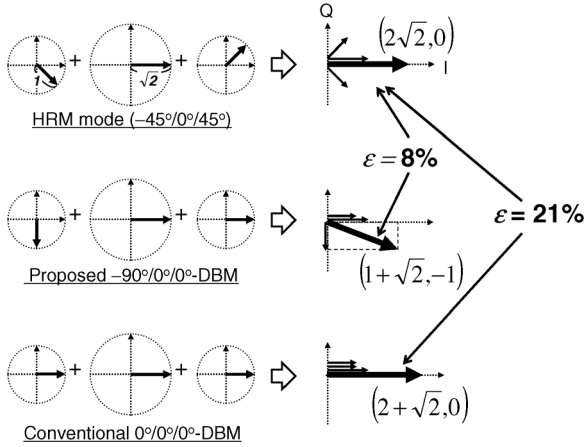


Fig. 8. Gain comparison of HRM,  $-90^\circ/0^\circ/0^\circ$ -DBM, and  $0^\circ/0^\circ/0^\circ$ -DBM.

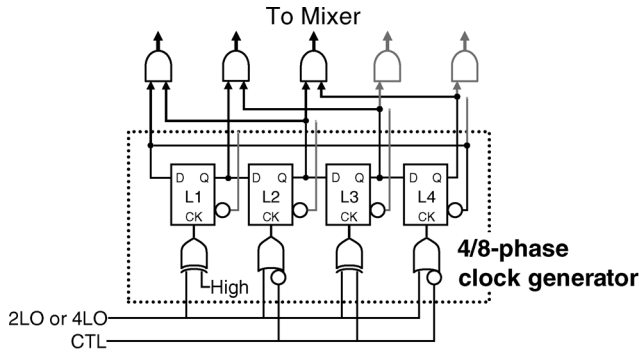


Fig. 9. Circuit diagram of divider.

frequency (2.4 GHz). If the delay time is equal to  $1/8$  the LO period, the operation of the proposed DBM is the same as that of the HRM.

The BB filter, which consists of an adder-merged LPF followed by two cascade-connected second-order LPFs, has the same configuration as the RF filter except for using a PMOS-based topology to reduce flicker noise. Another reason for using this topology is that the low common-mode voltage level of the pMOS input stage is optimal for using a small NMOS-based switching mixer, which can be driven by low-power LO drivers.

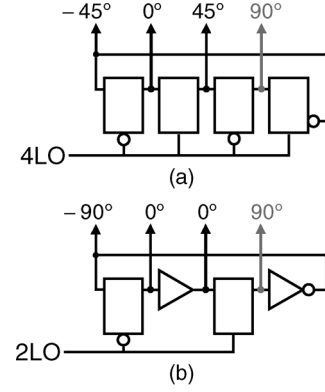


Fig. 10. Operation mode of divider: (a) harmonic rejection on and (b) harmonic rejection off.

The second-order LPFs, which consist of four unit circuits arranged in parallel, can be made to operate at an optimized noise level and power consumption in accordance with the desired signal level by changing the number of active unit circuits. The bandwidth can be widely tuned (from 0.2 to 30 MHz) by using six-bit capacitor arrays to support a variety of channel bandwidths.

### C. Energy Detector

An energy detector generally has a trade-off between its sensitivity in V/dB and its dynamic range. Our DR-scalable energy detector (Fig. 11) overcome this trade-off. It is based on a received signal strength indicator (RSSI) circuit, which comprises limiting amplifiers, rectifiers, and a passive RC filter with two poles. The independently controllable rectifiers, each with a programmable current mirror stage (Fig. 12), provide DR scalability, which enables shared use for both white-space sensing and interference-level detection. In addition, the energy detector, which is naturally applicable to observing the desired signal strength for automatic gain control (AGC), is area-efficient, unlike a dedicated detector [5]. Its area efficiency is further enhanced by the use of an I/Q configuration that can ideally cancel even-order components by adding the I/Q rectifier currents. Waveforms of the input I/Q signals, rectified signals, and I/Q-combined output are shown in Fig. 13. The small on-chip RC filter that follows sufficiently attenuates the residual harmonic components. This configuration reduces the convergence time, which speeds up spectrum sensing.

The operation principle of the energy detector is depicted in Fig. 14. In the high-sensitivity mode required for white-space detection, only the rectifiers in the last few stages are activated with large current mirror ratios (the other rectifiers do not output current) (Fig. 14(a)). This results in a steep RSSI feature (Fig. 15(a)), reducing the quantization errors of the following ADC equivalently. That is, RSSI sensitivity is enhanced. In the wide-DR mode required for interference-level detection, all of the rectifiers are activated and have low output currents (Fig. 14(c)), expanding the dynamic range (Fig. 15(c)). A medium DR/sensitivity RSSI feature is achieved by setting the mirror ratios as shown in Fig. 14(b). Thus, simple control of each rectifier's mirror ratio ( $M_j$ ) is used to achieve DR scaling. A replica biasing circuit, shown in Fig. 11, compensates for

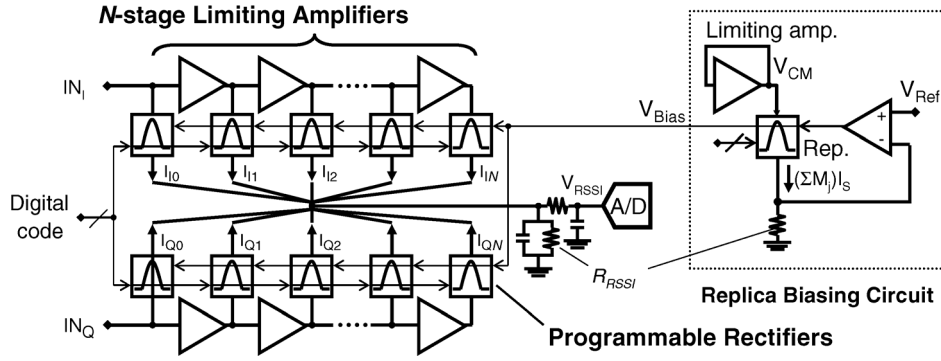


Fig. 11. Circuit diagram of DR-scalable energy detector.

TABLE I  
MIRROR RATIOS OF PROGRAMMABLE RECTIFIERS FOR EACH MODE

	$M_0$	$M_1$	$M_2$	$M_3$	$M_4$	$M_5$	$M_6$	$M_{\text{Rep}} = \sum M_j$
High sensitivity	0	0	0	0	3	3	3	9
Med. sensitivity/DR	0	0	0	2	2	2	2	8
Wide DR	1	1	1	1	1	1	1	7

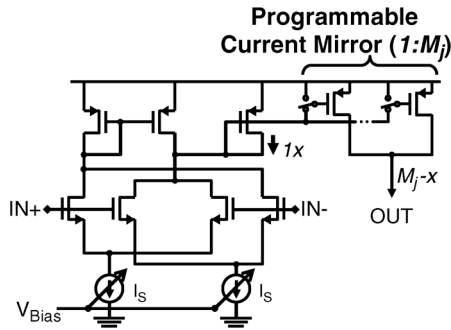
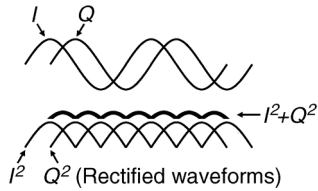
Fig. 12. Circuit diagram of  $j$ -th rectifier with programmable current mirror stage.

Fig. 13. Input and output waveforms of rectifiers.

process, voltage, and temperature variations in reference current  $I_S$  by tuning the maximum voltage level  $V_{\text{Max}}$  so that it is equal to half  $V_{\text{Ref}}$  for each mode.

In the prototype design, this detector is composed of six-stage limiting amplifiers merged with the PGA and seven rectifiers with two-bit programmable current mirrors for each I- and Q-signal path. The mirror ratios for each mode are shown in Table I, where  $M_{\text{Rep}}$  denotes the mirror ratio of the replica rectifier.

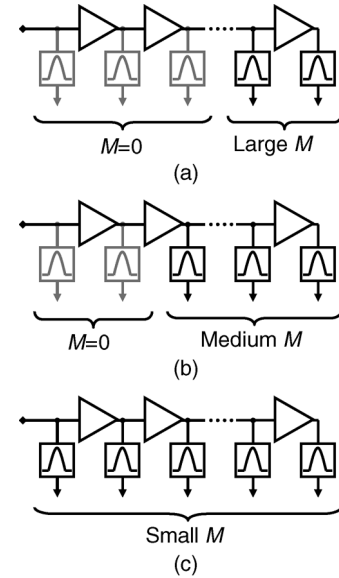


Fig. 14. Operation principle of DR-scalable energy detector: (a) high sensitivity mode, (b) medium sensitivity/DR mode, and (c) wide-DR mode.

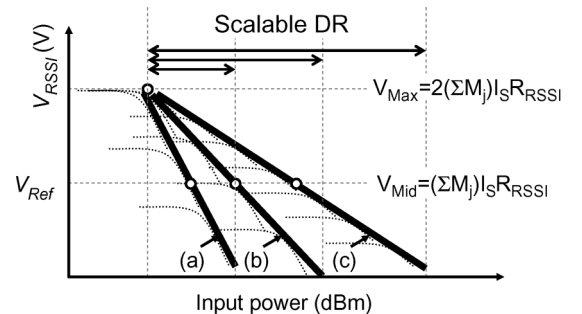


Fig. 15. RSSI characteristics with scalable DR.

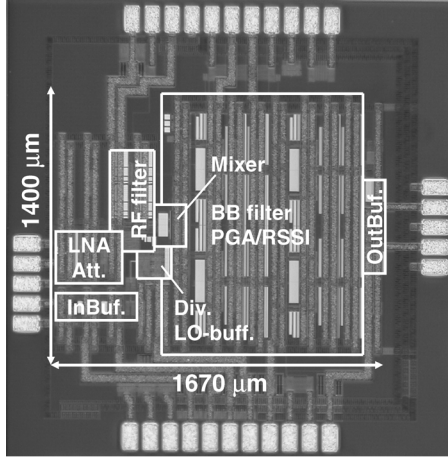


Fig. 16. Die photograph of fabricated chip.

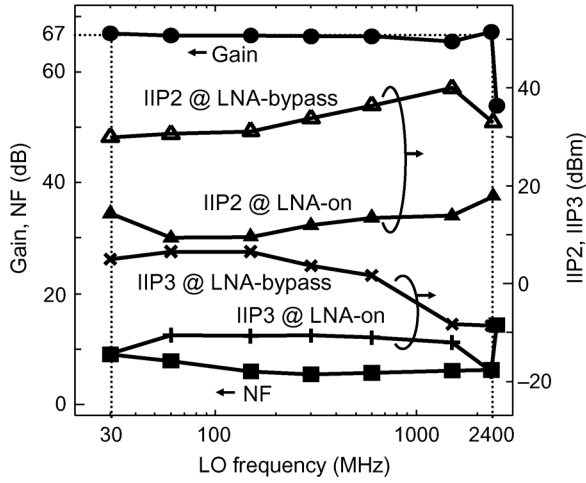


Fig. 17. Measured receiver performance.

#### IV. MEASUREMENT RESULTS

We fabricated a wideband receiver chip using 90-nm CMOS technology that is only 2.3 mm<sup>2</sup>. A die photograph of this test chip is shown in Fig. 16.

Fig. 17 shows the measured receiver performance: total gain, noise figure (NF), in-band IIP3, and IIP2 (second-order input intercept point). The receiver can support an RF range of 30 MHz to 2.4 GHz with an NF of 5–8 dB at the maximum gain of 67 dB. The IIP3 was –11 and +1.7 dBm at 600 MHz when the LNA was on and off, respectively. At the same gain settings, the average IIP2 was 14 +2/–3 and 38 +2/–5 dBm, respectively, at 600 MHz, as measured for five samples. The out-of-band IIP3 was measured to be –10 dBm at the maximum front-end gain. In this measurement, two-tone continuous-wave signals of 800 and 900 MHz were applied to the RF input port as out-of-band interferers, and the amplitude of third-order intermodulation product at the desired band of 700 MHz was measured.

The measured HRRs are plotted in Fig. 18. Rejection of over 42 dB was obtained for all odd-order harmonics without using external filters. The mean 3rd-order HRR was 45 dB with a standard deviation of 1 dB at 600 MHz, as measured for five chips.

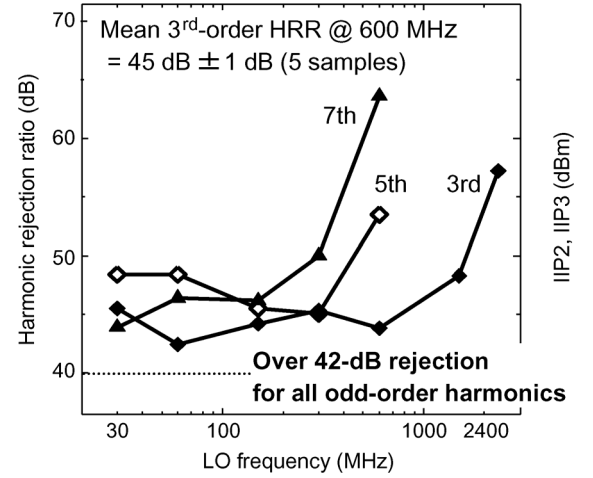


Fig. 18. Measured harmonic rejection ratio.

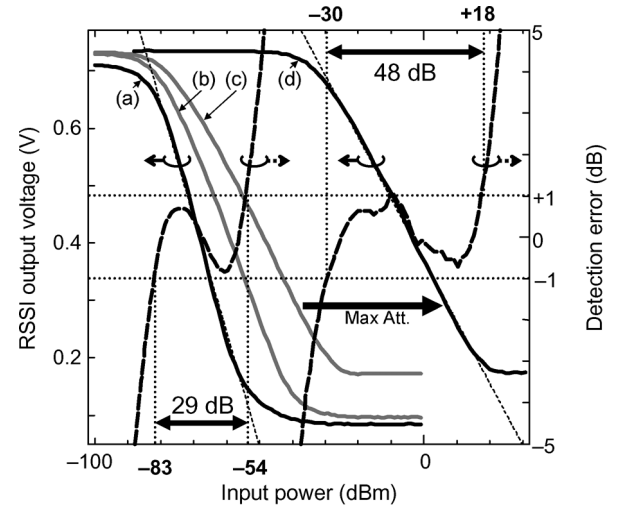


Fig. 19. Measured RSSI performance.

TABLE II  
PERFORMANCE SUMMARY AND COMPARISON OF SPECTRUM SENSING

	This work	[5]	[17]
Frequency (GHz)	0.03–2.4	0.4–0.9	0.05–1.5
Det. bandwidth (MHz)	0.2–30	0.025–0.8	0.1–1
Min. det. level (dBm)	–83	–74	–110 – –97 <sup>a</sup>
Dynamic range (dB)	29–48 <sup>b</sup>	32	– <sup>c</sup>
Power consumption (mW)	30–44	119 <sup>d</sup>	191
CMOS Technology	90 nm	0.18 μm	65 nm

<sup>a</sup> Estimated from NF with 1-MHz resolution bandwidth.

<sup>b</sup> Without changing front-end gain.

<sup>c</sup> Spurious free dynamic range was reported to be 89 dB.

<sup>d</sup> Excluding voltage-controlled oscillator and phase locked loop.

The receiver draws only 37 mA from a 1.2-V supply. This current can be reduced a further 30% even for carrier frequencies below 800 MHz through appropriate reconfiguration, such as switching off the RF and BB filters, if there is no interference or it is negligible.

TABLE III  
PERFORMANCE SUMMARY AND COMPARISON OF WIDEBAND RECEIVER

	This work	[14]	[15]	[16]	[6]	[7]	[8]
Frequency (GHz)	0.03–2.4	0.4–6	0.8–2	0.2–2	0.05–0.86	0.05–0.86	0.4–0.9
Max. gain (dB)	67	70	78	19	107	83	34
NF (dB)	5–8	3	3.1	6.5	5–8.5	4–7	4
In-band IIP3 (dBm)	–11	+6	–12	+11	–20 <sup>a</sup>	–14	+3.5
Out-of-band IIP3 (dBm)	–10	+10	–	–	–	–	+16
IIP2 (dBm)	38	70	45–50	65	–	17	46
HR3 (dB)	>42	–	–	–	43	72	60
HR5 (dB)	>42	–	–	–	60	–	64
HR7 (dB)	>42	–	–	–	–	–	17
Power cons. (mW)	30–44	30–55	55 mA <sup>b</sup>	67	65–77	540 <sup>c</sup>	60
CMOS technology	90 nm	40 nm	65 nm	65 nm	180 nm	180 nm	65 nm

<sup>a</sup> Estimated from figure.

<sup>b</sup> From battery.

<sup>c</sup> Analog portion including phase locked loop.

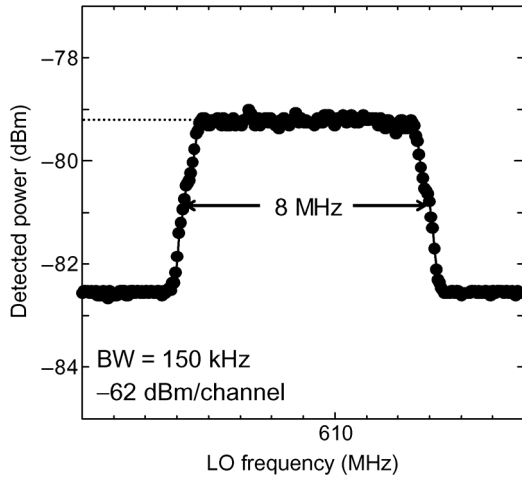


Fig. 20. Measured spectrum sensing results in white-space sensing mode.

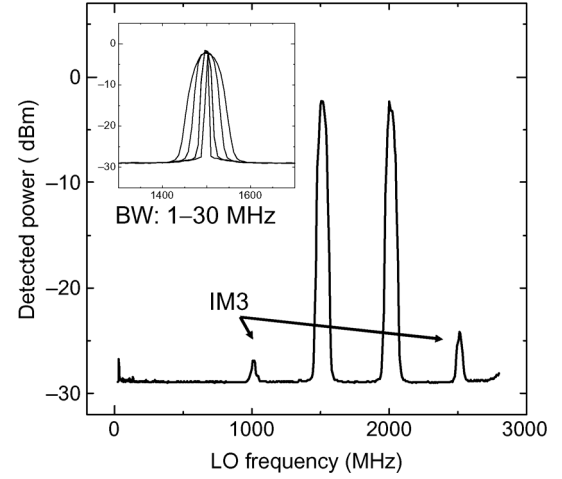


Fig. 21. Measured spectrum sensing results in interference-level detection mode.

The measured characteristics of the energy detector are plotted in Fig. 19. In the highest sensitivity mode with the maximum front-end gain (indicated by (a) in the figure), the minimum detection level within 1-dB error was  $-83$  dBm and the RSSI sensitivity was 20 mV/dB. Changing each rectifier's output current increased the DR to 48 dB, as indicated by (b) and (c). With the widest DR mode, (c), the maximum detection level was  $-27$  dBm, and this value shifted to  $+18$  dBm when the maximum front-end attenuation was applied, as indicated by (d). This demonstrates that our proposed detector can cover the entire range of  $-83$  to  $+18$  dBm. The results of white-space sensing with the detector in the highest sensitivity mode are plotted in Fig. 20. The detection bandwidth of 150 kHz was defined by the BB-filter cut-off. An 8-MHz channel-bandwidth DVB-T (digital video broadcasting-terrestrial) signal centered at 609 MHz with  $-62$ -dBm channel power, which is equal to  $-79$ -dBm/150-kHz, was successfully detected. Combining

the proposed energy detector with a feature detection technique would make it possible to achieve the higher sensitivity required for IEEE 802.22 applications [5]. The results of interference-level detection with the widest DR mode are shown in Fig. 21. The interference was created using 1.5- and 2.0-GHz 0-dBm two-tone continuous-wave signals. The energy detector was able to detect these strong interference signals with its widely tunable detection bandwidth (1 to 30 MHz). The detection results for the interference condition help determine the optimum receiver configuration in terms of noise, linearity, and power consumption. Performance is summarized in Table II and Table III in comparison with that of other recent work.

## V. CONCLUSION

A 30-MHz–2.4-GHz CMOS receiver with an integrated tunable RF filter and dynamic-range-scalable energy detector was described as a key building block for cognitive radio systems.

The receiver, which uses a newly proposed RF filter with only two stacked transistors, suppresses wideband interference with low power consumption and high linearity. Power consumption can be further reduced by adjusting the receiver configuration in accordance with the interference levels detected by the energy detector. A 2.3-mm<sup>2</sup> test chip, fabricated using 90-nm CMOS technology, achieved over 42-dB harmonic rejection including 7th-order harmonic component without any external device, a 67-dB gain, a 5–8-dB noise figure, a –11-dBm in-band third-order intercept point, and a +38-dBm second-order intercept point while drawing only 25–37 mA from a 1.2-V power supply. Multi-resolution spectrum sensing with a 0.2–30-MHz detection bandwidth, –83-dBm minimum sensitivity, and 29–48-dB dynamic range was demonstrated.

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