Bumpless Build-Up Layer Packaging

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***Abstract*—Bumpless Build-Up Layer (BBUL) is a novel package developed to meet future packaging technology requirements. The BBUL package provides the advantages of small electrical loop inductance and reduced thermomechanical stresses on low dielectric constant (low-*k*) die materials. Furthermore, it allows for high lead count, ready integration of multiple electronic and optical components [such as logic, memory, radio frequency, microelectromechanical systems (MEMS), among others], and inherent scalability. In the present paper we investigate and discuss some of the process, routing, electrical, thermal, and mechanical attributes of BBUL.**

1. Introduction

As integrated circuit technology advances, packaging high performance microprocessors becomes increasingly challenging. Future generations of Intel microprocessors are expected to have larger numbers of signal leads, stricter control of impedance and crosstalk on these lines, and greater demands for power delivery and heat extraction. For microelectronic packaging, two of the major challenges are electrical performance and thermal management. From an electrical standpoint, the goal of the packaging world is to maintain the signal integrity and operating frequency of the semiconductor device as much as possible. This task is complicated by the often large inductances introduced to the total device-package-motherboard circuit by the package. On the other hand, the package is almost completely responsible for providing a means for extracting thermal energy dissipated at the active semiconductor area.

Aside from the electrical and thermal performance considerations, other technical challenges remain. Continued reduction in end product size requires a package with a small form factor that allows for dense placement of input and output electrical connections. Future microprocessors may also require integration of multiple chips or other electrical and optical components on the same package with minimum component spacing, maximum number of interconnects between components, and tight restrictions on signal latency, impedance matching, and noise. Furthermore, the cost budget available for packaging and assembly is flat or declining, following the trend of microprocessor average sales prices. Meeting these demands stretches or exceeds the capabilities of current packaging technologies, such as Intel's flip-chip pin grid array (FCPGA) package [1].

An added challenge for future generations of logic technology is presented by the anticipated integration of low dielectric constant (low-k) materials on-chip. Low-k dielectric materials, especially those with dielectric constants at or approaching a value of 2, have very poor mechanical robustness and will be able to withstand little or no tensile or shear force. Mismatch of coefficients of thermal expansion (CTE) among the various component materials of a package makes satisfying this requirement difficult.

Many of these issues could be addressed with a chip-scale package (CSP) in which the package redistribution layers are built up on top of the die [2]–[5]. However, packaging advanced logic chips makes additional demands that require the area of the package to be considerably larger than the area of the chip. Area is needed for an adequate number of pins for the signals and power while meeting motherboard pitch limitations, and for added components such as decoupling capacitors. To meet these myriad requirements, we are developing a new package, the Bumpless Build-Up Layer (BBUL) package.

BBUL is designed to meet packaging technology requirements for Intel's 65 nm generation silicon technology and beyond. Microprocessors produced with this generation of silicon process technology are expected to reach speeds in excess of 10 GHz. BBUL provides advantages of low loop inductance for decoupling capacitors, high lead count, ready integration of multiple electronic and optical components [e.g., logic, memory, radio frequency, microelectromechanical systems (MEMS), etc.], low mechanical forces imposed on the die, and inherent scalability. BBUL does not specifically address the issue of heat extraction, but it is compatible with future advances in thermal systems that may be developed separately. In this paper we demonstrate the routing advantages provided by BBUL, as well as simulations showing significant improvement in electrical power delivery performance for BBUL vs. a standard FCPGA package. Reliability results and simulations demonstrating the mechanical

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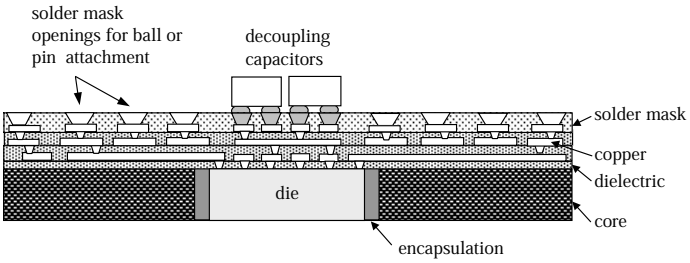


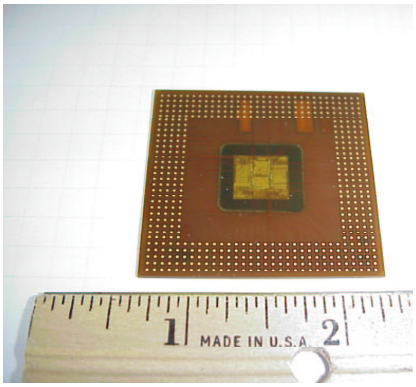
Figure 1: Schematic cross-section of a three-layer BBUL package.

advantages of BBUL for integration of on-chip low-k dielectric material are presented elsewhere.

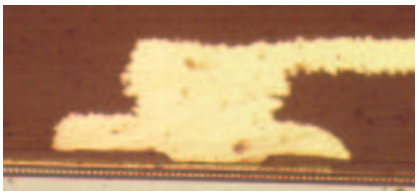
2. Process and routing

BBUL differs from traditional assembled packages in that it consists of a die or dice embedded in a substrate, such as bismaleimide triazine (BT) laminate or a copper heat spreader, which then has one or more build-up layers formed on top. A standard microvia formation process, such as laser drilling, makes the connections between the build-up layers and the die bond pads. This is analogous to a wafer level CSP (WLCSP) with the die embedded in the panel to increase the area. The embedding of the die or dice in the panel may be done with molding or dispensed encapsulation material. As with certain other proposed CSP technologies, the build-up layers are made with a standard high-density integration (HDI) patterning technology. This build-up technology is similar to what is typically used for advanced organic packages (e.g., FCPGA) and printed circuit boards. Die bond pads may be arranged in any pattern subject to the pitch limitations of the HDI process. To simplify the laser drilling process and to relax the via to bond pad alignment constraint, a copper pad expansion may be formed over the bond pad openings, as shown in the schematic cross-section of Fig. 1. In Fig. 2 we present photographs of a BBUL-packaged test chip [Fig. 2(a)] and this same package in cross-section [Fig. 2(b)]. The process flow is illustrated in Fig. 3.

The BBUL structure offers several routing advantages compared to flip-chip interconnection. First, the current via size and alignment capabilities of HDI via formation processes allow a tighter pitch for the die-package interconnections compared to flip-chip. Continuous improvements in HDI substrate patterning capabilities are driven by the requirements of a broad range of packaging and circuit board applications; BBUL die-package pitch can be scaled down as these improvements come on line. Also, unlike many versions of flip-chip assembly, die-package interconnections can be arbitrarily placed, because no restriction is imposed by limitations of the flip-chip underfill process. This capability provides a significant advantage in the number of signals that can be routed out from the die on a single layer, as shown in Fig. 4. Since the BBUL package is one-sided, there are no plated through-holes and no underutilized wiring layers on the backside of the package. The combination of these effects can typically reduce the required layer count by 50% or more. Table 1 shows some typical routing results comparing the current state-of-the-art for flip-chip and BBUL.



(a) Test chip in BBUL package with land grid array.



(b) Cross-sectional view of die-package interface.

Figure 2: Photographs of a BBUL package.

Due to the layer count reduction and elimination of the package core and die-package solder connection, BBUL technology allows the overall package to be very thin. The thickness of the package will exceed the die thickness by 100 μm or less, depending on the thermal and socketing solution used. This attribute is attractive for mobile (laptop) applications and is also a main contributing factor to the improvements offered by BBUL in power delivery and mechanical stress.

Of course, BBUL is subject to the same drivers for known good die (KGD) yield and assembly and packaging yield that apply to other build-up CSPs. The KGD issue can be addressed by testing the dice before they are embedded in the package panel. Yield loss in the packaging steps result in loss of the known good dice; this die yield loss adds to the overall cost of the package. However, we believe that, with appropriate yield optimization of

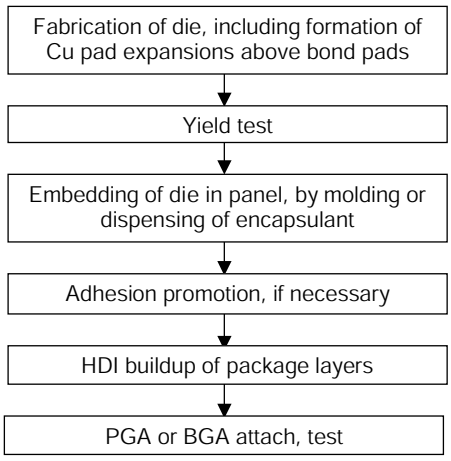
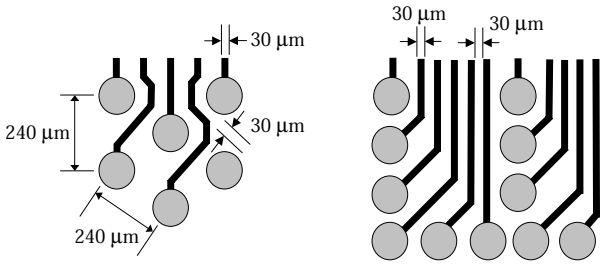


Figure 3: Process flow for formation of BBUL package.



(a) Standard package (constrained to fixed pitch).

(b) BBUL package with equivalent design rules.

Figure 4: Escape routing.

the package processing, the performance advantages combined with the package layer count reduction should allow this package to be cost effective in the advanced microprocessor market segment.

3. Electrical performance

In order to demonstrate and quantify some of the electrical performance enhancements offered by the BBUL technology, we conduct transient electromagnetic (EM) simulations for the core power delivery problem. We start out with a simplistic lumped-element theory, setting the stage for the EM simulations that consider realistic package designs and providing definitions of figures of merit used in the interpretation of the simulation results.

	Flip-chip	BBUL
Minimum pitch		
Bump pitch [μm]	240	No bumps
Build-up land size [μm]	150	150
Minimum land spacing [μm]	30	30
Minimum die-package pitch [μm]	240	180
Escape routing		
Core pitch [μm]	335×335	250×250
Periphery pitch [μm]	240×415	$\geq$180
Build-up line/space width [μm]	30/30	30/30
Build-up land size [μm]	150	150
Escape pitch [μm]	100 (4 rows)	75 (4 rows)

Table 1: Comparison of routing capabilities of flip-chip and BBUL, based on equivalent design rules (Intel 0.13 μm generation process technology for flip-chip and package).

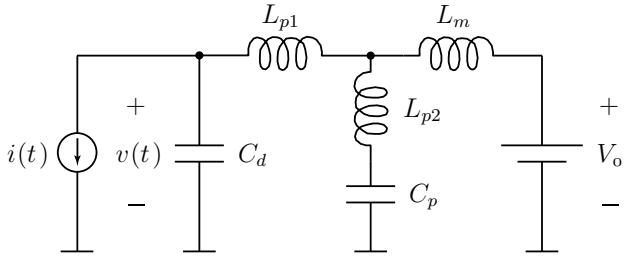


Figure 5: Lumped-element model of a power delivery structure.

Lumped-element power delivery modeling

Figure 5 shows a simplified lumped-element model of a power delivery structure involving an active die, a package, and a DC voltage supply [6]. For a quiet die, $i(t) = I_0 = \text{const.}$ with I_0 a leakage current flowing through the package inductance L_{p1} and the inductance L_m in between the package and the power supply located on the motherboard. The supply voltage V_0 appears as $v(t)$ across the on-die, high-frequency decoupling capacitance C_d that is inactive in the DC case, similar to the on-package, mid-frequency decoupling capacitance C_p with its associated parasitic inductance L_{p2}. Simultaneous switching of a large number of on-die core devices will draw a large current from the package which, in a simplistic manner, can be modeled as

$$i(t) = I_0 + \Delta I\, u(t) \tag{1}$$

where ΔI is the current step and $u(t)$ the unit step function. During the first few nanoseconds following the current step the relative large inductance L_m effectively isolates the power supply from the rest of the circuit and, letting $L_m \to \infty$, the inductances L_{p1} and L_{p2} combine as

$$L_p = L_{p1} + L_{p2} \tag{2}$$

where L_p is referred to in the following as the loop inductance of

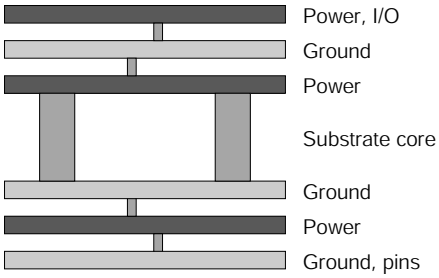


Figure 6: Stack-up of a six-layer standard package.

the package. Denoting

$$\omega_0^2 = \omega_1^2 + \omega_2^2 \tag{3}$$

where

$$\omega_1^2 = \frac{1}{L_p\, C_d}\ ,\ \ \omega_2^2 = \frac{1}{L_p\, C_p} \tag{4}$$

the initial-value problem is readily solved using the Laplace transform formalism and we obtain

$$v(t) = V_0 - \frac{\Delta I}{\omega_0\, C_d}\left[\left(1 - \frac{\omega_2^2}{\omega_0^2}\right)\sin\omega_0 t + \frac{\omega_2^2}{\omega_0}\, t\right] u(t) \tag{5}$$

Equation (5) describes the combination of oscillations of the resonator formed by decoupling capacitance and loop inductance on one hand, and the progressing discharging of the capacitors on the other. For typical microchips C_p is much larger than C_d. As $C_p \to \infty$, we find that Eq. (5) simplifies to

$$v(t) = V_0 - \Delta I \sqrt{\frac{L_p}{C_d}}\ \sin\omega_0 t\ u(t) \tag{6}$$

where

$$\omega_0 = \frac{1}{\sqrt{L_p\, C_d}} \tag{7}$$

The "drooping" of the die voltage as described by Eq. (5) and in simplified form by Eq. (6) can limit the performance of the microchip.[1] Equation (6) displays the dependence on loop inductance explicitly. BBUL targets the reduction of the inductance L_{p1} in Fig. 5 by reducing the thickness of the package. This in turn may allow usage of a smaller on-package capacitance C_p with lower associated parasitic inductance L_{p2}. Thus, the loop inductance L_p of the package can be reduced significantly. In the following section we demonstrate this by simulations based on an actual package design, quantifying the improvement in loop inductance BBUL is expected to provide.

[1] It is pointed out that the analysis holds only for the early portion of the response, as indicated by the unbounded behavior of Eq. (5). A correct description at later times needs to take into account losses and, more importantly, the influence of the power distribution system beyond the boundaries of the package [7].

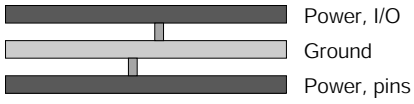


Figure 7: Stack-up of a three-layer BBUL package.

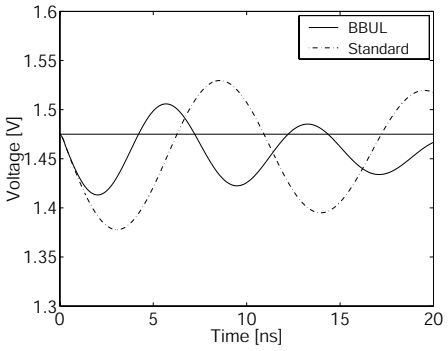


Figure 8: Transient simulation results for the mean die voltage of the two packages.

Design-driven electromagnetic simulation

We obtain power delivery time-domain results for a standard six-layer flip-chip package and compare them with a model of a similar three-layer BBUL package. The simulations are carried out using the commercial Sigrity SPEED2000$^{\mathrm{TM}}$ tool [8], incorporating EM wave propagation through the multiple layers of the complex package structures. The overall methodology employed allows a realistic comparison of the electrical performance of BBUL against a standard package for a major Intel product.

The power and ground nets of the standard package were extracted from the full design file and translated into the EM simulator format. Careful manual and semi-automatic editing was then applied to generate a structure that can be simulated successfully. The resulting model contains power and ground planes of various shapes and more than 4200 vias; the individual locations of these vias are fully taken into account during the simulation. The schematic stack-up structures of the two packages are shown in Fig. 6 and 7, respectively, indicating the basic functionality of the different layers. The BBUL package was generated by retaining the two top layers and the bottom layer of the standard package, reversing the polarity of the bottom layer, and reconnecting the vias as appropriate. In this BBUL package based on a realistic design we encounter about 2300 vias. A distributed $5{\times}5$ die model similar to what is shown in [7] and incorporating a power map is connected to the packages. Land-side decoupling capacitors amounting to a C_p of more than 20 μF are placed at the bottom of the package. The lumped parasitic inductance of these

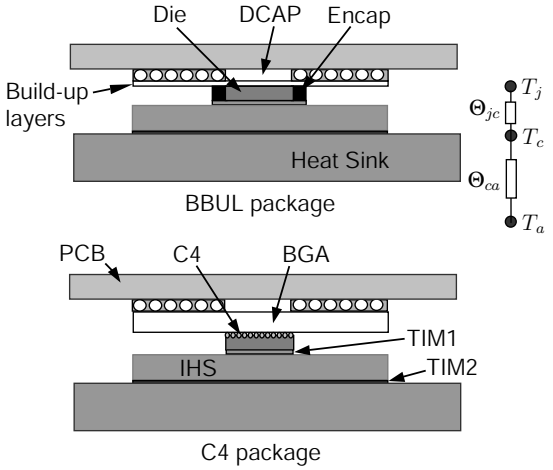


Figure 9: Thermal models of BBUL and C4 package.

	$\kappa_{\mathrm{th},x}, \kappa_{\mathrm{th},y}, \kappa_{\mathrm{th},z}$ [W/mK]	L_x, L_y, L_z [mm]
Sink	398, 398, 398	64, 64, 6.4
TIM2	30, 30, 30	34, 34, 0.2
IHS	398, 398, 398	34, 34, 15
TIM1	64, 64, 64	11.9, 11.9, 0.2
Die	120, 120, 120	11.9, 11.9, 0.775
Encap	0.2, 0.2, 0.2	13.9, 13.9, 0.775
Build-up layers	3, 3, 0.69	34, 34, 0.135
C4 bumps	0.5, 0.5, 1.24	11.9, 11.9, 0.1
BGA board	50, 50, 2	34, 34, 1.1
Solder balls	5, 5, 28	34, 34, 0.5
DCAP	0, 0, 0	11.9, 11.9, 0.5
PCB	3, 3, 0.3	64, 64, 1.6

Table 2: Thermal input parameters: thermal conductivities and dimensions of the different regions.

capacitors is given by L_{p2} =1.3 pH. Finally, an ideal power supply is connected directly at all the power and ground pins; there is no socket or motherboard in the simulated models. Thus, the inductance L_m in Fig. 5 is formed by the lateral plane inductance of the packages; the on-package decoupling capacitors are confined to the area directly underneath the die, whereas the pins are along the periphery of the package.

Figure 8 shows the die voltage as obtained from the time-domain EM simulation for the two packages, using identical die, decoupling capacitor, and power supply partial circuits. In each case, the voltages across the 25 independent current sources were averaged at each point in time. The results show the significant improvement of the power delivery performance that BBUL can provide. Based on the values in Fig. 8 of the first voltage minimum occurring between zero and 5 ns (the "first droop") and using Eq. (6), we can quantify this improvement in terms of a few simple numbers.

The magnitude of the first droop is found to be reduced by 36%. Whereas the loop inductance L_p of the standard package based on the simulations here is calculated to be 5.4 pH, the BBUL package exhibits an L_p of 1.4 pH; this is a reduction by 74%. Evidently, the loop inductance of the BBUL package is dominated by the lumped parasitic inductance L_{p2} of the discrete decoupling capacitors. In terms of the package inductance L_{p1} we have a reduction from 4 pH to 0.1 pH, or by 98%. This reduction is even more dramatic than one would expect from the mere reduction of the overall thickness of the package by 90%, highlighting the importance of taking into account the details of the package design.

The results described above show a clear benefit of BBUL for power delivery. Further improvements could apparently be made. For example, the closeness of the decoupling capacitors to the die makes them highly effective locally. Thus, an optimization of their placement may be interesting. Furthermore, a reduction of the nominal value of the decoupling capacitance can be investigated (under careful consideration of not only the first droop as in this paper). Physically smaller capacitors have smaller parasitic inductance, leading to further reduction of the package loop inductance in BBUL. In addition, choosing smaller capacitors yields increased flexibility for placement optimization and cost reduction.

4. Thermal modeling

Thermal management does not only face the challenges of increasing power and power density but also the increasing non-uniformity of the power distribution. Studies have shown that the thermal performance of a package is significantly affected by the non-uniformity of power dissipation [9]. The transistor junction to case thermal resistance with non-uniform power distribution might be 2 to 3 times larger than that for uniform dissipation. In order to simulate a realistic device, we randomly generated a non-uniform power map with a total power of 120 W. The average power density on the 1.19 by 1.19 cm die is 84.7 W/cm^2, and the peak power density is 5 times the average. In our model, a heat flux with this power distribution is applied on the front side of the die in order to represent the heat generated by the transistors and interconnect structures.

We studied the thermal performance of BBUL and standard flip-chip Controlled Collapsed Chip Connection (C4) packages using finite element method based commercial software, ANSYS. Cross-sectional views of the three-dimensional thermal models of BBUL and a C4 package are shown in Fig. 9. The DCAP region, as well as the core (see Fig. 1), are treated as voids and have zero thermal conductivity. The geometric parameters and thermal properties used in our models are given in Table 2. Because traditional thermal solutions are integrated at the exposed backside of the die, these thermal solutions [inte-

	BBUL	C4
T_j [°C]	98.7	97.4
T_c [°C]	78.9	79.1
Θ_{jc} [°C/W]	0.165	0.153
$\Theta_{jc,u}$ [°C/W	0.0866	0.0858
$\Theta_{jc}/\Theta_{jc,u}$	1.91	1.78
Θ_{ca} [°C/W]	0.283	0.284
$\Theta_{ca,u}$ [°C/W]	0.278	0.278

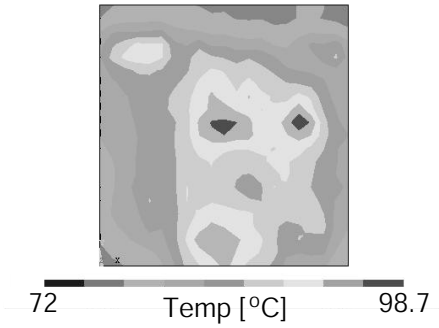
Table 3: Thermal performance comparison between BBUL and the C4 package.

grated heat spreader (IHS), heat sink, etc.] are identically utilized for both the BBUL package and the standard C4 package. To reflect the pursuits of thermal enhancement by the industry, several non-standard assumptions were made concerning the material properties and the boundary conditions in our simulation. For example, both thermal interface materials (TIM) are assumed to be 200 μm thick solder. The thermal conductivity of TIM1 is better than the TIM2 as shown in Table 3. A 30% performance gain of the heat sink is adopted to represent the numerous ongoing activities in the development of high performance heat sinks, such as heat pipe heat sink, among others [10]. While these solutions might not necessarily advance to the final products, it is evident that better thermal solutions are essential for the thermal budget of the future processors. In our model, a slightly better than natural convection is used on the surface of the printed circuit board, and the ambient temperature is assumed to be 45 °C. The junction to case thermal resistance Θ_{jc} and the case to ambient thermal resistance Θ_{ca} are typically used to characterize the overall thermal performance. The definitions are

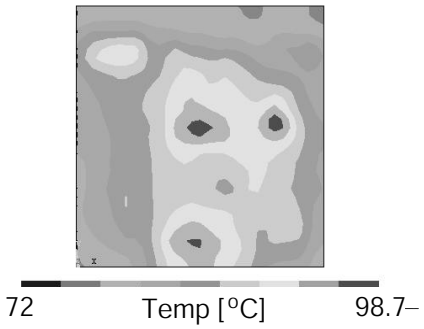
$$\Theta_{jc} = \frac{T_j - T_c}{Q} \ , \ \ \Theta_{ca} = \frac{T_c - T_a}{Q} \tag{8}$$

where Q is the total power, and T_a, T_j, and T_c are the ambient temperature, the maximum junction temperature, and the temperature at the center of the IHS, respectively. Traditionally, chip manufacturers are responsible for the Θ_{jc} and original equipment manufacturers (OEMs) or heat sink vendors provide the solution for Θ_{ca}. The two thermal resistances might not be easily separable as the power density keeps increasing. Closer cooperation between chip manufacturers and vendors is needed to address the problem at both chip level and system level.

The temperature contour maps of both packages on the front side of the die are shown in Fig. 10. The summary of results is given in Table 3. $\Theta_{jc,u}$ and $\Theta_{ca,u}$ are the junction to case and the case to ambient thermal resistances of the package with uniform heating. The maximum junction temperatures are 98.7 °C and 97.4 °C for BBUL and the C4 package, respectively, and they both appear at the hot spot with peak power density. The C4 package has slightly better thermal performance (2.5%) because the thicker ball grid array (BGA) layer can spread heat better



(a) BBUL package.



(b) C4 package.

Figure 10: Temperature contour maps on the die of the packages.

than the thin build-up layer when the DCAP regions are treated as voids in our models. From Table 3 we can also see that the Θ_{ca} of both packages with non-uniform power map is close to the packages with uniform heating, which indicates that the heat spreading in IHS is adequate. The $\Theta_{jc}/\Theta_{jc,u}$ ratio is dependent on power map and less than 2 for both packages with the power map used. Overall, the simulation shows that the thermal performance of the BBUL package is similar to that of the C4 package. As less than 5% of the thermal energy is removed through the front side of the silicon die, switching to BBUL has a minor impact on the thermal performance.

5. Mechanical attributes

Temperature excursions always occur during microprocessor use due to the turning on and off of devices. Materials with differing thermal expansion properties in intimate contact with one another will necessarily impart forces on each other. It can be expected that the BBUL package will impose relatively small forces on the surface of the die, as compared to a typical flip-chip package, during such temperature excursions. The reason for this expectation is that the relative thinness of the build-up lay-

ers, which are the only structures in contact with the die surface, means that forces which are small in magnitude will generate large deformations in the layers. Preliminary finite element modeling has shown that the shear stresses and shear plastic strains caused in vias on the die surface are smaller when using BBUL than for a flip-chip package, in some cases by more than a factor of two. However, it is possible that the stress concentrations due to the two packaging schemes will be different, and may not follow this trend; this remains to be investigated. A detailed discussion of the mechanical analysis of a BBUL package will be presented elsewhere.

6. Conclusions

We have described the BBUL packaging technology and some of its conceptual, process, routing, electrical, thermal and mechanical characteristics. Clear benefits for the problems of escape routing and power delivery have been identified and demonstrated. Thermally, the BBUL package performs similarly to existing technologies but is expected to be compatible with innovative thermal solutions. Furthermore, BBUL should impose a reduced level of thermomechanical stresses onto the active die surface and, thus, support the introduction of on-die dielectrics that are sensitive to such stresses.

Acknowledgments

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