EL 303 ANALOG INTEGRATED CIRCUITS
Design Homework Assignment 5:
Active-Filter Tuned Oscillator

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1) INTRODCUTION

The aim of this project is designing a signal waveform generator with the following specifications:

- The centre frequency shouldn't be lower than 10 kHz.
- The filter quality factor shouldn't be lower than 4

1.1 General Information

To create a sinusoidal basically a circuit that uses a positive feedback using an amplifier and a frequency selective circuit using R, C and L elements are used. The amplitude of the wave is limited by adding diodes by the limits of the amplifier. These kinds of circuits are called linear oscillators.

On the other hand some circuits create triangular waves and shape them into sinus dials by using diodes. These kinds of circuits are called non-linear oscillators.

1.2 Requirements for Oscillation

The requirement of the oscillation condition has two steps. In first the linear part of the equitation is examined, and in the second the non-linear part is examined.

1.2.1 Oscillator Feedback Loop

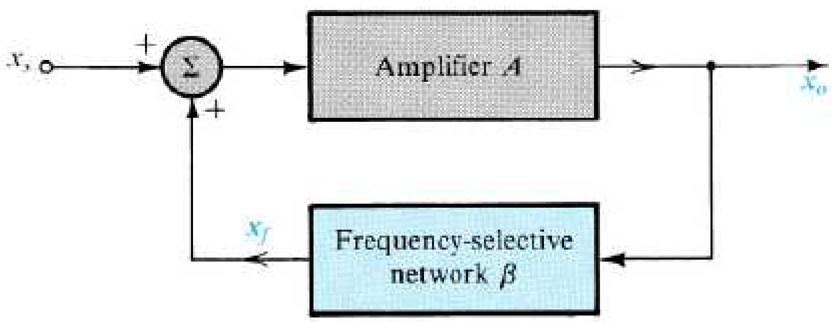

Figure 1: Black box of a sinusoidal oscillator.

The basic structure includes a frequency selective network connected to an amplifier by positive feedback. The closed loop gain is:

$$A_f(s) = \frac{A(s)}{1 - A(s)\beta(s)}$$

In which:

$$L(s) \equiv A(s)\beta(s)$$

Thus:

$$1 - L(s) = 0$$

1.2.2 Oscillation Criterion

At the selected frequency the gain o the closed loop network must 1, giving the equation:

$$L(j\omega_0) \equiv A(j\omega_0)\beta(j\omega_0) = 1$$

Which means in addition to closed loop gain's being 1, the closed loop phase should be 0 at the selected frequency fo. At the other frequencies due to the phase shift complex signals will occur. This is called Barkhausen Criterion. From these conditions it is derived that:

$$A\beta = 1$$

It is also observable that the frequency (fo) is determined by the phase condition only.

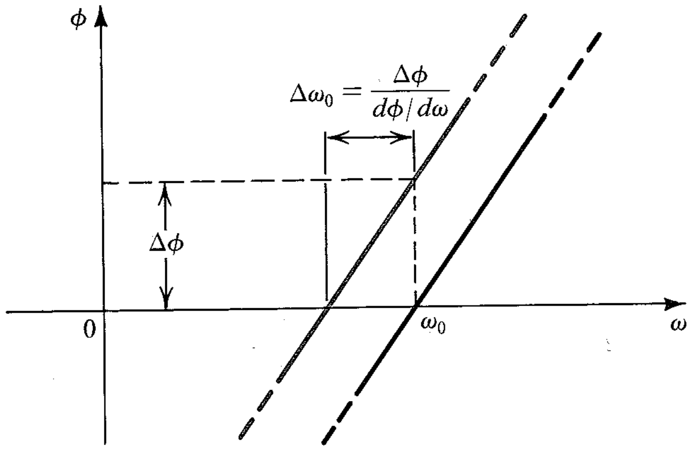

Figure 2: Dependence of the frequency on the slope of the phase response.

1.2.3 Active Filter Tuned Oscillator

Basically the circuit is made up of band-pass filter connected with a positive loop gain and limiters. A square wave generated by the limiters is given into the band-pass filter which gives out a sinusoidal wave at its fundamental frequency. Also the quality factor of the filter determines the purity of the sinusoidal wave.

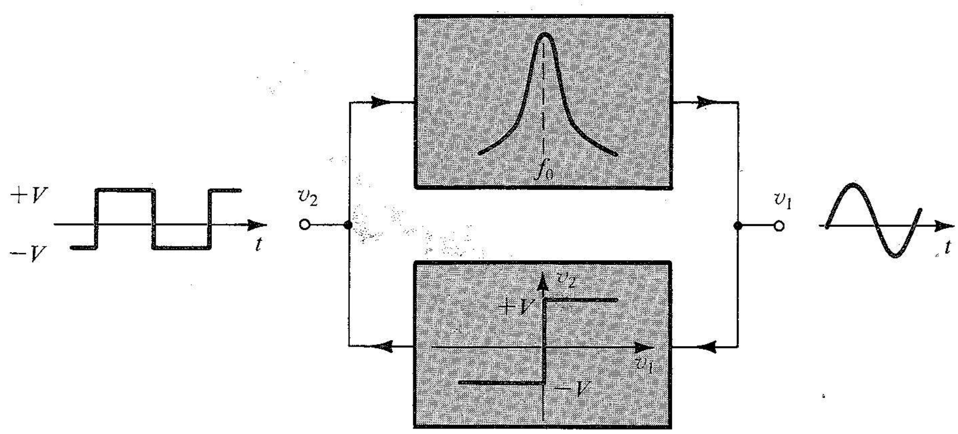

Figure 3: Black box diagram of an active-filter-tuned oscillator

2) DESIGN

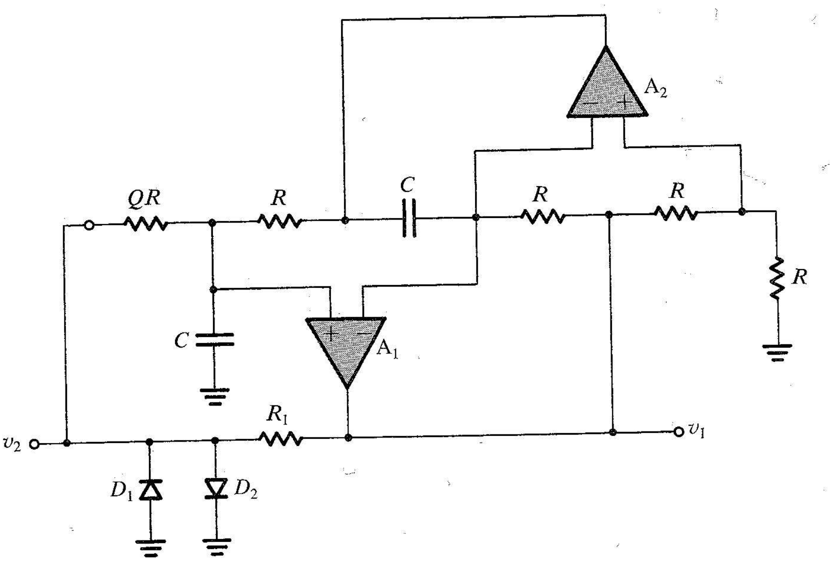

Figure 4: Simple implementation of the circuit

In which the band-pass filter is constructed as:

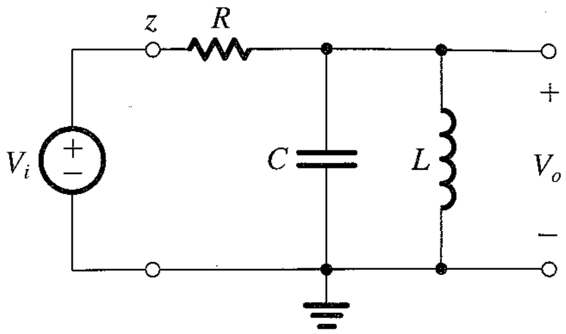

Figure 5: Band-pass filter

Also instead of the inductor, Antoniou inductance-simulation circuit is used:

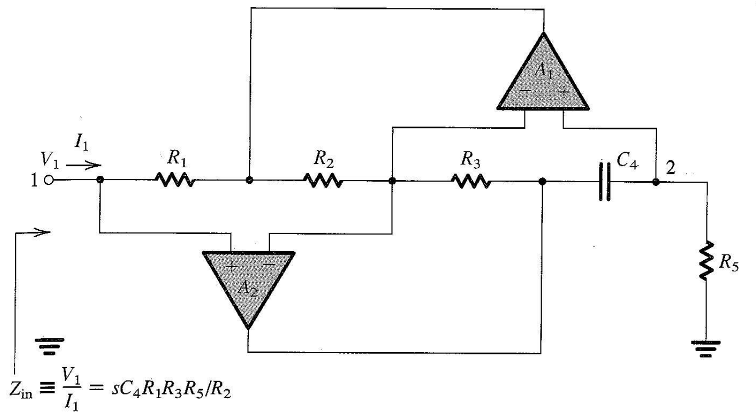

Figure 6: Antoniou Inductance-Simulation Circuit

From Antoniou inductance-simulation circuit the band-pass frequency is given by:

$$\omega_0 = 1/\sqrt{LC_6} = 1/\sqrt{C_4C_6R_1R_3R_5/R_2}$$

$$Q = \omega_0 C_6 R_6 = R_6\sqrt{\frac{C_6}{C_4}\frac{R_2}{R_1R_3R_5}}$$

Which can be simplified when taking R1=R2=R3=R5=R and C4=C6=C into:

$$\omega_0 = 1/CR$$

$$Q = R_6/R$$

Also the diodes are designed using BJT's.

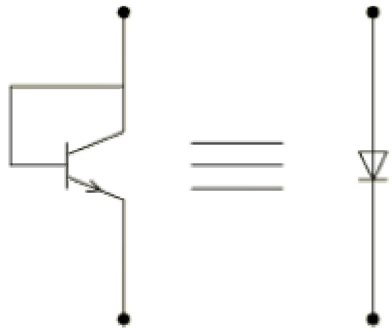

Figure 7: Realization of a diode using BJT

3) CADENCE SCHEMATIC LEVEL DESIGN AND SIMULATIONS

3.1 Schematic Level Design

The circuit is constructed as described above. And inserting values below:

C= 8pF
R= 1kΩ
QR= 15kΩ

The expected results are:

Wo= 19.89Mhz
Qfactor= 15

Achieved values:

Wo= 16.6Mhz (frequency of the output signal)
Wo= 17.51Mhz (peak of the band-pass filter)
Qfactor= 8.22

The difference between the expected values and the calculated values are due to the op-amp's being non-ideal. The specs for the op-amps are reasserted by using voltage controlled voltage sources and it has been seen that the main requirements were the 0dc input and output voltage. Also gain of the op-amp was important, effecting clipping of the output and ac response of the band-pass filter.

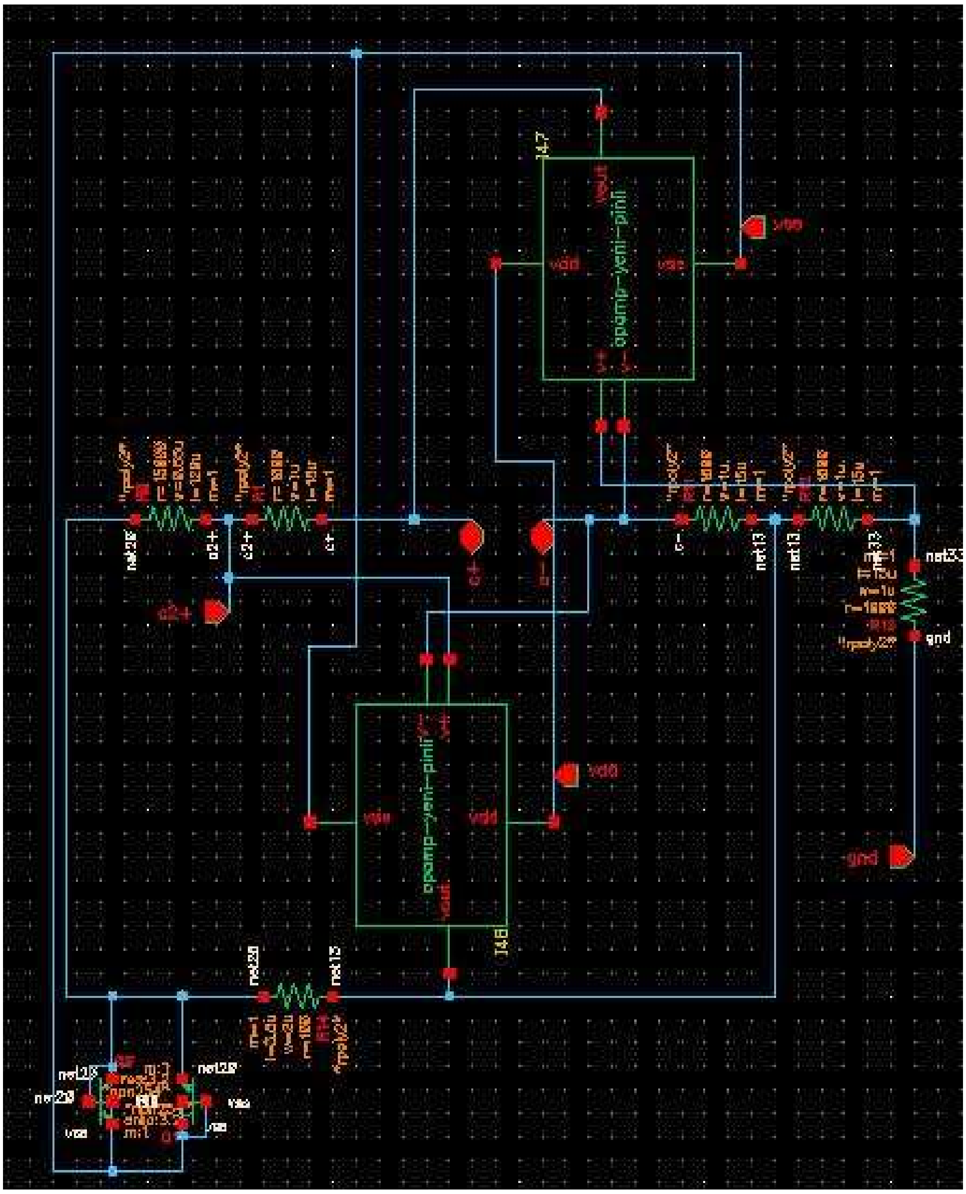

Figure 8: Schematic of the wave generator

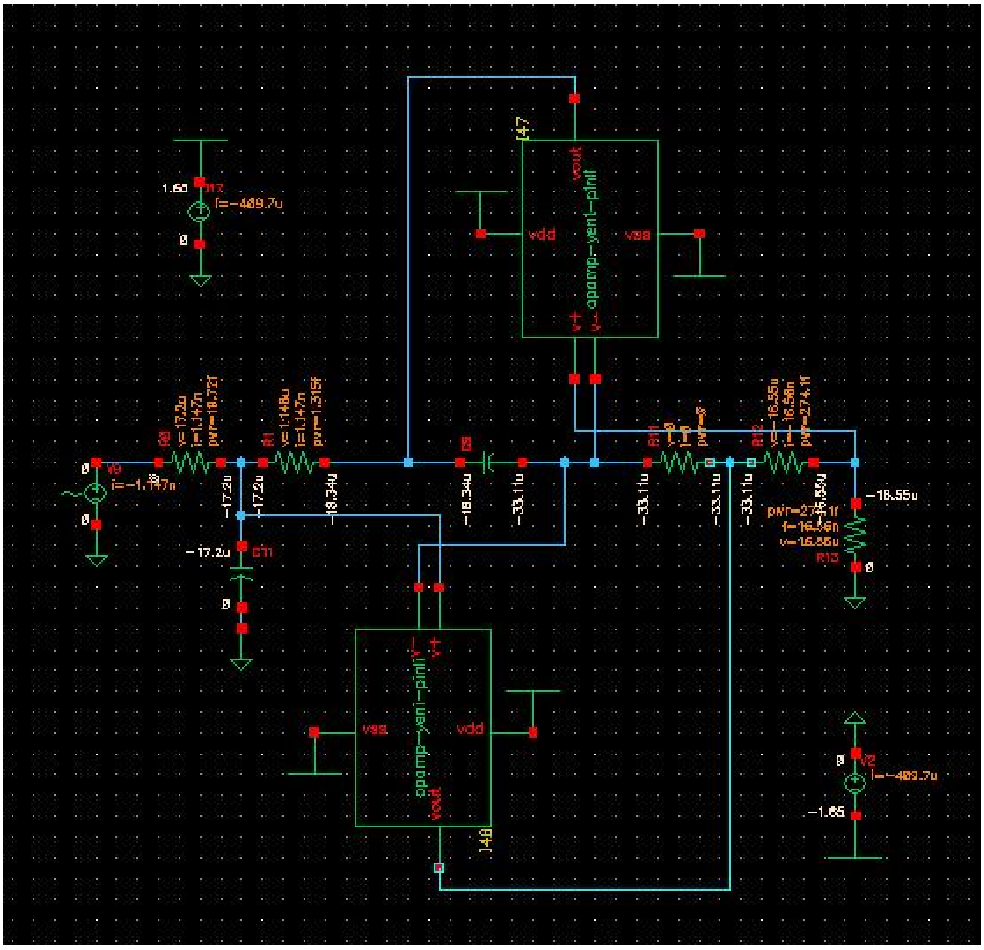

Figure 9: Realization of the band-pass filter

3.2 Schematic Level Simulations

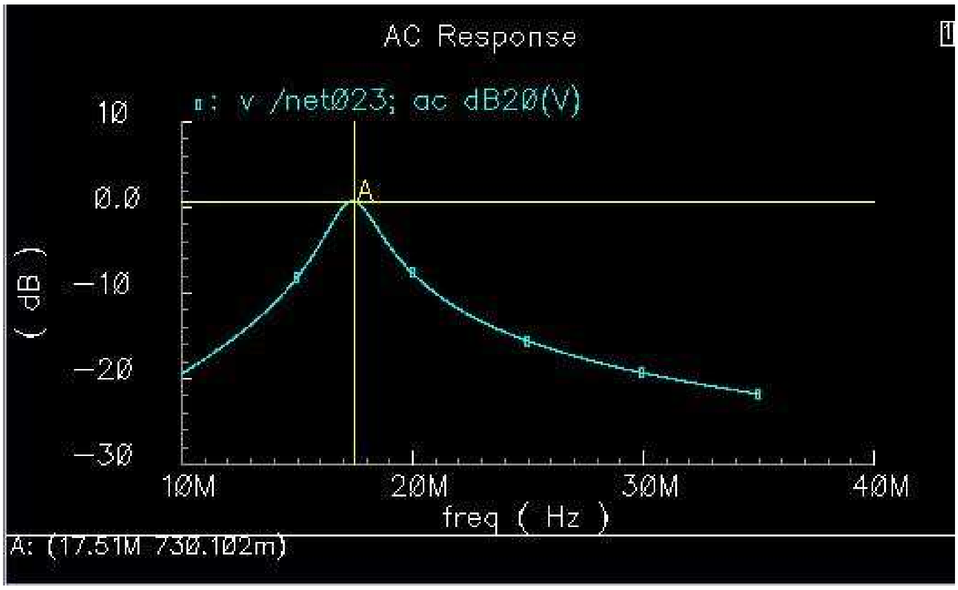

Figure 10: fundamental frequency of the filter

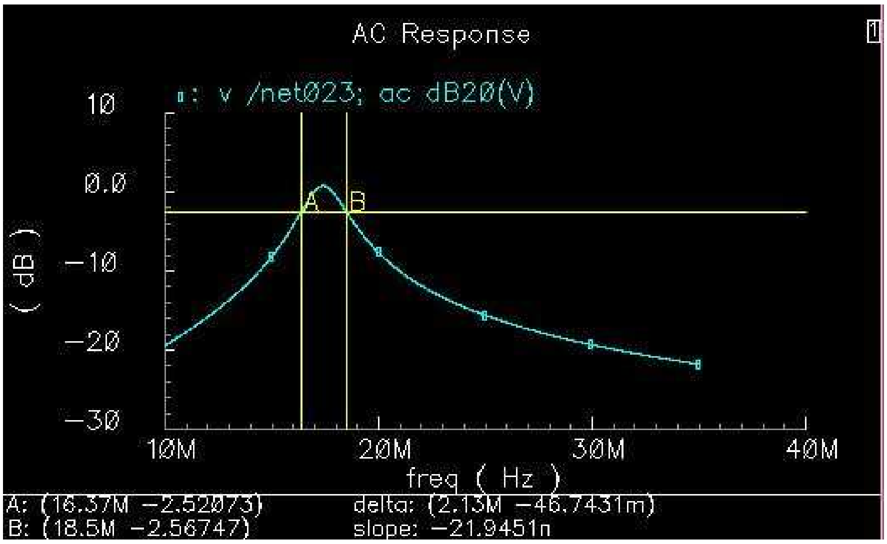

Figure 11: Q-factor of the filter

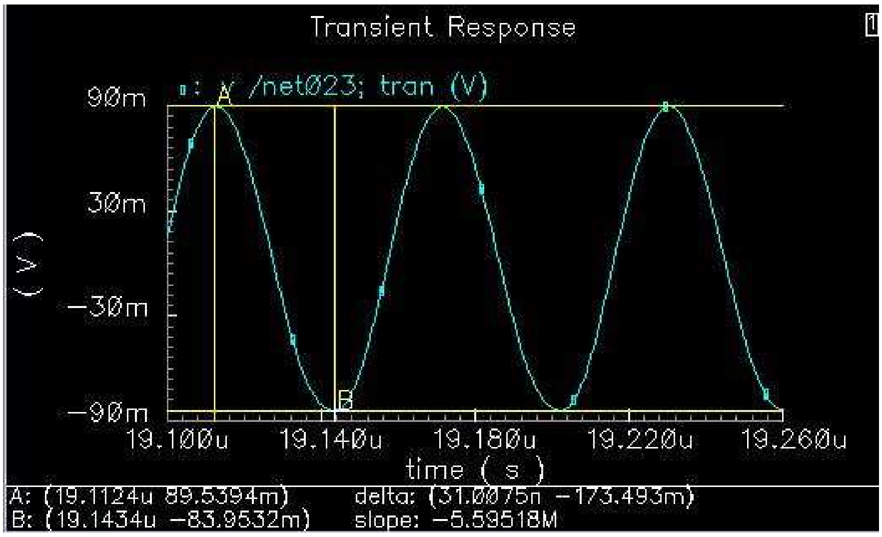

Figure 12: amplitude of the generated sinusoidal

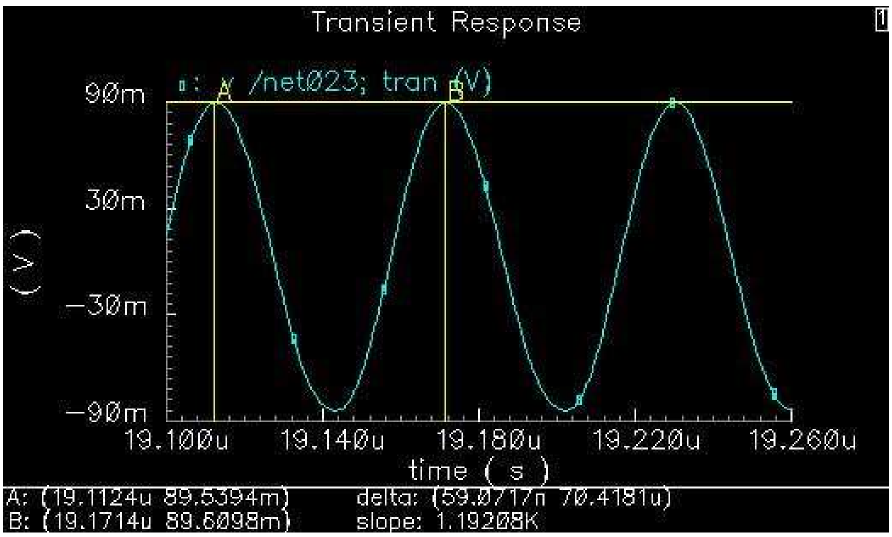

Figure 13: frequency of the generated signal

4) CADENCE LAYOUT LEVEL DESIGN AND SIMULATIONS

4.1 Layout Design

First the layout of the op-amp is drawn separately and checked after that the whole circuit brought together and drawn. The hardest challenge was with the diodes or to say the bjts operating as diodes, unlike nmos or pmos the body of the bjts are connected automatically to the lowest voltage value. This caused numerous LVS mismatches. Since initially the body was directly connected to emitter or collector relatively and by this “gnd” and “vss” crossed, causing the mismatches.

After the post-layout simulations it occurred that the signal was experiencing clipping on the lower arm. To correct that, capacitances have been increased; however as with this increase caused decrease in the fundamental frequency, increase in the area of the IC (not important since it is given outside), and also decrease in the amplitude of the signal. The decrease in the amplitude of the signal is the factor that disables the clipping. Further increasing the capacitor causes the signal to diminish as time passes. Also the total are of the design is 46 to 54.

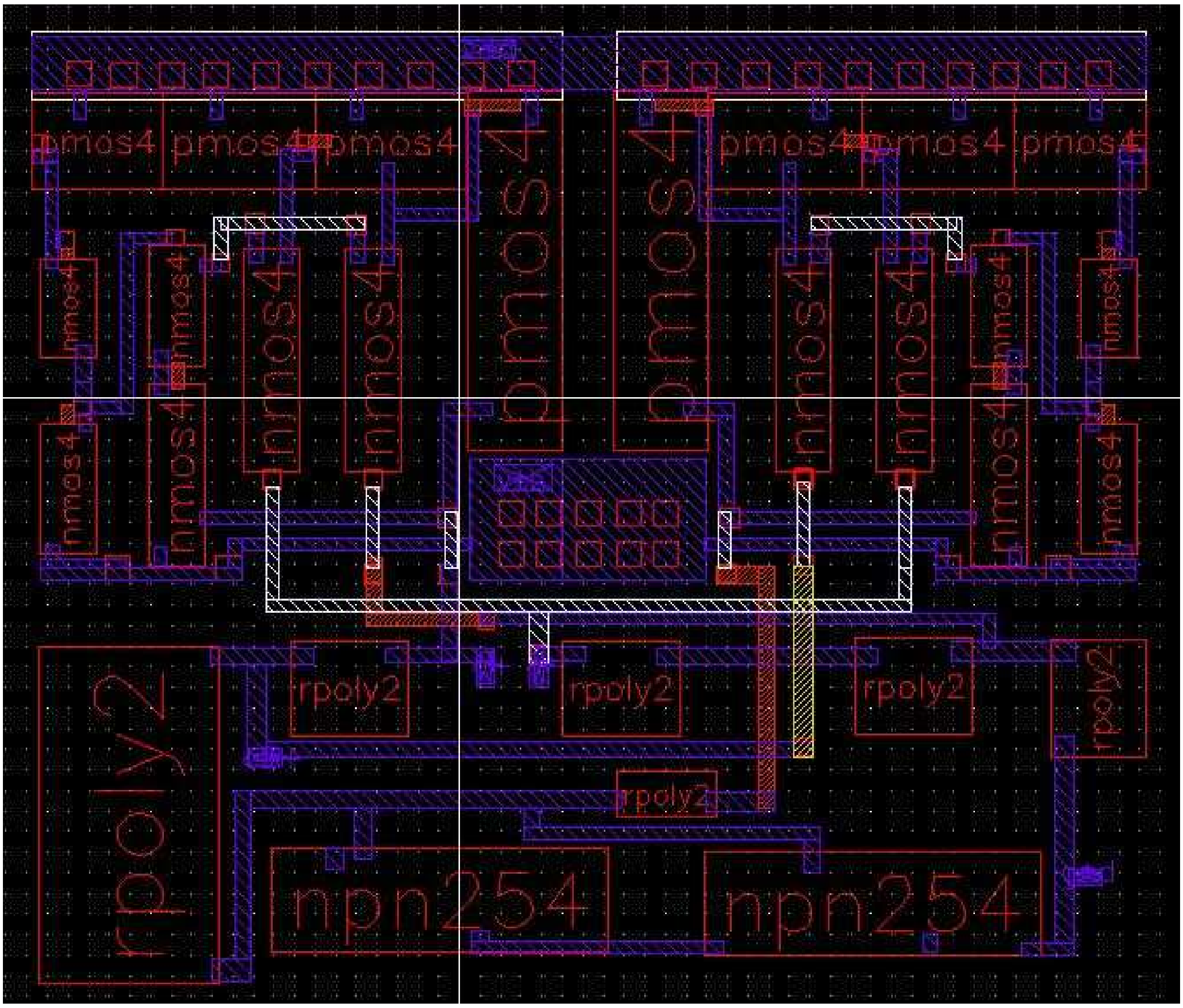

Figure 14: Layout of the overall design, with capacitors implanted from outside

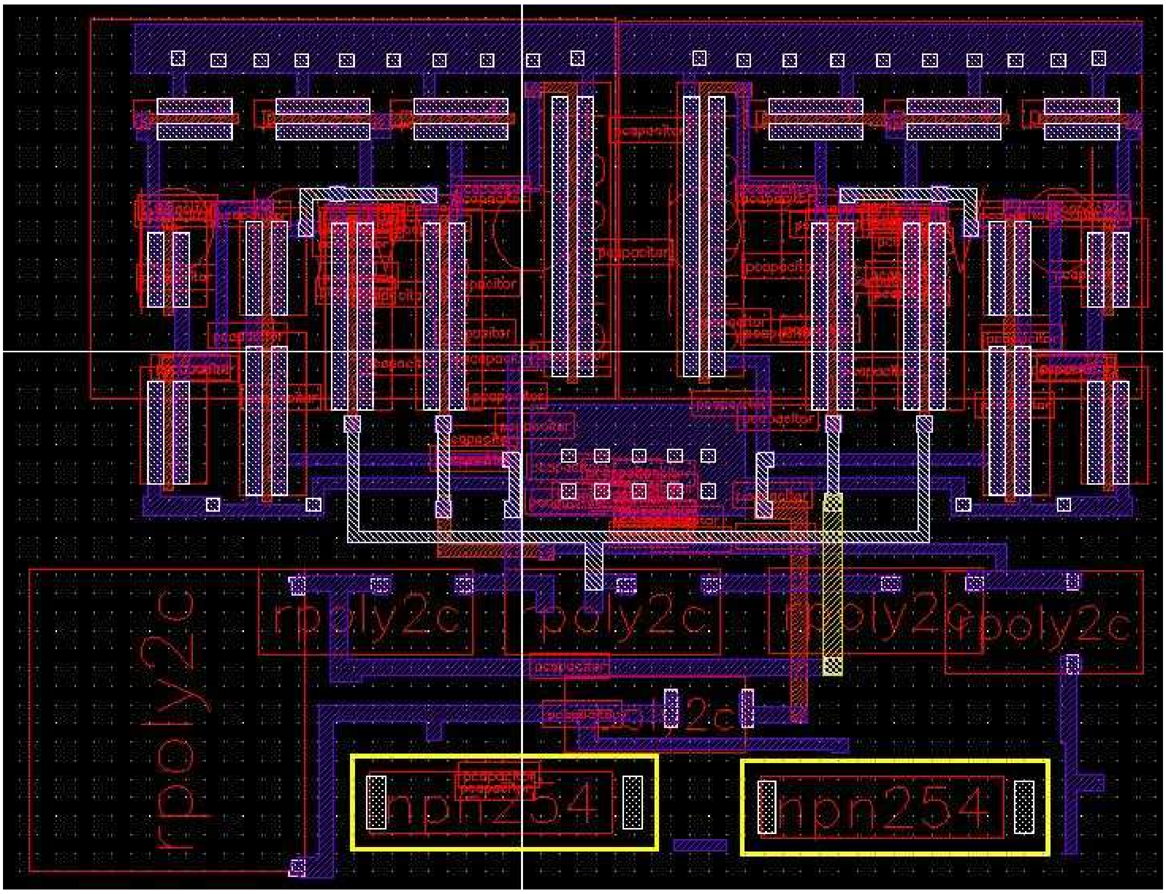

Figure 15: Extracted view of the overall design.

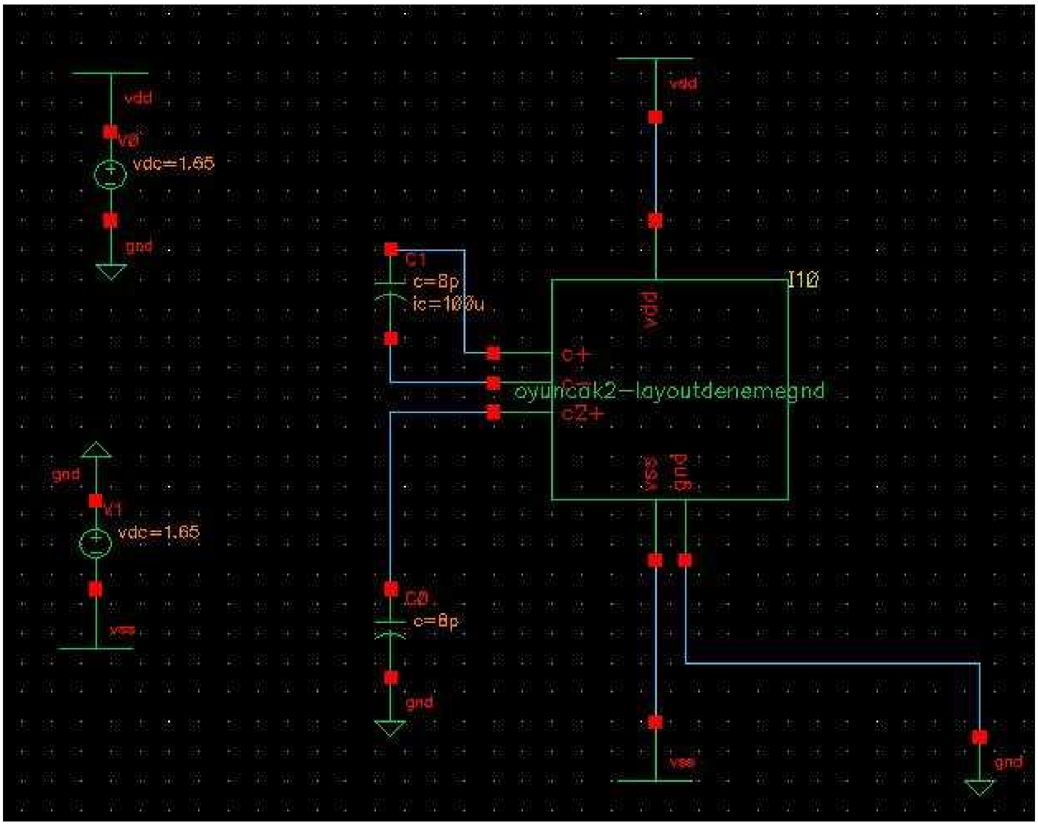

Figure 16: Overall design with 8pF capacitors

4.2 Layout Simulations

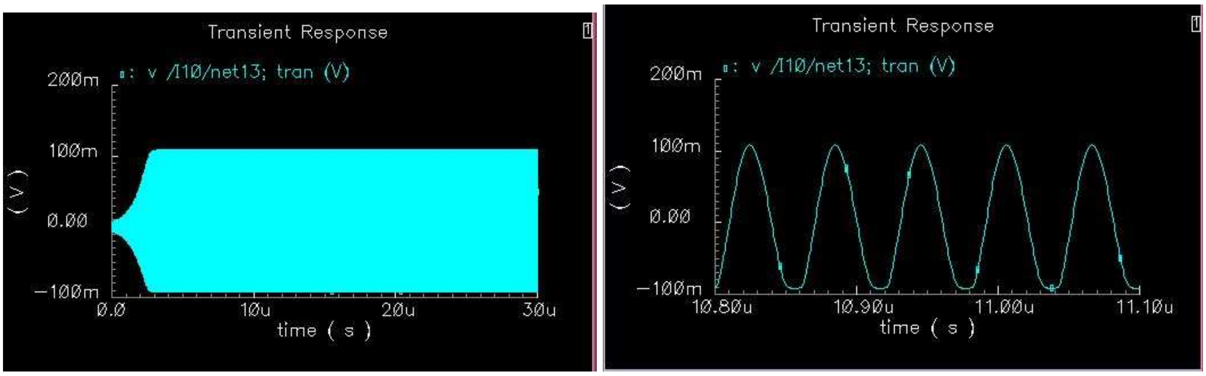

Figure 17: a) Output signal received with the layout b) Detail to show clipping

4.3 Post-Layout Design

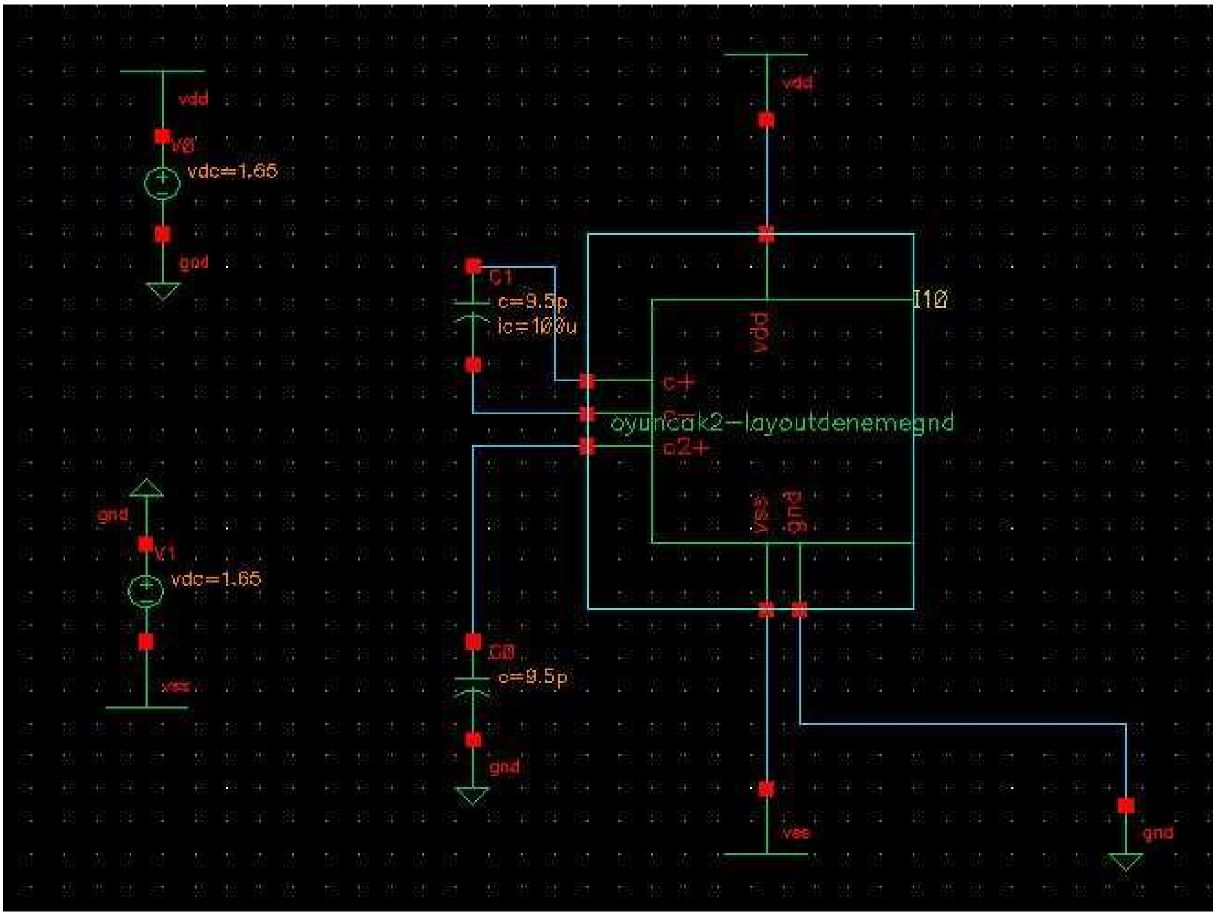

Figure 18: Overall circuit with 9.5pF capacitors.

4.4 Post-Layout Simulations

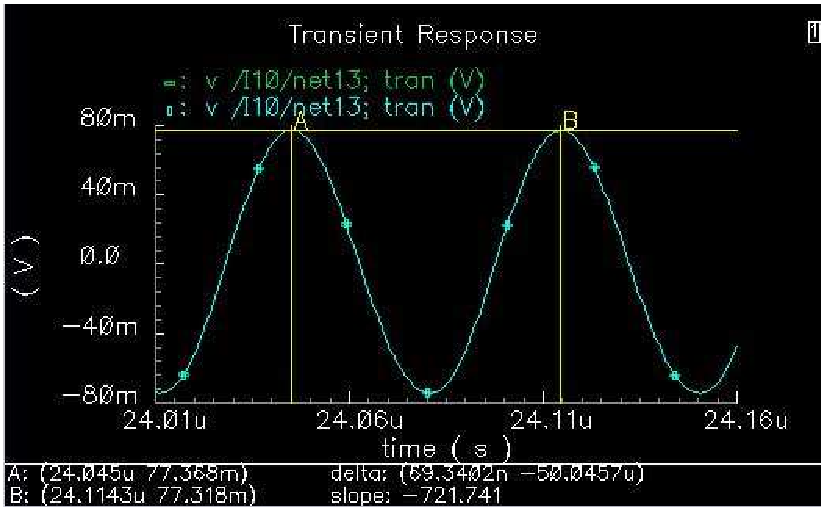

Figure 19: Output of the design after post-layout

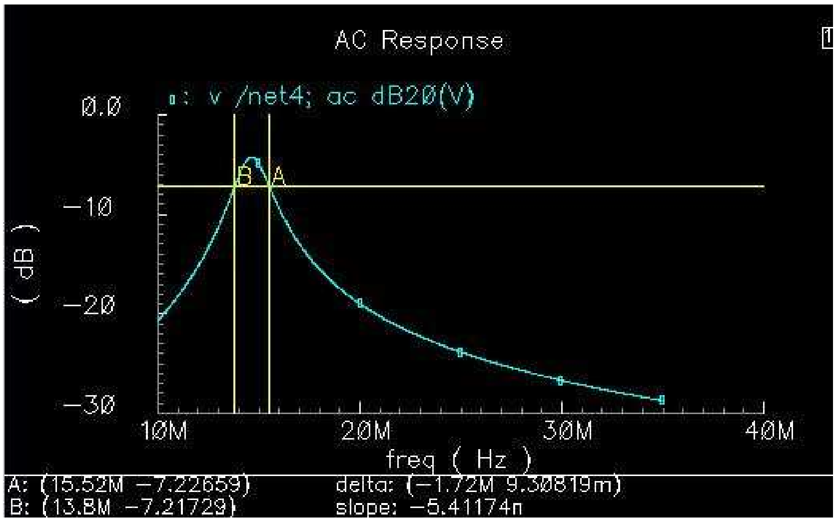

Figure 20: Q-factor after post-layout

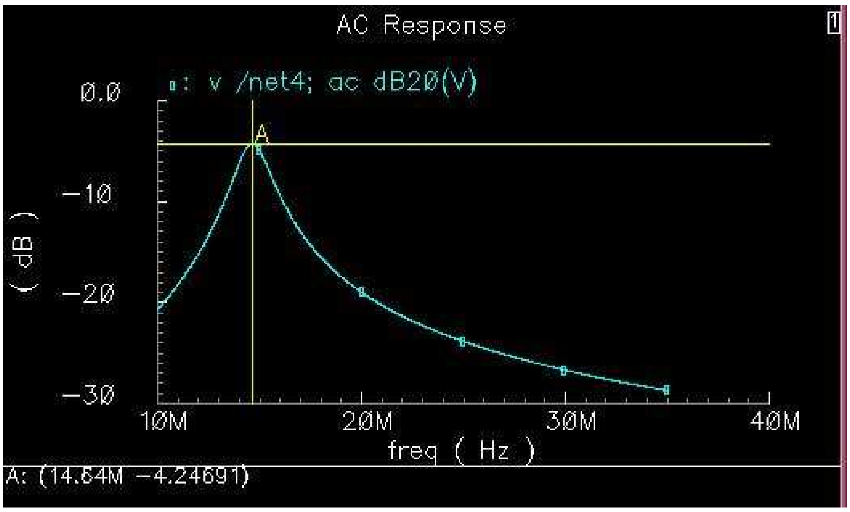

Figure 21: Wo after post-layout

5) CONCLUSION

It is observable that the due to the increase in capacitances, fundamental frequency with respect to band-pass filter has become 14.64 Mhz. Also Q-factor has become 8.511. The frequency of the signal is calculated as 14.49 MHz.

Moreover comparing the amplitudes of the both signals that are received after the layout simulations show that with the increase of the capacitances the amplitude decreases causing the avoidance of clipping.

As a conclusion the required specifications are achieved with an expected difference from the initial values, where the last output is a sinusoidal with 14.49 MHz frequency and a band-pass filter with a peak at14.64 MHz, and a quality factor of 8.511.