Session – 3

Session Name: Feng's and Handler's Classification

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Subject/Course: Advanced Computer Architecture

Session Objectives

At the end of this session, the learner will be able to:

- Recall the criteria for various architectural classifications.
- Describe average parallelism and processor utilization.
- Explain Feng's classification of computer architecture.
- Discuss Handler's classification criteria.
- Illustrate the characterization of a computer using Handler's triplet.

Teaching Learning Material

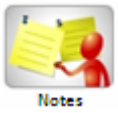
- White Board and Markers

Session Plan

Time (in min)	Content	Learning Aid and Methodology	Faculty Approach	Typical Student Activity	Skill and Competency Developed
05	Review of Criteria for Various Architectural Classifications	Quiz	Questions Facilitates	Answers Participates	Remembering Intrapersonal Linguistic
10	Average Parallelism and Processor Utilization	Board	Explains	Listens Writes	Remembering Understanding Intrapersonal Mathematical-Logical
25	Feng's Classification	Board Role play	Explains Facilitates Monitors	Listens Participates	Remembering Understanding Intrapersonal Logical
15	Handler's Classification	Board	Explains	Listens Writes	Remembering Understanding Intrapersonal Mathematical-Logical
05	Conclusion and Summary	Key words	Lists Facilitates	Recalls	Remembering Understanding Intrapersonal Linguistic

Session Inputs

Review of Criteria for Various Architectural Classifications



As the learners are already familiar with the criteria for architectural classification, we can conduct a quiz to help them recall the same.

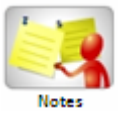
Suggested Activity: Quiz

A quiz can be conducted by posing short questions like:

1. What is the need for classification?
2. What is basis for Flynn's classification?
3. What is basis for Feng's classification?
4. What is basis for Handler's classification?

Responses from the learners can be listed on the board and the topic can be revised.

Average Parallelism and Processor Utilization



Now that we have reviewed the criteria for various architectural classifications, we can look into average parallelism and processor utilization.

If a processor is processing P bits in unit time, then P is called the maximum degree of parallelism.
Let i= 1, 2, 3, ..., T be the different timing instants and P1, P2, ..., PT be the corresponding bits processed.
Then,

Average parallelism, Pa = (P1 + P2 + ...PT) / T

Processor Utilization, U= Pa/P

The maximum degree of parallelism depends on the structure of the Arithmetic and Logic Unit. Higher degree of parallelism indicates a highly parallel ALU or processing element.
Average parallelism depends on both the hardware and the software. Higher average parallelism can be achieved through concurrent programs.

Feng's Classification

Through a role play, we can demonstrate Feng's classfication of computer architecture.

Suggested Activity: Role Play

The learners can be asked to sit in proper alignment as rows and columns. For example, 4 rows and 3 columns. The columns represent individual bits in memory. The rows represent a memory word. Clocks can be indicated by a tick sound produced by the instructor. Each learner can indicate bit processing by clapping over the head.

Each square below represents a learner and the number in the square indicates the clapping sequence. Clapping is done in the specified sequence at the tick of the clock. At the first tick, all learners representing 1 shall clap. At the second tick, all learners representing 2 shall clap. So on and so forth.

For WSBS

3	2	1
6	5	4
9	8	7
12	11	10

For WSBP

1	1	1
2	2	2
3	3	3
4	4	4

For WPBS

3	2	1
3	2	1
3	2	1
3	2	1

For WPBP

1	1	1
1	1	1
1	1	1
1	1	1

With the above activity, learners would have understood the differences in processing in each of the four classes as identified by Feng's classification. It would now be appropriate to share the formal description of the same.

According to Feng's classification, computer architecture can be classified into four. The classification is based on the way contents stored in memory are processed. The contents can be either data or instructions.

- Word Serial Bit Serial (WSBS)

One bit of one selected word is processed at a time. This represents serial processing and needs maximum processing time.

- Word Serial Bit Parallel (WSBP)

All bits of a selected word are processed at a time. Bit parallel means all bits of a word.

- Word Parallel Bit Serial (WPBS)

One bit from all words are processed at a time. Word parallel signifies selection of all words.

- Word Parallel Bit Parallel (WPBP)

All bits of all words are processed at a time. Maximum parallelism is achieved here.

Handler's Classification

With Flynn's and Feng's classifications covered, we can now move on to Handler's classification.

Handler's classification is based on the concept of parallelism and pipelining. Here, we check the degree of pipelining and parallelism implemented in the hardware structure of the computer.

Handler considered parallel pipeline processing at three sub-system levels.

- Processor control unit (PCU)
- Arithmetic logic unit (ALU)
- Bit level circuit (BLC)

Here, PCU is the control unit for controlling one processor, ALU represents one processing element and BLC is the combinational circuit needed to process one bit.

The parallelism in a system can be explained using a triplet containing six independent entities, as defined below.

A computer C can be characterized by

T(C) = < K X K' ; D x D' ; W x W' >

where,

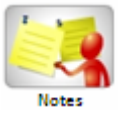
K = the number of processor control units within the computer.
D = the number of ALU or processing elements under the control of one PCU.
W = the word length of ALU or PE
K' = the number of PCUs that can be pipelined.
D' = the number of ALUs that can be pipelined.
W'= the number of pipelined stages on all ALUs or in a single PE.

Example: TI-ASC has one controller controlling four arithmetic units. Each ALU is an eight stage pipeline with 64-bit word length.

It can be represented using Handler's equation as:

T(TI-ASC)= <1 X1 ; 4 X 1; 64 X 8 >

Conclusion



We can conclude the session by conducting a key words activity.

Suggested Activity: Key Words

The following key words can be spoken out by the faculty and the learners can be asked to explain each of them.

The keywords would be:

- Architectural classification
- Average parallelism
- Processor utilization
- WSBS
- WSBP
- WPBS
- WPBP
- Handler's classification
- PCU
- Processing element
- Word length

Summary

In this session, we learnt to:

- Recall the criteria for various architectural classifications.
- Describe average parallelism and processor utilization.
- Explain Feng's classification of computer architecture.
  - WSBS
  - WSBP
  - WPBS
  - WPBP
- Discuss Handler's classification criteria.
  - PCU
  - ALU
  - BLC
- Illustrate the characterization of a computer using Handler's triplet.

Assignment

1. The CDC 6600 has a single main processor supported by 10 I/O processors. Each control unit controls one ALU with a 60-bit word length. The ALU has 10 functional units which can be formed into a pipeline. The 10 peripheral I/O processors may work in parallel with each other and with the CPU. Each I/O processor contains one 12-bit ALU. Arrive at the Handler's triplet describing the I/O processor as well as the main processor.

References

- Parallel Processing : Kai Hwang and Briggs
- Introduction to parallel processing : Kai Hwang