Double Patterning with Resist Freezing Process

M. Hori, T. Nagai, A. Nakamura, T. Abe, G. Wakamatsu, T. Kakizawa, Y. Anno, M. Sugiura, S. Kusumoto, Y. Yamaguchi, T. Shimokawa, M. Slezak

Semiconductor Materials Laboratory, JSR Corporation

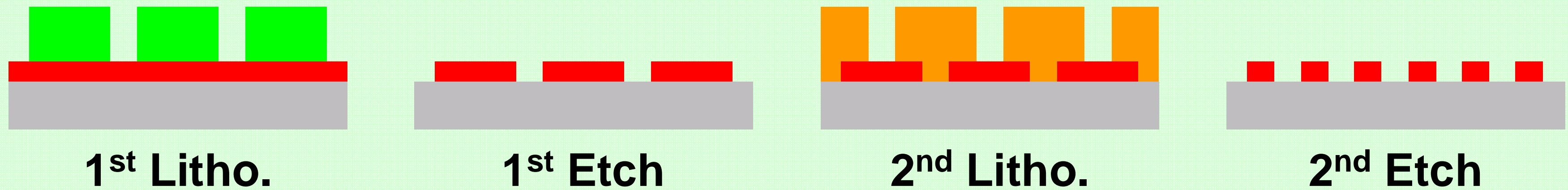
JSR SEMICONDUCTOR MATERIALS LABORATORY JSR

Contents

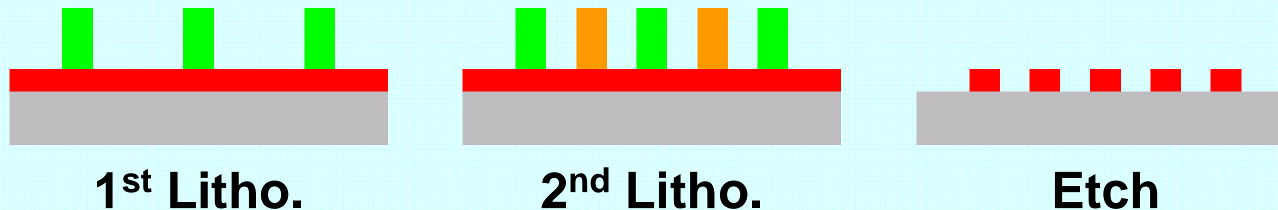
- ***Background***
  - ✓ **Various Double Patterning Techniques**
  - ✓ **Double Patterning Process with Resist "Freezing"**
- ***Lithographic performance of JSR Freezing Process***
  - ✓ **32nm LS formation and Etching Result**
  - ✓ **"Freezing" Process for 2D Logic Patterning**
  - ✓ **CH Formation by "Freezing" Process**
- ***Summary***

Various Double Patterning Techniques

Litho-Etch-Litho-Etch process: Dual-Etch

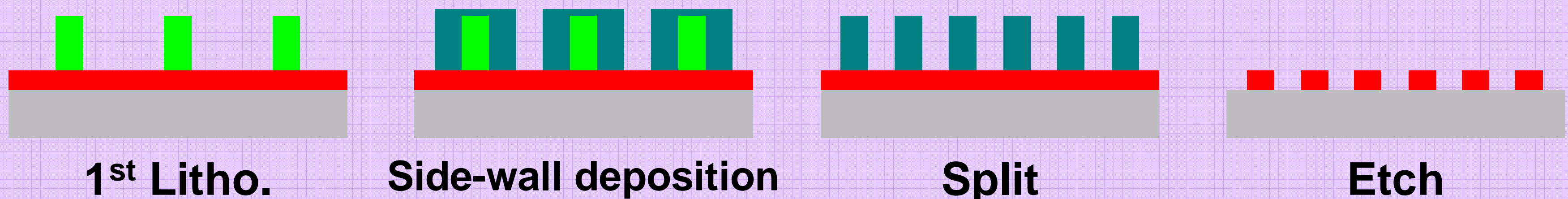


Litho-Litho-Etch process: Single-Etch



Less processes

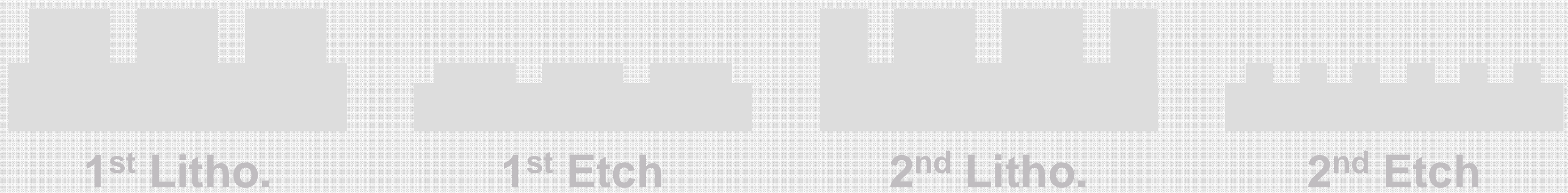
Side Wall process: Multiple Split and Etch



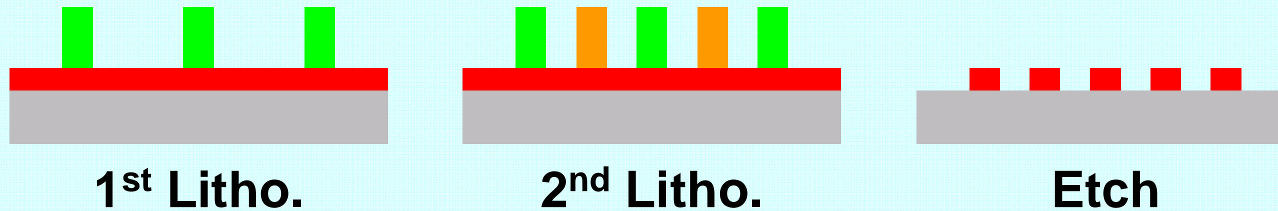
Higher throughput is enabled by Litho-Litho-Etch process.

Various Double Patterning Techniques

Litho-Etch-Litho-Etch process: Dual-Etch

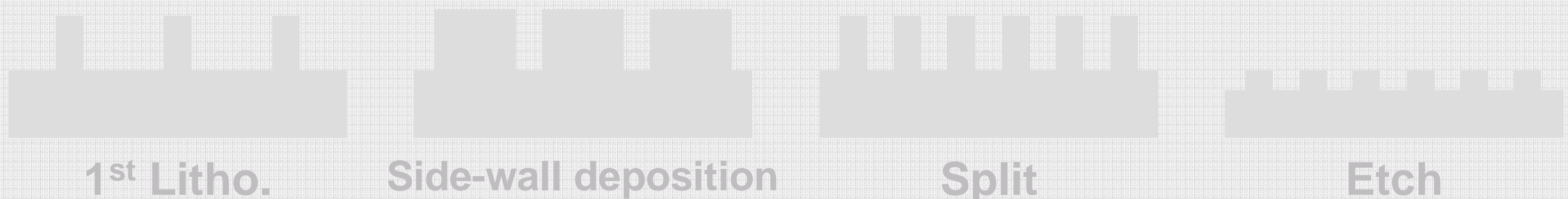


Litho-Litho-Etch process: Single-Etch



Less processes

Side Wall process: Single-Etch

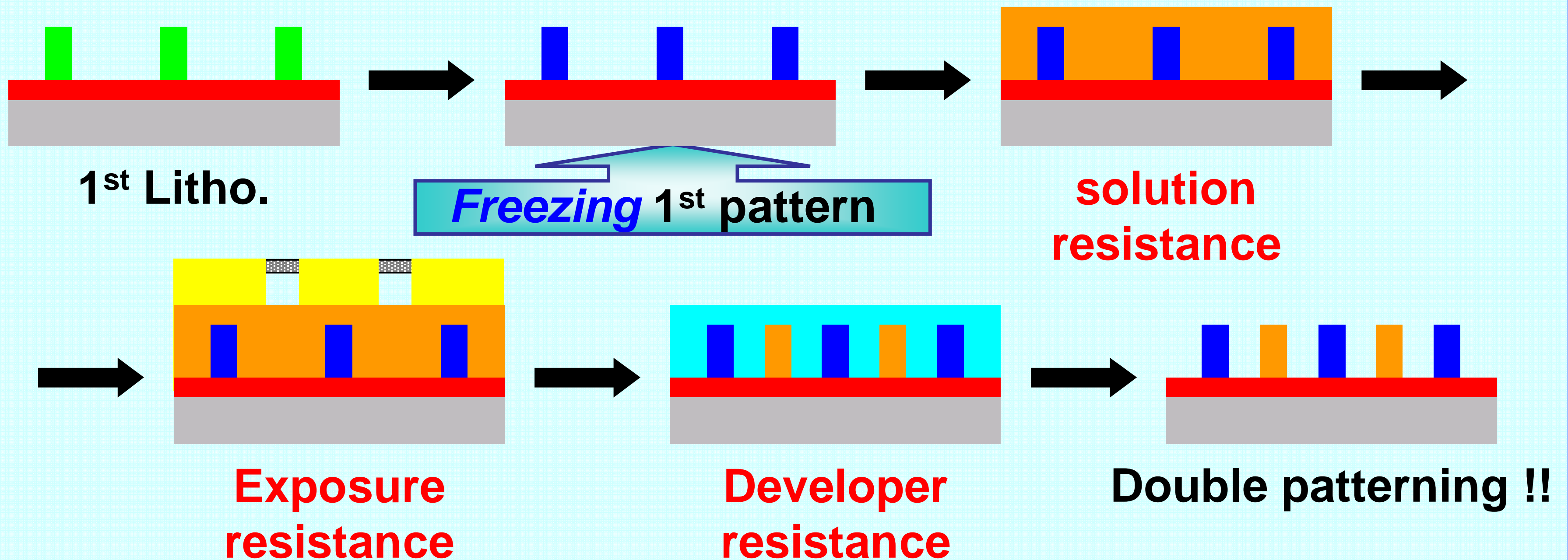


Higher throughput is enabled by Litho-Litho-Etch process.

Why "Freezing" Process is Required?

✓ ***New technique that protect 1st pattern must be required.***

➡ ***Development of "Freezing" process: Litho-Freezing-Litho-Etch***

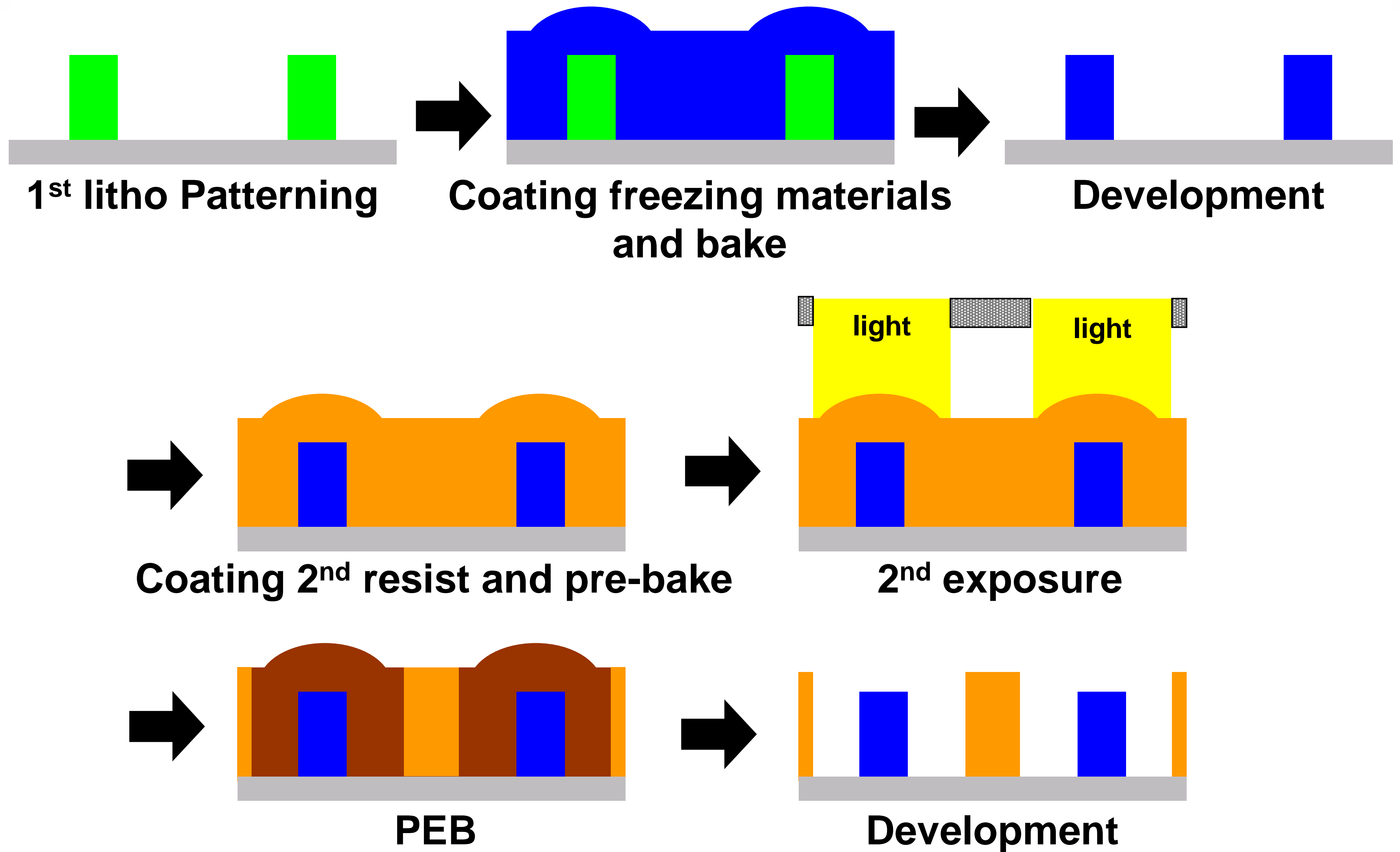


Freezing process provides multiple resistances to 1st pattern.

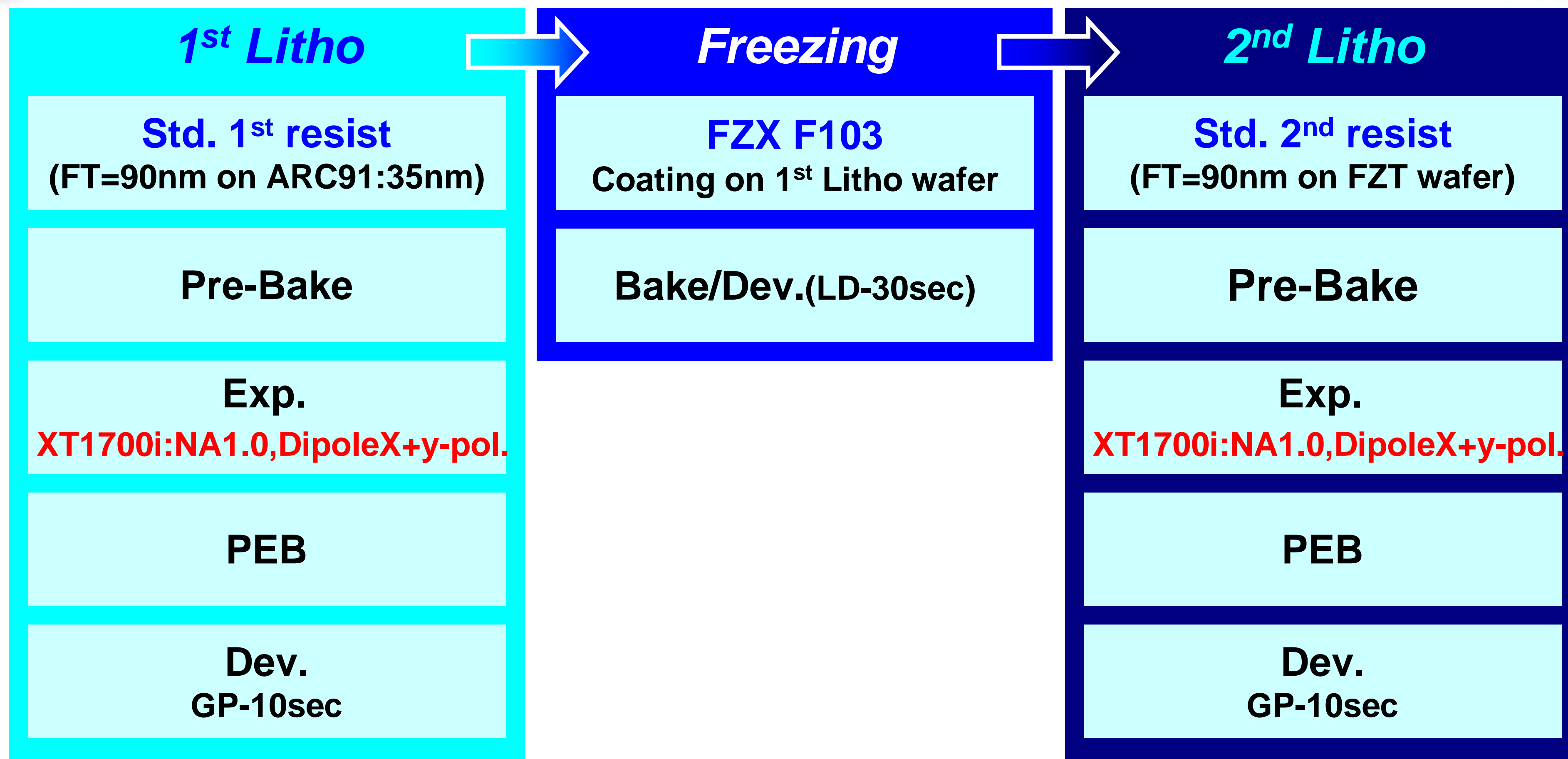
Contents

- ***Background***
  - ✓ Approaching Optical Limit
  - ✓ Double Patterning Process with Resist "Freezing"
- ***Lithographic performance of JSR Freezing Process***
  - ✓ **32nm LS formation and Etching Result**
  - ✓ "Freezing" Process for 2D Logic Patterning
  - ✓ CH Formation by "Freezing" Process
- ***Summary***

Process Flow of "Freezing" Process



Experimental Condition

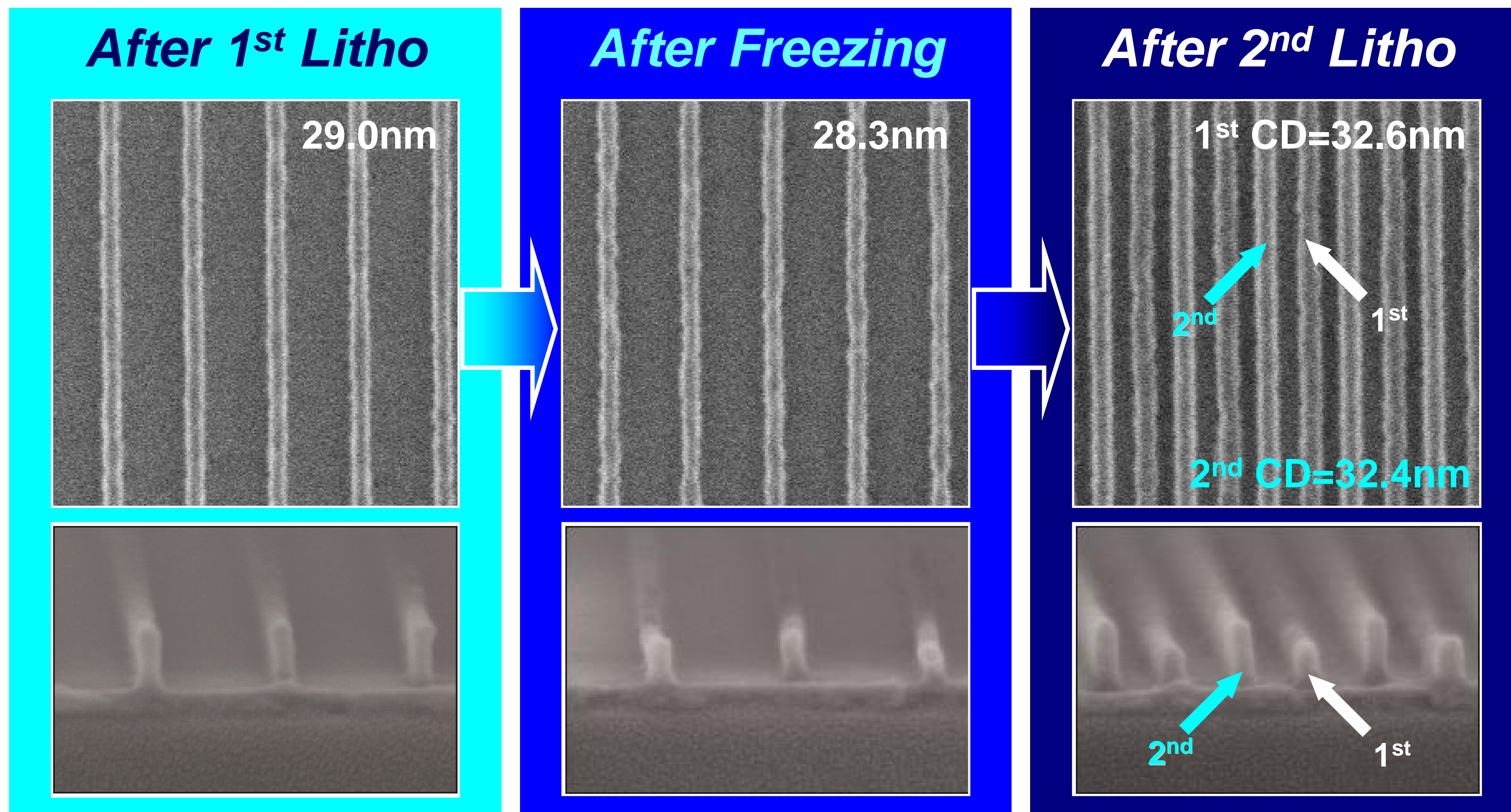


Tool: **CLEAN TRACK LITHIUS i (TEL)** for coating resist/freezing materials

XT1700i (ASML) for exposing

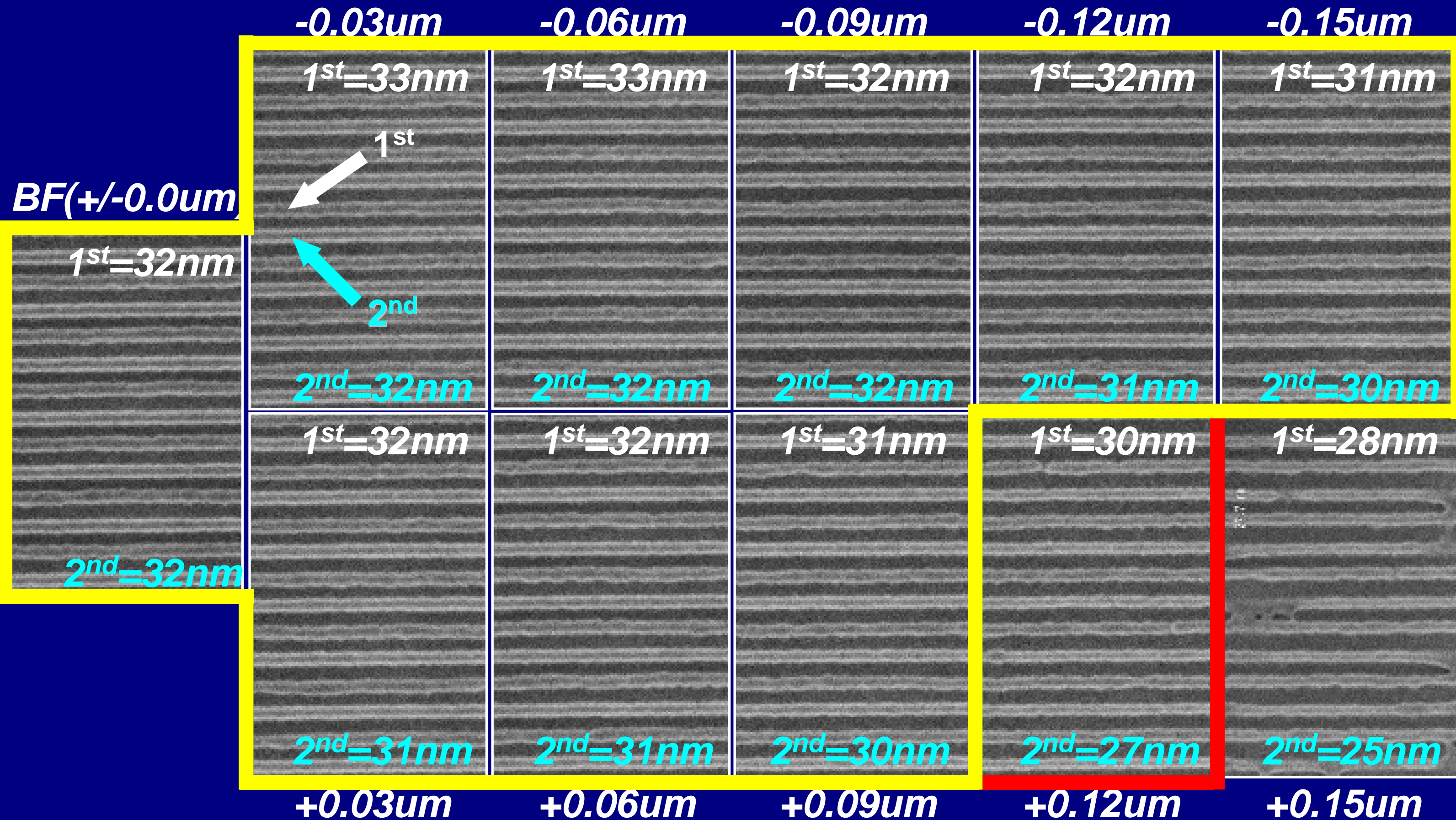
S-9380/S-5500 (Hitachi) for top-down/X-section SEM imaging

Formation of 32nmLS Pattern



➢ *Formation of 32nmLS double patterning was succeeded.*

Common DOF after 2nd Litho

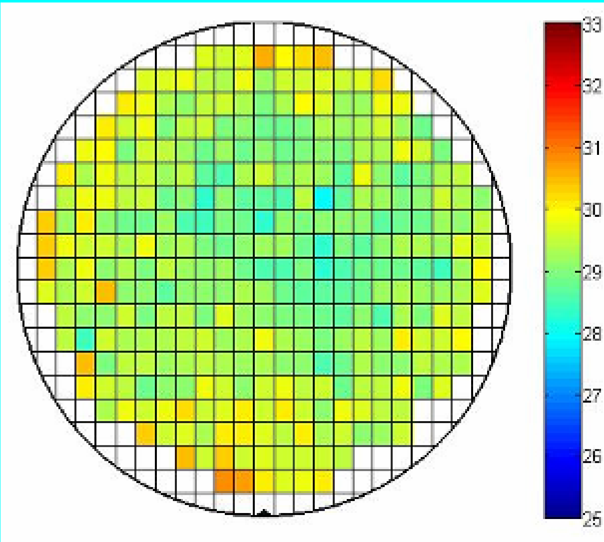


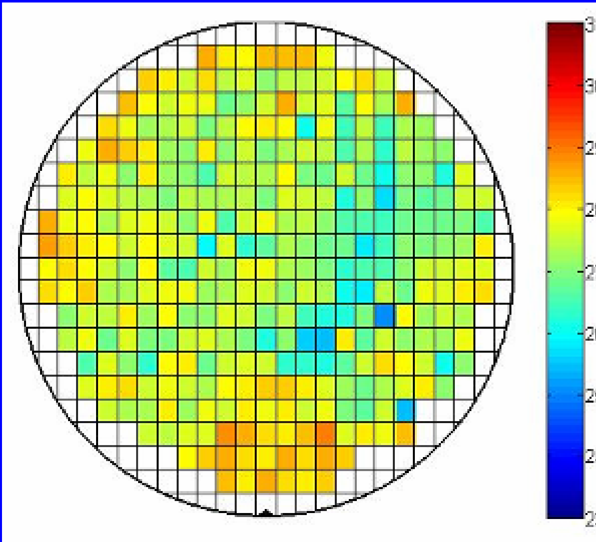
- ***After 2nd litho, good 0.24μm common DOF in both 1st and 2nd litho patterns of 32nmLS was obtained.***

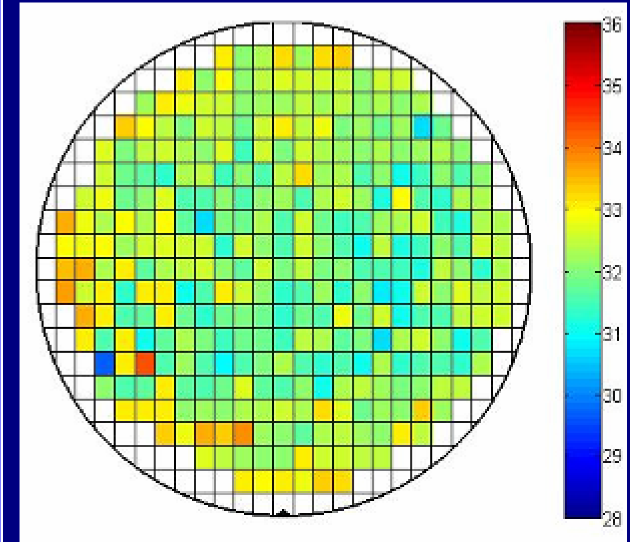
JSR SEMICONDUCTOR MATERIALS LABORATORY JSR

CD Uniformity of 32nmLS Pattern

After 1st Litho		After Freezing		After 2nd Litho (1st Pattern)	
average	29.3nm	average	27.4nm	average	32.2nm
3σ	1.36nm	3σ	1.96nm	3σ	1.86nm
max	30.8nm	max	28.9nm	max	34.3nm
min	28.0nm	min	25.1nm	min	29.7nm
range	2.8	range	3.8	range	4.6





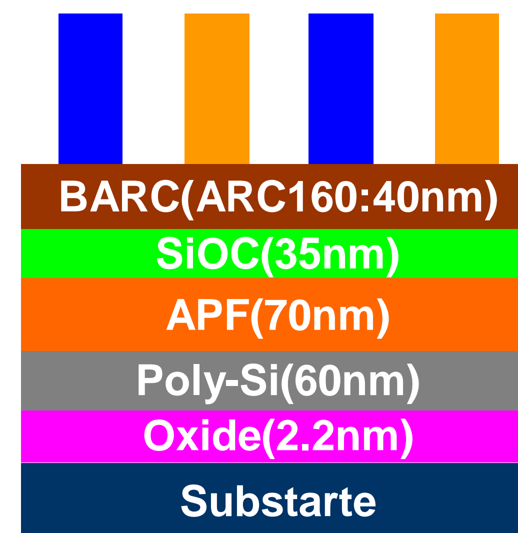


- CD uniformity of 1st litho pattern was kept within 2nm through double patterning step with freezing process.

Etching Experiment for "Freezing"

➢Materials

- 1st resist: **JSR standard resist** (FT=120nm(40nmL80nmP)/90nm(32nmL64nmP))
- Freezing materials: **FZX F103**
- 2nd resist: **JSR standard resist** (FT=90nm)



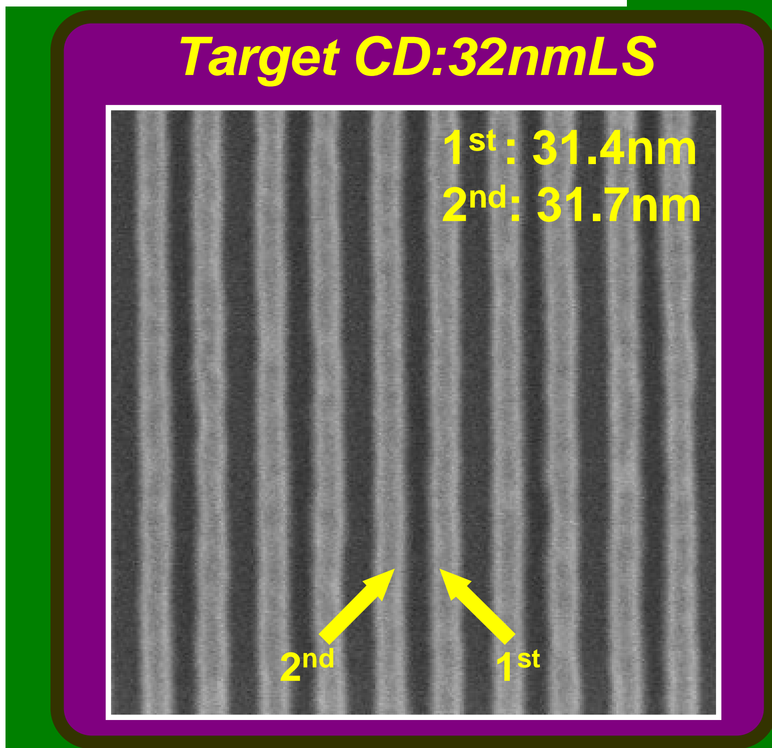
➢Organic/Inorganic stack

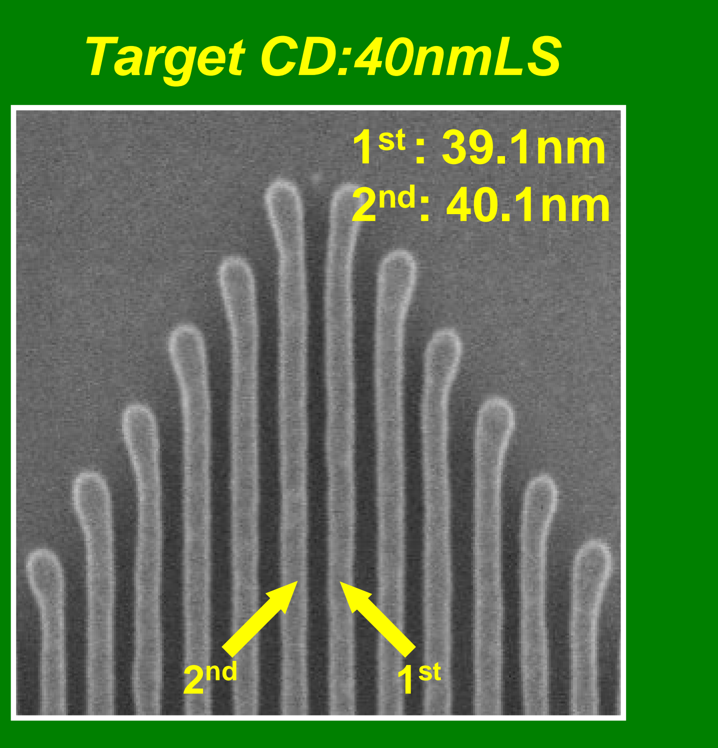
- BARC(ARC160):40nm / SiOC:35nm / APF:70nm/ Poly: 50nm/Oxide: 2.2nm

➢Target CD & Exposure/Illumination condition

- XT1700i(IMEC)
- ***40nmLS***: NA=1.2, Annular(0.8/0.5) + xy-pol.
- ***32nmLS***: NA=1.0, Dipole40 + pol.

Etching Results of 40&32nm LS Pattern





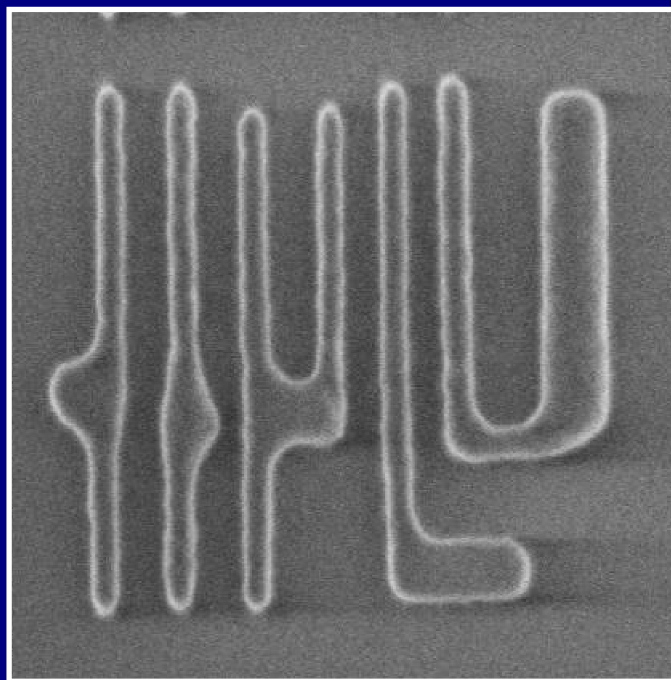
JSR SEMICONDUCTOR MATERIALS LABORATORY JSR

Contents

- *Background*
  - ✓ Various Double Patterning Techniques
  - ✓ Double Patterning Process with Resist "Freezing"
- ***Lithographic performance of JSR Freezing Process***
  - ✓ 32nm LS formation and Etching Result
  - ✓ **"Freezing" Process for 2D Logic Patterning**
  - ✓ CH Formation by "Freezing" Process
- *Summary*

"Freezing" Process for 2D Logic Pattern

After 2nd Litho
40nm Logic Pattern
CD~45nm



- ***Can we handle 2D logic patterning with "Freezing" process?***

JSR SEMICONDUCTOR MATERIALS LABORATORY JSR

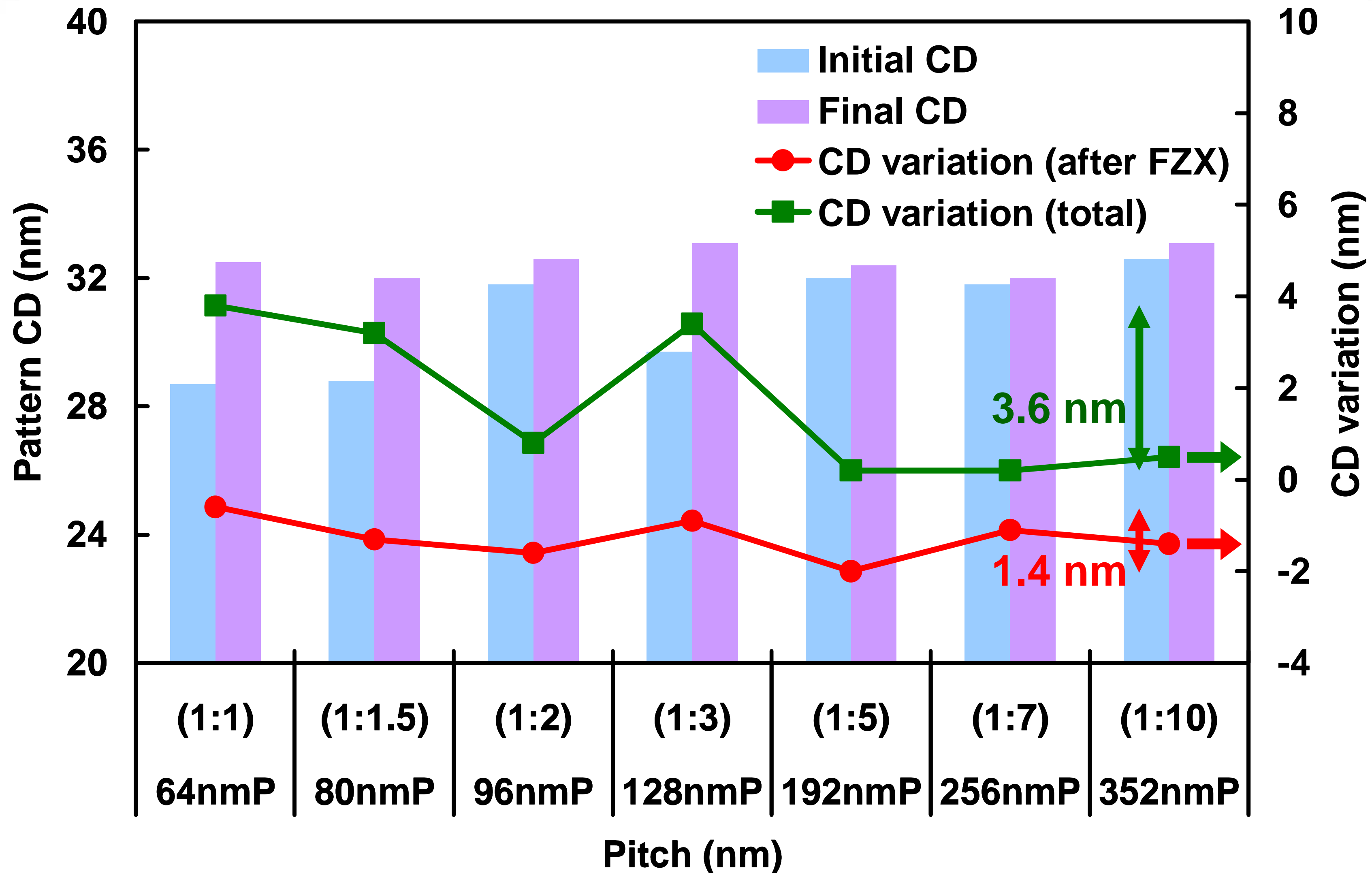
CD Control through "Freezing" Process

✓ *For complex 2D application, the pitch dependency of freezing process on 1st pattern CD variation is important.*

	64nmP (1:1)	80nmP (1:1.5)	96nmP (1:2)	128nmP (1:3)	192nmP (1:5)	256nmP (1:7)	352nmP (1:10)
After 1st Litho	28.7nm	28.8nm	31.8nm	29.7nm	32.0nm	31.8nm	32.6nm
After Freezing	28.1nm	27.5nm	30.2nm	28.8nm	30.0nm	30.7nm	31.2nm
After 2nd Litho	1st: 32.5nm 2nd: 31.9nm	32.0nm 32.2nm	32.6nm 33.1nm	33.1nm 33.2nm	32.4nm 32.7nm	32.0nm 32.8nm	33.1nm 33.3nm

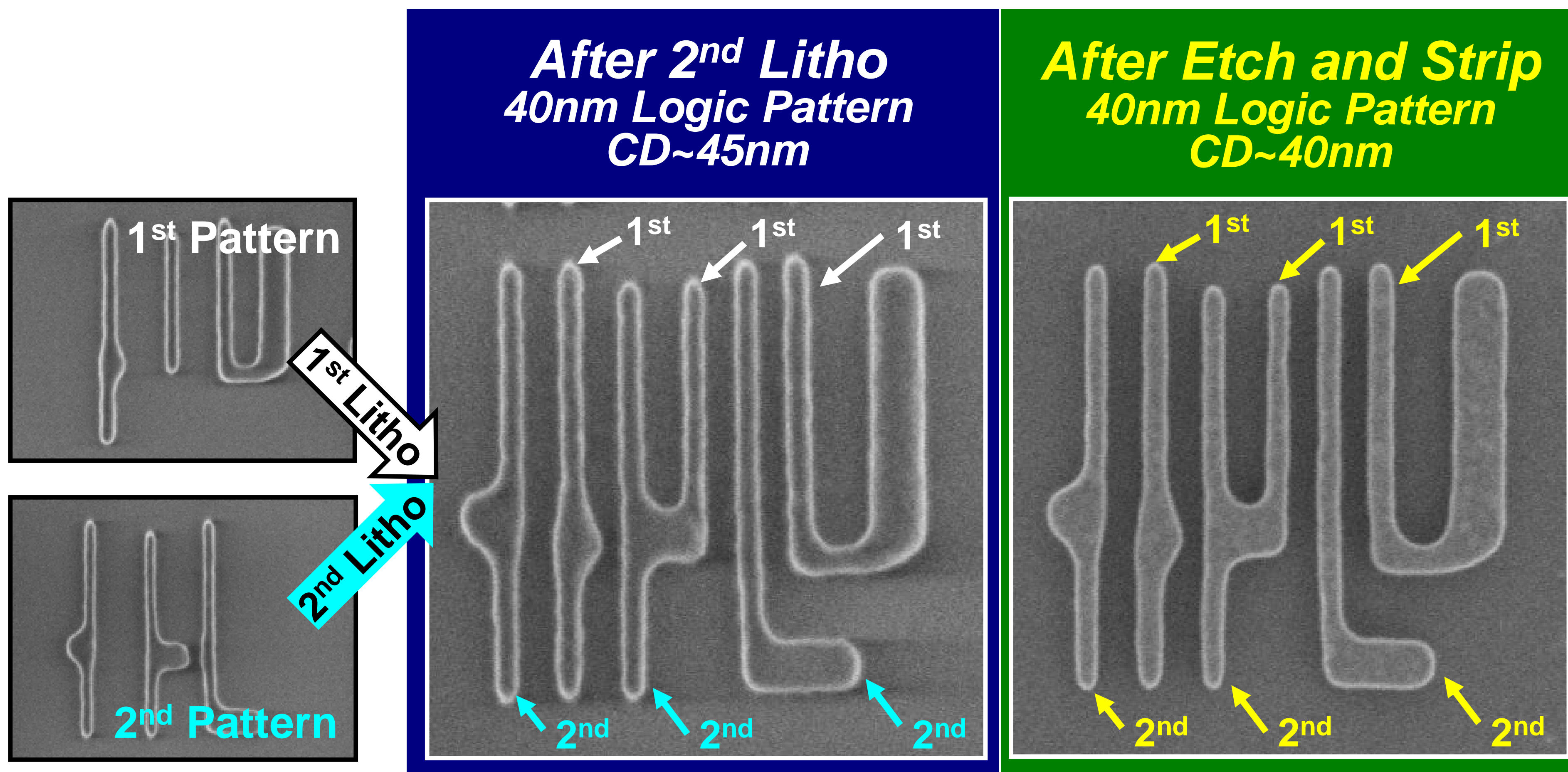
➢ *Freezing technique works well for 32nm various pitch patterns.*

CD Variation of 1st Pattern through Process



➢ ***Total CD variation was kept within 3.6nm though various pitches.***

Etching Results of 2D Logic Pattern

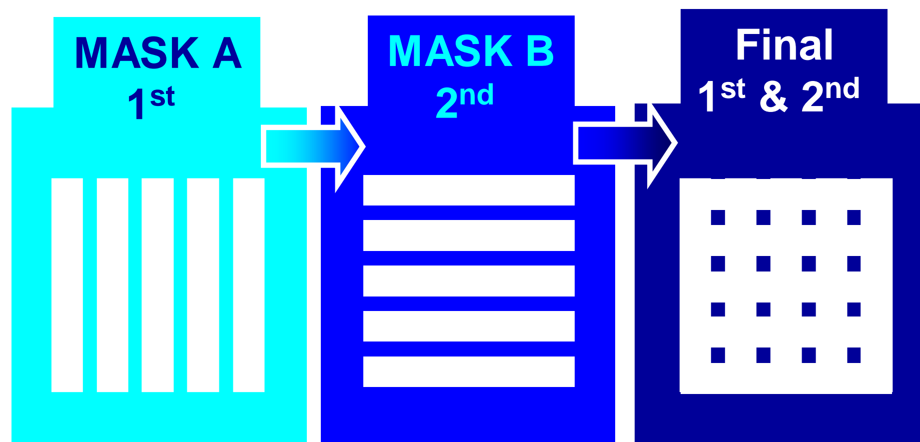


- Freezing technique is also available for complex 2D pattern.
- Configuration of litho pattern was kept after etching.

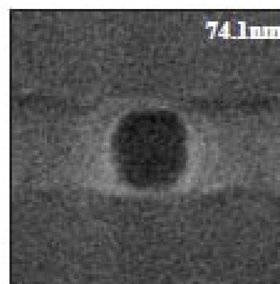
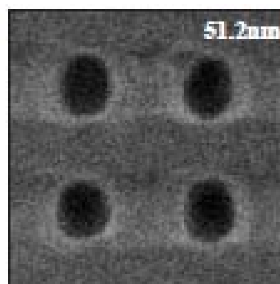
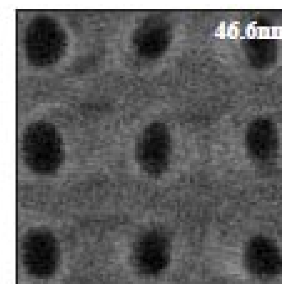
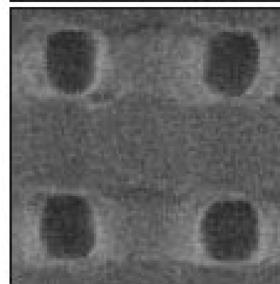
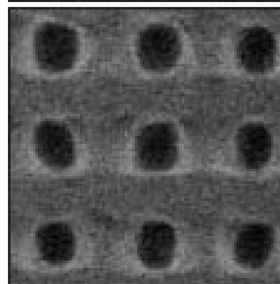
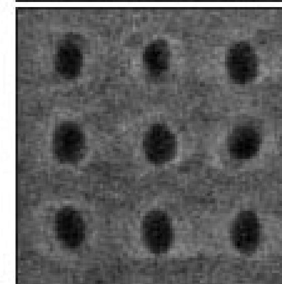
Contents

- ***Background***
  - ✓ **Various Double Patterning Techniques**
  - ✓ **Double Patterning Process with Resist “Freezing”**
- ***Lithographic performance of JSR Freezing Process***
  - ✓ **32nm LS formation and Etching Result**
  - ✓ **“Freezing” Process for 2D Logic Patterning**
  - ✓ **CH Formation by “Freezing” Process**
- ***Summary***

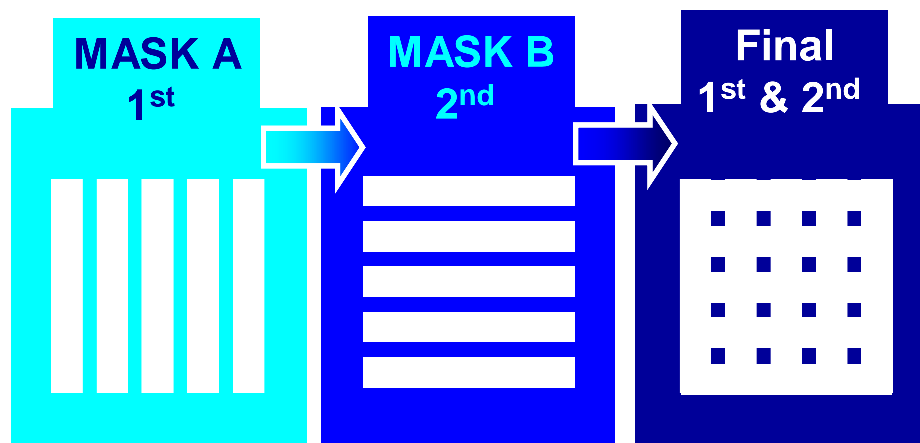
Cross-Lines CH Double Patterning



- Hole feature can be generated by using x/y-cross lines method with freezing process.

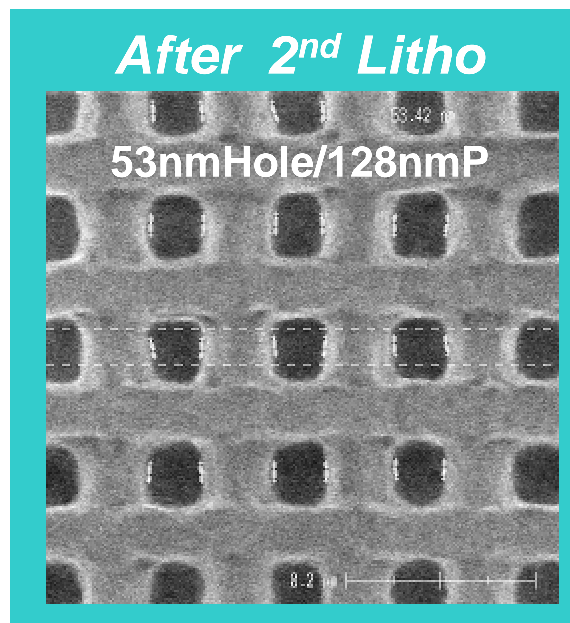
74nmHole/200nmP (125nm-line)	51nmHole/120nmP (70nm-line)	46nmHole/104nmP (60nm-line)
		
		

Cross-Lines CH Double Patterning



➢ **Hole feature can be generated by using x/y-cross lines method with freezing process.**

➢ **Exposure/Illumination** NA=1.2, Ann(0.8/0.5)+xy-pol.



Summary

- New resist "Freezing" process was developed for Litho-Litho-Etch double patterning process.
- 32nmLS and 2D Logic patterning formation was successfully demonstrated by double patterning with "Freezing" process.
- Possible application for CH pattern formation is also done by "Freezing" Process. Etching result will be presented in near future.