Double Patterning process development at IMEC

M. Maenhoudt, D. Vangoidsenhoven, T. Vandeweyer, R. Gronheid, J. Versluijs, A. Miller

Introduction

- Objectives of this work
  - budget verification for 32nm HP critical layers
    - 2 flavors of double patterning: double litho, double etch (LELE) and Self-Aligned DP (SADP)
  - status and feasibility of alternative processes to reduce DPT CoO

- 32nm half pitch specs (ITRS)

	Single exposure	Double patterning
– CDU	2.6nm	1.3nm
– Overlay	6.4nm	≅2.3nm
– LWR	1.7nm	1.7nm

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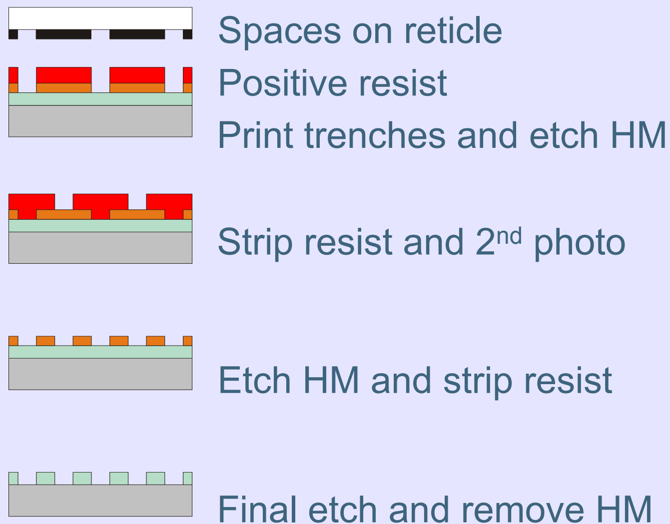
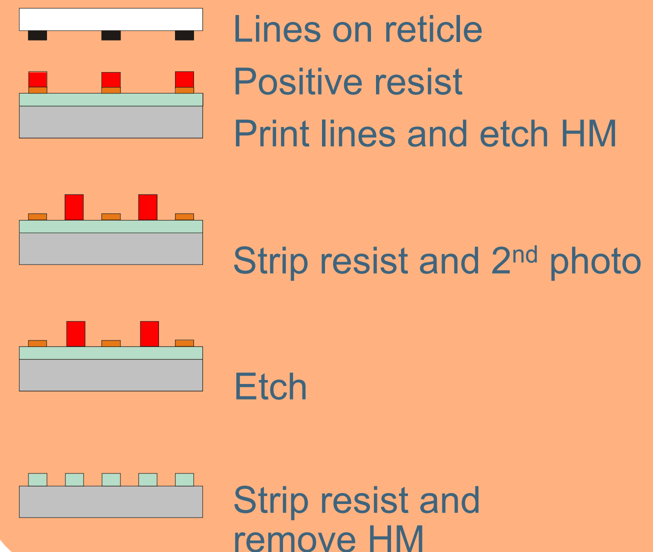
outline

- Litho-Etch-Litho-Etch
  - double line process for Active/Poly
    - CDU
    - overlay
  - double trench process for M1
  - alternative processes (CoO)
- Self-Aligned Double Patterning
  - 32nm HP process
    - CDU
  - alternative process (CoO)
- Conclusions

Litho-Etch-Litho-Etch

- 2D compatible processes
- double trench vs double line
  - DT most intuitive for Metal layers
  - DL most intuitive for Active, Poly layers





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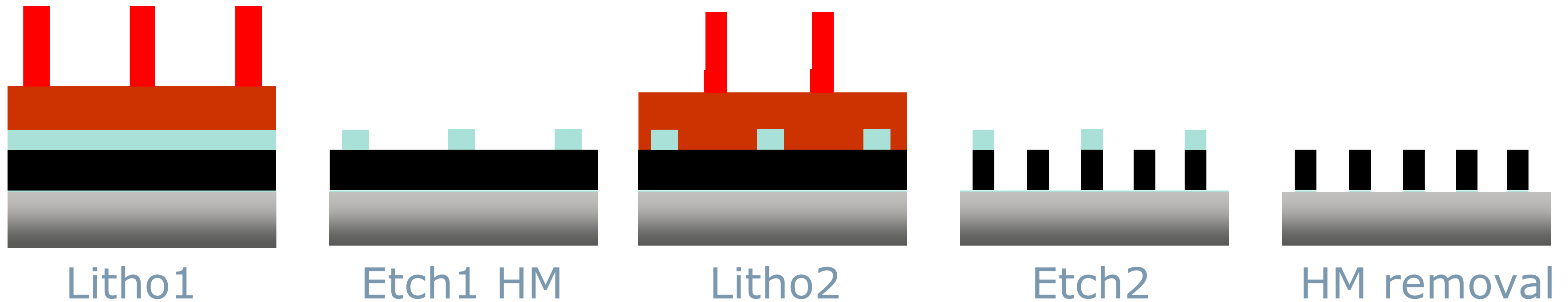
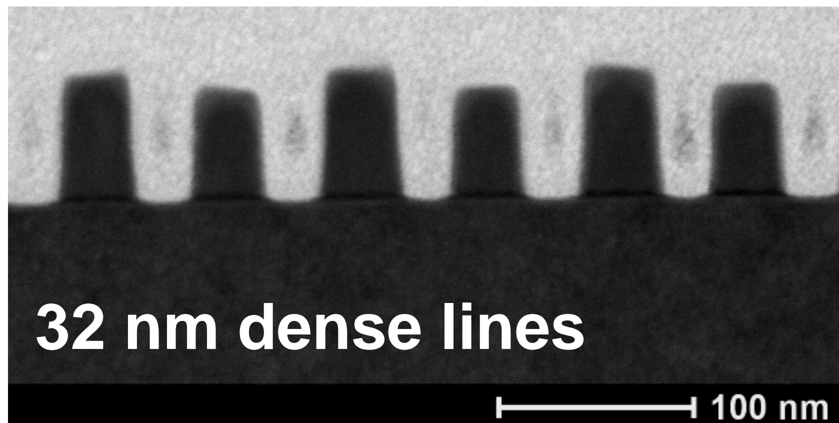
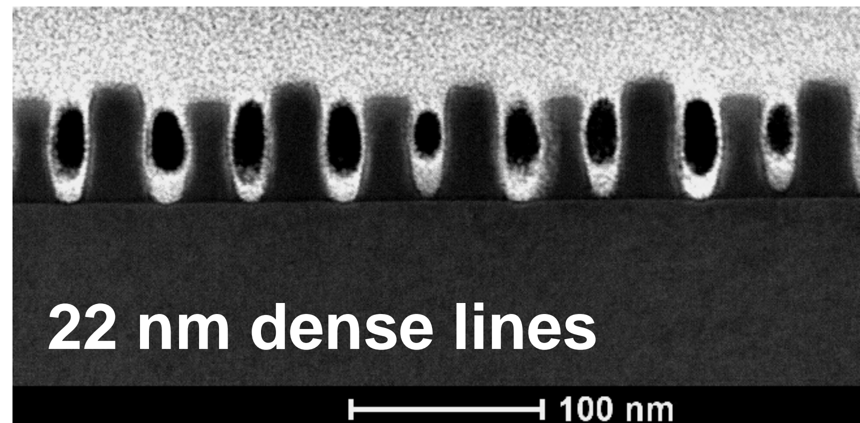
LELE double line process



- 32nm HP poly: single oxide HM (30nm) process
- 22nm HP poly: double HM needed

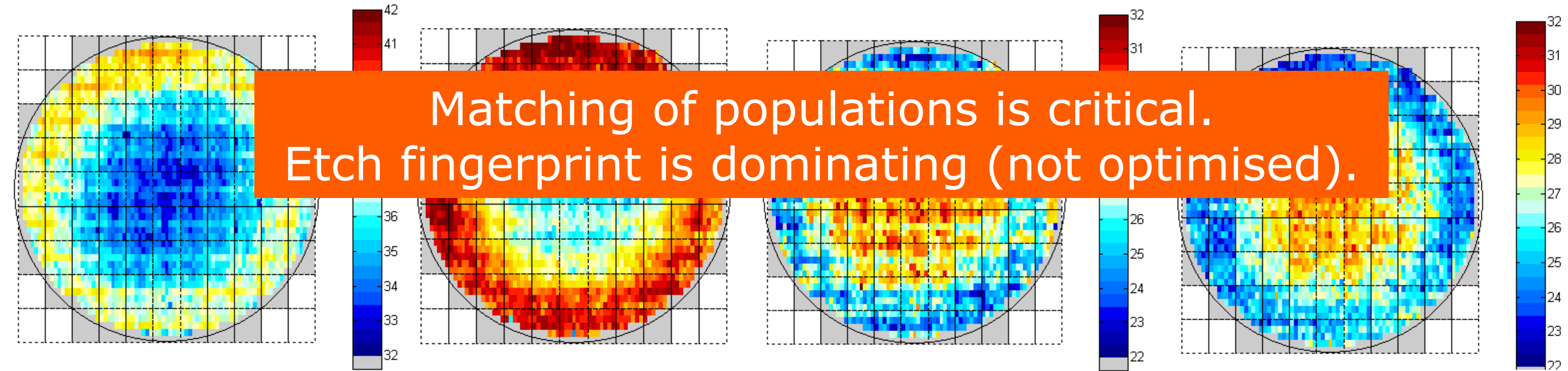




STEM imaging and sample preparation at ASML

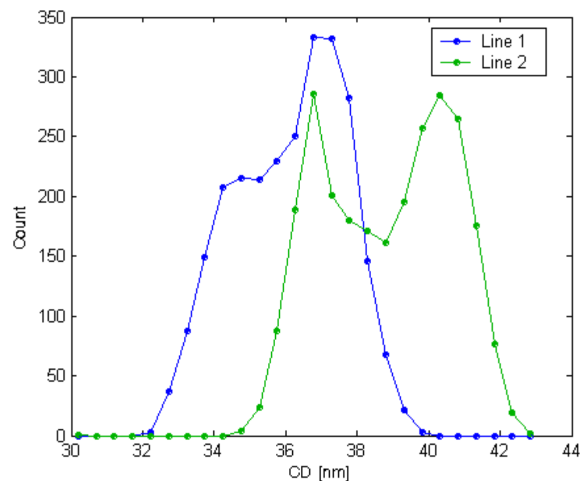
CDU 32nm LELE (raw experimental data)
CD's after final etch

NA=1.35
ann. ill. 0.8/0.5
$k1_f$=0.22

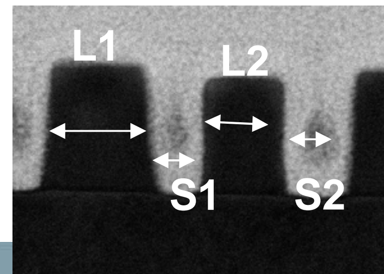


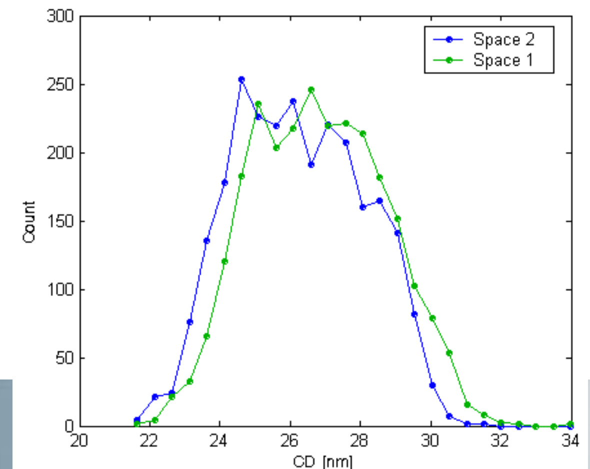
Matching of populations is critical.
Etch fingerprint is dominating (not optimised).

Line1:	Line2:	Space1	Space2
Mean=36.1	Mean=38.8	Mean=26.8	Mean=26.25
3σ=4.6nm	3σ=5.5nm	3σ=5.7nm	3σ=5.6nm



(CD SEM, 2579 measurements)

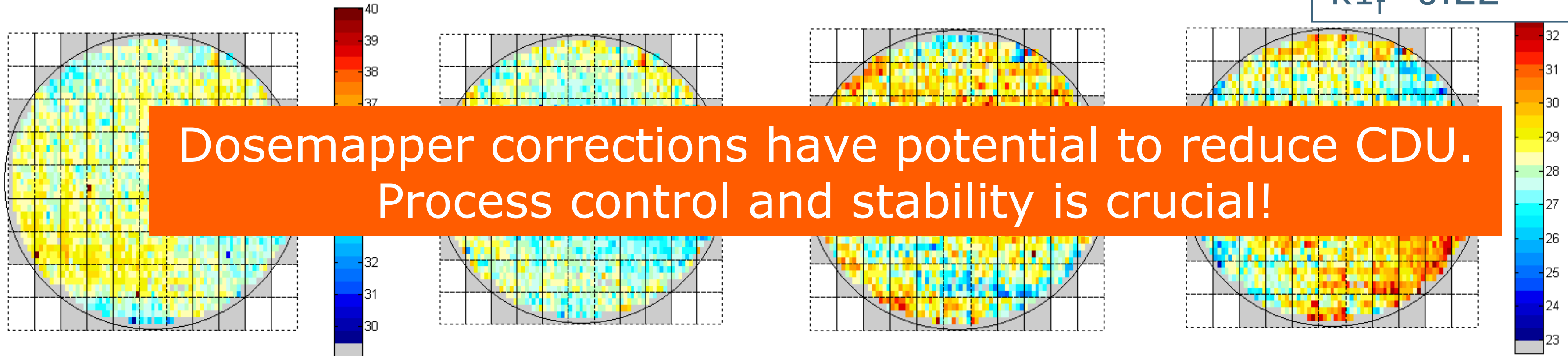




CDU 32nm LELE applying Dosemapper™

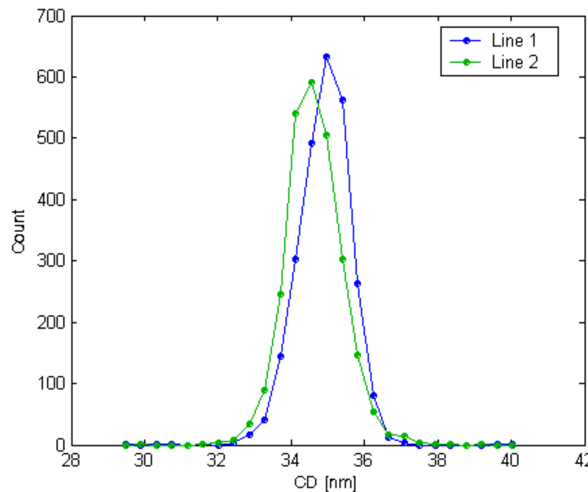
CD's after final etch

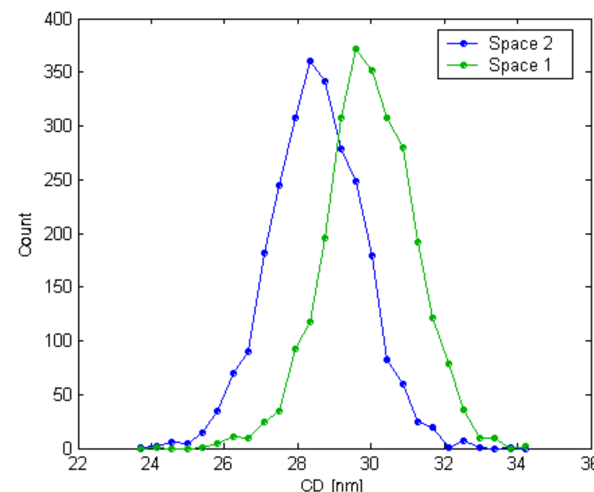
NA=1.35
ann. ill. 0.8/0.5
$k1_f=0.22$



Dosemapper corrections have potential to reduce CDU.
Process control and stability is crucial!

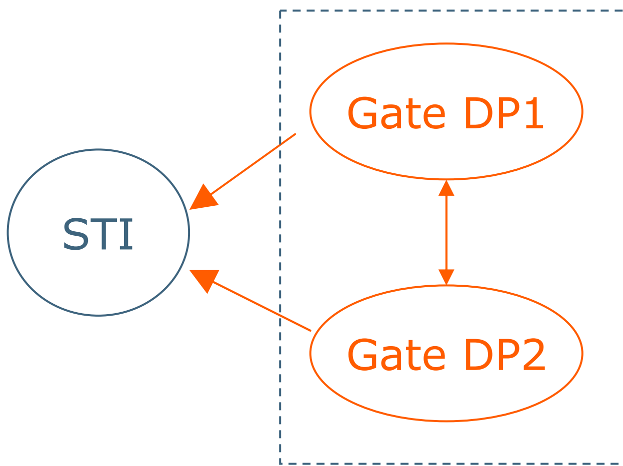
Line1:	Line 2	Space 1	Space 2
Mean=34.9	Mean=34.6	Mean= 30.0	Mean=28.5
3σ=2.2nm	3σ=2.3nm	3σ=3.7nm	3σ=3.8nm

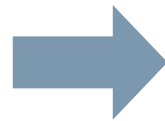


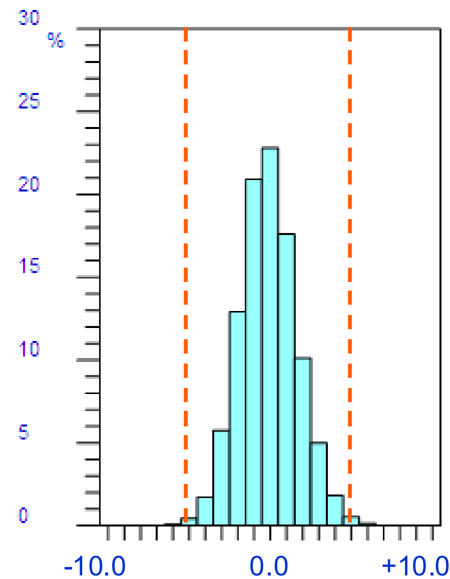


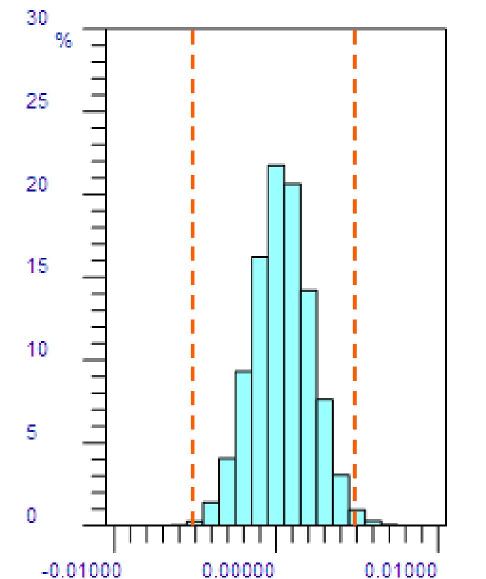
DPT overlay on product wafers (gate to STI)

Full batch DPT measured overlay on ASML XT:1700i (NA=1.2)









DP1, DP2 align to same reference layer

|m|+3σ: X = 5.5nm, Y = 5.8nm

30 points per field, 87 fields per wafer, 20 wafers.

D. Laidler, et al., SPIE 2008, 6922-23

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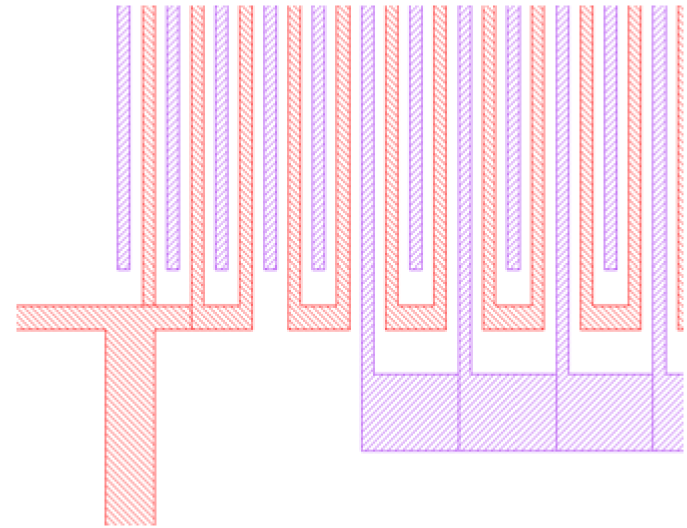
LELE double trench process: 30nm HP Metal1

- goal: 30nm 1:1 trenches for Single Damascene interconnects using 1.2NA scanner ($k1_f$ =0.19)
  - regular structures, no cuts, no gaps
- DP: 30nm at pitch 120nm for each patterning step
- LAM Motif™ shrink used because no litho process window for 30nm trench
- CD target = 60nm after litho, shrink to 30nm



e.g. meanderforks, after split of target design:

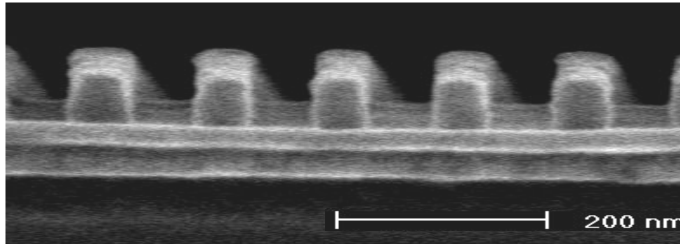
Trenches defined by image 1

Trenches defined by Image 2

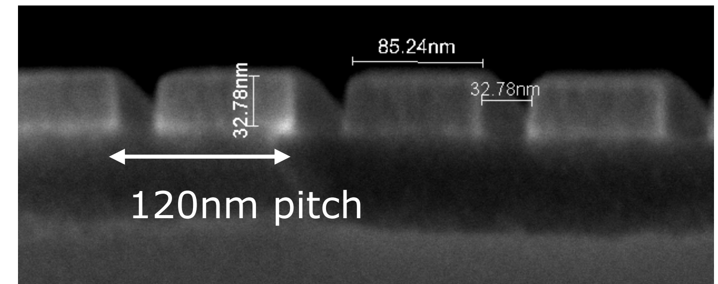
30nm HP M1: pics through process steps

NA=1.2
quasar ill.
$k1_f$=0.19

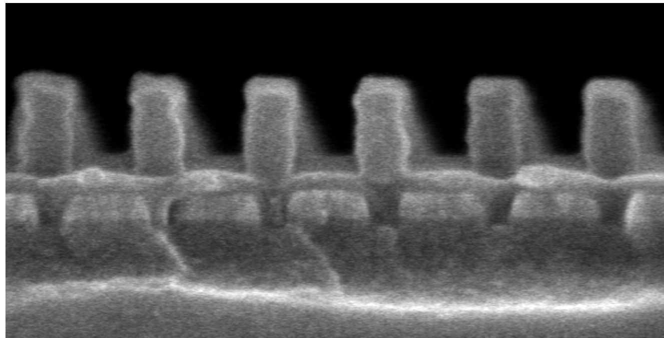
Litho1



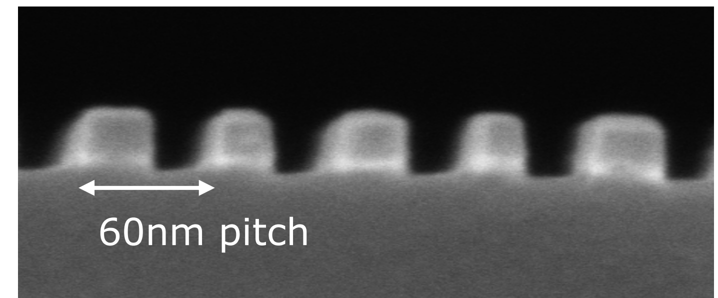
Etch1



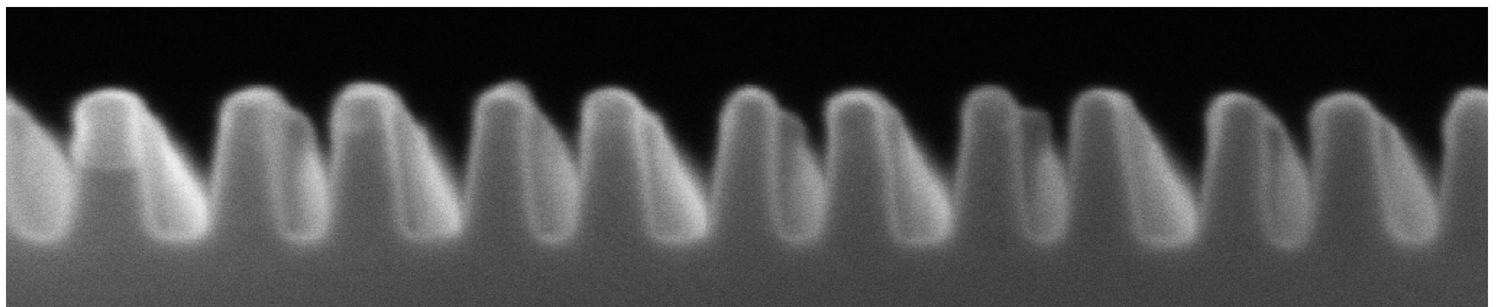
Litho2



Etch2



Etch3



30nm half-pitch structures etched into BDII low-k material

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CDU 30nm HP M1

- L1 CD uniformity

(full wafer; 357 dies)

-litho: 3σ = 2.5nm

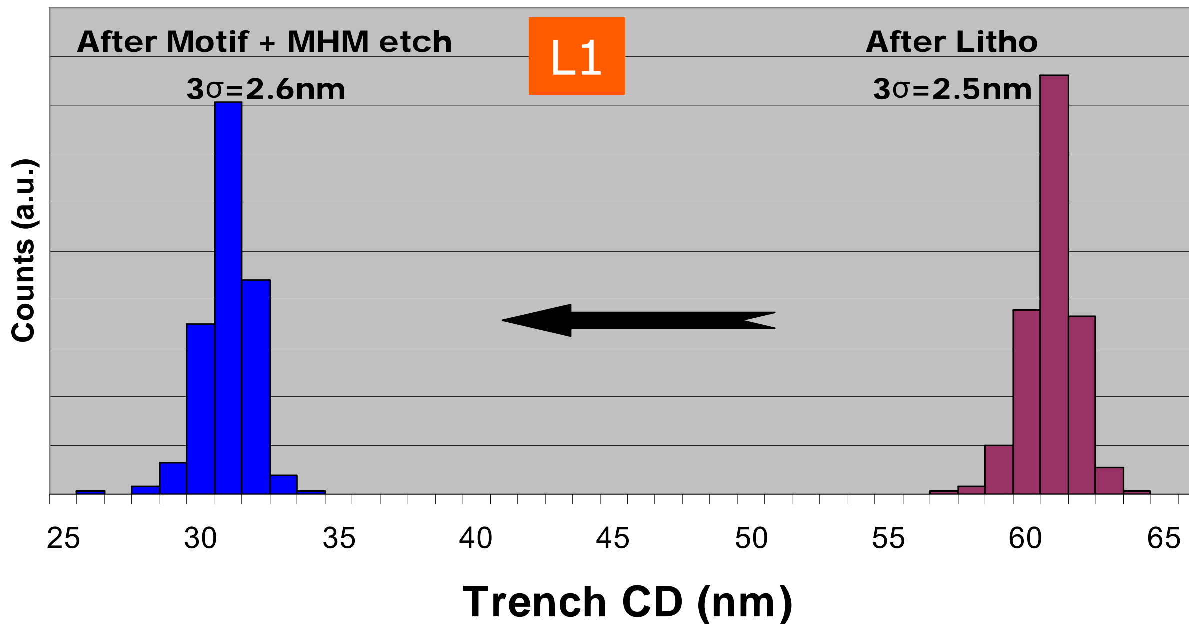
-MHM etch: 3σ = 2.6nm

- L2 CD uniformity

(full wafer; 25 dies)

-litho: 3σ = 3.1nm

-MHM etch: 3σ = 3.6nm



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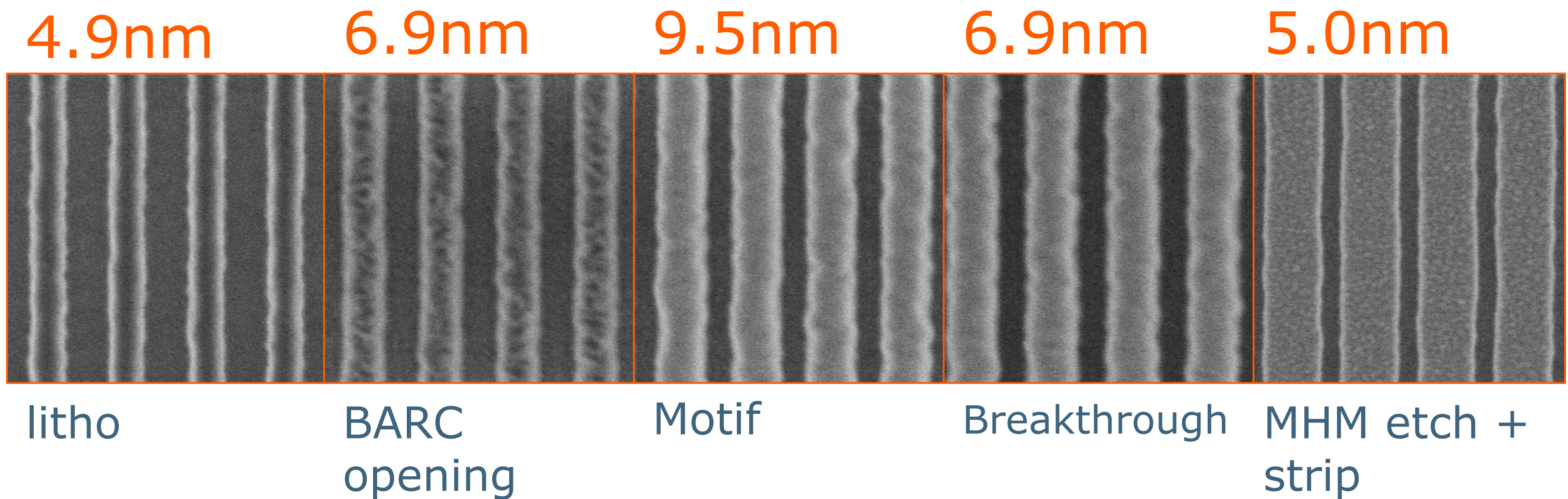
LWR 30nm HP M1 LELE

- L1 LWR 3σ:

(~200 images)

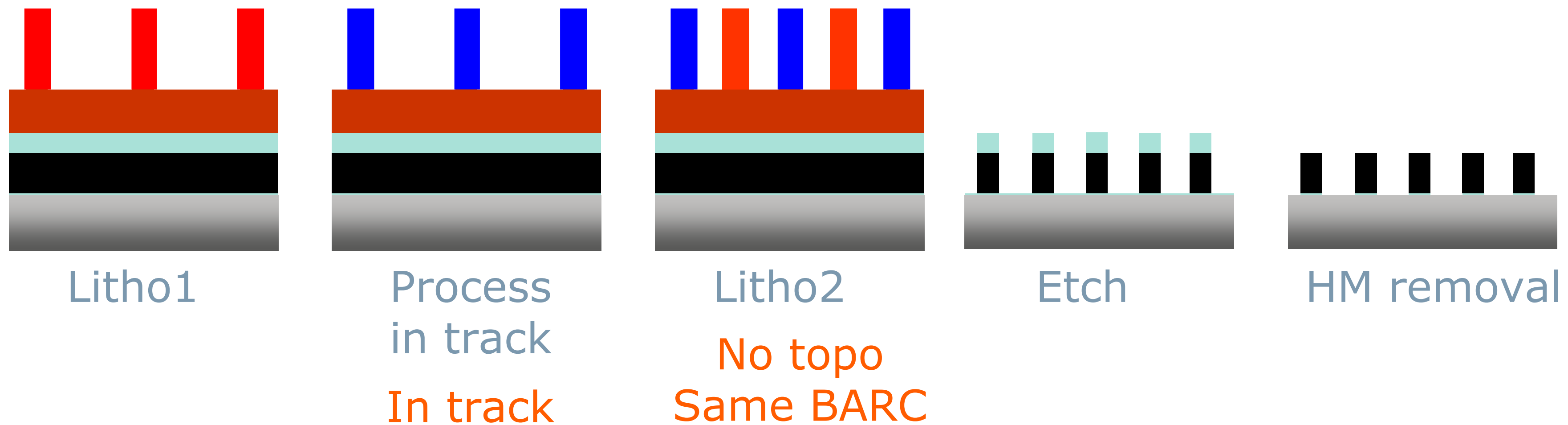


LWR after shrink + etch comparable to after Litho

outline

- LELE
  - double line process for Active/Poly
    - CDU
    - overlay
  - double trench process for M1
  - alternative processes (CoO)
- SADP
  - 32nm HP process
    - CDU
  - alternative process (CoO)
- Conclusions

Litho-Process-Litho-Etch



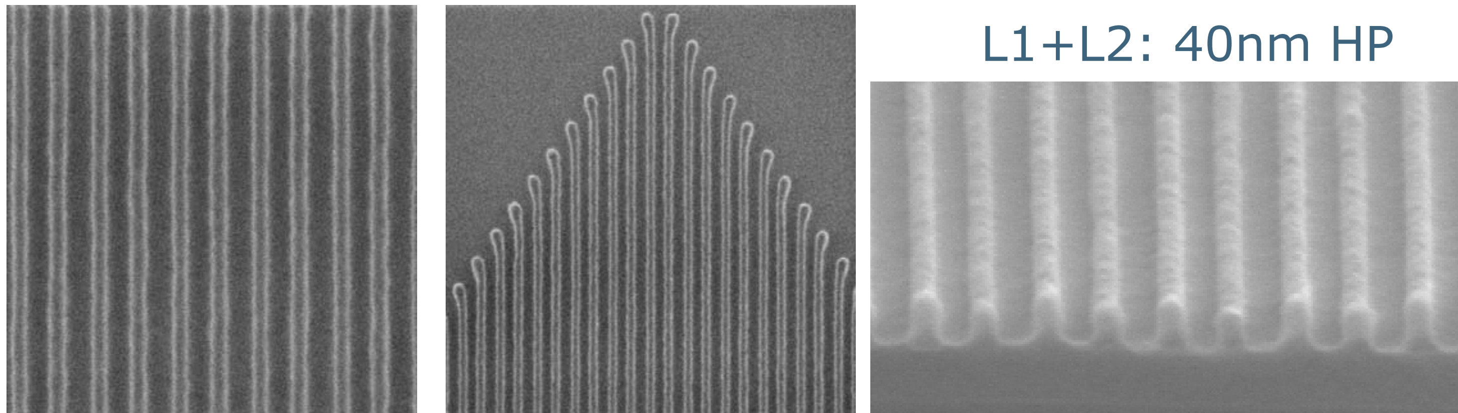
- Thermal freezing process (Shin-Etsu)
  - Exposure cure + bake cure
- Positive/negative resist (TOK)
  - No process treatment needed
- Coat freezing material (JSR)
  - Coat, bake, develop freezing material
- many other …

freezing material: resolution

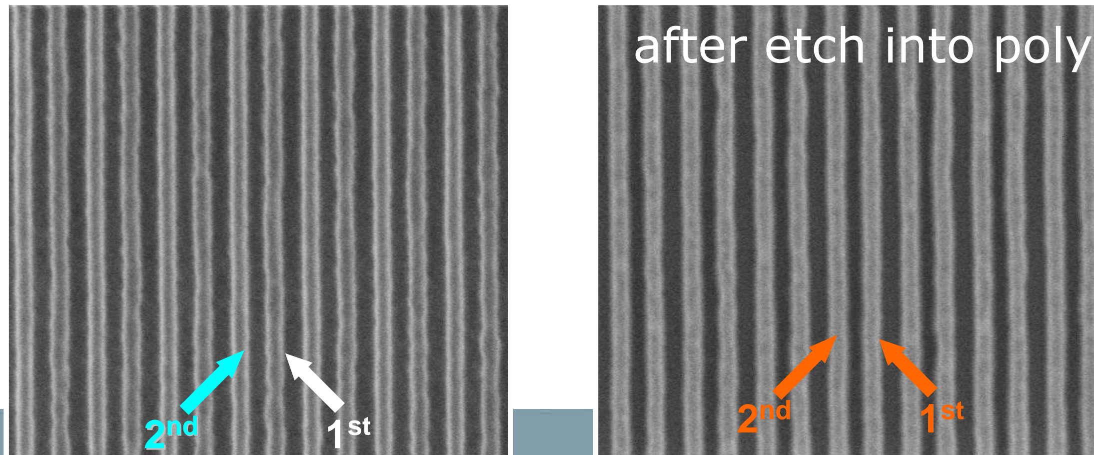
NA=1.2
ann. ill.

Ref. SPIE 6923-17, M. Hori et al.

- 44nm HP using NA=1.2, annular illumination



- 32nm HP using NA=1.0, dipole illumination



JSR Micro MATERIALS INNOVATION JSR

CDU freezing material: 44nm HP

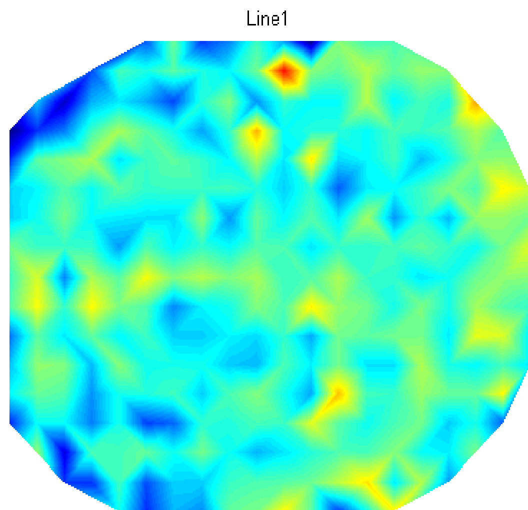
NA=1.2
ann. ill.

manual coatings

2 populations after L1+freezing+L2

Combined populations

Pop 1



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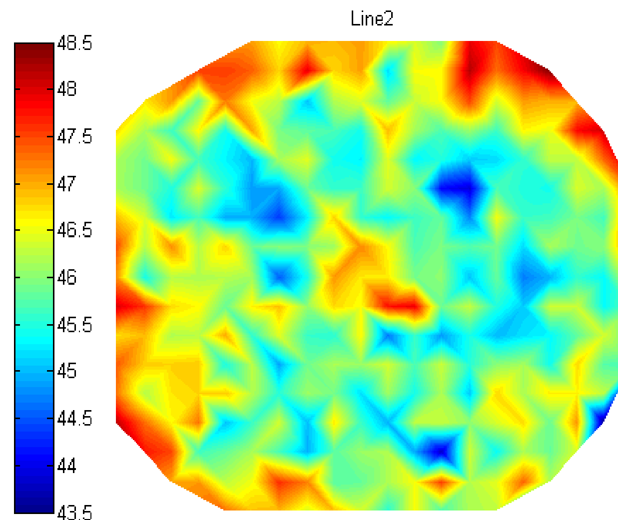
Pop 2



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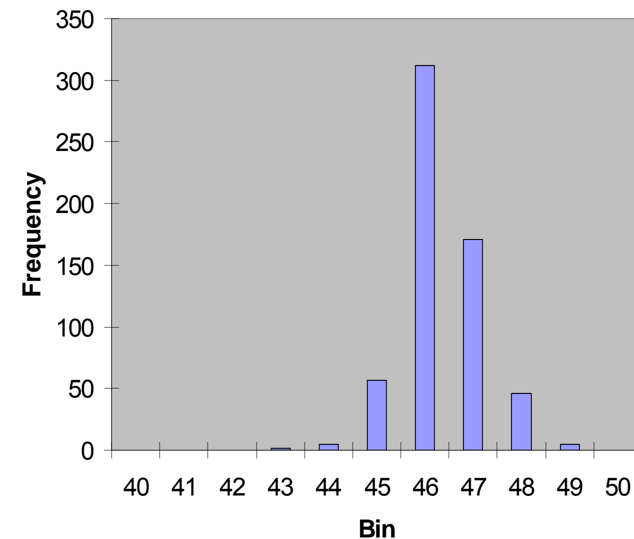


Average=45.5nm
3σ=1.8nm

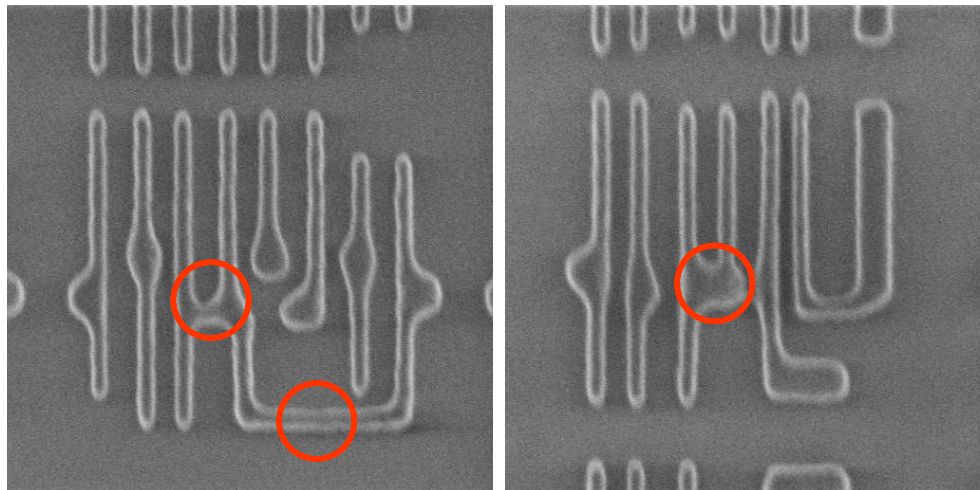
Average=46.2nm
3σ=2.5nm

Average=45.9nm
3σ=2.4nm

2D logic cells with freezing material

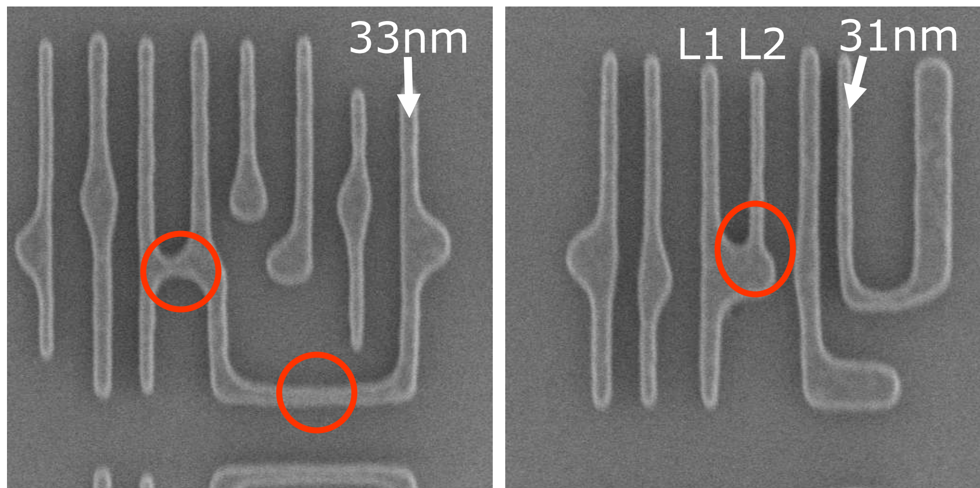
NA=1.2
ann. ill.

Litho

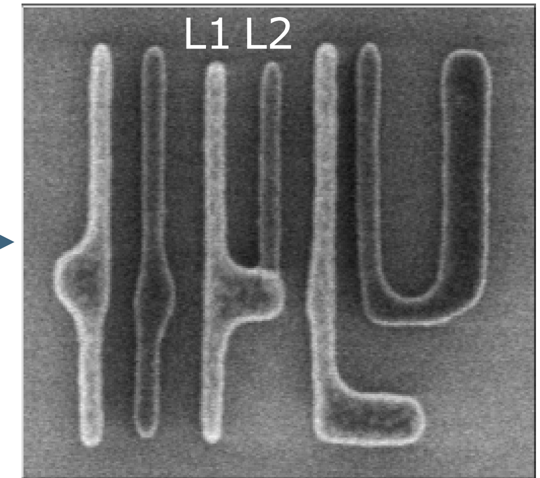


Non-optimized OPC

Etch



Litho-etch-litho-etch

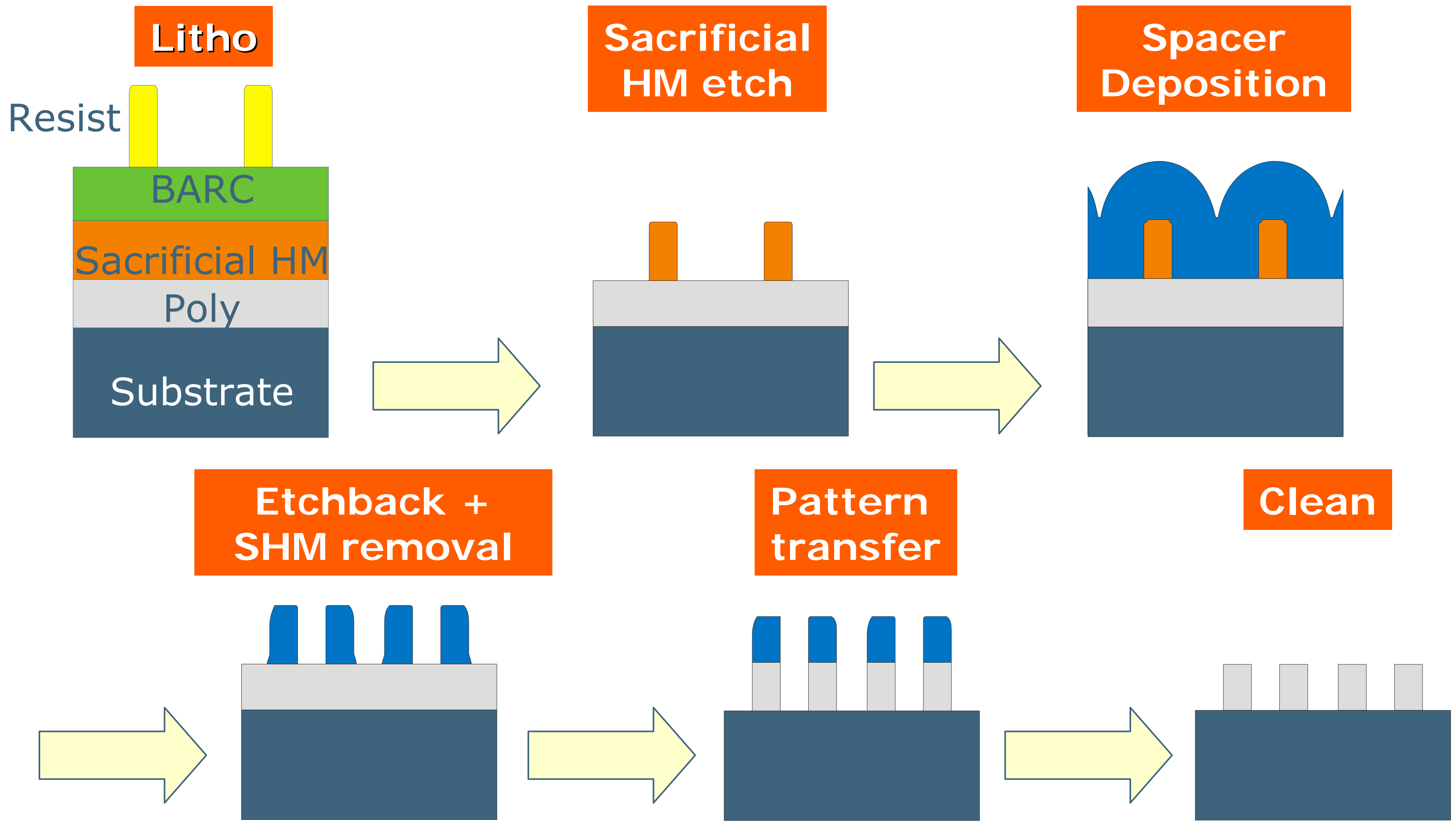


32nm node logic structures etched into 60nm poly using APF/SiOC HM

outline

- LELE
  - double line process for Active/Poly
    - CDU
    - overlay
  - double trench process for M1
  - alternative processes (CoO)
- SADP
  - 32nm HP process
    - CDU
  - alternative process (CoO)
- Conclusions

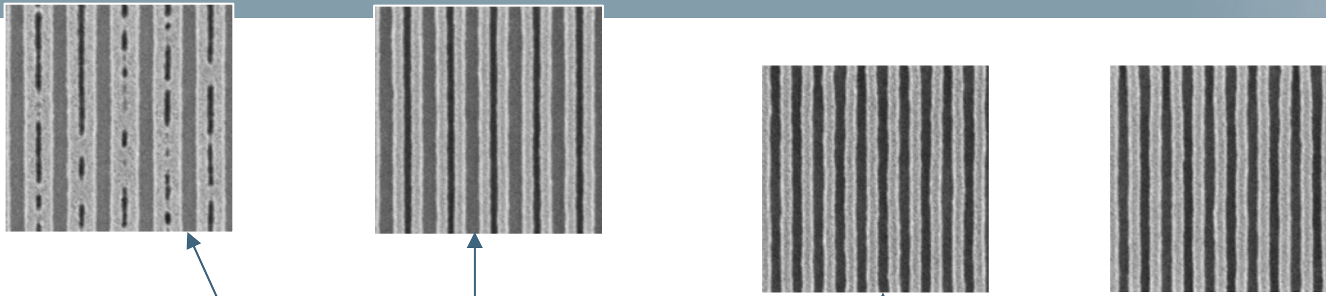
Positive Self-Aligned Double Patterning Process (SADP)

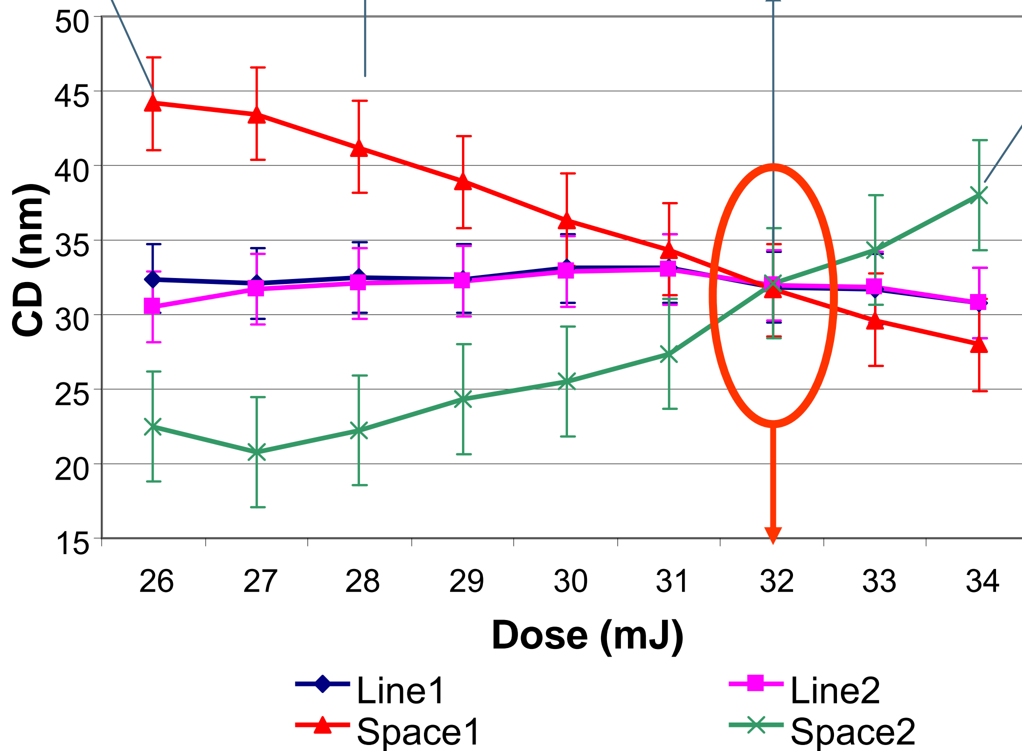


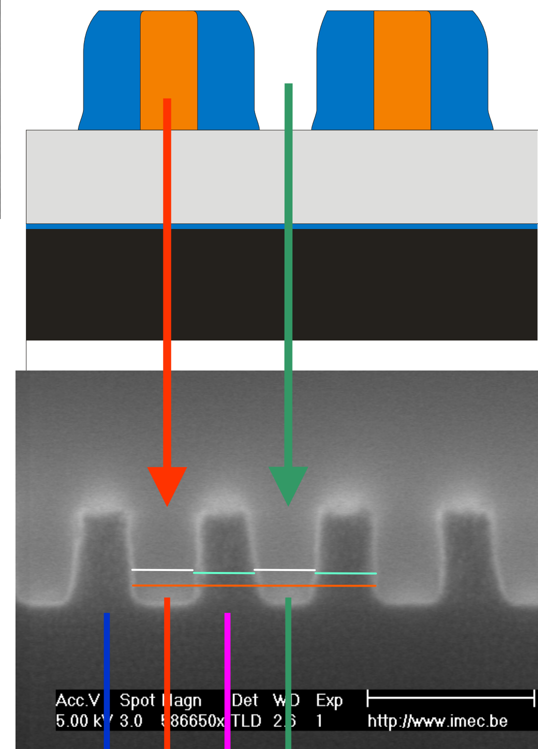
Extra trim mask + mask for non-critical periphery needed

Impact of the Dose on space CD

NA=1.2
0.8/0.5 ann.





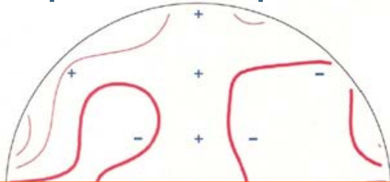
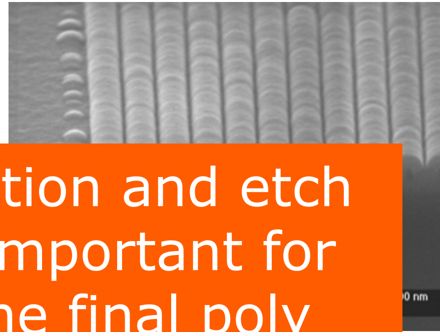


~700 measurements/data point

CDU of lines and spaces for 32nm HP process

NA=1.2
0.8/0.5 ann.

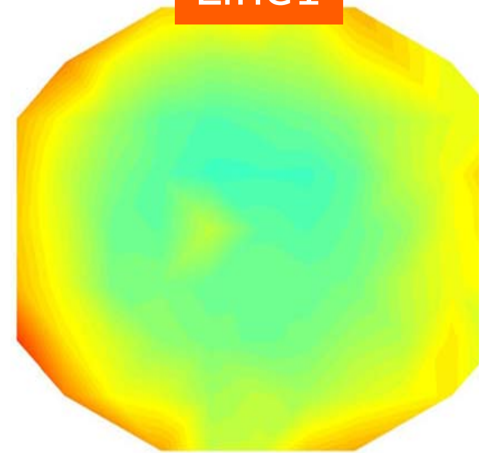
spacer deposition

Spacer deposition and etch uniformity is important for definition of the final poly width.

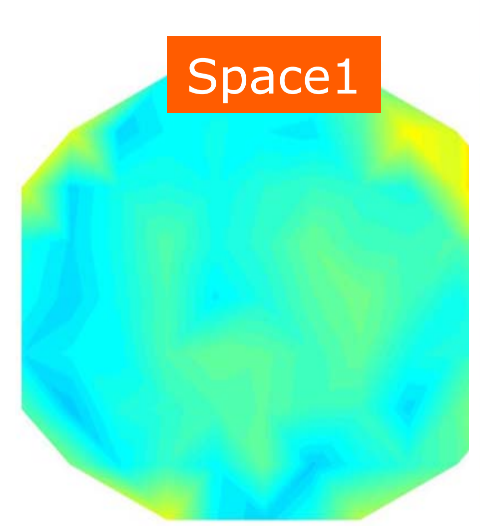
Dose control and etch uniformity is critical for space CD control (pattern placement).

non-optimised etch



Line1
CD = 32.8nm
3σ = 2.8nm

Line2
CD = 32.8nm
3σ = 2.6nm



Space1
CD=29.8nm
3σ=3.4nm

Space2
CD=32.4nm
3σ=5.9nm

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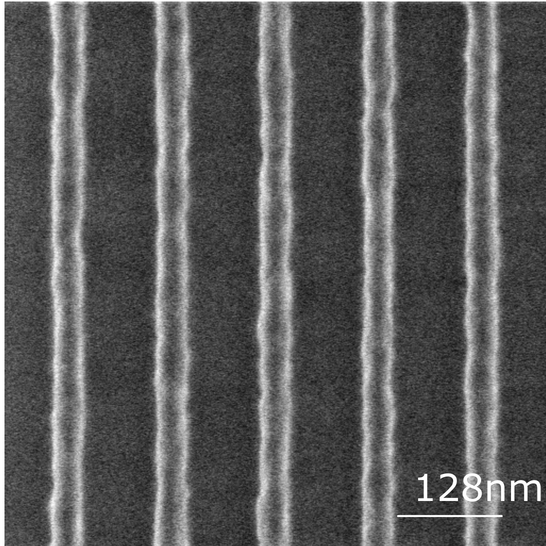
LWR/LER for SADP

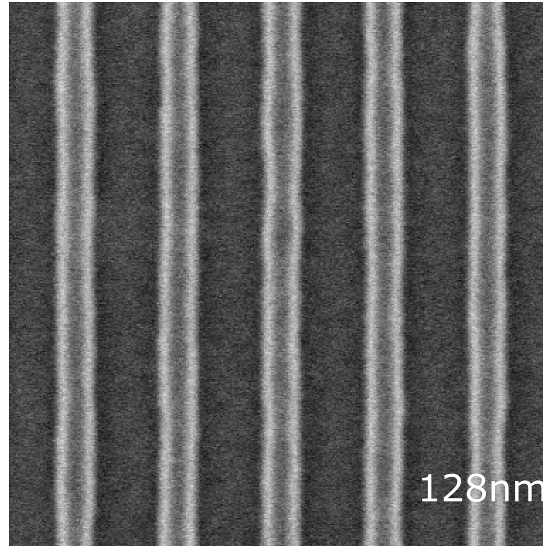
150 images/set

Litho



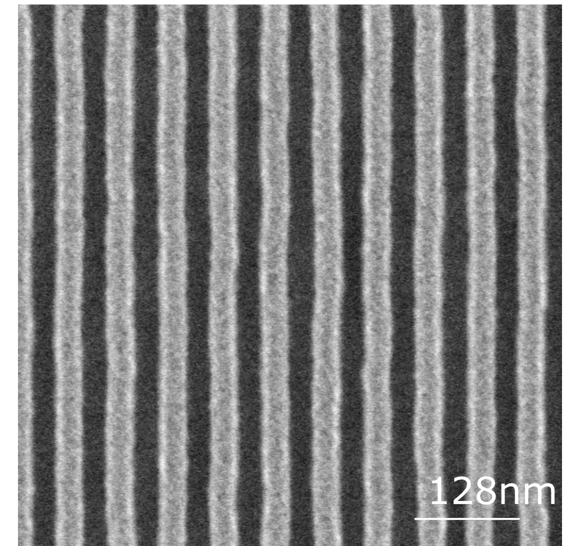
Average LWR
= (5.59 ± 1.08)nm
Average LER
= (3.7 ± 0.45)nm

Sacrifical HM



Average LWR
= (6.43 ± 2.94)nm
Average LER
= (3.9 ± 0.34)nm

Final poly lines



Average LWR
= (3.53 ± 0.52)nm
Average LER
= (4.1 ± 0.54)nm

LWR of the final pattern is half of the LWR after litho.
LER of the different steps is comparable!

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  - 32nm HP process
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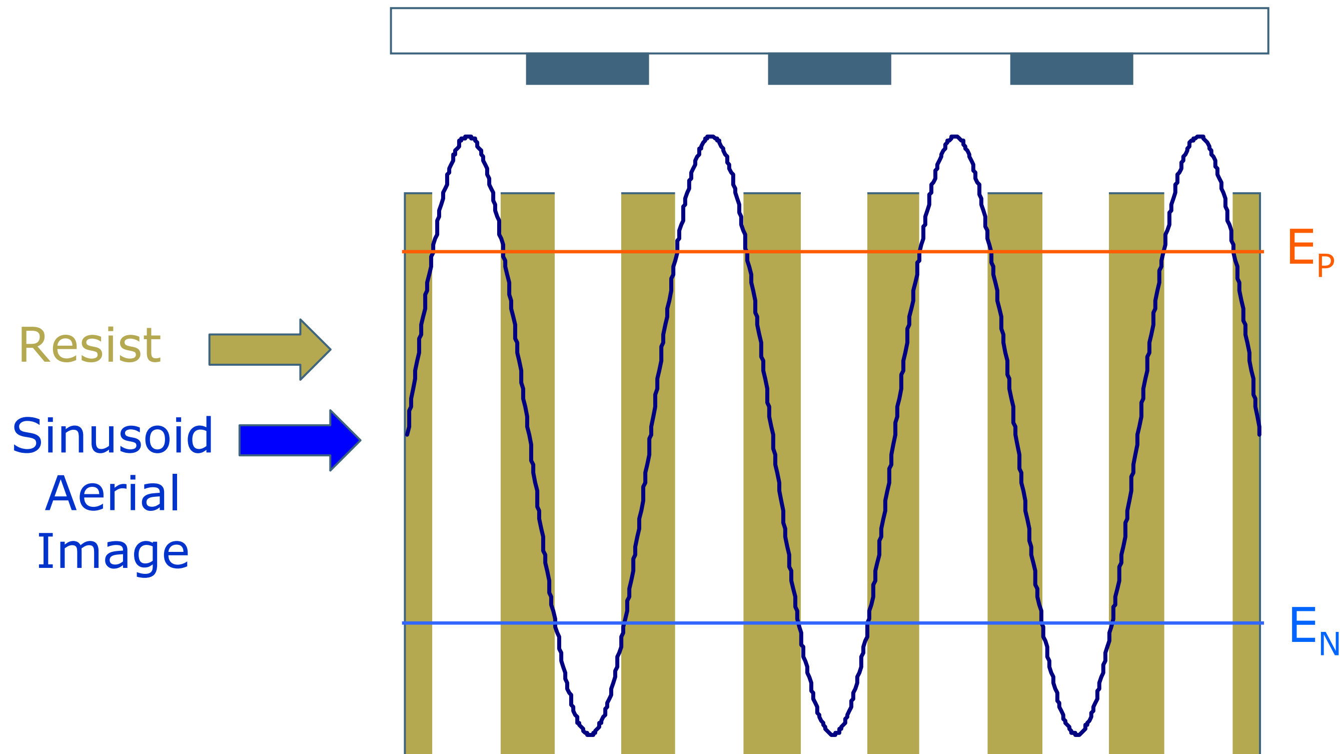
  - alternative process (CoO)

- Conclusions

Dual Tone development

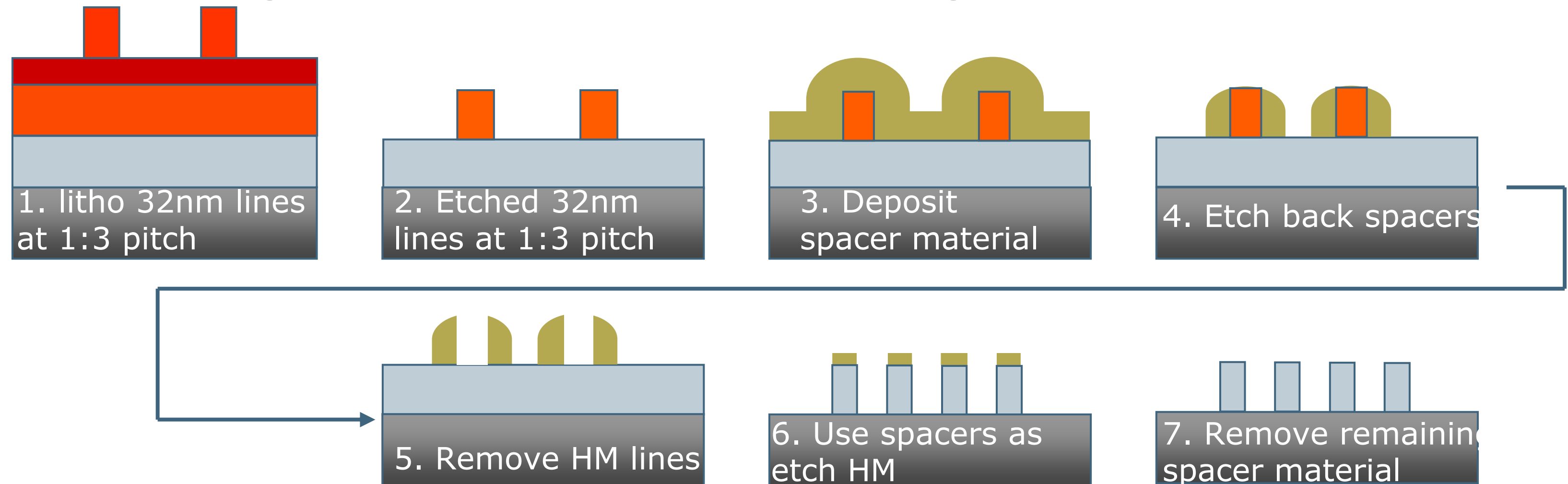
- Principle: Positive + Negative (Dual)-Tone Development on single exposed wafer

Frequency doubling in a single exposure!

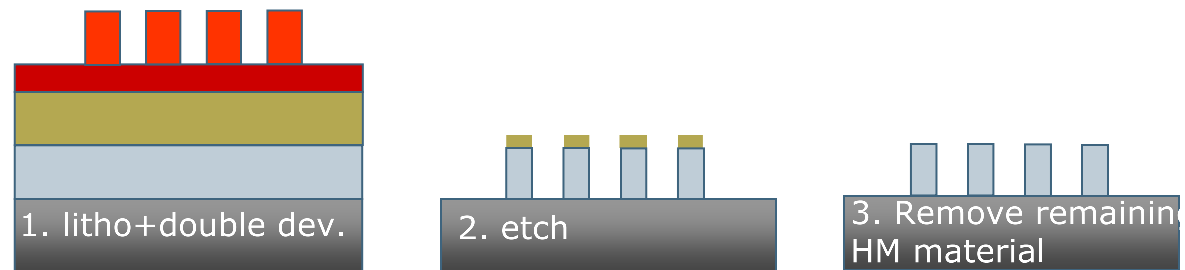


Dual Tone Development as alternative for Self- Aligned DP process

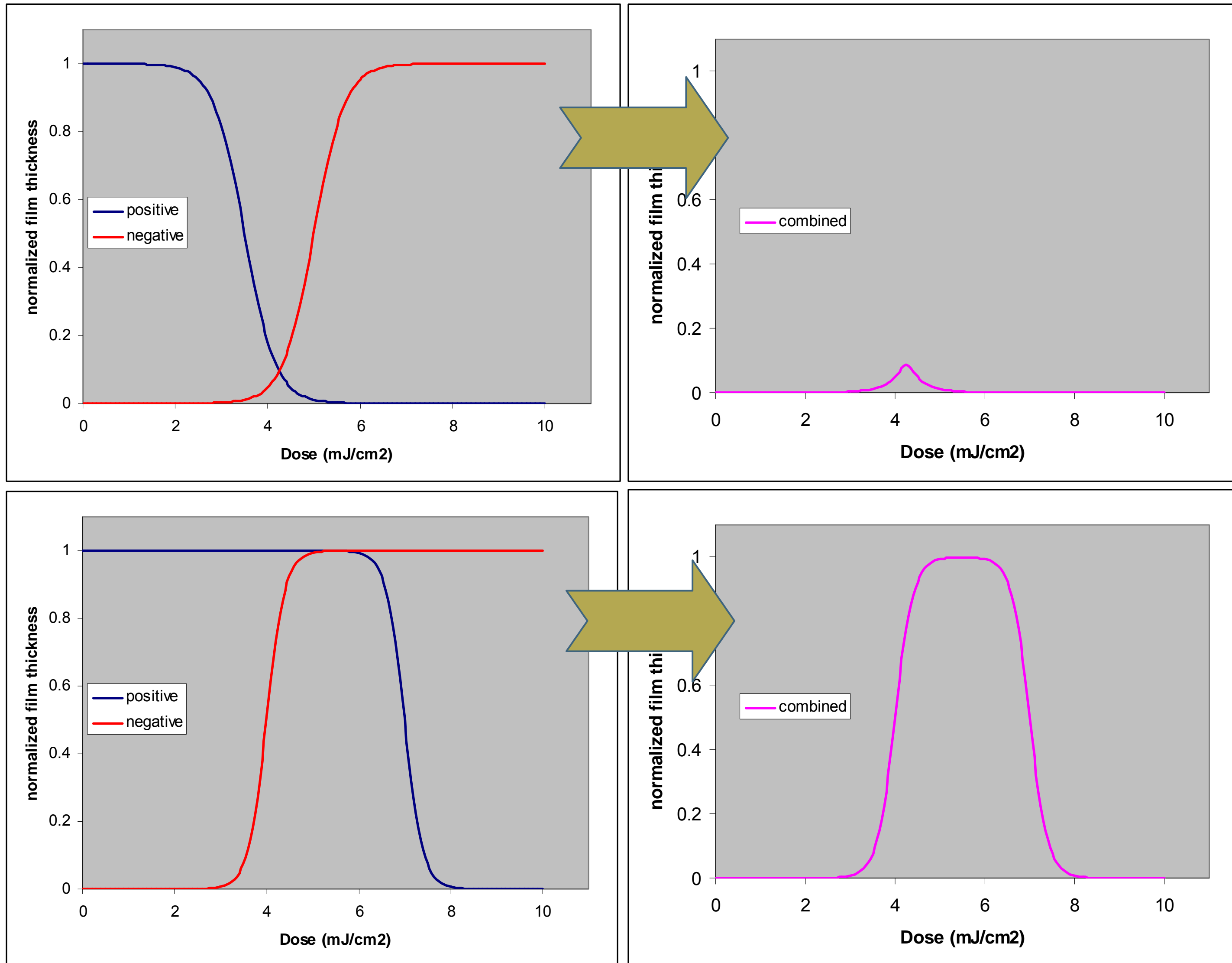
- Self Aligned double patterning



- Dual Tone development



Dual Tone Development Challenge: Need to match sensitivities



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Dual Tone development

On PAS5500/1100 (0.75NA)

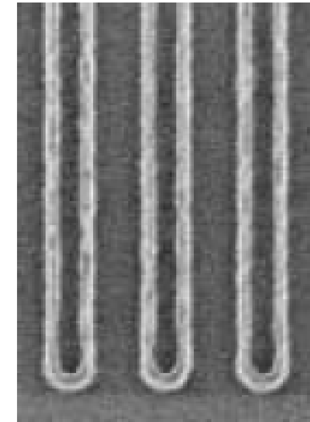
Negative + Positive development

E= 12.00 | 12.25 | 12.50 | 13.00 | 13.50 | 14.00 | 14.50 mJ/cm²

E= 18.00 | 17.50 | 17.00 | 16.50 | 16.00 | 15.50 | 15.00 mJ/cm²

400nm

Line ends:



14.6mJ/cm²

FUJIFILM

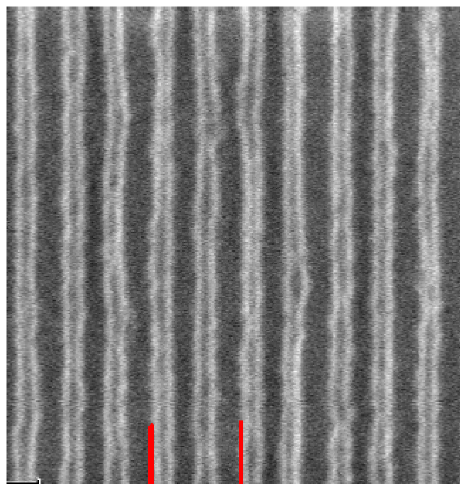
Ref. SPIE 6923-14, S. Tarutani et al.

1st results Dual Tone Development $k1<0.25$

$k_1=0.23$

60nm HP at 0.75NA

Pitch 240nm

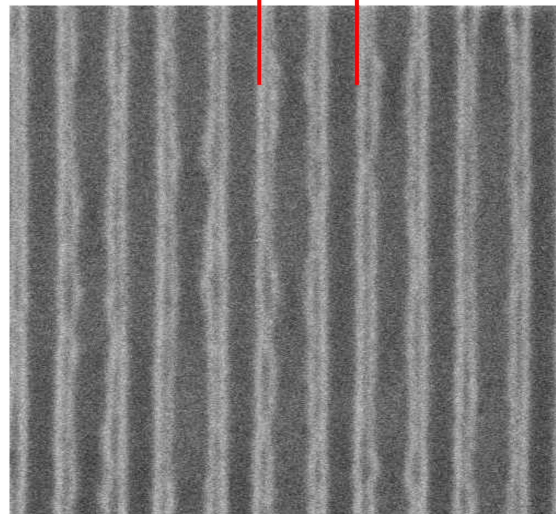


240nm

$k_1=0.22$

50nm HP at 0.85NA

200nm



Potential for further resolution improvements of the process

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outline

- LELE
  - double line process for Active/Poly
    - CDU
    - overlay
  - double trench process for M1
  - alternative processes (CoO)

- SADP
  - 32nm HP process
    - CDU
  - alternative process (CoO)

- Conclusions

Conclusions

- LELE
  1. The obtained results demonstrate that LELE double patterning will be able to meet the specs for 32nm half pitch critical layers, using state-of-the-art scanners.
  2. Very promising alternative processes are coming up to improve the costs and logistics for DPT

- SADP
  1. Very powerful for excellent CD control and not sensitive to interlayer alignment
  2. Placement accuracy of the lines requires champion dose control
  3. Dual tone development needs to be accelerated to reduce the cost of SADP (many process steps)

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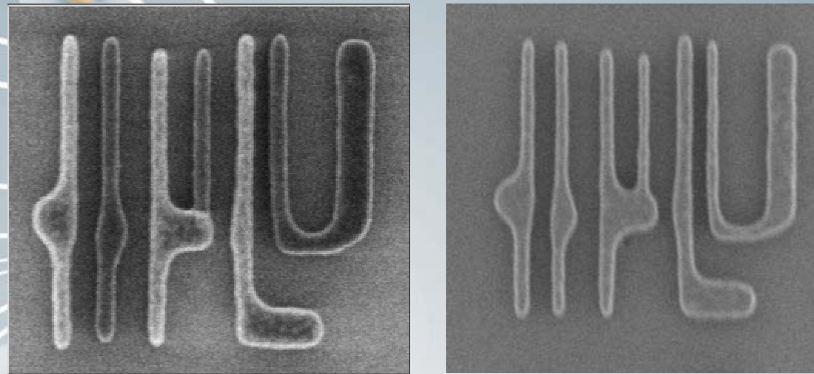
Thank you!



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