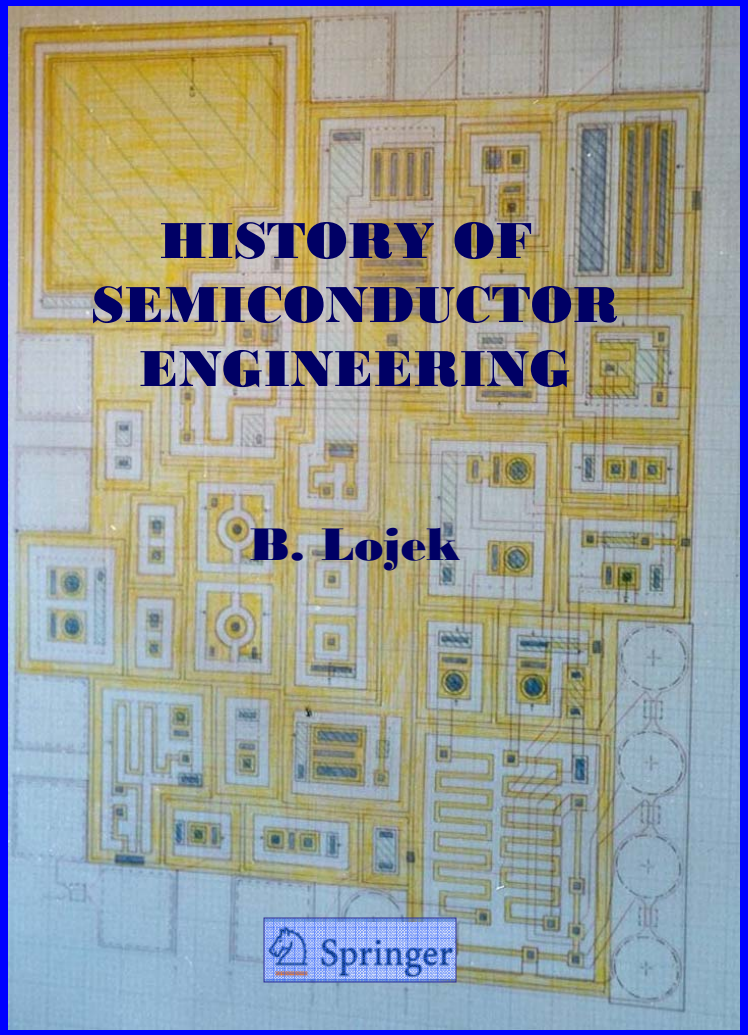
HISTORY OF SEMICONDUCTOR ENGINEERING

Bo Lojek
ATMEL Corporation
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
blojek@atmel.com



Layout of Fairchild's analog integrated circuits prepared by Dolores Talbert

(Circa 1963)

History of Semiconductor Engineering

Lojek, Bo
2006, Approx. 330 p. 222 illus., 2 in color.,
Hardcover ISBN: 3-540-34257-5

Available: August 2006 (www.springer.com)

CONTENTS

WE HAVE BEEN TOLD THAT KILBY OF TI AND NOYCE OF FAIRCHILD DID IT. THEN, WHY SHOULD THERE BE ANOTHER BOOK ABOUT THE HISTORY OF SEMICONDUCTORS?

BECAUSE WE HAVE NOT BEEN TOLD THE TRUTH!

"Who controls the past controls the future. Who controls the present controls the past."

George Orwell, 1948

WHY DID YOU NOT HEAR FROM THE PEOPLE WHO DID IT?

BECAUSE CREATIVE ENGINEERS ARE

- PEOPLE WITH A STRONG SENSE OF PERSONAL LIBERTY
- STRONG INDIVIDUALS WHOSE ACTIONS NEVER INCLUDE ACTING
- INDIVIDUALS WITH STRANGE INCLINATIONS OF THEIR OWN THAT THEY ARE NOT AFRAID TO EXPRESS AND ON WHICH THEY REFUSE TO COMPROMISE
- PEOPLE WHO ARE NOT LOOKING FOR RECOGNITION AND AWARDS

NOTE THAT THESE TRAITS ARE NOT COMPATIBLE WITH THE SO-CALLED CAREER PATH

FROM THE LETTER TO THE AUTHOR:

"You and I agree that, while the world loves a hero, semiconductor progress depended on the efforts and ideas of a large number of people, and that moving forward depended on contributors going back a few decades in some cases. Also, as is the case with most inventions, a number of people with access to the same pool of common knowledge were working independently at the same time to put it all together and to make the necessary extensions to the existing technology and who realized that the time was right for society to accept the new concepts."

Dr. Jay Last

Former Shockley Laboratories employee, co-founder of Fairchild Semiconductor, co-founder of Amelco Semiconductor, and manager of the Fairchild's group which designed and produced the world's first planar integrated circuit

SEMI-CONDUCTOR RESEARCH AT PURDUE UNIVERSITY [1942-1948]

National Defense Research Committee

Office of Scientific Research and Development

Division 14

Report NDRC 14-585

Contractor's Final Report

Purdue University
Department of Physics

on

PREPARATION OF SEMI-CONDUCTORS AND DEVELOPMENT

OF CRYSTAL RECTIFIERS

by

K. Lark-Horovitz

Covering the Period from March 1942 to November 1945

Title Page
136 Numbered Pages
30 Figures
1 Plate

OSRD Contract OEMsr-
Division 14, NDRC
Report No. 14-585

Lark-Horowitz, W. Hansen, D. Kerst
W. Pauli, J. Schwinger, E. Condon, J. Becker.
Purdue University, 1942

Proceedings of the American Physical Society

MINUTES ON THE MEETING AT MONTREAL, JUNE 19-21, 1947

Spreading Resistance **Discrepancies and Field Effects in Germanium.*** RALPH BRAY, K. LARK-HOROVITZ, AND R. N. SMITH, Purdue University. *Contact* and spreading resistance determine the forward resistance of metal-Ge point-contact rectifiers. Theoretically the spread-ing resistance is *p/2d;* p-semiconductor resistivity, d-contact diameter. Above one volt the contact resistance contribution is negligibleand the spreading resistance is then given by the slope of the current-voltage characteristic. However, the spreading resistance so determined on high resistivity (p~1 ohm-cm) n-type Ge decreases with in-creasing voltage and is lower by factor ten or more than the valuepredicted from bulk resistivity. The high current densities through the contact (~10 ma through 10-**6** cm2) suggest the possibility of field effects. Actually, the bulk resistivity (studied with exponential and constant current pulses) is field dependent and starts to decrease at fields of 100 volts/cm. The time constant of the field effects may be estimated from the progressive increase of spreading resistance with frequency

(about 100 Kc). Calculations were made relating at least qualitatively the spreading resistance discrepancies with field dependence measure-ments of bulk resistivity.

* This work was started under OSRD contract and is continued under Signal Corps contract.

f Now at Boeing Aircraft. Seattle, Washington.

' Experiments also show saturation of spreading resistance with increased load and contact area (R. E. Davis).

'H. J. Yearian. "Dependence of Forward Conductance and Back Resistance of High Back Voltage Germanium on Voltage and Fre-quency." NDRC report October, 1945.

Proceedings of the American Physical Society

MINUTES OF THE MEETING AT CHICAGO, NOVEMBER 25 AND 26, 1949

Dependence of the Germanium High Back Voltage Rectifier Resistance on Frequency.* R. BY AND H. J. YEARIAN, Purdue University. Germanium high back voltage rectifier units show anomalously poor rectification at high fre-quency. Detailed investigation,' involving measurement of the rectified d.c. current for voltages of frequencies from 60 cycles to 60 mc showed the forward resistance to increase with fre-quency *f,* for f100 kc. The effect is small at low voltage, increases with voltage and becomes almost constant above 0.6 volts r.m.s. where predominantly spreading resistance deter-mines the current. The effective back resistance at 1000 cycles and 30 mc were compared. It was found to be lower at 30 mc only when there was a forward swing to the applied voltage, otherwise it was higher. An interpretation is suggested in tern's of the motion in the high frequency field of the holes injected into the germanium from the point contact. Thus for *f2/r,* (r is lifetime of the holes), a decrease in the depth of penetra-tion of the holes results which increases the spreading re-sistance. The back resistance can be decreased by the return to the contact, and the collection there, of the holes injected during the forward swing of the voltage.

* Work partially assisted by Signal Corps Contract.

' H. J. Yearian, "Dependence of forward conductance and back resistance of high back voltage germanium on voltage and frequency," NDRC Report (October 1945).

BELL LABS' POINT CONTACT TRANSISTOR WOULD NOT HAVE WORKED IF J. BARDEEN HAD NOT ADVISED W. BRATTAIN TO USE HIGH BACK VOLTAGE GERMANIUM.

KILBY vs. JOHNSON

H. JOHNSON, 1953

2,816,228

SEMICONDUCTOR PHASE SHIFT OSCILLATOR AND DEVICE

Harwick Johnson, Princeton, N. J., assignor to Radio Corporation of America, a corporation of Delaware

Application May 21, 1953, Serial No. 356,407

10 Claims. (Cl. 250—36)

In the electron tube art, it is well known that a tube may be operated, in a suitable circuit, as a phase-shift oscillator. In such circuits, a resistance-capacity phase shifting network is connected between the output and the input of an amplifier tube, the circuit being proportioned to provide a 180° phase shift at the desired oscillation frequency. In accordance with the invention, a transistor may be similarly operated in such an external phase-shifting circuit. Also in accordance with a preferred embodiment of the invention, a semiconductor phase-shift oscillator is incorporated in a unitary body whereby much of the circuitry of the conventional phase-shift oscillator is eliminated.

The capacitance of a P-N junction biased in the reverse direction may be determined from the formula:

$$C=\frac{KA}{4\pi W}$$

wherein:

K=dielectric constant of the semiconductor material
W=thickness of the P-N junction
A=cross-section area of the P-N junction

The capacitance of a P-N junction biased in the forward direction may be determined from the formula:

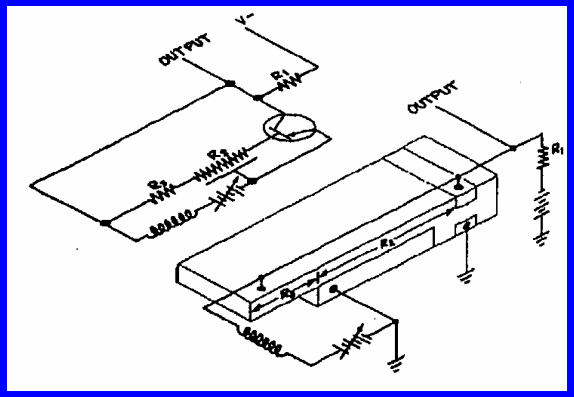
$$C=\frac{qL^2I}{kT4D}$$

wherein

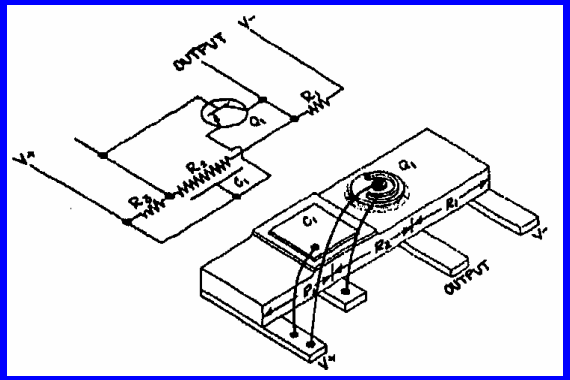
q=magnitude of electron charge
L=diffusion length of minority carriers
k=Boltzmann's constant
T=temperature in degrees Kelvin
D=diffusion constant
I=current

The resistance of a piece of semiconductor material may be determined from the formula:

$$R=\frac{rL}{A}$$



J.S. KILBY, 1959



3,138,743

MINIATURIZED ELECTRONIC CIRCUITS

Jack S. Kilby, Dallas, Tex., assignor to Texas Instruments Incorporated, Dallas, Tex., a corporation of Delaware

Filed Feb. 6, 1959, Ser. No. 791,602
25 Claims. (CL 317—101)

It is, therefore, a principal object of this invention to provide a novel miniaturized electronic circuit fabricated from a body of semiconductor material containing a diffused p-n junction wherein all components of the electronic circuit are completely integrated into the body of semiconductor material.

As will be apparent to one skilled in the art, ohmic connections are those which exhibit symmetry and linearity in resistance to flow of current therethrough in any available direction. If two resistors are to be connected together, it is not necessary to provide separate terminations for the common point. The resistance may be calculated from

$$R=\rho L/A$$

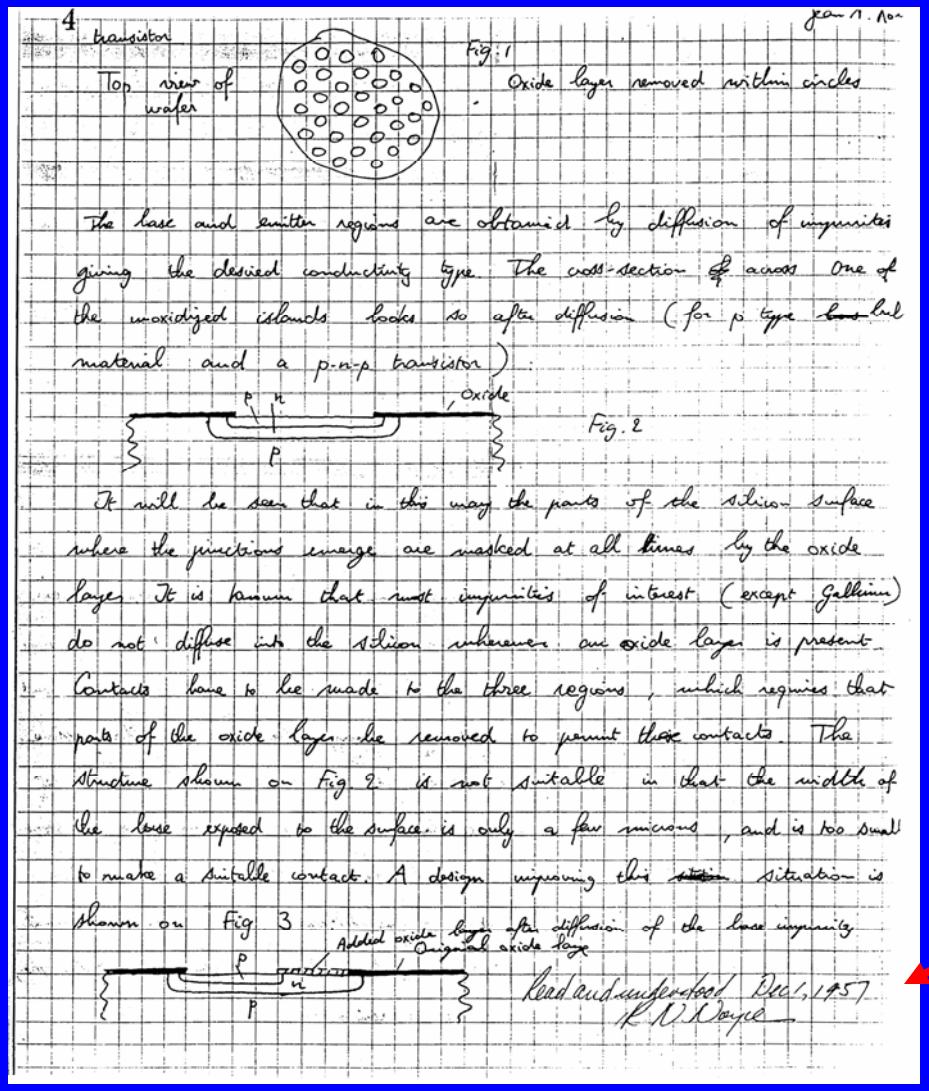
where L is the active length in centimeters, A is the cross sectional area, and ρ is the resistivity in ohm-cm. of the semiconductor material.

Capacitor designs may be obtained by utilizing the capacitance of a p-n junction, as shown in FIGURE 2, wherein a semiconductor wafer 15 of p-type conductivity is shown containing an n-type diffused layer 16. Ohmic contacts 17 are made to opposite faces of the wafer 15. The capacitance of a diffused junction is given by

$$C=A\epsilon\left(\frac{qa}{12\epsilon V}\right)^{1/3}$$

where A is the area of the junction in square cm., ϵ is the dielectric constant, q is electronic charge, where a is the impurity density gradient, and V is the applied voltage.

NOYCE vs. HOERNI and LAST



4

transistor

Top view of wafer

Fig. 1

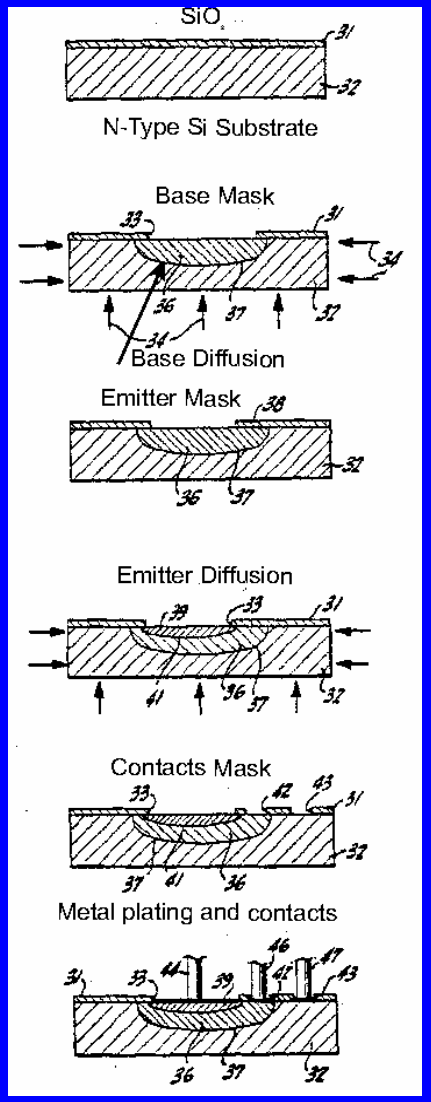
Oxide layer removed within circles

The base and emitter regions are obtained by diffusion of impurities giving the desired conductivity type. The cross-section of across one of the oxidized islands looks so after diffusion (for p type base material and a p-n-p transistor):

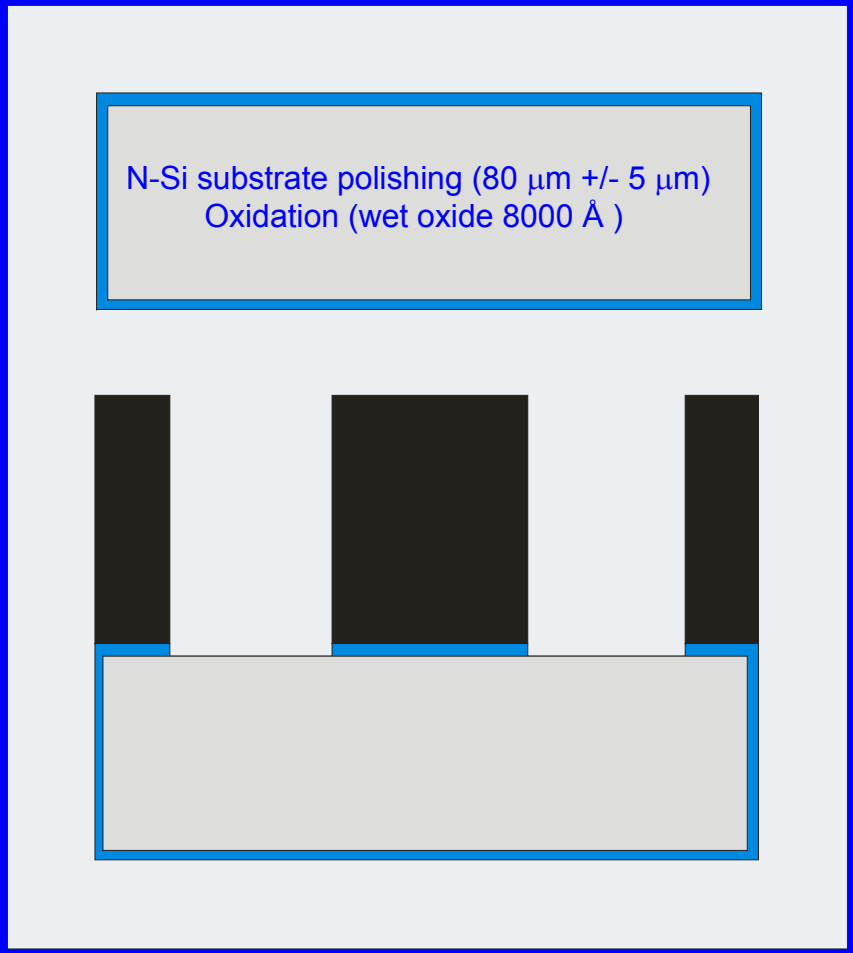
Fig. 2

It will be seen that in this way the parts of the silicon surface where the junctions emerge are masked at all times by the oxide layer. It is known that most impurities of interest (except Gallium) do not diffuse into the silicon wherever an oxide layer is present. Contacts have to be made to the three regions, which requires that parts of the oxide layer be removed to permit these contacts. The structure shown on Fig. 2 is not suitable in that the width of the base exposed to the surface is only a few microns, and is too small to make a suitable contact. A design imposing this situation is shown on Fig 3

Read and understood Dec 1, 1957
R N Noyce



THE WORLD'S FIRST PLANAR INTEGRATED CIRCUIT
[Fairchild Semiconductor, May – October 1960]



Group:

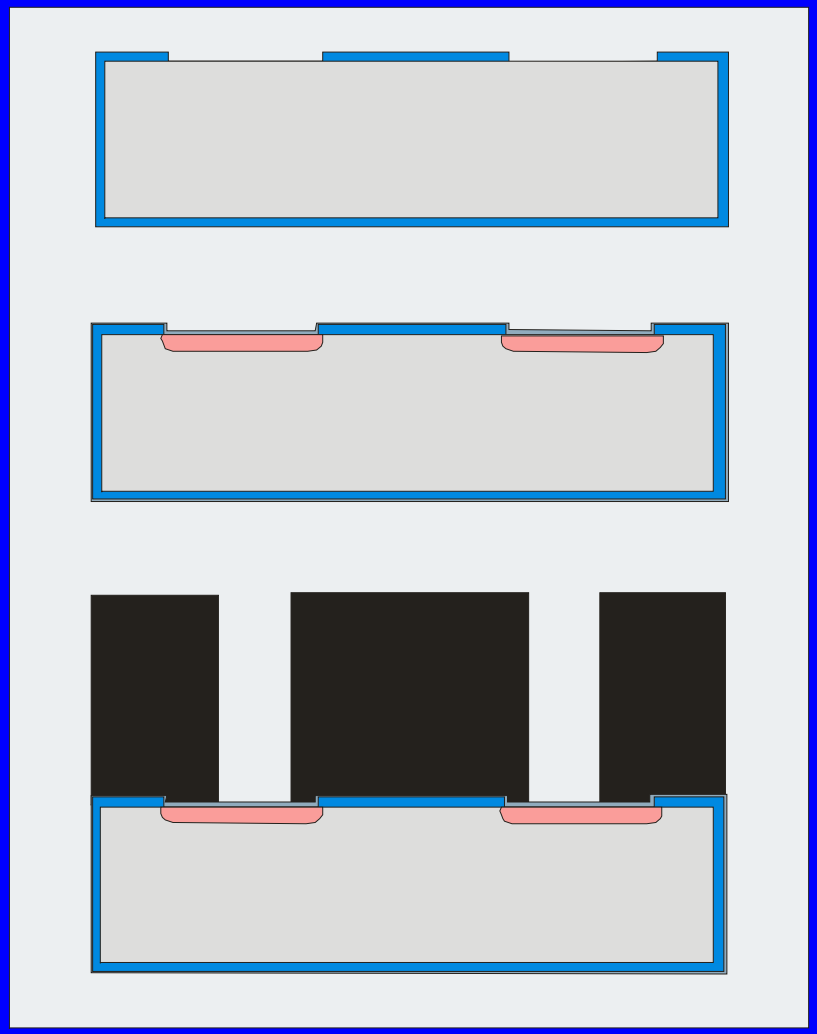
J. Last, *Group Manager*

L. Kattner – Concept & Assembly
I. Haas – Diffusion & Test
J. Nall – Masks Alignment
S. M. Fok – Wax bonding
G. Tripp
R. Marlin
C. Gunter
J. Wilkerson
J. Lessard
M. Hoar

R. Norman – Circuit Design
(Application Department)

BASE MASK
(Base and P-Resistor)

THE WORLD'S FIRST PLANAR INTEGRATED CIRCUIT
[Fairchild Semiconductor, May – October 1960]

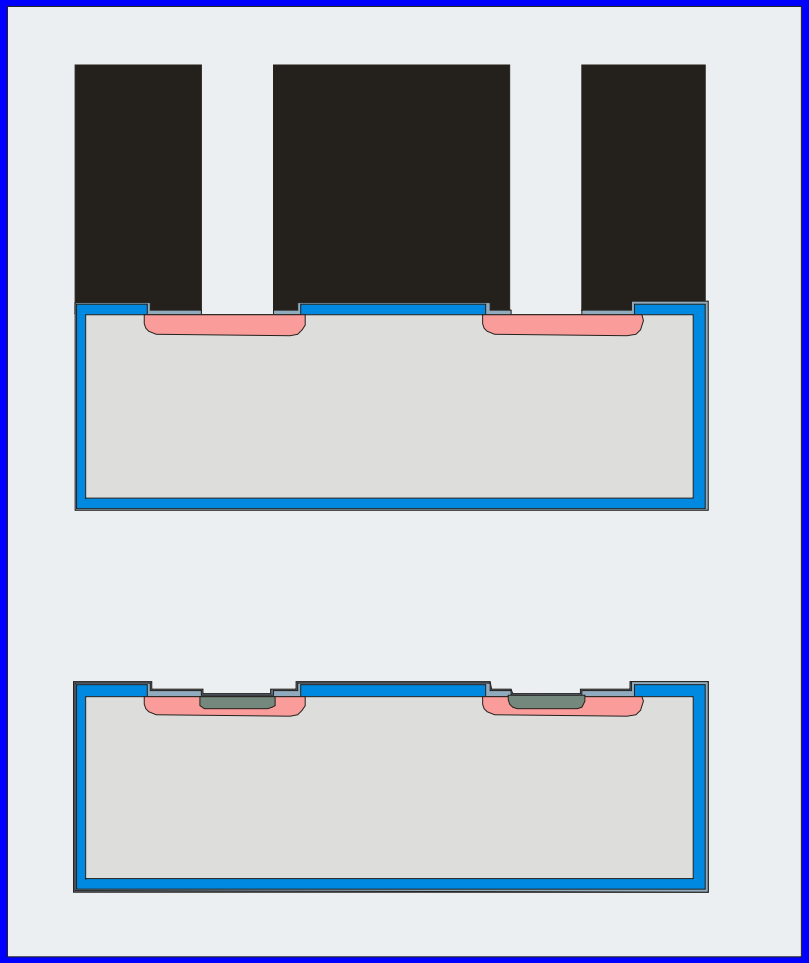


Wet Etch Oxide in Base Region

Base Pre-deposition and Drive-in
(~ 6000 Å oxide, ~150 Ω/sq)

EMITTER MASK
(Emitter and Collector Contacts)

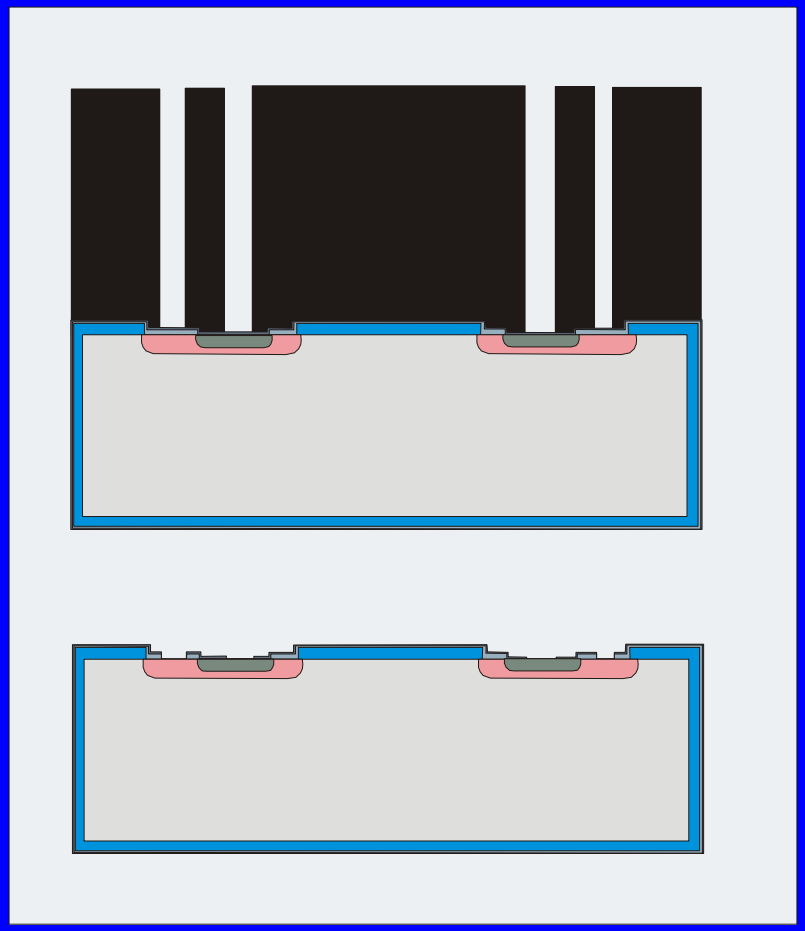
THE WORLD'S FIRST PLANAR INTEGRATED CIRCUIT
[Fairchild Semiconductor, May – October 1960]



Wet Etch Oxide in Emitter Region

Emitter Pre-deposition and Drive-in

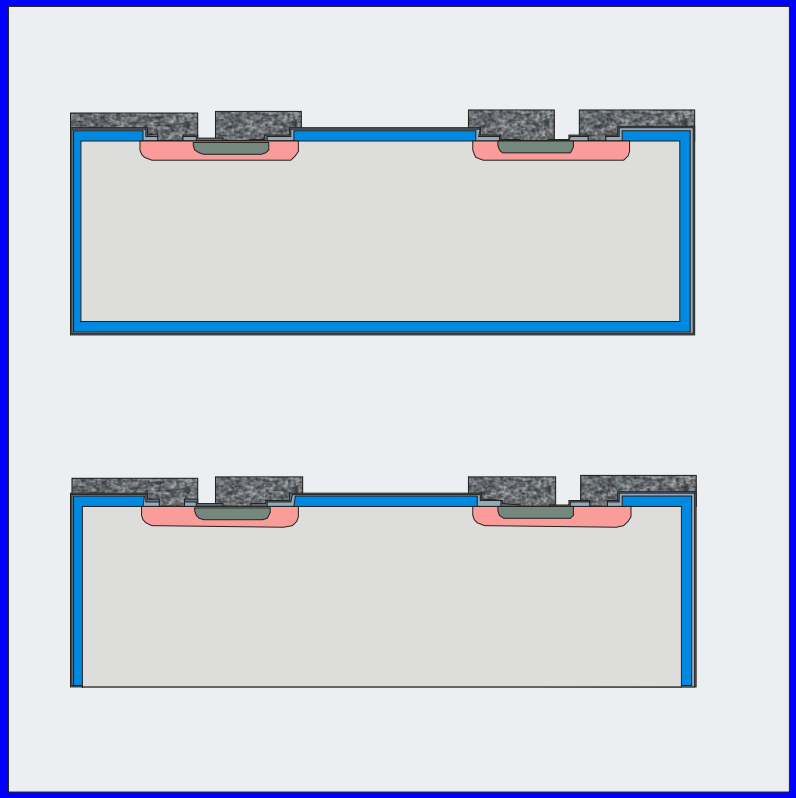
THE WORLD'S FIRST PLANAR INTEGRATED CIRCUIT
[Fairchild Semiconductor, May – October 1960]



CONTACT MASK

Base and Emitter Contacts windows after resist strip

THE WORLD'S FIRST PLANAR INTEGRATED CIRCUIT
[Fairchild Semiconductor, May – October 1960]



Evaporate Aluminum , 0.01 Ω/sq

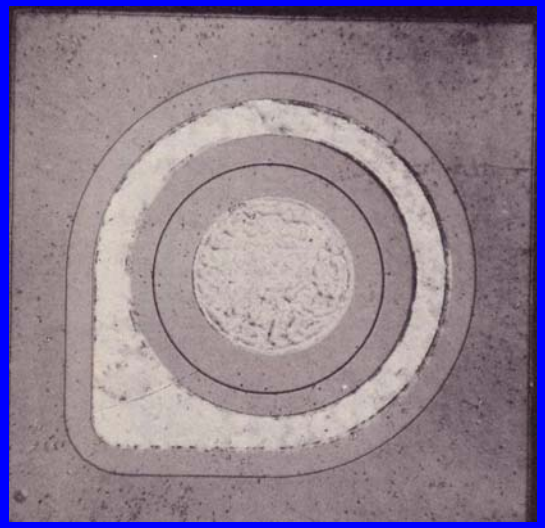
CONTACT MASK

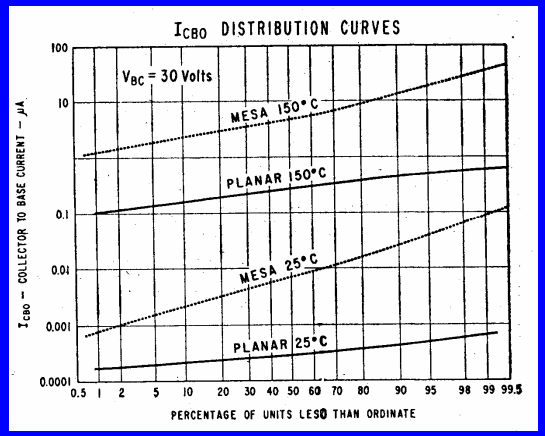
Wet etch metal (25 % solution sodium hydroxide)
Metal alloying (~ 600 °C/ Argon)

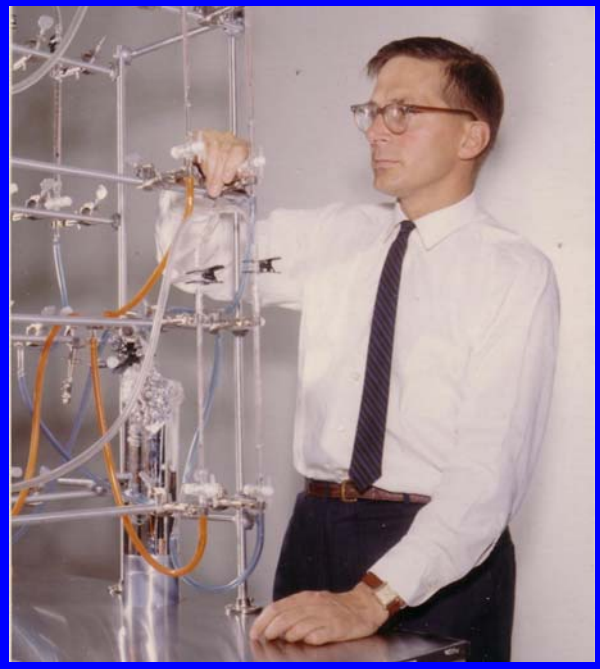
PLANAR TRANSISTOR

Wet etch oxide (back side only)
Vacuum Evaporation of Gold on the back side (~ 400 Å)
Gold Diffusion (~ 1050 °C/ ~ 15 min with fast cool)

HOERNI'S PLANAR VERSION OF 2N656 MESA TRANSISTOR [August 1960]



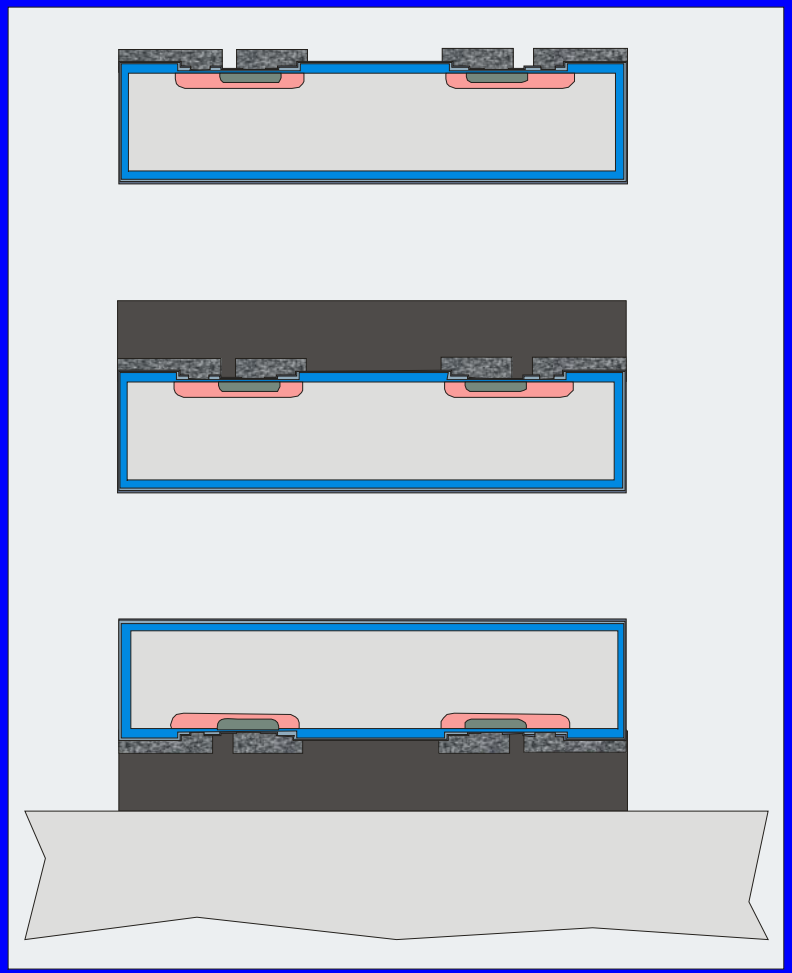




JEAN HOERNI

September 26 , 1924 - January 12 , 1997

THE WORLD'S FIRST PLANAR INTEGRATED CIRCUIT
[Fairchild Semiconductor, May – October 1960]

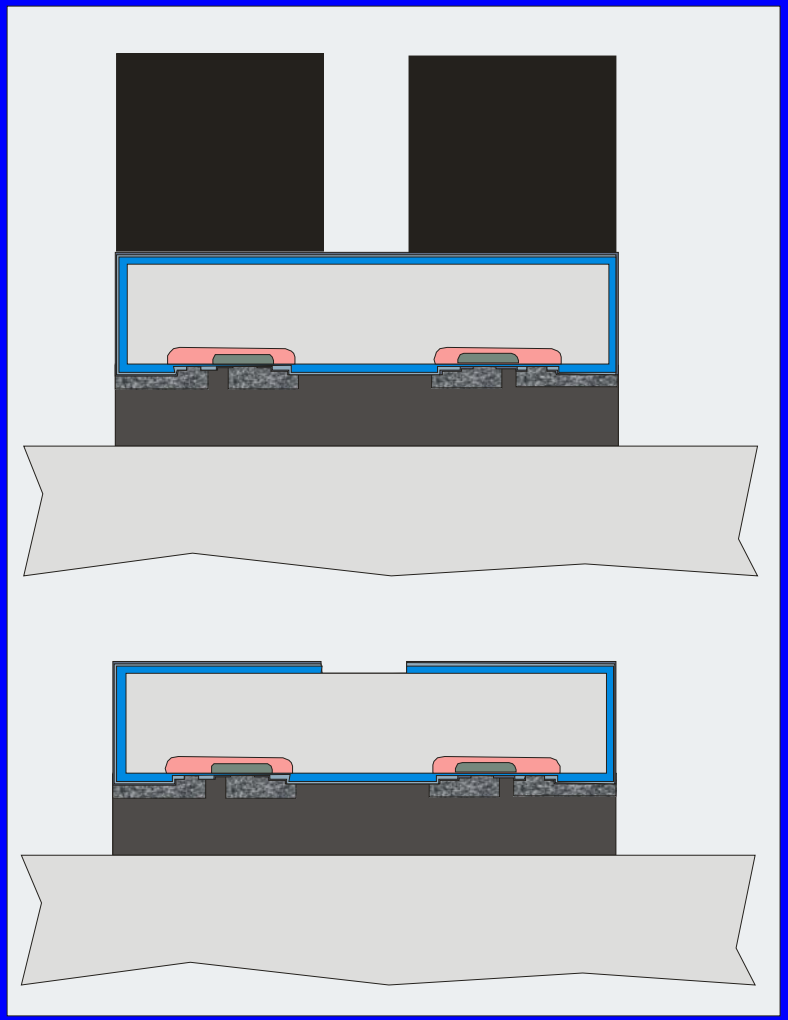


NO REMOVAL OF OXIDE ON THE BACK SIDE FOR ICs

Bonding Wax
- sugar (melting point 186 ^{o}C)
- APIEZON Wax

Glass Plate Wafer Support
(Front side of the wafer bonded to the Glass plate)

THE WORLD'S FIRST PLANAR INTEGRATED CIRCUIT
[Fairchild Semiconductor, May – October 1960]

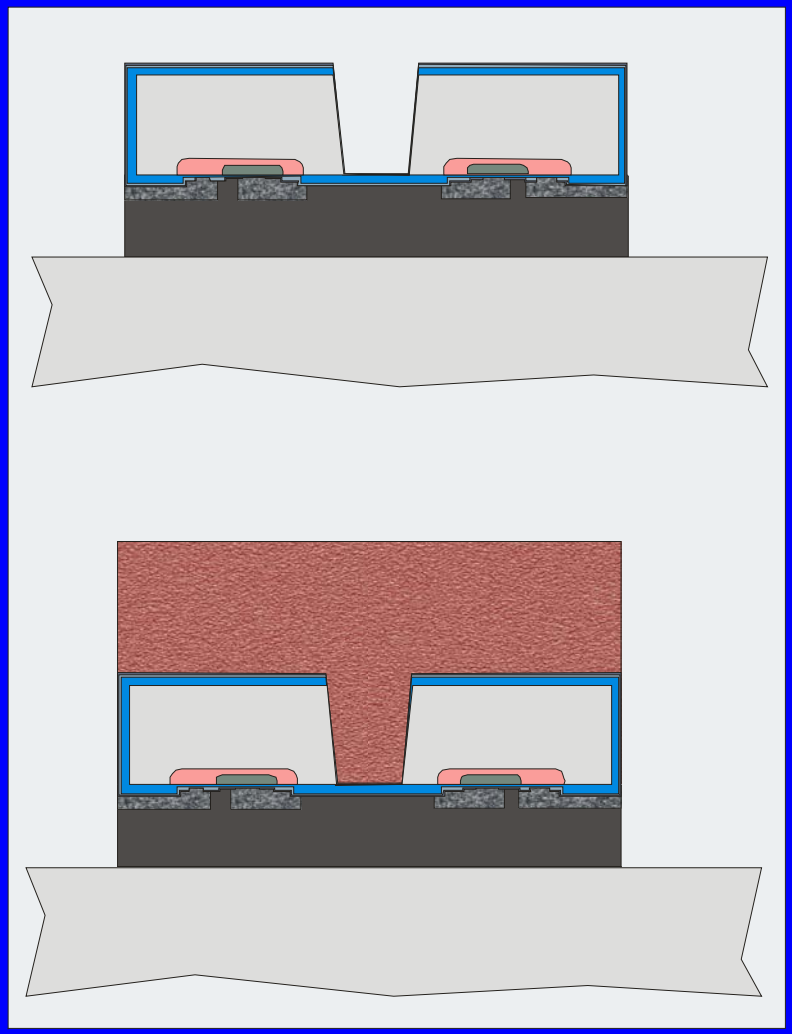


ISOLATION MASK
(Applied to the back side of the wafer)

Wet etch oxide (back side only)

Strip resist

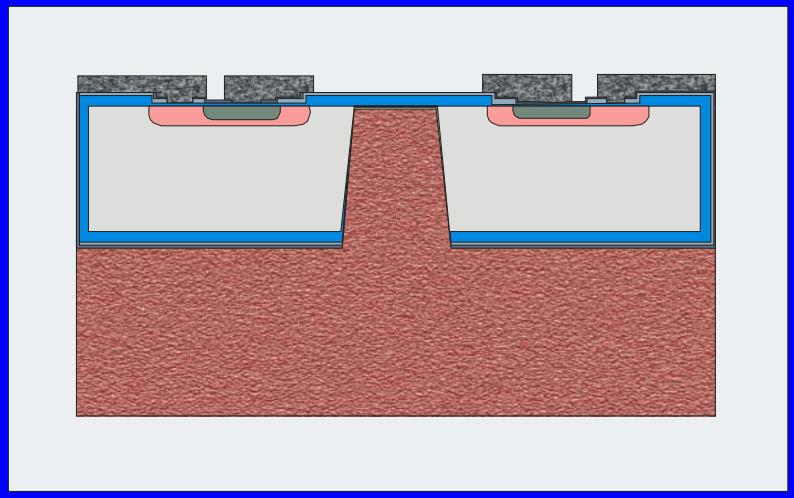
THE WORLD'S FIRST PLANAR INTEGRATED CIRCUIT
[Fairchild Semiconductor, May – October 1960]



Wet etch Silicon (stop on oxide)

Epoxy fill

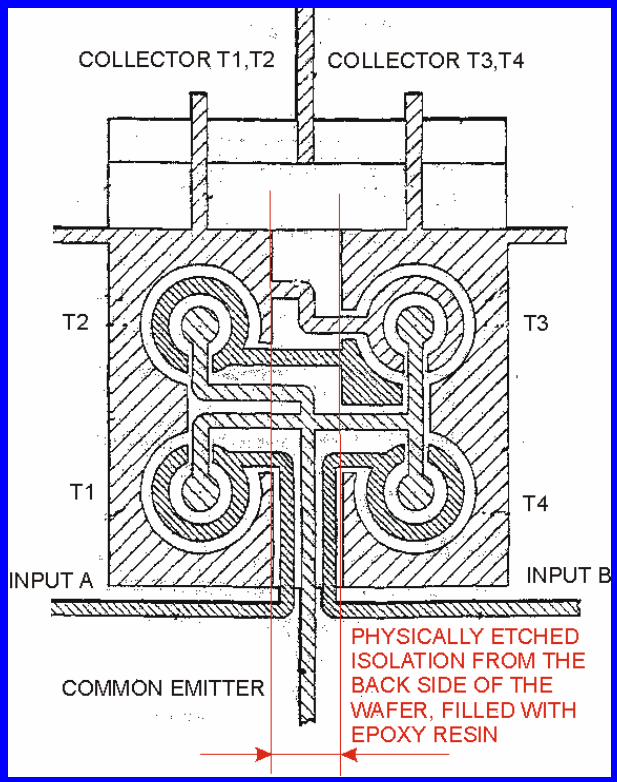
THE WORLD'S FIRST PLANAR INTEGRATED CIRCUIT
[Fairchild Semiconductor, May – October 1960]



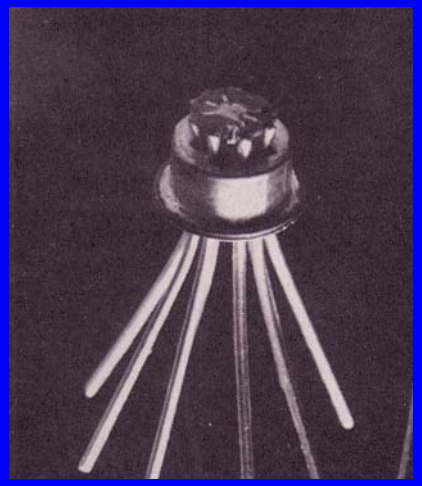
Remove Glass Plate and Bonding Wax

By November 1960 the yield was 5%.

The world's first planar integrated circuit produced by Jay Last, Lionel Kattner, and Isy Haas [Fairchild Semiconductor functional units were demonstrated in May 1960]



The First Fairchild Publication describing the Planar ICs:



FRIDAY, FEBRUARY 12, 1960 Irvine Auditorium
9:00 A.M.-12:00 Noon
SESSION VII: Microelectronic Considerations
7.4: **Solid-State Micrologic Elements**
R. NORMAN, J. LAST AND I. HAAS
Fairchild Semiconductor Corporation Palo *Alto, Calif.*

The advertisement for Micrologic Flip-Flop [Electronic News, May 8, 1961]

FAIRCHILD R&D MONTHLY REPORT (January 9, 1961)

INTER-DEPARTMENTAL CORRESPONDENCE

FAIRCHILD
SEMICONDUCTOR CORPORATION

TO: R. N. Noyce CC: DATE: January 9, 1961

SUBJECT: Research & Development
Progress Report - 1/1/61

FROM: G. E. Moore and
V. H. Grinich

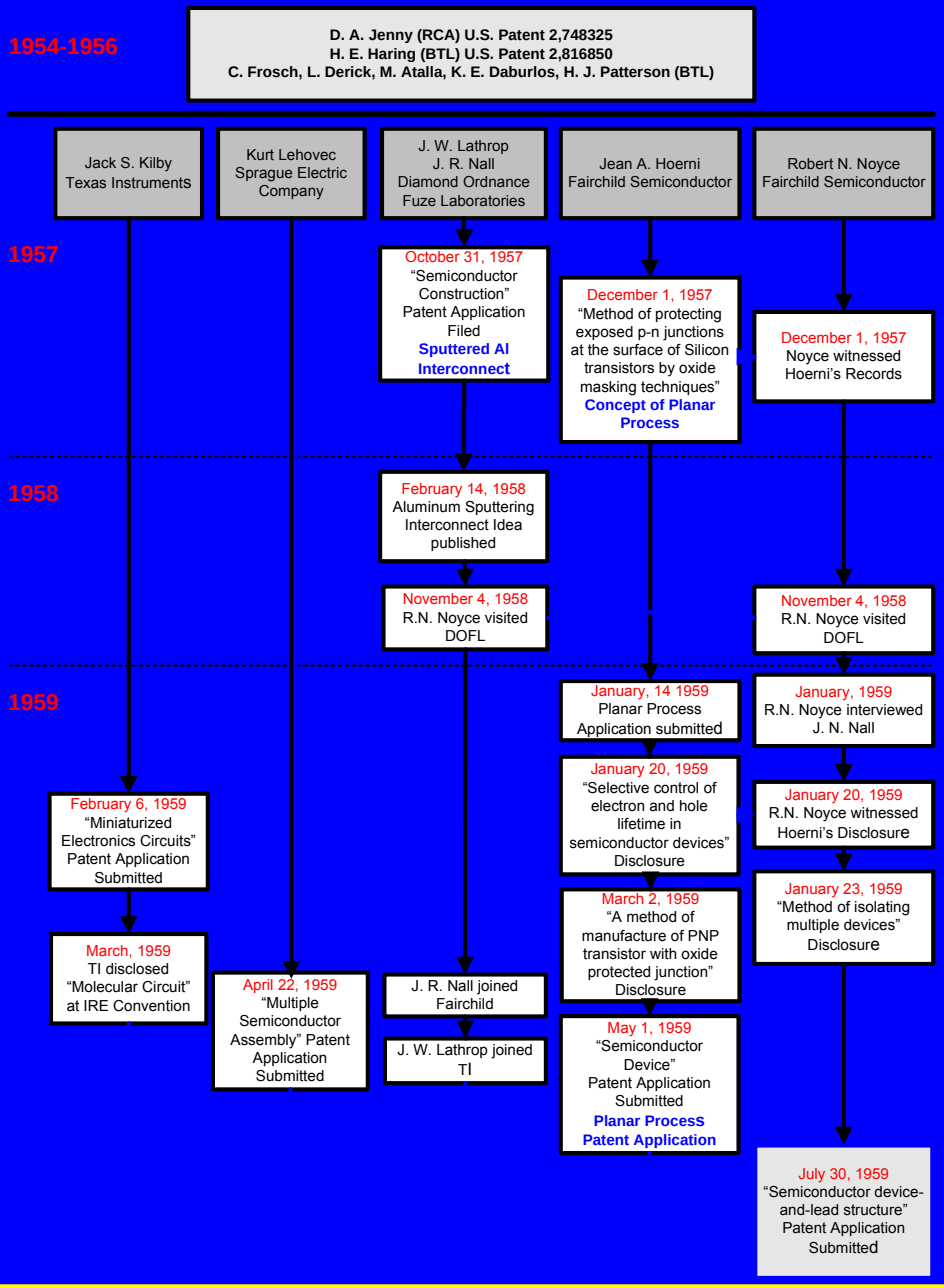
Progress Report - R&D -- 1/1/61
Page 2 January 9, 1961

Micrologic:

The first several flip-flops with the new pattern completely isolated by diffusion were mounted during the first week of January. These operate at 4 mc's and early estimates suggest they will have useful fan-out over most of the temperature range. Several more runs right behind these suggest that January will produce several thousand flip-flops. This is enough that we should be able to determine finally if we have a useful device or not. ~~I am~~ We are still somewhat skeptical.

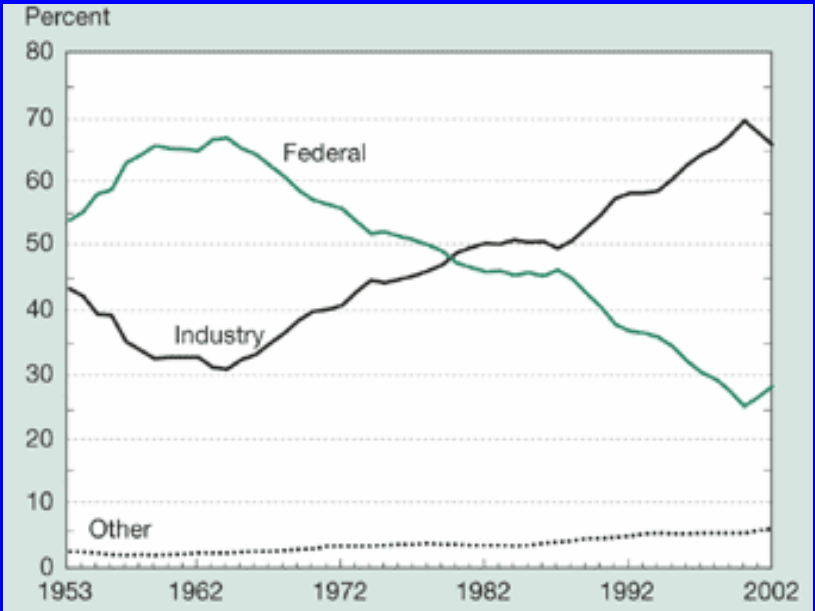
G. E. Moore/V. H. Grinich

GEM/VHG:hb/jj


1954-1956
D. A. Jenny (RCA) U.S. Patent 2,748325
H. E. Haring (BTL) U.S. Patent 2,816850
C. Frosch, L. Derick, M. Atalla, K. E. Daburlos, H. J. Patterson (BTL)
Jack S. Kilby
Texas Instruments
Kurt Lehovec
Sprague Electric Company
J. W. Lathrop
J. R. Nall
Diamond Ordnance Fuze Laboratories
Jean A. Hoerni
Fairchild Semiconductor
Robert N. Noyce
Fairchild Semiconductor
1957
October 31, 1957
"Semiconductor Construction"
Patent Application Filed
Sputtered Al Interconnect
December 1, 1957
"Method of protecting exposed p-n junctions at the surface of Silicon transistors by oxide masking techniques"
Concept of Planar Process
December 1, 1957
Noyce witnessed Hoerni's Records
1958
February 14, 1958
Aluminum Sputtering Interconnect Idea published
November 4, 1958
R.N. Noyce visited DOFL
November 4, 1958
R.N. Noyce visited DOFL
1959
January, 14 1959
Planar Process Application submitted
January, 1959
R.N. Noyce interviewed J. N. Nall
January 20, 1959
"Selective control of electron and hole lifetime in semiconductor devices"
Disclosure
January 20, 1959
R.N. Noyce witnessed Hoerni's Disclosure
February 6, 1959
"Miniaturized Electronics Circuits"
Patent Application Submitted
March 2, 1959
"A method of manufacture of PNP transistor with oxide protected junction"
Disclosure
January 23, 1959
"Method of isolating multiple devices"
Disclosure
March, 1959
TI disclosed "Molecular Circuit" at IRE Convention
April 22, 1959
"Multiple Semiconductor Assembly"
Patent Application Submitted
J. R. Nall joined Fairchild
J. W. Lathrop joined TI
May 1, 1959
"Semiconductor Device"
Patent Application Submitted
Planar Process Patent Application
July 30, 1959
"Semiconductor device-and-lead structure"
Patent Application Submitted

No one remembers even a few years ago!
George Orwell. No memory! Who is that guy?

Michael Crichton, State of Fear, 2004



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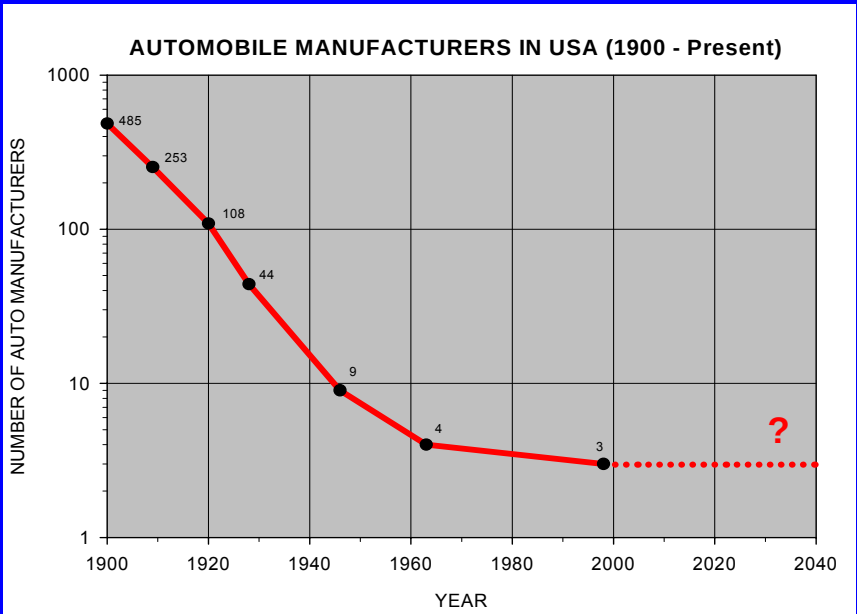


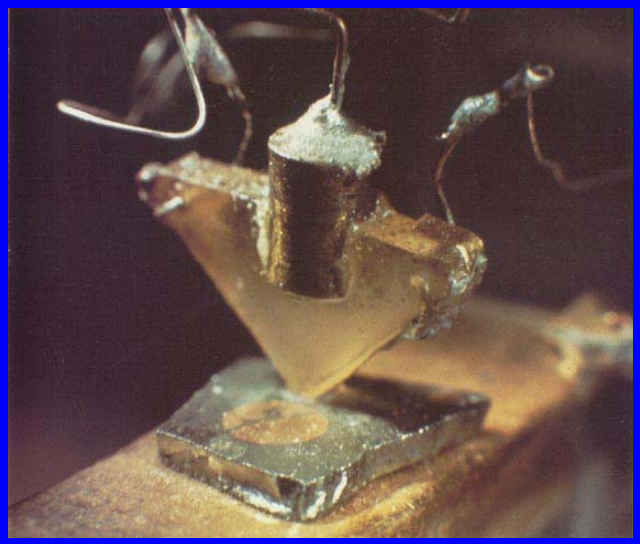
National R&D expenditures 1953-2002 [Source: National Science Foundation 2004]

Automobile Manufacturers in U.S. (1900 – Present)

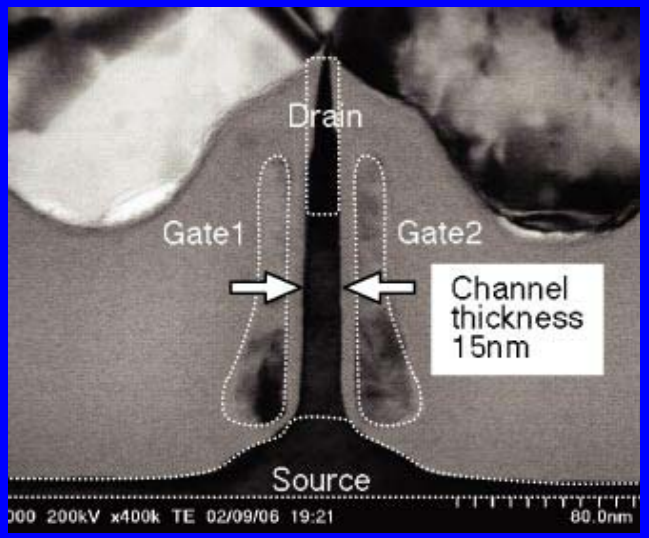
THANK YOU AND GOOD NIGHT!

DEAR NSF,
SINCE JUNE 1945, WHEN MARVIN KELLY ISSUED THE "AUTHORIZATION FOR WORK" AT BELL LABS, WE HAVE CREATED MANY OF THE "WORLD'S FIRSTS". NOW, SOME NATIONS ARE AHEAD OF US. IF YOU ARE A PATRIOT AND CARE ABOUT THE FUTURE OF THIS NATION, DO WHAT IS RIGHT – FUND THE nanoHUB PROJECT!
THANK YOU.

THE WORLD FIRST TRANSISTOR (USA)



THE WORLD'S SMALLEST TRANSISTOR (JAPAN)



Cross-sectional TEM image of the fabricated world's thinnest vertical double-gate MOSFET with a wall channel thickness of 15nm
[AIST Tokyo, 2006]