# *Manufacturing mechatronics using thermal spray shape deposition*

**James E. Beck, Fritz B. Prinz, Daniel P. Siewiorek, Lee E. Weiss**

**Engineering Design Research Center**
**Carnegie Mellon University**

## *Abstract*

A new technology for manufacturing mechatronics is described. The technique is based on recursive masking and deposition of thermally sprayed materials. Using these methods, mechanical structures can be created that embed and interconnect electronic components. This results in highly integrated mechatronic devices. A simple, electromechanical artifact was designed and produced to assess the feasibility of these techniques. The details and limitations of this project will be discussed. Areas of future research are identified which are aimed at realizing the full potential of this emerging manufacturing process.

Keywords: Mechatronics, Thermal Spray.

## *Introduction*

The phrases "solid freeform fabrication" and "shape deposition" are synonymous. They refer to the process of creating a physical artifact by incrementally and selectively depositing material in thin, 2-1/2 dimensional layers. Shape deposition can be done in many ways. Most methods, however, have focused on single material applications. The MD* process [1,2,3] is a thermal spray shape deposition system. In this process, thermal spray methods (i.e. plasma, electric arc, or combustion) are used to deposit thin, planar layers of material. Each of these layers is carefully shaped using disposable, laser generated masks. The artifact being produced is grown as a succession of thermally sprayed, cross-sectional layers within a sacrificial support structure.

The MD* process is driven by a 3-D CAD model of the artifact being produced. This model provides a complete spacial representation of the part, and is generated using the NOODLES CAD environment [4]. Next, the CAD model is sliced, and the slices are used to generate files that control the laser mask cutting station [7]. Each mask that is generated corresponds to a slice of the CAD model. A semi-automated version of the MD* process has been implemented which includes two stations: a laser mask cutting station and a thermal (electric arc) spray station. Masks are manually transferred between stations. This system was used to create a prototype turbine blade shape which established these techniques in the mechanical domain.

The MD* masking system also allows selective material deposition within each layer. As a result, multi-material artifacts can be produced in an integrated fashion using a single process. This type of artifact represents a much broader class of applications which is no longer limited to the mechanical domain. Consequently, a methodology was conceived for manufacturing complete, integrated electromechanical assemblies [1,2]. One possible implementation of an MD* system for manufacturing multi-material, composite parts is shown in figure 1 [1].

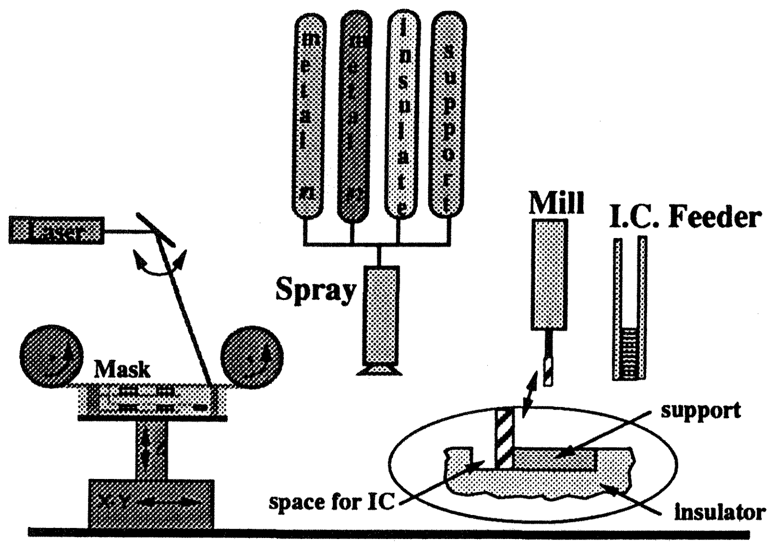


FIGURE 1. Envisioned MD* System

One class of multi-material, composite parts which could be produced with MD* is mechatronics. Mechatronics is a term for a new type of hybrid system component that performs both mechanical and electronic functions [5]. These parts contain embedded electronic components, and have become especially pervasive in the automotive industry. Manufacturing these components traditionally involves separate production of the electronic circuits and the mechanical structures. The electronic and mechanical sub-assemblies are then coupled to form the final part. The research described in this paper is aimed at using MD* to manufacture mechatronics in an integrated way. With this approach, a single manufacturing process is used to perform concurrent fabrication in the mechanical and electronic domains. The direct advantage of this is a high degree of integration not available using the traditional approach. This also accommodates high density, conformable embedded circuitry since three dimensional electronic part placement and interconnection is possible. Furthermore, since a single manufacturing process is used which is driven by a single CAD representation of the composite part, concurrent, multi-domain design is supported.

To demonstrate the feasibility of using MD* to manufacture mechatronics, a simple electromechanical artifact was designed and produced. A version of the familiar, hand-held "simon" electronic game was chosen to be implemented. This game consists of a mechanical housing that contains a reset button, two play buttons and two LEDs. The LEDs are lit in a pseudorandom sequence which must be duplicated by the user via the play buttons. Physically, the device consists of an insulating housing and embedded electronic components that are interconnected using two planar routing layers. This device was ideal for our purposes because of its balanced electrical and mechanical requirements and modest complexity. The "simon" game that was produced is shown in figure 2.

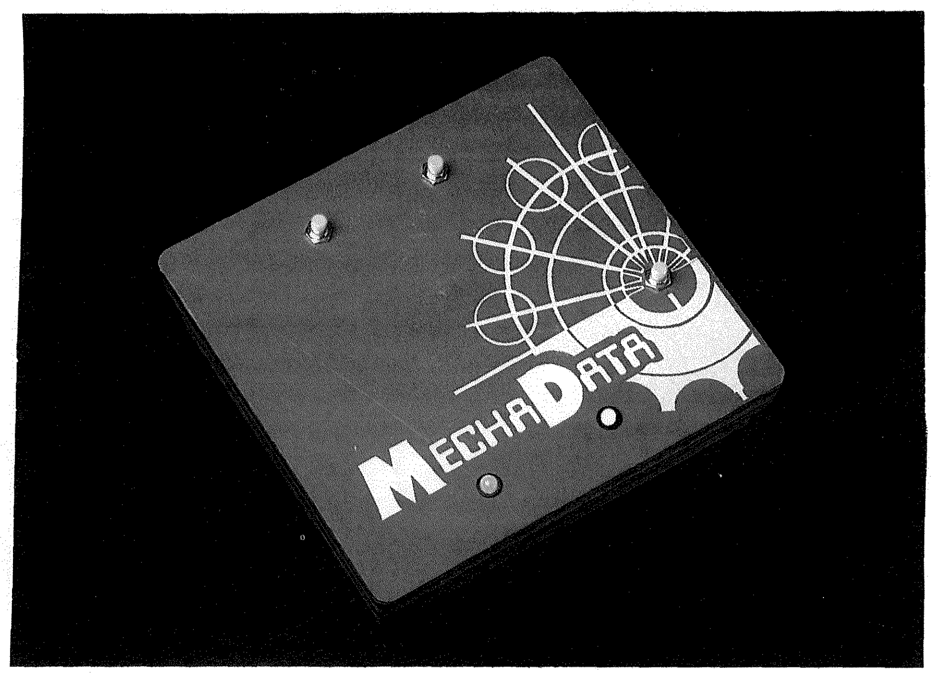


FIGURE 2. "Simon" game

Producing a device of this nature requires design in multiple engineering domains as well as enhancement of the MD* manufacturing process. The manufacturing process was extended to allow electronic components to be embedded and interconnected into a mechanical structure. The multi-domain design effort was largely dominated by design in the electronic domain since this was the first time that the linkage from a physical electronic design to MD* manufacturing had been attempted. These research thrusts proceeded concurrently and are described in detail in this paper.

## *Fabrication Process Experimentation*

Manufacturing the "simon" device required deposition of both metallic and insulating materials. The current spray station, however, is only equipped to perform electric arc and flame spraying. Electric arc spray techniques can only be used to deposit metallics. Insulating materials can be deposited using flame spraying, but the flame destroys the masking material and has a high potential for damaging embedded electronic components. This prompted the decision to use a castable insulator to form the mechanical housing of the "simon" game. In the future, however, the MD* system will be equipped to support plasma spraying which can accommodate a wide range of materials and masks. As another alternative, it may be possible to deposit the castable insulators using non-thermal spray techniques. Castable insulators are formed by combining fast-curing resin and hardener materials. These materials can easily be atomized and mixed in a spray system. Experimentation with these techniques has not yet been completed.

Little information existed concerning the electrical characterization of sprayed conductors. Initial experimentation was done to gauge the feasibility of using sprayed conductors in the "simon" device. Although these experiments were not extensive, preliminary results indicated that thermally sprayed zinc conductors, 0.004 inches thick, 0.10 inches wide and greater than 20 inches in length, were capable of carrying digital signals in excess of 25MHz. Furthermore, these results were robust with respect to manufacturing process variations such as atomization gasses and particle velocities. Although these results are not conclusive in the absence of a complete characterization, they proved that sprayed zinc interconnections were more than adequate for the "simon" design.

Experimentation was also done to establish a method for embedding electronic components in insulating material and spraying interconnections to the exposed leads. The ability to spray 3-D interconnections was hindered by the absence of a sprayable insulator. The decision was therefore made to only allow planar layers of sprayed interconnections. To provide multiple interconnection layers between components, "vias" were needed to interconnect the planar sprayed layers. These "vias" were inserted as discrete components. On a given plane, sprayed connection was made to an inserted "via" which provided a conduction path to other planar layers. In this way, all intra-layer connections were thermally sprayed and all interlayer connections were formed with inserted "vias". Furthermore, all sprayed connections to the leads of embedded components other than "vias", such as resistors, capacitors and integrated circuits, were restricted to the first planar sprayed layer. All subsequent sprayed layers were used to interconnect vias.

Initial experiments with the use of "vias" showed that shadowing effects degraded the quality of the electrical connection. Inserted "vias" were necessarily longer than the leads of other embedded components, since they must extend through the insulator to the next layer of sprayed interconnections. The length of the exposed "via" impeded the flow of the sprayed material causing a void (i.e. shadow) near the interconnection interface. To combat this, insulator layer thickness (i.e. "via" height) and "via" lead diameter were kept to a minimum.

## *Design Flow*

The primary design goal in the electronic domain was maximum functionality for minimum physical part count. This motivated the decision to use programmable logic devices (PLDs) and a traditional design methodology rather than synthesis tools.

The gate level design was completed first. This provided a baseline for the electronic complexity. At this point the game was pruned from four buttons to two, and the decision to use two, twenty-four macrocell PLDs to implement the logic was made. The selection of the PLDs was also based on assumptions about the manufacturing process. The method developed for interconnecting embedded components restricted the type of integrated circuit packages that could be used.

A commercially available software package was used to generate the programming files for the PLDs. Input files were manually translated from the gate-level design. Test vectors were written and the design was thoroughly simulated. Slight modifications were made in the design between the gate level and the PLD representation. This is largely explained by modifications that were made to fit the design into the two PLDs. Behavioral constructs were favored that closely matched the PLD macrocell architecture.

Functionally, the "simon" circuitry consists of a clock generator, reset circuitry and a clocked, sequential circuit. The sequential circuit was implemented with the PLDs. Specifically, the sequential circuit consists of eight functional blocks controlled by a finite state machine. One of the functional blocks was a linear feedback shift register that was used to generate the pseudorandom lighting sequence. A free-running counter that was enabled during the reset state was used to generate a random seed. Other functional blocks were included to capture button depressions made by the user and compare them to the lighting sequence. Other counters were included to track the length of the lighting sequence, the state of the current sequence and a visible delay for displaying and blanking the LEDs. The finite state machine was a Mealy type and contained fourteen states.

Because time was an issue and the number of physical parts and signals was small, part placement and routing was done by hand. One layer of planar part placement was assumed. Two levels of planar interconnections were assumed. The first interconnection level consists of electrical signals while the second level includes power, ground and battery cable connections.

The physical design was completed next. This was done by creating 3-D models of the electronic parts and 2-D models of the interconnection layers. These models were constructed using the NOODLES user interface DISH. These models were entered into the CAD tool manually, by adding dimensional information to the part placement and routing. The NOODLES models of the two interconnection layers were extracted and sent to the laser mask cutting station. Masks of the interconnection layers were produced that were later used to manufacture the device. NOODLES models of the interconnection layers are shown in figures 3.

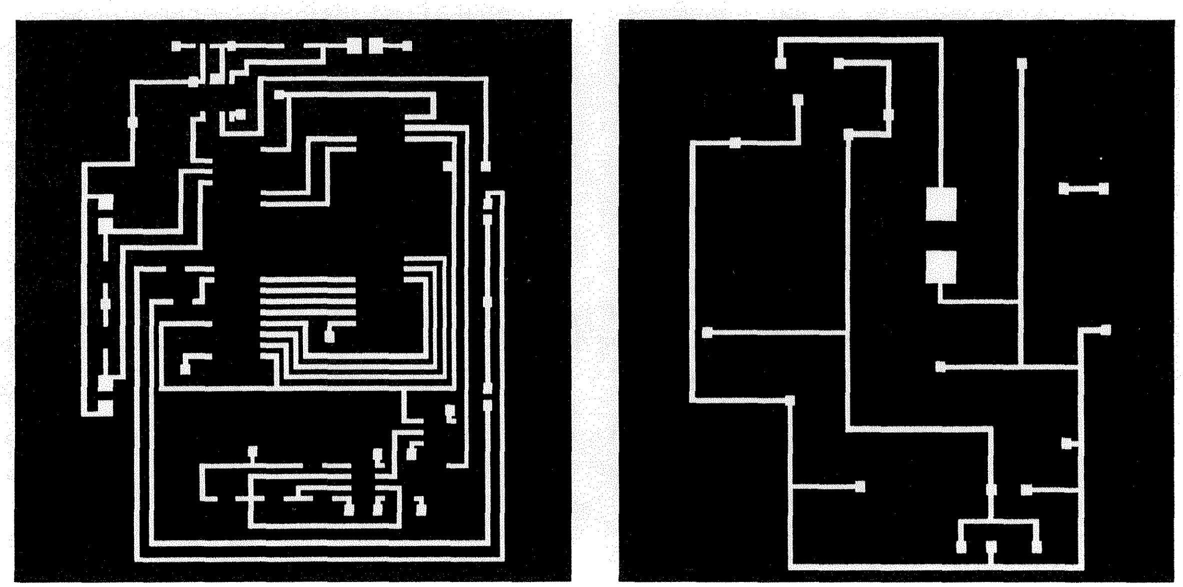

FIGURE 3. NOODLES models of interconnection layers. Left: layer 1. Right: layer 2.

The circuit which implements the simon game is a regulated, 5V digital synchronous circuit with a maximum internal frequency of 2 kHz. Physically, the simon circuit contains the following components:

- One (1) reset button
- Two (2) play buttons
- Two (2) play LEDs
- One (1) voltage regulator (3-pin SIP)
- Two (2) EPLDs (40-pin DIP)
- One (1) "MicorMonitor" IC (8-pin DIP)
- One (1) timer (8-pin DIP)

- One (1) counter (16-pin DIP)
- One (1) 9V battery cable
- Seven (7) resistors
- Three (3) capacitors

The design flow for the simon game was chosen to match the complexity of the device. More complex designs may warrant the use of design synthesis tools, such as MICON [6] rather than traditional, manual design. Automated placement and routing tools would also be a benefit, as well as an enhanced NOODLES interface. The NOODLES representation of the physical design is linked directly to the MD* manufacturing process and provides the final target for design synthesis tools. Once a design has been represented in NOODLES, the manufacturing steps are generated automatically.

With the MD* process, design of the mechanical structure can be done directly in NOODLES. Two factors limited the mechanical structure of the "simon" design. The first was the decision to use a castable insulator for the bulk material, thereby limiting geometries. Secondly, conservative decisions concerning the manufacturing process and placement and interconnection of embedded parts drove physical design in the electronic domain, thereby dictating the rectangular solid shape of the final artifact.

## *Manufacturing Steps*

Once physical design of the "simon" device was completed and MD* had been extended to accommodate embedded electronics, manufacturing commenced. This section will describe the steps used to produce the "simon" game.

First, an aluminum mold was made for the castable insulator. This mold was used to house the growing device and also acted as a support frame for spraying. Next, a thin (1/8") face plate was cast using the mold. Switches and LEDs were mounted to the face plate, and discrete components such as resistors and capacitors were attached to the underside. The mask for the first layer of interconnections was used to determine part placement. Integrated circuit packages and "vias" were also inserted in this manner. A total of twenty-two electronic components and eighteen "vias" were needed for the "simon" circuit. Before proceeding, the circuit was completed using microclips and functionality was verified. All of the circuit components were then embedded by casting another layer of insulating material onto the underside of the faceplate. Only the component leads were visible, and they were trimmed to a uniform height. Again, "vias" were naturally longer; once the first layer of interconnections are complete and embedded, the via leads must still reach through the insulator and be exposed so they can be connected in the next sprayed layer.

To prepare the material for thermal spraying, the insulating material and exposed leads were grit blasted. Initial experimentation showed that grit blasting increased the adhesion strength of the sprayed interconnections. The mask for the first layer of interconnections was then applied over the exposed leads to the grit blasted surface and the first interconnection layer was sprayed (see figure 4). At this point, microclips were again used to complete the circuit and test functionality. Once functionality was verified, another layer of insulator was cast which embedded the sprayed interconnections so that only the "via" leads were exposed. The 9-V battery cable was also inserted at this time.

The second sprayed layer of interconnections was needed to interconnect the exposed "vias" and the battery cable. The surface was once again grit blasted. Care was taken not to damage the battery cable. Next, the mask for the second interconnection layer was set in place and the spray process was repeated. The battery was attached and functionality was confirmed. The final step was another cast layer of insulating material to embed the exposed interconnections. At this point the buttons and LEDs were accessible from the initial, top surface, and the battery cable protruded from the final, bottom surface.

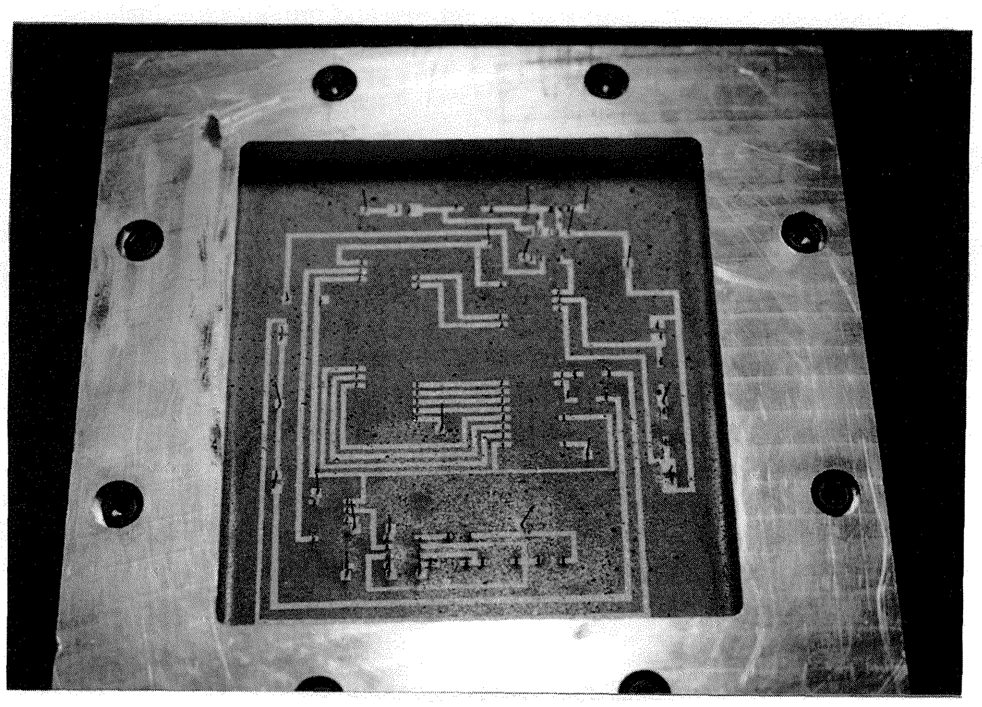

FIGURE 4. Sprayed Interconnections: Layer 1

## Conclusions

The simon experiment successfully demonstrated the ability to embed and thermally spray electrical connections between electronic components. Although the insulator that was used was cast and not sprayed, adequate techniques do exist to deposit insulators. Adaptation of the simon manufacturing process to include sprayed insulators will provide a novel, integrated method of manufacturing mechatronics.

To narrow the gap between the vision and reality of MD*, research spanning many disciplines is required. In the material science domain, research is needed to increase and identify the spectrum of sprayable materials for multi-material, composite devices. This should be accompanied by an analysis and taxonomy of material properties that affect thermal spraying.

In the mechanical domain, experimentation with the masking scheme is needed. This would assuage the use of multiple materials per layer, where a planar surface is a concern. Also, finer masking geometries are desirable. This is especially true in the context of embedded electronic circuits, considering the densities afforded by existing electronic packaging techniques. Another issue is thermal properties, including heat dissipation and accommodating the CTE (Coefficient of Thermal Expansion) range of various materials. For more complex devices, the thermal environment of the embedded electronic components must be insured for reliable operation.

In the electronic domain, more thorough characterization of sprayed conductors and connections is warranted. A comparison should also be made to existing approaches such as printed circuit boards and hybrid circuits, which clearly set the standard regarding minimum acceptable circuit density. Ultimately, the MD* approach will allow arbitrary 3-D placement and interconnection of embedded electronic components. This illustrates a potential not inherent in existing approaches. Other areas of research include thermally sprayed circuit components such as high precision resistances and capacitances. The architectural implications of creating fully embedded circuit assemblies should also be explored. These include concerns regarding partitioning, modularity and serviceability.

One of the key advantages of the MD* manufacturing system is that a direct link is provided between a CAD tool design representation and a single, integrated manufacturing process. Software development is needed to strengthen the links between domain-specific CAD tools and the final NOODLES representation.

## *Acknowledgments*

The simon game could not have been produced without the help and effort of many dedicated faculty, staff and students of Carnegie Mellon University. The authors wish to thank: *Janaki Akella, Kevin Hartmann, Jack Kirr, Robert Merz, Christoph Pichler, Dave Sealfon, Larry Shultz, John Stivoric* and *Dave Thuel* for their contributions.

## *References*

[1] L. Weiss and F. B. Prinz. A conceptual framework for a masks and deposits thermal spray shape deposition system. in *DARPA Workshop on Manufacturing,* Univ. of Utah, Feb. 1991

[2] L. Weiss, F. B. Prinz, D. P. Siewiorek. A framework for thermal spray shape deposition: The MD* system. in *Solid Freeform Fabrication Symposium,* Univ. of Texas at Austin, Aug. 1991

[3] L. Weiss, F. Prinz, D. Adams. Solid freeform fabrication by thermal spray shape deposition. in *ASM International Thermal Spray Conference,* Orlando FL, Jun 1992

[4] A. Sudhalkar, R. Bhargava, R. Mattikalli, J. Chen. An Introduction to the NOODLES Geometric Modeling System (Version 7). in *Technical Report,* Carnegie Mellon University, Pittsburgh PA, Oct 1990

[5] L. Berardinis. Mechatronics: A new design strategy. in *Machine Design, Apr. 26, 1990*

[6] W. P. Birmingham, A.P. Gupta, D. P. Siewiorek. *Automating the Design of Computer Systems: The Micon Project.* Jones and Bartlett, 1992.

[7] R. Merz, F.B. Prinz L.E. Weiss. Planning Mask Cutting for Thermal Spray Shape Deposition. in *Technical Report,* EDRC 24-74-91, Carnegie Mellon University, Pittsburgh PA, 1991