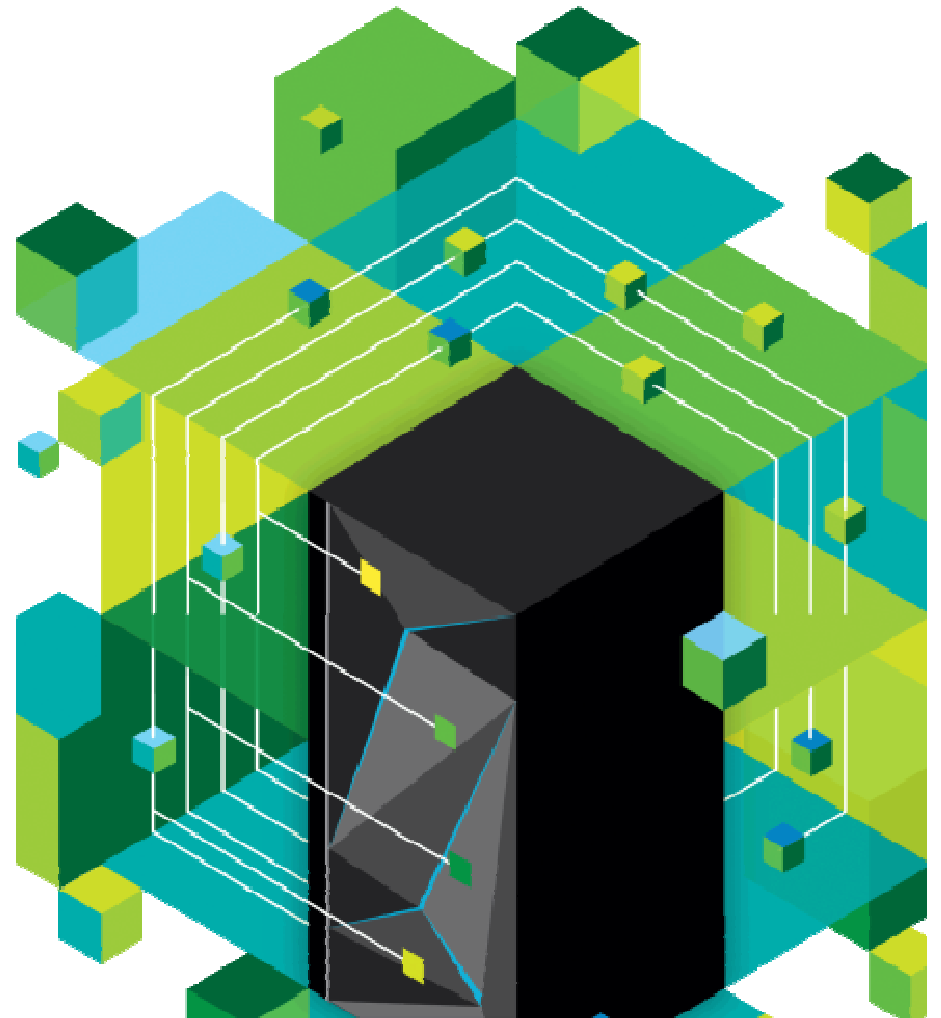


IBM Power Systems

5 February 2013 Announcement
Hardware Deep Dive





IBM Power Systems – The Ultimate Platform for Compute Intensive Workloads

9,000+

Patents since 2001

\$4.2B

Investment POWER7 & POWER7+

100+

Industry leading benchmarks

200M

Pages processed in 3 seconds by IBM Watson for healthcare delivering personalized medicine & cancer research

5 of 10

World's fastest super-computers run on POWER, including Sequoia

88%

More SAP Users per core than x86 when running on POWER7+

3,000+

Competitive displacements

20,000+

ISV apps running on IBM Power Systems

#1

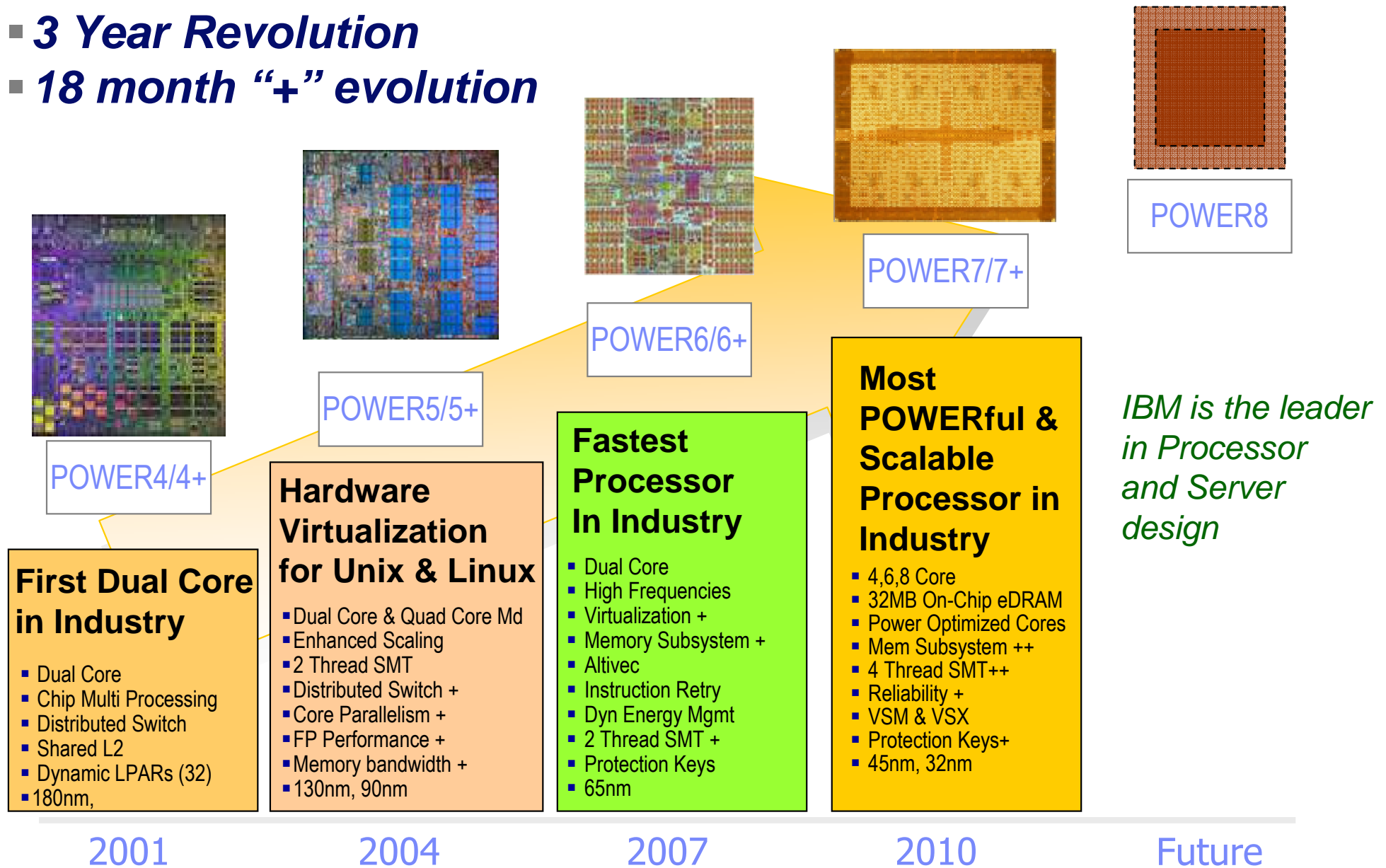
UNIX server revenue share leader 6 years running

<http://www-03.ibm.com/systems/power/hardware/benchmarks/>

[#ibmpowersystems](#)

IBM POWER Processor Roadmap

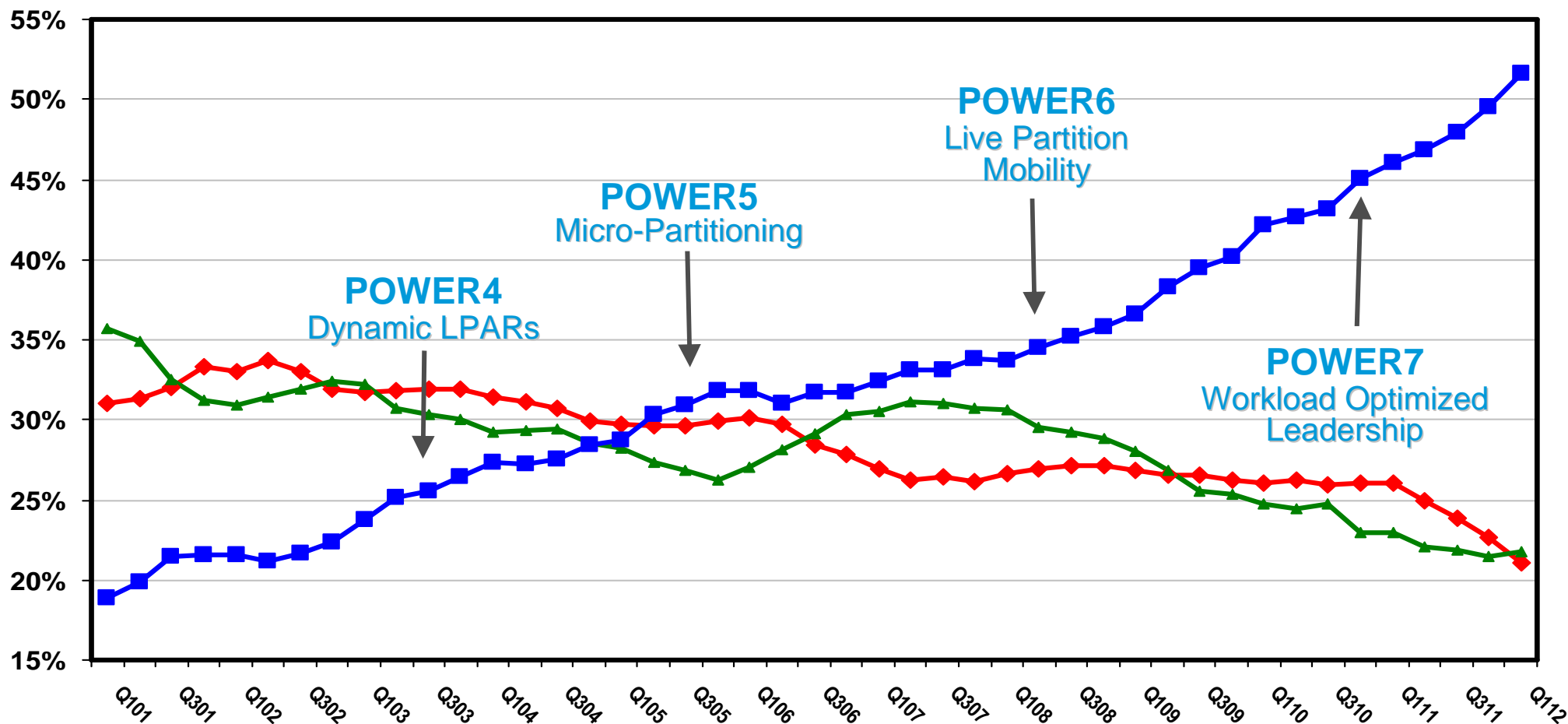
- **3 Year Revolution**
- **18 month “+” evolution**



10Yr History Four Quarter Average Revenue Share

UNIX Server Rolling Four Quarter Average Revenue Share According to IDC

◆ HP ▲ SUN/Oracle ■ IBM

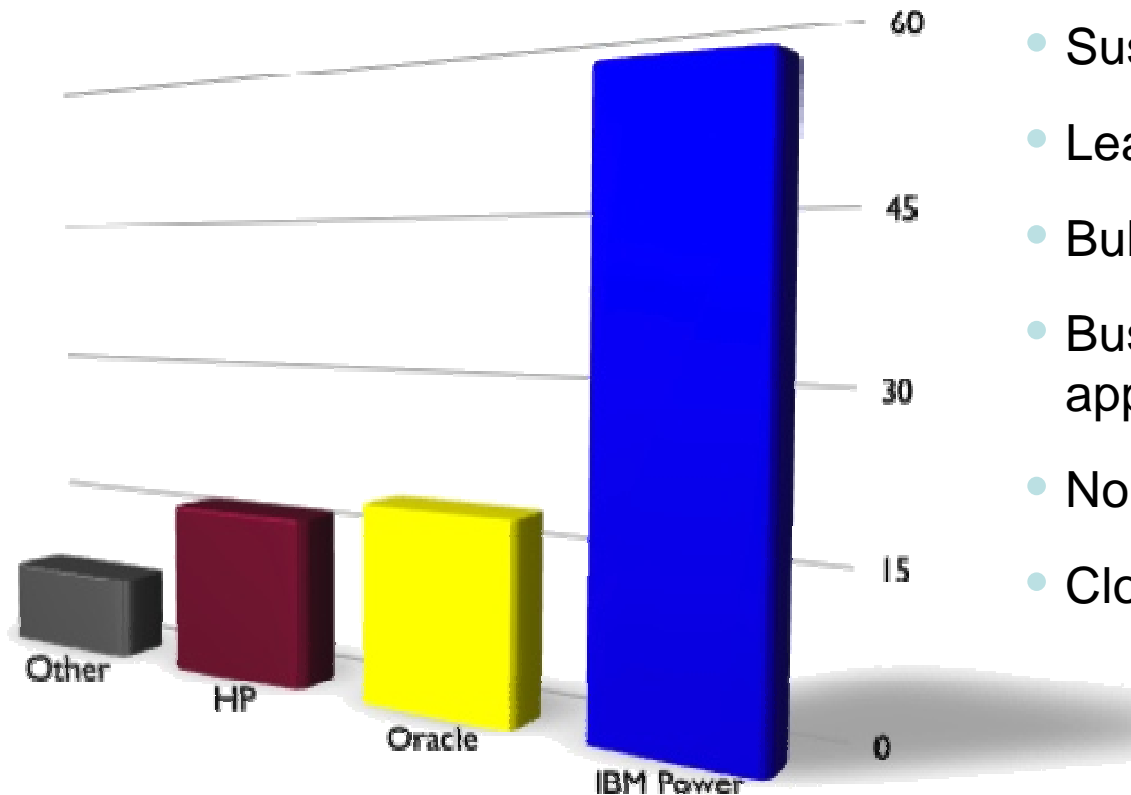


Source: IDC Worldwide Quarterly Server Tracker, http://www.idc.com/getdoc.jsp?containerId=IDC_P348

IBM Power Systems ships over 3X the volume of high value systems vs. HP, Oracle or other vendors

Worldwide Server Unit Share >\$100K

R4Q volume (less System z)

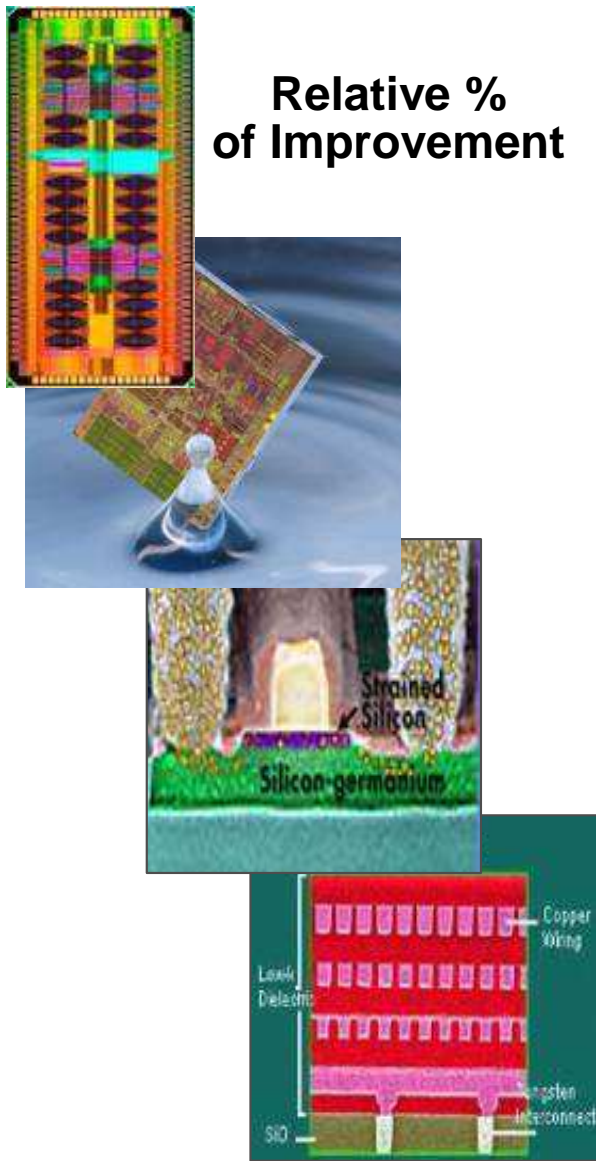


- Industry's most popular enterprise servers
- Sustained performance leadership
- Leadership virtualization efficiency
- Bullet proof security
- Business resiliency for mission critical applications
- Non-disruptive growth with CoD
- Cloud enabled for greater flexibility

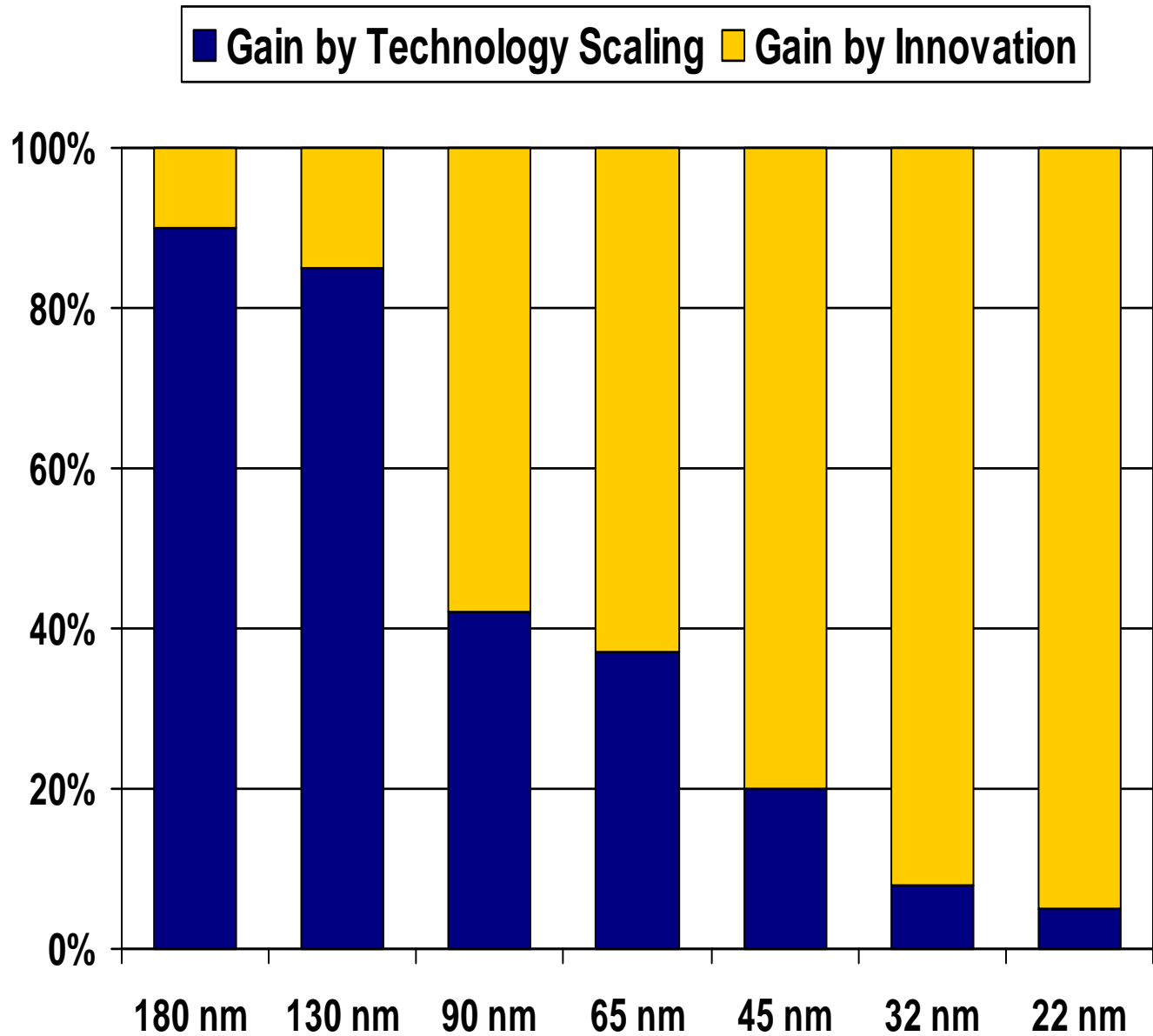
Source: IDC Server Tracker Q212 Release, August 2012



Innovation Drives Performance

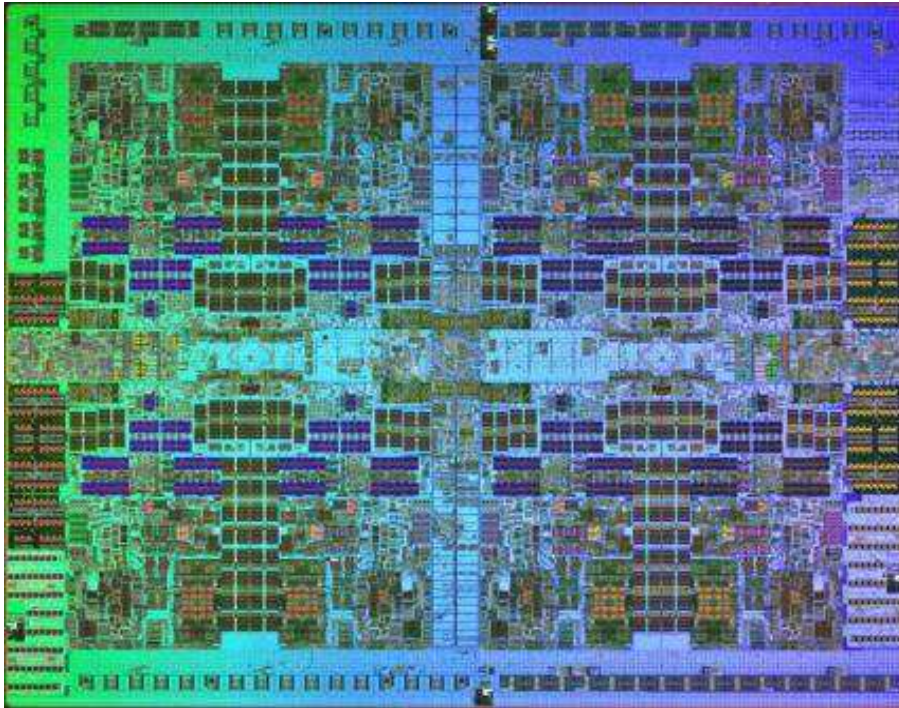


Relative % of Improvement

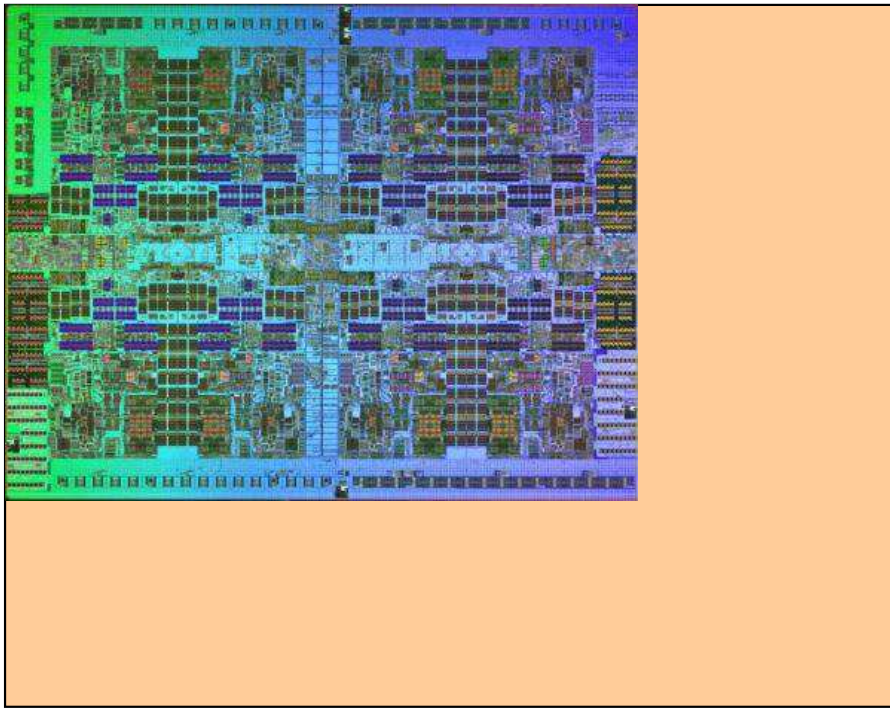


IBM plans for future 22 nm technology are subject to change.

POWER7+

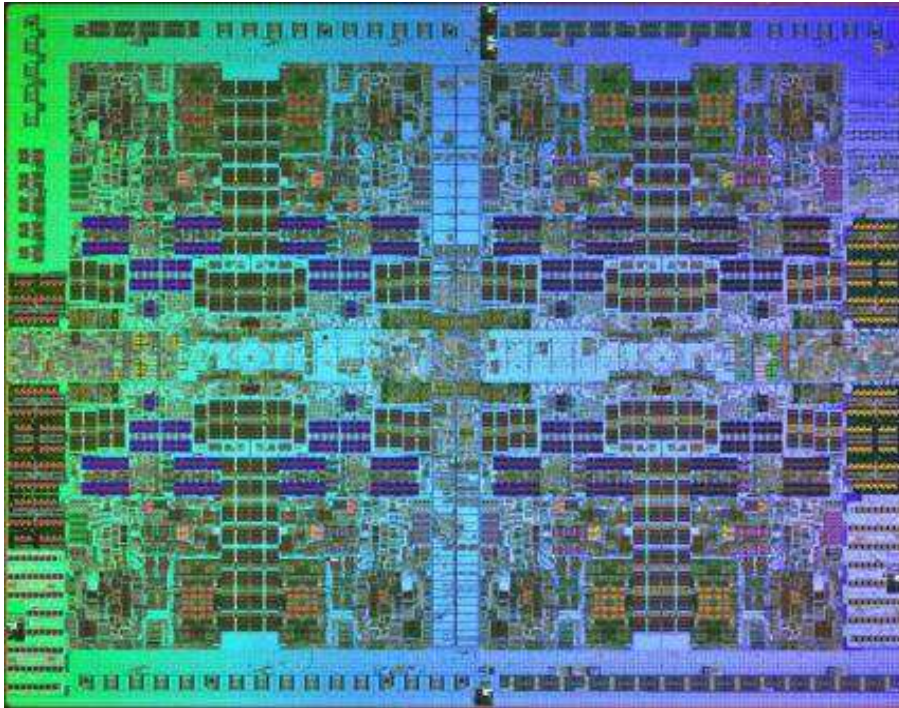


POWER7
45 nm

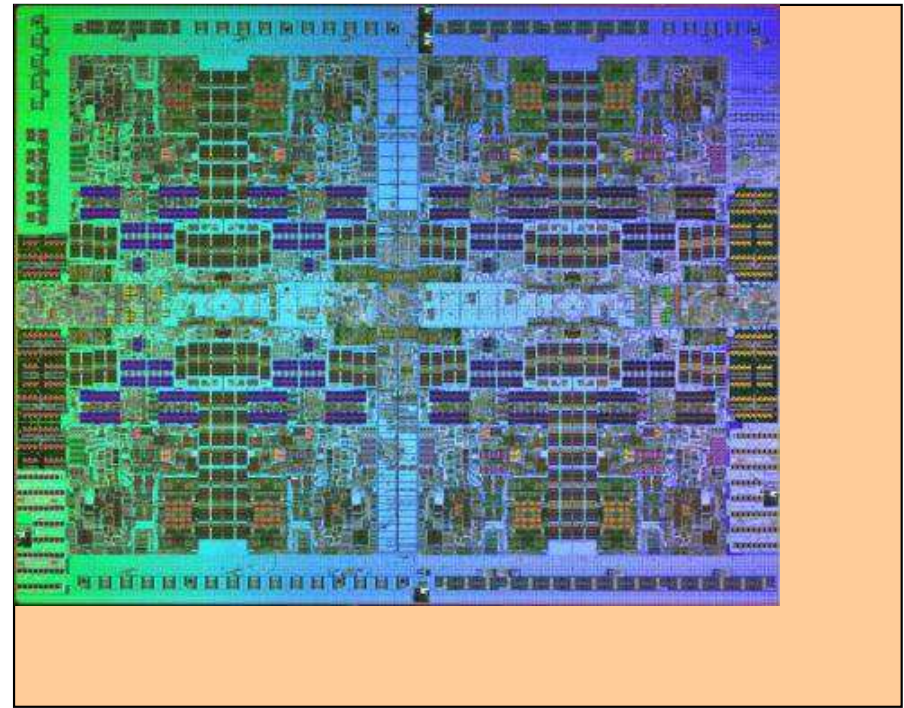


POWER7
32 nm

POWER7+



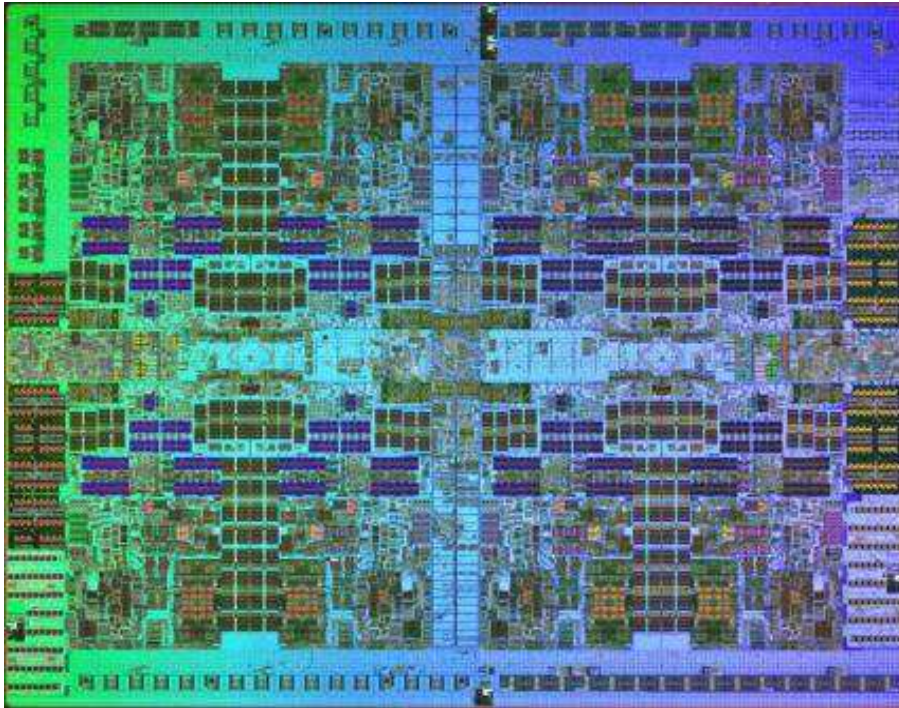
**POWER7
45 nm**



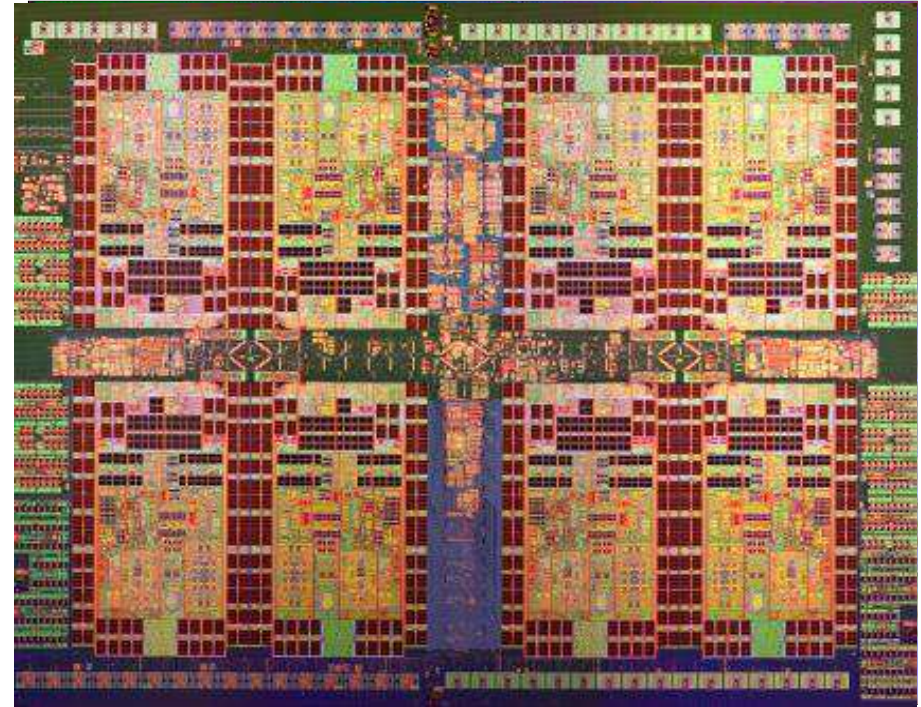
**POWER7
32 nm**

Add additional Cache

POWER7+



POWER7
45 nm



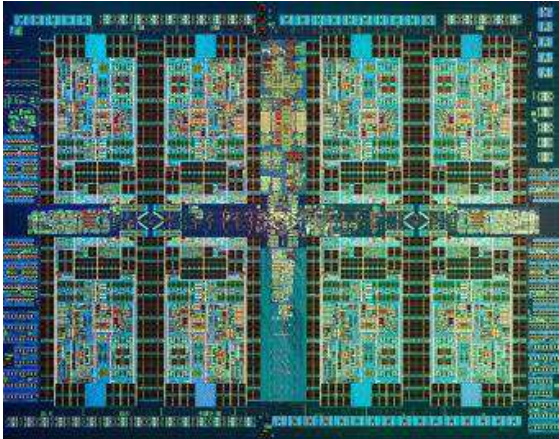
POWER7
32 nm

Add additional Cache

Add on Chip Accelerators

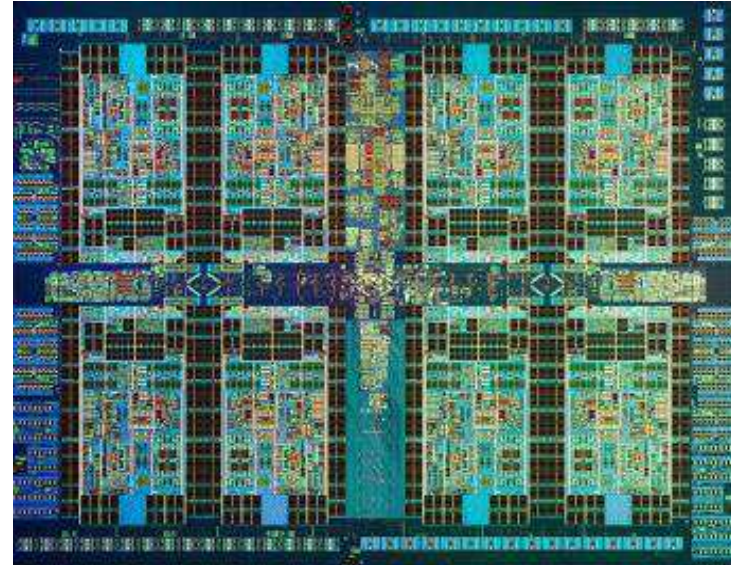
Benefits of eDRAM for POWER7+

With eDRAM



2.1B Transistors
567 mm²

Without eDRAM



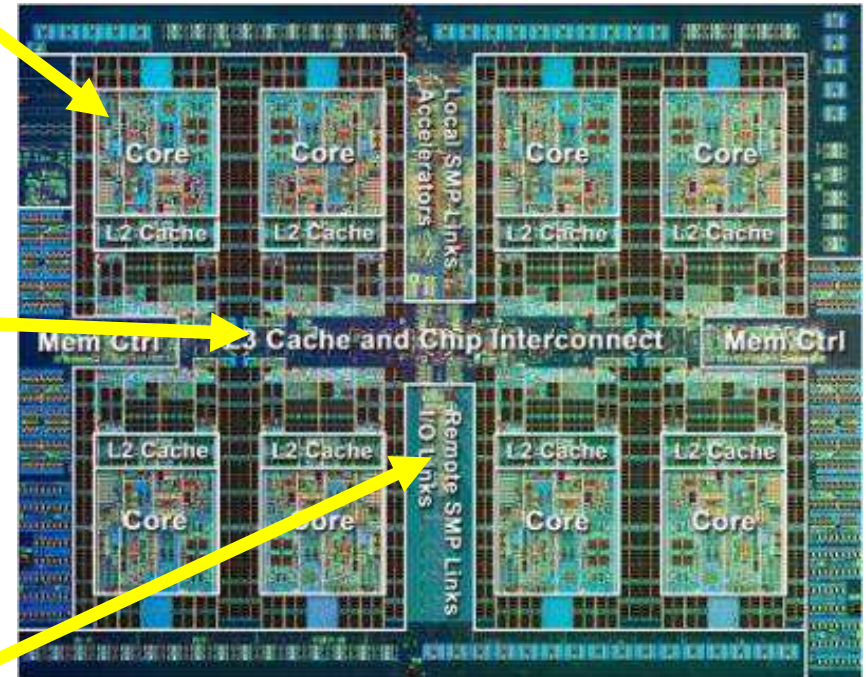
5.4B Transistors
950 mm²

IBM's eDRAM Benefits:

- **Greater density: 1/3 the space of 6T SRAM implementation**
- **Less power requirements: 1/5 the standby power**
- **Fewer soft errors: Soft Error Rate 250x lower than SRAM**
- **Better Performance**

POWER7+ RAS Specific Features

- New Power On Reset Engine (PORE)
 - Enables a processor core to be re-initialized while system remains up and running
 - Directly used to:
 - *Allow for Concurrent Firmware Updates:* In cases where a processor initialization register value needs to be changed
- L3 Cache dynamic column repair
 - New self-healing capability that complements cache line delete
 - Uses PORE feature to substitute a failing bit-line for a spare during run-time.
- New Fabric Bus Dynamic Lane Repair
 - POWER7+ has spare bit lanes that can dynamically be repaired (using PORE)
 - For Busses that connect CEC drawers
 - Avoids any repair action or outage related to a single bit failure.



POWER7+ Processors & Architecture

Faster Performance

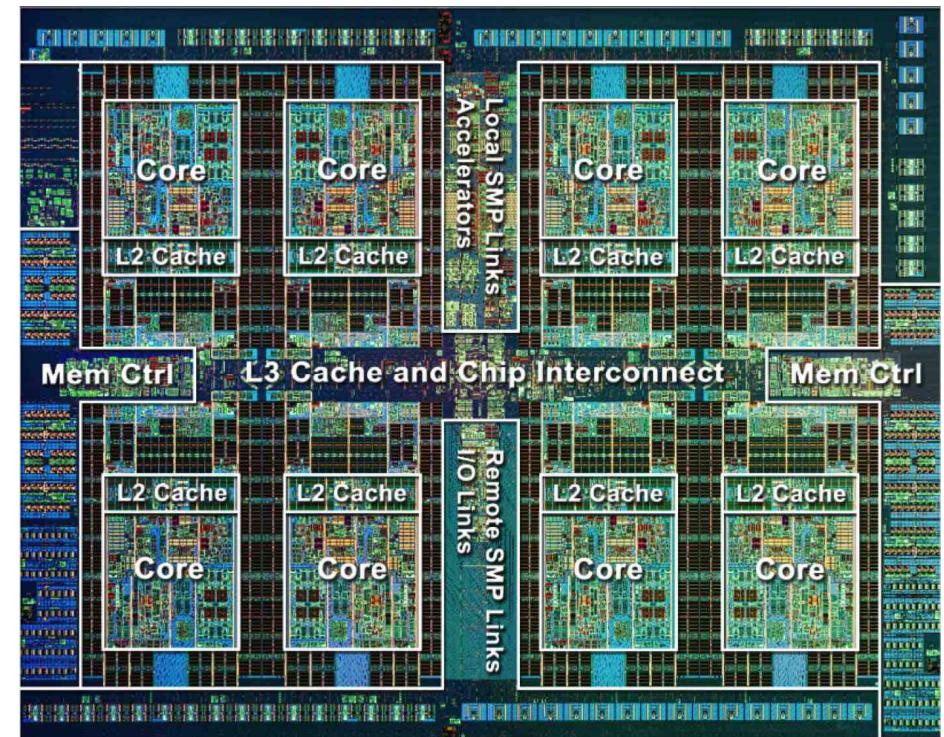
- Faster frequencies... up to 4.4 GHz POWER7+ processors
- 10 MB L3 Cache
- Random number generator
- Enhanced Single Precision Floating Point performance
- Enhanced GX system bus

Increased Efficiency and Flexibility

- Active Memory Expansion accelerator
- On-chip encryption acceleration for AIX
- Delivering 5x more performance per watt
- Enhanced energy / power gating
- 20 Virtual Machines per core

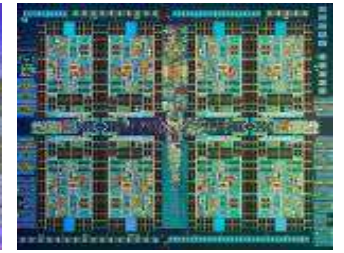
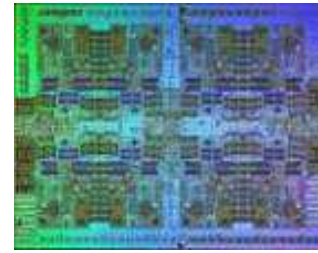
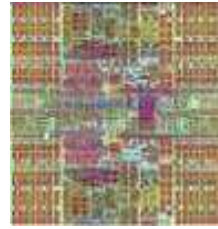
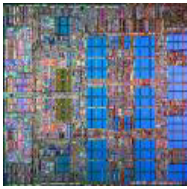
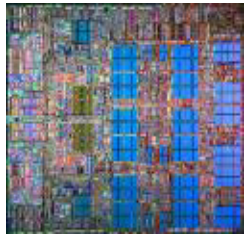
Better Availability

- Self-healing capability for L3 Cache functions
- Dynamic processor fabric bus repair
- Processor re-initialization



POWER7+
32 nm

Processor Designs



| | POWER5 | POWER5+ | POWER6 | POWER7 | POWER7+ |
|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| Technology | 130nm | 90nm | 65nm | 45nm | 32nm |
| Size | 389 mm ² | 245 mm ² | 341 mm ² | 567 mm ² | 567 mm ² |
| Transistors | 276 M | 276 M | 790 M | 1.2 B | 2.1 B |
| Cores | 2 | 2 | 2 | 8 | 8 |
| Frequencies | 1.65 GHz | 1.9 GHz | 4 - 5 GHz | 3 - 4 GHz | 3.6 - 4.4+ GHz |
| L2 Cache | 1.9MB Shared | 1.9MB Shared | 4MB / Core | 256 KB per Core | 256 KB per Core |
| L3 Cache | 36MB | 36MB | 32MB | 4MB / Core | 10MB / Core |
| Memory Cntrl | 1 | 1 | 2 / 1 | 2 / 1 | 2 / 1 |
| Architecture | Out of Order | Out of Order | In of Order | Out of Order | Out of Order |
| LPAR | 10 / Core | 10 / Core | 10 / Core | 10 / Core | 20 / Core |

Transition from POWER6

Cores:

- 8 Intelligent Cores / chip (socket)
- 4 and 6 Intelligent Cores available on some models
- 12 execution units per core
- Out of order execution
- 4 Way SMT per core
- 32 threads per chip
- L1 – 32 KB I Cache / 32 KB D Cache per core
- L2 – 256 KB per core

Chip:

- 32MB Intelligent L3 Cache on chip

Memory:

- Dual DDR3 Controllers
- 100 GB/s sustained Memory bandwidth / chip

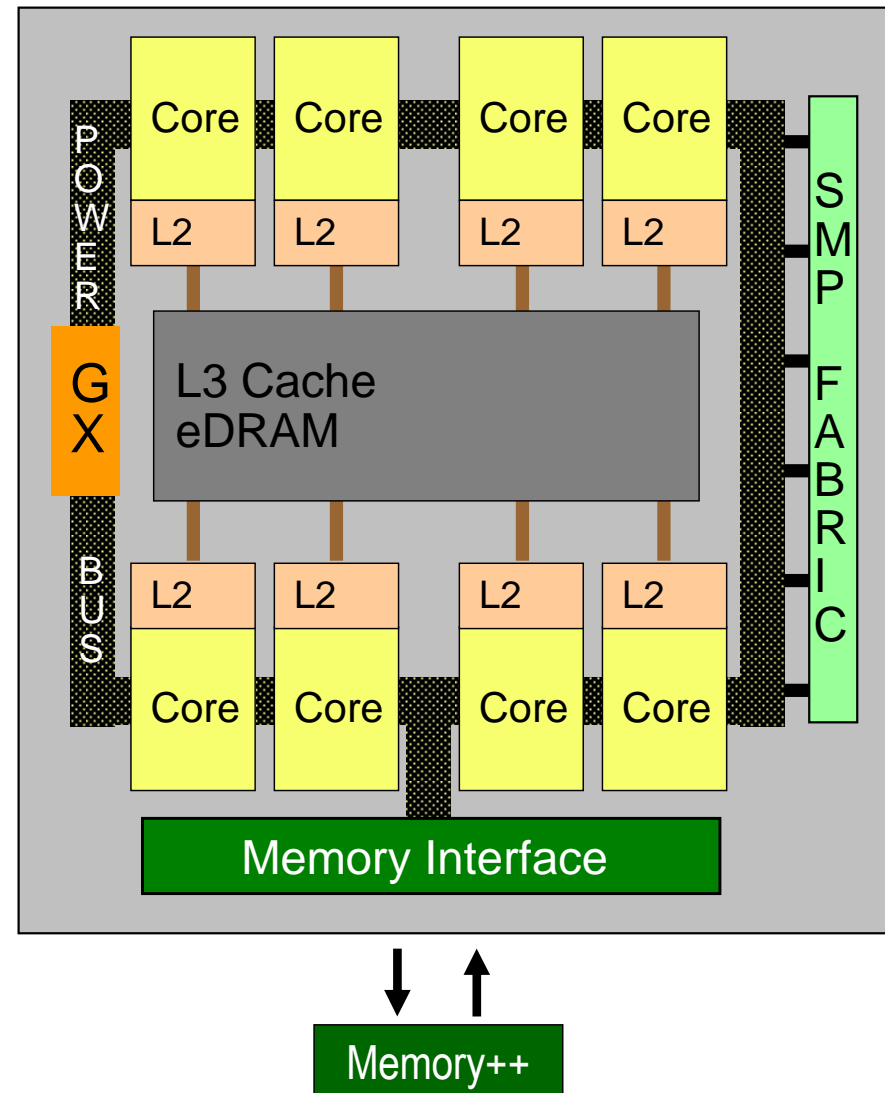
Scalability:

- Up to 32 Sockets
- 360 GB/s peak SMP bandwidth / chip
- 590 GB/s peak I/O bandwidth / chip
- Up to 20,000 coherent operations in flight

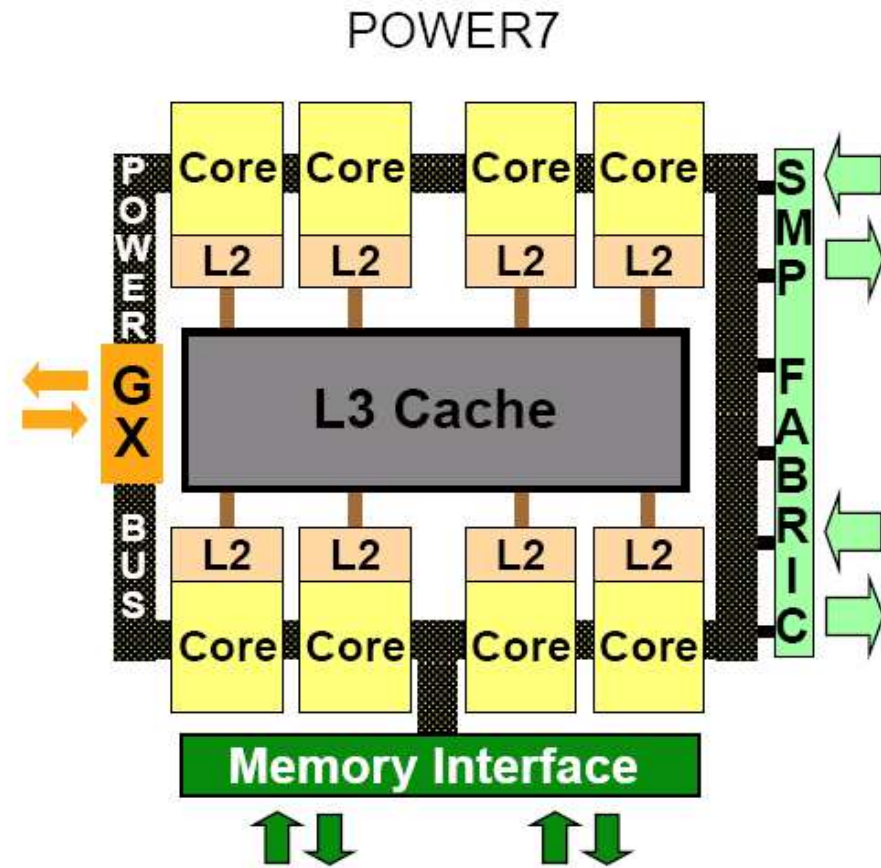
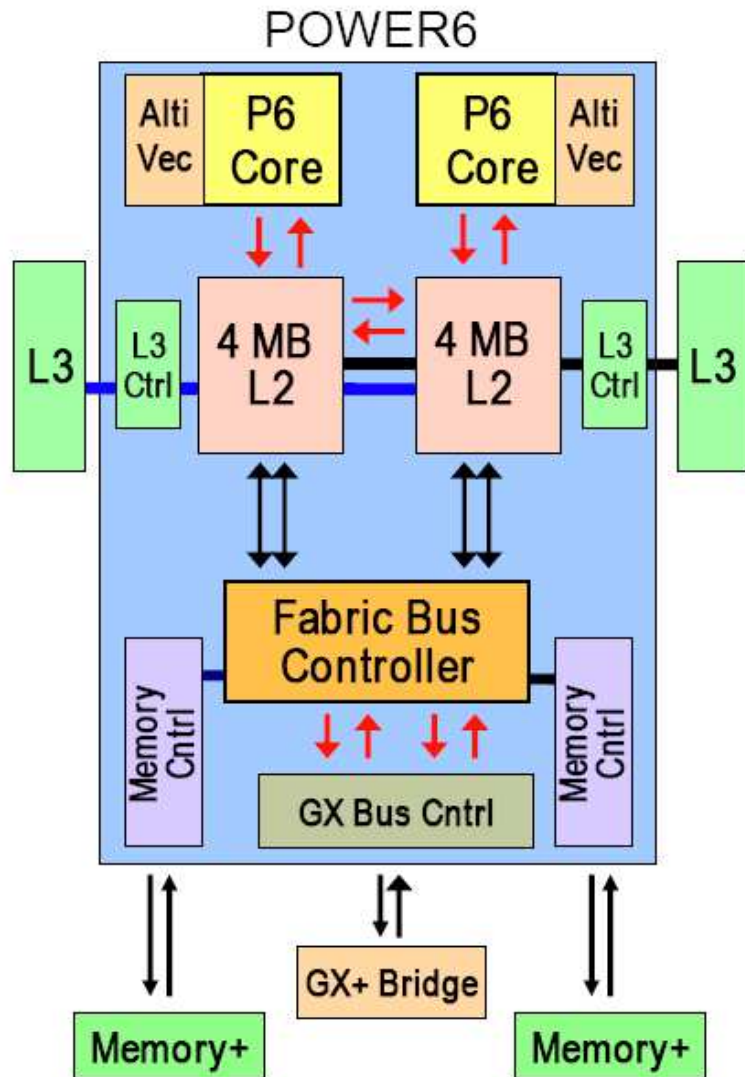
Energy:

- Aggressive processor Nap & Sleep modes
- 10% “Over clock” when thermals are good

POWER7



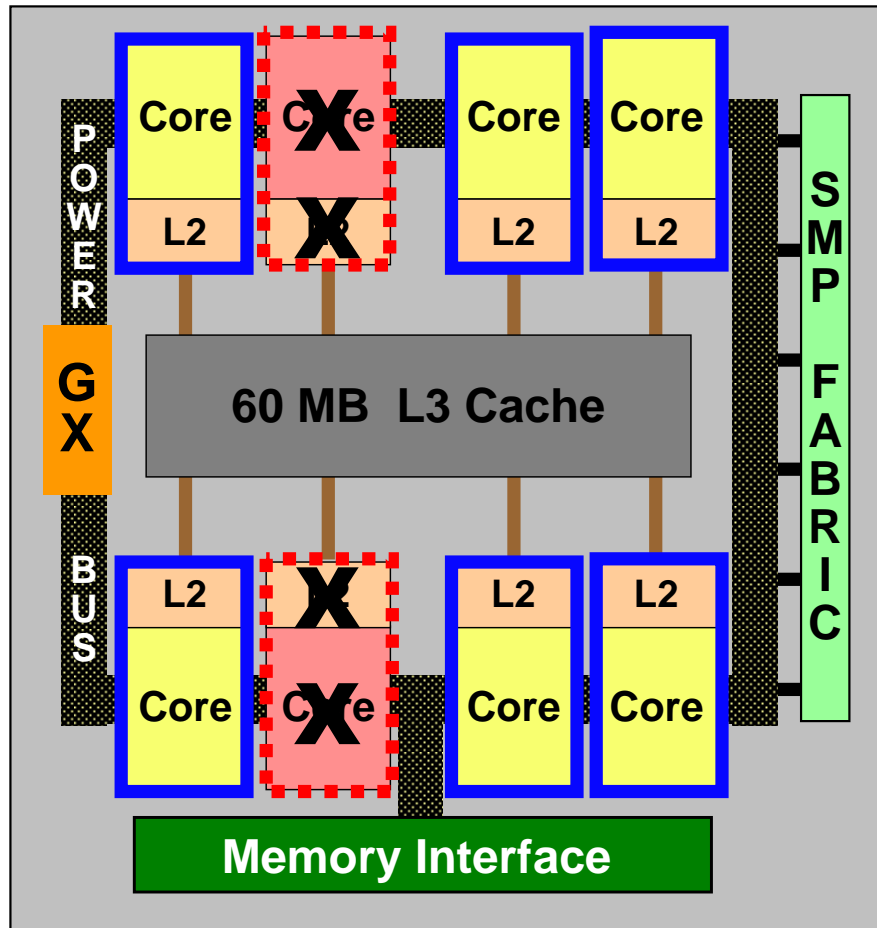
POWER6 - POWER7 Compare



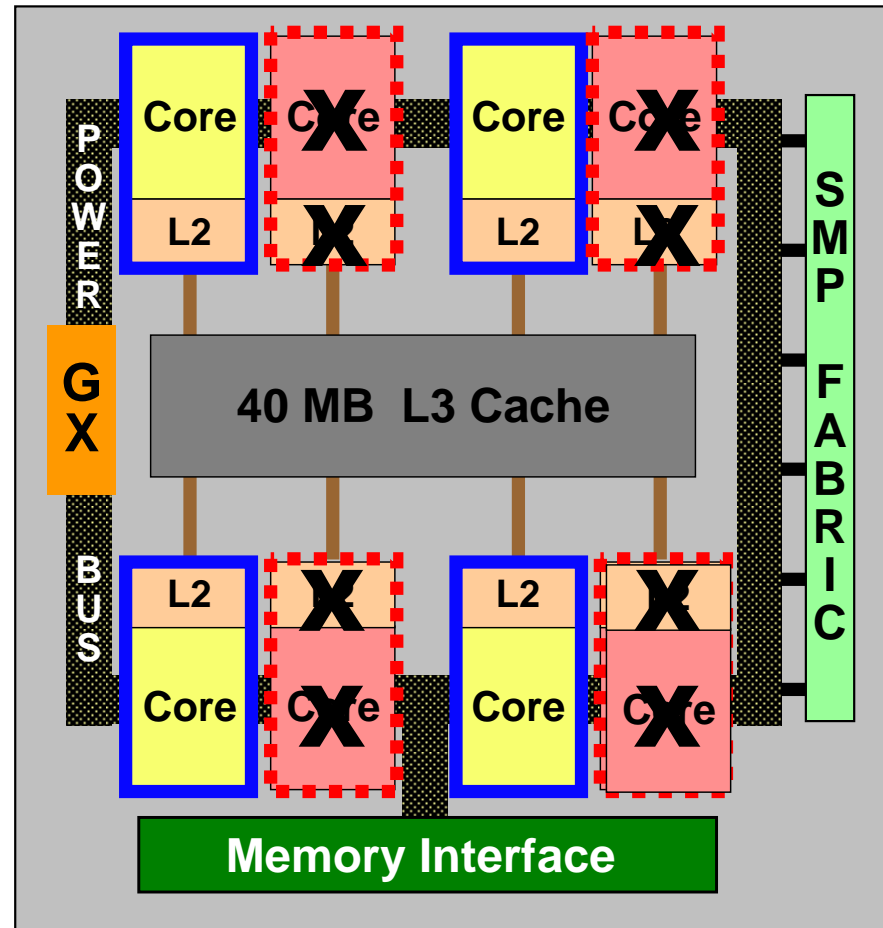
- ▶ Up to 8 cores / die
- ▶ 3rd Generation Multithreading – SMT4
- ▶ Integrated on-chip L3 Cache – lower latency
- ▶ 4th Generation SMP Fabric Bus
- ▶ Energy Optimized Design

POWER7 Core / Cache options

POWER7+ 6 Core Chip

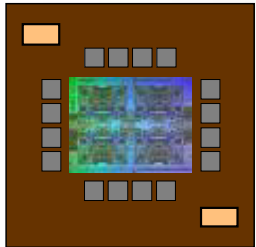
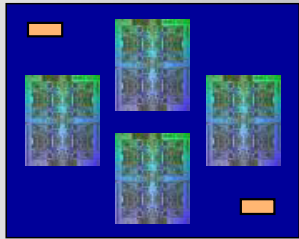


POWER7+ 4 Core Chip

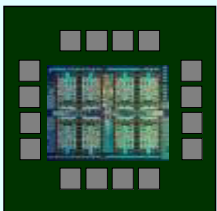
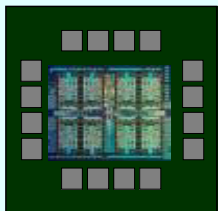
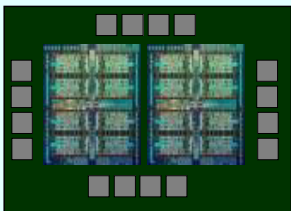
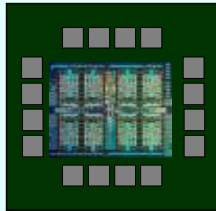


Conceptual diagrams above show one of several options to result in 6-core or 4-core chips

POWER7 / POWER7+ Module Packaging

| | | |
|---|--|----------------------|
| <p>Power 795 Single Chip Glass Ceramic</p>  | <p>Power 775 Quad-chip MCM</p>  | <p>POWER7</p> |
|---|--|----------------------|

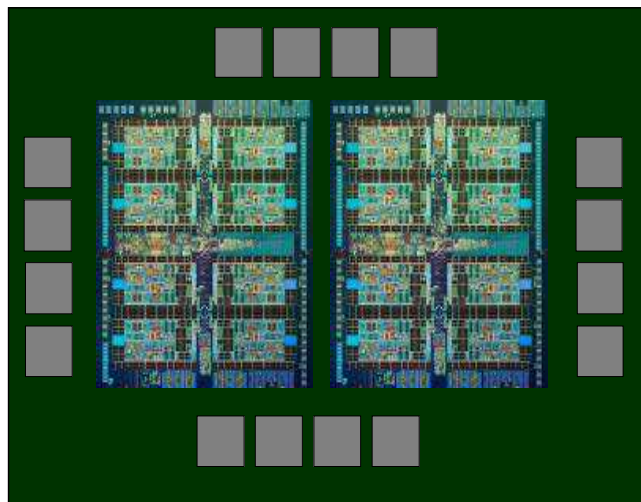
| | |
|---|----------------------|
| <p>Power 770 / 780 Single Chip Glass Ceramic</p>  | <p>POWER7</p> |
|---|----------------------|

| | | | | |
|---|---|--|---|-----------------------|
| <p>Power 710 / 730 Single Chip Organic</p>  | <p>Power 720 / 740 Single Chip Organic</p>  | <p>Power 750 / 760 Dual Chip Organic</p>  | <p>Power 770 / 780 Single Chip Organic</p>  | <p>POWER7+</p> |
|---|---|--|---|-----------------------|

POWER7+ DCM

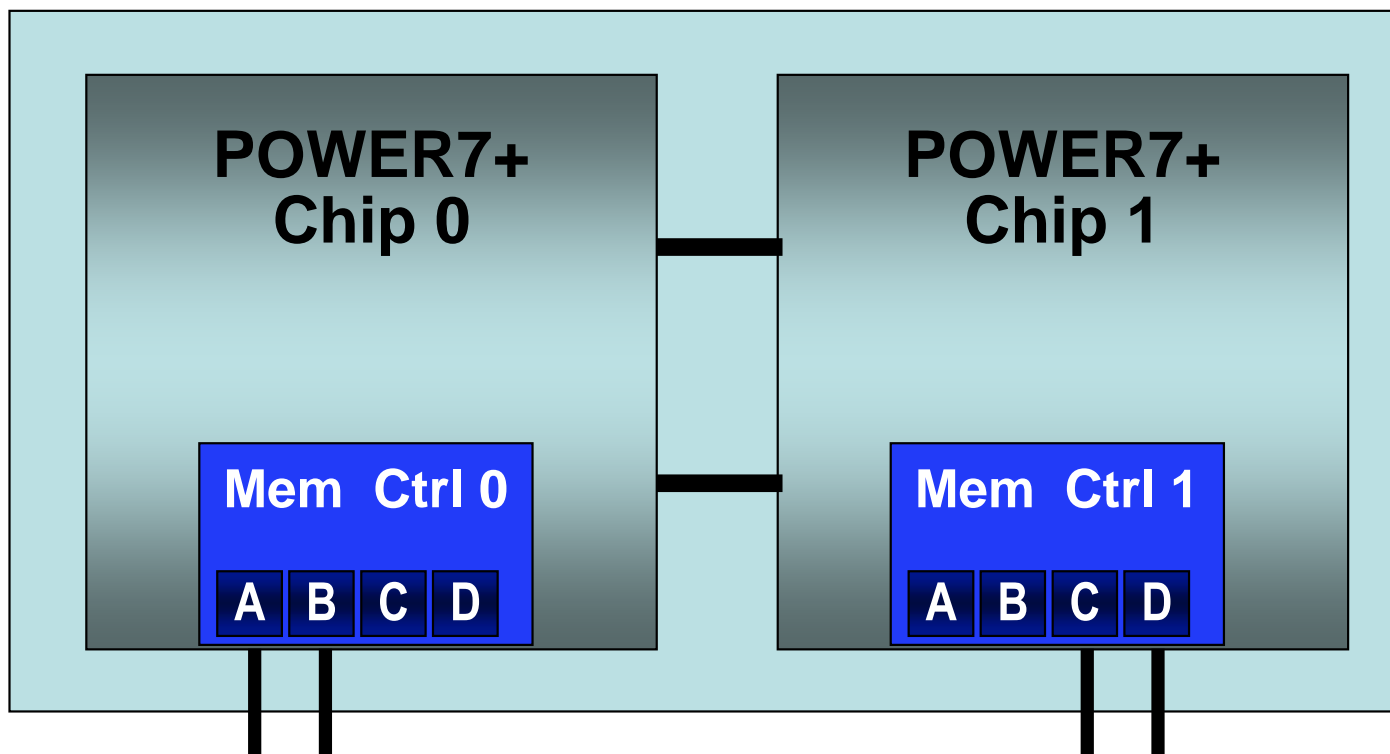
One Socket
Two POWER7+ Chips

- 4 Core option
- 6 Core option



Results in

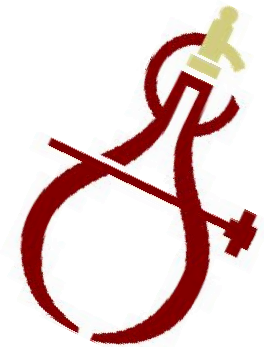
- 8 Core DCM
- 12-Core DCM



Processor Frequencies

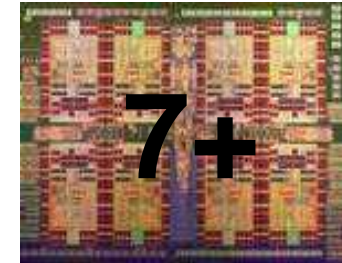
- The single decimal GHz values used in announcement letters and brochures (for example [3.6](#)) are simplified descriptions of the actual GHz provided by IBM
- The actual frequencies are 3 digit numbers:

| Announcement Letter Values | Actual Values |
|--|---|
| POWER7+ 4-core @ 3.6 GHz 6-core @ 4.2 GHz 8-core @ 4.2 GHz | 4 Core @ 3.612 GHz 6 Core @ 4.284 GHz 8 Core @ 4.228 GHz |
| POWER7+ 8-core @ 4.3 GHz 12-core @ 4.2 GHz 16-core @ 3.6 GHz 16-core @ 4.2 GHz | 8 Core @ 4.312 GHz 12 Core @ 4.284 GHz 16 Core @ 3.612 GHz 16 Core @ 4.228 GHz |

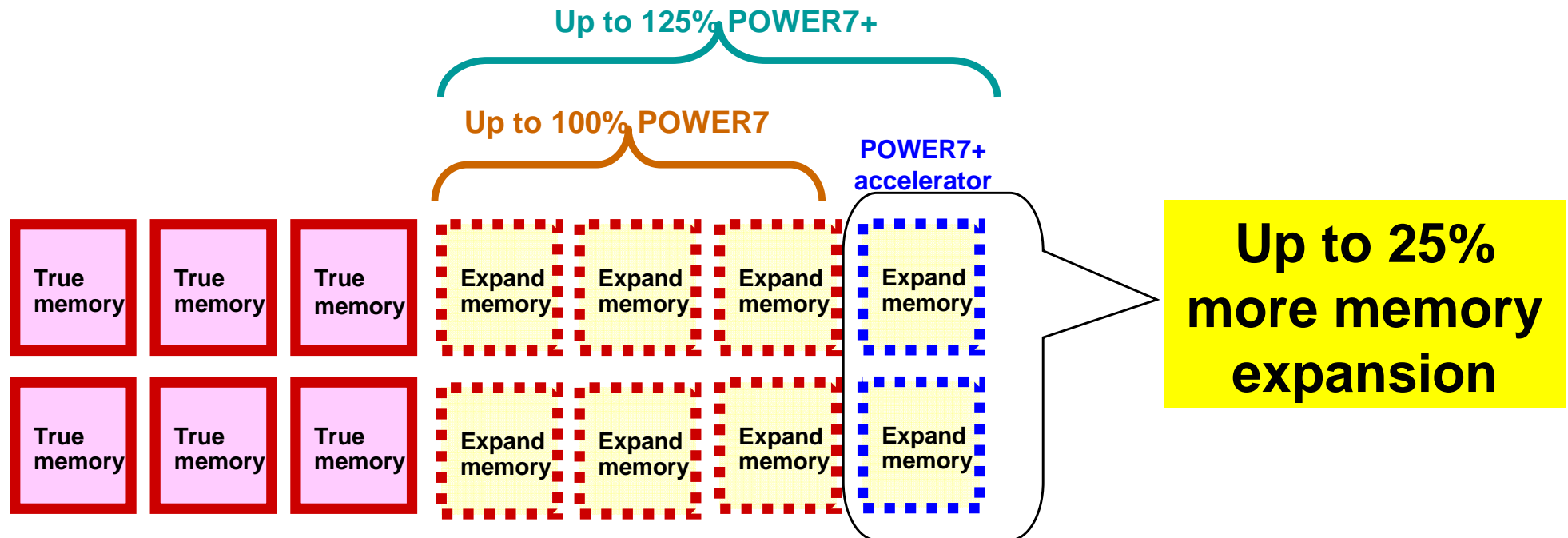


POWER7+ Active Memory Expansion

- POWER7+ AME Hardware Accelerator
 - Enhanced Power Systems value for AIX
 - On-chip enhancement

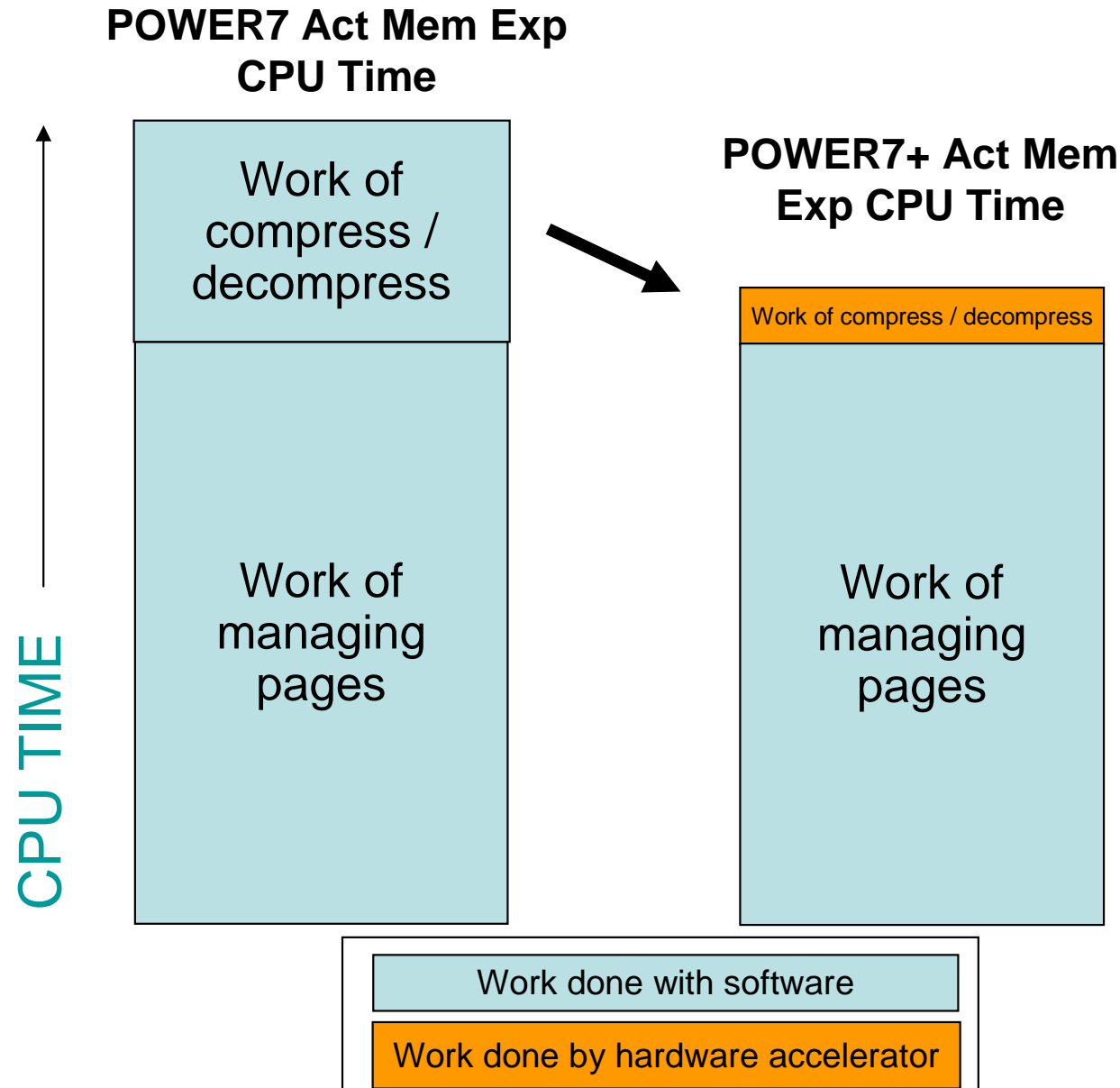


- Compared to POWER7, more efficient memory expansion (less processor overhead for the same compression/decompression – or even more equivalent memory for the same processor overhead)



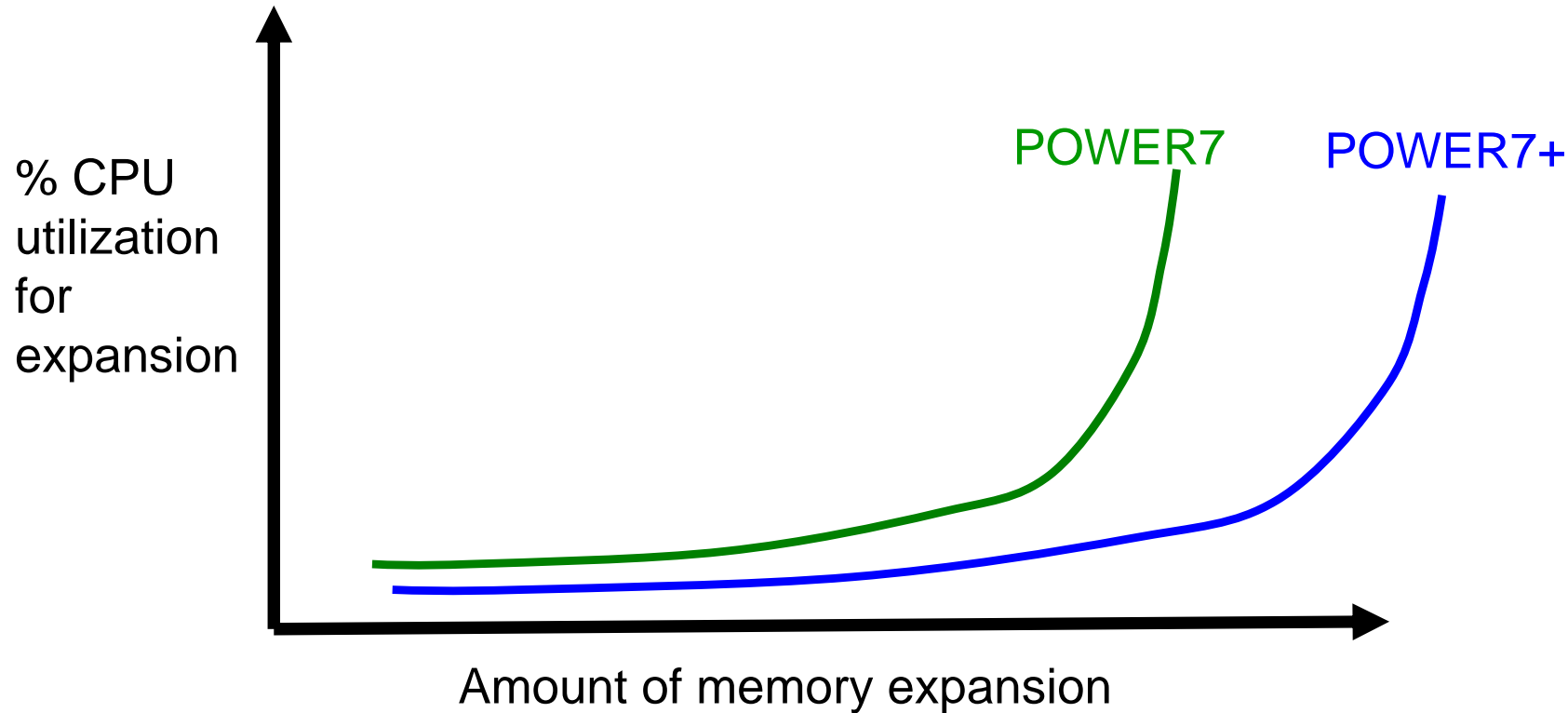
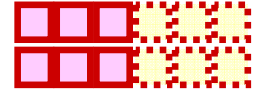
Note expansion percentage very workload dependent

Benefit of POWER7+ HW Accelerator



- **Less CPU for the same amount of memory expansion**
 - Can then run more partitions or work per partition
 - If fewer cores needed, may result in lower software licensing
- **OR more memory expansion for the same amount of processor**
 - Better able to relieve memory shortages and improve performance
 - May be able to do more work

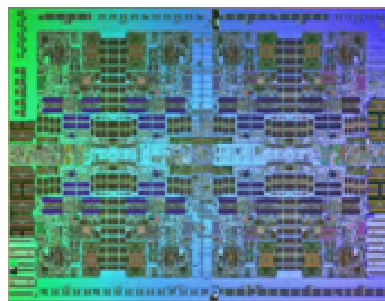
Active Memory Expansion - CPU & Performance



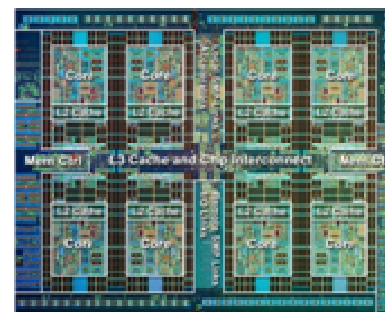
- POWER7+ uses on-chip hardware accelerator to do some of the compression / decompression work. There is a knee-of-cure relationship for CPU resource required for memory expansion
 - Even with POWER7+ hardware accelerator there is some resource required.
 - The more memory expansion done, the more CPU resource required
- Knee varies depending on how compressible memory contents are

POWER7 vs Intel Poulson

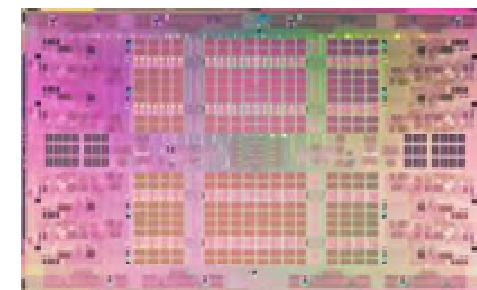
POWER7



POWER7+



Intel Poulson

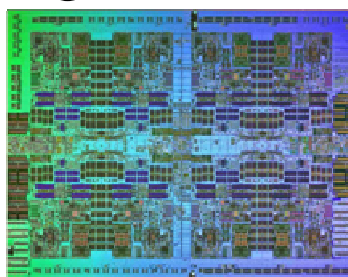


| | | | |
|-----------------------------|---|---------------------------|-----------------------------|
| Cores | 8 | 8 | 8 |
| Threads per Core | 4 | 4 | 2 |
| Frequency | 4.0 Ghz | 4.5 GHz | 2.53 GHz |
| Chip Size | 567mm2 | 567mm2 | 544 mm2 |
| Technology | 45nm SOI 11 LM EDRAM | 32nm SOI 13 LM Edram | 32nm 9 LM |
| Max Socket support | 32 | 32 | 32 |
| Power | 250 Watts | 250 Watts | 170 Watts |
| Spec_int Rate/Chip | 340 | 390 | 180 |
| Memory BW (70% utilization) | 96GB/s (16 DDR3 channels) | 96GB/s (16 DDR3 channels) | 45 GB/s (4 DDR3 channels) |
| L3 | 32MB | 80MB | 32MB |
| Extras | Advanced Prefetch HPC Features Energy management Turbo Mode/Core | Need to add | QPI busses to IO interfaces |

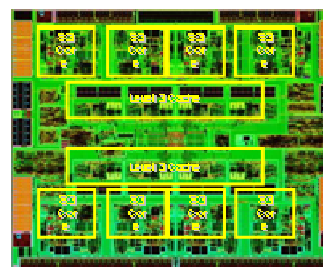
Chip Comparison

POWER7 vs Oracle T4

POWER7



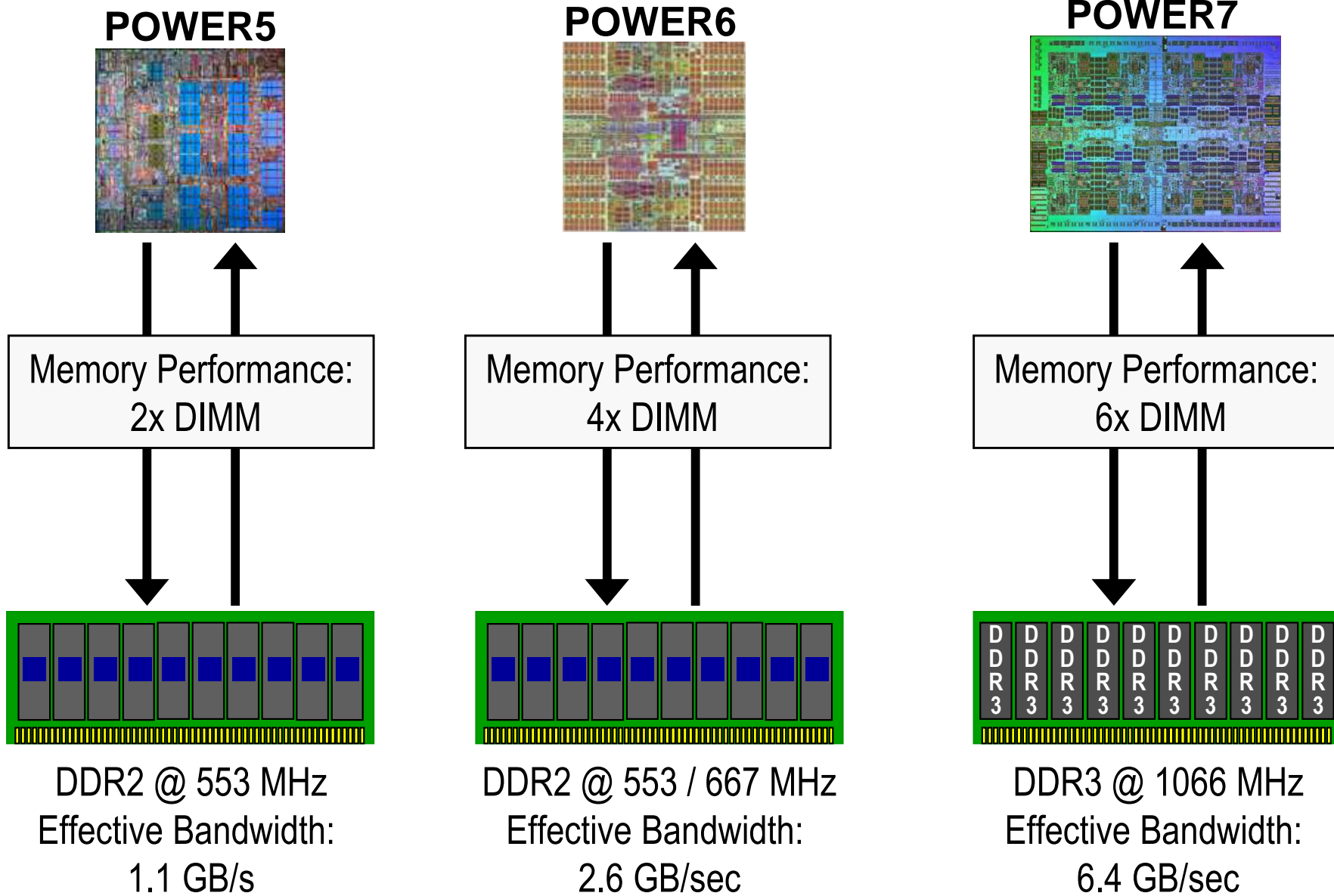
Oracle T4



Oracle T5

| | | | |
|------------------------------------|---|---|------------------------------------|
| Cores | 8 | 8 | 16 |
| Frequency | 4.0 Ghz | 3.0 Ghz | 3.6 GHz |
| Chip Size | 567mm2 | 403mm2 | 450 mm2 (est) |
| Technology | 45nm SOI 11 LM EDRAM | 40nm TSMC 12LM | 28nm TSMC xxLM |
| Max Socket support | 32 | 4 | 8 |
| Power | 250 Watts | 240 Watts | 240 Watts (est) |
| Spec_int Rate/Chip | 340 | 170 (est) | 300 (est) |
| Memory BW (70% utilization) | 96GB/s (16 DDR3 channels) | 24GB/s (4 DDR3 channels) | |
| L3 | 32MB | 4MB | 12MB |
| Extras | Advanced Prefetch HPC Features Energy management Turbo Mode/Core | 16 lanes PCI 2X10 Gb Enet Encryption/Decryption | 32 PCI lanes (est) 2X10 Gb Enet |

Memory Channel Bandwidth Evolution



POWER7+ technology in a mid-range system provides enterprise class availability, modular flexibility and Capacity on Demand for critical business workloads

■ *What's New*

- POWER7+ technology brings faster frequencies and larger L3 cache sizes which helps improve performance by over 20% on most workloads
- Hardware assisted memory compression helps reduce memory requirements without penalizing performance
- Hardware assisted AIX file system encryption improves security without penalizing performance
- Improved RAS and energy efficiency features improve system attractiveness
- Increased VM's per core improve virtualization efficiency

■ *Features / Business Value*

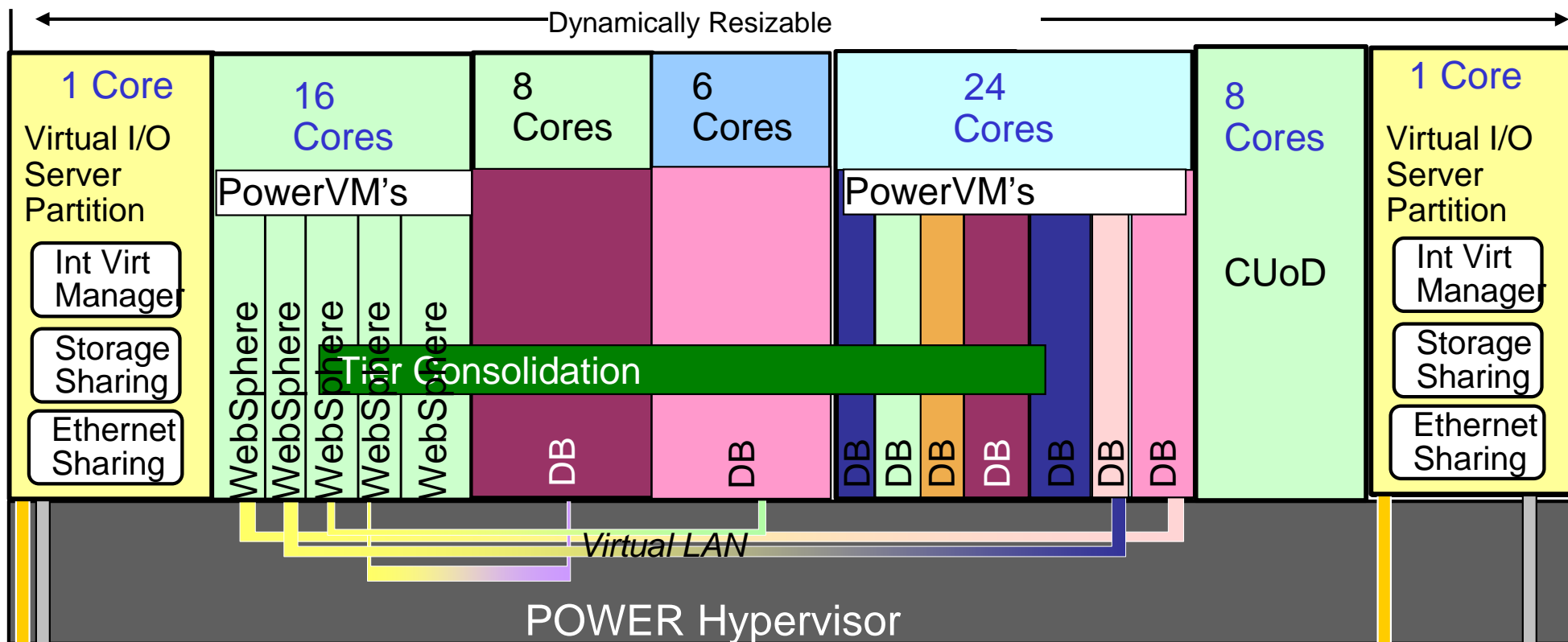
- Industry leading performance per system and per-core, especially OLTP/database applications
- Advanced virtualization capabilities including Micro-Partitions and the ability to move live applications from one physical system to another without user interruption which enables higher system utilization and efficiency
- Extraordinary reliability with comprehensive redundancy and system enablement for reduced unplanned downtime and elimination of planned application downtime
- Modular systems design, Utility CoD, and Hot-Node Add capabilities for easy "pay-as-you-grow" scenarios that respond quickly to change yet are easy on the bottom line
- Highly stable and reliable POWER roadmap

■ *Client Benefits*

- Easily handles virtualized consolidation of large mission critical applications and workloads
- Enables OLTP workloads to be managed in the most demanding service level agreements
- Supports highly secure environments for commercial applications
- Enables flexible, non-disruptive growth for highly available workloads

Power Systems Virtualization

- Tier Consolidation & Virtualization -



ISV Pricing on Power 64 core system

DB: 38 cores

WebSphere: 1920 PVUs

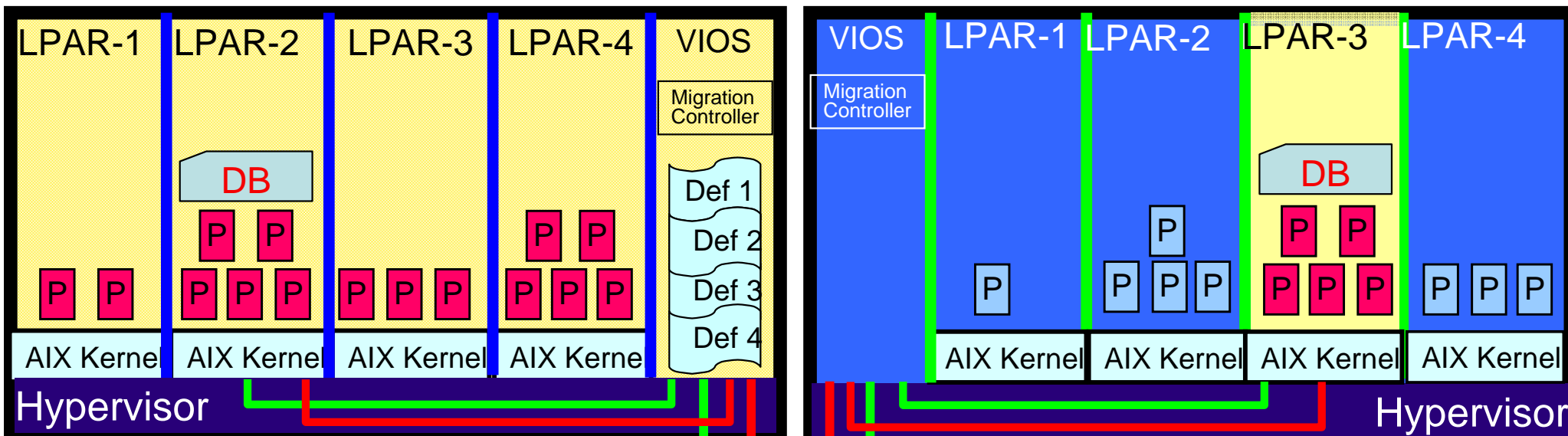
Do not pay for VIO server or CUoD cores



Virtual Network WebSphere to DB works at memory speeds

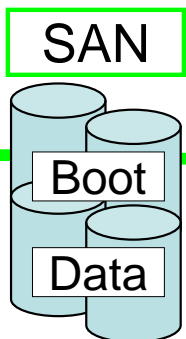
Live Partition Mobility On DB Workloads

Reduce impact of planned outages, relocate workloads to enable growth, provision new technology with no disruption to service



Partition Mobility Requires:

- POWER6
- AIX 5.3 / 6.1 or Linux
- All resources must be "Virtualized"
 - No real resources
- SAN storage environment
 - SAN Boot, temp space, same network



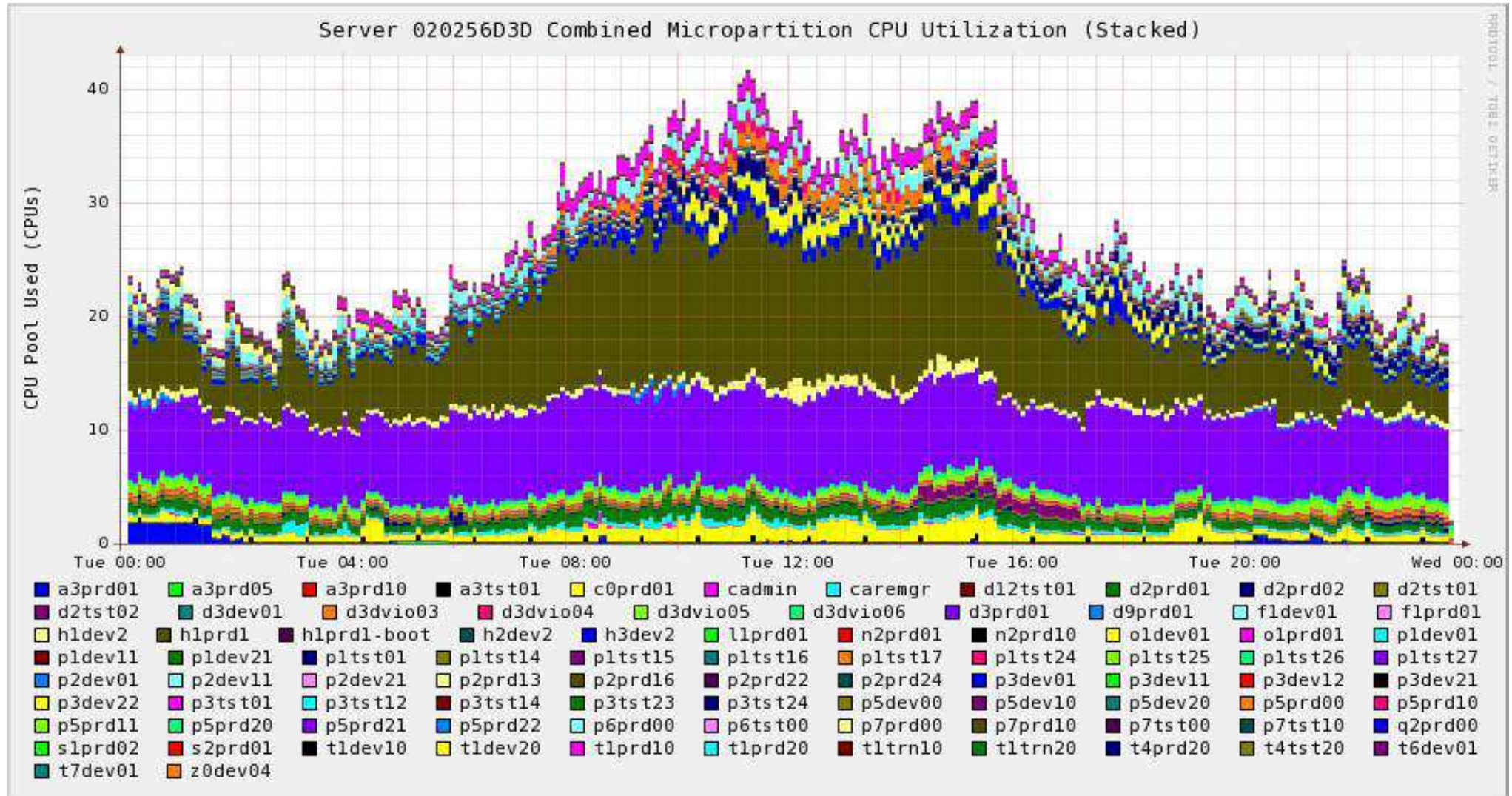
Ethernet

Partition Mobility Steps

- Validation
- Copy memory pages
 - ❖ Host to target systems
- Transfer
 - ❖ Turn off Host resources
 - ❖ Activate Target resources

The number of DB licenses needed does not change before and after the migration

Customer Shared Pool



POWER7+ RAS Feature Overview

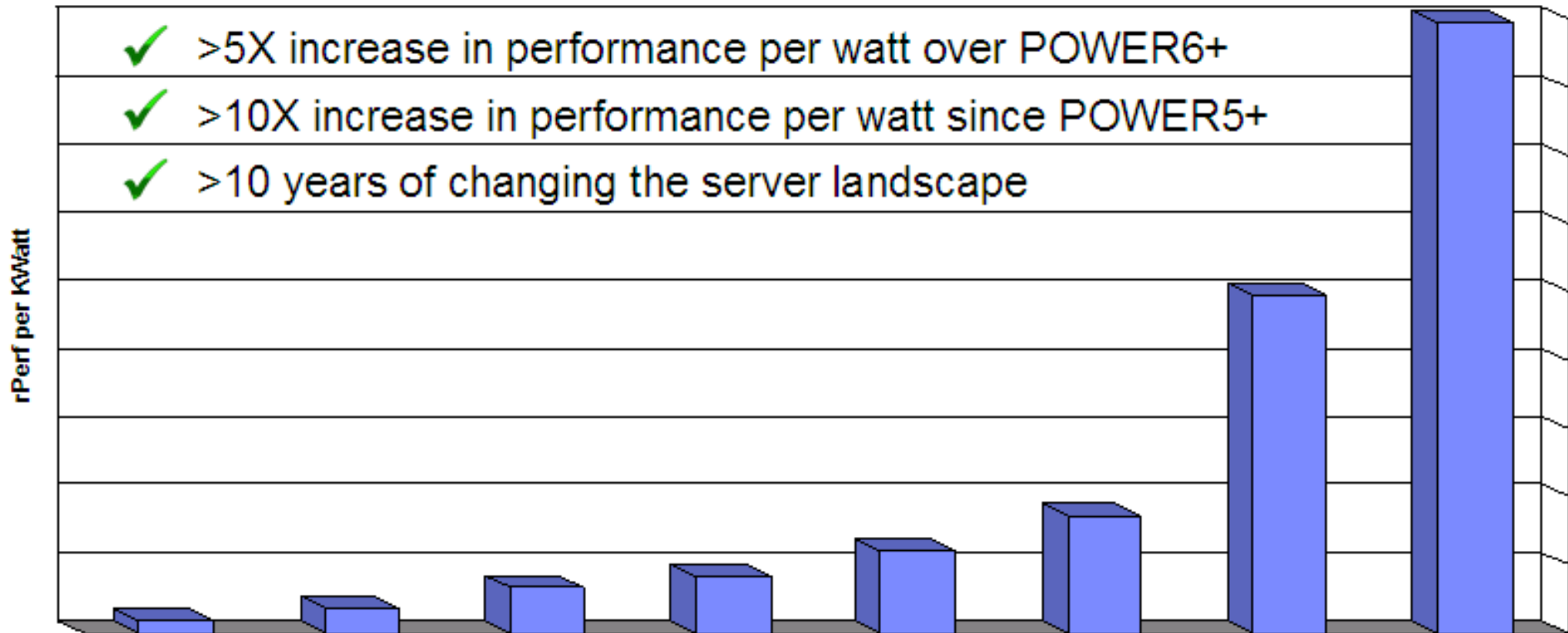
- Standard
- ◻ Optional
- Not Available

| RAS Item | Power 750+ | Power 760+ | Power 770+ | Power 780+ | Power 795 |
|---|------------|------------|------------|------------|-----------|
| Redundant / Hot Swap Fans & Blowers | ● | ● | ● | ● | ● |
| Hot Swap DASD / Media / PCI Adapters | ● | ● | ● | ● | ● |
| Concurrent Firmware Update | ● | ● | ● | ● | ● |
| Redundant / Hot Swap Power Supplies | ● | ● | ● | ● | ● |
| Dual disk controllers (split backplane) | ● | ● | ● | ● | ● |
| Processor Instruction Retry | ● | ● | ● | ● | ● |
| Alternate Processor Recovery | ● | ● | ● | ● | ● |
| Redundant / Hot Swap Power Regulators | ● | ● | ● | ● | ● |
| PowerVM™/Live Part. Mobility/Live App Mobility | ◻ | ◻ | ◻ | ◻ | ◻ |
| Dynamic Processor Sparing | — | ◻ | ◻ | ◻ | ◻ |
| Memory Sparing | — | — | ◻ | ◻ | ◻ |
| Redundant Service Processors | — | — | ●* | ●* | ● |
| Redundant System Clocks | — | — | ●* | ●* | ● |
| Hot GX Adapter Add and Cold Repair | — | — | ● | ● | ● |
| Hot-node Add / Cold-node Repair | — | — | ●* | ●* | ●* |
| Hot-node Repair / Hot-memory Add | — | — | ●* | ●* | ●* |
| Dynamic Service Processor & System Clock Failover | — | — | ●* | ●* | ● |
| Hot-node Repair / Hot-memory Add for all nodes** | — | — | ●* | ●* | ●* |
| Enterprise Memory | — | — | ● | ● | ● |
| Hot GX Adapter Repair | — | — | ● | ● | ● |
| Active Memory Mirroring for Hypervisor | — | — | ◻ | ● | ● |
| Power Pools | — | — | — | ● | ● |

* Requires two or more nodes



POWER7+ continues to deliver more Performance per Watt



| | | | | | | | |
|--|---|---|--|---|--|---|---|
| POWER4™ p670 1.1 GHz rPerf: 24.46 KWatts: 6.71 | POWER4+™ p670 1.5 GHz rPerf: 46.79 KWatts: 6.71 | POWER5™ p5-570 1.65 GHz rPerf: 68.4 KWatts: 5.2 | POWER5+™ p570 1.9 GHz rPerf: 85.20 KWatts: 5.2 | POWER6™ Power 570 4.7 GHz rPerf: 134.35 KWatts: 5.6 | POWER6+™ Power 570 4.2 GHz rPerf: 193.25 KWatts: 5.6 | POWER7™ Power 780 3.8 GHz rPerf: 685.09 KWatts: 6.9 | POWER7+™ Power 780 3.7 GHz rPerf: 1380.19 KWatts: 7.7 |
|--|---|---|--|---|--|---|---|

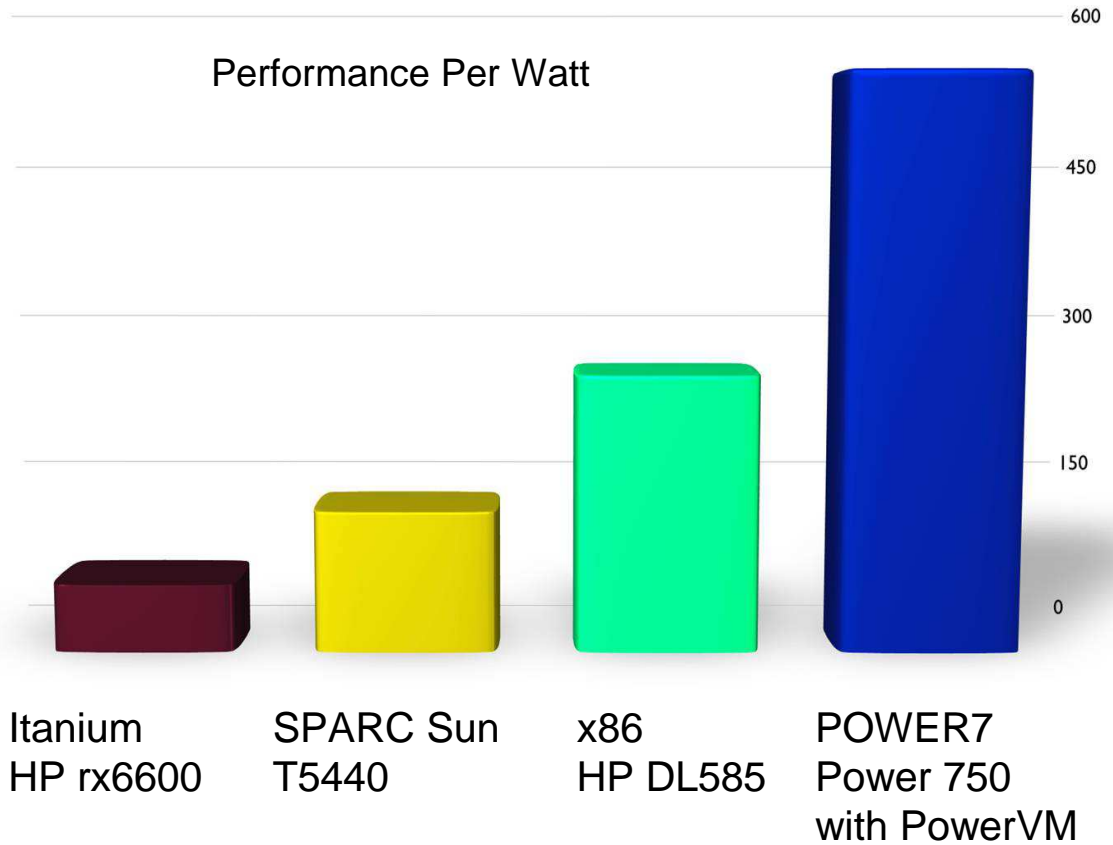
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The first Energy Star certified RISC system

Power 750



Most energy efficient systems



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- ✓ Availability
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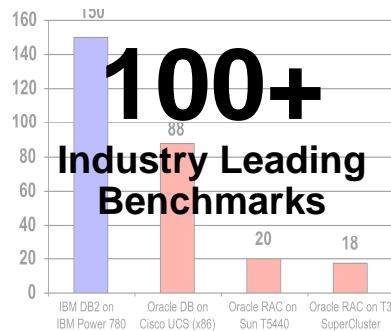


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transforming industry innovation



Top 500

Powering 5 of the world's top 10 supercomputers



9,000+
Patents since 2001

3,000+
Competitive migrations 1Q 2010-3Q 2012



CPW

GHz (#core/socket) : CPW (# core)

| | |
|---|---|
| <p>POWER7+ 710 3.6 GHz (4): 28,400 (4) 4.2 GHz (6): 49,400 (6) 4.2 GHz (8): 64,500 (8)</p> | <p>POWER7+ 730 4.3 GHz (4): 59,700 (8) 4.2 GHz (6): 89,200 (12), 3.6 GHz (8): 104,700 (16) 4.2 GHz (8): 117,600 (16)</p> |
| <p>POWER7+ 720 3.6 GHz (4): 28,400 (4) 3.6 GHz (6), 42,400 (6), 3.6 GHz (8): 56,300 (8)</p> | <p>POWER7+ 740 4.2 GHz (6): 49,000 (6), 91,700 (12) 3.6 GHz (8): 56,300 (8), 106,500 (16) 4.2 GHz (8): 64,500 (8), 120,000 (16)</p> |
| <p>POWER7+ 750 3.5 GHz (8): 52,000(8), 96,000(16), 141,500(24), 185(32) 4.0 GHz (8): 59,000(8), 108,000(16), 158,000(24), 208,000(32)</p> | |
| <p>POWER7+ 760 3.1 GHz (12): 69,800(12), 129,000(24), 194,700(36), 258,000(48) 3.4 GHz (12): 75,200(12), 137,000(24), 209,000(36), 274,000(48)</p> | |

rPerf

GHz (#core/socket) : rPerf (# core)

| | |
|---|--|
| <p>POWER7+ 710</p> <p>3.6 GHz (4): 53.9 (4) 4.2 GHz (6): 90.6 (6) 4.2 GHz (8): 115.5 (8)</p> | <p>POWER7+ 730</p> <p>4.3 GHz (4): 120.4 (8), 4.2 GHz (6): 176.6 (12), 3.6 GHz (8): 197.7 (16) 4.2 GHz (8): 223.1 (16)</p> |
| <p>POWER7+ 720</p> <p>3.6 GHz (4): 53.9 (4) 3.6 GHz (6), 79.5 (6), 3.6 GHz (8): 102.4 (8)</p> | <p>POWER7+ 740</p> <p>4.2 GHz (6): 90.6 (6), 176.6 (12) 3.6 GHz (8): 102.4 (8), 197.7 (16) 4.2 GHz (8): 115.5 (8), 223.1 (16)</p> |
| <p>POWER7+ 750</p> <p>3.5 GHz (8): 104.5 (8), 197.0 (16), 275.9 (24), 354.9 (32) 4.0 GHz (8): 117.1 (8), 220.7 (16), 309.2 (24), 397.7 (32)</p> | |
| <p>POWER7+ 760</p> <p>3.1 GHz (12): 142.1 (12), 264.8 (24), 370.7 (36), 476.7 (48) 3.4 GHz (12): 151.4 (12), 282.1 (24), 395.0 (36), 507.8 (48)</p> | |

Q & A

IBM Power Systems

5 February 2013 Announcement
Hardware Deep Dive



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Revised September 26, 2006

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Fußnoten zum vorherigen Slide

Reference the PowerLinux 7R2 SAP SD 2-Tier Performance chart in the 710/730/7R2 section

- (1) The SAP Sales and Distribution (SD) Standard Application Benchmark performed on December 9, 2012 by IBM in Austin, TX, USA, has been certified with the following data: Number of SAP SD benchmark users: 8,016, Average dialog response time: 0.98 seconds, Throughput: Fully processed order line 876,000 items/hour, Dialog steps/hour: 2,628,000, SAPS: 43,800, Average database request time 0.020 sec / 0.018 sec (dialog/update): CPU utilization of central server: 99% Operating system, central server: SUSE Linux Enterprise Server 11 SP2, RDBMS: DB2 10, SAP Business Suite software: SAP enhancement package 5 for SAP ERP 6.0, Configuration: Central server: IBM PowerLinux 7R2, 2 processors / 16 cores / 64 threads, IBM POWER7+, 4.22 GHz, 32 KB (I) and 32 KB (D) L1 cache, and 256 KB L2 cache per core, 10 MB L3 cache per core, 256 GB main memory. The SAP certification number was not available at press time and can be found at the following Web page:
www.sap.com/benchmark

- (2) The SAP Sales and Distribution (SD) Standard Application Benchmark performed on December 24, 2012 by Cisco Systems in Walldorf, Germany, was certified on January 8, 2013, with the following data: Number of SAP SD benchmark users: 6,530 Average dialog response time: 0.98 seconds, Throughput: Fully processed order line items per hour: 713,670, Dialog steps per hour: 2,141,000, SAPS: 35,680 Average database request time (dialog/update): 0.015 sec / 0.036 sec, CPU utilization of central server: 99% Operating system, central server: Red Hat Enterprise Linux 6.3 RDBMS: Sybase ASE 15.7 SAP Business Suite software: SAP enhancement package 5 for SAP ERP 6.0 Configuration: Central server: Cisco UCS B200 M3, 2 processors / 16 cores / 32 threads, Intel Xeon Processor E5-2690, 2.90 GHz, 64 KB L1 cache and 256 KB L2 cache per core, 20 MB L3 cache per processor, 256 GB main memory

Notes on benchmarks and values

The IBM benchmarks results shown herein were derived using particular, well configured, development-level and generally-available computer systems. Buyers should consult other sources of information to evaluate the performance of systems they are considering buying and should consider conducting application oriented testing. For additional information about the benchmarks, values and systems tested, contact your local IBM office or IBM authorized reseller or access the Web site of the benchmark consortium or benchmark vendor.

IBM benchmark results can be found in the IBM Power Systems Performance Report at http://www.ibm.com/systems/p/hardware/system_perf.html.

All performance measurements were made with AIX or AIX 5L operating systems unless otherwise indicated to have used Linux. For new and upgraded systems, the latest versions of AIX were used. All other systems used previous versions of AIX. The SPEC CPU2006, LINPACK, and Technical Computing benchmarks were compiled using IBM's high performance C, C++, and FORTRAN compilers for AIX 5L and Linux. For new and upgraded systems, the latest versions of these compilers were used: XL C for AIX v11.1, XL C/C++ for AIX v11.1, XL FORTRAN for AIX v13.1, XL C/C++ for Linux v11.1, and XL FORTRAN for Linux v13.1.

For a definition/explanation of each benchmark and the full list of detailed results, visit the Web site of the benchmark consortium or benchmark vendor.

| | |
|-----------------------------|---|
| TPC | http://www.tpc.org |
| SPEC | http://www.spec.org |
| LINPACK | http://www.netlib.org/benchmark/performance.pdf |
| Pro/E | http://www.proe.com |
| GPC | http://www.spec.org/gpc |
| VolanoMark | http://www.volano.com |
| STREAM | http://www.cs.virginia.edu/stream/ |
| SAP | http://www.sap.com/benchmark/ |
| Oracle, Siebel, PeopleSoft | http://www.oracle.com/apps_benchmark/ |
| Baan | http://www.ssaglobal.com |
| Fluent | http://www.fluent.com/software/fluent/index.htm |
| TOP500 Supercomputers | http://www.top500.org/ |
| Ideas International | http://www.ideasinternational.com/benchmark/bench.html |
| Storage Performance Council | http://www.storageperformance.org/results |

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For a definition/explanation of each benchmark and the full list of detailed results, visit the Web site of the benchmark consortium or benchmark vendor.

| | |
|-----------------------|---|
| SPEC | http://www.spec.org |
| LINPACK | http://www.netlib.org/benchmark/performance.pdf |
| Pro/E | http://www.proe.com |
| GPC | http://www.spec.org/gpc |
| STREAM | http://www.cs.virginia.edu/stream/ |
| Fluent | http://www.fluent.com/software/fluent/index.htm |
| TOP500 Supercomputers | http://www.top500.org/ |
| AMBER | http://amber.scripps.edu/ |
| FLUENT | http://www.fluent.com/software/fluent/fl5bench/index.htm |
| GAMESS | http://www.msg.chem.iastate.edu/gamess |
| GAUSSIAN | http://www.gaussian.com |
| ANSYS | http://www.ansys.com/services/hardware-support-db.htm |
| | Click on the "Benchmarks" icon on the left hand side frame to expand. Click on "Benchmark Results in a Table" icon for benchmark results. |
| ABAQUS | http://www.simulia.com/support/v68/v68_performance.php |
| ECLIPSE | http://www.sis.slb.com/content/software/simulation/index.asp?seg=geoquest& |
| MM5 | http://www.mmm.ucar.edu/mm5/ |
| MSC.NASTRAN | http://www.mssoftware.com/support/prod%5Fsupport/nastran/performance/v04_sngl.cfm |
| STAR-CD | www.cd-adapco.com/products/STAR-CD/performance/320/index/html |
| NAMD | http://www.ks.uiuc.edu/Research/namd |
| HMMER | http://hmmer.janelia.org/ |
| | http://powerdev.osuosl.org/project/hmmerAltivecGen2mod |

Revised December 2, 2010

Notes on performance estimates

rPerf for AIX

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Revised April 2, 2007