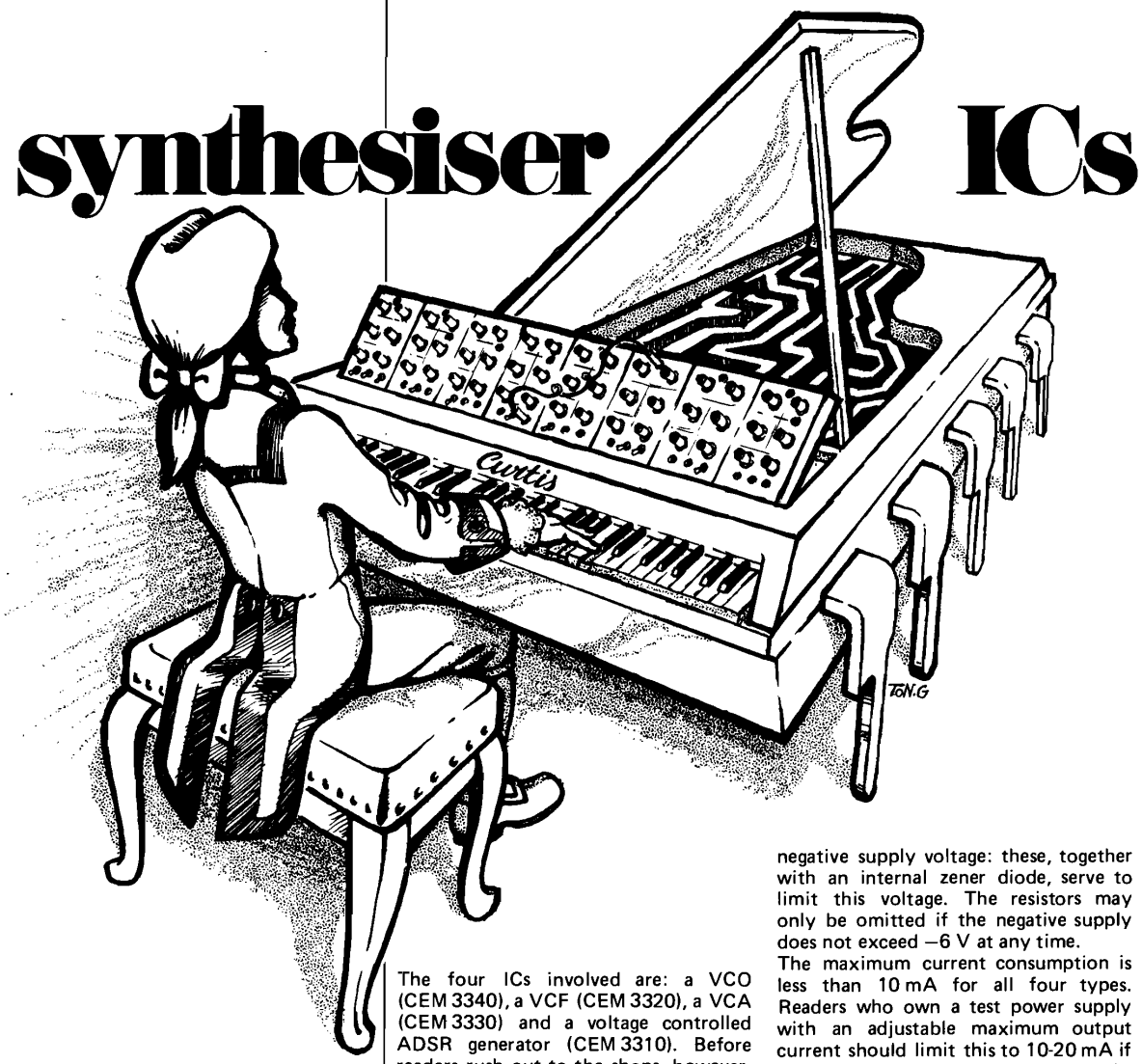
H.P. Baumann

synthesiser ICs



makes building synthesisers less of a headache

The American Curtis company has recently introduced a set of special music synthesiser ICs onto the market. These 'musical chips' have now found their way across the Atlantic and are well worth looking at (and listening to). The following analysis weighs up the pros and the cons.

The four ICs involved are: a VCO (CEM 3340), a VCF (CEM 3320), a VCA (CEM 3330) and a voltage controlled ADSR generator (CEM 3310). Before readers rush out to the shops, however, it should be mentioned that although their quality is very good, this does not herald the 'perfect IC', able to do anything. This simply does not exist. However, the ICs we're about to introduce are very clever, but nonetheless still require the assistance of a few other components. Readers will find the ICs to be quite useful – provided they are properly used. So if you are thinking about building a synthesiser based on the Curtis ICs, take heed of the following information and advice . . . and read the next issue of Elektor, there is definitely something up the editorial sleeve!

General remarks

Although the chips are fairly rugged, 24 volts between any two pins will almost certainly lead to sudden death. The supply voltage should not exceed 18 V. The data sheets show that series-resistors must be included to limit the negative supply voltage: these, together with an internal zener diode, serve to limit this voltage. The resistors may only be omitted if the negative supply does not exceed –6 V at any time.

The maximum current consumption is less than 10 mA for all four types. Readers who own a test power supply with an adjustable maximum output current should limit this to 10-20 mA if they intend to use it to power the circuit. This affords protection in the event of a short circuit – the chips are not designed to survive one!

One further warning: don't add capacitors when the power is still 'on'. This could cause voltage transients which would immediately send the IC to 'the big siliconmaker in the sky'. Thus, the warning in the data sheet 'not short circuit proof' is to be taken quite literally!

The voltage controlled oscillator CEM 3340

The block diagram in figure 1 shows that the IC contains all the bits that are needed to convert a control voltage into an output frequency. Input adders, temperature compensated exponential converters, and VCO; and resonance frequency converters for triangle and square waves, pulse width modulation and sawtooth.

Temperature compensation works here

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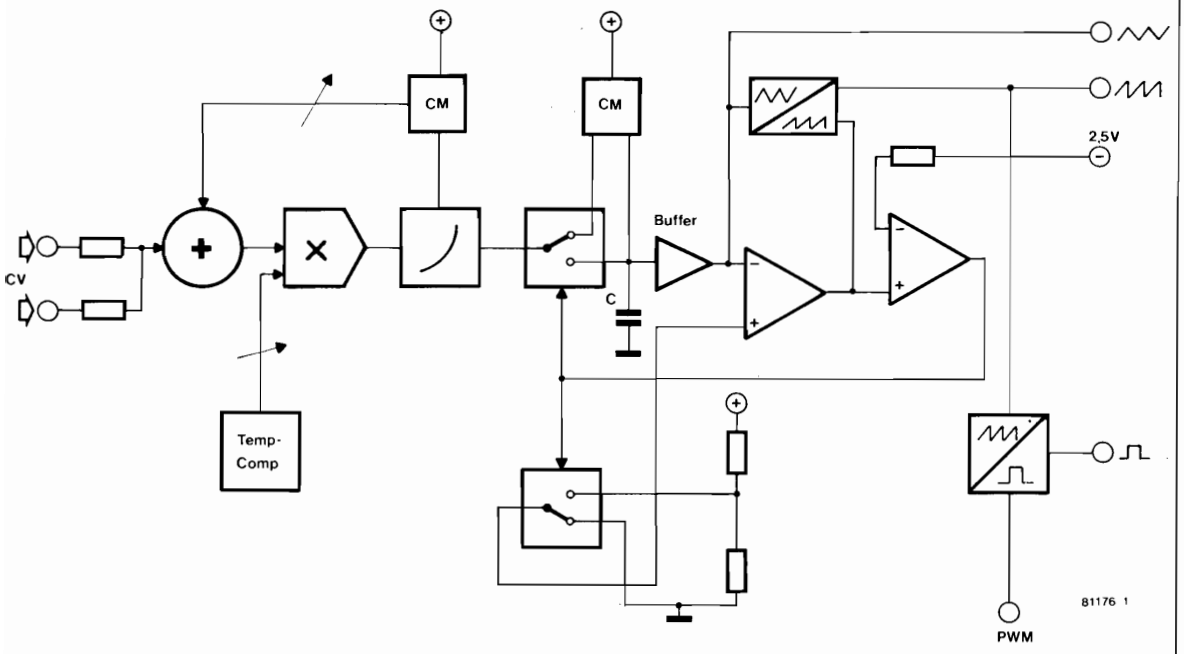

Figure 1. The block diagram of the CEM 3340. It contains all the components required to construct an exponential synthesizer VCO: input adders, a temperature compensated exponentiator, a triangle oscillator, a triangle-to-sawtooth and sawtooth-to-squarewave converter. The latter has a control input for pulse width modulation. The IC is highly suitable for use in precision function and wobble generators.

on the basis of multiplying the VCO's current with a coefficient which is derived from the absolute temperature. Provided this coefficient is correctly adjusted, variations in the exponential converter's temperature will be completely compensated.

The exponential converter's operating range covers a total ratio of 1:500,000; the highest accuracy is in the operating current range between 50 nA and 100 μA. In the 5 Hz . . . 10 kHz frequency range C_F = 1 nF is a reasonable value. It is preferable to use good quality capacitors (such as polycarbonate types).

The reference current is set by means of R_R. In the interests of optimum linearity and stability, this current should be between 3 and 15 μA. The value of the summing resistors at the input adder (pin 15) should be 100 k, to provide the 1 V per octave standard control feature.

In principle, it is quite possible to obtain a precise linear volts-per-octave curve by calibrating every single summing resistor. It is simpler, however, to use a preset potentiometer as part of R_Z, since this acts on the total summed control voltage.

Once the temperature effects have been fully compensated and the conversion factor has been set at 1 V per octave, discrepancies in the exponential curve for the frequency range above 3 . . . 5 kHz have still to be ironed out. Due to various effects (the transistors' base-spreading resistance, which becomes increasingly important at higher control currents, and the internal comparator's delay time) the higher frequencies tend to go 'flat'. One way to compensate for this has been provided: using a current mirror, part of the exponential converter output current is fed to pin 7. This is converted into a voltage, and a fraction of this is fed back to the input adder. In this way, an increasing control voltage is produced at the VCO for higher frequencies. Provided the level is correct, this will straighten out the volts-per-octave curve.

Practical results

Although the circuit provided in the Curtis data sheet does work (figure 1), it is not advisable to use it in this simplified form. The manufacturer states that the VCO IC can be operated on +15 V/ −15 V, but omits to mention that the positive voltage should be adequately stabilised.

The reason for this can be seen in figure 1. The reference voltage for the upper threshold of the comparator is derived directly (at pin 9) from the positive supply voltage with the aid of two integrated resistors of 14.4 k and 7.2 k, respectively. However, since the control voltage for the oscillator is not affected by the supply voltage, every ripple in the positive supply will greatly affect the output frequency. The same is true, to a lesser extent, for the negative voltage: the internal 6.5 V zener diode serves to protect the circuit against excessive voltages – it is not intended as a voltage regulator. If its temperature stability has been better, things might have been different. As it stands, however, the potential at pin 3 alters when the temperature changes, taking the voltage across R_Z and R_T with it. The best results are obtained by stabilising both supply voltages and by leaving the internal zener diode out of action.

A further point concerns the supply voltages. The full +/−15 V has been found to increase the chip's leakage currents considerably. This leads to excessive drift and poor linearity. In general, therefore, the supply voltages should be kept as low as possible.

Also apparent from figures 1 and 2 is the fact that the buffered triangular wave form is connected to pin 10. Without any further buffering this is only suitable for constant loads due to the relatively high output resistance. Even a 100 k load will shift the oscillator frequency by 0.15%. This is not surprising, considering that the same (internal) buffer stage also drives the

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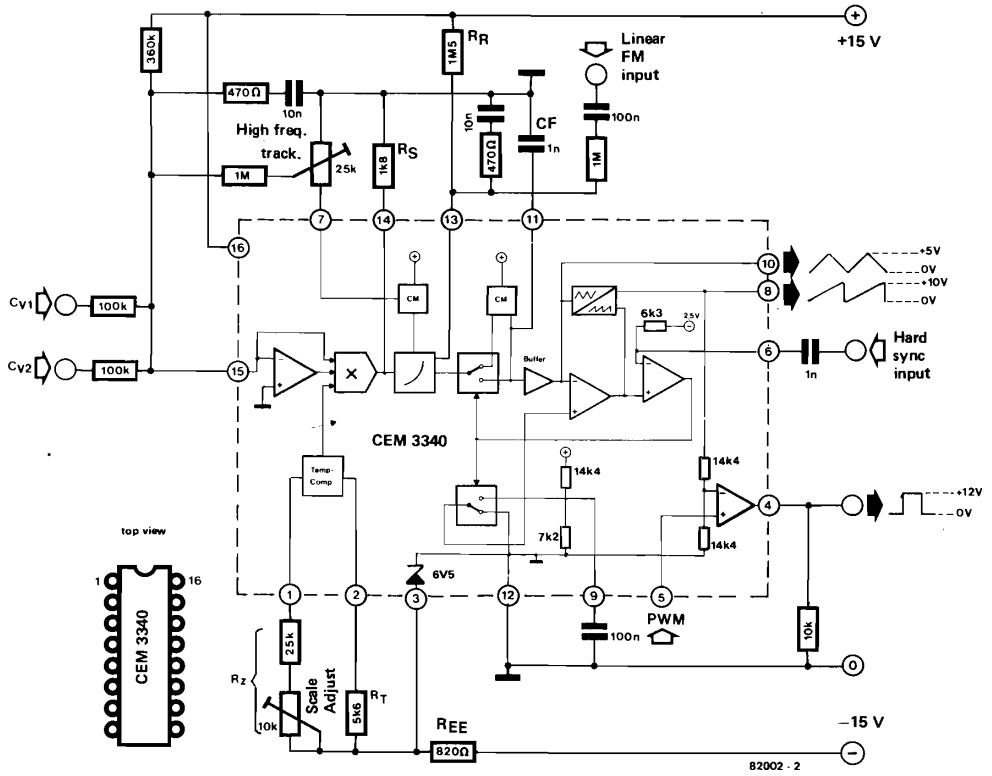

Figure 2. The practical circuit, as suggested by the manufacturer, involves very few components.

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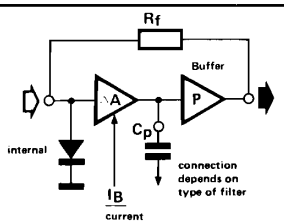

Figure 3. The block diagram of one filter stage in the CEM 3320. This IC contains four of these stages.

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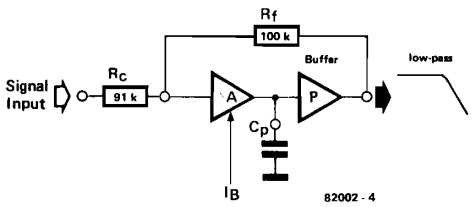

Figure 4. One filter stage connected as a low-pass filter with a slope of 6 dB per octave and unity gain in the passband.

comparator: its output impedance together with the load resistance make a voltage divider which alters the switching threshold. Thus, where variable loads are involved, an external buffer stage at pin 10 is indispensable.
Whereas the frequency drift values using the IC in the manner indicated in the data sheet (and figure 1) were around 0.25% per hour at even highly stable operating voltages, the circuit in figure 2 will give a drift of only 0.08% per hour.

The filter IC: CEM 3320

The CEM 3320 chip is a 24 dB filter, consisting of four identical filter sec-

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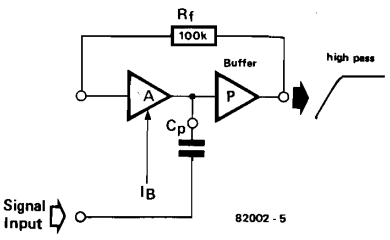

Figure 5. A 6 dB per octave high-pass filter, again with unity gain in the passband.

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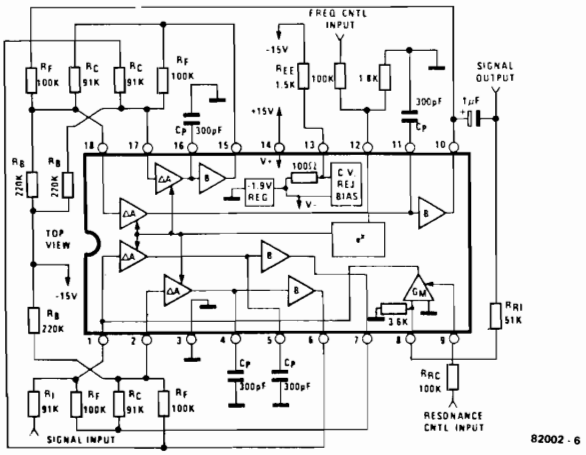

Figure 6. The circuit diagram of a 3320 connected as a 24 dB per octave low-pass filter. A special feature is the filter resonance voltage control system (Q factor), using a transconductance (G_M) amplifier as an electronic potentiometer.

tions of the type shown in figure 3. Operation is simple. Each section produces a filter 'pole' with the aid of a variable-gain amplifier Δ_A, a capacitor C_p and a buffer amplifier. The latter ensures a low output impedance. The variable-gain amplifier is current-driven, both at the signal and control inputs. Moreover, it is fully temperature compensated.

The centre frequency is calculated as follows:

$$f_c = \frac{A_{IO}}{2\pi R_{EQU}} \cdot e^{-V_c/V_t}$$

where A_{IO} represents the current gain of the first stage at zero control current (typical value = 0.9) and R_{EQU} stands for the actual feedback resistance (this is determined mainly by R_f; the typical value is 91 k). V_c is the control voltage at pin 12 of the IC and V_t the 'temperature voltage' (about 26 mV at room temperature).

Figure 4 shows a stage connected as a low-pass filter. The input signal is fed in through a resistor R_c = 91 k; this sets the overall gain to unity. The filter capacitor is grounded. In the same straightforward manner, a 6 dB high-pass filter may be constructed (see figure 5). The signal is now fed in through C_p. R_c is omitted in this case to obtain unity gain.

The complete internal block diagram of the IC is shown in figure 6. All the variable-gain stages Δ_A are internally linked to the output of an exponential converter.

In order to be able to vary the resonance of the filter (right up to the point where it oscillates!) a common transconductance amplifier G_M has been integrated on the chip. This simply acts as a VCA to vary the 'overall' feedback signal.

The best output range and least 'break-through' of the control voltage is obtained at a quiescent buffer output voltage of 0.46 V_{CC}, thus at 15 V this will be 6.9 V.

The filter circuit

Figure 7 gives a clearer view of a complete 24 dB low-pass filter. The circuit contains all the components required to buffer and adjust the system. An input adder has been connected to pin 12, for multiple control voltages. This neatly takes care of one further point: the basic circuit given in figure 4 would provide a filter cut-off frequency that *drops* when the control voltages *rises*. The inverting adder stage ensures that a rise in control voltage will correspond to a rise in the cut-off frequency.

This circuit allows a range of 10 octaves to be covered with great accuracy. P1 sets the lowest frequency (for zero control voltage). P2 is used to minimise break-through of the 'resonance' control voltage to the output; P3 does the same job for the filter frequency control voltage. P3 is the easiest to adjust, by con-

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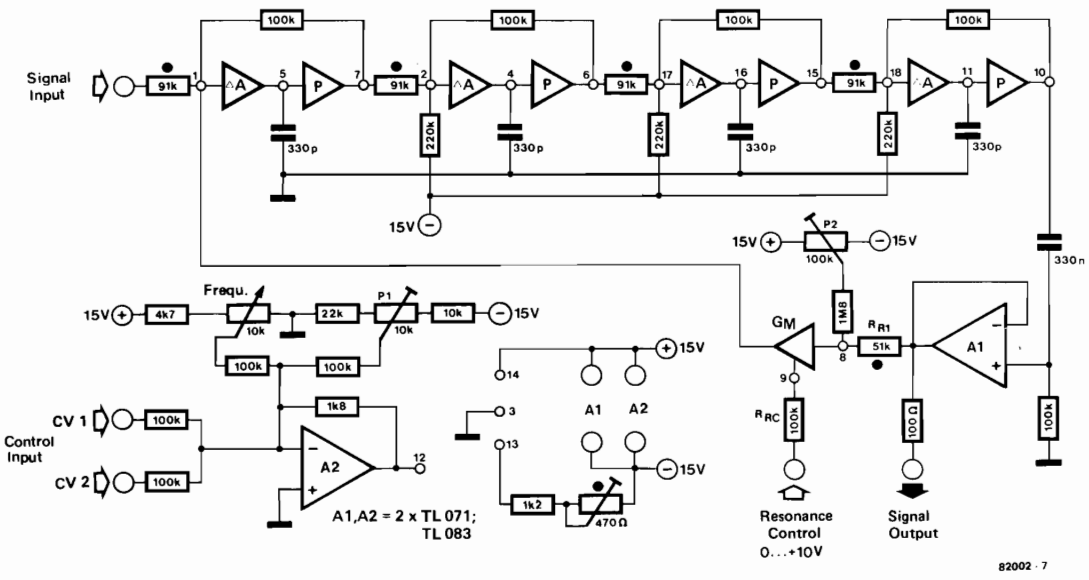

Figure 7. The complete, tested circuit of a 24 dB VCF (low-pass) using the CEM 3320. When high stability requirements need to be met (if the filter is used as a sine wave VCO, for instance) the resistors and potentiometers that are marked with a dot should be metal foil and Cermet types.

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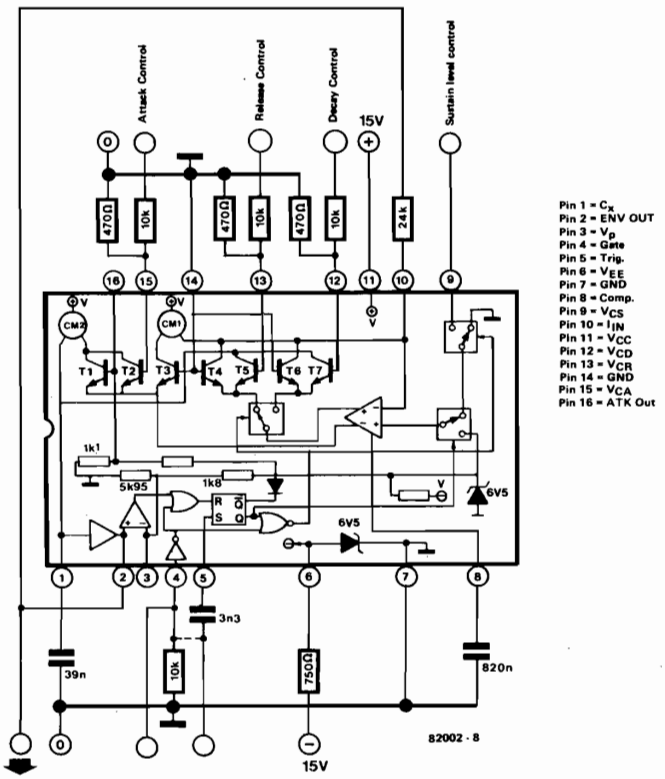

Figure 8. The circuit diagram of the CEM 3310 envelope generator. Very few additional components are required. The normal ADSR envelope voltage is produced.

necting a ± 300 Hz square wave signal and a full 0 . . . +10 V swing (control voltage range!) to either CV1 or CV2. With no input signal applied, the level at the filter output is reduced to a minimum with P3.

Practical results

The noise level of the circuit given in figure 7 proved to be around 78 dB, which is well within the manufacturer's specifications. Distortion is low: around 0.12% depending on the frequency and signal amplitude. The break-through of a 10 V control voltage jump was found to be only 25 mV once P3 was calibrated (52 dB below the signal level, in other words). At the output, the resonance control voltage was measured as —40 dB.

The maximum output signal of the filter was around 13 V peak-to-peak. When used as an oscillator a fairly symmetrical sine wave form was obtained.

The transition from filter to oscillator is remarkably smooth. The filters did not 'howl' at critical points like some of their counterparts. This is partly due to the uncritical type of filter used and partly to the modified linear curve featured by the resonance VCA. At higher values the feedback slows down and so allows for fine adjustment.

Since the remaining temperature drift is around 0.3% per degree centigrade, it is hardly worth compensating. As far as filters are concerned, the total drift may

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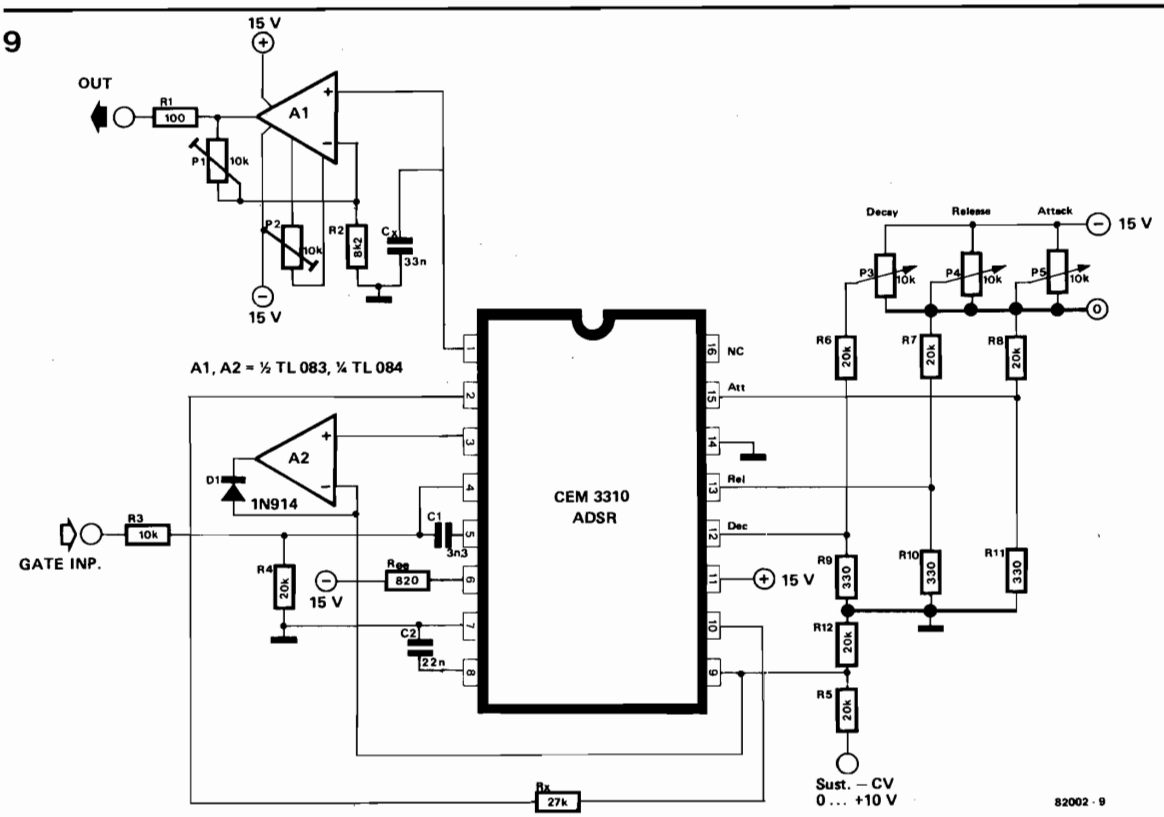

Figure 9. The complete circuit diagram for a standard ADSR generator using the CEM 3310.

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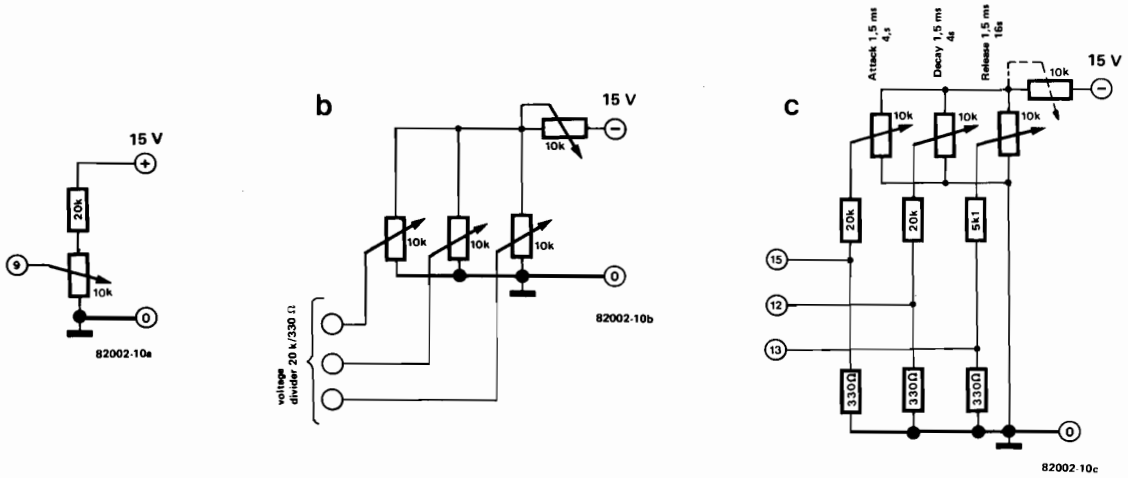

Figure 10. Potentiometers offer various preset facilities in the envelope generator in figure 9. Figure 10a shows a possible sustain preset and figure 10b shows how the Attack, Decay and Release times can be adjusted simultaneously with the aid of an additional potentiometer.

well be 6% (at 20° temperature change, for instance) and still not affect the filters, quite apart from the fact that such drastic changes in temperature hardly ever occur.

The envelope generator CEM 3310 IC

The IC requires very few external components, as shown in figure 8, and has excellent features. The attack-decay-sustain-release times are voltage controlled over an (exponential) range of about 1 : 50,000. The conversion factor is 60 mV per decade, which corresponds to 18 mV per octave. Over an operating range of 1 : 10,000 the voltage must therefore vary by 240 mV. This can be done with the aid of a voltage divider which derives the voltage from the supply. The sustain level is determined by a linear control voltage.

If several envelope generators are used, all the control voltage inputs can be driven in parallel from a single potentiometer. A good control range is obtained when C_X is 33 . . . 68 nF. R_X should not be more than 240 k when the internal buffer is used and not more than 1 M when an external FET opamp acts as a buffer. The time values are smallest at 0 V and increase when the control voltage becomes negative. The circuit in figure 8 gives the longest periods for −5 V at the control inputs (corresponds to −240 mV at the pins). The sustain level voltage must be in the 0 . . . +5 V range.

Figure 9 shows an example of an envelope generator using the CEM 3310. Potentiometers are provided to set the period times and there is a control input for the sustain level.

The envelope signal is produced across C_X. P1 sets the gain of the output amplifier, A1; P2 sets the output slightly negative (about −10 mV) under

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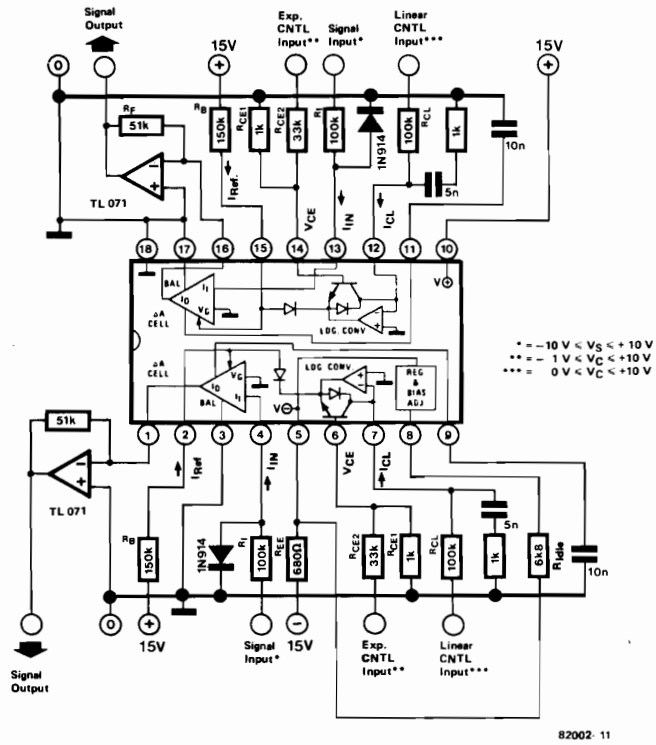

Figure 11. The circuit diagram of the DUAL VCA CEM 3330. This IC contains two voltage controlled amplifiers which can be operated either linearly or exponentially.

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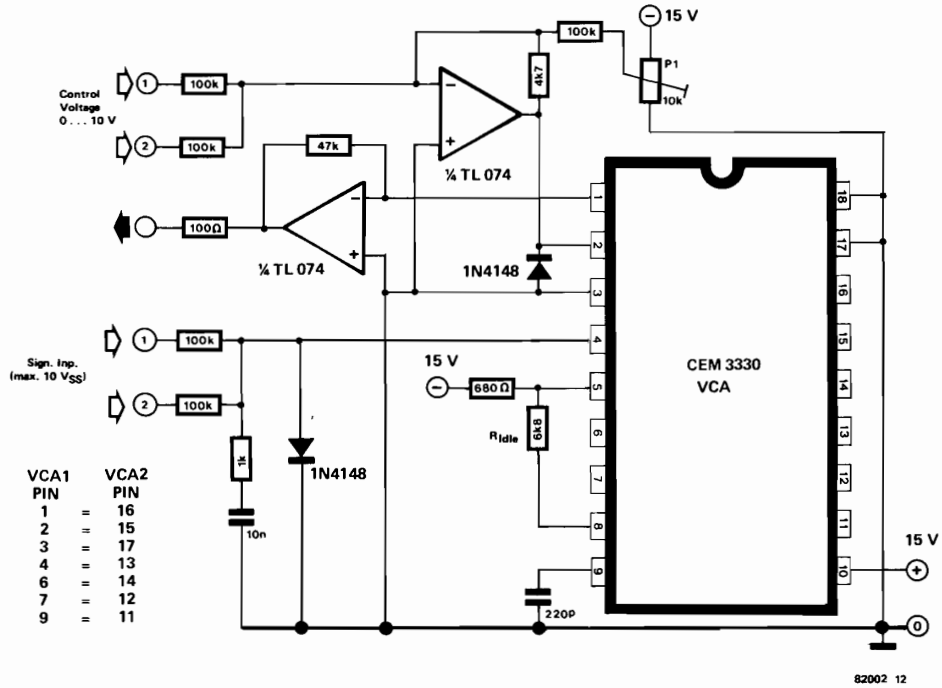

Figure 12. The complete circuit diagram of the CEM 3330 for linear control. The second VCA is identical to the first, except for the pin assignment.

quiescent conditions, to turn following VCAs hard 'off'.

A useful reference voltage appears at pin 3: the comparator threshold for the envelope's peak value. To prevent this level from being exceeded by the sustain voltage, the latter is 'clamped' to it by means of an additional opamp. At pin 4 there should be a gate voltage of 3 . . . 15 volts. It is a good idea to add an attenuator at this input, to protect the IC.

A 3n3 capacitor derives the trigger signal required for pin 5 from the positive gate edge. R_{EE} is the series resistor in the negative supply.

The potentiometers and voltage dividers provide the 0 . . . −240 mV control voltages. Several alternative arrangements are possible, and figure 10 gives a few examples. The circuit shown in figure 10a may be used to preset the sustain level using a potentiometer, instead of the voltage divider at pin 9. In figure 10b, an additional control reduces all the time values simultaneously. When P6 is turned fully clockwise, for instance, the slowest attack will only take 25% of the normal time. Since the total voltage across every potentiometer also drops by 25%, the potentiometers can be regulated with greater accuracy. Figure 10c shows the basic ranges for attack, decay and release.

The dual VCA: CEM 3330

Two identical VCAs are included in an 18-pin DIL package and operate according to the same principle as the CA 3080 OTAs. Each VCA has its own exponential converter so that they can all be controlled either linearly or logarithmically.

Resistor R_{IDLE} at pin 8 of the ICs sets the bias current – the smaller the value, the greater the current, and vice versa. A low value resistor (not less than 2 k) leads to less distortion, a high slew rate and band width, but also to more noise and less control voltage suppression. If a greater value (up to 200 k) is chosen for the resistor, the noise will be reduced, but at the same time the distortion will be increased and the band width and slew rate will be reduced. A good compromise between the two extremes is a value of about 6k8.

The VCA in practice

The circuit diagram as published in the Curtis data sheets required some modification. Instead of connecting the RC network 1 k/10 nF between pin 7 and ground, it should be between pin 4 and ground. The capacitor at pin 9 can then be reduced to about 220 pF. If the VCA is to be controlled by way of the EXP.CONTR.INP. pin, either pin 7 or pin 12 must be connected to 10 . . . 15 V by way of the resistor R_{CL} (100 k).

The amplifier gain is decreased by 6 dB for each 18 mV rise in control voltage. Since most envelope generators already produce logarithmic control voltages, the circuit in figure 12 only uses the linear control voltage input. The circuit for one VCA is shown; the second is identical except for the pin numbers (see figure 11). P1 is the only calibration point and must be adjusted for unity gain at the maximum control voltage level.

The circuit has an excellent linearity of 0.1 . . . 0.2%. At 18 kHz bandwidth, the signal-to-noise ratio was 90 dB. The crosstalk between the two VCAs is 60 . . . 70 dB.