Integration of the General Network Theorem in ADE and ADE XL

Toward a Deeper Insight Into Circuit Behavior

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Integration of the General Network Theorem in ADE and ADE XL

General Network Theorem

Integration in ADE (XL)

Application example

General Network Theorem

Decomposition of transfer function in simpler parts: lower-level transfer functions, *useful for design*

Using test signal injection and nulling techniques

$$H = H_\infty \frac{1 + \frac{1}{T_\mathrm{n}}}{1 + \frac{1}{T}} = H_\infty \frac{T}{1+T} + H_0 \frac{1}{1+T}$$

Using multiple injections T, Tn and H0 can be further factored

Ref: R. D. Middlebrook 2006, IEEE Microwave Magazine

General Network Theorem: N-EET and CT

Injection points determine decomposition and interpretation

GNT morphs into three interpretations

N-Extra Element Theorem (N-EET) — N injections

$$H = H_\infty \frac{1 + \frac{1}{T_n}}{1 + \frac{1}{T}}$$

Extra Elements absent

Effect of Extra Elements

Chain Theorem (CT) — single V or I injection

$$H = H_\infty \frac{1}{1 + \frac{1}{T}}$$

Buffered gain

Loading effect of second stage

General Network Theorem: GFT

Injection points determine decomposition and interpretation

GNT morphs into three interpretations

General Feedback Theorem (GFT) | **V and I injection**

$$H = H_\infty \frac{1 + \frac{1}{T_n}}{1 + \frac{1}{T}}$$

$$= H_\infty \frac{T}{1+T} + H_0 \frac{1}{1+T}$$

- ‘Ideal’ transfer function, infinite loop gain
- Loop gain
- Null loop gain
- Direct feedthrough, zero loop gain

Lower-level TF factorization example: loop gain T

$$T = \frac{T_{\text{fwd}}}{1 + T_{\text{rev}}}$$

$$T_{\text{fwd}} = T_{\text{v,fwd}} \,||\, T_{\text{i,fwd}}$$

$$T_{\text{rev}} = T_{\text{v,rev}} \,||\, T_{\text{i,rev}}$$

Compare to *stb* loop gain T_t

$$T_t = T_{\text{fwd}} + T_{\text{rev}}$$

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General Network Theorem

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Integration in ADE (XL): motivation

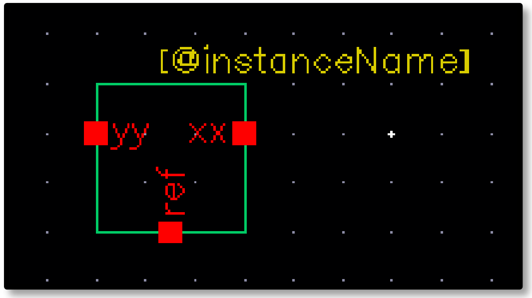
GNT advantages

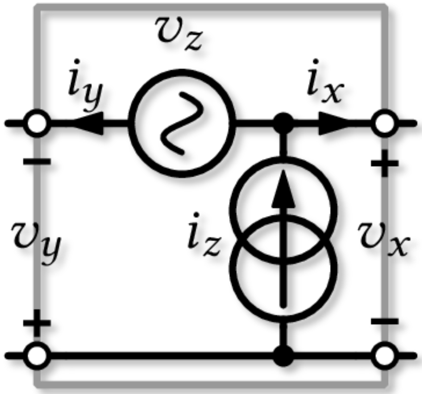
- General framework
  - Same techniques for different applications, hand calculations
  - Well-known results derive cleanly from GNT
- Results are useful for design
- Divide-and-conquer approach

Integration in Virtuoso

- Application of GNT to real-world designs
  - Deeper insight into complex circuit behavior
- Find out dominant lower-level TFs (a priori)
- Validate hand-analysis results (a posteriori)

Integration in ADE (XL): circuit setup





Insert GNT Probes in schematic at appropriate points

- Inject small-signal test signals: voltage and/or current

Uninvasive

- Does not interfere with other analyses
- Layout XL and Calibre LVS tools supported

Integration in ADE (XL): analysis setup

- New analysis 'gnt' in Choosing Analysis…
  - Same use model as stb, ac, …
- Familiar options
  - Sweep variable, sweep range, sweep type
- Source instance, output net or probe
  - Indicates the transfer function H to decompose
- (Nested) GNT analyses
  - GNT Probe instance(s)
  - Analysis type: GFT, N-EET, CT

Integration in ADE (XL): internals

Internally always flat N-EET calculated

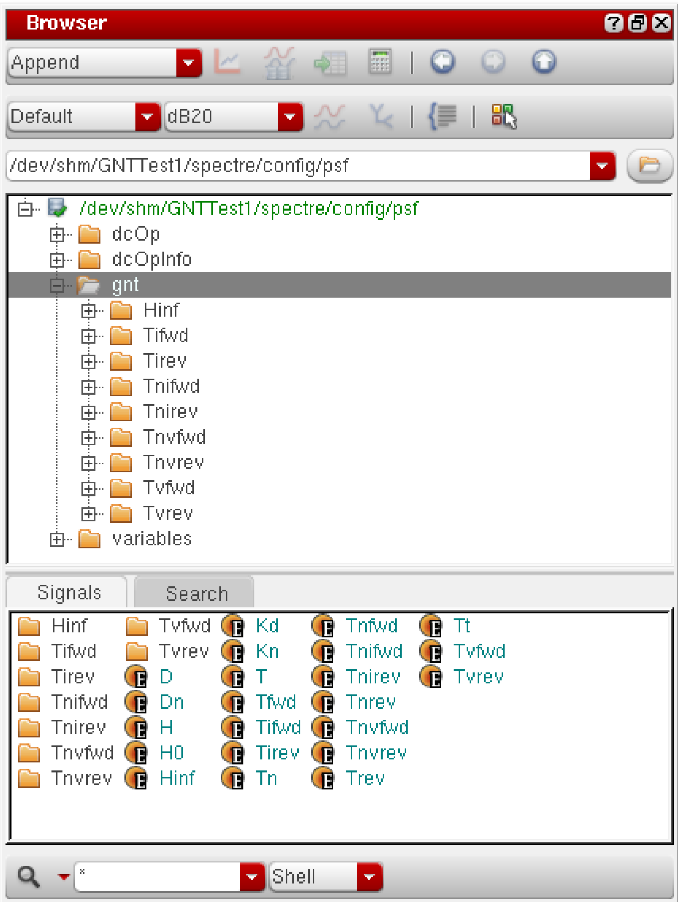
Using AC analysis per injection

- Data to be saved optionally

Flat N-EET results

Any possible permutations of nested analyses

Integration in ADE (XL): results



Results included in psf data

Nested results as folders

Accessible in the usual ways

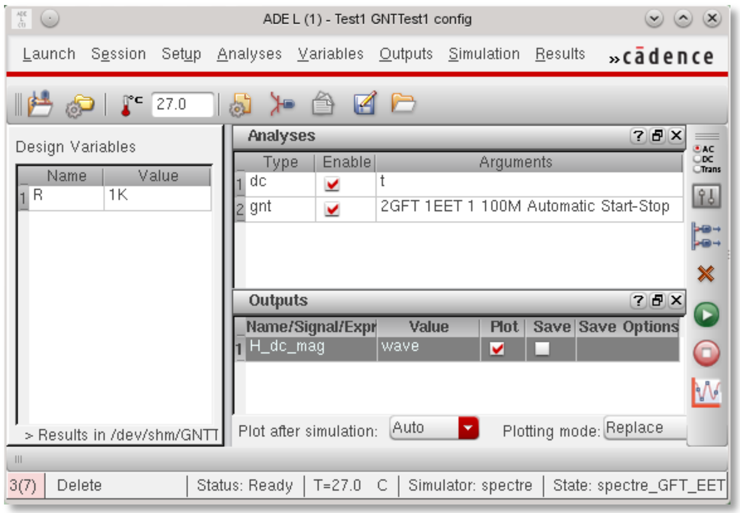
ViVa’s Results Browser

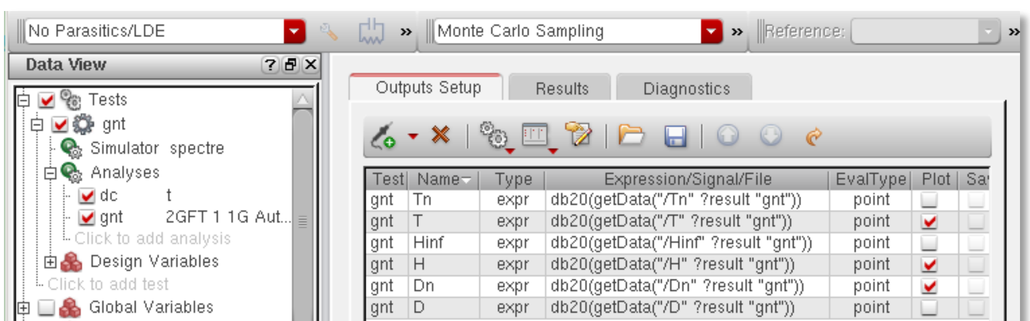
getData() SKILL API

GFT Tt identical to *stb* loop gain

Given identical reference nodes

Integration in ADE (XL): ADE support





ADE L

- Incl. parametric sweep

ADE (G)XL

- Corners
- Parameters
- Monte Carlo sampling
- Sensitivity analysis
- Optimization
- Worst-case corners
- …

Tested in IC 6.1.5 and IC 6.1.6

Integration of the General Network Theorem in ADE and ADE XL

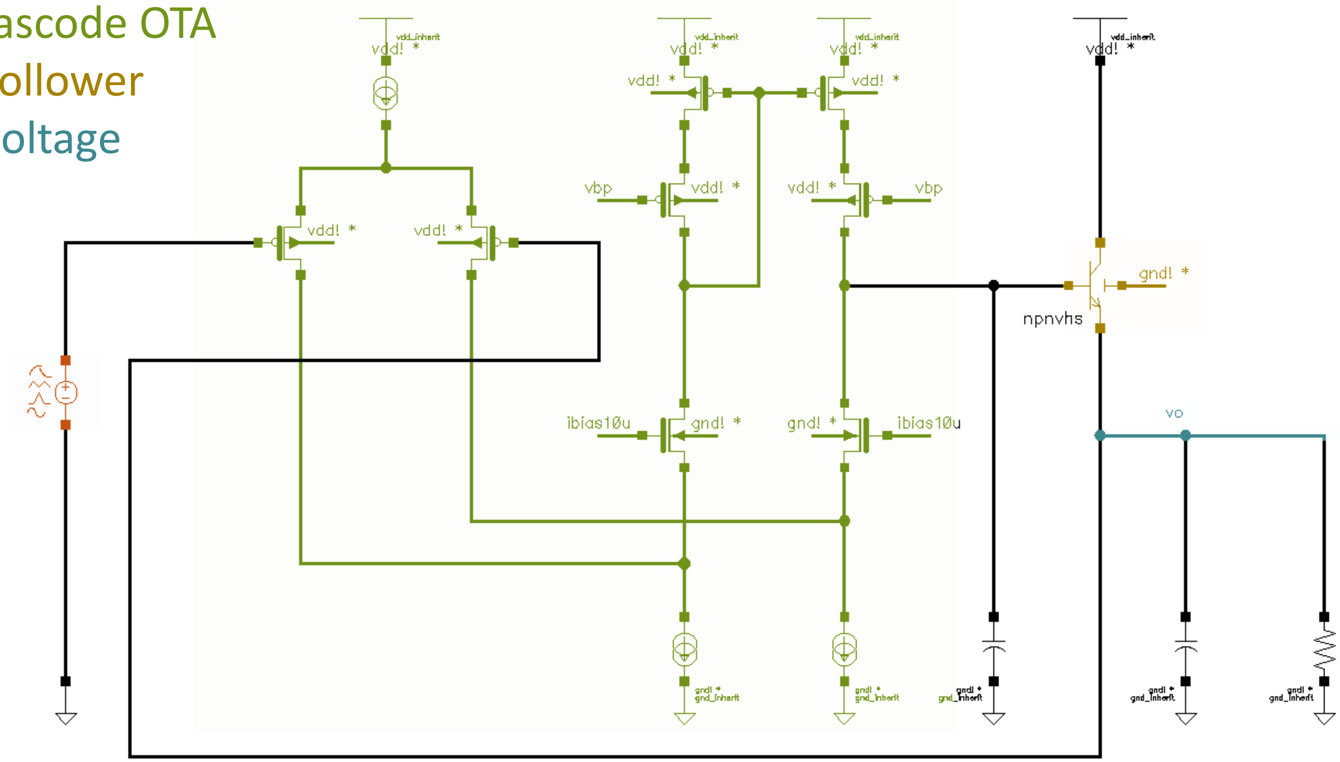
General Network Theorem

Integration in ADE (XL)

Application example

Application example: voltage regulator

- Input voltage source
- Folded cascode OTA
- Emitter follower
- Output voltage

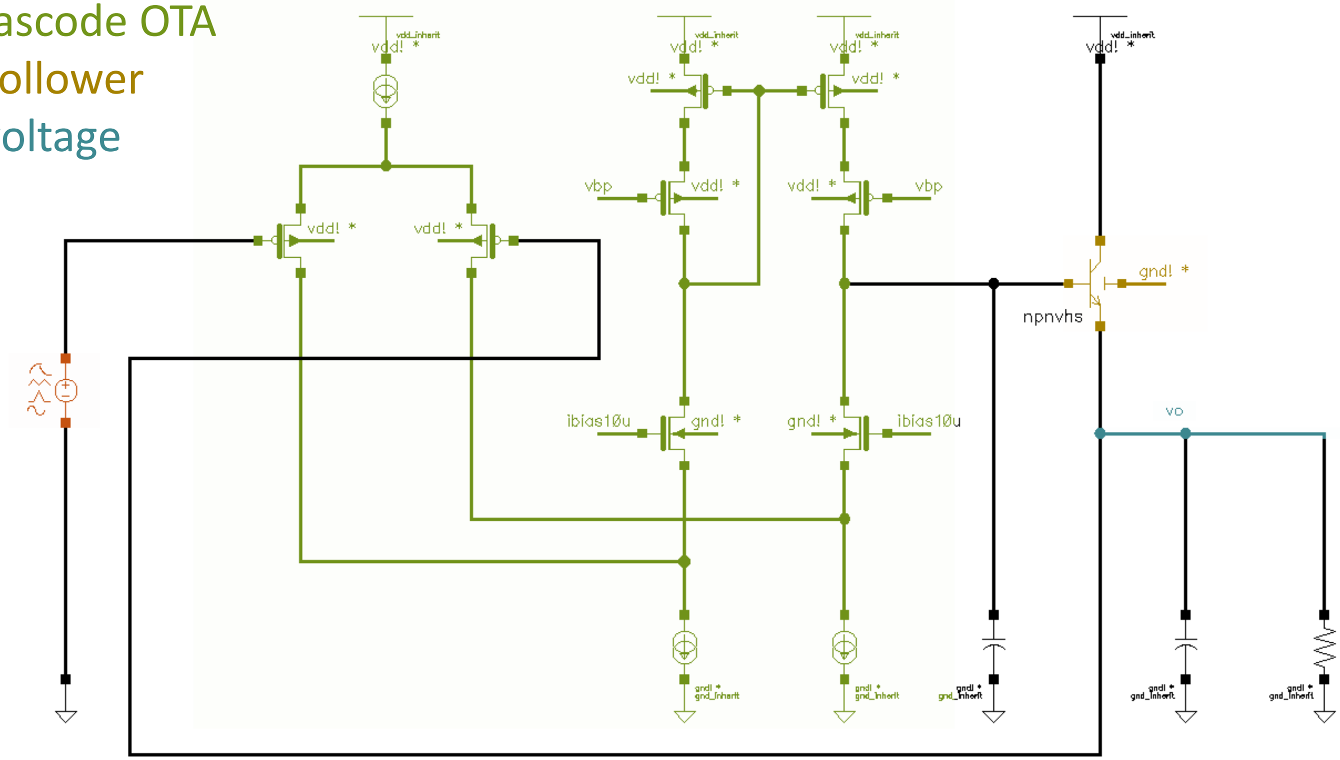


Application example: voltage regulator

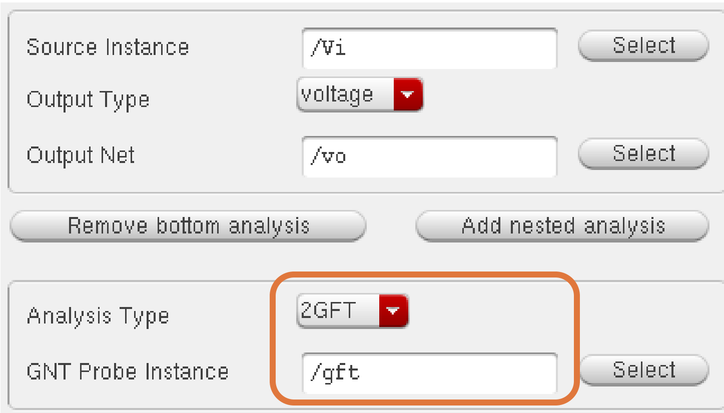
Problem

Output voltage inaccurate

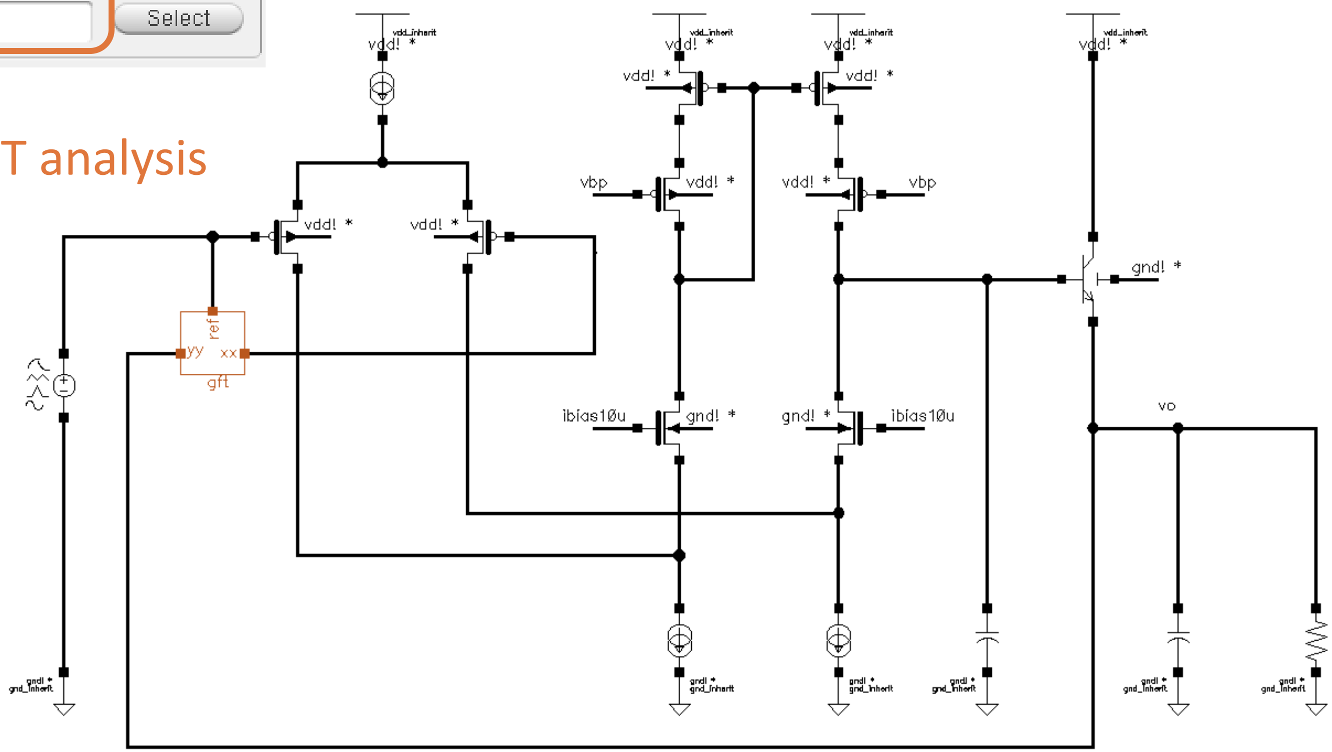
- Input voltage source
- Folded cascode OTA
- Emitter follower
- Output voltage



Application example: GFT analysis - setup



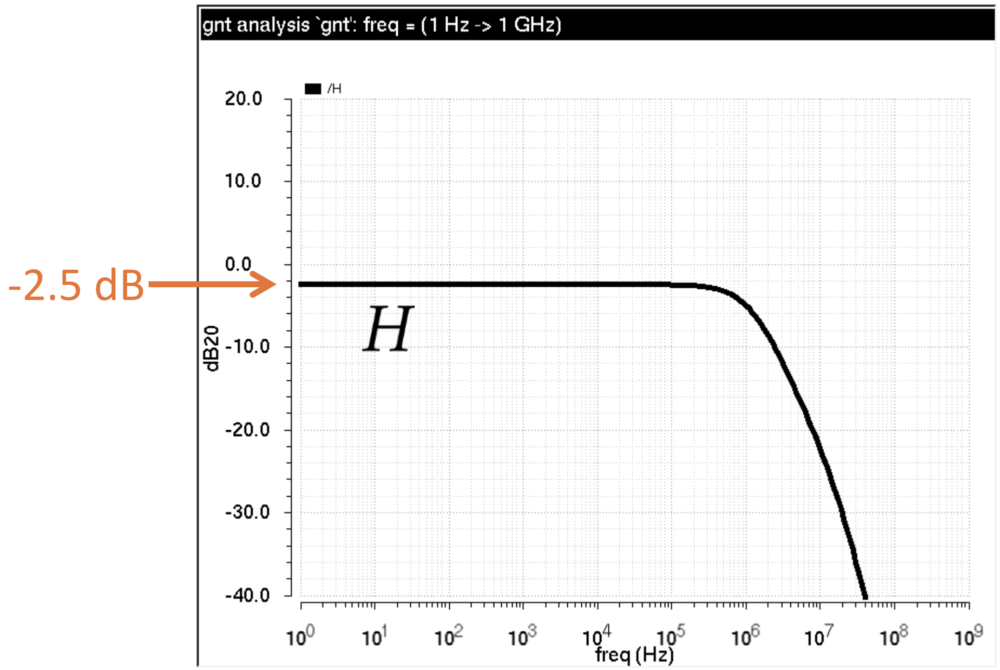
GFT analysis



Application example: GFT analysis - results

Problem

Output voltage inaccurate

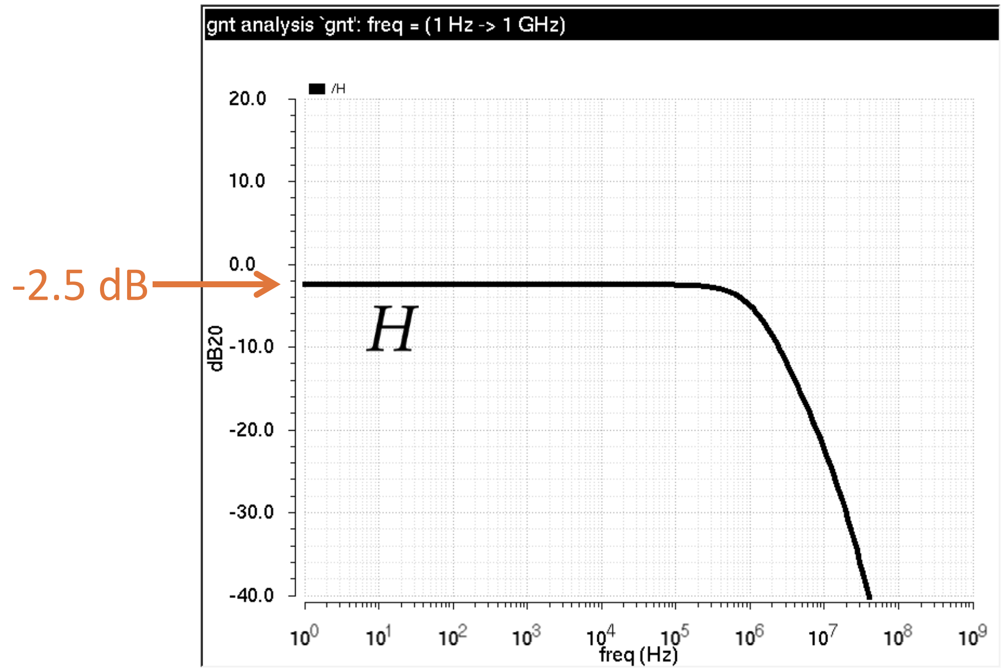


$$H = H_\infty \frac{T}{1+T} + H_0 \frac{1}{1+T}$$

Application example: GFT analysis - results

Problem

H too low
↳ Output voltage inaccurate



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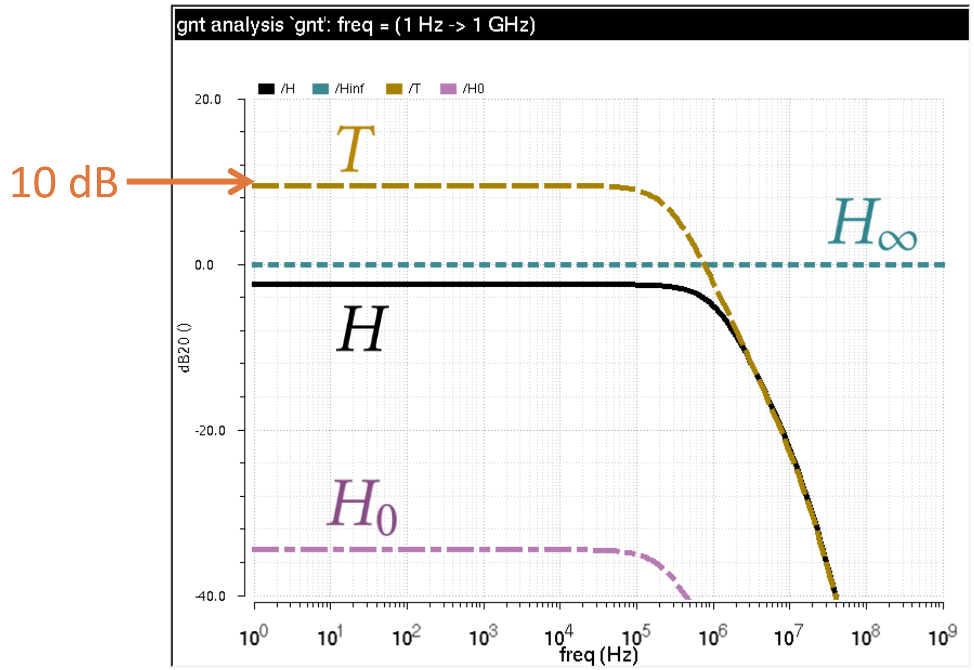
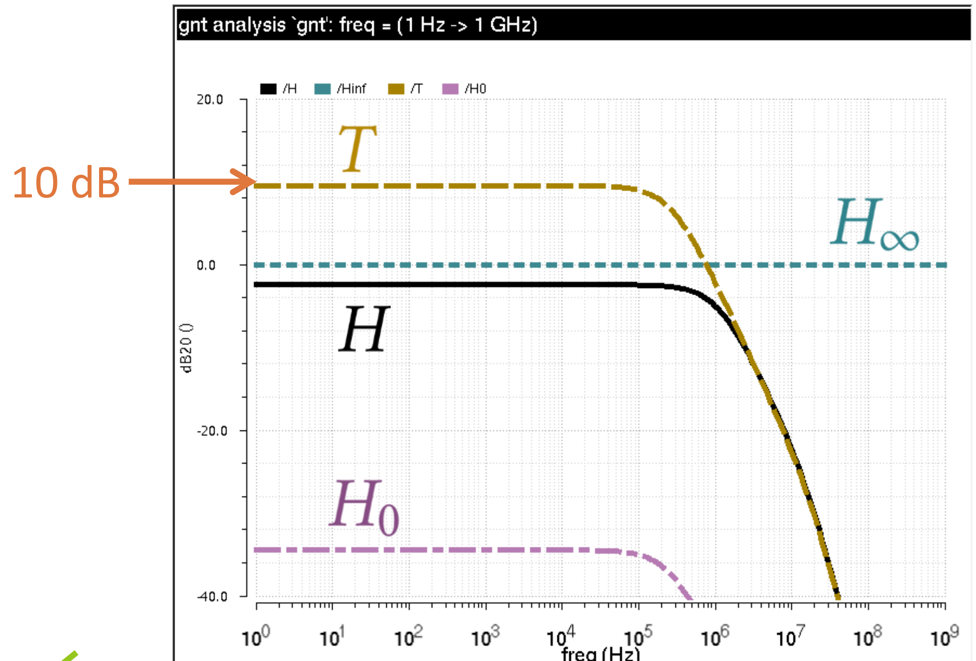


$$H = H_\infty \frac{T}{1+T} + H_0 \frac{1}{1+T}$$

Application example: GFT analysis - results

Problem

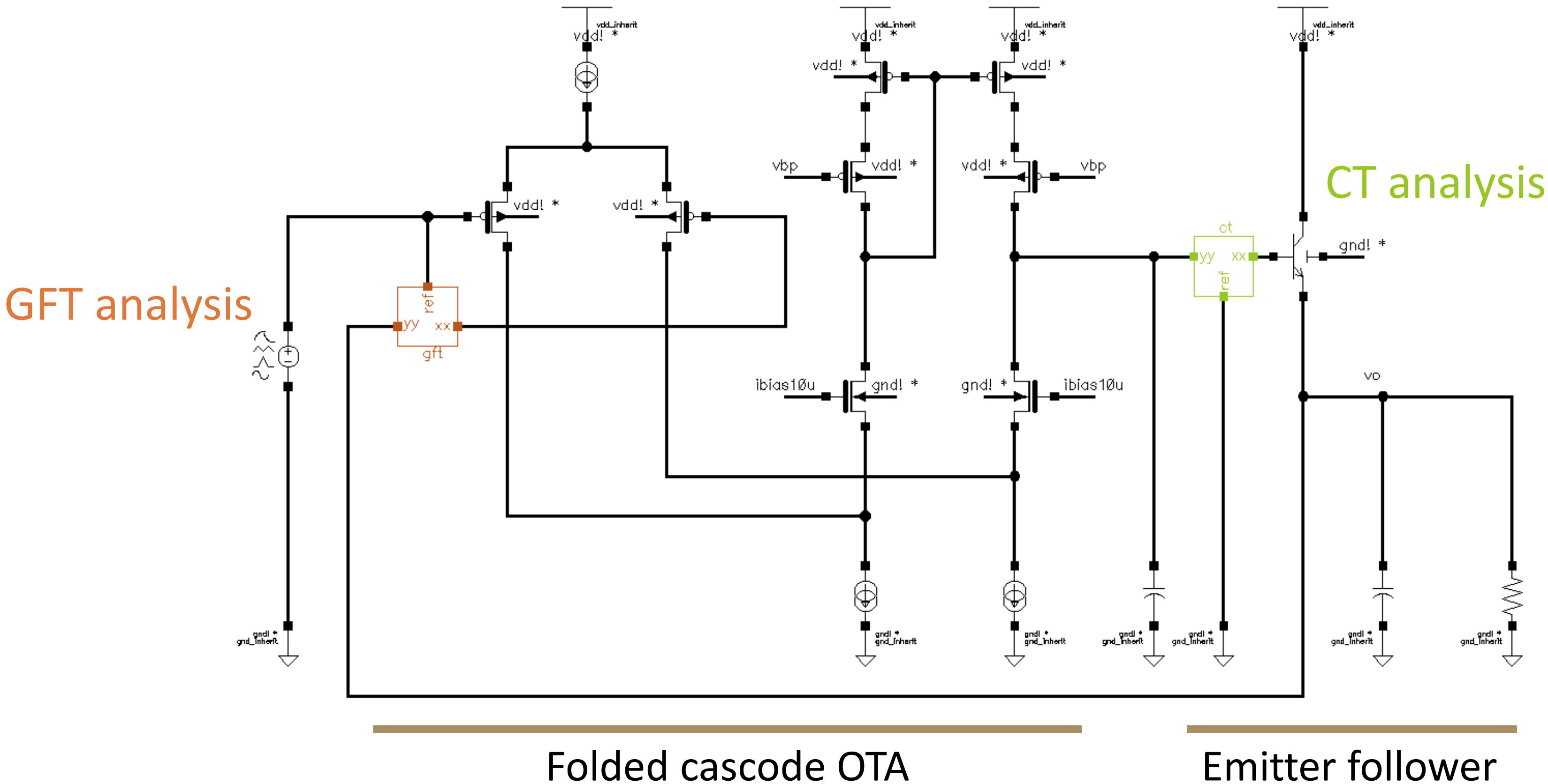
Forward voltage loop gain insufficient
↳ H too low
↳ Output voltage inaccurate



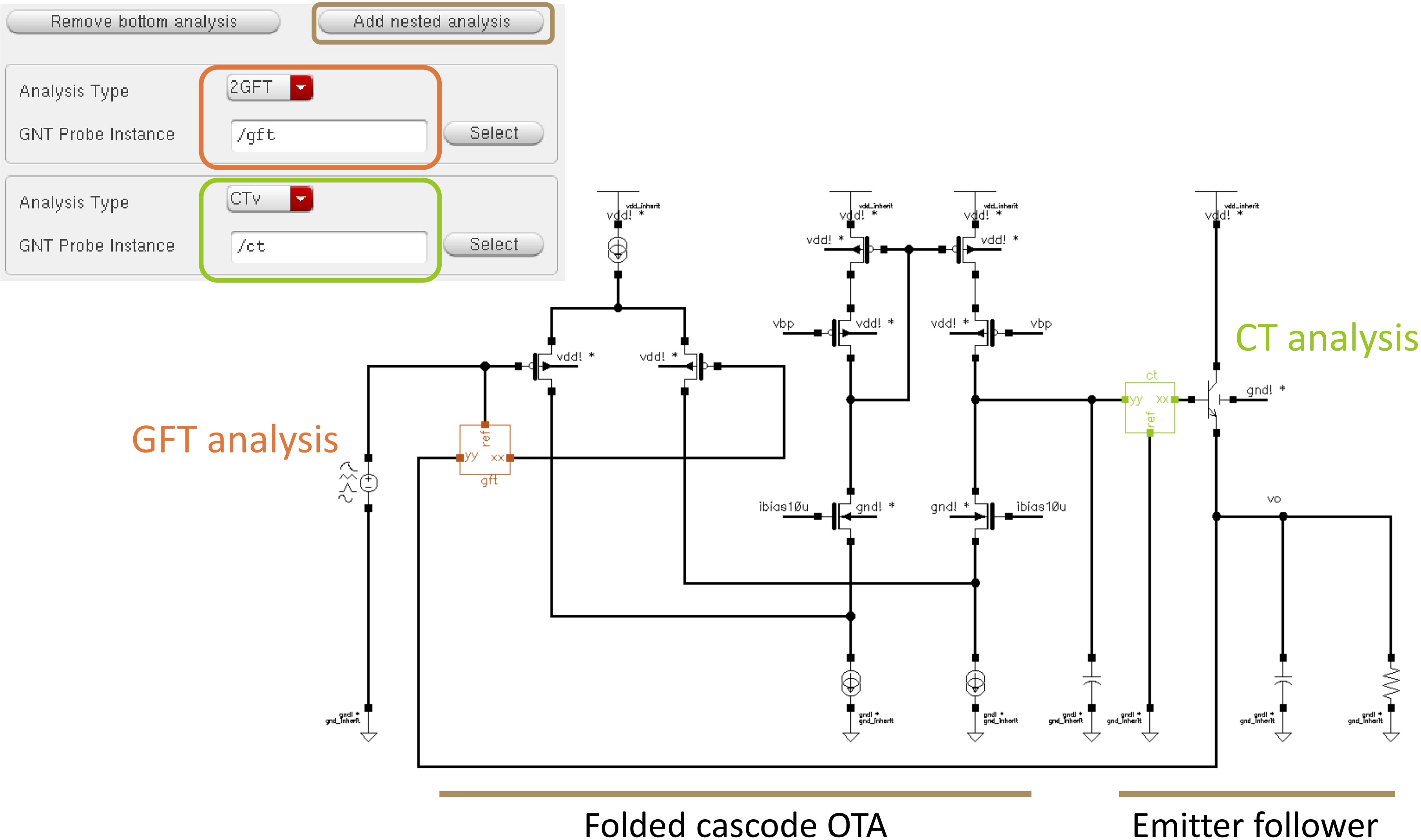
$$H = H_\infty \frac{T}{1+T} + H_0 \frac{1}{1+T}$$

$$T \approx T_{\mathrm{v,fwd}}$$

Application example: CT analysis nested in GFT analysis - setup



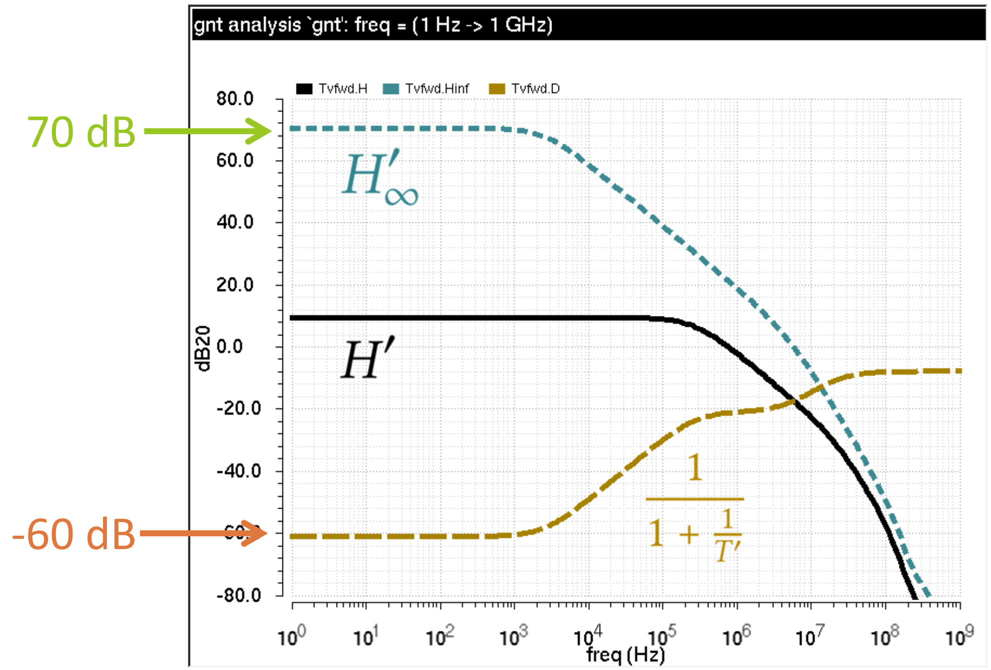
Application example: CT analysis nested in GFT analysis - setup



Application example: CT analysis nested in GFT analysis - results

Problem

Forward voltage loop gain insufficient
↳ H too low
  ↳ Output voltage inaccurate



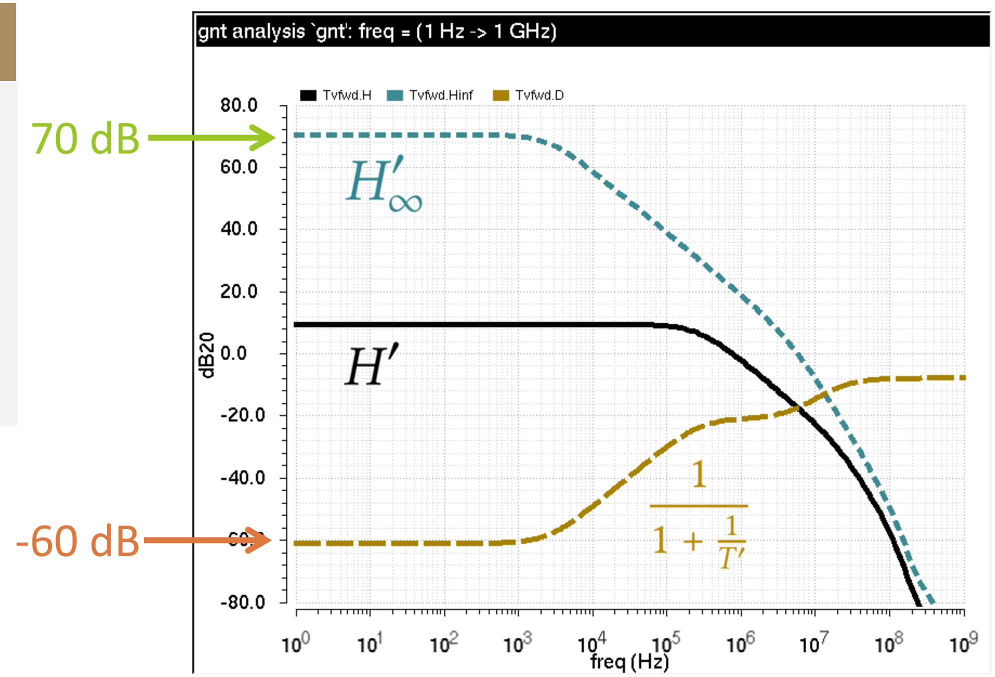
$$T_{\mathrm{v,fwd}} = H'$$

$$H' = H'_\infty \frac{1}{1 + \frac{1}{T'}}$$

Application example: CT analysis nested in GFT analysis - results

Problem

Excessive interaction between stages
↳ Forward voltage loop gain insufficient
↳ H too low
↳ Output voltage inaccurate

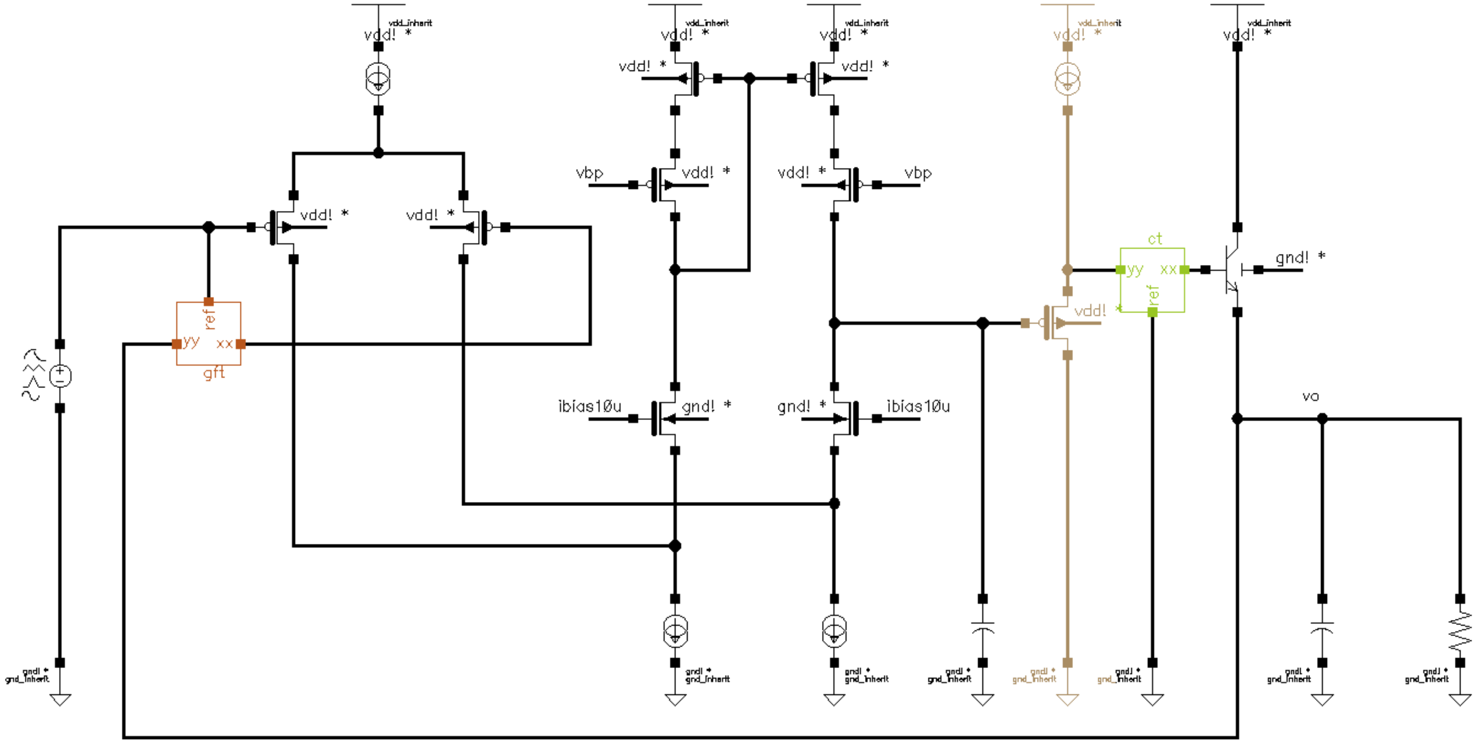


$$T_{\text{v,fwd}} = H'$$

$$H' = H'_\infty \frac{1}{1 + \frac{1}{T'}}$$

Application example: reducing the interaction between stages

Insert a PMOS source follower



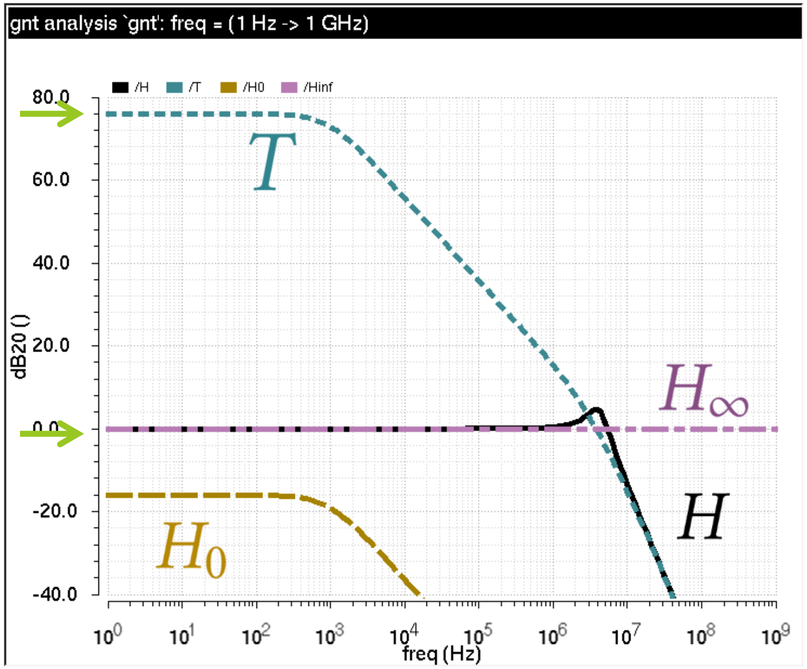
Application example: reducing the interaction between stages - results

Problem

Excessive interaction between stages
↳ Forward voltage loop gain insufficient
  ↳ H too low
    ↳ Output voltage inaccurate

70 dB

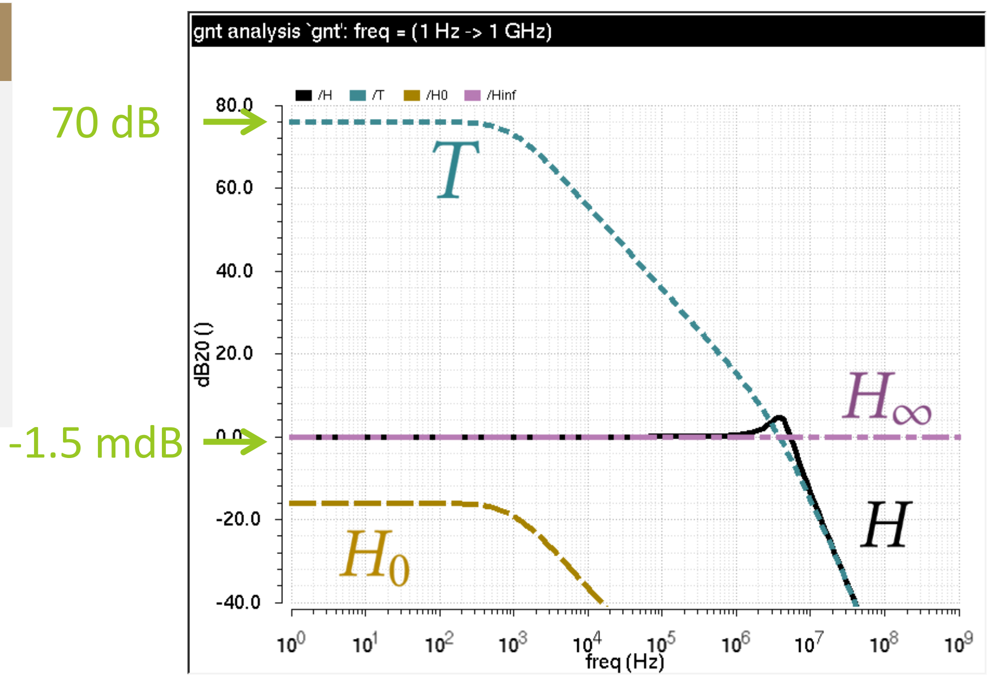
-1.5 mdB



Application example: reducing the interaction between stages - results

Problem

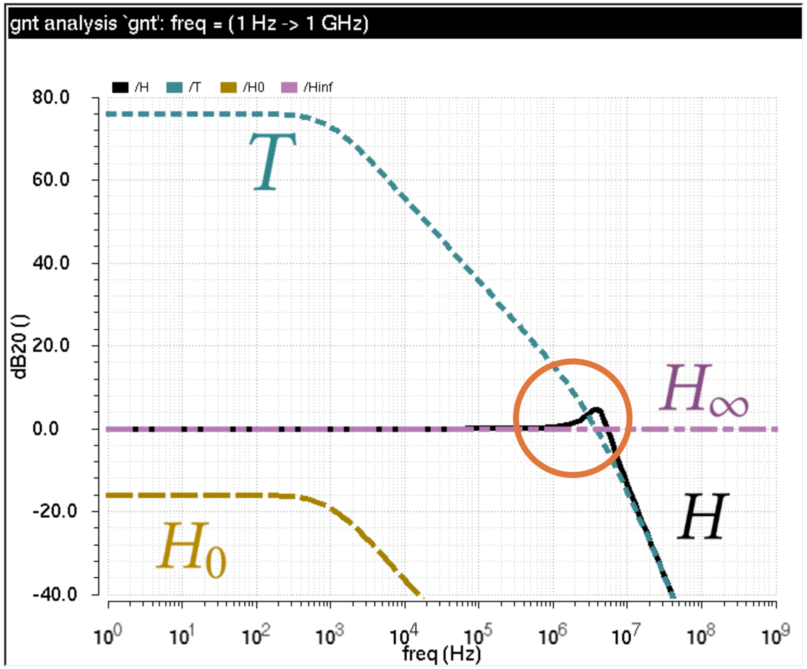
Excessive interaction between stages
↳ Forward voltage loop gain insufficient
↳ H too low
↳ Output voltage inaccurate



Application example: reducing the interaction between stages - results

Problem

H shows peaking

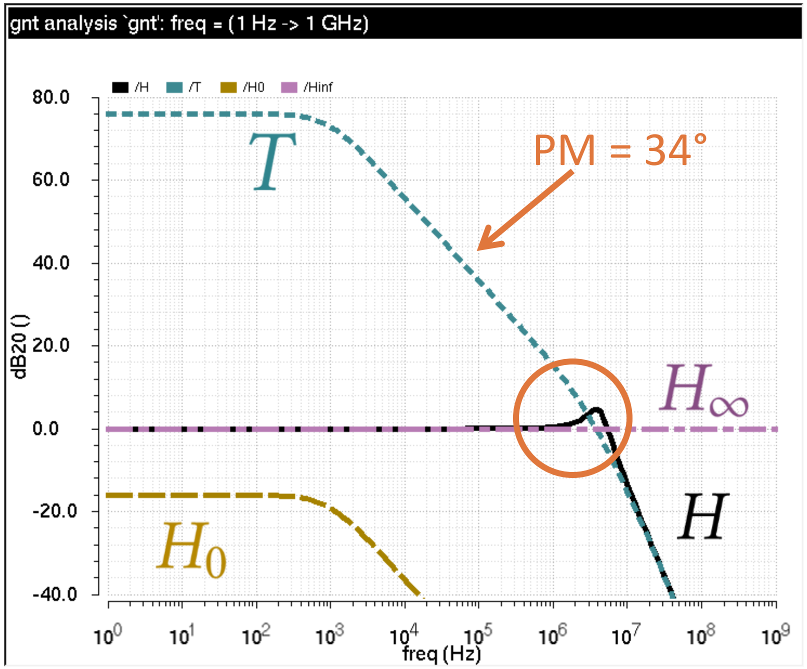


$$H = H_\infty \frac{T}{1+T} + H_0 \frac{1}{1+T}$$

Application example: reducing the interaction between stages - results

Problem

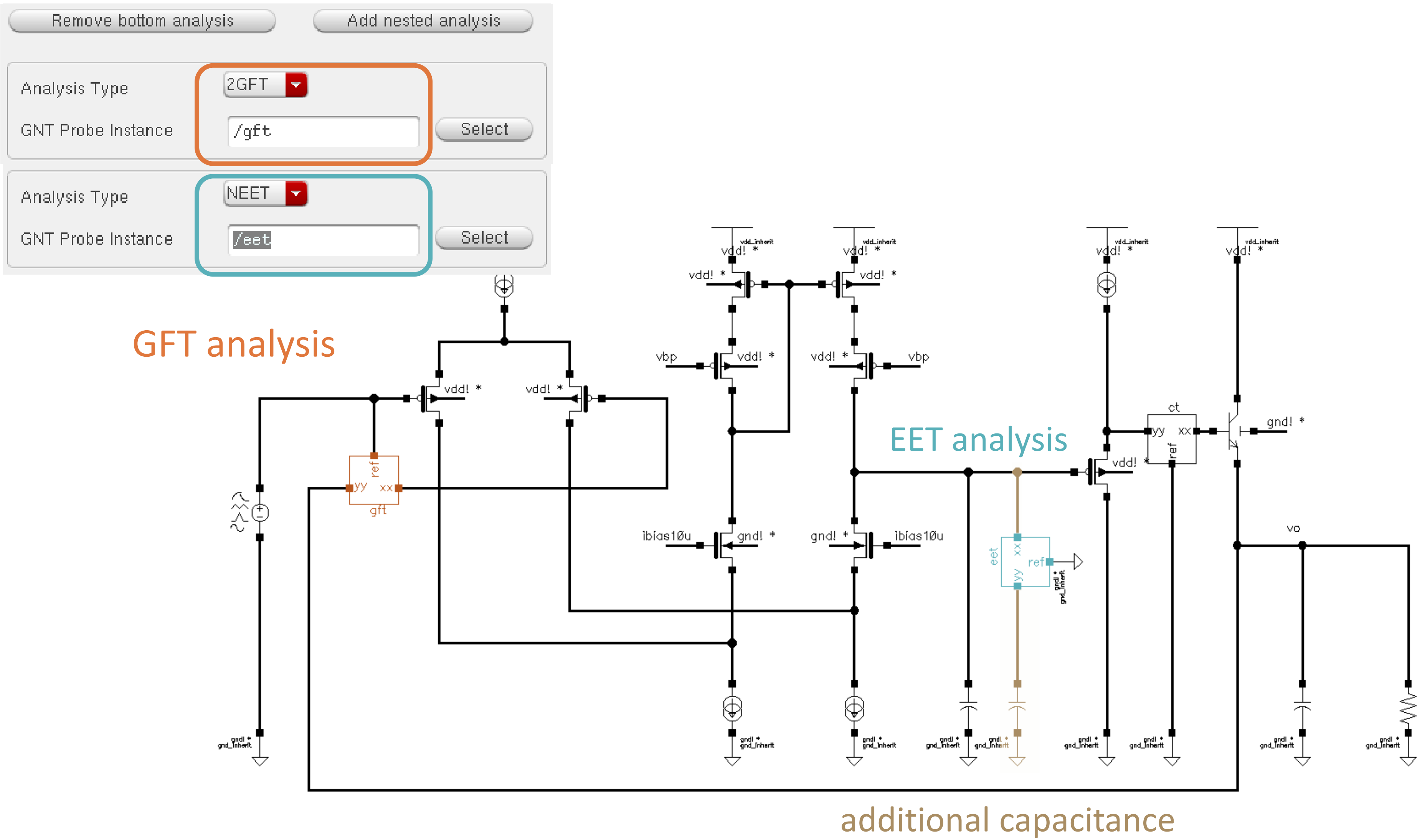
Forward voltage loop gain insufficient phase margin
↳ H shows peaking



$$H = H_\infty \frac{T}{1+T} + H_0 \frac{1}{1+T}$$

$$T \approx T_{\mathrm{v,fwd}}$$

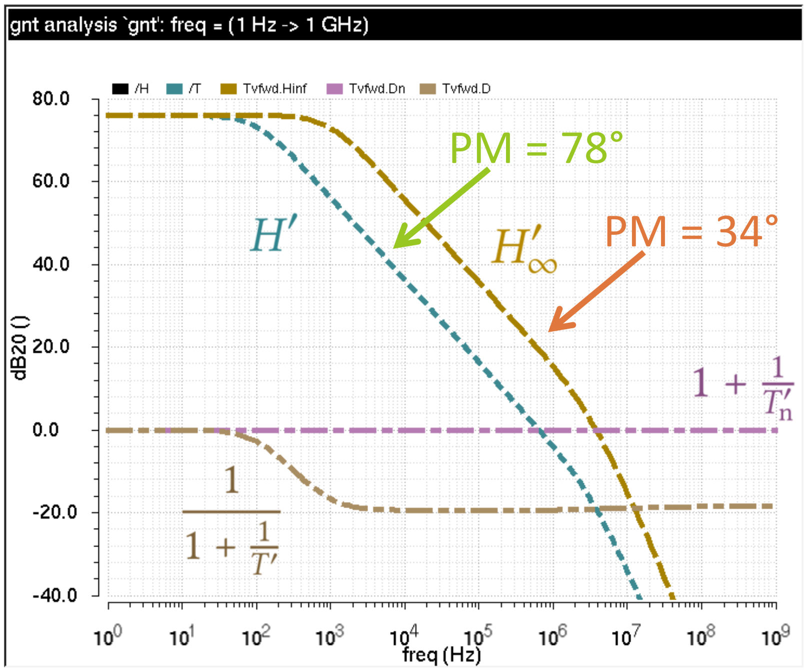
Application example: reducing peaking, EET analysis nested in GFT analysis - setup



Application example: reducing peaking, EET analysis nested in GFT analysis - results

Problem

Forward voltage loop gain insufficient PM
↳ H shows peaking



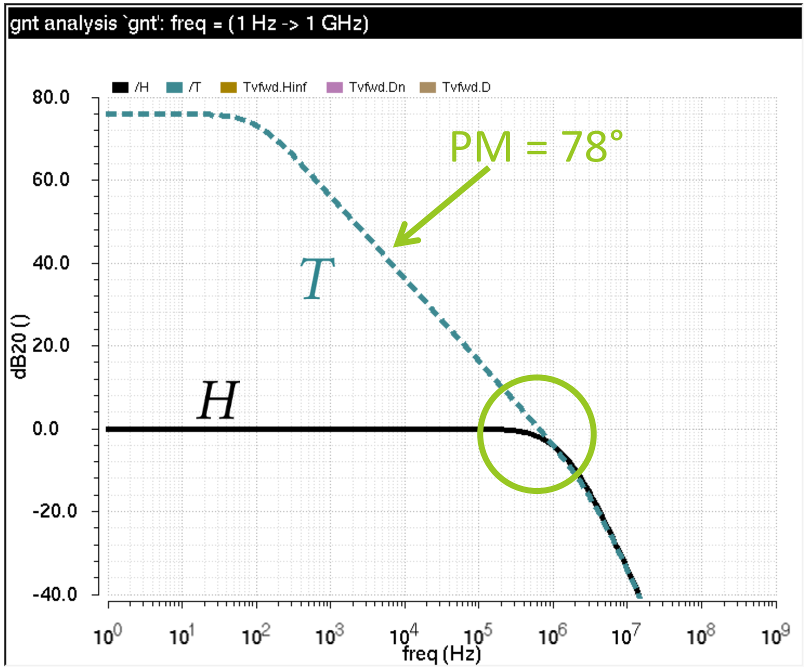
$$T_{\mathrm{v,fwd}} = H'$$

$$H' = H'_{\infty} \frac{1 + \frac{1}{T'_{\mathrm{n}}}}{1 + \frac{1}{T'}}$$

Application example: reducing peaking, EET analysis nested in GFT analysis - results

Problem

Forward voltage loop gain insufficient PM
↳ H shows peaking



$$T_{\mathrm{v,fwd}} = H'$$

$$H' = H'_\infty \frac{1 + \frac{1}{T'_\mathrm{n}}}{1 + \frac{1}{T'}}$$

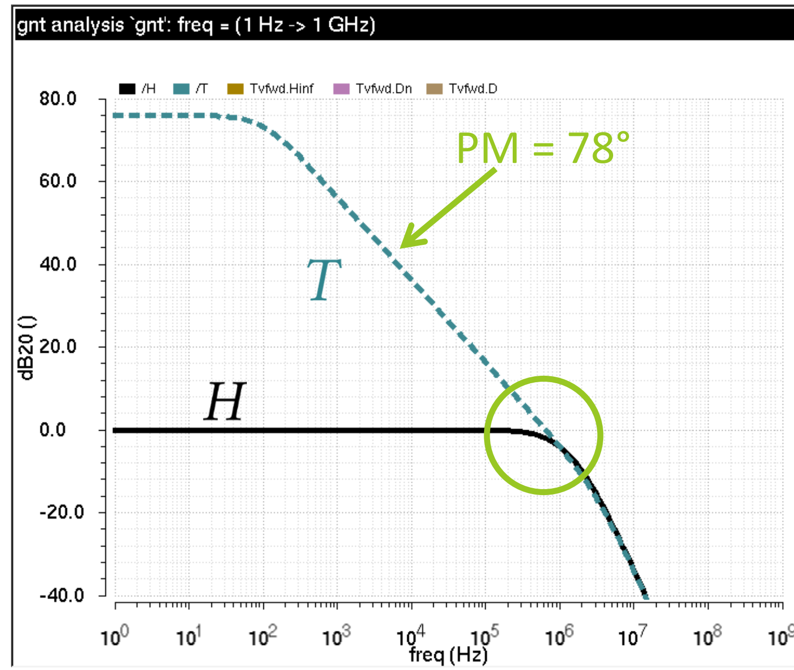
Application example: reducing peaking, EET analysis nested in GFT analysis - results

Problem

Forward voltage loop gain
insufficient PM
↳ H shows peaking

$$T_{\mathrm{v,fwd}} = H'$$

$$H' = H'_{\infty} \frac{1 + \frac{1}{T'_{\mathrm{n}}}}{1 + \frac{1}{T'}}$$



Conclusion

GNT analysis integrated in ADE and ADE XL

Allows direct application of theorem

Valuable to increase insight, provides design guidance

Helpful instrument for design and analysis of electronic circuits and education of future designers

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References and acknowledgement

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