INVITED PAPER

Circuit Design Advances for Wireless Sensing Applications

Many recent designs for miniature, millimeter-scale, long-lifetime, ultralow-power wireless sensors are described with applications in areas such as medical diagnosis, infrastructure monitoring, and environmental sensing.

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ABSTRACT | Miniature wireless sensors with long lifetimes enable new applications for medical diagnosis, infrastructure monitoring, military surveillance, and environmental sensing among many other applications in a growing field. Sensor miniaturization leads to decreased on-sensor energy capacity, and lifetime requirements further constrain the sensor's power budget. To enable millimeter-scale wireless sensors with lifetimes of months to years, a new class of low-power circuit techniques is required. Wireless sensors collect and digitize environmental data before processing and transmitting the data wirelessly to base stations or other sensor nodes. Recent low-power advances for each of these functions shed light on how ubiquitous sensing can become a reality.

KEYWORDS | Energy harvesting; low power; power management; sensors; standby mode; wireless

I. INTRODUCTION

Wireless sensors vary greatly in application and distribution but universally benefit from longer device lifetimes, smaller size, and reduced cost. Low-power operation and energy harvesting from the environment increase the time before energy stored on-sensor is depleted, extending lifetimes. Low-power operation is vital for sensors used to monitor flow rates in oil pipelines [1] or in heating, ventilation, and air conditioning (HVAC) systems [2] since the sensors are inaccessible and battery replacement often requires disassembling the infrastructure. It is equally important for implanted medical sensors, where battery replacement requires costly, invasive surgery and high-power densities can cause tissue heating and damage [3]. Tiny sensor nodes are needed for many applications to collect and communicate environmental data without interfering with the subject under study. For example, a pebble-sized sensor can be attached to a bumblebee to track a colony's territory without impeding the insect's movement [4]. Similarly, tiny sensors can be mixed into concrete to measure a building's structural integrity during an earthquake without compromising the concrete's strength [5]. Lower sensor cost is vital for the mass deployment of ubiquitous sensors and for creating large wireless sensor networks. Cheaper sensors make it more economical to monitor conditions as individual items are transported through a supply chain or to use wireless sensors to track inventory in a store.

Today's wireless sensors are composed of multiple components on a printed circuit board (PCB). Bulky batteries are included in the system to power the circuit components with adequate lifetimes. Many modern wireless transmission protocols also require centimeter-scale antennas or larger. The result is a milliwatt-powered system that is centimeters or tens of centimeters in at least one dimension. New circuit design advances are creating exciting opportunities to dramatically reduce the size and cost of future wireless sensors without affecting device lifetime. Continued scaling of transistor, sensor, and packaging technologies will enable unprecedented integration, and decrease size, power, and cost. Robust low-power circuit design will enable the use of smaller, less expensive power sources while still increasing device lifetime to reduce maintenance costs for battery replacement or recharging. New wireless transmission methods will require less power and smaller antennas. The result will be a millimeter-scale wireless sensor suitable for a multitude of applications not feasible today.

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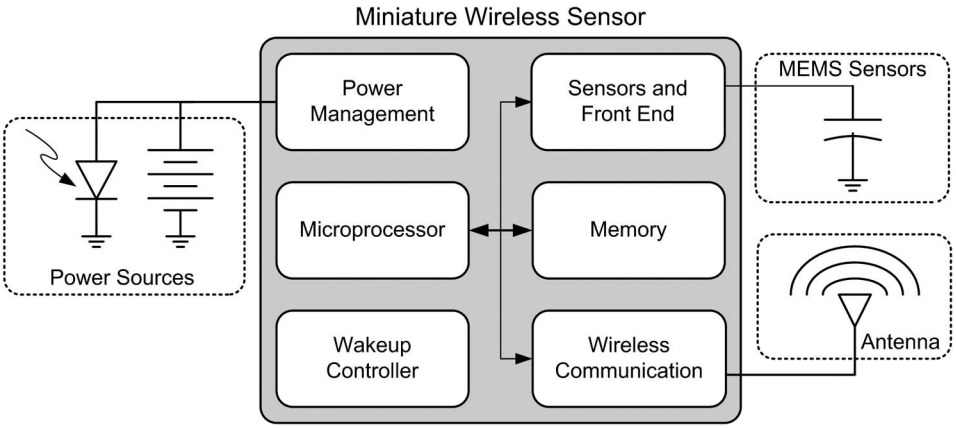

Fig. 1. ***The sensor collects, processes, and transmits environmental data.***

Consider a hypothetical intraocular pressure (IOP) monitor as an example to better understand the possibilities created by, and constraints placed on, future millimeter-scale wireless sensor systems. Intraocular sensors provide the opportunity for continuous pressure monitoring to detect and track the progression of glaucoma and also study the underlying mechanisms of the disease [6], [7]. Current eye pressure measurement techniques are invasive and must be performed at a doctor's office, so they are performed infrequently. With an implanted sensor, IOP can be recorded nearly continuously (i.e., every few minutes) using a capacitive microelectromechanical system (MEMS) sensor (Fig. 1). This provides doctors with a much more accurate picture of the eye pressure during normal daily activities. It also allows them to customize medication levels throughout the day to adjust to the circadian rhythms in the patient's eye pressure and to determine patient compliance with the prescribed medication regime.

The data logged by the sensor are stored into memory by an on-sensor microprocessor and are periodically wirelessly transmitted to the doctor's or patient's personal computer. Additionally, the microprocessor can perform signal processing on the pressure data to check for abnormally high or low pressures, as well as sharp changes in pressure. In case an abnormally high ocular pressure is detected, the sensor transmits a warning signal to the personal computer, which relays the message to the patient and physician so that the proper medical actions are taken with faster response time. The intraocular sensor is powered by a thin-film battery that is recharged through radio-frequency (RF) power transmitted from a wand that is periodically held to the eye for a short period of time. The battery is assembled with the integrated circuits (ICs) as well as energy harvesting elements or antenna, as recently demonstrated and shown in Fig. 2 [8].

Since the sensor is implanted in the eye, its volume is heavily constrained and a cubic-millimeter sensor node is required. This limits the area of its thin-film battery to 1 mm^2. Even if the patient fully recharges this battery daily and the battery has an energy density of 1.5 $\mu Ah/mm^2$, the power budget of the sensor is 240 nW. This translates to the power of roughly 5000 minimum sized complementary metal–oxide–semiconductor (CMOS) inverters doing nothing and only ten of the same inverters when switching in a 1.8-V, 0.18-μm CMOS process. Moreover, the sensor must perform a multitude of functions, including collecting, processing, storing, and transmitting IOP data, all using its limited power supply. Fig. 3 shows the maximum power budget of such sensors as a function of the desired system lifetime, assuming a nonrechargeable system with commercial batteries, along with an academic fuel cell and commercial thin-film battery scaled down to millimeter-scale dimensions [9]–[12]. To meet the stringent power requirements of miniature wireless sensors, significant strides have been made in each wireless sensor component to achieve robust ultralow-power operation. In this paper, we present recent research findings of a new class of

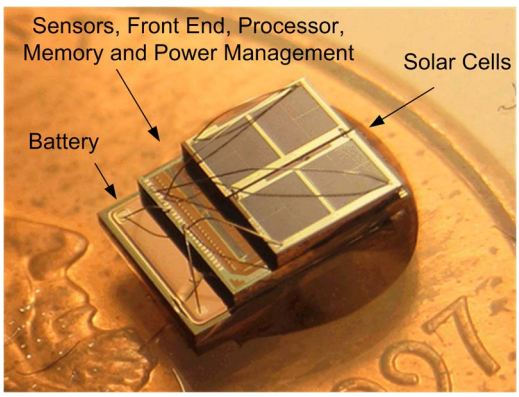

Fig. 2. ***A highly integrated millimeter-scale low-power sensor [8].***

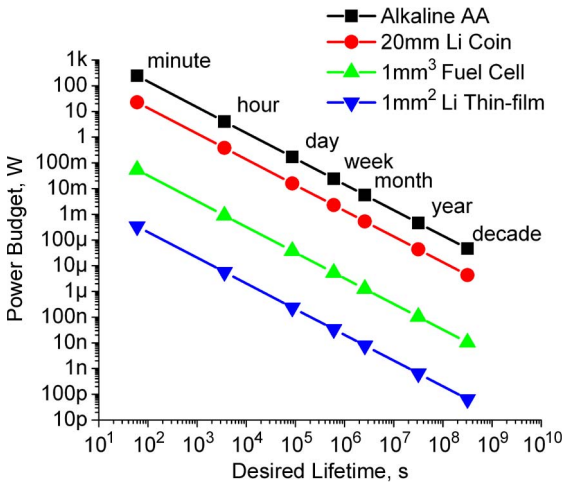

Fig. 3. *Sensor power budgets with common power sources.*

ultralow-power circuits and techniques aimed at providing these unprecedented low-power levels. Using these techniques, an IOP sensor with a 1-mm^3 volume and lifetimes of months to years is possible.

In Section II, we will take a closer look at sensors and front end design for sensor nodes. Section III examines microprocessors that log, analyze, and compress sensor data. Section IV discusses low-power memory to store data on-sensor and Section V reviews wireless communication to move data off of the sensor node. Section VI describes the power electronics needed to supply low-power sensor nodes and Section VII details standby mode operation. We then examine open challenges in Section VIII and conclude in Section IX.

II. SENSORS AND FRONT END

Wireless sensors monitor environmental conditions, such as light, temperature, pressure, vibration, or electricity. Many common sensors output a voltage or a current. For example, photodiodes generate a voltage and current, which are related to light intensity. Capacitive or piezoresistive pressure sensors can output a voltage based on the pressure-induced deflection of a MEMS diaphragm [13]. In a typical sensor front end shown in Fig. 4, the raw sensor output is amplified to magnify alternating current (ac) components and supply adequate drive strength for subsequent circuits. The data are then digitized with an analog-to-digital converter (ADC) before it is digitally processed, stored, and transmitted. It is vital that the low-noise amplifier (LNA) and ADC introduce minimal noise while operating on a tight power budget. In this section, we discuss light and temperature sensors since they are easily implemented in CMOS processes. In addition, we examine LNA and ADC circuits that receive inputs from CMOS, MEMS, and other sensors.

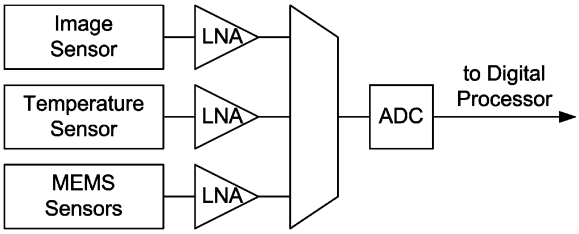

Fig. 4. *Signals from sensors are amplified and converted to a digital value.*

A. Temperature Sensors

Temperature sensors commonly digitize a voltage based on the temperature-sensitive nature of parasitic p-type n-type p-type (PNP) bipolar devices in CMOS processes. The base-to-emitter voltage (VBE) of a PNP device with fixed current is complementary to absolute temperature (CTAT). Also, the difference in VBE between two PNP devices with different sizes or currents is proportional to absolute temperature (PTAT) [14]. Either of these voltages or some combination of the two can be fed into an ADC to produce a digital representation of the temperature. The PNP bias is typically greater than 250 nA to ensure accurate current ratios between devices, and ADCs commonly require microwatts of power for sampling frequencies in the kilohertz range [15]. Alternatively, a 1-nW temperature sensor can be realized by leveraging the temperature-sensitive nature of subthreshold leakage, as shown in (1) [16]. A capacitor is precharged to a set value and then discharged with a subthreshold biased metal–oxide–semiconductor field-effect transistor (MOSFET). A CMOS inverter or Schmitt trigger buffers the capacitor's voltage and generates a pulse when the capacitor crosses the buffer switching threshold. The duration of the pulse is temperature dependent and can be digitized with a time-to-digital converter (TDC), discussed in Section II-D. A temperature sensor must either heavily duty cycle a PNP device or use a low-power circuit such as the discussed subthreshold device to fit within the power budget of a nanowatt system

$$I_{\mathrm{SUB}} = \mu_o C_{\mathrm{OX}} \frac{W}{L} v_T^2 e^{((V_{\mathrm{GS}}-V_{\mathrm{TH}})/nv_T)} \left(1 - e^{(-V_{\mathrm{DS}}/v_T)}\right). \quad (1)$$

B. Image Sensors

Image sensors on sensor nodes can be used for military surveillance, gastrointestinal scans, and automobile traffic monitoring. CMOS image sensors are easily integrated with digital circuits to allow for a small form factor. A traditional CMOS image sensor consists of an array of photovoltaic diodes. Upon exposure to light, electron–hole pairs are generated in the diode's depletion region. These

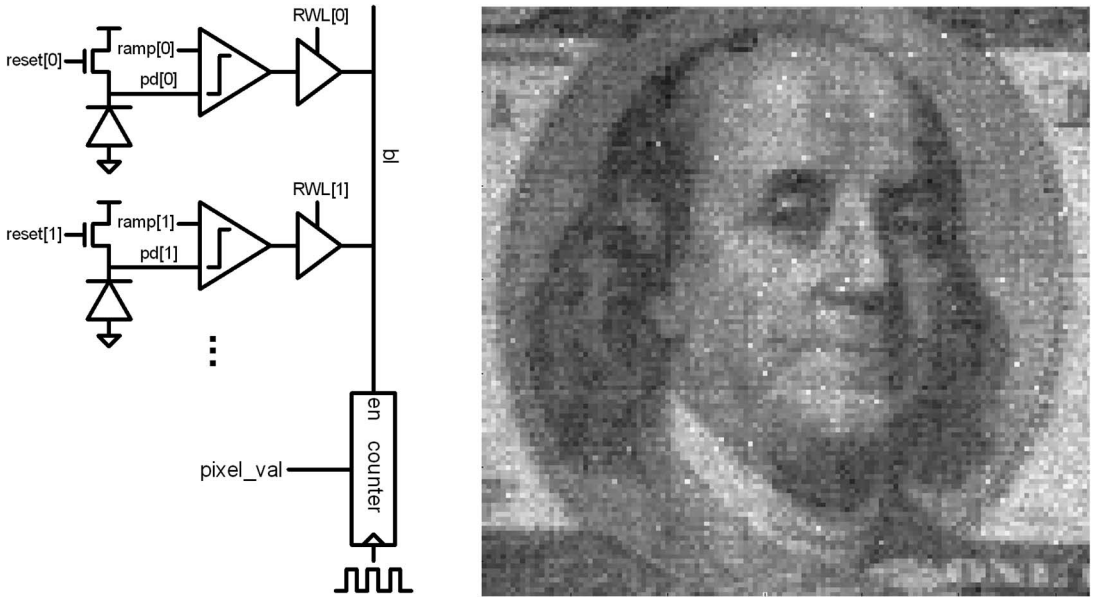

Fig. 5. ***PWM image sensor BL structure and 128 × 128 test image [18].***

carriers are then swept out of the depletion region through diffusion, creating a photovoltaic current that is related to light intensity. The photovoltaic voltage is commonly driven onto a column-shared bitline (BL), digitized with an ADC, and processed to determine the original light intensity [17].

For lower power operation, the V_{DD} of the array can be voltage scaled to reduce dynamic switching energy, as further discussed in Section III. However, this reduces the I_{ON} to I_{OFF} ratio of pixel devices, increasing the relative amount of leakage onto BLs from unaccessed pixels and decreasing the functional robustness of the analog BL scheme. For more robust low-voltage operation, pulse-width modulation (PWM)-based image sensors have been proposed that drive a pulse onto the BL instead of a voltage [18], [19]. Each pixel in the image sensor array contains a photovoltaic diode, comparator, and a read buffer. The reverse-biased photodiode is precharged to a set voltage and then exposed to light, causing photocurrent to lower the voltage on the capacitor. This voltage is compared with a ramp signal to generate a pulse with duration from the beginning of the ramp until the ramp voltage equals the photodiode voltage. The resulting pulse is driven onto the BL with a read buffer, composed of two n-channel metal–oxide–semiconductor (NMOS) devices, controlled with a read wordline (WL). One counter per BL is enabled for the duration of the pulse, and the counter value represents the photodiode current. During each cycle, one pixel on each BL is read, and by sequentially firing all of the read WLs, the entire array is measured and an image is recorded. This mostly digital analog-to-time-to-digital technique can be voltage scaled to 0.45 V with suitable robustness and signal-to-noise ratio (SNR). A reported 128 × 128 image sensor achieves 23.4-dB SNR at 8.5 frames/s while consuming only 140 nJ per frame [18]. The low-power time-based scheme is more suited for the peak and average power requirements of a millimeter-scale system. A traditional CMOS image sensor would require battery overload protection and could only operate infrequently.

C. Amplifiers

Amplification is needed to provide gain for low-swing sensor outputs and provide adequate drive strength for subsequent circuits. For example, microvolt signals picked up by neural probes are too small for ADCs to digitize [21]. Noise sources, such as thermal and flicker noise from resistors or devices, can easily mask the intended signal. For this reason, the first stage of the sensor node's front end after the sensor itself is an LNA, designed to amplify the signal while maintaining a high SNR. In this section, we will focus on LNAs for sensor front ends. Many sensors, such as temperature, humidity, and certain medical sensors, have low-frequency outputs, so the required bandwidth is low. However, these applications have strict offset and SNR requirements. LNAs with vastly different requirements are also used in RF receivers to amplify signals picked up by the receiver antenna for chip-to-chip or chip-to-base station communication, as will be discussed in Section V.

LNAs for sensor front ends have been reported with power as low as 0.935 μW, using devices biased in weak inversion [22]. Although amplifiers are typically designed with devices in strong inversion, weak inversion provides a higher gain to direct current (dc) power ratio. However,

bandwidth and SNR are degraded. The following discussion provides a general, first-order analysis of these effects. Gain is the product of transconductance and load resistance ($g_m R_o$). If the load is an active device and all devices are switched from strong to weak inversion, g_m decreases with the square root of drain current (I_D) and R_o increases almost inversely with I_D. Therefore, gain is not catastrophically degraded [see (2)]. Bandwidth scales with the reciprocal of the product of resistance and capacitance at the node causing the dominant pole. R increases, but C remains constant, so bandwidth degrades [see (3)]. Thermal noise increases with R, decreasing SNR [see (4)]. The noise floor for weakly inverted devices does not depend as heavily on dc bias current, allowing for further power savings [23]

$$\text{Gain} \propto g_m R_o \propto \sqrt{I_D}\frac{1}{I_D} \propto \frac{1}{\sqrt{I_D}} \tag{2}$$

$$\text{Bandwidth} \propto \frac{1}{RC} \propto \frac{1}{1/I_D \times 1} \propto I_D \tag{3}$$

$$\text{Thermal Noise} \propto 4kTR \propto 4kT\frac{1}{I_D} \propto \frac{1}{I_D}. \tag{4}$$

A 3.5-μW LNA for amplifying low-frequency electroencephalographic (EEG) signals from electrodes placed on the scalp is presented in [20]. The chopper-stabilized LNA mitigates the effect of flicker noise and dc voltage offsets, making it applicable for a variety of low-frequency sensor outputs. EEG signals are generated by electrical activity in the brain and contain information used to diagnose epilepsy and comas. Since EEG signals have frequencies of less than 200 Hz, they lie within the noise envelope of $1/f$ flicker noise, making low-noise amplification difficult [24]. As shown in Fig. 6, the LNA mixes the input signal (x) with the chopper signal (c). The chopper signal is often a square wave with 50% duty cycle. The square wave must have a frequency that is higher than the corner frequency of flicker noise and two times the highest frequency component of the signal to prevent aliasing. The mixed signal is amplified with an LNA that introduces noise and offset (n). The amplified version of the original signal is created by mixing the output of the amplifier with the chopper signal again. The flicker noise and amplifier offset are transposed only once and modulated to higher frequencies at harmonics of the chopping signal [25]. The modulated noise and offset, as well as charge injection from the mixers, is filtered out with a low-pass filter.

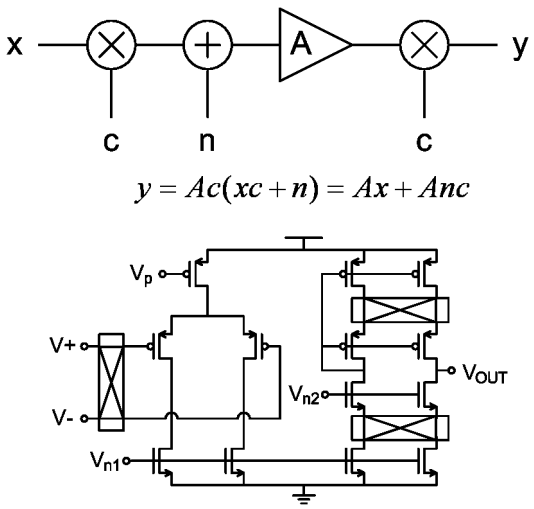

Fig. 6. *Chopper LNAs cancel out flicker noise and dc offset [20].*

D. Analog-to-Digital Converters

After amplification, data from analog sensors are converted to a digital value so they can be processed, stored, and transmitted. Successive approximation register (SAR) ADCs have been widely used and perform a binary search of the voltage range to find the input voltage. A digital-to-analog converter (DAC) is used to create the analog representation of the digital value stored in a register. This is compared with the input voltage and the register is adjusted accordingly based on whether the input voltage is higher or lower than the register value. Microwatt SAR ADCs with figures of merit (FOMs) down to 4.4 fJ per conversion step have been designed for sensor applications [26]–[28]. Voltage and frequency scaling in SAR ADCs offers promising tradeoffs for power and performance, showing the potential for a lower bound on FOM. Challenges with voltage scaling include implementing a low-voltage comparator with very low voltage offset to minimize nonlinearity.

Dual-integrating slope (DIS) and pulse position modulation (PPM) ADCs convert the analog input values to a time and then create a digital output with a TDC. These mostly digital techniques are more robust for low-voltage operation than analog techniques, providing another opportunity for even lower FOM. As shown in Fig. 7, DIS ADCs charge a capacitor with the input voltage (V_{IN}) through a resistor for a fixed time. V_{IN} has sufficient drive strength to charge the capacitor since it was buffered in the previous stage. After the capacitor is charged, a TDC is started and the capacitor is discharged to ground. The capacitor voltage is measured with a comparator and a stop signal for the TDC is generated when the capacitor is discharged [22]. This topology is ideally insensitive to the circuit parameters R and C, making it more tolerant to process and temperature variations, which are especially prevalent in low-voltage operation. PPM ADCs operate on a similar principle where pulse position instead of duration is modulated. The power of the ADC is directly related to the ADC sampling frequency. Uniform sampling requires a sampling rate of 8× the frequency of interest. Using nonuniform sampling techniques, the oversampling rate can be reduced to 1.7× by using a postprocessor to

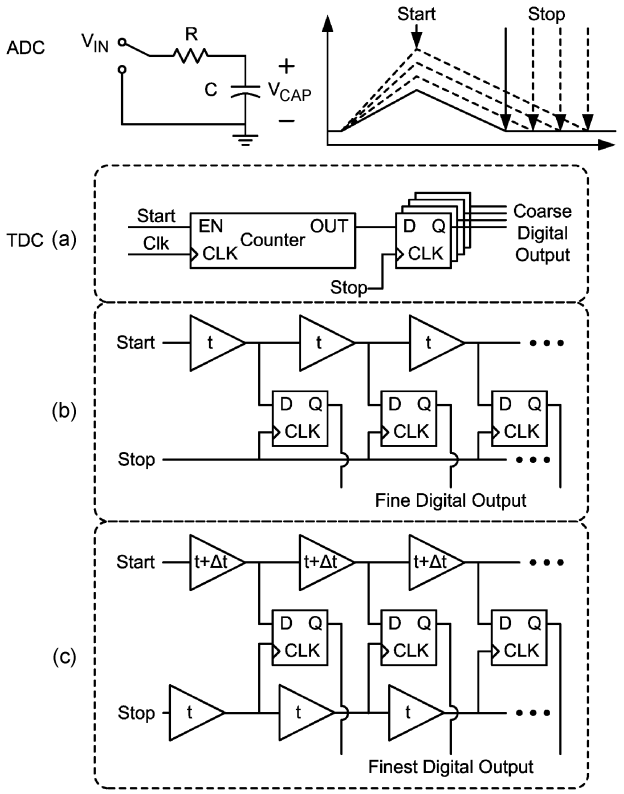

Fig. 7. *TDC topologies used in time-based ADCs [29], [30].*

reconstruct an analog signal with the same maximum frequency of interest. This technique used with a PPM ADC achieves an FOM of 98 fJ per conversion step [29].

The TDCs used in these ADC topologies can be implemented by starting a counter when the capacitor is charged and recording the counter value when it is discharged. Alternatively, a TDC can send a pulse down a delay line when the capacitor is charged and monitor the position of the pulse when it is discharged. If the delay of each element is t, then the time resolution is also t. The delay line resolution can be improved with differential-delay Vernier chain techniques. The start and stop signals are delayed t and $t + \Delta t$ between each register, making the time resolution Δt [30], [31].

III. PROCESSORS

Sensors have the ability to gather large amounts of data about their surrounding environment. However, not all of these data contain useful information. For example, sensors monitoring stress in bridges only need to report when faults are found. Transmitting raw sensor data wirelessly requires a great deal of energy, since active radios are generally power hungry compared to other sensor node circuitry. Moreover, frequent wireless traffic leads to data congestion in wireless sensor networks, increasing data latency. To avoid these effects, many wireless sensor nodes perform digital signal processing to extract and compress useful sensor data with a microprocessor before transmission.

The power used by the microprocessor is a concern. In general, simple processor instruction set architectures and microarchitectures trade off performance, in terms of frequency and possibly cycles per instruction, for power and require less energy to complete an identical task. While conventional designs employ clock gating and operand isolation to further reduce power, these methods alone are insufficient to meet the stringent power budgets of miniature wireless sensors.

V_{DD} scaling is perhaps the most effective way of reducing processor power, with several designs achieving 2 pJ per instruction [22], [32], [33]. Voltage scaling has a strong effect on energy consumption since the dynamic switching energy of the microprocessor scales quadratically with V_{DD}. Voltage scaling also increases latency, especially when V_{DD} is scaled below the device threshold voltage (V_{TH}) to the subthreshold region. Even though leakage power scales down with V_{DD}, leakage energy per cycle increases because of this increased latency. In typical operation (V_{DD} of $\sim$1 V today), active energy is orders of magnitude higher than leakage energy, however, as shown in Fig. 8, the competing trends in dynamic and leakage energy result in an intermediate voltage (V_{MIN}) where total energy per instruction (E_{MIN}) is minimized [34]–[36].

Although low-voltage operation increases energy efficiency, the robustness of circuits is reduced because of smaller noise margins and increased susceptibility to process variations. Noise margins degrade with V_{DD} because of reduced on-to-off current ratio. Also low-voltage devices are more sensitive to process variations, further reducing noise margins. V_{TH} variations due to random dopant fluctuations (RDF) dominate other sources of variation at such

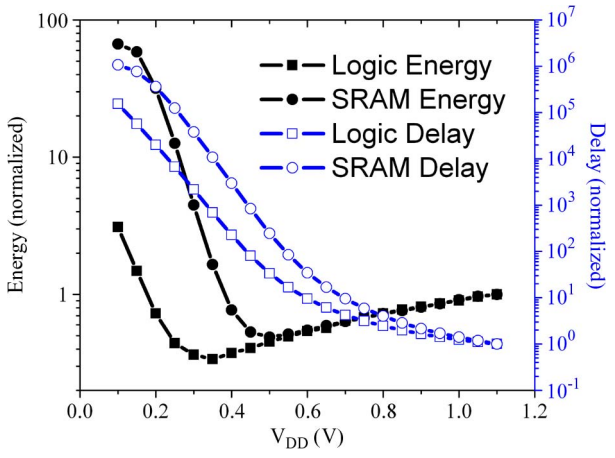

Fig. 8. *Dynamic energy and leakage power decrease as V_{DD} is scaled down. Latency and leakage energy per cycle increase. The minimum total energy per cycle is achieved at an intermediate voltage (V_{MIN}).*

low voltages. While removing high fan-in gates, series transmission gates, and dynamic logic is sufficient to maintain functional robustness, process variations create up to a 300% delay variation in a subthreshold logic gate, leading to high margins to meet timing yield. Since RDF variation is uncorrelated, its effects on critical path delay can be decreased by increasing the logic depth between pipeline stages [37].

IV. MEMORY

Increased memory sizes permit wireless sensors to perform more complex digital signal processing algorithms and log more sensor data. Memories should be dense to increase capacity in a fixed system volume, while exhibiting robust operation within the sensor's power budget. In this section, we discuss volatile, CMOS-compatible memories including static random-access memory (SRAM) and embedded dynamic random-access memory (DRAM).

A. SRAM

Voltage scaling reduces dynamic energy consumption in memories as well as in processors (Fig. 8). However, low-voltage SRAM is prone to functional failures because process variations lead to destructive read operations and insufficient write margin [38]. In addition, since many sensor systems require large amounts of SRAM in which the vast majority of bitcells must function for chip yield, SRAM bitcell yield must be extremely high. A write operation in the common differential six-transistor (6T) bitcell [Fig. 9(a)] is performed by raising the WL voltage and asserting a differential value on the BLs. A read operation is performed by precharging BLs to V_{DD}, letting them float, and then asserting the WL so the bitcell can drive its value on the BLs. Write margin is improved by increasing the strength of the pass gates (A_3, A_4) relative to the pull-up devices (A_1, A_2). Read stability is improved by increasing pull-down strength (A_5, A_6) relative to the pass gates. Designing the bitcell for higher write margin generally decreases read stability and *vice versa*, creating a fundamental robustness limit. Device sizing and SRAM assist circuits such as dual-V_{DD} WL circuits can improve low-voltage SRAM robustness, but are not sufficient to enable robust near-threshold or subthreshold SRAM [39].

The eight-transistor (8T) bitcell [Fig. 9(b)] achieves higher low-voltage robustness at the expense of lower density by using a separate buffer for read accesses (B_7, B_8) [38], [40], [41]. This allows the cross-coupled inverters

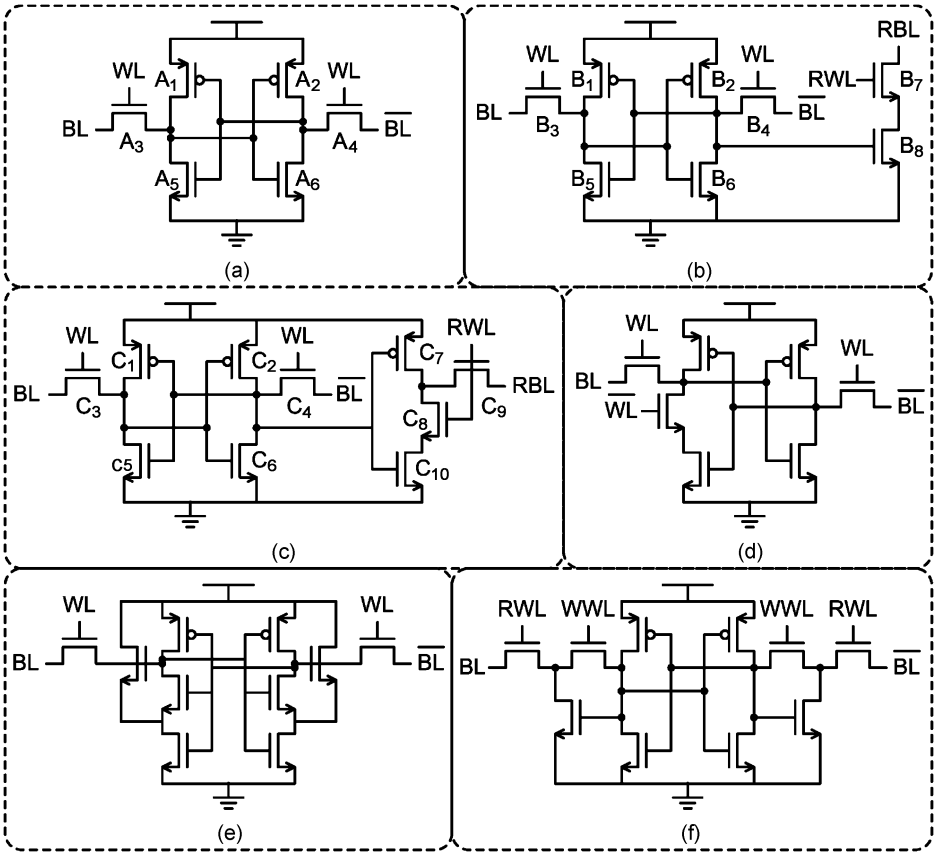

Fig. 9. *SRAM designs for low-voltage low-power operation.*

and pass gates to be sized optimally for writes, while making the bitcell virtually immune to destructive reads. A 4-kB commercial 8T subarray was demonstrated with 295-MHz operation at 0.41 V [41]. Although the 8T bitcell is tolerant to destructive reads, read operations can still fail if the bitcell is unable to pull the read bitline (RBL) down quickly enough to meet timing constraints. Another read-failure mechanism is undesired RBL discharge because of leakage from unaccessed bitcells. This failure mode is aggravated when V_{DD} is scaled because of reduced on-to-off current ratio. To reduce contention from unaccessed bitcells, the ten-transistor (10T) bitcell [Fig. 9(c)] lowers read buffer leakage current by placing two off n-channel field-effect transistor (NFET) devices (C_8, C_9) in series between the RBL and ground and also pulls the RBL up during the read of a one to prevent undesired discharge [42]. BL leakage can be mitigated further through compensation with leaking column headers or footers [43]. 8T and 10T bitcells have demonstrated access energies as low as 0.22 fJ/b [32], bitcell leakage as low as 3.3 fW/b [8], robustness during minimum energy operation, and reasonable area overheads, making them viable candidates for sensors.

While 8T and 10T bitcells improve read and write margins, write margins can still be an issue, hold margins are not addressed, and bit interleaving is more cumbersome. The read-SNM-free bitcell [Fig. 9(d)] improves read margin by cutting the feedback loop during accesses [44]. Hold errors occur when SRAM state is lost between accesses and hold margins can be improved by incorporating Schmitt triggers into the cross-coupled inverters [Fig. 9(e)] [45]. Pseudowrite errors occur when unaccessed bitcells on the same WL as accessed bitcells experience destructive read errors. The 8T and 10T bitcells are not tolerant to pseudowrite errors since unaccessed bitcells experience read-like conditions similar to the differential 6T bitcell. In these bitcells the WL must be segmented if column multiplexing is employed, making bit interleaving difficult. Bit interleaving is desirable to prevent single-event upsets caused by neutrons from corrupting multiple bits of one word. Having at most one error per word allows these failures to be fixed with simpler error correction codes (ECCs). A subthreshold differential 10T SRAM [Fig. 9(f)] that tolerates pseudowrite accesses can be implemented with series pass gates driven with WLs in orthogonal directions [46]. Both pass gates are turned on during write and only one pass gate is turned on during read.

B. Embedded DRAM

While 8T and 10T SRAM have higher robustness than differential 6T SRAM at low voltages, they are considerably larger because of increased device count. The increased bitcell area can limit memory sizes in sensor nodes that require a small form factor. Embedded DRAM (eDRAM) (Fig. 10) is fully compatible with CMOS logic and only requires two or three devices per bit, substantially

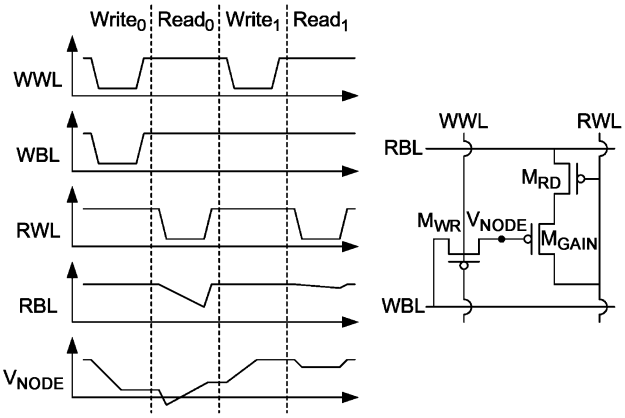

Fig. 10. ***Embedded DRAM is denser than SRAM [47].***

increasing memory densities. Its access power is high, thus it is most suitable for long-term storage of data that is accessed infrequently. While traditional DRAMs connect the data storage capacitor to the RBL with a pass gate, gain cells use the transconductance of a gain device (M_{GAIN}) to increase read speeds [48]. Read speed is further improved in boosted gain cells since the voltage on the data storage node is boosted during a read operation. During a read operation, RWL transitions from V_{DD} to V_{SS}. This voltage change couples charge into the storage node (V_{NODE}) through the gate-source capacitor of M_{GAIN}. Boosting the storage node increases the overdrive of the gain device and decreases read latency by 41% [47]. In addition to increased density, eDRAM can achieve higher read and write margins than differential 6T SRAM and has lower leakage power due to reduced device counts.

eDRAM stores data as a floating charge that must be periodically refreshed, requiring dynamic power. Therefore, data retention time is a critical metric for determining refresh rate and overall memory power. To increase retention time, the subthreshold leakage through the write device (M_{WR}) should be minimized. Subthreshold current is especially large in cells containing a ZERO during the write of a ONE to an adjacent cell sharing the same write bitline (WBL). A boosted voltage on the write wordline (WWL) can be used to super-cutoff the write device, but this requires a costly charge pump or external V_{DD}. Super-cutoff NMOS devices have negative gate-source voltages (positive for PMOS), resulting in lower-than-off drain currents [49]. Alternatively, a lower WBL voltage can be used to write a ONE. One convenient voltage to use is the steady-state voltage of V_{NODE} when storing a ONE. Writing a ONE with this voltage keeps unaccessed M_{WR} devices super-cutoff, but does not increase the off-current during the read of a ONE. Retention power has not been fully studied for low-voltage operation, but refresh power of 91 pW/b at a rate of 1 ms is reported at a V_{DD} of 1 V [47].

V. WIRELESS COMMUNICATION

Wireless communication is a critical function for any wireless sensor and can be achieved using a variety of media including light [50], sound [51], electric fields [52], and RF electromagnetic fields. RF communication is the predominant approach for wireless sensor networks and is the focus of this section. Without proper attention, the RF transceiver can easily dominate the power budget of a wireless sensor. Even the most energy-efficient transceivers based on standards like ZigBee, Bluetooth, and WiFi consume tens of milliwatts of power today, which is well in excess of the power budget of a typical wireless sensor node. The power consumption of wireless transceivers must be reduced both at the circuit level by developing more energy-efficient RF circuits and at the system level by using RF communication more judiciously. We discuss circuit-level and system-level techniques in the remainder of this section.

A. Circuit Techniques

Fig. 11(a) shows a simplified diagram of an RF transmitter. A digital bitstream (generated by a data encoder) is overlaid on a carrier frequency (created by a frequency generator) using a modulator. The modulated signal is then driven onto an antenna by a power amplifier. Fig. 11(b) shows a simplified diagram of an RF receiver. The incident RF signal is first filtered to remove unwanted signals and then amplified by an LNA. The digital signal is then extracted from the RF signal using a frequency generator and a demodulator. The raw data are finally extracted using a data decoder.

The power consumption of each of these RF building blocks must be minimized. One promising circuit technique is the use of weak inversion operation in the RF building blocks. It has long been known that analog circuit power can be reduced dramatically by operating transistors in the weak inversion region (i.e., using leakage current) [53], and it has been shown more recently that weak inversion operation is useful for RF circuits like LNAs [54]. Low-voltage operation has begun to receive attention from researchers as well. For example, the receiver presented in [55] is able to achieve significant power reductions by operating at either 0.5 or 0.65 V. However, due to low bandwidth, weak inversion and low-voltage design are not suitable for components requiring high-frequency operation.

The use of high-quality RF-MEMS passive components also holds promise for power reduction. Bulk acoustic wave (BAW) resonators can be used to achieve excellent filtering in receivers. The use of high-quality filters relaxes the design requirements on other components in the receiver, thus enabling power reductions. For example, the receiver in [56] uses BAW-based filtering to relax frequency precision requirements and to enable the use of a low-power ring oscillator for local frequency generation. RF-MEMS components can also be used to generate a high-frequency carrier signal without the need for a crystal and power-hungry frequency multiplication circuitry. A thin-film bulk acoustic wave resonator (FBAR) is used in [57] to generate a 1.9-GHz carrier frequency with only 300 μW of power.

Significant improvements to energy efficiency can also be achieved by selecting radio architectures different than the standard narrowband architectures. Ultrawideband (UWB) transceivers, which send narrow pulses of energy to transmit data, have a number of attributes that are well suited to low-power operation. In particular, UWB transmitters can be extremely simple with only a pulse generator driving a power amplifier and antenna. It is not necessary to generate a precise carrier frequency using a local oscillator, a power-intensive task in conventional

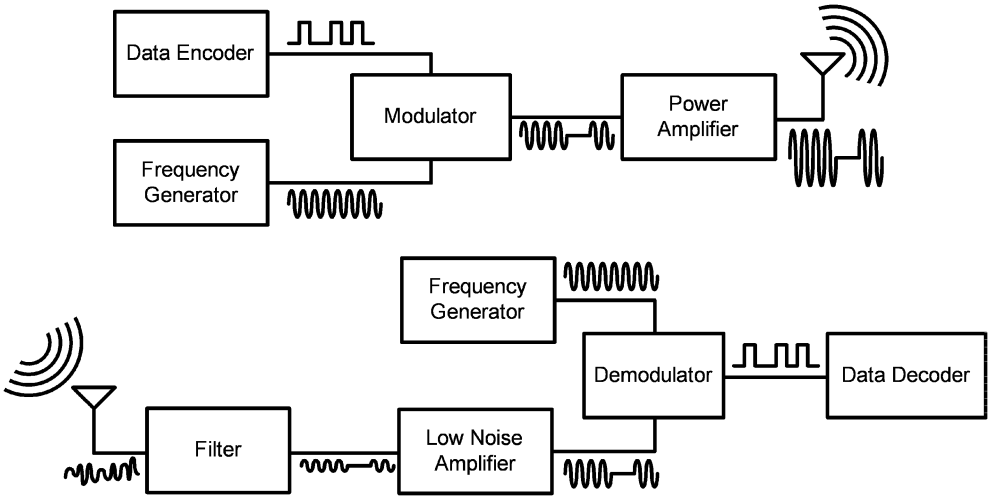

Fig. 11. *Simplified diagrams of (a) an RF transmitter and (b) an RF receiver.*

radios. Without a carrier frequency generator, a UWB transmitter can very quickly power up and power down, making duty cycling simple. The simplicity of UWB transmitters also makes an all-digital implementation possible, thus eliminating the large bias currents demanded by typical analog blocks. UWB transmitters have been demonstrated with energy consumption as low as 47 pJ/pulse [58]. One disadvantage of UWB is that transmission power is generally low, and the signal is affected by all noise within the broad frequency spectrum of the signal. These constraints increase the receiver complexity and power requirements to achieve high SNR. The receiver complexity makes UWB a good candidate for systems with asymmetric communication, but nonideal for peer-to-peer networks, as discussed in Section VIII-C.

Backscattering radio architectures have also received significant attention for systems with stringent power constraints, particularly radio-frequency identification (RFID) tags [59]. In a backscattering system, a high-power reader device broadcasts an RF signal to a simple, low-power transponder device. The transponder device, which does not have a power amplifier or a carrier frequency generator, transmits data back to the reader device by modulating the impedance of its antenna, effectively reflecting incident RF energy back to the reader (i.e., "backscattering" the signal). The receiver may also be implemented in a simple, energy-efficient fashion, permitting both the transmitter and the receiver to be powered exclusively by energy harvested from the incident RF signal. For example, the transceiver in [59] only needs to scavenge 16.7 μW of incident power to run both the transmitter and the receiver. The primary drawbacks of a backscattering system are limited communication distance (< 10 m) and the need for an asymmetric communication scheme with a high-power reader and a low-power transponder.

B. System Techniques

While the energy efficiency of circuit components will play an important role in reducing the power overhead of RF communication, system-level techniques play perhaps a more important role in determining energy efficiency. One of the simplest solutions is shortening the transmission distance. The Friis transmission equation [60] indicates that a shorter communication distance may be exploited by reducing transmission power and/or receiver sensitivity (which is tightly coupled to receiver power). Longer communication distances can be achieved using multihop communication. The energy required to pass a message increases only linearly with distance in a multihop network while it increases super linearly with distance under realistic conditions in a single-hop network [61].

Similarly, power can be reduced significantly by minimizing the amount of data sent over the RF link. An onboard microprocessor can analyze data locally to determine which pieces of data should be sent off-chip and can also compress data packets to further reduce the burden on the transceiver. With microprocessor power consumption as low as several hundred nanowatts [32], local data processing is far more energy efficient than RF transmission.

The greatest opportunity for power reduction lies in heavy duty cycling. By powering down the transceiver during idle periods, the average power consumption of the transceiver can be reduced dramatically. A radio that consumes 20 mW in active mode and 1 μW in sleep mode consumes only 1.6 μW on average if it is active for 100 ms every hour. The primary challenge posed by heavy duty cycling is determining when to power on the transceiver. Asynchronous protocols constantly "listen" for radio traffic and fully wake the transceiver only when demanded by inbound radio traffic. Conventional receivers draw a great deal of power (milliwatts or more), but simplified "wake-up" receivers can listen for power-on requests. Recent work has shown that these receivers can be implemented with power as low as 52 μW [56]. Alternatively, synchronous protocols [62] use local timers to periodically wake up the transceiver for communication. To minimize power-on time, the local timers must be as accurate as possible, with minimal jitter and drift. This is an extremely challenging problem under tight power constraints and will be considered in more detail in Section VIII.

VI. POWER MANAGEMENT

Microprocessors and other digital circuits in a sensor node run with the highest energy efficiency at subthreshold or near-threshold V_{DD} ranging from 300 to 600 mV. Analog components usually require higher V_{DD} in the range of 1.2–2.5 V to ensure proper voltage headroom and transmission power levels. Meanwhile, common power sources incorporated in sensor nodes, such as batteries and fuel cells, are limited in their output voltages by their chemistries and their voltages degrade with use. Lithium (3.3–4.2 V), alkaline (1.5 V), and zinc-air (1.5 V) battery chemistries are common. Thin-film batteries are created by depositing layers of electrolytic materials using semiconductor manufacturing techniques [63]. These batteries can be very small in size with reasonably high-energy densities. While many thin-film batteries are planar, the energy density can be further increased by using 3-D processing to increase the surface area between the electrolytic materials [64]. Fuel cells draw their energy through chemical reactions with an external fuel source such as ethanol and can be integrated with CMOS processes [11]. Since battery voltages do not usually match the desired circuit supply, dc-to-dc converting power electronics are necessary. Most power electronics are designed for high output power levels and do not efficiently convert the low levels of power needed by sensor nodes. For effective sensor nodes, power electronics must be specifically designed for low-power applications. A summary of

Table 1 Demonstrated Power Management Results

DC-DC Down Conversion	Power Efficiency	Load Power	Conversion Ratio
Hybrid [73]	55 %	125 nW	9
Buck Converter [76]	80 %	1 μW	2.4
DC-DC Harvesting	**Power Efficiency**	**Load Power**	**Input Voltage**
SCN [8]	41 %	0.93 μW	872 mV
Boost Converter [78]	50 %	0.75 μW	20 mV
AC-DC Rectification	**Power Efficiency**	**Load Power**	**Input Amplitude**
Telemetry [82]	65 %	140 μW	1.5 V
Harvesting [80]	98.3 %	90 μW	3 V

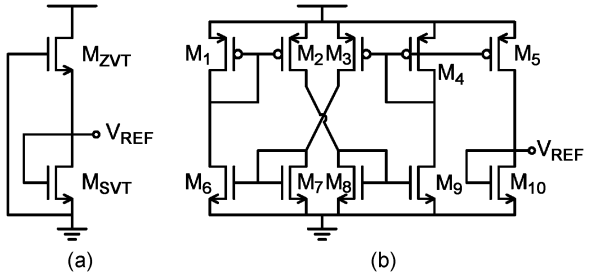

Fig. 12. *References voltage generators for linear regulation [68], [69]. (a) Constant reference. (b) CTAT reference.*

results for demonstrated power management units is shown in Table 1.

A. Linear Regulation

Linear regulators create an output supply by buffering an analog reference voltage using an amplifier that is powered from a higher input supply voltage. The ideal power efficiency of a linear regulator is the ratio of the output to input supply voltages, however additional power overhead is needed to supply the quiescent current for the amplifier. Minimizing this power overhead is vital for low-power operation, but can reduce the amplifier bandwidth. This in turn degrades the regulator's transient response to load power fluctuations, resulting in power supply noise that can increase circuit latency and decrease SRAM robustness [65], [66]. For ultralow-power design, bias currents as low as 30 nA are reported, with adequate transient response for powering a subthreshold processor [8]. One method of maintaining proper transient response while minimizing regulator power is to dynamically increase the bias current and increase bandwidth when load power surges are detected [67]. In this regulator design, power surges are detected by dropping the supply voltage across a diode. This diode voltage controls both switches that limit the supply surges and the tail current devices used in the linear regulator.

The output voltage of a linear regulator is determined by a reference voltage generator. Band gap and constant-g_m references are commonly used in power management systems, but tend to have microamp-level quiescent currents that can single-handedly exceed the power budgets of low-power sensor nodes. A picoamp voltage reference [Fig. 12(a)] with low V_{DD} and temperature sensitivity can be generated based on the subtraction of threshold voltages [68]. Although device threshold voltage changes with temperature, the threshold voltage of devices with different V_{TH}'s scale together so the difference is constant with temperature. One method of obtaining this voltage is to connect a diode-connected nominal-V_{TH} NFET device (M_{SVT}) in series with a super-cutoff zero-V_{TH} NFET device (M_{ZVT}). When the devices are properly sized, the output voltage will settle to one half of the difference of the V_{TH}'s because of the equal current condition. Since both devices are in the subthreshold region, this 19.4 ppm/°C temperature reference can be realized with only 2.2-pW power consumption.

Other voltage references with low-temperature coefficients can be created by combining a CTAT device threshold voltage with a multiple of the PTAT thermal voltage [70]. While these voltage references have a low-temperature coefficient, a CTAT power supply can be used in subthreshold circuits to keep the frequency of CMOS logic supplied by the regulator constant with temperature [69]. One CTAT reference voltage [Fig. 12(b)] supplies a constant current through a diode connected device (M_{10}). The temperature-independent current is generated by equating the currents of a high V_{TH} subthreshold device (M_6, M_8) with low-V_{TH} saturated devices (M_7, M_9). When temperature increases, the device threshold of M_{10} and the reference voltage decrease. The CTAT power supply balances the effects of temperature on subthreshold logic, which is faster at high temperatures because threshold voltage decreases, resulting in less than 5% frequency variation with temperature.

B. Switched Capacitor Networks

Linear regulation provides a stable level-converted output voltage, but is limited in its power efficiency to the ratio of the load voltage to the input voltage. For systems where the conversion ratio is high, such as when down-converting a 3.6-V Li-ion battery to subthreshold levels, high efficiency is not attainable. In these scenarios, switched capacitor networks (SCNs) or buck down-converters can be used to attain higher power efficiencies [33], [71]. SCNs connect the voltage input and output to capacitors in different configurations to convert dc voltage levels. The capacitors are connected in different configurations using switches, such as MOS devices, and can be used to up-convert or down-convert voltages. SCNs commonly alternate between two configurations, converting voltages at a fixed ratio. However, more than two configurations can be used to allow the circuit to convert voltages with several different ratios [72].

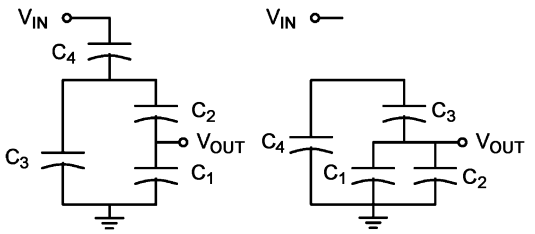

Fig. 13. *Fibonacci switched capacitor network for dc-to-dc conversion [73].*

A hybrid SCN and linear regulator system has been reported that can convert from a 3.6-V Li-ion battery to subthreshold voltage levels for 5–500-nA loads with up to 55% efficiency, representing a 4.6× efficiency improvement over ideal linear regulation [73]. A Fibonacci SCN network, shown in Fig. 13, is used to divide the battery voltage by 5. Normally, MOS switches in SCNs are large to reduce conductive losses within the network. However, since this SCN network was designed for very low-power loads, nearly minimum sized devices are used for switches. This reduces the power overhead required to switch the gate capacitances of these switches and increases the overall efficiency of the system. Typical SCNs are clocked at megahertz levels, but this network uses a 2-kHz clock to reduce power overhead. The slow clock is efficiency generated using a slow timer circuit, discussed in Section VII. The outputs of SCN networks are noisy unless the switching frequency of the network is very high. Since the power budget precludes such high-frequency operation, a linear regulator with a low conversion ratio is used to eliminate voltage ripples on the output supply.

C. Buck Converters

Buck converters alternately connect a power source to an inductor to store energy and discharge that energy into the load (Fig. 14) [74], [75]. Efficiencies of 80% at a 1-μW load power and with a 2.4× conversion ratio have been reported [76]. The duty cycle between storing and discharging energy determines the dc-to-dc conversion ratio. This duty cycle can be dynamically adjusted to keep the output voltage at the minimum energy point (V_{MIN}) for the highest efficiency computation in CMOS logic [76]. The energy used by the circuit is measured by supplying the circuit from a capacitor (C_{SUPPLY}) charged to V_1. The load circuit is run for a set number of instructions (N) and then the voltage on C_{SUPPLY} after operation (V_2) is measured. The energy consumed (E_{OP}) is computed with (5). For stable operation, V_1 and V_2 should be nearly the same. This also allows for the energy consumed to be approximated with (6). V_1 is set by the system and the difference between V_1 and V_2 is determined by measuring how long it takes to discharge a copy of C_{SUPPLY} from V_1 to V_2 at a known rate. Once E_{OP} is known, a hill climbing algorithm

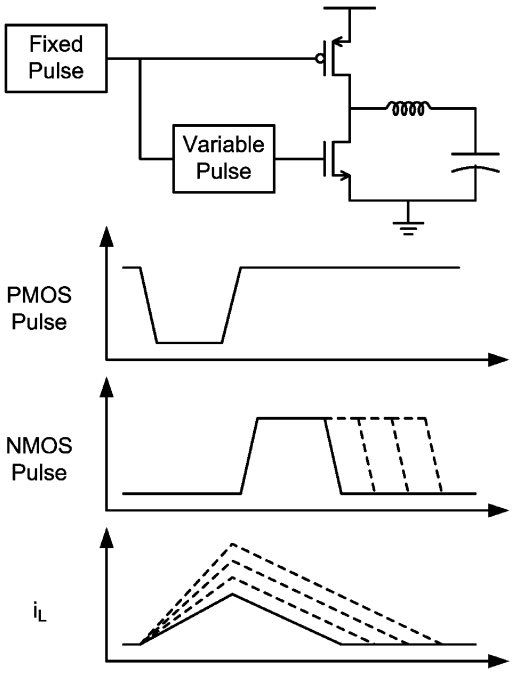

Fig. 14. *Buck converter that tracks the energy optimal* V_{DD} *[76].*

is used to control the buck converter's duty cycle and find V_1 where the minimum energy is consumed

$$E_{\mathrm{OP}} = \frac{C_{\mathrm{SUPPLY}}(V_1 - V_2)^2}{2N} = \frac{C_{\mathrm{SUPPLY}}(V_1 + V_2)(V_1 - V_2)}{2N} \tag{5}$$

$$E_{\mathrm{OP}} \approx \frac{C_{\mathrm{SUPPLY}} V_1 (V_1 - V_2)}{N}. \tag{6}$$

D. DC Energy Harvesting

Since batteries and fuel cells have limited energy capacities, they must be replaced or recharged for longer sensor lifetime, regardless of dc-to-dc conversion efficiency. Switched capacitor networks and boost converters can be used to up-convert voltages from energy harvesting sources. Energy harvesters such as photovoltaic solar diodes and thermocouples produce a dc voltage output. In solar diodes, light generates electron–hole pairs in the diode's depletion region, resulting in a potential gradient. Thermocouples produce an electric potential across a metal through the Seebeck effect when a temperature gradient is applied. The availability of harvested energy varies heavily with the environment, so it must be stored in a secondary power source, such as a battery, to ensure a reliable supply. Since harvesting sources usually have voltages below 600 mV, up-conversion is needed [77]. A boost converter converts harvested voltage from a

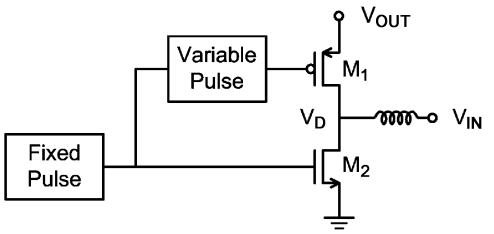

Fig. 15. *Boost converter for harvesting from 250-mV sources [78].*

thermoelectric generator (TEG) between 20 and 250 mV to a 1-V supply (Fig. 15) [78]. The boost converter alternately connects the harvested voltage through an inductor to the load and to ground. This alternately stores harvested energy in the inductor and delivers this energy to the load. The duty cycle between charging and discharging the inductor is dynamically adjusted to keep the output voltage at 1 V regardless of input. The boost converter operates in the discontinuous conduction mode and has the highest efficiency when the current through the inductor falls just to zero at the end of the discharge stage. This condition will result in mode V_D settling to zero volts immediately after M_1 opens. The value of V_D at this time point is measured with a comparator and used to increment or decrement a counter that controls the boost converter duty cycle.

E. Telemetry

Power can be delivered to a sensor node via RF telemetry to enable nearly infinite lifetimes, as done in passive RFID tags. RF energy can be received with an antenna and then rectified to create a dc voltage for supplying the load or recharging a secondary battery supply. Many passive RFID tags use cascaded voltage doublers to rectify the RF signal [Fig. 16(a)] [40]. Telemetry is a useful power delivery method for transcutaneous medical implants, since the RF source can be placed on top of the skin and close to the sensor, but battery replacement would require surgery. Several power receivers for medical implants have been proposed, but many of them require centimeter scale antennas since megahertz-frequency power is delivered to minimize power loss in tissue [81]. A power receiver for transcutaneous medical implants has been proposed using gigahertz-frequency power and a millimeter-scale antenna without preclusive power losses in tissue [82]. A matching circuit composed of a fixed inductor and tunable capacitor is used in the receiver to compensate for unpredictable factors such as antenna misalignment and variations in tissue composition to maximize power transfer. The received ac signal is rectified with a synchronous rectifier [Fig. 16(b)]. Diodes could be used to rectify the ac signal, however, the output voltage would be lower because of the diode voltage drop. Instead, MOS devices are actively turned on when the ac signal polarity is correct to supply

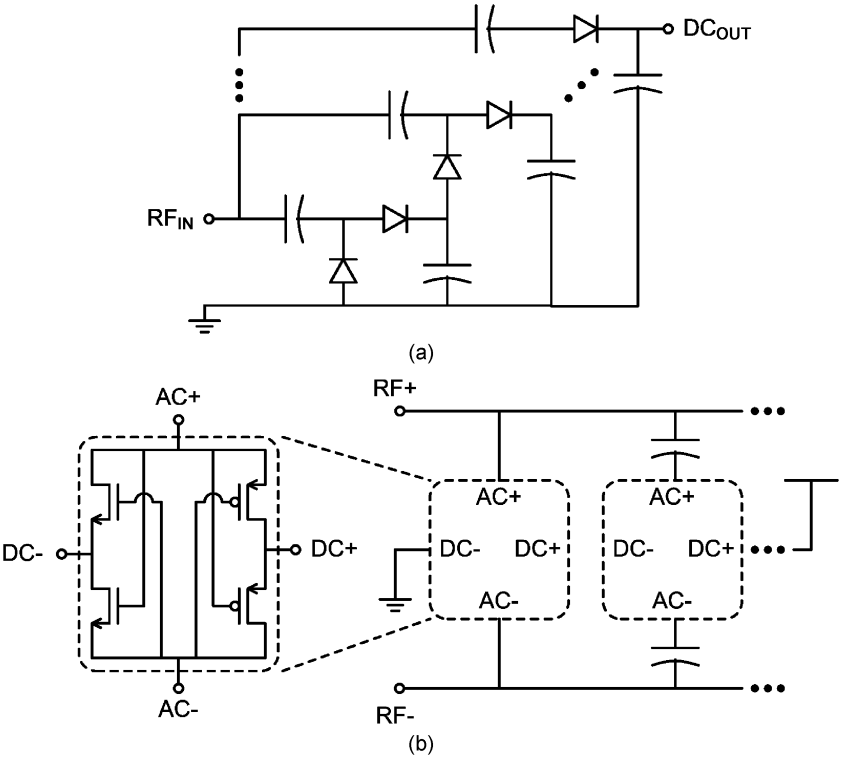

Fig. 16. *Rectifiers for ac-to-dc power conversion [79], [80]. (a) Voltage doubler. (b) Synchronous rectifier.*

the dc source. A gain of −33.2 dB is measured while transmitting RF power through 15 mm of bovine tissue.

F. AC Energy Harvesting

Synchronous rectifiers and other rectifier topologies can be used to convert harvested ac energy sources, in addition to telemetric sources. A permanent magnet can be shaken with a vibrating environmental source, such as a tire in a car, to generate ac current [79]. A piezoelectric cantilever or disk can also be vibrated to generate an ac supply [80]. A piezoelectric disk can generate multiple ac supplies at different points on the disc with different phases. A rectifier circuit that can harvest multiple phase-offset supplies can be generated by connecting multiple rectifiers in parallel.

VII. STANDBY MODE OPERATION

Many sensor measurements do not need to be taken continuously since environmental conditions can be periodically sampled. A sensor taking one image per second could adequately monitor automobile traffic, whereas one measurement per hour would be adequate for monitoring water levels in reservoirs. Even when sensor nodes must forward data from other sensors in the same wireless network, it is likely that a sensor node will be idle for long periods of time. Turning off unnecessary circuitry during these idle periods is necessary to meet the total energy budget of miniature sensor systems. The sensor front end and wireless communication can be power gated, eliminating static currents used in amplifiers and reducing leakage in sensors and ADC circuitry. The microprocessor can also be power gated, although some SRAM and balloon (retentive) latches must remain powered to retain previously logged sensor data and system state. Power gating can be achieved by powering the front end, microcontroller, and wireless communication circuitry from virtual supply rails that are collapsed during standby mode using either high threshold voltage (HVT) header or footer power gates (Fig. 17). For the microprocessor, the power gates must be properly sized to achieve both high active mode performance and low standby mode leakage. In analog circuits, the power gates must be turned on long enough before active system operation to allow the circuits to reach a stable dc state. While charging the power rails quickly has the benefit of faster system response time to external wake-up signals, it can cause resonance on the power rails due to the inductance of the supplies. Supply resonance can cause large voltage swings on the supply rails, resulting in the loss of data held in SRAMs and latches because the data-retentive voltage is violated. Supply resonance can be mitigated by gradually stepping the gate voltage of power gating devices [83] or by bypassing resonant current with supply monitors [84].

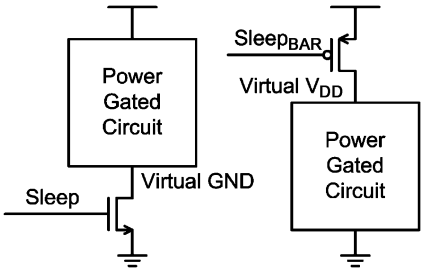

Fig. 17. *Power gating with an NMOS footer and a PMOS header [32].*

If the duty cycle of the sensor node is low, then the total system power is dominated by standby mode power. Sensors have been reported with standby power as low as 30 pW [32]. This power is limited by the leakage of circuits that are not power gated during sleep and the switching energy in the wake-up controller, which coordinates the sleep and wake-up procedure. To reduce overall standby leakage power, SRAM leakage and the amount of non-power-gated SRAM should be minimized. SRAM device V_{TH} selection and sizing is vital for leakage reduction. A 10T bitcell optimized for standby operation achieves a standby power of 3.3 fW/b while retaining state [8]. The bitcell shares the same configuration as the 10T bitcell discussed in Section IV-A but uses HVT devices and gate-length biasing for the cross-coupled inverters and pass gates. The read buffer is power gated during sleep since it is not needed for data retention. A similar 14T bitcell uses transistor stacking in the cross-coupled inverters to reduce leakage [32].

The sleep and wake-up controller must keep track of the time between sensor measurements. Crystal oscillators are widely used as process, voltage, and temperature-insensitive frequency references, but they violate the power budgets of many sensor systems. Low-power timer circuits have been reported. One typical approach for slow timers is to create a ring oscillator with current starved devices [Fig. 18(a)]. These devices use NMOS footers, PMOS headers, or both that are driven with analog bias voltages to reduce device currents and oscillator speed. However, obtaining very slow speeds requires biasing the starving elements deeply into subthreshold mode with the consequences of reduced voltage swing and increased frequency variation due to process and temperature variation. Also, bias voltage generation consumes additional power. Full-swing slow timers with reduced sensitivity to process variation can be realized using differential monostable multivibrational delay elements [Fig. 18(b)] [73]. These delay elements are reset into a high-impedance mode by the previous stage of the ring oscillator. Leakage slowly initiates a positive feedback loop that turns on devices in the delay element and causes the output to switch. However, these delay elements are still highly sensitive to temperature changes. Another topology uses device gate

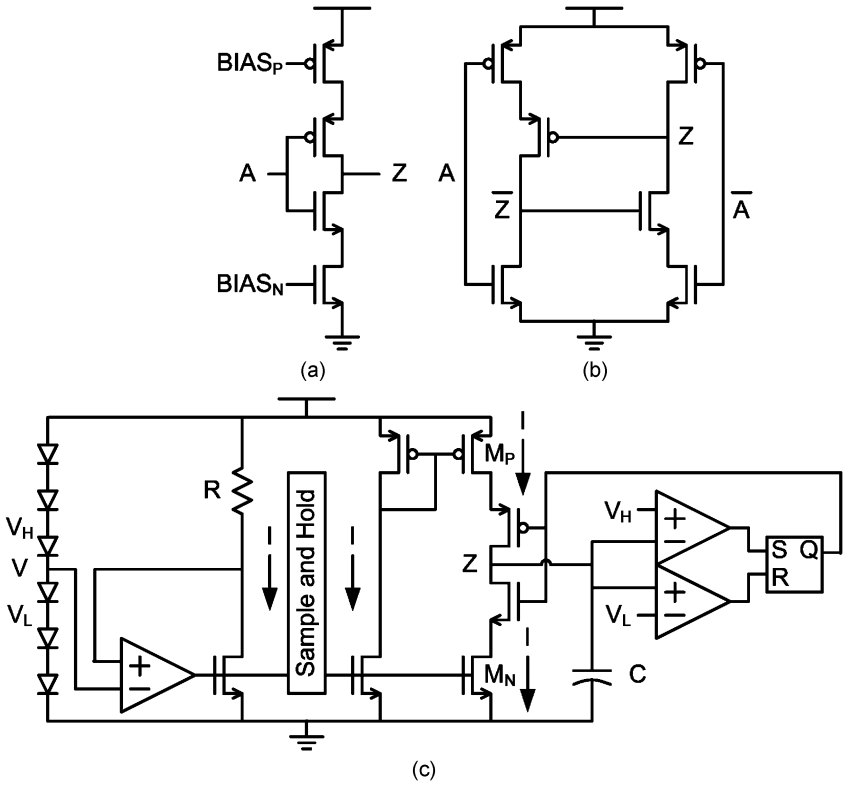

Fig. 18. *Timers for standby mode control [73], [86].*

leakage to generate subhertz oscillations with 1 pW of power [85]. Gate leakage is less sensitive to temperature changes than subthreshold drain current. However, it is highly sensitive to process variations in oxide thickness and is often poorly modeled.

Self-calibrating temperature compensation schemes can be employed for more accurate frequency references. One reported timer [Fig. 18(c)] generates a fixed current by dividing the supply voltage and forcing that voltage across a polysilicon resistor (R) [86]. This resistance has a low-temperature coefficient and can be trimmed to compensate for process variations. The fixed current is then mirrored to alternately charge and discharge a capacitor (C) to fixed voltage levels that are also derived from divided supply voltage references. This timer has a 5% cycle time error due to temperature variation and consumes 150 pW.

VIII. DESIGN TRENDS AND OPEN CHALLENGES

Important advances have been made to achieve millimeter-scale wireless sensors, but many design challenges remain. Chief among these challenges is wireless communication. While these challenges are tackled, the IC industry will inevitably evolve, providing new resources and obstacles in the field of wireless sensors. This section examines the effects of CMOS process scaling on ultralow-power circuits. We then discuss three related major obstacles to wireless sensors: antenna miniaturization, peer-to-peer communication, and sensor synchronization.

A. CMOS Process Scaling and Optimization

Process technology has a large effect on the minimum energy point and delay variation for digital circuits. It also strongly influences the variability in analog circuit metrics due to process variation. While newer processes are denser, ICs are often not the limiting factor for sensor size. In fact, trading area for lower power can reduce the total size of the system by allowing for smaller batteries. Newer processes have smaller device capacitances and lower dynamic energy, whereas older technologies exhibit lower subthreshold leakage and standby power. Thus, sensor systems with high duty cycles and short idle periods achieve lower energy with newer processes. Conversely, sensors with low duty cycles and long idle periods (the more common case) are more energy efficient with older processes [87]. Fig. 19 shows typical processor energy numbers at technology nodes from 0.25 μm to 65 nm. For a clock period of 40 F04 delays and an active versus standby mode duty cycle of 0.01, the lowest energy per operation is achieved with 0.18-μm CMOS. Delay variation is highly dependent on the difference between the device V_{TH} and selected V_{DD} for a process. Newer process

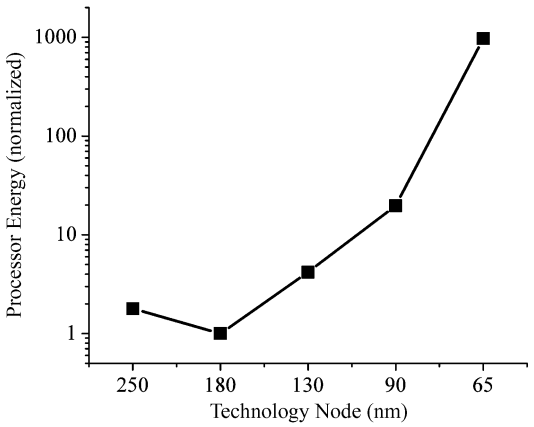

Fig. 19. *Normalized processor energies with a clock period of 40 FO4 delays and an active versus standby mode duty cycle of 0.01 [87].*

technologies have higher minimum-energy supply voltages (V_{MIN}) since the circuits have a higher ratio of leakage to dynamic energy. At the same time, V_{TH} is being scaled down slowly with each new technology generation. Thus, circuits operating at V_{MIN} will experience less delay variation in newer processes than older nodes.

Apart from intelligent selection of process node, CMOS processes can be optimized specifically for subthreshold or near-threshold operation. A key factor in subthreshold CMOS devices is the subthreshold swing (S_S). The S_S measures the decrease in gate voltage needed to reduce drain current by $10\times$ in the subthreshold region. Smaller S_S leads to higher on-to-off current ratios, lower device leakage, and greater functional robustness. The ratio of device length (L_{EFF}) to oxide thickness (t_{OX}) and the device doping profile largely determine S_S and can be optimized for low-voltage operation, at the possible expense of higher voltage performance. For standard superthreshold CMOS, L_{EFF} scales with each process generation to increase device speed and density. Recently, t_{OX} has not scaled down as rapidly because of gate tunneling leakage limitations. However, for subthreshold devices, L_{EFF} has a weaker impact on performance, and S_S can be reduced as the ratio of L_{EFF} to t_{OX} increases. While increasing L_{EFF} improves S_S and leakage power, it increases gate capacitance and dynamic power. An L_{EFF} for a low-voltage-optimized technology node can be chosen where overall energy is minimized [88].

In conventional superthreshold CMOS processes, nonuniform doping profiles are used, including so-called halo implants at the edges of the channel, to reduce the effect of drain-induced barrier lowering (DIBL). DIBL reduces the device V_{TH} for large drain to source voltages (V_{DS}) due to modulation of the source-to-channel energy barrier by the drain depletion region. For subthreshold operation, DIBL is not a large factor since V_{DS} is low. This allows for the removal of halo implants, which improves S_S and overall subthreshold device performance [89].

B. Antenna Miniaturization

Volume constraints on a sensor node limit the size of antennas in the system. This is problematic because with small antennas low-frequency radios suffer from poor transmission distances due to low antenna efficiencies, whereas high-frequency signals require high-bandwidth, high-power circuits. Passive 900-MHz ultrahigh-frequency (UHF) RFID tags can be read up to 9.25 m away while scavenging 16.7 μW of RF power [59]. However, while the antennas in these systems are smaller than in lower frequency RFID tags, they are still several centimeters in each dimension. Thus, for millimeter-scale antennas, efficient radios require frequencies of several gigahertz. In addition, the RFID readers are complex high-power devices. To communicate with other sensors in a homogeneous network, either power requirements increase or transmission distances decrease. Since mandates limit the maximum possible transmitted power, longer distance communication relies on more efficient use of this power. Designing a low-power miniature transmitter that is capable of communicating with other sensor nodes at a distance of tens of meters or more remains a design challenge for future wireless sensor networks.

C. Peer-to-Peer Communication

UWB and passive RF circuits are presented in Section V for low-power wireless communication. However, each of these techniques relies on an asymmetric communication scheme with simple low-power transmitters and complex and power-hungry receivers. This makes peer-to-peer communication, where each sensor has a transmitter and a receiver, difficult. Narrowband signals are easier to receive, but require higher power to transmit.

UWB signals have a wide frequency spectrum, which it shares with other wireless protocols. Since the frequencies are shared, the Federal Communications Commission (FCC) regulates the transmitted power to be low, as to not interfere with other communications. UWB receivers commonly amplify the signal, mix it down to baseband, and perform energy detection to demodulate the transmitted data. UWB LNAs must be wideband amplifiers, whereas wireless communication schemes that send a tone can use narrowband amplifiers. For a given technology, the gain bandwidth product at a given energy level is roughly constant. Thus, wideband LNAs are more power hungry than narrowband LNAs for the same gain. In addition, the energy detection circuit integrates the noise, as well as the signal energy over the wide frequency band. This is contrasted with narrowband schemes, where noise that is not at the tonal frequency can be filtered out. The integrated noise and low transmitted power create SNR challenges for UWB receivers.

Backscattered RFID signals are difficult to receive because of low signal power and signal interference. A transmitter, or RFID reader, transmits power to the RFID sensor. The sensor then modulates its antenna impedance to modulate its reflected signal, which the RFID reader detects. The backscattered signal is weak, since it is not actively driven by the sensor itself. In addition, interference between the transmitted and backscattered signals creates signal integrity issues. Both of these limitations necessitate that the backscattering RFID receiver have high SNR, which increases power demands.

Narrowband signals are easier to receive, but require more energy to transmit. Since narrowband signals do not share a frequency spectrum with other wireless protocols, its FCC regulated transmission power is higher. In addition, narrowband LNAs can be used, and noise that is not at the tonal frequency can be filtered out. However, generating higher transmission powers requires higher transmitter power. This power is primarily consumed by the power amplifier that drives the antenna.

D. Sensor Synchronization

Data collected from a network of wireless sensors are aggregated to form a larger picture of the environment covered by the devices. In order to form a clear picture of the overall environment, many wireless protocols require each sensor node to be synchronized with all other nodes in the network [90]. Complete synchronization allows data from sensors to be forwarded toward a central base station through other sensor nodes in an *ad hoc* fashion. Although each sensor node is equipped with a timer that nominally has the same frequency as other nodes in the network, time differences are accumulated if there is no communication between the sensor nodes. Timers for synchronization are constantly running and must be extremely low power. Today, typical sensors use quartz crystals to provide a stable frequency reference, but do not fall into the power or size budget for a millimeter-scaled device. The low-power timers, such as those discussed in Section VII, are highly susceptible to cycle-to-cycle time variations, called jitter. This necessitates more frequent wireless synchronization broadcasts, in the process consuming large amounts of energy. RF-MEMS devices, such as BAW and FBAR resonators, provide a lower power reference, with frequency stability that rivals quartz crystals. To date, these frequency references have been implemented in separate dedicated process flows. This increases the cost of integrating and packaging these devices with CMOS circuits. Miniature wireless sensors will require either low-power low-jitter timers or network protocols that relax synchronization requirements.

IX. CONCLUSION

To create miniature wireless sensors with long lifetimes, the system architecture and all circuit components must be completely reconsidered for ultralow-power operation. Recent low-power circuit and system design advances, along with techniques in development, make devices for new applications possible, such as IOP sensing. IOP sensing is representative of emerging volume-constrained sensing applications with aggressive power budgets, asymmetric communication requirements, and low duty cycles. The combination of these factors brings both challenges and opportunities to circuit and system designers. Looking ahead, continued progress in energy harvesting, power management circuits, and wireless communication represent particularly exciting areas of research in this field. In summary, myriad sensor applications have similar use models to the IOP device of the introduction, collectively pointing to the need for millimeter-scale systems to replace today's bulky, expensive, and power-hungry wireless sensors. These miniaturized sensors offer end users the promise of a wealth of environmental data and open the door to truly ubiquitous wireless sensing. ■

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