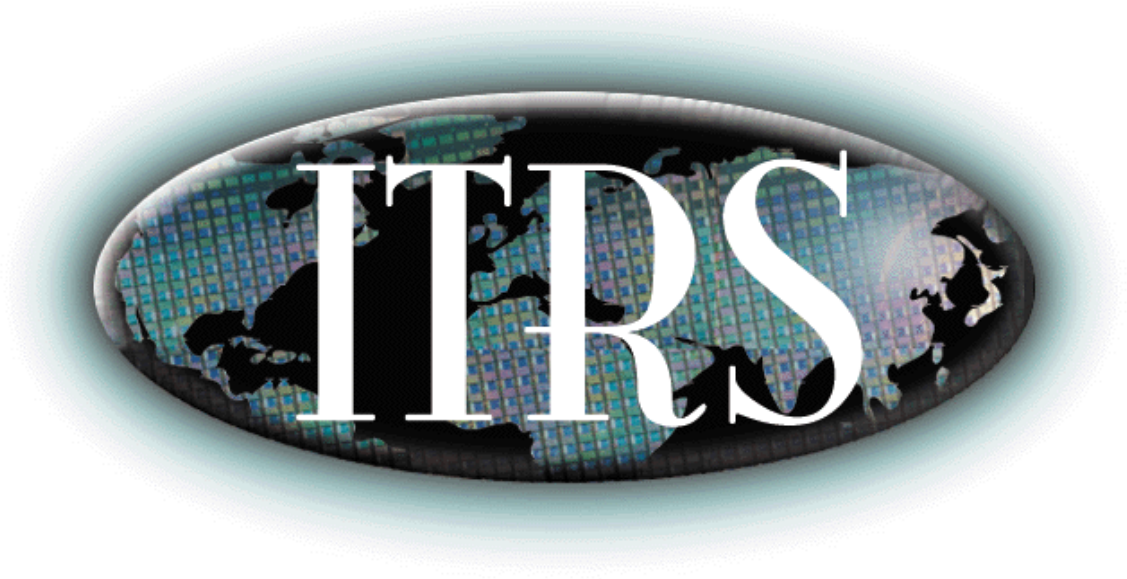

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2013 EDITION

EMERGING RESEARCH DEVICES SUMMARY

THE ITRS IS DEVISED AND INTENDED FOR TECHNOLOGY ASSESSMENT ONLY AND IS WITHOUT REGARD TO ANY COMMERCIAL CONSIDERATIONS PERTAINING TO INDIVIDUAL PRODUCTS OR EQUIPMENT.

EMERGING RESEARCH DEVICES SUMMARY

Continued dimensional and functional scaling[1] of CMOS is driving information processing[2] technology into a broadening spectrum of new applications. Many of these applications are enabled by performance gains and/or increased complexity realized by scaling. Because dimensional scaling of CMOS eventually will approach fundamental limits, several new alternative information processing devices and microarchitectures for existing or new functions are being explored to sustain the historical integrated circuit scaling cadence and reduction of cost/function into future decades. This is driving interest in new devices for information processing and memory, new technologies for heterogeneous integration of multiple functions (a.k.a. "More than Moore"), and new paradigms for system architecture. This chapter, therefore, provides an ITRS perspective on emerging research device technologies and serves as a bridge between CMOS and the realm of nanoelectronics beyond the end of CMOS dimensional and equivalent functional scaling. (Material challenges related to emerging research devices are addressed in a complementary chapter entitled *Emerging Research Materials*.)

An overarching goal of this chapter is to survey, assess and catalog viable new information processing devices and system architectures for their long-range potential, technological maturity, and to identify the scientific/technological challenges gating their acceptance by the semiconductor industry as having acceptable risk for further development. Another goal is to pursue long term alternative solutions to technologies addressed in More-than-Moore (MtM) ITRS entries.

This is accomplished by addressing two technology-defining domains: 1) extending the functionality of the CMOS platform via heterogeneous integration of new technologies, and 2) stimulating invention of a new information processing paradigm. The relationship between these domains is schematically illustrated in Figure ERD1. The expansion of the CMOS platform by conventional dimensional and functional scaling is often called "More Moore". The CMOS platform can be further extended by the "More-than-Moore" approach which was first introduced into ERD chapter in 2011. On the other hand, new information processing devices and architectures are often called "Beyond CMOS" technologies and have been the main subjects of this chapter. The heterogeneous integration of "Beyond CMOS", as well as "More-than-Moore", into "More Moore" will extend the CMOS platform functionality to form ultimate "Extended CMOS".

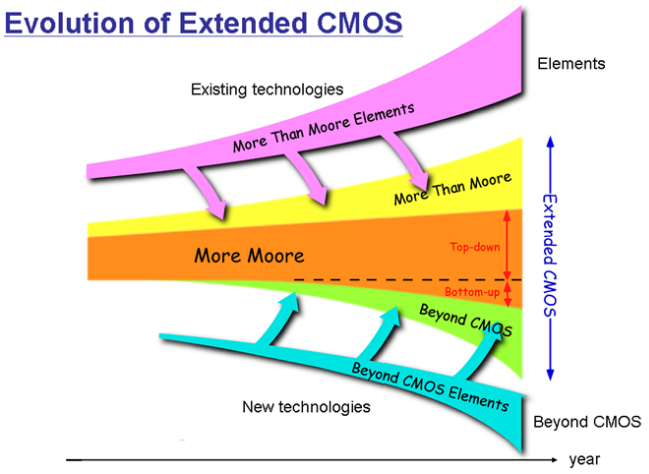

Figure ERD1 Relationship among More Moore, More-than-Moore, and Beyond CMOS (Courtesy of Japan ERD)

The chapter is intended to provide an objective, informative resource for the constituent nanoelectronics communities pursuing: 1) research, 2) tool development, 3) funding support, and 4) investment, each directed to developing a new information processing technology. These communities include universities, research institutes, and industrial research

[1] *Functional Scaling: Suppose that a system has been realized to execute a specific function in a given, currently available, technology. We say that system has been functionally scaled if the system is realized in an alternate technology such that it performs the identical function as the original system and offers improvements in at least one of size, power, speed, or cost, and does not degrade in any of the other metrics.*

[2] *Information processing refers to the input, transmission, storage, manipulation or processing, and output of data. The scope of the ERD Chapter is restricted to data or information manipulation, transmission, and storage.*

laboratories; tool suppliers; research funding agencies; and the semiconductor industry. The potential and maturity of each emerging research device and architecture technology are reviewed and assessed to identify the most important scientific and technological challenges that must be overcome for a candidate device or architecture to become a viable approach.

The chapter is divided into five sections: 1) memory devices, 2) information processing or logic devices, 3) More-than-Moore device technologies, 4) emerging research information processing architectures, and 5) a critical assessment of each technology entry. Some detail is provided for each entry regarding operation principles, advantages, technical challenges, maturity, and current and projected performance. Also included is a device and architectural focus combining emerging research devices offering specialized, unique functions as heterogeneous core processors integrated with a CMOS platform technology. This represents the nearer term focus of the chapter, with the longer term focus remaining on discovery of an alternate information processing technology to eventually replace digital CMOS.

The memory device section is expanded to include a new technology entry: carbon-based memory. With growing research activities in ReRAM, a separate table is created for this technology entry to track different types/mechanisms. The logic device section is organized based on state variables and novelty of materials/structures. The "More-than-Moore" section introduces new discussions on devices with learning capabilities and continues covering emerging devices for RF applications. Finally, the critical assessment section continues to cover a survey-based benchmark and quantitative benchmarks reported in literature to provide a balanced assessment of these emerging new device technologies. A brief section is also included to propose a set of fundamental principles that will likely govern successful extension of information processing technology substantially beyond that attainable solely with ultimately scaled CMOS.

This chapter continues the technology highlights: (1) "Carbon-based Nanoelectronics" as a rapidly emerging information processing technology; (2) Spin Transfer Torque Magnetostatic RAM (STT-MRAM) and Redox Resistive RAM as rapidly emerging memory technologies. These three technologies exhibit substantial potential such that they will likely be ready for manufacture within a five – ten year period. Highlighting also suggests that a technology is an attractive candidate for accelerated development.

As in previous editions, the chapter includes "transition tables." The purpose of these transition tables is twofold. The first is to track technologies that have appeared in or have been removed from the 2013 tables and so provide a very brief explanation of the reason for this change. The second is to identify technologies that are considered important but do not meet the criteria for full inclusion into the more detailed tables. These may be expected to become more or less visible in future editions of the roadmap and hence the name.

DIFFICULT CHALLENGES

The semiconductor industry is facing three classes of difficult challenges related to extending integrated circuit technology to new applications and to beyond the end of CMOS dimensional scaling. One class relates to propelling CMOS beyond its ultimate density and functionality by integrating a new high-speed, high-dense, and low-power memory technology onto the CMOS platform. Another class is to extend information processing substantially beyond that attainable by CMOS using an innovative combination of new devices, interconnect and architectural approaches for extending CMOS and eventually inventing a new information processing platform technology. The third class is to invent and reduce to practice long term alternative solutions to technologies that address existing MtM ITRS topical entries currently in wireless and eventually in power devices, image sensors, *etc*. These difficult challenges, all addressing the long term period of 2018 – 2026, are presented in Table ERD1.

Table ERD1 Emerging Research Devices Difficult Challenges

Difficult Challenges – 2018– 2026	*Summary of Issues and opportunities*
Scale high-speed, dense, embeddable, volatile/nonvolatile memory technologies to replace SRAM and possibly FLASH for manufacture by 2018.	SRAM and FLASH scaling in 2D will reach definite limits within the next several years (see PIDS Difficult Challenges). These limits are driving the need for new memory technologies to replace SRAM and possibly FLASH memories by 2018. Identify the most promising technical approach(es) to obtain electrically accessible, high-speed, high-density, low-power, (preferably) embeddable volatile and nonvolatile memories. The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing. Reliability issues should be identified & addressed early in the technology development.
Scale CMOS to and beyond 2018 - 2026	Develop 2nd generation new materials to replace silicon (or InGaAs, Ge) as an alternate channel and source/drain to increase the saturation velocity and to further reduce V_{dd} and power dissipation in MOSFETs while minimizing leakage currents for technology scaled to 2018 and beyond. Develop means to control the variability of critical dimensions and statistical distributions (e.g., gate length, channel thickness, S/D doping concentrations, etc.) Accommodate the heterogeneous integration of dissimilar materials. The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing Reliability issues should be identified & addressed early in this development.
Extend ultimately scaled CMOS as a platform technology into new domains of application.	Discover and reduce to practice new device technologies and primitive-level architecture to provide special purpose optimized functional cores (e.g., accelerator functions) heterogeneously integrable with CMOS.
Continue functional scaling of information processing technology substantially beyond that attainable by ultimately scaled CMOS.	Invent and reduce to practice a new information processing technology eventually to replace CMOS. Ensure that a new information processing technology has compatible memory technologies and interconnect solutions. A new information processing technology must be compatible with a system architecture that can fully utilize the new device. Non-binary data representations or non-Boolean logic may be required to employ a new device for information processing, which will drive the need for new system architectures. Bridge the gap that exists between materials behaviors and device functions. Accommodate the heterogeneous integration of dissimilar materials. Reliability issues should be identified & addressed early in the technology development.
Invent and reduce to practice long term alternative solutions to technologies that address existing MtM ITRS topical entries currently in wireless/analog and eventually in power devices, MEMS, image sensors, etc.	The industry is now faced with the increasing importance of a new trend, “More than Moore” (MtM), where added value to devices is provided by incorporating functionalities that do not necessarily scale according to "Moore's Law“. Heterogeneous integration of digital *and* non-digital functionalities into compact systems that will be the key driver for a wide variety of application fields, such as communication, automotive, environmental control, healthcare, security and entertainment.

DEVICE TECHNOLOGIES

Difficult challenges gating development of emerging research devices are divided into three parts: those related to memory technologies, those related to information processing or logic devices, and those related to heterogeneous integration of multi-functional components, a.k.a. More-than-Moore (MtM) or Functional Diversification. (Refer to Table ERD1.)

One challenge is the need of a new memory technology that combines the best features of current memories in a fabrication technology compatible with CMOS process flow scaled beyond the present limits of SRAM and FLASH. This would provide a memory device fabrication technology required for both stand-alone and embedded memory applications. The ability of an MPU to execute programs is limited by interaction between the processor and the memory, and scaling does not automatically solve this problem. The current evolutionary solution is to increase MPU cache

memory, thereby increasing the floor space that SRAM occupies on an MPU chip. This trend eventually leads to a decrease of the net information throughput. In addition to auxiliary circuitry to maintain stored data, volatility of semiconductor memory requires external storage media with slow access (e.g., magnetic hard drives, optical CD, etc.). Therefore, development of electrically accessible non-volatile memory with high speed and high density would initiate a revolution in computer architecture. This development would provide a significant increase in information throughput beyond the traditional benefits of scaling when fully realized for nanoscale CMOS devices.

A related challenge is to sustain scaling of CMOS logic technology beyond 2018. One approach to continuing performance gains as CMOS scaling matures in the next decade is to replace the strained silicon MOSFET channel (and the source/drain) with an alternate material offering a higher potential quasi-ballistic-carrier velocity and higher mobility than strained silicon. Candidate materials include strained Ge, SiGe, a variety of III-V compound semiconductors, and graphene. Introduction of non-silicon materials into the channel and source/drain regions of an otherwise silicon MOSFET (i.e., onto a silicon substrate) is fraught with several very difficult challenges. These challenges include heterogeneous fabrication of high-quality (i.e., defect free) channel and source/drain materials on non-lattice matched silicon, minimization of band-to-band tunneling in narrow bandgap channel materials, elimination of Fermi level pinning in the channel/gate dielectric interface, and fabrication of high-κ gate dielectrics on the passivated channel materials. Additional challenges are to sustain the required reduction in leakage currents and power dissipation in these ultimately scaled CMOS gates and to introduce these new materials into the MOSFET while simultaneously minimizing the increasing variations in critical dimensions and statistical fluctuations in the channel (source/drain) doping concentrations.

The industry is now addressing the increasing importance of a new trend, “More than Moore” (MtM), where added value to devices is provided by incorporating functionalities that do not necessarily scale according to "Moore's Law“. A MtM section was first introduced into the ERD chapter in 2011 with the initial coverage on wireless technologies. This version expands the coverage to devices with learning capabilities. Traditionally, the ITRS has taken a “technology push” approach for roadmapping “More Moore”, assuming the validity of Moore’s law. In the absence of such a law, different methodologies are needed to identify and guide roadmap efforts in the MtM-domain.

A longer-term challenge is invention and reduction to practice of a manufacturable information processing technology addressing “beyond CMOS” applications. For example, emerging research devices might be used to realize special purpose processor cores that could be integrated with multiple CMOS CPU cores to obtain performance advantages. These new special purpose cores may provide a particular system function much more efficiently than a digital CMOS block, or they may offer a uniquely new function not available in a CMOS-based approach. Solutions to this challenge beyond the end of CMOS scaling may also lead to new opportunities for such an emerging research device technology to eventually replace the CMOS gate as a new information processing primitive element. A new information processing technology must also be compatible with a system architecture that can fully utilize the new device. A non-binary data representation and non-Boolean logic may be required to employ a new device for information processing. These requirements will drive the need for new system architectures.

MATERIALS TECHNOLOGIES

The most difficult challenge for Emerging Research Materials is to deliver materials with controlled properties that will enable operation of emerging research devices in high density at the nanometer scale. To improve control of material properties for high density devices, research on materials synthesis must be integrated with work on new and improved metrology and modeling. These important objectives are addressed in the companion chapter entitled Emerging Research Materials.

PROCESSING

In considering the many disparate new approaches proposed to provide order of magnitude scaling of information processing beyond that attainable with ultimately scaled CMOS, the Emerging Research Devices Working Group proposes the following comprehensive set of guiding principles. We believe these “Guiding Principles” provide a useful structure for directing research on any “Beyond CMOS” information processing technology to dramatically enhance scaling of functional density and performance while simultaneously reducing the energy dissipated per functional operation. Further this new technology would need to be realizable using a highly manufacturable fabrication process.

GRAND CHALLENGES

COMPUTATIONAL STATE VARIABLE(S) OTHER THAN SOLELY ELECTRON CHARGE

These include spin, phase, multipole orientation, mechanical position, polarity, orbital symmetry, magnetic flux quanta, molecular configuration, and other quantum states. The estimated performance comparison of alternative state variable devices to ultimately scaled CMOS should be made as early in a program as possible to down-select and identify key trade-offs.

NON-THERMAL EQUILIBRIUM SYSTEMS

These are systems that are out of equilibrium with the ambient thermal environment for some period of their operation, thereby reducing the perturbations of stored information energy in the system caused by thermal interactions with the environment. The purpose is to allow lower energy computational processing while maintaining information integrity.

NOVEL ENERGY TRANSFER INTERACTIONS

These interactions would provide the interconnect function between communicating information processing elements. Energy transfer mechanisms for device interconnection could be based on short range interactions, including, for example, quantum exchange and double exchange interactions, electron hopping, Förster coupling (dipole–dipole coupling), tunneling and coherent phonons.

NANOSCALE THERMAL MANAGEMENT

This could be accomplished by manipulating lattice phonons for constructive energy transport and heat removal.

SUB-LITHOGRAPHIC MANUFACTURING PROCESS

One example of this principle is directed self-assembly of complex structures composed of nanoscale building blocks. These self-assembly approaches should address non-regular, hierarchically organized structures, be tied to specific device ideas, and be consistent with high volume manufacturing processes.

ALTERNATIVE ARCHITECTURES

In this case, architecture is the functional arrangement on a single chip of interconnected devices that includes embedded computational components. These architectures could utilize, for special purposes, novel devices other than CMOS to perform unique functions.