3D Integration: A Progress Report

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PURPOSE

This report was created to help accelerate the adoption of 3D integration using TSV interconnect technology by identifying the crucial barriers preventing widespread acceptance. It offers a comprehensive snapshot of the progress made thus far, while also shining a light on what is left to be addressed before first market adoption, and then volume production can be achieved.

EXECUTIVE SUMMARY

3D integration schemes can be classified by their level of interconnect hierarchy at the global (package), intermediate (bond pad) and local (transistor) level. While schemes at the global level have been in production for some time using traditional methods of interconnect such as wire bond and flip chip, the next-generation of 3D integration proposes to incorporate through-silicon via (TSV) technology as the primary method of interconnect.

The drivers for market adoption of 3D ICs with TSVs are increased performance, reduced form factor, and cost reduction. Additionally, achieving true heterogeneous integration at the local level will require a high-density TSV solution.

Critical areas in the TSV formation and subsequent stacking processes include those that address insulator/ barrier/seed, plating/stripping etching, thin wafer handling for permanent and temporary bond/debond process, and pick-and-place stacking.

Additionally, limitations to market adoption of 3D integration using TSVs have been identified as a lack of design tools, thermal management issues, test solutions, and supply chain issues.

The successful achievement of all of these technologies relies on collaboration and participation across the supply chain. There is a call for more communication and information sharing between the design, test, and manufacturing communities to accelerate the march towards market adoption. To this end, a variety of consortia, collaborations, joint development projects ad multi-project wafers have been formed to promote development of 3D integration.

Standards, while necessary for volume production, will most likely follow initial market adoption, as processes of record are determined.

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Eric Beyne, IMEC; Sitaram Arkalgud, SEMATECH; Nicholas Sillon, CEA-LÉTI; Jerome Baron, Yole Developpement; E.Jan Vardaman, TechSearch, International; Lisa McIlrath, R3Logic; Bob Patti; Tezzaron Semconductor; Bill Bottoms, Nanonexus; Ritwik Chatterjee, Georgia Tech; Lee Smith, Amkor; Ho-Ming Tong and Daniel Yang, ASE; Flynn Carson, STATS ChipPAC; David Wang, ChipMos.

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SUPPORTED BY:

INTRODUCTION

Developments in processes and technologies in 3D integration, as well as industry-wide acknowledgement that these technologies are anticipated to be pivotal for future growth of the semiconductor industry, has accelerated interest in market adoption over the past few years. Countless initiatives have been established involving both industry and academia in pursuing this "Holy Grail", with full-scale involvement reaching across the supply chain.

Therefore, for the purposes of this report, we canvassed the supply chain, from those involved in R&D through final manufacturing. While not all those contacted were able to participate, those who did are also most deeply involved in bringing these technologies to market.

CLASSIFYING 3D INTEGRATION CONFIGURATIONS

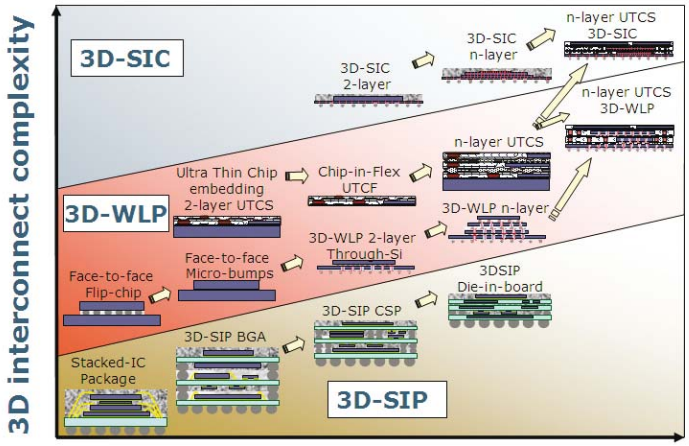
As 3D integration technologies have emerged over the years, there has been some confusion in the classification and terminology. To address this, organizations such as the Jisso International Council (JIC) and the International Technology Roadmap for Semiconductors (ITRS) have worked to classify these to further the establishment of standards and roadmaps of 3D integration.

The Jisso International Council is made up of key technologists from various industry leading companies comprising three regional councils, Jisso Japan Council (JJC), Jisso European Council (JEC) and Jisso North America Council (JNAC). The organization recently concluded their 10th annual meeting, which focused on ongoing efforts to harmonize standardization and industry terminology for electronic interconnections. Cooperatively, the council has reached agreement on key terminology that helps to facilitate better understanding in an increasingly global electronics environment.

As such, based on interconnect wiring hierarchy and the industrial infrastructure set forth by JIC , IMEC Research Institute has classified the levels of 3D integration as follows:

3D system-in-package (3D-SIP)

3D-SiP can be classified as 3D integration based on traditional packaging interconnect technologies at higher levels of packaging interconnect hierarchy such as wire-bond die stacks (level 2) and package-on-package (PoP) stacking (level 3). [1]



IMEC's roadmap for 3D Technology (Courtesy of IMEC)

This category of 3D integration has already reached volume production, and inroads continue to be made in advancing these technologies. It relies on established infrastructure, and is driven by a need for increased functionality in a smaller form factor at low cost. A recent example of new technologies of this kind would be Amkor's through-mold via package-on-pacakge (TMV POP) which incorporates a through-mold via as a 3rd level package-to-package interconnect.

3D wafer-level-packaging (3D-WLP)

3D-WLP is classified as integration technology that is based on wafer-level-packaging (WLP) infrastructure and technology, such as redistribution and flip-chip bumping. The 3D interconnects are processed at the wafer level, using a post-IC-passivation process, and correspond to interconnects at the bond-pad level (Jisso level 1). [2]

According to Eric Beyne, director of Advanced Packaging Research at IMEC, this involves post-fab (post IC passivation) connections between die with 'regular' I/O drivers, ESD protection, and bond pad sizes/pitches.

Therefore, it corresponds to the industrial WLP supply chain, using typical WLP tools and processes, as used for redistribution wiring and bumping. Fan-in flip-chip and CSP technologies are categorized here, in addition to the recently developed fan-out wafer-level CSP class, such as Freescale's redistributed chip package (RCP), Infineon's eWLB (developed collaboratively with ST Micoelectronics and STATS ChipPAC,) and IMEC's ultra-thin chip package (UTCP).

These 3D interconnects can also be realized using either "via-last" through silicon vias (TSVs) or some alternate through-package-via. It's important to note that TSV is not only reserved for 3D IC stacking processes, but also functions as a method of interconnect for other technologies such as MEMS, CIS, silicon interposers, and compound semiconductors.

3D stacked-IC (3D-SIC)

3D-SIC is classified as 3D integration using wafer-fab technology (Jisso level 0) for realizing 3D interconnects at the global or intermediate levels of on-chip wiring hierarchy, as set forth by the ITRS. The 3D interconnects connect large circuits blocks on different 2D planes; containing 2D blocks with multiple layers of interconnect metallization layers. [3]

Beyne explains that this category refers to applications where large circuit blocks (i.e.: tiles, IP-blocks, memory–banks) are stacked, rather than final ICs. It is similar to a 2D system-on-chip (SOC) approach, except that circuits exist physically on different layers. Interconnects are typically at the level of the 'global-interconnect' circuitry on-chip.

3D I/O connections do not have big drivers and large ESD protection circuits typical for a finalized IC. This allows the 3D interconnects to function fast with low power consumption but requires adopted strategies for testing and assembly. Applications for this approach include heterogeneous technology stacks and high bandwidth memory on logic stacks.

True 3D-IC

The Holy Grail of 3D integration, the 3D IC is more a monolithic super die than a super package. Classified as using wafer-fab technology (Jisso level 0) for realizing 3D interconnects at the local levels of the on-chip wiring hierarchy as set forth by the ITRS, this results in direct vertical interconnects between device layers and in a common 2D interconnect metallization stack. [4]

Beyne explains that 'at the local interconnect level' refers to stacking of transistor layers, rather than die, and implies the use of TSV technology of the same density as contact technology to the individual transistors.

Currently, Beyne says, no wafer bonder can align wafers with processed transistors or memory cells at that deep sub-micron level. Therefore, to use this technology, the transistors of a second tier die have to be processed on the already processed bottom transistor layer. The difficulty here is processing the second tier so as not to alter or destroy the bottom tier devices. Nevertheless, this technology is of interest and has been around for at least 25 years (Koyanagi of Tohoku University was one of the pioneers). Recent developments, such as ultra-short pulsed lasers for local heating (re-crystallization and annealing) have revived this area. It is mainly a front-end integration technique.

The final device consists of a stack of front-end-of-line (FEOL) layers with a single back-end-of-line (BEOL) interconnect stack (in 3D-SIC, the stack alternates both FEOL and BEOL.)

Beyne says the "killer" application for this technology is memory stacks : one layer with line and word 'pass'-transistors, other layer(s) with the actual memory element(s) (transistors, C, R.)

"Stacking a memory in two layers would give an area scaling similar to two nodes of standard scaling, although at an increased cost," says Beyne.

While all of the above configurations exist at the R&D level, they are all at different stages of development. The next section of this paper addresses market adoption and industry roadmaps for achieving this.

MARKET ADOPTION OF 3D CONFIGURATIONS AND ROADMAPS

Defining Market Adoption

It is important to note that while some timelines may be more aggressive than others may, it partly has to do with defining "market adoption." Whilst the market may have identified a need to adopt TSV technology, taking the technology from viability through the established process of prototype development, product qualification and manufacturability at production levels is a lengthy process. Some equipment manufacturers indicated that realistically, this could push the predicted dates out 1-2 years.

There is general consensus that when it comes to TSV as a method of interconnect, it's a matter of when and not if. There is also consensus that as with most packaging technologies, it is unlikely that there will be a one-size-fits all solution to processes and approaches currently being developed. Rather, there will be application specific solutions involving the participation of the entire supply chain.

As previously mentioned, some configurations, such as 3D SIP in the form of PoP, have already been adopted and reached volume production. Others that rely on TSV as a method of interconnect, such as 3D WLP, have reached market adoption and volume production in niche applications, such as CMOS image sensors (CIS).

3D WLP

Both Beyne and Jerome Baron, of Yole Developpement note that 3D WLP using TSV as a method of interconnect has already been adopted for backside-contacted CIS, and for Si interposer substrates. According to E. Jan Vardaman, CEO of TechSearch International, almost every global research institute has a program to develop silicon interposers with TSV. Prototypes have been demonstrated by companies including IPDIA (formerly NXP's Caen operation), IBM, NEC, and Shinko Electric.

Micron and Samsung reportedly have demonstrated DRAM stacks connected at the I/O pads using TSV stacking, but this is not considered "fully integrated" as if they were a 3D SIC.

According to Baron, Yole's market research indicates that the 3D WLP infrastructure is ready for volume production in such MEMS foundries as Silex, Dalsa, TMT, IMT and foundries such as Xintec, TSMC and Nemotec. He says the next step this year will be availability of fan-out WLP such as RCP and eWLB as ASE and STATS ChipPAC go into volume production.

3D SIC

There are some slight differences in opinion between IMEC and Yole regarding the 3D SIC timeline. Beyne says that DRAM memory and logic-on-memory requirements will bring market adoption in the 2011-2012 timeframe.

While Baron agrees that the first "genuine" 3DIC product will be arriving in the 2011-2012 timeframe, and has already appeared in the wireless SiP market, it is coming slowly. For homogenous stacks, Baron says cost of ownership needs further reduction to enable broad adoption of TSV in the cost-driven memory market. But he says a portion of the industry is working hard on this, so expect full market adoption to become viable in the 2012-2013 time frame.

3D IC

Beyne predicts that true 3D IC for memory will come when 2D possibilities "run out of steam" targeting 2020 as the timeframe for that.

IDENTIFYING THE ROADBLOCKS

Global Economy

One question is whether the state of the economy and its effect on the semiconductor industry as a whole will slow down the projected timelines. While acknowledging that some projects are experiencing delays, Beyne says others are seeing it as an opportunity to prepare for the future.

Bill Bottoms, of Nanonexus, says while current economic conditions may slightly affect the expected projected dates for market adoption, more importantly, technology bottlenecks and limitations such as the lack of design tools, methodologies, thermal management solutions, supply chain issues and test strategies will all affect the timeline if they are not addressed.

Baron reports that although 'cost sensitive' applications seem to have been delayed in the roadmap, logic and logic+memory 3D ICs are coming more quickly than expected. Moreover, Yole's research shows that despite a worldwide economic recession, the R&D activity linked to 3-D companies has reached "unprecedented levels". Therefore, Yole predicts that the industry will come out of the recession by "stimulating innovations they have 'in their box'. "We clearly see 3-D integration by mean of TSV interconnects or embedded WLP technologies leading the way," states Baron.

Cost Considerations

Beyne says that not just the cost of TSV formation, but rather the full picture of the 3D-process has to be considered when looking into the cost model: there is a cost for the TSV process itself, for wafer thinning and backside processing; stacking the die; and the cost for packaging the die stack. Many cost models only consider the first part.

Additionally, current cost models focus on the unit processes themselves, overlooking the opportunity to reduce costs by optimizing between the processes.
Then, there is the cost associated with the compound yield problem: die yield, stacking yield, and impact of KGD testing. This deters the bulk of applications from wafer-to-wafer (W2W) stacking.

However, the impact of "clever design" may significantly overrule added 3D technology costs. According to Beyne, repartitioning the system may result in cheaper overall Si cost: lower Si-area, cheaper Si processes (e.g.: less interconnect layers in the BEOL) or lower cost technology nodes.

According to Vardaman, the availability of lower cost, alternative technologies such as Vertical Circuits' vertical interconnect pillar (VIP) and 3D Plus' wireless die-on-die technology (WDoD) may also affect market adoption for certain applications.

VPI was developed as an alternative to both wire bond and TSV, overcoming scaling limitations of the former (up to 100 die have reportedly been proven) and design and cost limitations of the latter. The process flow begins with standard die in wafer form. Die pads are re-routed to the periphery, and the die goes through an insulation process. The wafer is then thinned and die are singulated. Next the die are stacked and laminated together with an adhesive. Finally, conductors are jet dispensed on the edge of the die stack using Asymtek's high-speed, high-accuracy jetting technology. The process involves existing equipment, and can be integrated into any existing back-end assembly line. Target applications include memory modules, embedded memory, and system-in-package. VPI has reportedly been licensed some IDMs and OSATs.

The WDoD is based on using a 'known rebuilt good wafer' (KRGW) with edge connection and through polymer via (TPV). The process also begins with standard die, which are pick-and-placed on a sticky membrane to build the KRGW. These rebuilt wafers are stacked without TSVs using a double adhesive. The stack is then diced. The dicing streets are collectively electroless plated along the edges, which are then laser patterned and electrically tested. The main applications for this technology are SiP for smart cards, mobile phones and flash memory.

Technology Limitations

Beyne says he does not consider design tools and thermal management bottlenecks for 3D technology adoption. Rather he identifies the "main bottlenecks" as follows:

- Some of the process tools used are only offered by a limited number of vendors and are new to the IC-fabs and/or OSATs.
- The supply chain: Are OSATS ready to handle post-fab processes or will fabs install that capability? Additionally, how will wafers from different suppliers be combined into one product and address "typical business issues," such as those that occurred with PoP vs. wire bond stacking.
- Added value of TSVs must be high enough. If purely cost driven, TSVs are a cost adder and not required. One example is the stacking of NAND flash where TSVs face difficult economics.

Baron concurs, and says that Yole sees the supply chain as the biggest immediate issue, especially for 3D SICs and memory+logic 3D IC applications. The infrastructure must be available first for the fast adoption of these 3D ICs into the market place.

Additionally, Baron cites thermal management as the most serious barrier with the potential of reducing the 3D IC product application window. He identified design, test and software as "second order issue" that will be solved as market adoption draws closer. "Don't under estimate the capabilities of IDMs, design and test industries to rapidly overcome these issues," he states. Vardaman says that while there has been a lot of work on thermal issues, additional work is needed in design and test.

Nicolas Sillon of CEA-Léti points out that the hold-up is not technology. Everyone is advancing in parallel. Léti sees the main roadblocks as design tools and supply chain issues. Additionally, while equipment exists for development purposes in the R&D setting, tools for volume production don't exist yet for some of the critical steps. For example, there is still yet to be a pick-and-place tool that can also achieve alignment specifications at the throughput necessary for volume production.

Roadmaps

Sitaram Arkalgud, director of SEMATECH's 3D Interconnect Program, stresses the need for an updated industry roadmap to address the adoption of 3D integration process. SEMATECH works off the IRTS roadmap, which has been a challenge, because up until 3 years ago, there was nothing included about 3D IC integration. In 2007, the issue was addressed, and according to Bill Bottoms, the 2009 ITRS Roadmap will reflect a major revision. After it is published it should be the most complete and accurate roadmap for 3D IC integration.

TECHNOLOGY PROGRESS

This segment will review the different approaches being developed to achieve reliable 3D chip stacks at low cost. In his book, Handbook of 3D Integration: Technology and Applications of 3D Integrated Circuits, Phil Garrou identifies, 9 3D IC process variations. All involve via formation, (vias-first, -middle, or -last); thinning (on temp. carrier or 3D stack); temporary and/or permanent bonding (face up or face down).

It is expected that the industry will settle on 2 or 3 of these process variations as standard. Most suppliers polled are developing their toolsets to accommodate all of these variants. Primary considerations and discussions focus on via-first, -middle and -last processes for via formation; and wafer-to-wafer (W2W), die-to-wafer (D2W) or die-to-die (D2D) approaches for die stacking.

Via-first, via-middle or via-last

According to Arkalgud, the concept of TSV formation is straightforward. It is a question of putting the steps together in the right order. He says that true "via-first" is formed even before CMOS processes, and reports that there has not been much success with that in the industry to the cost involved. Rather, SEMATECH's

program will focus on "via-middle", which is defined as via formation between first metallization and finished high temperature CMOS processes. At SEMATECH, these vias are tungsten-filled, rather than copper, and Arkalgud considers them to be a good compromise between via-first and last.

Beyne concurs that via-middle offers the highest added value of via formation options. Baron reports that Yole's data also indicate that via-middle (also called via-first by many, which causes much confusion) is showing the most progress, but that there are still many via-last scenarios being developed and considered.

Samsung has published success with stacked NAND and stacked DRAMS using via-last processes. Additionally, for the purpose of CIS, via-last is already used in production.

Nicolas Sillon, CEA-Léti Research Institute says the organization is focusing on an integration scheme using via-last, because they think it will be easier to introduce to fab partners. Via-last can be done using existing die, and does not rely on new chip design. Sillon predicts that the first products to reach volume production will likely take a via-last approach for this reason, and that once 3D is accepted into the market, via-first will take over.

Sillon also reports that Léti's program with CIS has been transferred to ST Microelectronics for volume production on 200mm wafers, and that they are now working on qualifying the process on 300mm wafers.

The EMC3D Consortium, a supplier-base open alliance whose mission is to "rapidly develop a cost-effective and manufacturable TSV for 3D chip stacking and MEMS integration," has been working to qualify a via-first and a via-last approach. The organization claims to be successfully integrating both iTSV (via-first) and pTSV (via-last) with aspect ratios up to 10:1. The consortium partners are currently balancing equipment for a production via-first iTSV line that will offer an overall CoO of under $150/wafer. [5]

However, aside from cost considerations, there are other value considerations to examine. A via-last approach risks damaging otherwise fully assembled devices, thereby causing a bigger loss to investment than with via-first. Additionally, "ownership" and thereby liability issues ensue between fab and OSAT with the via-last approach. With via-first, the foundry "owns" the liability of the device wafer, whereas if the wafer is delivered to the OSAT and vias formed there, its' questionable who carries the liability if the wafer is damaged.

W2W, D2W, D2D Die Stacking

W2W stacking is a very attractive approach because it brings the power of the front end to the stacking process. However, because of KGD issues, W2W yield is still below 85%, and therefore is still cost prohibitive. Arkalgud notes that once yield is improved, it will be a better cost model, primarily because it is a parallel process. Conversely, both D2W and D2D model are sequential processes. There is a differentiation in the cost model. The question is which will prove to be more manufacturable.

SEMATECH is working through each process flow to determine the cost differentials. They are using a 300mm line, and are examining both W2W and D2W processes. Additionally, SEMATECH's research focuses on copper-to-copper bonding, using simple processes to evaluate at the materials level.

Wilfried Bair, GM of SUSS MicroTec's wafer bonder division, and VP of business development worldwide, believes that once all the technology limitations have been addressed, via -middle (first) and W2W processes will become standard for volume production of 3D SIC and 3D IC, because ultimately the cost of the end product will be less. Via-last, and D2W will serve to open the path to market adoption for 3D integration schemes, as they can be performed with existing infrastructure, but ultimately will be used for low volume and niche markets.

Thin Wafer Handling/Bonding

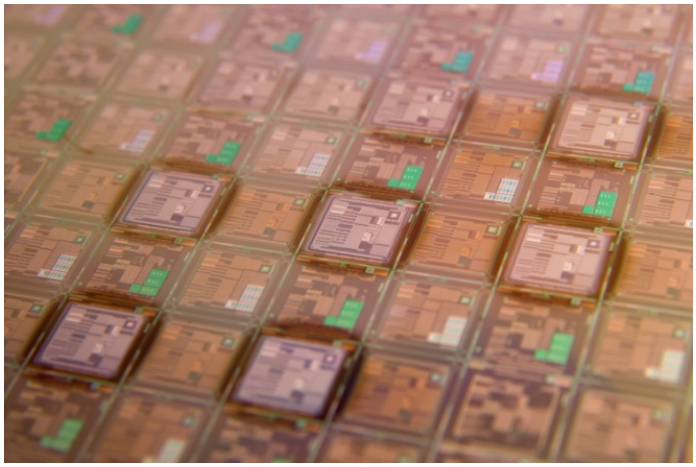
Beyond TSV formation and stacking approaches, other critical area that affects the end device cost and yield are thin wafer handling and bonding processes. These are grouped together, because they tend to go hand-in-hand. They are both critical to both W2W and D2W approaches.

Ultra-thin wafers are subject to considerable stress throughout the back-end processes (thinning, microbumping, stacking and bonding), regardless if the via is formed first or last. W2W stacking involves permanent bond steps before dicing and final assembly. D2W requires the device wafer to first be temporarily bonded to a carrier wafer for added support prior to dicing and stacking. Another consideration is face-to-face vs. back-to-face bonding. Arkalgud says face-to-face bonding works, but only for 2 wafers. Back-to-face bonding is required for more than 2 wafers in a stack.

With regard to the stresses caused by backside processing and subsequent bonding, Arkalgud notes that the greatest issues still lies with thermal stresses caused by processing conditions, and material requirements for temporary bonding and debonding methodologies. He says that SEMATECH's 3D program is actively involved in establishing standard methodologies with which to evaluate current processes and materials that are available, so to establish its own data that can be compared "apples-to-apples", rather than rely on data provided by individual suppliers. The organization is currently evaluating 300mm bonding tools to determine which will be most suited to carry out this work.

Beyne pointed out that although there are multitudes of companies who supply equipment for via formation steps, only two are involved in bonding processes at 300mm, EV Group and SUSS MicroTec. Both are working with material suppliers, research institutes and technology providers to develop the most cost effective, viable solution to address this. The companies' progress will be discussed later in this paper, in the section devoted to suppliers' progress reports.

Beyne points to sequential processing as being part of the issue. As such, IMEC is developing a hybrid parallel process to reduce the handling and stress placed on the die and wafer. The process involves a temporary bonding step during which all the die placed on the wafer, and then bonded collectively.



Seven ultra-thin die (25µm) with TSV connections bonded to a 200 mm device wafer using a collective D2W bonding technique. (Courtesy of IMEC).

Arkalgud says wafer thinning processes also still need to be addressed. For example, thin wafers often end up with a knife-edge that can chip. Incorporating metrology steps in the process flow can help determine solutions to this. As such, SEMATECH has partnered with Rudolph Technologies to address this.

Sillon notes that it's not so much the thinning process that is an issue, but handling of the thin wafers, and need for temporary bonding solution. He referenced the Disco process, which involves thinning only the center of the wafer and leaving a "frame" around the edge. This process requires no temporary bonding step; in this scenario, the wafer is transferred directly to dicing tape and then diced and stacked D2W.

Three materials-based temporary bonding processes of note are Brewer Science's thermoslide process, 3M's debond process, and Dupont's temporary PI adhesive concept.

In the Thermoslide process, the device wafer is flipped face down and temporarily bonded to a carrier wafer that has been first coated with an adhesive by spin-coating and baking. The device wafer is aligned and bonded and

backside processing occurs. During the debond process, an electrostatic chuck is secured to the backside of the wafer (now on top) and by applying heat, is slid off the carrier wafer. It is then flipped while still attached to the chuck, cleaned, and then either flipped again and attached to a dicing frame for D2W stacking; or aligned and permanently bonded for W2W stacking.

The 3M process requires only one carrier transfer in the temporary bonding step. In this scenario, both the device wafer and the glass carrier are spin coated with a material; adhesive on the wafer, and a release layer on the carrier. The wafer is then flipped and bonded to the carrier by means of a UV curing step. After backside processing, the thinned device wafer is flipped and attached to the dicing frame, the release layer is activated at room temperature by means of a laser to ash the material and remove the carrier wafer, and then the adhesive is peeled away from the device wafer, which is subsequently cleaned and ready for stacking.

Dupont's process is based on a polyimide-based temporary bonding materials, which the company claims shows superior qualities to Most conventional bonding adhesives, which exibit temperature/chemical resistance limitations. The bonding process involves coat/prebake, cure, and thermocompression steps. After backgrind, the debond can either be performed by laser ablation or application of heat to deactivate the adhesive. There is no release layer involved.

ADDRESSING TECHNOLOGY BOTTLENECKS

We have already identified the current technology bottlenecks to achieving market adoption of 3D IC with TSV interconnects as the lack of design tools, methodologies, thermal management solutions, and test strategies, although not all polled agree that any of these are really the hold-up. Therefore, this segment of the paper will report on the progress, if any that has been made in these areas, and discuss what still needs to be accomplished. Additionally, although it is not a technology limitation, supply chain issues have also been identified as one of the primary roadblocks for market adoption. Therefore, this will be discussed separately.

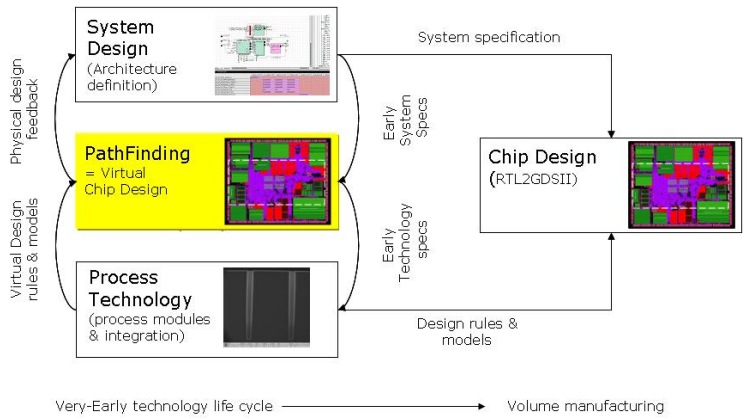
Design Tools

Offering an R&D perspective, Eric Beyne stated that he did not consider design tools to be a limiting factor. One school of thought suggests these integration schemes can be achieved without them, and designed by hand if necessary. Vardaman disagrees, noting that while IDMs such as Intel and IBM have the capability to develop their own internal-use-only design tools; many fabless companies must have their own design tools to achieve the full advantages of TSV. However, when it comes to market adoption and volume production, it is unanimous that without the right design tools, 3D IC using TSV as the method of interconnect cannot be achieved.
From the design community, the perspective is that without process technologies, characterization, parameters and tested prototypes, it's difficult to establish design rules. Lisa McIlrath, of R3Logic, says that as 3D integration is still very young, everyone is in "pathfinding" mode, exploring different designs before having the parameters figured out. She said that there is lots of advance work being done to discover different customer needs. Design tools needed now for CIS and soon for stacked memory may not necessarily turn out to be the same ones needed down the road for heterogeneous integration.

While none of the larger design houses report having developed EDA tools for 3D integrations schemes using TSV interconnects, there are rumblings that internal work is being done at Cadence. Additionally, some of the smaller companies have reported progress in this area.

At this year's DATE 2009, in Nice, France, several industry experts discussed the requirements for 3D design tools. Among them was Riko Radojcic from Qualcomm, who discussed Qualcomm CAD strategy for 3D TSV, and identified "Pathfinding," "TechTuning," and "Design Authoring" as necessary elements. He underlined the thermo-mechanical challenges related to 3D TSV and the new paradigm coming. Difficulties will come from the multi-scale thermo-mechanical analysis that will be required with 3D structures: millimeter scale at packaging level, micrometer at chip level, and nanometer scale at the transistor level.

He added a 2.5D design environment should be enough at the beginning for stacks of dies up to 2. Then, a real 3D environment will be required. [6]



j360 Silicon PathFinder 3D Platform (courtesy of Javelin Design Automations.)

In 2008, IMEC developed a PathFinding flow to determine design rules and models for virtual chip design. The result of PathFinding are clear specifications for process and design teams. The PathFinding flow creates an accurate estimate of performance, power, and cost of a 3D stack. Repeating this flow from system architecture to physical design allows designers to evaluate options, and process engineers to fine-tune their technology to the system specs. To accomplish this quickly, IMEC leveraged existing design tools, as well as developing a prototyping tool with EDA vendor, Javelin Design Automation.

A test chip was designed using a 3D environment created by extending existing 2D tools, then shared with IMEC's partners in the 3D program so they can design proprietary structures on forthcoming test chips. Case study results in which IMEC researchers validated the PathFinding flow on a 3D stacked DRAM indicate a potential power savings in the IO interface when adapting 3D technology to be. According to Beyne, since this announcement, further integration has continued, involving more than just Javelin. The next step is to involve EDA tool suppliers in the 3D program.

Just last month, R3Logic announced the establishment of its French subsidiary, R3Logic-France, which will include an R&D design center in conjunction with CEA-Léti and ST Microelectronics in Grenoble, France, to develop and enhance its design tools for 3D heterogeneous system and SiP design. The goal is to build a full 3D design flow that combines multiple-point tools to address all aspects of SOC design, substrate design, signal integrity, thermal management, environmental constraints, and RF issues, rather than handing them individual. CEA –LÉTI expects that these design solutions will accelerate developments in 3D chip-package co-design.

Thermal Management

Baron notes that thermal management issues are the most serious barrier Yole has identified, with the most potential to reduce the application window of 3D IC product. These issues include concerns like co-efficient of thermal expansion (CTE) mismatch due to heterogeneous materials, avoiding hotspots in stacked devices, difficulty of removing heat from individual layers, and power distribution between layers. One application that thermal management is not an issue is with Memory. Arkalgud says possible solutions could involve using dummy TSVs as heat sinks; developing design tools that dynamically detect where hotspots would be and designing accordingly; or even incorporating chanels for microfluidic cooling. However, these options are still at the R&D level.

The 2009 IMAPS Device Packaging conference featured a presentation about the development of a thermal test vehicle being developed by the University of Arkansas to prove feasibility of a 3D VSLI process that include TSV and flip chip stacking.

Paul Magill, of Nextreme Thermal Solutions, says that while thermal issues will be paramount for 3D structures Nextreme's involvement is still early stage. The company has developed a copper pillar thermal bump technology that addresses cooling at the chip level, which could ultimately address identified issues such as how to avoid hot spots in stacked devices.

Bill Bottoms suggests integrating carbon nanotubes into TSV processes may provide a solution to thermal issues due to their high thermal conductivity, low cost, and the fact that they can easily be incorporated as a filler to change the property of a matrix material.

While certainly research exists to address thermal management, no one contributing to this paper identified qualified solutions at this point. Magill notes that although traditionally thermal management is addressed last, in this case, leaving it to the end could be disastrous.

Test

Ho-Ming Tong, GM and chief R&D officer, and Daniel Yang, VP corporate R&D of ASE, one of the top OSATS providers, commented that test needs more attention. They pointed to contact issues, KGD or pretty good die (PGD), and that in terms of high-end products, test is a big issue. They also said quality assurance (QA) needs attention.

David Wang, VP of R&D at ChipMOS, concurred with ASE regarding test, adding that that Memory test takes longer given the time involved (in wafer sort, it takes average of four hours to test some 300mm flash product wafer).

As most methodologies being developed for 3D TSV stacks assume KGD, test continues to be one of the more elusive areas to be addressed. Perhaps it was expressed best during the 3D Panel at IMAPS Device Packaging Sympsium. From a practical perspective, Bob Patti of Tezzaron says he's not sure how a wafer with 1.5M channels will ever be tested. Tezzaron's solution is built-in self-testing and self–repair for DRAM memory stacks. Ultimately, though, he said, you will need to test the final package.

Approaches of testing memory and logic are completely different, said Beyne. He suggested that inspection is a more viable approach, such as with metrology tools. "A lot of metrology issues can be measured to compliment the testing. "In the end, the final structure will need to be tested."

Arkalgud agreed that test is a huge issue, and compared it to similar issues faced in system-on-chip (SOC) applications. While SEMATECH is not directly involved with test, they have partnered with IC CAD to hold workshops to stimulate discussion. He agreed that self-test and repair is being considered by SEMATECH as well.

Recent work done by Dean L. Lewis, Xin ShaoProfessor Hsien-Hsin S. Lee, Professor , Sung Kyu Lim, Georgia Tech, investigated the possibility of using pre-bond, scan-based test technology to test each chip after TSV formation. The study shows that traditional boundary scans can be employed to test the quality of the actual TSV bonds. These technology solutions are simple extensions of current scan-based test technology, enabling simple integration of 3D into current test systems. Results show that full pre-bond test can be achieved at equal or lower cost than testing an equivalent planar design. [7] The test reportedly works for D2W and D2D approaches, but not W2W.

Obstacles to pre-bond testing of wafers in 3D integration include probing issues for face-to-face bonding; hundreds of thousands of copper pads on the bottom die, in addition to the small size and large numbers makes probing signals impossible. Top wafer cannot be probed from the copper side. TSVs are buried and C4 pads are not fabricated prior to bonding. [8] TSV stacking also opens up new defect possibilities. In D2W stacking, only the top layer die is exposed for testing after stacking.

Some possible solutions are being worked on and include test access mechanisms and partial functionality testing. [9] However, to date all of these solutions are still being researched.

SUPPLY CHAIN ISSUES

How the supply chain will handle post-fab processes—beginning with backgrinding (thinning), bonding (both permanent for W2W and temporary bond/debond for D2W and D2D, microbumping and stacking processes—has been identified by most surveyed for this paper as a roadblock to market adoption.

Baron notes that the supply chain issue is a sensitive topic because addressing it points to the strategy of individual players. The potential supply chain value change opened up by TSV interconnects has added more value to the package, and as such is strategic with the coming of 3D integration era.

While the question being asked seems to expect an either/or answer—fab/foundry, OSAT, or a third location—the general consensus was that it will be some of each. Based on his work with the ITRS, Bottoms said that post fab processes are already being done at fabs, OSATs and IDMs. However, he says that independent of who owns the facility, post-fab processes will take place in a separate facility from the front end and traditional assembly and test floor clean rooms.

In Arkalgud's opinion, where the processes are done will be product specific. Packaging approaches will be handled at OSATs; front-end foundry steps will include TSV formation, fill, CMP, but from dicing processes on, processes are more suited to the OSATs arena.

Beyne categorized IMEC's perspective on who will do what as follows:

- 3D-SIC TSV process will be done in the fabs/foundry.
- Thinning and backside processing will fall into the jurisdiction of IDM's and OSATS
- Likewise, stacking will take place mainly at the OSATs or by the packaging groups at IDMS.

In response to the question of whether the fabs will invest in post-fab processes, Beyne says that while some will, most will partner with OSATS for thinning and backside processing. It is well known that these so-called "dirty processes" are better accommodated in the OSATS.

One concern about passing delicate and expensive device wafers from fab, to post-fab, to OSAT is the number of times a wafer is handled. However, even in the larger IDMS that have separate divisions dedicated to front-, middle- and back-end processes, the wafers go through several transfer processes. So ultimately, transporting the wafer should not weigh in to this issue.

IDMs and Foundries

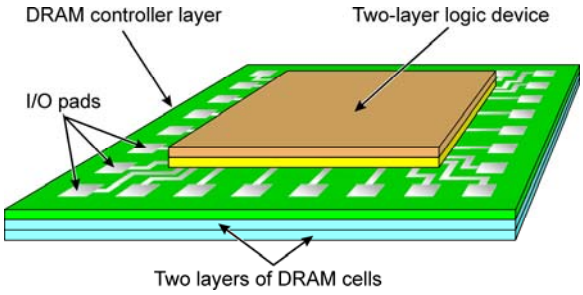
While Chartered Semiconductor was the only foundry to respond to our questionnaire, and Tezzaron was the only device manufacturer, we heard from 4 of the major packaging houses regarding their intentions. Jan Vardaman also weighed in with some notes about Intel and TSMC.

Intel closed assembly lines in Malaysia and the Phillipines, choosing instead to outsource final manufacturing to OSATs; TSMC announced the installation of 300mm TSV production tools, indicating their intention to ready themselves for 3D ICs. According to Vardaman, installation of 300mm production lines is key to the expansion of the technology outside of niche applications such as image sensors for camera modules. In addition, the foundry announced an expanded partnership with IMEC, with the intention of locating their European R&D there.

Chartered Semiconductor reports involvement in TSV processes for both 3D SIC and 3D IC heterogenous stacking and repartitioning. However, they do not plan to invest in post-fab processes. The company is in collaboration with Singapore's International Microelectronics center (IME) with the main objective of engineering studies on generic model involving TSVs and its application from FEOL to BEOL. Studies include simulations on electrical, thermal and mechanical aspects, with results used to understand individual process components and variations for better control and manufacturing purposes.

Tezzaron Semiconductors

Tezzaron has been a pioneer in consumerization of TSV and 3D integration schemes, and have been building devices that integrate 3D in low volumes for customers since 2004, beginning with CMOS image sensors.



Logic-on-memory devices, assembled in a die-to-wafer process using TSV interconnects. (Courtesy of Tezzaron Semiconductors)

According to CEO Bob Patti, the company's flagship is DRAM memory using tungsten-filled TSV interconnects. Unlike the stacked DRAMs announced by Micron and Samsung, which are connected at the I/O pad and therefore not fully integrated, Tezzaron's DRAM will connect at the row/column level.

The company is also actively working with heterogenous stacking of bulk silicon for logic on memory stacks, and repartitioning of system-on-chip (SOC) devices. Patti sees both as extremely viable for volume production.

The company is taking memory and CIS to volume production this year, and will continue to offer stacking services to customers.

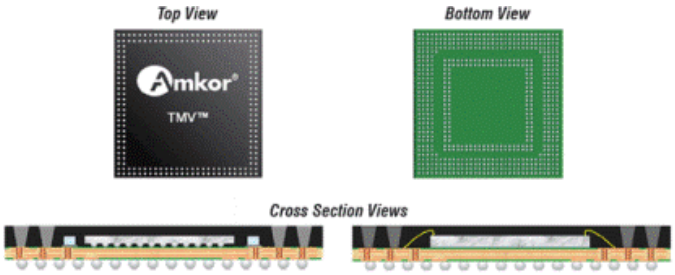
Patti does not see design tools or test as a limiting factor for Tezzaron, although improved design tools would be helpful. They have developed their own built-in test and self-repair (B-STAR). While supply chain and equipment issues have been aggressively addressed this year, there is still work in the tool development area.

Patti predicts that at some point, via-first will be abandoned, via-last will be a niche, via-middle will be done in volume. All 3 types of stacking will be in volume production, but for different applications.

OSAT PERSPECTIVES

Amkor

Amkor is an industry leader of technology and high volume manufacturing for a broad range of 3D packaging technologies. At the 3D SiP level, Amkor has been involved in developing first and next-generation PoP technologies, the most recent innovation being the through-mold via PoP (TMV POP); and wire-bond die stacks for combined memory including 8 die stacking for high capacity NAND requirements. High-density wire bond, and flip chip + wire bond die stacking for logic + memory integration round out the company's current portfolio.



Additionally, the company is involved in development of 3D WLP such as redistribution and flip-chip bumping, fan-out WLP for future production requirements. Lee Smith says that while they are not involved with CIS, the company is involved with developments in 3D SIC for memory, and 3D IC for repartitioning.

Smith says Amkor supports a via middle approach, and sees die-to-substrate stacking as offering the best flexibility for integration of mixed silicon technologies or devices from different fabs. Amkor is investing in post-fab processes for 3D IC stacking, as this is an area of opportunity for the OSATS. In fact, the expertise for these processes lies with the OSAT rather than the foundry.

ASE

ASE is considered one of the top OSAT companies, and handles all packaging products for a global customer base. As such, they have no choice but to be involved in and prepared for advanced 3D technologies, though R&D is very expensive. According to Tong and Yang, of ASE, TSV is not a matter of if but when, and the company has programs in both via-first and via-last approaches. They have a line that includes etch and CMP process tools. Although they are not involved in any consortia, partially due to the cost of joining, they are working with leading customers in developing these processes.

They predict that a via-first approach will likely be targeted for high-end performance applications like CPU and baseband products, while via-last is targeted for cost-driven products, such as CIS. They expect gradual migration of DRAM to TSV, with first migration for high-end server applications. Moreover, as expected, they see supply chain integration as one of the biggest hurdles to be overcome.

They believe that the foundries and OSATS need to work closely in cooperation with the customer, and that chip companies will not only rely on the foundry partner for TSV, but will need to also partner with the OSAT.

At ASE, they report that assembly is "generally ready for prototyping," although cost of ownership (CoO) needs to come down, and more robust processes need to be developed. They see a need for more cost competitive tools, not only for etch and other processes, but testing too.

ChipMOS

As a major OSAT, ChipMOS' key focus areas are packaging for memory and LCD drivers, and mixed-signal business. David Wang, VP of R&D at ChipMOS, provided information on the company's position on 3D integration technologies.

In the TSV realm, the company has taken a cautious approach, and although they have development activities, they are at the test vehicle stage.

Wang says that while TSV initially may be good for an IDM and for memory manufacturing because of performance requirement for server applications, there are still questions of how to implement TSV for high I/O applications. He sees cost issues in processing and testing. As such, beyond CIS, the question remains: who will be the first to take the leap for volume production?

ChipMOS runs a lot of stacked-die, wire bond packages in high-volume, achieving high yields with good reliability. Therefore, TSV will need to be cost effective to compete with the 3D wire bond die stack.

Wang categorizes test, KGD, thermal management, and design tool availability among the supply chain issues yet to be addressed.

As Wang and his TSV team leaders are very cautious about bringing front-end processes in-house. Back-end companies traditionally do not have experience with etch and PVD for example. Additionally, back-end clean rooms are not the same class as front-end clean rooms. Therefore, they believe via etching belongs in the front-end. Additionally, back-end companies' strengths lay in thin wafer handling and in wafer thinning, assembly, test etc. and so those processes should continue to be handled there.

Therefore, ChipMOS does not intend to build a front-end line (etching, via formation). Rather, they intend to leverage their back-end infrastructure to handle process such as post-fab processing (plating thinning, handling, bonding, test, etc) while having their customers use their own existing infrastructure to focus on via etching.

STATS ChipPAC

With regard to post-fab processes for 3D IC stacks, Flynn Carson, VP of Technology Marketing for Emerging Products at STATS ChipPAC, says he doesn't expect OSATs to be a major player in the front-end TSV, and that it will fall to the IDMS and OSATS to handle the 'mid-end' processes. He sees collaboration between foundries and OSATS to enable TSV 3D integration.

Therefore, STATS ChipPAC has invested in developing capabilities for post-fab processes including microbumping, thin wafer handling, backgrinding, and both D2W and D2D stacking processes. Additionally, the company is investing in supporting via-last processes for TSV interposers, and interposer substrates. However, they will leave the via-first process to the fabs.

Carson says the capabilities are currently being developed, cost is the driver. The company's timeline for rolling out capabilities will begin with interposers and possibly via last next year, and 3-5 years for advanced processes for 3D IC. He estimates volume production readiness for 3D IC post-fab processes in 3-5 years.

With regards to memory stacks, Carson notes that memory suppliers will handle stacking memory themselves, and STATS will be involved in the assembly of heterogeneous stacks.

STANDARDS DEVELOPMENT

While not necessary for market adoption of 3D integration technologies, the general opinion is that yes, standards will be important to volume production at all levels of 3D. However, the jury is still out on how those standards will be established, and who/which organizations will lead the way.

Opinions vary on both the necessity and the ability to establish design rules when there are so many variables to consider. Beyne notes that first, we need definitions and roadmaps, standards come after that. However, he adds that processes will not be standardized; only the interfaces and interface dimensions.
Most agree that there are benefits to standardizing the interface of memory to logic in a 3D IC configuration. Design rules will be needed to address the gaps between front-end and back-end players, notes Wang. Beyond that, he points out that flip chip processes have been in volume production without being standardized.

Some point to industry organizations, and primarily the ITRS, while others suggest it will be the larger IDMS who will dictate what standards will be as they integrate these technologies into their devices. Ultimately, the task will fall to whoever has the most vested interest in the resources to make it work.

ASE's position is that standards will evolve as volume production ramps, and be driven by market leaders and key players along the way. As standards minimize risk, they will be critical to reach volume levels. Additionally, for CPU and baseband applications, time-to-market is critical, so standards across the supply chain allow companies to meet time-to-market requirements.

A lack of standards will not prevent volume manufacturing from a process perspective. While standardization at the pin or packaging level can affect individual TSV package adoption, this is no different from the current market. Standardization will be developed as needed, and customization will happen as desired.

EQUIPMENT/MATERIAL SUPPLIER PERSPECTIVES AND UPDATES

Many of the suppliers polled offered input on information previously discussed, and as such, this paper reflects the collective input of many. Here, we address individual company involvement in emerging 3D IC integration schemes; and progress with their tools, materials, and processes.

Alchimer S.A.

Alchimer develops innovative chemical formulations and processes for semiconductor-related nanometric coating deposition. It is 3-tiered process, AquiVia, process replaces conventional dry process flow for insulation (CVD), barrier (PVD/CVD/ALD), and seed (PVD) layers with proprietary wet-based electrografting, chemical grafting, and electrografting processes, respectively.

According to business development manager, Kathy Cook, Alchimer is involved in several JDPs. They are active members of VERDI, an R&D consortium involving, among others, Tegal Semiconductor, ST Microelectronics and CEA-Léti. The objective is to develop 3D IC technologies for very small, high-density TSVs in very thin 300-mm wafers. Recent achievements with Alchimer's eG ViaCoat process were just announced that reportedly provide customer cost savings of up to 80% compared to dry vacuum processes.

AZ Electronic Materials

As lithography is paramount to TSV formation, AZ Electronic Materials is involved in 3D integration schemes at all levels by supplying lithography materials and application process support for their products. Although they are not directly involved in consortium activities, they participate indirectly through relationships and interactions with IDMs and research organizations globally.

According to AZ, several key 3D lithographic processes and respective performance demands include definition of vias (withstand severe dry etch conditions), Cu RDL processes, and bump formation (strong chemical and thermal resistance properties). Some current thick-film AZ resists perform for all three noted steps. However, newer materials available have been specifically engineered to meet the increasing performance requirements. These resists include both negative-acting and positive-acting resists that provide increased resolution and higher aspect ratios in varying film thicknesses.

AZ has reportedly developed positive resists that enable 10:1 aspect ratios and the formation of sub 500 nm vias. Additionally, the company's negative resist for thicknesses up to 100 µm is well suited for solder bump build-up. Another negative-acting resist in AZ's product portfolio is said to provide film thickness up to 15 µm, with higher aspect ratios and better resolution than equivalent thickness positive resists.

Brewer Science

Brewer Science is involved in materials development for 3D WLP, 3D SIC and 3D IC heterogeneous stacking. The company reports it is developing technologies to enable BEOL processing on wafers thinned to <100µm. The company has invested in R&D equipment for materials development that are required for post-fab processes for TSV stacking.

Brewer Science is materials partner within the EMC3D consortium, and also recently entered into a JDA with CEA-Léti research programs include both via-first and via-last development, but all require technology to support and protect thinned wafers through handling and high temperature processes. As such, Brewer Science stressed its interest in the thinned wafer handling work at this time, as this is the first, and possibly most difficult, hurdle to overcome.

Dow Chemical (formerly Rohm and Haas)

While Dow does not get involved with developing processes for 3D integrations schemes, they are working with device manufacturers and equipment makers on materials technologies for 3D integration. They have a JDA with IBM (announced publicly last year), and are members of the EMC3D consortium.

EV Group

EV Group's involvement in developing processes and tools spans the levels of integration schemes. They readied themselves for various 300mm TSV and WLP applications with such production-worthy equipment as bonders, aligners (bond aligner and mask aligner), coaters, cleaners, IR inspection systems, temporary bonders and debonders. Bioh Kim, director of business development for 3D and advanced packaging, detailed EVG's involvement in each. EVG is engaged in overall lithography business for wafer-level backside metallization such as RDL, pillar, solder, etc., for various device manufacturing. They also handle carrier bonding and debonding with lamination tape or spin-on adhesive for fan-in and fan-out WLP.

With CIS, they cover nano-imprint lithography for wafer-level optics; UV bonding for lens wafer stacking; polymer bonding or silicon direct bonding for stacking CIS device wafer onto carrier wafer; nano-spray coating for TSV passivation or etch mask layer formation; overall lithography for backside metallization; temporary bonding and debonding for thin device wafer handling, etc.

For DRAM or NAND stacking and heterogeneous integration, in addition to the aforementioned capabilities, EVG supports W2W or C2W thermo-compression bonding or direct oxide bonding; temporary bonding and debonding for thin device wafer handling.

EVG reports recent alignment accuracy achievements with its bonder tool, reaching 1 µm post-bond alignment accuracy at a throughput of up to 4Bph for Cu-Cu bonds, with a future goal of 0.5 µm accuracy; and 0.5 µm accuracy with a throughput of up to 24Bph for Si02 bonds, with a future goal of 0.25 µm accuracy.

Recently EV Group and CEA-Léti announced the partnership to accelerate adoption of TSV and 3D integration technology. EVG will provide CEA-Léti with its 300mm temporary bonding and debonding technology. EVG is a Board Member of the EMC-3D Consortium and is considering joining the 3D ASSM Consortium sponsored by Georgia Tech and the Fraunhofer IZM.

Lam Research Corporation

In the 3D space, Lam Research is involved in developing processes in CMOS, memory and logic applications and sees expanded opportunities in wafer thinning processes. They report having TSV etch systems installed in production/pilot lines for 3D SICs.

The company's research efforts are focused on improving unit process performance, such as delivering required results with a thinner photoresist, and tailoring performance from the etch system to reduce overall cost. Lam Research is working with industry consortia to advance 3D IC integration from a fundamental etch and final performance perspective. They have established programs with peer companies and within internal groups to understand better the interactions of sequential 3D TSV unit processes. For example, Lam Research is exploring the interactions of etch and clean to optimize and potentially integrate unit process capabilities to achieve the final desired on-wafer results.

NEXX Systems

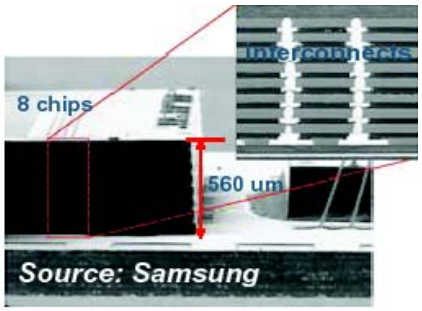
Tom Walsh, CEO of NEXX Systems, reports that the company is involved in developing processes and tools a variety of 3D integration schemes including RDL, flip chip and fan-out for 3D WLP. At the production level for CIS, they are working with multiple customers including Xintec and ST Micro. Additionally, they are involved in R&D programs with both SEMATECH and IMEC for stacked memory, and at IMEC for heterogenous integration with, for example, GaAs with CMOS logic. The SEMATECH program is focused on via-first with vias starting at 5µm and going to 1µm. The goal is for wafer stacking for memory and memory logic. Additionally, NEXX is working with IBM; however project information has not been thus far disclosed.

NEXX is addressing the challenge of processing thin wafers below 50µm, which then sets via size as aspect ratios are limited to about 10:1 with current seed/barrier technology. Walsh says progress is being made with production starting in 2010.

They are also working to replace iPVD with CVD barrier and wet seed layer processes thanks to the availability of improved plating chemistry for higher deposition rate. CVD and wet seed process will permit higher aspect ratio and therefore smaller vias for a given wafer thickness.

S.E.T

S.E.T's flagship tool is an accurate die bonder that can perform both face-to-face and back face-to-face die bonding processes. The SAMSUNG memory stack shown here, was performed on a FC250 from SET (SUSS at the time of purchase) Additionally, LÉTI used the SET FC150 for stacking memory as early as 1997. SET is also talking to other memory companies with the new bonder FC300.



Samsung memory stack

As SET's tools feature high accuracy rather than speed, they are currently best suited to an R&D setting. They have a JDP with IMEC with an SET-FC300, high-accuracy (0.5µm), high -force (4kN) die bonder installed at IMEC for a 3-year 3D IC program. IMEC will develop a process with scaling capability for ahigh throughput machine; SET supports the tool and handles modifications required to achieve it. Additionally, asn FC300 was ordered by SEMATECH for Cu-Cu bonding techniques; however, no JDA is in place yet. The company is also engaged in a 3-year European Program, JEMSiP_3D, which involves the development of a high-speed, high accuracy die bonder And lastly, SET is involved with Minalogic Project that is under evaluation for 3D integration using direct Cu/Cu or oxide bonding.

SUSS MicroTec

SUSS MicroTec has launched its new business strategy around 3D integration, developing the 300mm toolset to be optimized for 3D processes first and foremost, which will also benefit the other markets they serve, such as MEMS and WLP. Regardless of which variations shake out as standard for 3D integration schemes, SUSS offers the tools to cover it from development to production. This includes 3D interconnect applications such as lithography to create the etch masks for Through Silicon Vias and dicing streets for plasma dicing, backside redistribution layers (RDLs) or bumping applications (mask aligners, spin coaters), bonding and stacking for either wafer-to-wafer or die-to-wafer stacking (permanent bonding).

In addition to wafer level optics assembly (microlens printing and stacking) for CIS SUSS MicroTec supports wafer bonding for CIS backside illumination using fusion or adhesive bonding, CIS packaging applications using backside alignment, infra-red alignment and custom solutions to accommodate handling of warped wafers, high topography lithography.

For heterogeneous integration for memory or logic the company offers metal bonding at 1um accuracy (eg. Cu Cu bonding) with a future goal of 350nm and fusion bonding at 350nm, and wafer-to-wafer alignment accuracy with a future goal of 150nm.

SUSS MicroTec's most recent accomplishment in 3D is its temporary bonding and debonding system for thin wafer handling, which can be configured for a variety of materials and processes including common thermoplastics, Thin Materials AG, Dupont and 3M. The debonding capabilities include both mechanical and thermal release processes.

Ultratech

Ultratech supports all three categories of advanced packaging processes, and believes that 3D WLP will be utilized by the industry to meet the short-term (next 1 – 2 years) integration requirements while 3D stacked ICs will be utilized in the long term (3 – 5 years).

While the company is not involved in any 3D integration consortiums, they work closely with select customers to enable leading-edge advanced packaging processes, because they feel that JDAs allows them to focus on the uniqueness of a particular process flow.

Ziptronix

Ziptronix is an IP company that has developed and patented the ZiBond and Direct Bond Interconnect (DBI) processes, which can be integrated into all levels of 3D integration schemes. For example, with 3D SiP, the technology allows existing PoP solutions to be converted into D2D at wafer level and save on packaging. CTO Chris Sanders reports that the company is working with customers looking to integrate this process into mature processes and older nodes. Both processes are applicable for CIS and allow for scalability for future applications without drastically changing the existing (or soon to be developed) architectures. Additionally, both 3D SIC and 3D IC are target applications for DBI.

SUMMARY

3D Integrations schemes have been categorized by levels of interconnect. 3D SiP refers to traditional methods of package interconnect such as wire-bonded stacked die and PoP configurations. 3D SiP is the first 3D configuration to have reached volume production.

3D WLP refers to wafer level interconnects occurring at the bond-pad level. Via-last TSVs for CIS are classified here. CIS and silicon interposer technologies are the first TSV applications to reach market adoption.

3D SiC uses wafer-fab processes to realize interconnects at the 0 level, such as with via-middle TSV formation and D2W stacking processes for DRAM memory stacking, or logic on memory stacks. Pending industry readiness (equipment, processes and materials), product prototyping, and design tool readiness; market adoption and volume production are predicted for 2012-2013 time frame. This could come sooner, if a champion IDM or foundry (such as TSMC or Intel) targets an application.

"True" 3D IC is the Holy Grail – a "super die" that involves repartitioning and stacking at the transistor level. This configuration is driven by functionality, rather than cost, and will appear on the scene closer to 2020.

The successful achievement of all of these technologies relies on collaboration and participation across the supply chain. There is a call for more communication and information sharing between the design, test, and manufacturing communities to accelerate the march towards market adoption. To this end, a variety of consortia, collaborations, joint development projects ad multi-project wafers have been formed to promote development of 3D integration.

Standards, while necessary for volume production, will most likely follow initial market adoption as processes of record are determined.

While first-generation products are likely to be rolled out using via-last/D2W processes, as via-middle and W2W technologies are perfected, they will likely pave the way for volume production.

Equipment and materials suppliers stand at the ready with tools and processes for development, with volume production clearly in their sights. Design and test communities are lagging slightly, waiting for design rules to be established, and still working out test models to address that issue. Thermal management has been a tertiary concern, but experts in thermal solution caution about waiting until the end of the development processes to come up with cooling solutions for 3D stacking.

While via first/middle formation will fall under the fab jurisdiction, post-fab processes will become the responsibility of those packaging houses that invest in building the necessary facilities to accommodate them, and will require more collaboration and partnership with the foundries.

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