

# A Band-Reject Nested-PLL Clock Cleaner Using a Tunable MEMS Oscillator

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**Abstract**—This paper presents the Band-Reject Nested-PLL (BRN-PLL) scheme that simultaneously improves filtering of a noisy input signal and relaxes the requirements for the loop bandwidth. As the architecture employs a modified PLL as a divider of another PLL, a stability analysis is presented to demonstrate suitable operation. The BRN-PLL close-to-carrier output noise is dominated by the PFD/CP of the inner PLL and the far-from-carrier output noise is dominated by the LO of the outer PLL. The PFD/CP noise can be reduced by approximately 20 dB when the output is disconnected from the VCO during idle states, and a low noise floor is achieved using a passively biased double-switching pair LC VCO. Additionally, to maintain lower integrated phase noise, the proposed scheme uses a high- $Q$  MEMS-based VCO to effectively smoothen the transition of the response between the two dominant noise sources. Absolute figures equal to  $-105$  dBc/Hz at 1 kHz and  $-155$  dBc/Hz at 10 MHz are measured from a 104 MHz clock-cleaner.

**Index Terms**—Band rejection, Bode plots, LC VCO, MEMS resonator, Nyquist stability criterion, PLL, pole-zero locations, switching network.

## I. INTRODUCTION

CLOCK conditioners are used to minimize the effect of clock inaccuracy on the signal to noise ratio (SNR). The function of this block is to reduce jitter and improve the spectral purity of the clock signal in synchronous systems. A phase-locked loop (PLL) can be used as a clock cleaner because it behaves as a highly selective tunable band-pass filter. In the locked state, the PLL allows the phase noise (PN) of the input signal to pass close to the carrier frequency, while that of the PLL local oscillator (LO) will dominate at large offset frequencies (noise floor) [1].

For clock conditioners, a narrow loop-filter bandwidth is desirable to reduce the input signal noise contribution at the output. However, reducing the bandwidth is usually at the cost of increased loop-filter area, and the very close-to-carrier signal is still dominated by the input signal. On-chip integration can be

compromised due to the large capacitors, if passive filters are used to reduce noise.

Since clock cleaners are dominated by PLLs with narrow loop-bandwidth, ultra-clean LOs have become a challenge to the system integration. Existing solutions mostly use crystal LOs [2]. However, using just one LO to improve the cleaner performance requires complex strategies to guarantee noise specs, stability and chip-level integration [3]–[5]. The cascade-type PLL architecture can be employed to clean the clock signal in two steps [6], [7]. With this approach, the input-signal PN can be divided into two regions, and two LOs are used to target each section independently, with the noise at very close-to-carrier is still determined by the reference signal.

Modifications to the basic PLL architecture involving nested loops can be introduced to improve system performance [8]. It has been shown that using two loops and a high-pass filter (HPF) in a composite configuration produces an effective input signal-cleaning scheme [9]. The Band-Reject Nested-PLL (BRN-PLL) architecture provides a notch in the input transfer function that attenuates the input PN, relaxes bandwidth requirements and allows a substantial reduction in loop-filter footprint.

Attenuating the close-to-carrier input noise, the output PN of the proposed configuration is dominated by the building blocks involved in the architecture composed of inner and outer loops. Phase detector (PD) and charge pump (CP) noise dominates the very close-to-carrier output PN, while LO in the outer loop determines the noise floor of the output signal (typically an LC-based LO is used). Due to the introduced notch, outer-loop PD/CP and inner-loop LO become the dominant noise sources near the passband [9]. This paper reports on the use of a high- $Q$  oscillator as inner-loop LO to favor smooth shaping of the output-signal PN that eliminates the hard transitions between the PFD-CP noise and that of the LO that dominates the noise floor as compared with [9].

For integrating high- $Q$  oscillators, MEMS resonators have emerged as viable candidates that can be fabricated on silicon wafers similar to integrated circuits, offering excellent close-to-carrier noise performance, albeit with increased temperature sensitivity compared to quartz resonators [10], [11]. Therefore, successful insertion of integrated MEMS resonators into cost and power sensitive applications requires appropriate tuning and compensation techniques [12].

The paper starts with describing the BRN-PLL scheme, addressing system stability and explaining how the performance is affected by noise sources within the structure. Then, the design criteria for the building blocks are extracted, and the noise-oriented implementation of PDs and LOs is explained, including

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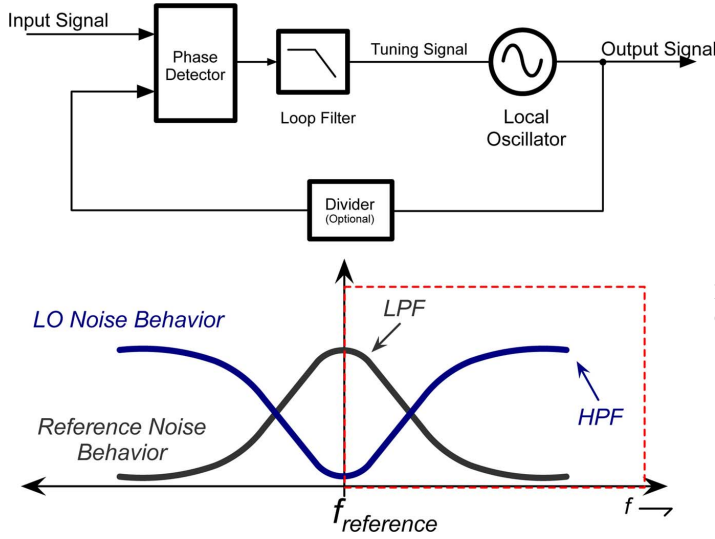


Fig. 1. Basic configuration of a PLL and its behavior with respect to input (i.e., reference) and LO noise sources.

an implementation of a MEMS-based VCO. Finally, the measurement set-up and results of a 104 MHz MEMS-based clock cleaner are described from which conclusions are drawn regarding the system behavior.

## II. BAND-REJECT NESTED-PLL ARCHITECTURE

A PLL can be configured with a PD, a loop filter and an LO as shown in Fig. 1. For this work, the PD is selected as a phase-frequency detector (PFD), and the LO as a voltage-controlled oscillator (VCO) without loss of generality. A PFD is preferred for its frequency acquisition capabilities; however, this choice imposes the use of a CP to interface the loop filter.

From a noise point-of-view, a PLL behaves as a band-pass filter for the input noise and as a stop-band filter for that of the LO. When the system locks to the input signal, the one-side-noise-spectrum transfer functions [13] can be used to define the PLL behavior as low-pass and high-pass, respectively (Fig. 1).

For clock cleaning applications, the PLL bandwidth is desired to be sufficiently narrow such that the noise on the input clock is filtered. However, complete rejection of the input noise is not possible because it implies moving the filter dominant pole close to the origin impacting the phase margin and therefore system stability.

On the contrary, the alternative BRN-PLL scheme exhibits a notch in the input noise transfer function to attenuate the input-clock noise as illustrated in Fig. 2. Compared to the filtering procedure of a cascade-type PLL [6], [7], the BRN-PLL exhibits one cut-off frequency that can be used to take advantage of the notch for attenuation. Increasing the bandwidth of the proposed system extends the stopband of input-noise filter. Since it is assumed that the input is a digital signal, the BRN-PLL output is adjusted to the amplitude levels of the line-coding scheme used before delivered to other parts of the system.

The notch in the BRN-PLL response is created by introducing a zero in the system using inner and outer loops and a HPF as shown in Fig. 3. The HPF is used as the divider of the inner loop, which as a whole, is utilized as the divider of the outer loop. Negative feedback is satisfied in the system by the appropriate

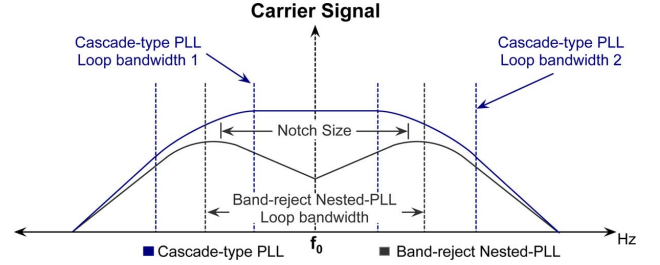


Fig. 2. Input transfer function filtering of the BRN-PLL. Comparison with a cascade-type PLL is provided.

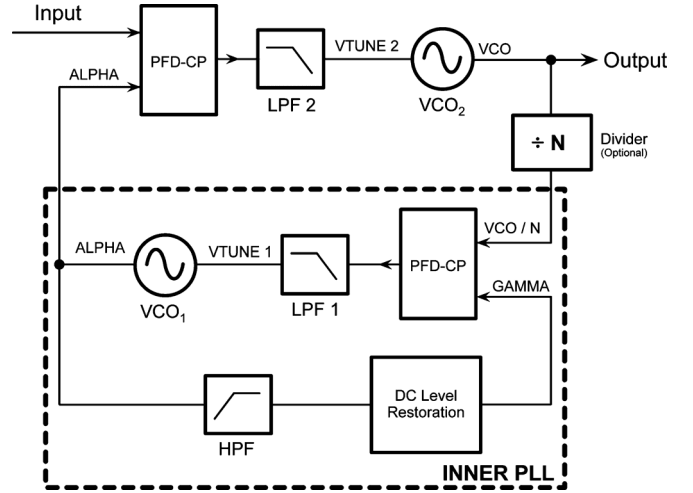


Fig. 3. The BRN-PLL architecture for clock cleaners.

connection of the PFD ports, which allows the two loops to track each other concurrently to the input signal.

### A. Stability Analysis for the BRN-PLL Architecture

Stability analysis for the BRN-PLL is required to assure the system will work as the intended PN filter with proper transient response. Since the system has a nested PLL, the stability analysis will be developed in two steps. First, the inner PLL will be analyzed both open loop and closed loop anticipating its effect on the outer PLL. Second, the inner PLL is replaced with a closed-loop equivalent and the stability of the complete BRN-PLL is addressed.

**Inner-PLL Stability Analysis:** When the PFD/CP combination is used, the tuning voltage is determined by the charge stored (removed) to (from) the loop filter. That charge is obtained by integrating the current, which is equivalent to a pole at the origin of the system. The additional pole and zero provided by the loop filter offer the required compensation for stability.

In the inner-PLL case, the HPF bandwidth should be selected so that the VCO signal can pass through without appreciable amplitude loss that deteriorates PFD detection. In addition, the loop-filter bandwidth should be wide enough to reduce the inner-PLL capture time, and therefore the effect on the acquisition and tracking processes of the BRN-PLL.

Fig. 4 summarizes the zeros and poles in the inner PLL. For simplicity, the inner PLL employs a second-order current-type loop filter and a first-order HPF. Although a CP-based PLL creates a type-II system that eliminates both step and ramp phase errors, the HPF zero located at the origin reduces the inner PLL to a type-I system, which will be able to eliminate up to the error

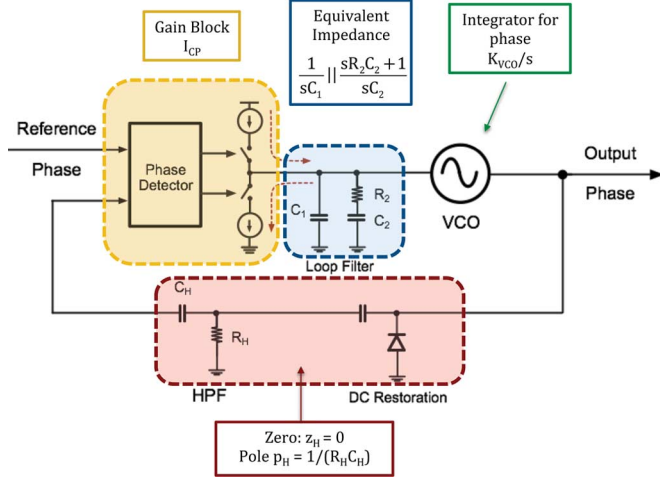


Fig. 4. Pole-zero roots for the inner PLL.

produced by a phase step. This condition cannot be considered critical since a type-I system can still track its reference signal.

Minimizing the roots becomes a suitable design criterion for the inner PLL, since the closed-loop equivalent will be passed to the outer PLL. From Fig. 4, the transfer function of the filters used in the inner PLL can be defined as

$$LPF_1(s) = \frac{s(R_2 \cdot C_2) + 1}{s^2(C_1 \cdot C_2 \cdot R_2) + s(C_1 + C_2)}, \quad (1)$$

with two time constants,  $T_1$  and  $T_2$ .

$$T_1 = \frac{1}{\omega_1} = R_2 \cdot \frac{C_1 \cdot C_2}{C_1 + C_2}, T_2 = \frac{1}{\omega_2} = R_2 \cdot C_2. \quad (2)$$

These expressions along with the definition of the HPF as

$$HPF(s) = \frac{s \cdot R_H \cdot C_H}{s \cdot R_H \cdot C_H + 1}, T_H = R_H \cdot C_H \quad (3)$$

let define the closed-loop gain as

$$TF_1(s) = \frac{G_1(s)}{1 + G_1(s)H_1(s)} \quad (4)$$

$$TF_1(s) = \frac{K_\phi K_1 \frac{1}{C_1 + C_2} \frac{1}{s} \frac{(sT_2 + 1)}{s(sT_1 + 1)}}{1 + K_\phi K_1 \frac{1}{C_1 + C_2} \frac{1}{s} \frac{(sT_2 + 1)}{s(sT_1 + 1)} R_H C_H \frac{s}{sT_H + 1}}, \quad (5)$$

where  $K_\phi$  is the PFD/CP gain and  $K_1$  is the gain of VCO<sub>1</sub>. Setting the constants  $A$  and  $B$  as  $K_1 \cdot K_\phi \cdot 1/(C_1 + C_2)$  and  $A(R_H \cdot C_H)$  respectively, (5) can be simplified as

$$TF_1(s) = \frac{A(sT_2 + 1)(sT_H + 1)}{s(s(sT_1 + 1)(sT_H + 1) + B(sT_2 + 1))}. \quad (6)$$

Time constant  $T_2$  is made equal to  $T_H$  to further simplify (6). The final expression for the closed-loop transfer function ( $TF$ ) is

$$TF_1(s) = \frac{A(sT_2 + 1)}{s(s^2T_1 + s + B)}, \quad (7)$$

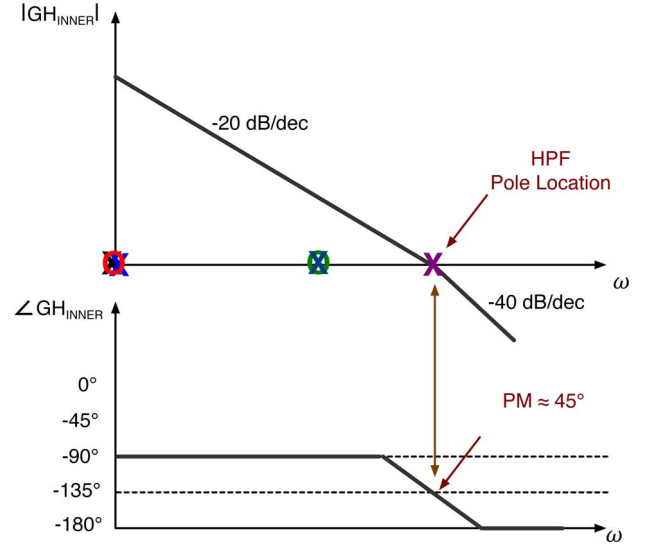


Fig. 5. Bode plot displaying the effect of poles and zeros for the inner PLL.

which shows one zero at  $1/T_2$ , one pole at the origin and a pair of real or conjugate complex poles. Once the closed-loop transfer function has been simplified, it is possible to go back to the open-loop expression and select the root locations for the inner PLL.

Making  $T_2$  equal to  $T_H$ , the inner PLL open loop translates to

$$G_1(s)H_1(s) = B \frac{1}{s} \frac{(sT_2 + 1)}{(sT_1 + 1)} \frac{1}{(sT_H + 1)} = B \frac{1}{s(sT_1 + 1)}, \quad (8)$$

which shows one pole at the origin and one at  $1/T_1$ . For the inner loop, the gain drops with a  $-20$  dB/dec slope and the phase equals to  $-90^\circ$ . The remaining pole can be located around the open-loop crossover frequency of the inner PLL,  $\omega_T$  (the frequency where the open-loop magnitude crosses the 0 dB marker), to obtain a phase margin of  $45^\circ$ . The upper limit for this pole location becomes the HPF bandwidth. Fig. 5 shows the Bode plot for the inner-PLL open loop.

**Outer-PLL Stability Analysis:** As observed, the inner-PLL stability has been checked as standalone feedback system (open-loop case), and as compact unit (closed-loop case) that will function as the divider of the outer PLL. In particular, the latter is critical because the outer-PLL stability analysis requires the inner PLL to be considered in its closed-loop form; that is, the mathematical expressions need the inner PLL to be replaced by its closed-loop transfer-function equivalent. In this work, the outer loop is considered a second-order current-type loop filter is employed and provides two additional time constants,  $T_3$  (pole) and  $T_4$  (zero).

The open-loop transfer function needs (6) for the closed-loop equivalent of the inner PLL. Thus, the required transfer function,  $TF_2(s)$ , is

$$TF_2(s) = \frac{K_\phi K_2}{N} \frac{1}{C_3 + C_4} \frac{1}{s} \frac{(sT_4 + 1)}{s(sT_3 + 1)} \frac{A(sT_2 + 1)}{s(s^2T_1 + s + B)}, \quad (9)$$

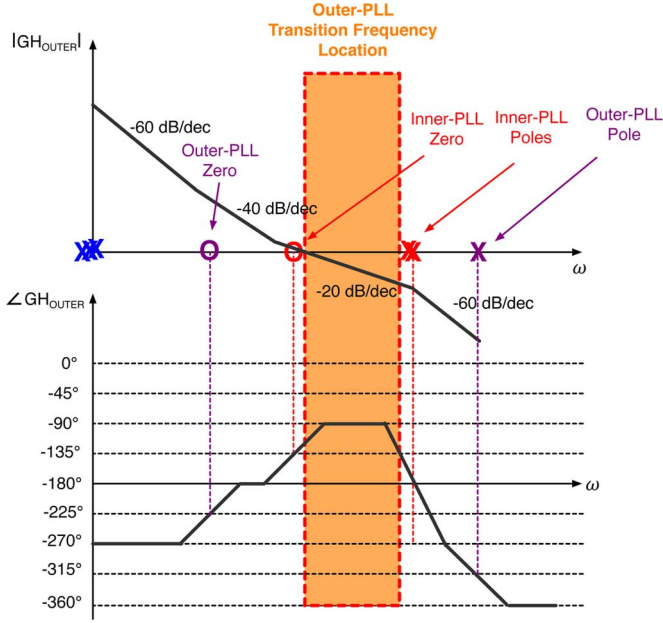


Fig. 6. Outer PLL Bode plot.

where  $K_2$  is the gain of  $VCO_2$  and  $N$  corresponds to the divider. Defining the constant  $D$  as  $K_2 \cdot K_\phi \cdot (1/N)1/(C_3 + C_4)$ , (9) can be simplified as

$$TF_2(s) = A \cdot D \frac{(sT_4 + 1)}{s^3(sT_3 + 1)} \frac{(sT_2 + 1)}{(s^2T_1 + s + B)}, \quad (10)$$

which shows three poles at the origin, one zero at  $1/T_2$ , one zero at  $1/T_4$ , one pole at  $1/T_3$  and a pair of poles that can be complex conjugate depending on the product  $4T_1B$ .

To improve the stability of the whole system, it is required to locate the two zeros before any pole to bring the total phase from  $-270^\circ$  to a value close to  $-90^\circ$ . Hence, since the zero at  $1/T_2$  is already fixed, the zero at  $1/T_4$  must be placed at low frequency (dominant root), and the pole at  $1/T_3$  can be located at high frequency. Fig. 6 shows the optimum range where the outer-loop crossover frequency can be chosen to maintain suitable phase margin.

### B. BRN-PLL Design Guidelines

From Section II-A, it can be observed that the BRN-PLL architecture can be designed using the Nyquist stability criterion in two steps. The inner PLL is addressed first and then replaced with its closed-loop equivalent to design the outer-PLL loop filter.

*Inner-PLL Design Guidelines:* Equation (8) reveals just one pole to locate at the inner-PLL crossover frequency. Since a wideband inner PLL is preferred, while maintaining its treatment as a continuous system, its bandwidth upper limit equals the operating frequency divided by 20 [1].

The pole is placed with respect to the loop bandwidth, since this parameter is equivalent to the passband of the noise transfer functions. Loop bandwidth and crossover frequency are close to each other and related by  $\omega_T \approx \omega_3 \text{ dB}/1.33$  [1].

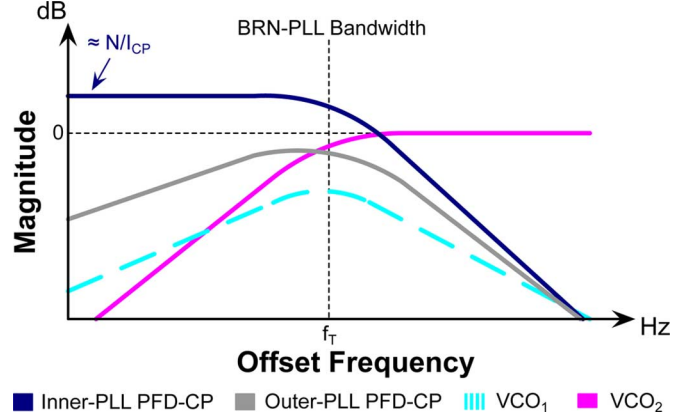


Fig. 7. Theoretical one-side-noise-spectrum PN transfer function for the BRN-PLL scheme.

From the discussion of stability, the location of the HPF pole will be at  $\omega_T$ , while  $\omega_H$  and  $\omega_2$  (which are equal) can be placed a decade before to guarantee a phase margin of  $45^\circ$ .

*Outer-PLL Design Guidelines:* Once the inner PLL is closed, (7) shows the zero at  $\omega_2$  and two more poles, whose nature (real or complex) and location is determined by the constant  $B$ . The value of  $B$  is expected to be a big number since it is inversely proportional to capacitors. Therefore, the two additional poles from (7) will be likely complex conjugate and located in the vicinity of  $1/T_1$ .

Thus from Fig. 6, the zero associated with  $T_4$  can be located as low as two decades below the zero at  $1/T_2$ , while the pole at  $1/T_3$  can be placed as high as two decades above the location of the complex conjugate poles, so that the phase does not drop too quickly. Fine locations for both  $\omega_3$  and  $\omega_4$  will be determined using phase models [14] for trading off peaking in the noise response and fast capture time.

### C. PN Contribution of the BRN-PLL Building-Blocks

The behavior of the BRN-PLL is analyzed for the different noise sources appearing in the scheme. A set of transfer functions can be derived by activating the associated noise source of each building block, one at a time. Following the BRN-PLL design guidelines, it is possible to relate the root locations in terms of one frequency variable (i.e.,  $\omega_2$ ) producing the typical set of Bode plots for the transfer functions observed in Fig. 7.

It can be noticed that only the inner-loop PFD/CP noise shows low-pass transfer characteristics. The passband gain is proportional to the divider value  $N$  (if present) and inversely proportional to the CP current. This behavior is the same as that obtained with a traditional PLL system. On the other hand, the outer-PLL PFD-CP noise gets attenuated at very-close-to-carrier offset frequency, which reduces the input clock noise contribution to the output when compared to cascade-type PLLs.

Fig. 7 shows that the BRN-PLL produces significant attenuation for both the inner-PLL VCO and the input, which implies that cleaning for these two noise sources is effective. Fig. 7 also indicates that the PN around the BRN-PLL bandwidth is determined by the input, inner-PLL VCO and outer-PLL PFD/CP. Their noise contributions depend on the associated passband local maxima. Thus, the CP noise becomes critical for the performance of this clock cleaner. The LOs are selected as a LC

VCO for VCO<sub>2</sub> (for noise-floor performance), and a high- $Q$  LO for VCO<sub>1</sub> (to reduce any *bump* or hard transition between the inner-PLL PFD and the LC VCO). A MEMS-based VCO becomes a suitable candidate for the high- $Q$  LO based on its performance and footprint.

The noise contribution of each block involved in the system is established by means of simulations or measurements. Since PN simulations are required to predict how the system will conform the spectrum of the output signal, the frequency is assumed captured allowing the different blocks to be modeled in terms of how the phase is modified. For this work, *phase models* are used since they provide a quick tool to check how modifications in the different transfer functions are reflected in the output PN [14].

Verilog-A models are preferred to express phase models since the language contains the functions *white\_noise*, *flicker\_noise*, and *noise\_table* that provide several levels of description for the noise of the different blocks. For accurate prediction, the *noise\_table* function is used from measurements. A detailed and complete procedure for each specific block can be found in [14].

### III. PHASE-FREQUENCY DETECTOR AND CHARGE-PUMP DESIGN

Section II showed that the close-to-carrier PN of the BRN-PLL is dominated by the noise of a PFD, which makes it critical for the overall system performance. Since a PFD/CP is used, it can be concluded that the PFD will only set the conditions to enable the required current sources, making the CP current noise the main contribution for the whole block.

The work presented in [15] can be applied to favor the linearity of the PFD/CP using two CPs and a modified *triflop*. The inclusion of a second CP will double the current but also increases the noise, which can affect the performance of the BRN-PLL. Hence, the proposed clock cleaner can be fully exploited if the CP current is increased while the noise effect is reduced.

First, from the theoretical implementation of the CP [13], the current switches are moved to the rails to alleviate direct charge-injection to the output node, and the transistors that implement the current sources will be located next to the output in a cascode configuration. However, it can be noticed that this architecture maintains an active path to the output port, and therefore interaction with their corresponding noise sources.

Therefore, a switching network is located at the CP output to maximize the isolation between the current sources and the loop filter. The switching network monitors N\_UP (negated version of UP) and DN signals and opens the connection anytime the PFD is idle. In the case that the tuning voltage deviates from the desired value due to leakage of the loop-filter capacitors, the loop dynamics will force the PFD to produce the required signal recovering it, which means that the switching network does not interfere with the PLL tracking.

The addition of the switching network needs to take into account the resistance associated with the transistors that implement the required passgate. When the switching network is not included, the interconnection between CP and loop filter is able

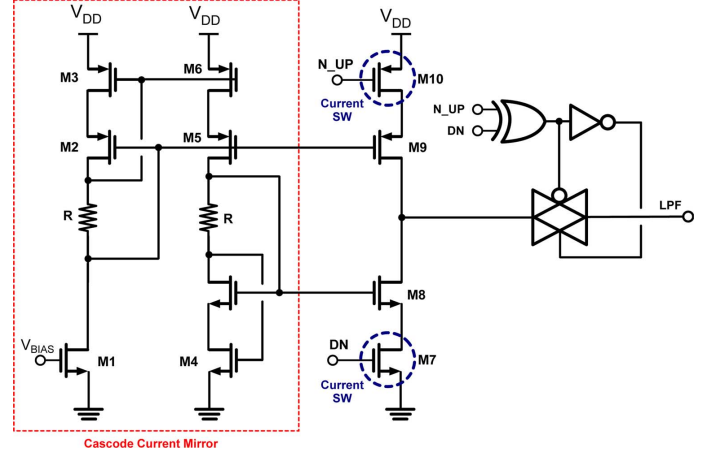


Fig. 8. CP architecture with cascoded current mirror and isolation switching network.

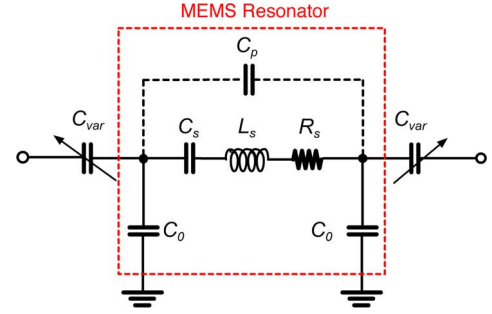


Fig. 9. MEMS resonator equivalent model including the series tuning elements.

to process phase variations with current changes allowing the detection of very small differences between the signals at the PFD inputs. However, when a resistor is placed between the CP and the loop filter, the current-type nature becomes a typical voltage-voltage network and the phase information is then handled as a voltage signal. Therefore, the parasitic capacitances in the interconnection increase the possibility of spurious tones due to perturbations from a dead-band zone. Hence, the switch on-resistance must be minimized without a significant increase in parasitic capacitances that would limit the loop filter bandwidth.

A complementary topology is employed to reduce the on-resistance of the switches without limiting the tuning voltage (i.e., it can swing to the rails). In addition, dummy switches are added to PMOS and NMOS transistors to alleviate charge injection and clock feedthrough. Minimum-length transistors are selected for the switching network to increase the figure of merit [16].

A self-biased cascode current mirror is used to bias the current sources and to account for the stacking of the transistors in the CP. The cascode current reference has a higher output resistance ( $\approx g_m r_{ds}^2$ ) and its theoretical current-gain error is zero, which favors matching of the CP currents [17]. The  $V_{DS}$  of the cascode transistors M8 and M9 are biased at about  $V_{th} - 2V_{ov}$ . When the current reference is interfaced with the CP, an active current switch operates in triode region and establishes source degeneration to improve the linearity. Fig. 8 shows the final implementation of this CP.

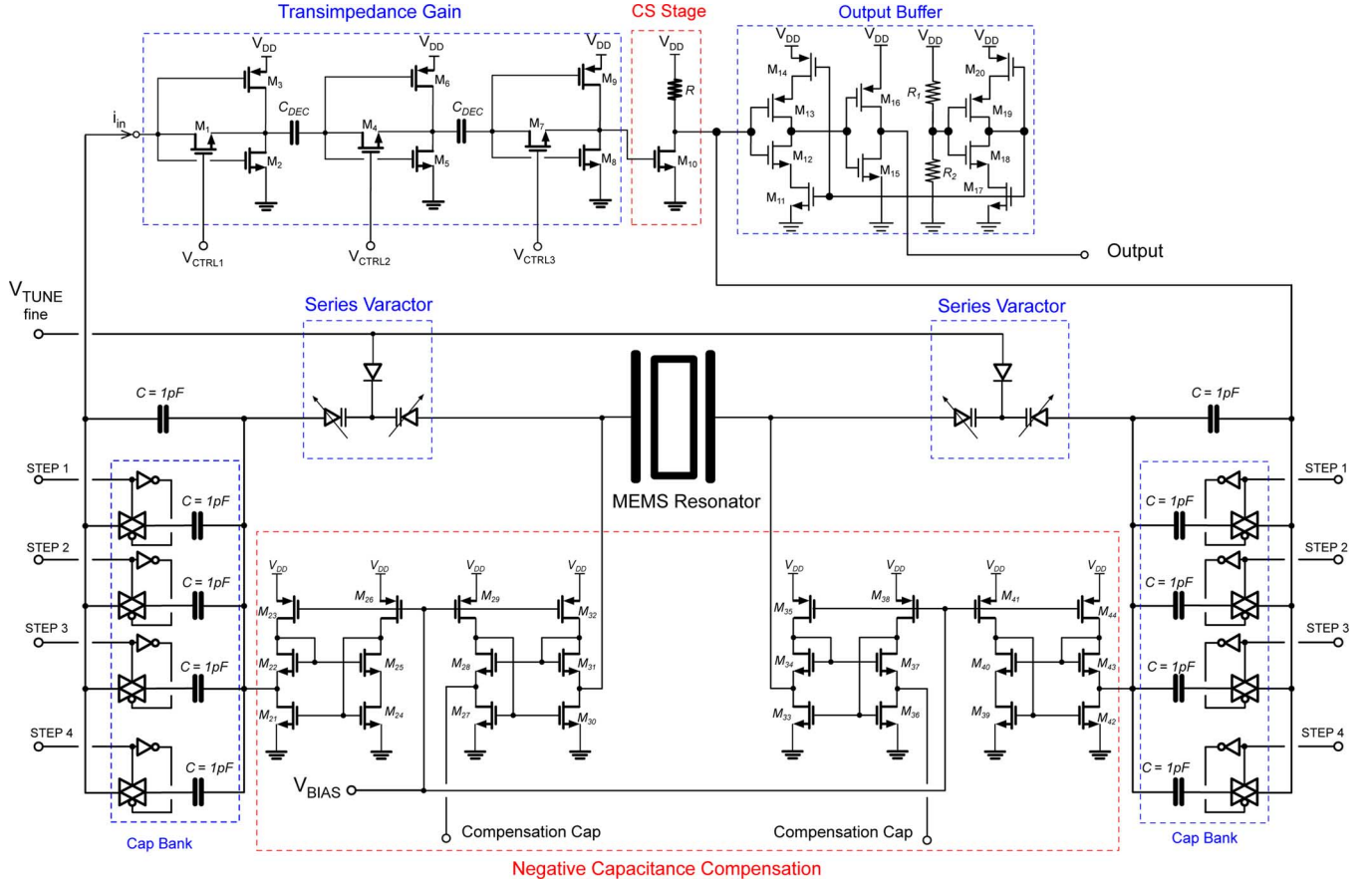


Fig. 10. Block diagram of the MEMS-VCO.

#### IV. MEMS VCO DESIGN

A MEMS VCO uses a micromechanical resonator as its frequency-selecting element, and such device can be modeled as a series RLC tank circuit with parasitic elements [18]. The oscillator is configured when the resonator is interfaced with sustaining electronics in feedback configuration to satisfy the Barkhausen criterion.

The series tank is complemented with the addition of shunt-parasitic capacitances  $C_0$  and  $C_p$  as presented in Fig. 9, where  $L_s$  and  $C_s$  are the resonator motional inductance and capacitance, respectively; while the loss of the device is represented by the motional resistance,  $R_s$ . A tuning mechanism can be obtained when a variable capacitor ( $C_{var}$ ) is placed in series with the MEMS resonator. Thus, the ideal expression for the series-resonance frequency is modified following

$$\omega_s \approx \sqrt{\frac{1}{L_s \frac{C_s(C_0 + C_{var})}{2C_s + C_0 + C_{var}}}}. \quad (11)$$

Equation (11) shows that if  $C_0$  is much larger than  $C_s$  and  $C_{var}$ , the resonance frequency will be practically the same, and the pulling provided by  $C_{var}$  will be minimum. This is in fact the case for piezoelectric devices, where  $C_0$  can be large ( $\approx 1$  pF) due to an increased transduction area for reducing the resonator motional resistance,  $R_s$ .

Negative capacitors can be used to compensate the shunt-parasitic capacitances. A negative component is generated by inverting the relationship between current and voltage through a

negative impedance converter (NIC). Since the resonator emulates a floating node for the series varactors, the NIC can also be used to provide proper biasing for the tuning elements. This condition suggests that the capacitance change can be maximized if the NIC provides low DC voltage for the varactors. The architecture, incorporated in Fig. 10, is based on the *Sooch* cascode current-mirror [19], and it is used for that purpose. Two back-to-back varactors can configure a series-tuning element using the common terminal as tuning interface.

A wideband transimpedance amplifier (TIA) with at least 120 dB $\Omega$  of gain is designed to operate with the series-tuning technique. High gain is required because the insertion loss that the sustaining amplifier needs to overcome is increased by the effect of the series tuning-element. The TIA is comprised of three inverter-based amplifiers (they are implemented with shunt-shunt feedback decoupled from each other through a capacitor  $C_{DEC}$ ), a CS amplifier to provide extra gain (also to introduce an additional 180° phase-shift for MEMS resonators with 0° at the resonance peak), and a comparator to work as a digital buffer (to maintain constant amplitude prior to the PN measurement equipment [20]). The complete schematic for the MEMS VCO is presented in Fig. 10.

#### V. LC VCO DESIGN

The LC VCO is built using a double-switching (DS) pair negative-resistance generator (cross-coupled architecture). The

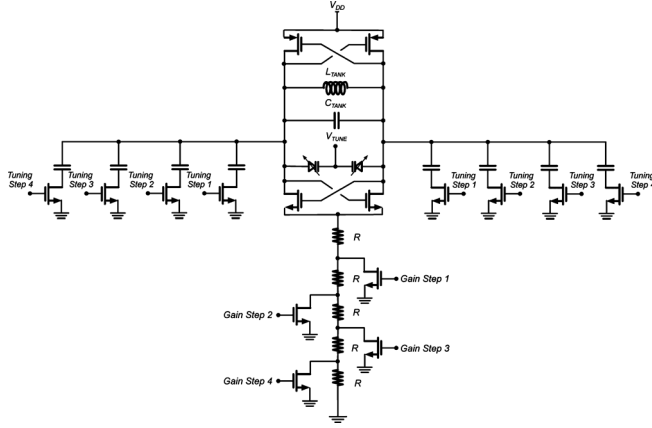


Fig. 11. Architecture for the DS LC-VCO.

tuning scheme is implemented with varactors and discrete frequency steps. Passive biasing is employed to eliminate the noise from the tail current [21]. Fig. 11 shows the LC VCO schematic.

Because each switching pair in this architecture only operates half of the time [22], each switch generates only half as much noise as a single-switching (SS) version. Therefore, the oscillation amplitude of DS LC VCO is twice as large as that of SS LC VCO, which leads to a 6 dB improvement in the PN.

For the operation of the oscillator, either on-chip or off-chip inductors can be used. The operating frequency or the required  $Q$  of the LC VCO will determine the inductor type to use.

## VI. EXPERIMENTAL VERIFICATION OF THE MEMS-BASED BRN-PLL ARCHITECTURE

### A. PFD/CP Characterization

The PFD/CP was fabricated in a  $0.18\ \mu\text{m}$  1P6M CMOS process, and the method used to determine the CP current is based on the characterization of the MOS current with fixed gate voltage.

To use the matching technique of [15], two CP blocks are added to the final implementation producing an estimated current of  $540\ \mu\text{A}$  with a correlation coefficient of 99.9835% between pumping and sinking currents. The self-biased current mirror allows higher correlation coefficient compared to [9] at lower current.

An indirect measurement technique estimating the very-close-to-carrier PN can be employed to compare the performance of PFD/CPs. The noise effect of different CP architectures can be compared using a wideband PLL (a basic loop with no divider) since the passband gains for the input and PFD/CP transfer functions are 0 dB and  $20\log(1/I_{CP})$  dB, respectively.

Using an Agilent E4438C vector signal generator as input source during all the tests, the PN was measured using an Agilent E5500 PN analyzer. As observed in Fig. 12, compared to the performance of the architecture used in [9] ( $I_{CP}$  equal to 1.5 mA), it is observed that the very-close-to-carrier phase noise is improved by approximately 15 dB with  $3\times$  less current, which estimates a total improvement of 23 dB when the switching-network technique is applied.

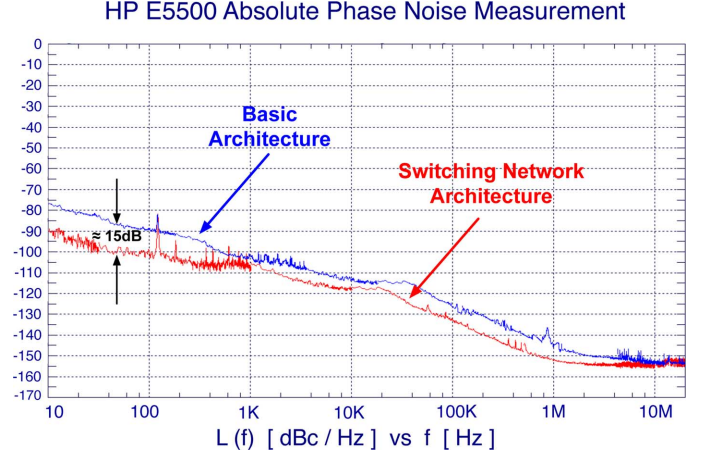


Fig. 12. Measured PN performance of a wide-PLL to analyze the noise performance of the two CP configurations.

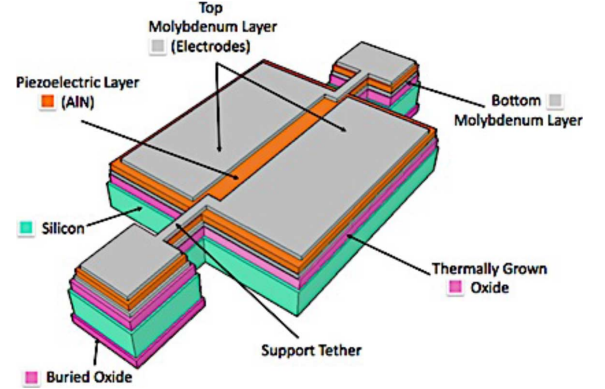


Fig. 13. Schematic of the two-finger design composite AlN-on-Si MEMS resonator illustrating the material layers of the composite stack.

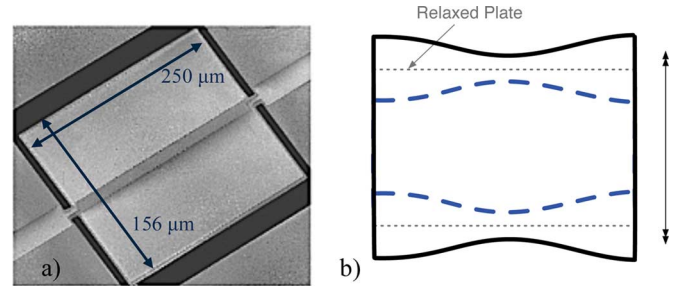


Fig. 14. (a) SEM image of the AlN-on-Si resonator used in this work. (b) Representation of the length extensional (LE) resonance-mode shape.

### B. VCOs Characterization

A composite aluminum-nitride-on-silicon (AlN-on-Si) laterally vibrating microresonator is employed for the MEMS VCO. The resonator stack composition and thicknesses are  $9/2/0.1/1/0.1\ \mu\text{m}$  of Si/SiO<sub>2</sub>/Mo/AlN/Mo, respectively. The design utilized is a two-finger electrode configuration on top of a plate with lateral dimensions of  $156\ \mu\text{m} \times 250\ \mu\text{m}$  [23]. Details of the composite material stack are shown in Fig. 13, while Fig. 14(a) shows an SEM image of the device. Details of the resonator low-temperature fabrication process are described in [24].

The two-finger electrode configuration excites and senses a length extensional (LE) mode at 26 MHz with  $0^\circ$  phase shift at resonance. The shape of the excited mode is presented in

## MEMS-VCO PN Performance

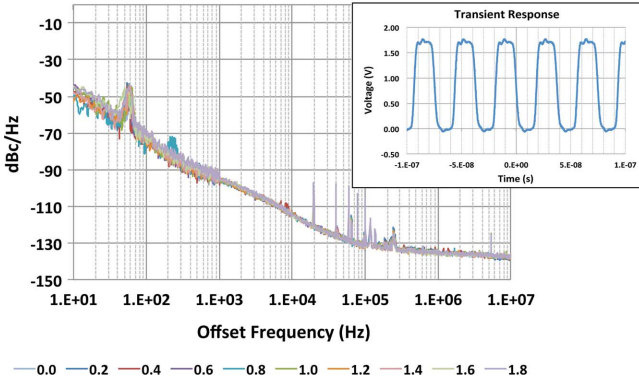


Fig. 15. PN performance for the MEMS VCO using the series-tuning technique.

Fig. 14(b). The outline corresponds to the peak displacement of each half cycle of oscillation.

Device characterization is performed using an Agilent E5071C vector network analyzer (VNA) with 50  $\Omega$  terminations. The measured  $Q$  and motional resistance of the resonator in air are 3 628 and 1 831  $\Omega$ , respectively.

The sustaining amplifier for the MEMS VCO was fabricated in a 0.18  $\mu\text{m}$  1P6M CMOS process. Considering Fig. 10, setting a discrete step and varying only the on-chip varactors, the measured tuning range is 11.183 kHz (450 ppm) with a minimum effect in the PN (Fig. 15). For this work, the MEMS-VCO tuning follows an electronic strategy only.

Transient response shown in Fig. 15 indicates that is possible to have noise folding due to the hard limiting of the amplitude causing noise folding at higher frequency offsets [25], [26]. The effect of noise folding can be assuaged when the LC-VCO becomes the dominant noise source defining the noise floor.

On the other hand, for the LC-VCO, the decision of using an on-chip or an off-chip inductor is determined by the intended operating frequency of the clock cleaner. Since the goal is to demonstrate the operation of a MEMS-based clock cleaner, the reduction of the noise level due to the divider becomes the main design criterion. Thus, the use of an off-chip inductor is preferred so that the divider value can be reduced. Although the inductor is placed off-chip because of its value, this selection adds two advantages to the LC-VCO. First, the off-chip inductor saves area on the IC die, and second, the expected  $Q$  of the LC-VCO will be higher than that using an on-chip passive [27]. Hence, trading off inductor value,  $Q$  and operating frequency, a 330 nH off-chip inductor is chosen, which sets the divider value to 4 and the cleaner output frequency to 104 MHz. The measured PN of the DS LC-VCO is compared with a prediction using Leeson's model [28] in Fig. 16. Tuning based on varactors is an effective way to modify the operating frequency, and a total tuning range of about 949.5 kHz is measured using an Agilent E4407B spectrum analyzer (for a single step of discrete tuning).

It is important to notice that it is possible to integrate the inductor as the operating frequency of the cleaner is increased. Keeping a low divider value is possible since MEMS devices working at the GHz range are possible [29].

## LC VCO PN Performance

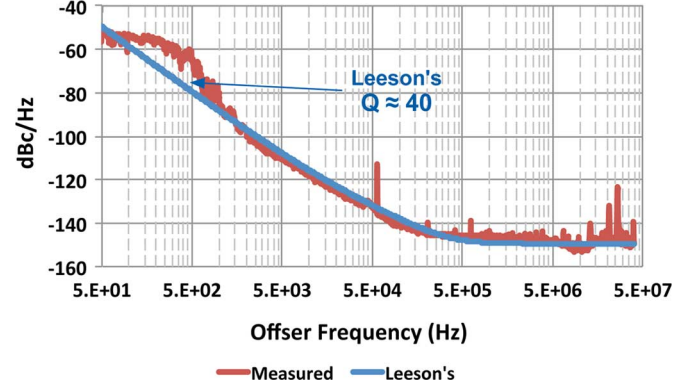


Fig. 16. Measured LC-VCO PN performance.

TABLE I  
DESIGN PARAMETERS FOR INNER-PLL (MEMS-VCO)

Parameter	Value
Operating Frequency	26 MHz
Charge-pump Current	540 $\mu\text{A}$
VCO Gain ( $K_V$ )	6.2128 kHz/V
Divider Value	1
3dB Bandwidth	90 kHz
$f_1 (\omega_1)$	650 kHz
$f_2 (\omega_2)$	65 kHz
$f_H (\omega_H)$	130 kHz
$C_1$	1 pF
$C_2$	9.5 pF
$R_2$	235 k $\Omega$
$R_H$	10 k $\Omega$
$C_H$	10 pF

## C. BRN-PLL PN Performance

Using the guidelines of Section II, the inner PLL is designed first. Although a wideband loop is desired, due to the small value for  $K_1$ , the capacitances for the filter are extremely small to be realized with practical components. Therefore, a trade-off between the element values and bandwidth is required for this case. For the given design parameters, the value of the passives for the inner-PLL filters are summarized in Table I.

Stability of the inner PLL shows the expected 45° phase margin for closing the loop and passing the system to the outer PLL.

The selection of a divide-by-4 block to interface the signal from the LC VCO eases its implementation using D flip-flops in feedback configuration because it is a power-of-2 divider.

The PN profiles of the MEMS and the LC VCOs can be used to determine a suitable BRN-PLL bandwidth. Fig. 17 indicates that a cut-off frequency in the offset-frequency range from about 2 kHz to 50 kHz can provide a smooth transition for the output-signal PN. Notice that proper location of the outer-PLL roots with respect to the already set inner-PLL poles and zeros will control any peaking in the PN response. Since the relation between peaking in the noise behavior and capture time is inversely proportional, the locking process can be long when the PN performance is designed to avoid hard transitions between

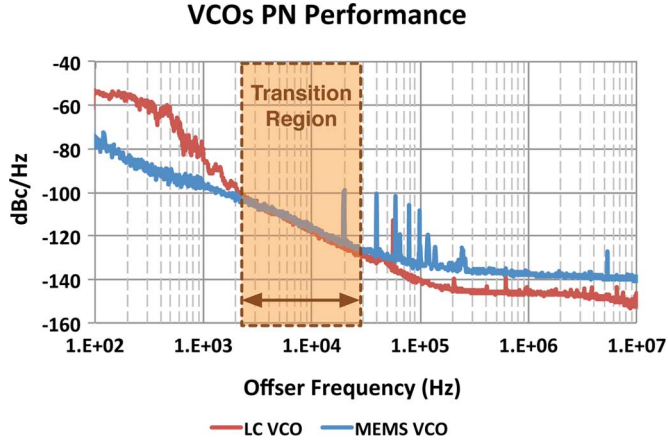


Fig. 17. Optimum offset-frequency range for the BRN-PLL transition.

TABLE II  
DESIGN PARAMETERS FOR OUTER-PLL (LC-VCO)

Parameter	Value
Operating Frequency	104 MHz
Charge-pump Current	540 $\mu$ A
VCO Gain ( $K_2$ )	527.5 kHz/V
Divider Value	4
3dB Bandwidth	35 kHz
$f_3$ ( $\omega_3$ )	65 kHz
$f_4$ ( $\omega_4$ )	1.1 kHz
$C_3$	4.5 nF
$C_4$	0.25 $\mu$ F
$R_4$	500 $\Omega$

the different noise sources. From Section II and the required design parameters, the values of the passive components for the outer-PLL filter are summarized in Table II.

Fig. 18 shows the chip and the test setup as an evaluation board allowing the connection of different filters of the scheme. The input source is an Agilent E4438C vector signal generator, and the Agilent E5500 PN analyzer system is used to determine the PN performance of the BRN-PLL.

The different PN profiles for the building blocks that comprise the BRN-PLL are extracted, and phase models are generated to simulate the total PN of the proposed clock cleaner. The testing of the total BRN-PLL shows proper capture process and zero steady-state phase error. The measured PN performance is included along to the simulation results in Fig. 19. A good agreement between prediction and measurement is observed, and the output PN profile has the expected slopes.

## VII. CONCLUSION

Fig. 19 reveals that the performance of BRN-PLL is capable of filtering the input signal properly and replace its contribution with that of the inner-PLL PFD/CP. The introduction of a notch in the reference signal TF have shown that the bandwidth of the nested architecture can be extended and therefore the size of loop-filter capacitors can favor IC integration. Although not included here, strategies for further enhancing system integration such as dual path filtering can be explored and implemented [3].

With respect to the results presented in [9], the PN performance is comparable, even when the MEMS-based scheme con-

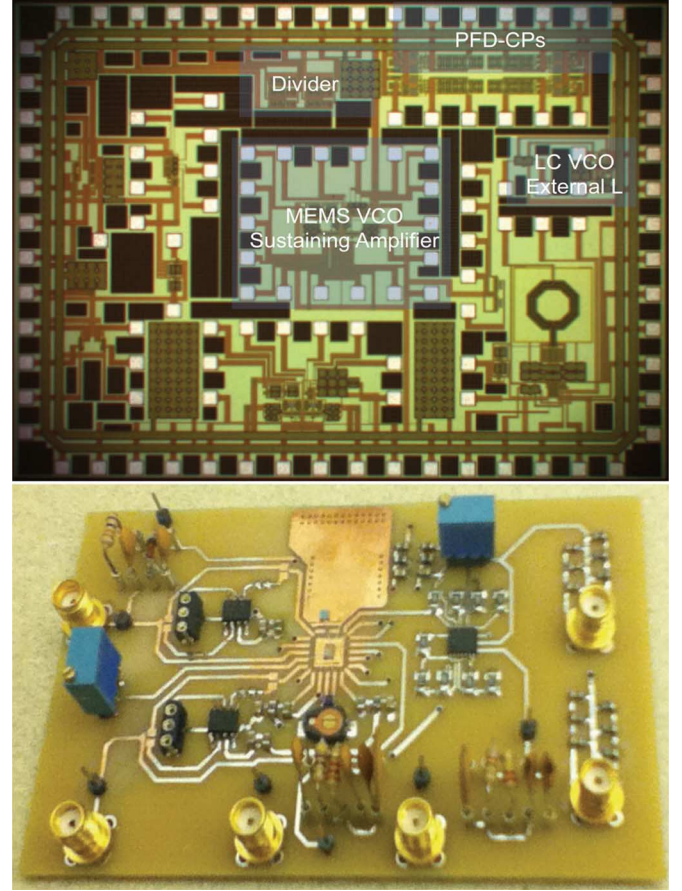


Fig. 18. Chip and test setup for the MEMS-based BRN-PLL.

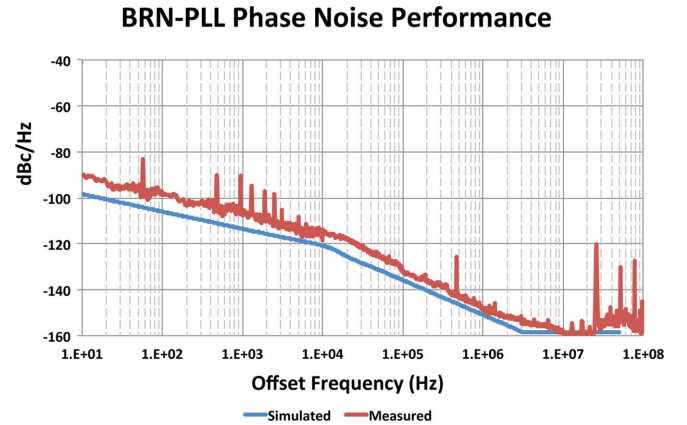


Fig. 19. Measured performance the MEMS-based BRN-PLL.

tains a divide-by-4 block that increases the noise by about 12 dB. Hence, it can be concluded that the utilization of a MEMS VCO in a BRN-PLL clock cleaner can effectively shape the transition region in the PN response, and its very-close-to-carrier contribution is further improved by the attenuation from the corresponding transfer function. The BRN-PLL scheme takes full advantage of a high- $Q$  MEMS oscillator.

As commented, a lower  $K_1$  can be selected to restrict the inner-PLL bandwidth. Increasing the tuning range of the MEMS VCO can provide two beneficial effects for the BRN-PLL when used with caution. First, a larger VCO gain leads to a wider loop bandwidth with realizable on-chip filter-component values. Second, the MEMS VCO itself can compensate deviations of

the resonance frequency due to fabrication variations of the MEMS device without the need to change the divider value. In particular, alternative fabrication techniques for MEMS devices are already available that increase the operating frequency and can eliminate the divider in the BRN-PLL. Modern fabrication strategies like the ones described in [30], [31] can also reduce the PVT variations due to the MEMS resonator itself. Further deviations in the expected operating frequency can be addressed with schemes based on fractional dividers that provide the required compensation, for example using look-up tables.

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