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Recent Advances in System-Level Interconnect Prediction

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CAS President

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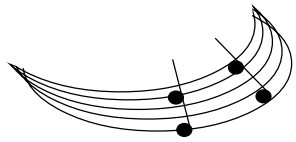
Thanks for the Memories...



Well, the moment has arrived. This is the final issue of the *IEEE Circuits and Systems Society Newsletter*.

44, 11, 952

Numerically, this is the 44th consecutive number in the current series of eleven volumes, with the first number coming into being eleven years ago in March 1990. In terms of pages, this eleven-year run began at 16 per issue, expanded to 24 per issue eight years later, on the occasion of the passing of Sidney Darlington, rose to 32 per issue just four numbers later, and finally jumped to 48 per issue in December 1999, the issue marking the Society's Golden Anniversary. Cumulatively that is 952 pages, the last nine numbers being in full color.

An Appreciation

We have many, many people to thank at this time. Here in the editor's office, where we have for these eleven years produced the *IEEE Circuits and Systems Society Newsletter* by means of desktop publishing, we wish to acknowledge our associates over the years, without whom these pages would not have come to be. The opening mention goes to Julia Jordan, who got the project off the ground. Thank you, Julia. We are indebted also to Joanne Birdsell, managing editor in Notre Dame's Engineering Graphics and Publications Office, who helped us out from time to time early on, when we experienced transitions of one sort or another. Susan Larsen, a wizard with Pagemaker, and Martha Van Overberghe, who also helped with the Society budget, were with the Newsletter for a year or two, and both participated in the development of the publication style. We appreciate all that they did along the way. Finally, we give a very heartfelt special thanks to Eric Kuehner, who has been with us as we went to a new level, tripling the number of pages and introducing full color.

At the IEEE end of things, we wish to express our sincere appreciation to Bob Smrek, whose office receives our films and interfaces with the printer to produce very high quality issues and see them off to the CAS members all around the world. Thanks so much, Bob, to you and your staff.

And it all started with Tony Michel, who asked me one day if I would like to take on another challenge in editing. Tony and I had worked together on the *IEEE Transactions on Automatic Control*, during one of my five years as Editor there. Thanks for asking, Tony....

A seminal role has been played by Rui de Figueiredo, who contacted me in the Fall of 1997 to say that the Society wanted to begin publishing technical articles in the Newsletter, to expand in an orderly manner and eventually to seek the conversion of the Newsletter into a Magazine. This was a most challenging goal; and it has led to some of the most interesting editorial experiences that I have ever had. I am deeply indebted to Rui for all his help, his advice, his ideas, and his direct participation in all steps of this process. We would not be where we are without Rui, who along the way became an official Features Editor for our Newsletter. Thank you, Rui.

Another special thank you goes to Ron Chen, who wrote the cover article in that March 1998 issue, our first technical article. Over these last three years, Ron has written in several different ways on the pages of our Newsletter, displaying a most enjoyable versatility, whether writing a meeting report, a book review, or a newsletter article. Also accepting a post as Features Editor, Ron has worked hard behind the scenes on behalf of our readers, even during his leave-of-absence time when others would have declined.

Early on in the Newsletter evolution, we were joined by Shlomo Karni, who is the creator of the 'Umble Ohm. This regular cartoon has lent a very human side to all our more mundane efforts to publish news and articles. Thank you Shlomo for those many, many images. We are happy to say that we have in hand another 'Umble Ohm for the first issue of the forthcoming Magazine!

For a couple of years we were able to run a most unusual crossword puzzle with technical hints. Thanks for this effort go first to Pat Sain and Cheryl Schrader, and then to Pat who continued on for a time after Cheryl graduated. Once again, little worldly advantage accrued from this effort, but we are aware of quite a number of folks who used to work those puzzles.

We have come to believe that it takes a very community oriented CAS member to write for the Newsletter. The whole purpose of the Newsletter is to make information available to everyone in the Society. Much of this type of writing is nontechnical in nature, and will not score many points with one's supervisor as an item on the resume. The situation is even more critical for an article of technical nature. On the one hand, the way to write for a general audience is quite different from the way to write for, say, a transactions. Of course the benefit is a much, much larger audience. On the other hand, many of our superiors would discourage even listing a Newsletter article in one's list of activities during the year, for various reasons which we can all recite.

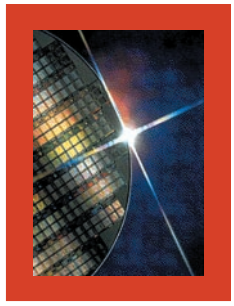
We have during these eleven years been fortunate indeed to encounter many CAS members who were community oriented enough to write for the Newsletter, with virtually no recompense other than that of knowing that they were serving the Society. In honor of these persons we have prepared a special list of credits, which appears on Page 29. You all know who you are, everyone from Society officers to chapter members. We feel most truly indebted to each and every one of you. Thank you so much for participating when we were "only" a Newsletter.

And so it is time to lead the caterpillar into its cocoon, from which it will emerge next quarter, in 2001, as *IEEE Circuits and Systems Magazine*. This metamorphosis was finally approved last June in Vancouver at the TAB meetings.

We hope that each of you who participated in the Newsletter these eleven years will feel very much a part of the Magazine, for indeed you have been such a part. Thanks again for the memories....

Michael K. Sain, Editor-in-Chief

Recent Advances in System-Level Interconnect Prediction



Abstract—*The exciting, new field of System-Level Interconnect Prediction emerged from research of the early 1970's but it took until 1999 before a cohesive research community for interconnect prediction was established. New research results are becoming available and the last couple of years have brought both more interest and more progress in the field than in the thirty years before. This paper is an introduction to the field and provides an overview of some of the recent advances in system-level interconnect prediction.*

Introduction

As mainstream processors surpass gigahertz global clock frequencies and new design and process technologies enable even higher performance, much attention is directed toward managing the influence of interconnects in deep submicron designs. Today, interconnects are the limiting factor for both performance and density, *i.e.*, the value and the cost of the VLSI system.

Guided by better models of interconnect performance at the atomic and grain levels of structure and at multi-gigahertz operating frequencies, we adopt new process technologies (e.g., reverse-scaled copper wires, low-permittivity dielectrics). Effects previously considered unimportant become significant (e.g., mutual inductance), and previously reasonable approximations (e.g., lumped-capacitance gate load models) become useless.

Due to these trends, chip planning and layout tools must embrace new paradigms. System-level interconnects must be treated as distributed RLC lines with embedded repeaters. Wiring layer assignment, e.g., based on statistical models of the system interconnect structure, becomes critical.

Today, a focal point for improved interconnect modeling, more cost-effective system architectures, and more productive design technology centers on new methods and models for *system-level interconnect prediction*. Although basic works in this area are almost thirty years old, no cohesive research community for interconnect prediction was established until the First International Workshop on System-Level Interconnect Prediction [1] in April 1999. A collection of recent research work in the System-Level Interconnect Prediction field can be found in a special issue of *IEEE Transactions on VLSI Systems* [2]. In 2001, the SLIP Workshop will be held for the third time and a new special issue of *TVLSI* is planned.

This paper aims at introducing the field of System-Level Interconnect Prediction and at providing an overview of recent research work in this new and exciting area. The next section starts with an introduction on *a priori* interconnect prediction and the

Dirk Stroobandt*

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importance of Rent's rule, the basis for all modeling. The third section gives an overview of wirelength estimation models and provides a common framework for such models. In the last section applications of wirelength estimations are presented.

A Priori Interconnect Prediction and Rent's Rule

The Computer-Aided Design (CAD) tools for placement of logic gates in a circuit optimize for small interconnection lengths between gates. This requires knowledge of the interconnect routing. Routing, on the other hand, can only be done after the place of the gates is known. Hence, during the layout of computer chips, several iterations between placement and routing are needed. To reduce or even eliminate the number of placement/routing iterations, *a priori* estimations of interconnection lengths are very helpful because they allow an evaluation of placements without a routing step, leading to a better initial placement and a better initial routing result. CAD tools for layout generation therefore could benefit from *a priori* (*i.e.*, pre-layout) wirelength estimation techniques.

Current applications of *a priori* interconnect estimation are found in technology extrapolation [3], e.g., the International Technology Roadmap for Semiconductors (ITRS) [4]. For estimations of the performance of future designs, very little is known about the design and *a priori* techniques are essential. The same applies to the evaluation of new computer architectures. *A priori* estimates immediately provide

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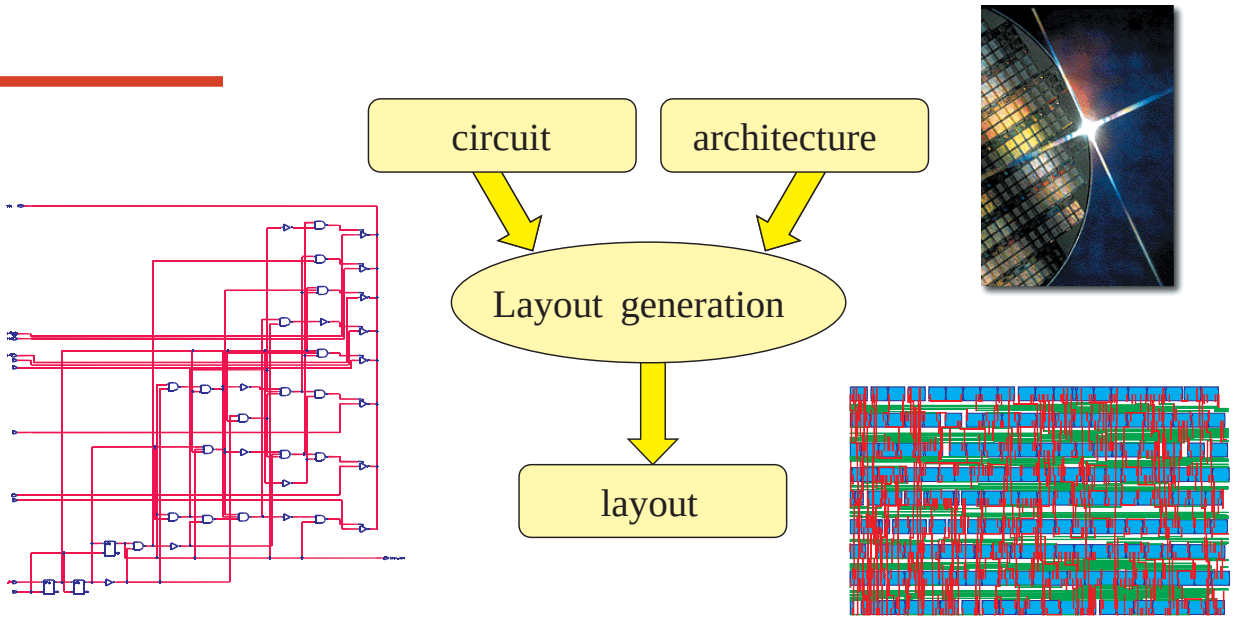

Figure 1. The three components of models for physical design: the circuit, the architecture and the layout generation. The combination of these models results in the (model for the) layout.

Current practice models the circuit as a collection of logic gates connected to each other through interconnections, models the architecture as a (two-dimensional) Manhattan grid, and assumes a "good" placement (*i.e.*, one that successfully minimizes wire lengths) and enough space available to route all interconnects along the shortest (Manhattan) path. However, these simple models do not suffice to make powerful estimations about the resulting layout. For this, one needs to have a notion of (i) the complexity of the interconnection topology and (ii) the quality of the placement. This information is provided by the so-called Rent's rule.

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a solid ground for drawing preliminary conclusions about the benefits of new architectures and for comparing different architectures to each other. These applications are discussed in the last section.

A priori interconnect estimation typically requires three models (Fig. 1): (i) a circuit model (ii) a model for the physical architecture the circuit will be placed in, and (iii) a model for the layout generation (placement and routing). Current practice models the circuit as a collection of logic gates connected to each other through interconnections, models the architecture as a (two-dimensional) Manhattan grid, and assumes a "good" placement (i.e., one that successfully minimizes wire lengths) and enough space available to route all interconnects along the short-

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In 1971 Landman and Russo [5] described a relationship between the average number of terminals ***T*** of a part of the circuit (a *module*) and the average number of logic gates (basic logic blocks ***B***) inside the module. This relation is given by

$$T = t\,B^{p} \qquad (1)$$

and is called *Rent's rule*. The parameter ***t*** is the average number of terminals per logic gate and the exponent ***p*** is the *Rent exponent*. Its value depends on the complexity of the interconnect topology (with higher values for more complex topologies) and on the quality of the placement (with higher values for less placement optimization). The maximal value of the Rent exponent ***p*** is **1** for a very complex topology or a random placement [6]. Rent's rule proves to be valid for most designs and it is recently shown that it applies to any homogeneous design [6]. Rent's rule has also been extended for heterogeneous systems in [7, 8]. Figure 2 shows the result of a circuit partitioning in a log-log plot of number of terminals versus number of logic gates. The validity of Rent's rule follows from the fact that all points follow—on average—a straight line in the plot.[1] With Rent's rule, sufficiently accurate

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[1] The deviation from the straight line for high values of ***T*** and ***B*** is known as Rent's region II and has been described in [5, 11]. Another deviation at the low end is described in [12].

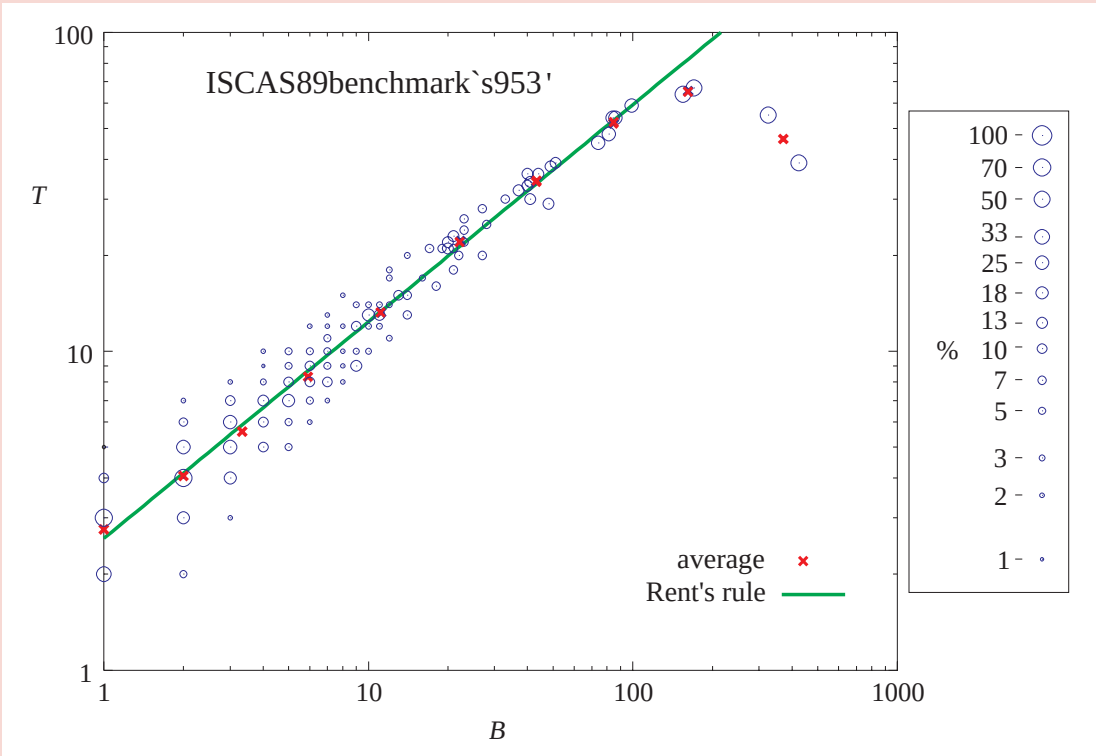

Figure 2. Rent's rule: number of terminals per module **T** *versus number of gates per module* **B** *during the partitioning of a benchmark circuit (ISCAS'89 [9] benchmark 's953') with the* 'ratiocut' *partitioning method [10]. The size of the circles corresponds to the percentage of modules (on a total number of modules around an average number of gates, at equal distances in the log-log plot) that has* **B** *gates and* **T** *terminals.*

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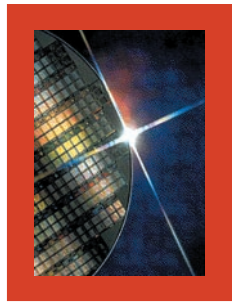

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estimates of interconnection lengths can be made.

In the remainder of this paper the use of Rent's rule for wirelength estimation is described. Some direct applications of Rent's rule include:

- estimation of the number of terminals to aid circuit partitioning [13];
- generation of benchmark circuits [14–17].

Wirelength Estimation

Donath's Model

Rent's rule has been used for wirelength estimation for the first time by Donath in 1979 [18]. The idea is simple: the circuit is partitioned hierarchically into equally large parts (see Fig. 3(a); four parts in each hierarchical step). The Manhattan grid is partitioned as well in a symmetrical way (Fig. 3(b)) and each circuit part is mapped to a grid part. This partitioning process is repeated recursively until all logic gates are assigned to a single grid cell in the Manhattan grid. The average number of interconnections between parts at a certain hierarchical level is estimated from Rent's rule (details can be found in [18]) and the average length of a connection at each hierarchical level is estimated by assuming that source and destination cells are uniformly distributed over the grid part for that hierarchical level (Fig. 4). This placement model ensures that shorter interconnects (at deeper hierarchical levels) will outnumber longer ones (due to the use of the hierarchical model together with Rent's rule) but keeps the placement of cells within a hierarchical part simple (random).

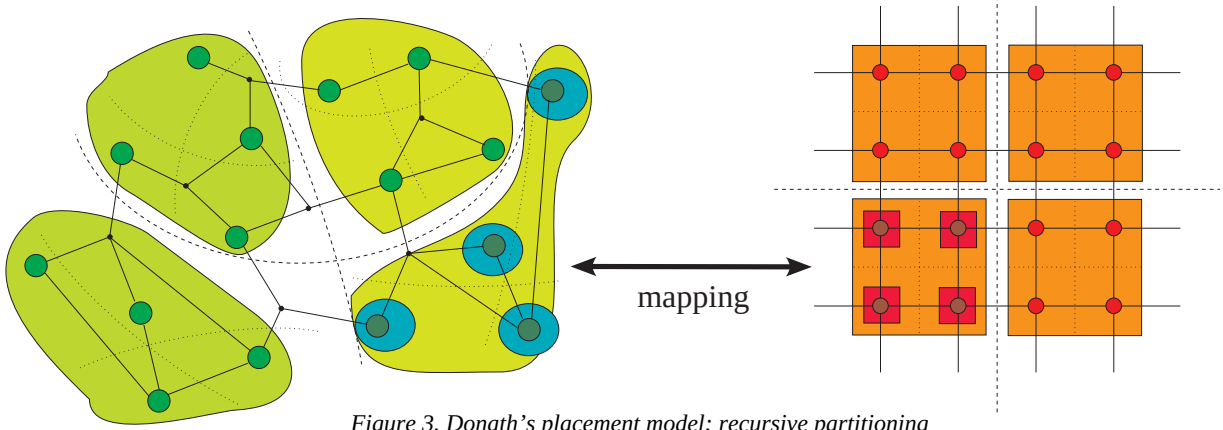

Figure 3. Donath's placement model: recursive partitioning of both circuit (a) and Manhattan grid (b) and mapping of circuit parts to grid parts.

Despite the simplicity of Donath's

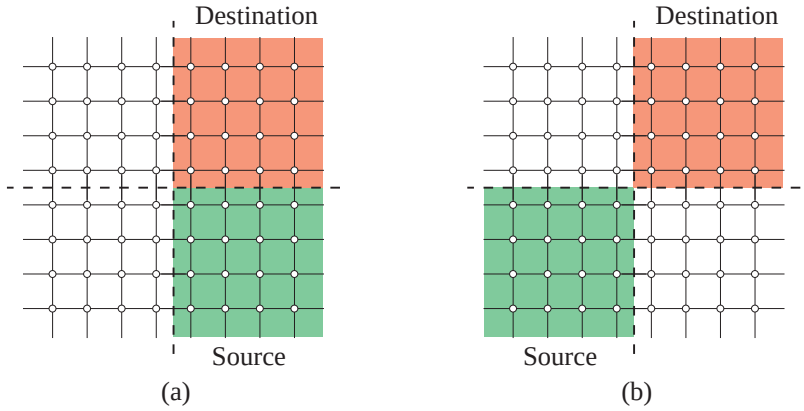

Figure 4. The average length on a hierarchical level is estimated by assuming that source and destination cells are uniformly distributed over the grid cells within the partition. We distinguish adjacent combinations *(a) and* diagonal combinations *(b).*

model, it is able to predict the scaling of the average wirelength as a function of circuit size quite well. Figure 5

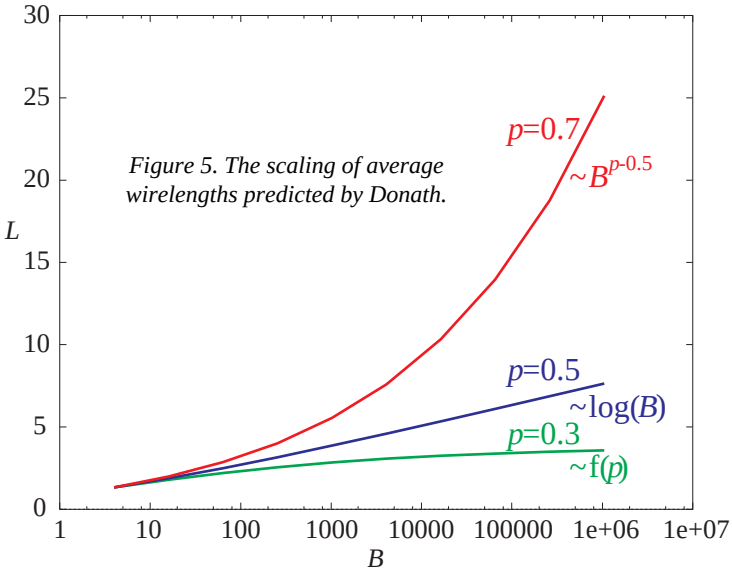

Figure 5. The scaling of average wirelengths predicted by Donath.

shows that circuits of low complexity (**$p < 0.5$**) result in an average wirelength that converges to a constant value (depending on the value of the Rent exponent) for large circuits. The average wirelength of circuits of average complexity (**$p = 0.5$**) scales with the logarithm of the circuit size and for complex circuits the average wirelength increases without bounds for increasing circuit sizes. This result has also been observed for real circuit placements. However, Donath found that his quantitative average wirelength predictions were approximately a factor of 2 off from measured values for real circuits, as can be seen from Fig. 6.

Introducing the Occupying Probability

In [19, 20] Stroobandt *et al.* attributed the discrepancy between Donath's model and real results to the uniform placement of source and destination cells within a hierarchical level. Indeed, a good placement will try to place connected gates closer to each other and hence will favour the placement of source and destination cells closer to the border between connected hierar-

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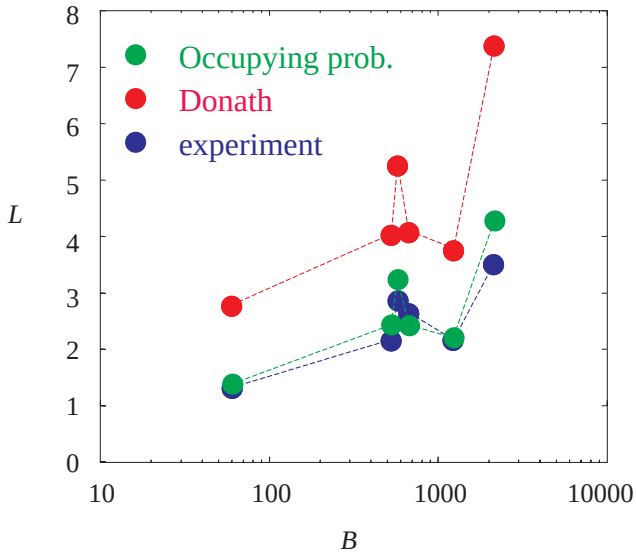

Figure 6. Donath's average wirelength estimates and estimates considering the occupying probability versus measurements on actual circuit designs.

The use of the third dimension, especially with the introduction of optical links, leads to anisotropic systems. Third dimension interconnects have different properties (possibly larger latency, lower interconnection density requiring detours, possible limitation of the minimal distance in the third dimension, ….).

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chical parts, as in Fig. 7. To model this, they separate the wirelength distribution into two parts [20, 21–23]: (i) a *site density function* that enumerates all possible paths between all possible cell pairs in the Manhattan grid [24, 25] and (ii) an *occupying probability* that assigns a probability of occurrence

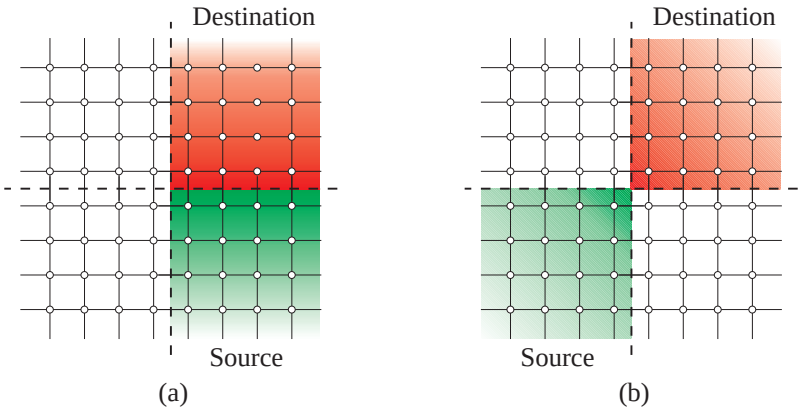

Figure 7. Placement of source and destination cells according to a probability distribution (darker regions have higher probability) for adjacent (a) and diagonal (b) combinations.

to each of the possible paths [20]. With Donath's assumption of uniform cell placement within a hierarchical level, this occupying probability is a constant but the actual occupying probability is a decreasing function of path length. Based on theoretical arguments and Rent's rule [20], it is found to be proportional to ℓ^{2p-4} where ℓ is the interconnection length. The results of this improvement on the average wirelength are shown in Fig. 6. Figure 8 shows the difference in the entire wirelength distribution between Donath's estimates and the ones using the occupying probability and compare both to an actual wirelength distribution for a placed design.

Independently, Davis *et al.* [26] proposed a non-hierarchical method for wirelength estimation that uses Rent's rule on Manhattan circles (diamonds) around each gate. This results in a more accurate occupying probability that can be approximated by ℓ^{2p-4} and hence leads to very similar results as in [20]. A more detailed analysis of different wirelength models can be found in [6].

Other Model Extensions

The introduction of three-dimensional computer systems has induced the need to extend the wirelength estimation models to three-dimensional

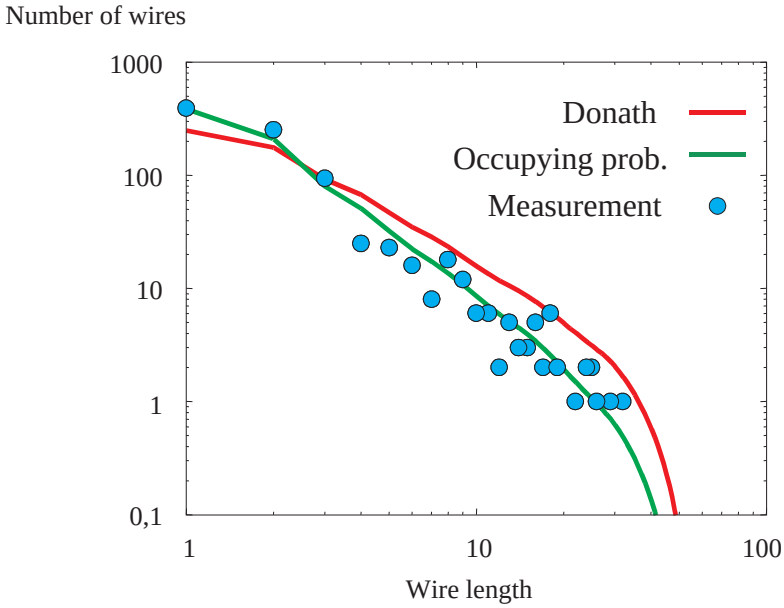

Figure 8. Donath's wirelength distribution and the distribution with probability function versus actual measurements for a placed circuit.

grids. An initial extension of Donath's model was presented by Masaki and Yamada [27]. The occupying probability for three-dimensional systems was introduced in [28] and Davis' technique has been extended to 3D in [29]. The use of the third dimension, especially with the introduction of optical links, leads to anisotropic systems. Third dimension interconnects have different properties (possibly larger latency, lower interconnection density requiring detours, possible limitation of the minimal distance in the third dimension, etc.). Extensions to include issues for anisotropic systems have been presented in [30, 31] and were mainly used to evaluate opto-electronic three-dimensional anisotropic systems [32–35].

Other extensions include taking into account external interconnections [36] and multi-terminal nets [37, 38] and estimating the global wirelength distribution (for heterogeneous systems-on-a-chip) separately [8].

Applications of Wirelength Estimation

Up to now, the most common application of *a priori* wirelength estimation was found in methods and tools to predict the performance of future circuits. The wirelength estimation methods are used to estimate the average interconnection length in the critical path model for determining the attainable operating frequency [39–43]. An interesting project has been developed at UCLA where the MARCO GSRC Technology Extrapolation (GTX) system [3] provides a robust, portable framework for interactive specification and comparison of modeling choices

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Unlike previous "hard-coded" systems such as [40, 41, 43], GTX adopts a paradigm wherein *parameters* and *rules* allow users to flexibly capture an essentially unbounded space of attributes and relationships that are germane to VLSI technology and design. User-defined rules can be composed in numerous ways to define *rule chains*, which are then executed by a *derivation engine* to perform studies.

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(e.g., for predicting system cycle time or power dissipation). Unlike previous "hard-coded" systems such as [40, 41, 43], GTX adopts a paradigm wherein *parameters* and *rules* allow users to flexibly capture an essentially unbounded space of attributes and relationships that are germane to VLSI technology and design. User-defined rules can be composed in numerous ways to define *rule chains*, which are then executed by a *derivation engine* to perform studies. The results can then be plotted by the *graphical user interface* (Fig. 9). A similar use of wirelength prediction techniques can be found in the analysis of process yield [44].

Other uses of wirelength estimation models combine the resulting estimations (which represent the required routing resources) with models for available routing resources (considering routing efficiencies, loss of space due to power and ground wires, and the impact of vias) [42, 45–47]. This combination allows one to predict the number of wiring layers needed for given technological layer parameters or, if this number is fixed, to decide whether or not the design will be routable (prior to any layout step!). Accurate estimates of routing demand and supply could also be used to guide layout tools to promising solutions (wire planning). One can also optimize the characteristic layer parameters for

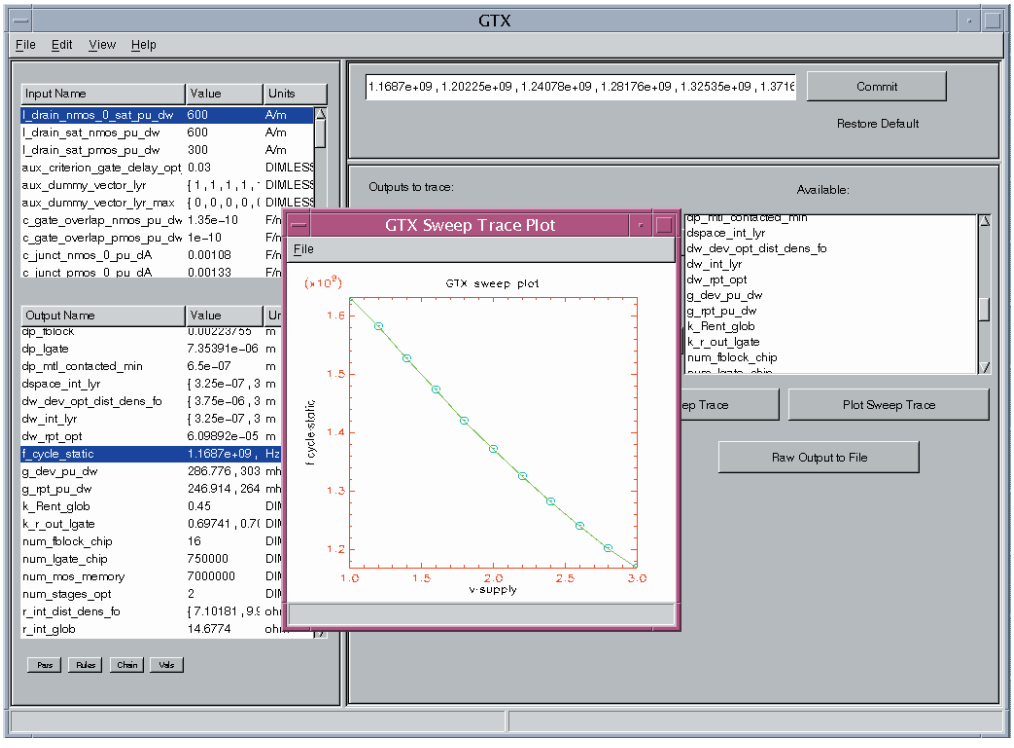

Figure 9. Graphical user interface of the GTX system [3].

Level Interconnect Prediction

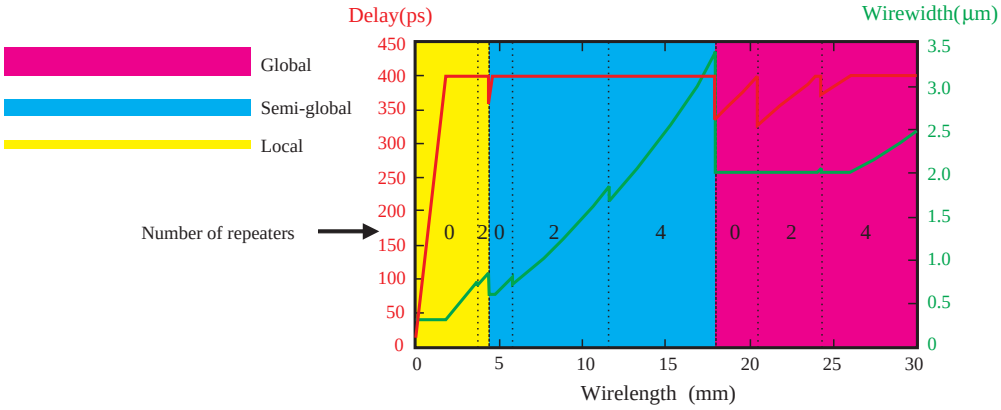

Figure 10. A typical example result of the layer assignment method of [48].

future designs (number of layers, wire width and pitch per layer, …). For this, a layer assignment model is needed. In [48] an optimal layer assignment scheme is searched for by taking into account (i) the optimal wire width, number and size of the repeaters for each wire on each possible layer; (ii) the requirement to meet consistent stage delay constraints for all wires; (iii) a total repeater area constraint; and (iv) the impact of vias on routing. The method minimizes the number of layers needed and returns the optimal width for each wire and the number and size of the repeaters that have to be used. The method can also easily handle different delay constraints on different wires, *i.e.*, a 2-D distribution of wire lengths and required wire performances.

Figure 10 shows a typical result for a layer stack with local, semi-global and global wiring layers [48]. For the shortest wires, a minimum-sized wire at the local layers is sufficient to meet the delay constraint. Once the constraint is reached (in this case the constraint was set to 400 ps), the wire width increases as the length increases. At some point it is beneficial to add repeaters.[2] For longer wires a semi-

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The layer assignment method allows an interesting study of the optimal layer stack. The authors of [48] confirmed that the traditional monotonic layer stack with wide wires (global wires) on top performs much better than a uniform layer stack (all layers are equal). A more interesting result shows that a non-monotonic layer stack sometimes performs even better.

[2] For the reported result, the number of repeaters was limited to an even number to allow the use of inverters.

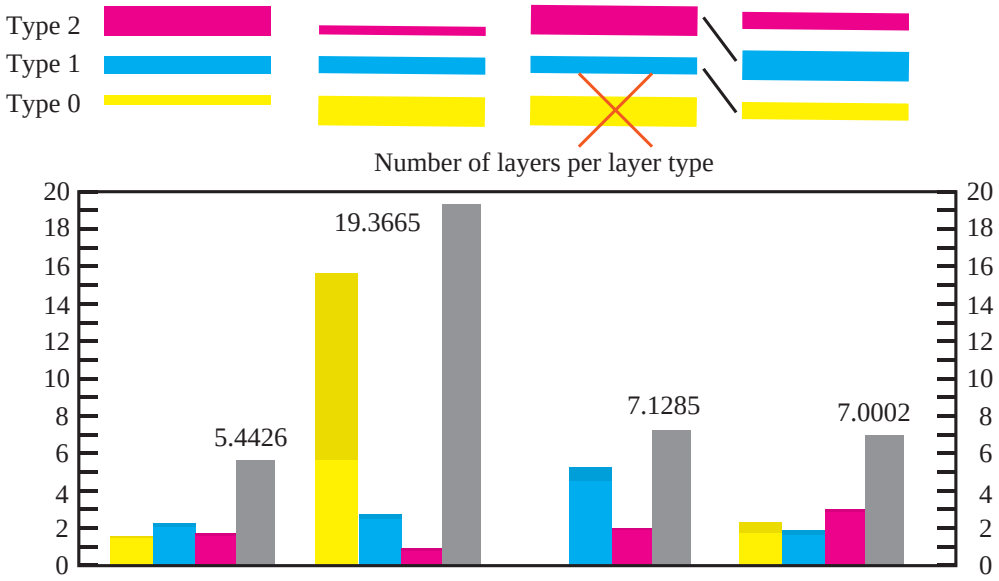

Figure 11. Results for different wiring layer configurations: number of layers needed for each layer type (corresponding colors) with darker colors representing the space lost due to the via impact. The total number of layers needed for each combination is represented in grey.

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global layer is needed and for the longest wires only the global layers are sufficient.

The layer assignment method allows an interesting study of the optimal layer stack. The authors of [48] confirmed that the traditional monotonic layer stack with wide wires (global wires) on top performs much better than a uniform layer stack (all layers are equal). A more interesting result shows that a non-monotonic layer stack sometimes performs even better. In Fig. 11 four layer stacks are evaluated. The first one is the traditional approach, the second one is its inverse (local layers on top). Clearly, this layer stack is less optimal in terms of number of layers needed than the original one, mainly because of the huge via impact on the lower layers. We can also investigate non-monotonic layer stacks such as the third one, which has a global layer type on the bottom and a "conventional" layer stack on top of that. As could be expected, the bottom type is not used at all. This indicates that the conventional approach is indeed better. However, a conventional layer stack with a local layer type at the top (last stack in Fig. 11) does not result in a vacant top layer. Indeed, the results show it is beneficial to move some of the wires to the top layers! Note, however, that the difference in total cost is small.

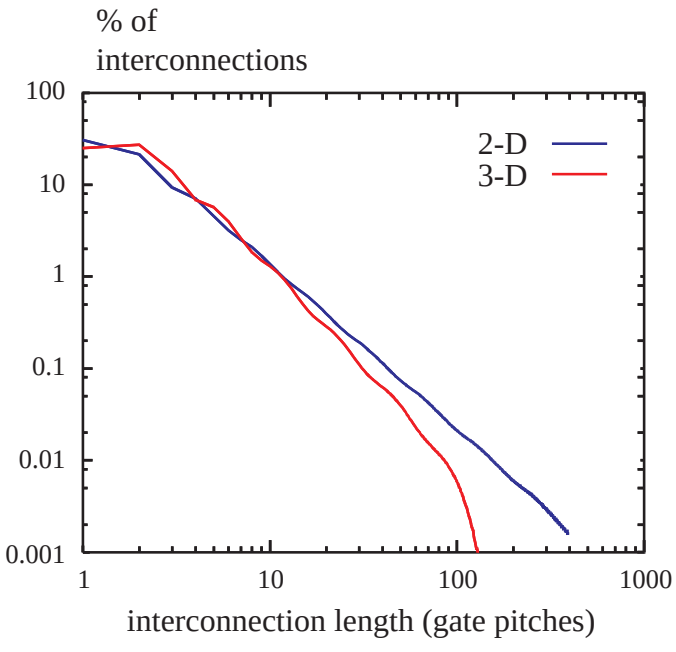

Figure 12. Wirelength distribution for three-dimensional and two-dimensional architectures.

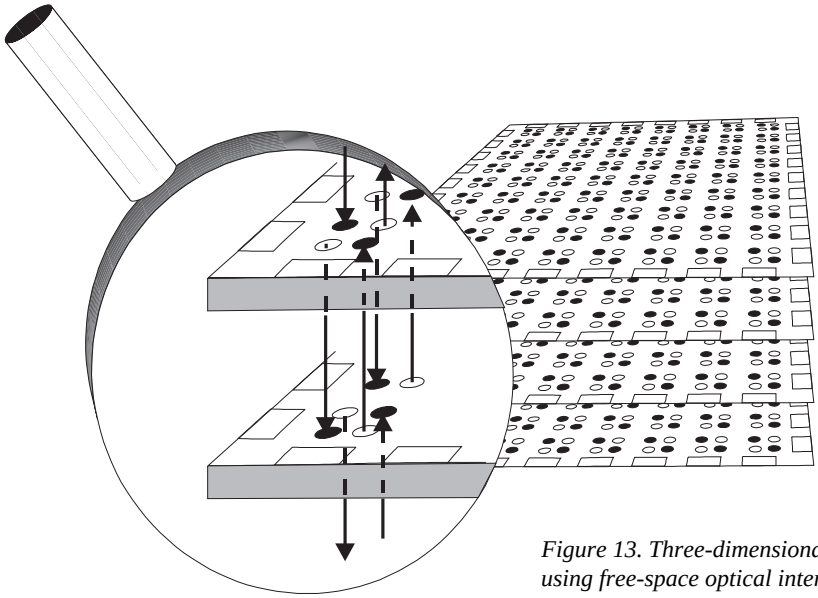

Figure 13. Three-dimensional chip layout using free-space optical interconnections.

A last example of the use of *a priori* interconnect prediction is the evaluation of new computer architectures [49], especially three-dimensional opto-electronic architectures. Since such architectures are not yet available, their possible benefits have to be quantified by predictive techniques. Results show [28, 29, 33, 35, 50] that three-dimensional systems (*i.e.*, where the gates are placed on a three-dimensional grid) have significantly lower wire lengths than two-dimensional systems (Fig. 12). The connections in the third dimension could be implemented as optical links as in Fig. 13. Whatever the implementation, it is likely that the third dimension interconnects will behave differently from their two-dimensional electrical counterparts. Therefore, a cost has to be included in the predictions.

A last example of the use of a priori interconnect prediction is the evaluation of new computer architectures [49], especially three-dimensional opto-electronic architectures. Since such architectures are not yet available, their possible benefits have to be quantified by predictive techniques. Results show [28, 29, 33, 35, 50] that three-dimensional systems (*i.e.*, where the gates are placed on a three-dimensional grid) have significantly lower wire lengths than two-dimensional systems (Fig. 12). The connections in the third dimension could be implemented as optical links as in Fig. 13. Whatever the implementation, it is likely that the third dimension inter-

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Dirk Stroobandt

It took thirty years for research on system-level interconnection prediction to mature but significant progress has been made in the last couple of years. We have introduced the field and the models that are the basis for wirelength prediction: Rent's rule and Donath's wirelength estimation model. Recent advances have been highlighted and we have reviewed some of the applications of *a priori* interconnect prediction, notably technology extrapolation, wiring layer assignment and the evaluation of three-dimensional opto-electronic systems. In each of these applications, system-level interconnect prediction techniques allow the *a priori* estimation of interconnection lengths and resource demands for interconnects.

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connects will behave differently from their two-dimensional electrical counterparts. Therefore, a cost has to be included in the predictions. Such anisotropic three-dimensional architectures have been evaluated in [30, 35] and the benefits quantified as a function of the cost of the third dimension interconnects (see Fig. 14).

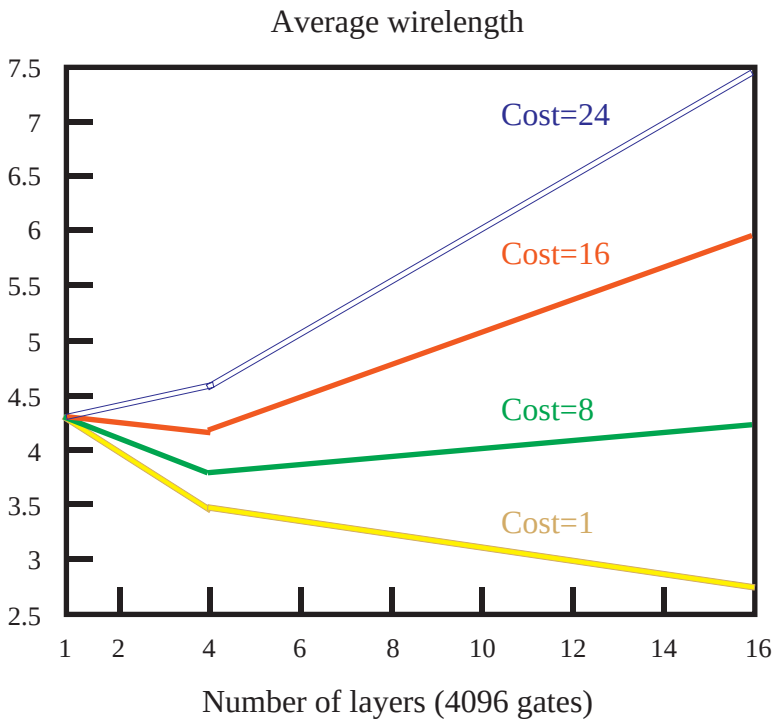

Figure 14. Average wirelength as a function of number of layers and the cost of the third dimension interconnection. For higher costs, the optimal number of layers (for minimal average length) decreases.

Based on the results from the interconnect length prediction analysis, an opto-electronic demonstrator has been built as part of a European project [35, 51]. A prototype is shown in Fig. 15.

Conclusions

It took thirty years for research on system-level interconnection prediction to mature but significant progress has been made in the last couple of years. We have introduced the field and the models that are the basis for wirelength prediction: Rent's rule and Donath's wirelength estimation model. Recent advances have been highlighted and we have reviewed some of the applications of *a priori* interconnect prediction, notably technology ex-

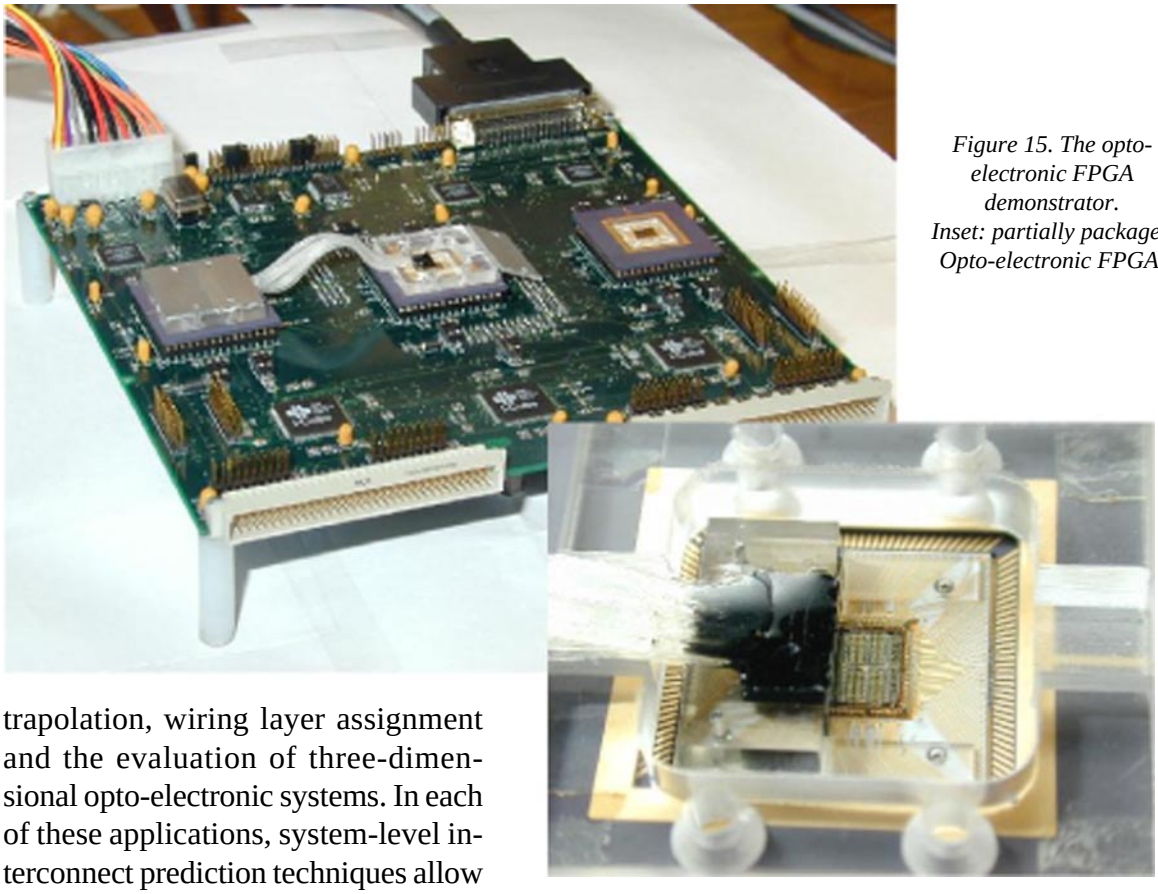

Figure 15. The opto-electronic FPGA demonstrator. Inset: partially packaged Opto-electronic FPGA.

trapolation, wiring layer assignment and the evaluation of three-dimensional opto-electronic systems. In each of these applications, system-level interconnect prediction techniques allow the *a priori* estimation of interconnection lengths and resource demands for interconnects.

In summary, system-level interconnect prediction will be enabling tomorrow's convergent system-level design and hand-off to physical implementation. The field provides a key bridge between process technology, system architecture, and design tools. The references in this paper provide a unique view of the state-of-the-art in system-level interconnect prediction. We hope that they will inspire many researchers to increase their efforts in this important research domain.

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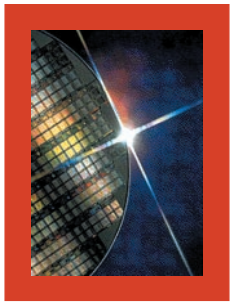

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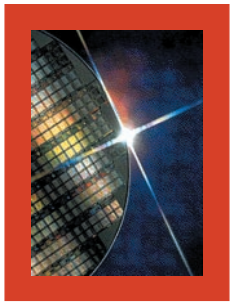

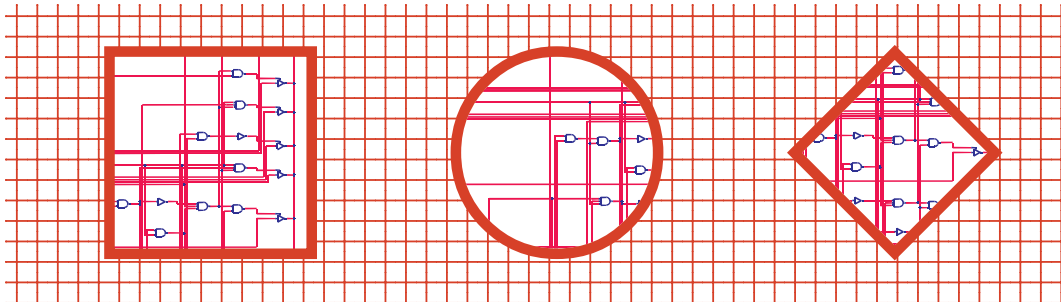

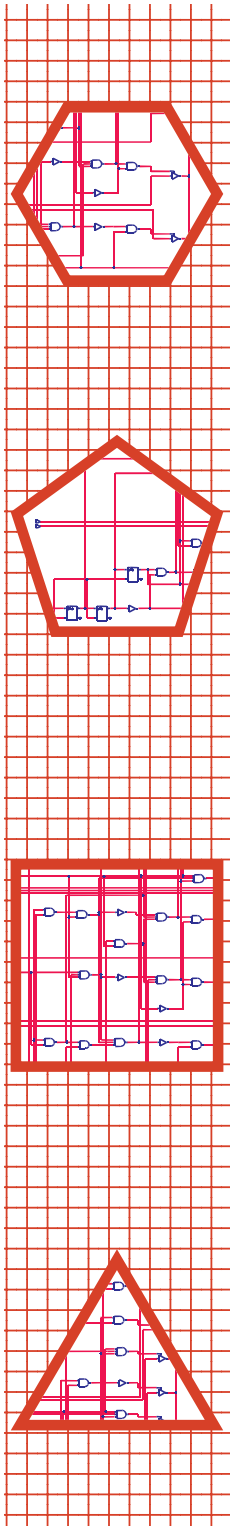

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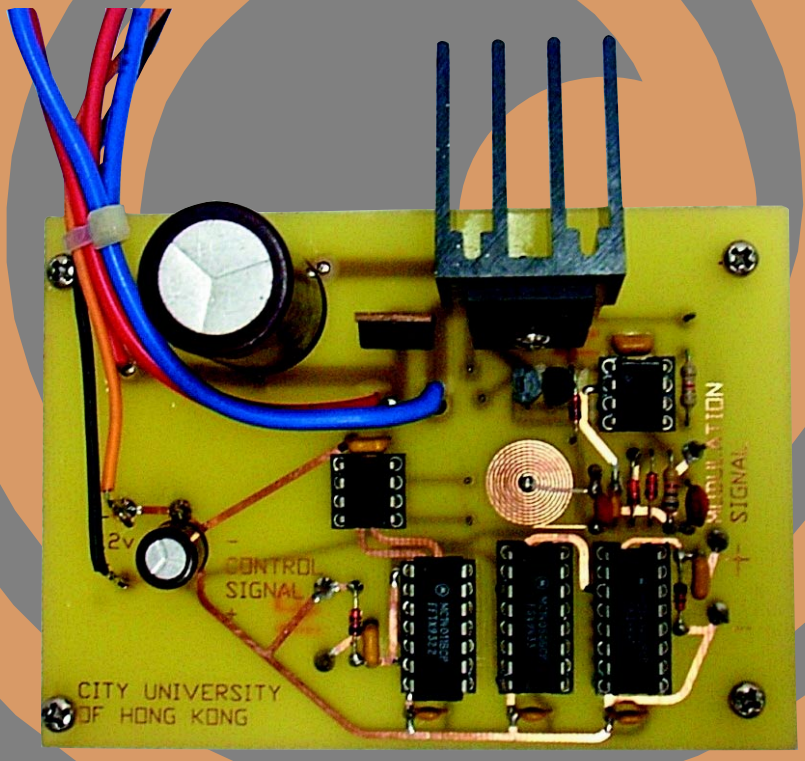
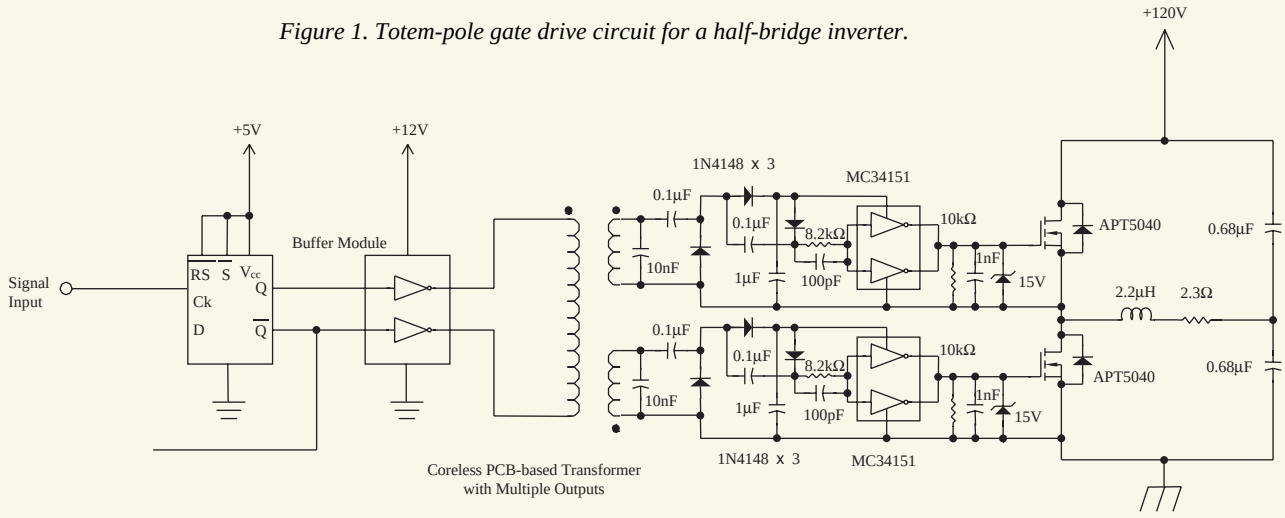
Addendum on CORELESS PRINTED CIRCUIT BOARD (PCB) TRANSFORMERS—



FUNDAMENTAL CHARACTERISTICS AND APPLICATION POTENTIAL

S. Y. (Ron) Hui *S. C. Tang* *H. Chung*

Figure 1. Totem-pole gate drive circuit for a half-bridge inverter.



Since the article [1] on coreless PCB transformers was published in the last *IEEE Circuits and Systems Newsletter*, many inquiries about the details of their applications have been received. This supplementary article is a collective response to these inquiries.

PCB Laminate Thickness

In our research, we use standard FR4 PCBs. Nominal thickness of standard PCB is: 0.4mm, 0.6mm, 0.8mm, 1.0mm and 1.5mm. For the gate drive circuits for power mosfets and IGBTs, we use PCB with thickness of 1.5mm. For power transfer applications such as power transformers for power converters, we use PCB with thickness of 0.4mm. The choice of thickness depends on the applications. The magnetic coupling of coreless PCB transformers increases if the PCB thickness (*i.e.*, the distance between the two printed planar transformer windings) becomes smaller. For signal transfer with low power involvement, a standard PCB of 1.5mm is acceptable. However, for high power transfer, using thin PCB is more appropriate because it offers higher magnetic coupling than thick PCB. In general, we use standard low-cost PCB with 1 ounce copper/sq. ft. for low-power applications. The results obtained so far are based on low-cost PCBs. However, we are now studying coreless PCB transformers for power transfer applications using PCB with 3 ounce copper/sq. ft.

Power Electronic Gate Drives

We have compared the core-based and the coreless approaches in some applications. An example is the totem pole gate drive circuit shown in Fig. 1. The same circuit has been tested with

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We have compared the core-based and the coreless approaches in some applications. An example is the totem pole gate drive circuit shown in Fig. 1. The same circuit has been tested with both core-based transformer and coreless transformer [2].

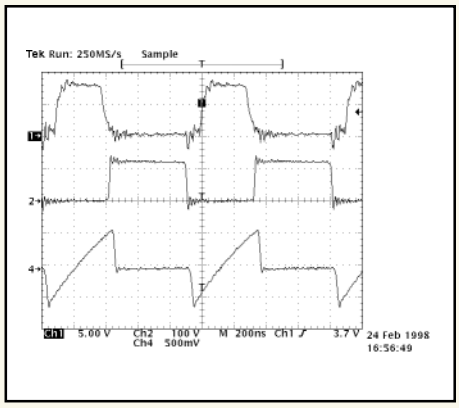

Figure 2a. Measured switching waveforms using ***core-based*** *transformer at 1.1 MHz.*
Top trace: Gating Signal (5V/div)
Middle trace: Drain-source voltage (100V/div)
Bottom trace: Drain current (5A/div)

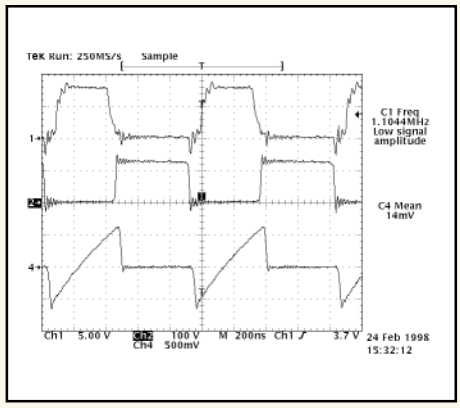

Figure 2b. Measured switching waveforms using ***coreless*** *transformer at 1.1 MHz.*
Top trace: Gating Signal (5V/div)
Middle trace: Drain-source voltage (100V/div)
Bottom trace: Drain current (5A/div)

PCB Transformers Addendum… continued from Page 23

both core-based transformer and coreless transformer [2]. Figure 2a and Fig. 2b show the measured results of the ***core-based*** and ***coreless*** approaches, respectively. Essentially, there is no major difference in the gate drive performance in both cases. This is a good indication that the coreless approach is as good as the core-based approach in some existing applications. Figure 3 shows the PCB of the control and gate drive circuit for a neutral-clamped 3-level power inverter motor drive system that has 12 power switches. This PCB contains 12 gate drives and thus 12 coreless PCB transformers. Despite the notorious noise problems in motor drive environments, this control PCB has been working reliably for over 2 years [3].

At high frequency operations, the shortcomings of core-based transformers (such as frequency limits, core saturation and core losses) could become limiting factors for their applications. The advantages of coreless PCB transformers over their core-based counterparts become more obvious when the operating frequency increases.

Other Application Potentials

It is envisaged that coreless PCB transformers can replace core-based transformers in some industrial applications. At high frequency operations, the shortcomings of core-based transformers (such as frequency limits, core saturation and core losses) could become limiting factors for their applications. The advantages of coreless PCB transformers over their core-based counterparts become more obvious when the operating frequency increases. There are many other aspects of coreless PCB transformers or similar structures to be explored. For example, when fabricated on dielectric materials, the coreless printed windings can form part of an integrated circuit structure. Coreless

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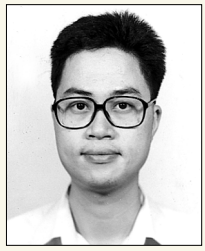

H. Chung

PCB transformers can also be printed on flexible PCBs. The primary and secondary planar windings need not be printed on the same PCB. Thus, the coreless PCB transformer technology may be potentially useful for smart card applications because both energy and signal (information) can be transferred to the smart card integrated circuits. The potentials and limitations of coreless PCB transformers deserve more investigation.

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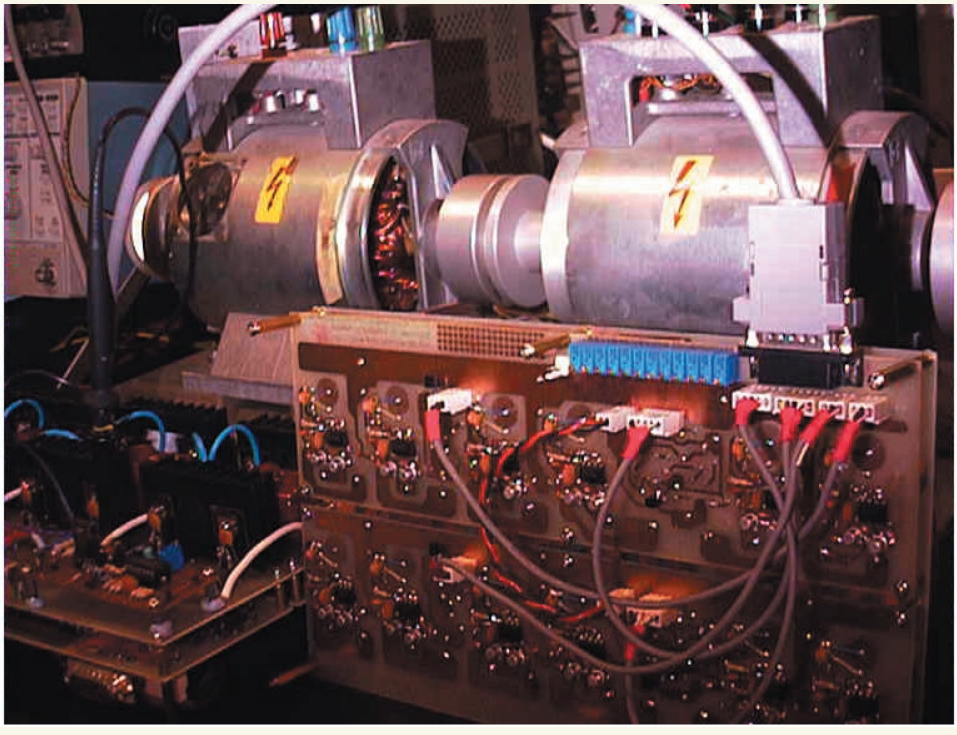
Figure 3. Picture of the control PCB for a neutral-clamped 3-level power inverter motor drive system. (The PCB has 12 coreless PCB transformers for 12 gate drive circuits.)



St. Petersburg

Figure 1. Dom Uchenyh (House of Scientists) - Conference venue.

Control of Oscillations and Chaos:

Report of the 2nd International Conference

The emerging field of controlling chaotic behavior of complex systems attracted increasing attention during the last decade, from both control experts and general audiences. Although the theme of controlling chaos and oscillations has been well represented in the programs of several major conferences related to nonlinear dynamics and control systems during recent years, common interest in the theme has been so strong that conferences where control of complex behavior would be the main topic were still strongly demanded. The first such international conference, entitled "Control of Oscillations and Chaos" (COC'97) took place in St. Petersburg, Russia, in 1997. It attracted about 200 participants from more than 30 countries (for more details, see http://www.ipme.ru/coc97.html). Because of the success of COC'97, it was decided to organize the second such conference three years after, also in St. Petersburg. Thus, the 2nd International Conference "Control of Oscillations and Chaos" (COC 2000) took place in St.Petersburg on July 5–7, 2000. It was organized by the Institute for Problems of Mechanical Engineering of the Russian Academy of Sciences, St. Petersburg State University, and the St. Petersburg Informatics and Control Society, and co-sponsored by the IEEE Circuits and Systems Society, the International Union of Theoretical and Applied Mechanics (IUTAM), the Russian Academy of Sciences and the Russian Foundation for Basic Research, along with technical co-sponsorship of the IEEE Control Systems Society and the Russian IEEE Section. Various problems related to analysis, synchronization and control of complex oscillatory dynamical systems, with emphasis on both theory and applications, were presented and discussed. Many papers from different scientific fields (mathematics; physics; mechanics; chemistry; mechanical, electrical and civil engineering; biology; economics; and so forth) were presented and published in the conference proceedings.

About 180 papers were selected by the International Program Committee from among 210 submissions for inclusion in the final conference Program. More than 170 participants, including 68 speakers from outside of Russia, registered. A total of 7 plenary, 9 semi-plenary, 96 regu-

Russia

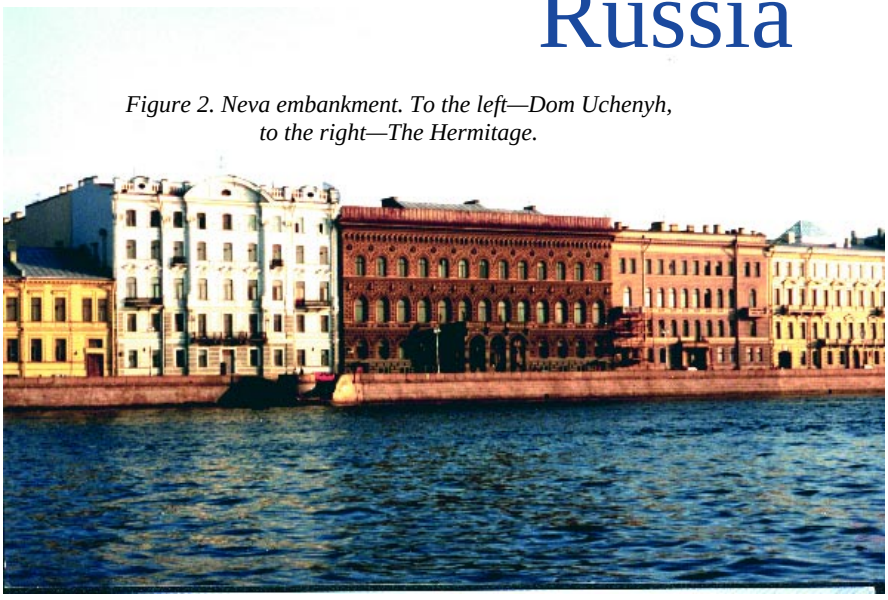


Figure 2. Neva embankment. To the left—Dom Uchenyh, to the right—The Hermitage.

lar and 40 poster papers were presented. Three volumes of conference proceedings were published, which include 165 papers representing 33 countries. The numbers of papers presented are from Russia (87), USA (14), Italy (8), Japan (6), Germany (6), Brazil (4), Korea (4), Argentina (3), P.R.China (3), France (3), Ukraine (3), and Yugoslavia (3). The conference took place in the "Dom Uchenyh" ("House of Scientists")—a beautiful palace in the historical center of St. Petersburg, next to the Tsar's Winter Palace and the Hermitage museum. Social Programs included sightseeing tours: survey bus tour of St. Petersburg, tours of the Hermitage, and a bus tour to Peterhof. The conference banquet took place on Friday, July 7 in the House of Scientists.

Summary of the Scientific Program

The conference as a whole has demonstrated continuing interest in analysis and control methods for chaotic dynamics and oscillations. Papers from various scientific fields were presented at the conference. Most papers were devoted to dynamics and control of systems from the two broad fields: mechanical systems (main applications are motion control, robotics, and vibrational technologies); and electrical or electronic systems (main applications are in the field of telecommunications and power systems). It brought together many experts to cross-fertilize ideas from these fields that have common features and similarities. Such a gathering was made possible by the financial support to the conference from different resources, particularly from the IEEE and the IUTAM.

A number of the papers addressed the problems of analysis of complex behavior in physical systems. Significant attention was paid to analysis and design of neural networks, and studies of complexity and synchronization in nonlinear systems. Also, many papers with applications to chemical technologies, geophysics, medicine, economics, and so forth, were presented. Some plenary and semi-plenary papers contained important theoretical results: O. M. Belotserkovsky, Yr.D. Shevelev, and F. A. Maksimov(Russia): "Some Problems of Turbulence and Instabili-

. . . continued on Page 28

Figure 3. From left to right: Prof. F. L. Chernousko, member of the Russian Academy of Sciences and chair of International Program Committee of COC 2000; Prof. Rui J. P. de Figueiredo, University of California, Irvine, and IEEE CAS Society Distinguished Lecturer; Prof. W. Schielen, University of Stuttgart, Germany, and president, International Union of Theoretical and Applied Mechanics; and Prof. A. L. Fradkov, St. Petersburg State University and chair of the National Organization Committee, COC 2000.

COC Report… continued from Page 27

ties"; I. I. Blekhman and K. A. Lurie (Russia-USA): "Creating Dynamical Materials as a Problem of Control"; F. L. Chernousko (Russia): "Snake-Like Motions of Multibody Systems over a Rough Plane"; M. Dimentberg, D. Iourtchenko and A. Bratus (USA-Russia): "Optimal Bounded Control of Random Vibration"; K. S. Hedrih (Yugoslavia): "Nonlinear Dynamics of a Gyrorotor and Sensitive Dependence on the Initial Conditions of the Forced Vibration of a Heavy Gyrorotor"; P. C. Mueller (Germany): "Nonlinearity Estimation and Compensation by Linear Observers—Theory and Applications"; A. N. Sharkovsky and S. A. Berezovsky (Ukraine): "Phase Transitions in Computer Turbulence"; and F. Udwadia (USA): "New Developments in Dynamics of Constrained Systems with Applications to Tracking Control".

Other speeches were devoted to applications in telecommunications, mechanical engineering, and biology; A. S. Dmitriev, A. L. Panas, and S. O. Starkov (Russia): "Multiple Access Communication Based on Control of Special Chaotic Trajectories"; E. Kreuzer and M. Wendt (Germany): "Nonlinear Dynamics of Ship Oscillations"; E. Mosekilde (Denmark): "Chaotic Synchronization in Living Systems"; F. Pfeiffer, Th. Rossmann, and K. Loffler (Germany): "Control of a Tube Crawling Machine"; and W. Schiehlen (Germany): "Motion Control of Vehicles in Convoy". Finally, the IEEE Distinguished Lecture entitled "A Reproducing Kernel Hilbert Space (RKHS) Approach to the Optimal Modeling, Identification, and Design of Nonlinear Adaptive Systems" was delivered by Prof. Rui J.P. de Figueiredo (USA), at the closing plenary session. Regular papers were distributed over the following eleven theme sections (four sessions in parallel):

Figure 4. White Night in St.Petersburg. Dom Uchenyh and The Hermitage are behind halfs of the opened bridge.

- *Control of Oscillations*, A. Fradkov, chairman;
- *Control of Chaos*, R. Genesio, A. Tesi, A. Pogromsky, co-chairmen;
- *Control of Mechanical Systems*, V. Yu. Rutkovsky, chairman;
- *Mathematics of Stability and Instability*, G. A. Leonov, chairman;
- *Identification and Reconstruction of Parameters*, A. N. Sharkovsky, chairman;
- *Synchronization*, I. I. Blekhman, chairman;
- *Nonlinear Dynamics and Chaos in Physical Systems*, A. K. Abramyan, S. A. Vakulenko, co-chairmen;
- *Nonlinear Dynamics and Chaos in Mechanical Systems*, D. A. Indejtsev, chairman;
- *Nonlinear Dynamics and Chaos in Electronics, Communications and Power Systems*, A.S. Dmitriev, chairman;
- *Nonlinear Dynamics and Chaos in Biomedical, Ecological and Neural Systems*, V. S. Anischenko, chairman;
- *Methods of System Analysis*, E. N. Rozenwasser, chairman.

The major goal of the conference—to bring together researchers from various fields, to advance the state-of-the-art control theory and technology for the control and analysis of complex oscillatory dynamical systems, and to gain some general and unified perspectives in this interdisciplinary field of advanced research—was achieved. Another goal of the conference—to get the world scientific community acquainted with recent achievements of Russian experts in nonlinear dynamics and nonlinear control—was achieved too.

—Prof. Alexander Fradkov
NOC Chairman, COC2000

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Committee Report
Meeting Report
Executive Report
Obituary
Publications Report
Technical Article
Ω 'Umble Ohm–Shlomo Karni
Crossword Puzzle–Patrick Sain
Crossword Puzzle–Patrick Sain & Cheryl Schrader

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CAS Society Distinguished Lecturer Program—Part II

2000 Distinguished Lecturers

Professor José E. da Franca

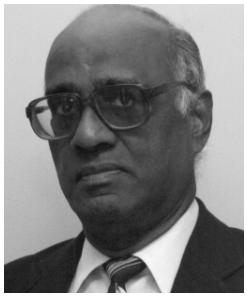
Analog Libraries in Digital CMOS

Abstract—Advanced digital CMOS technologies are becoming an increasingly important manufacturing platform for mixed analog-digital integrated circuits. While such technologies provide ever improving performance for digital circuits, by contrast, analog circuits face a variety of design hurdles not usually present in "older" technologies with analog options. Chief among these are the unavailability of double-poly capacitors and high resistivity poly, poor transistor models and poorly characterized compatible bipolar transistors, and of course operation in highly "polluted" digital environments.

In this lecture we will review the fundamental problems and will provide practical answers for designing high performance analog circuits in mainstream digital CMOS. By making extensive use of such techniques as oversampling and noise-shaping, current-mode processing, self-calibration and digital correction, among others, several mixed-signal chip designs will be shown that can achieve the level of performance and robustness required in some of today's most relevant applications, thus allowing their integration in cost competitive digital VLSI processes.

Multirate Analog Signal Processing

Abstract—Multirate signal processing emerged in the 70's as a specialized branch of digital signal processing, driven by the need for solving, in the most efficient possible way, a number of problems mainly related to the migration of telephone multi-

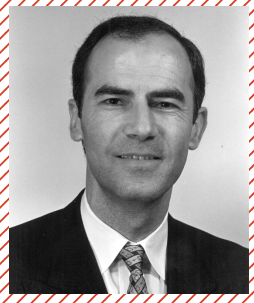


The following article is the second in a series, taken from an article written by B. A. Shenoi detailing the CAS Distinguished Lecturer Program, the lecturers, and their lectures. Begun in the June 2000 issue of the CAS Newsletter *and continued here, it is a reminder to all of the excellent Distinguished Lecturers Program, a tribute to longtime chairman Belle Shenoi, and an introduction of Ellen Yoffa, the new chair of the program effective July 1, 2000.*

—Editor

plexing and transmission systems from analog and digital solutions. Subsequently, the technique found many more application areas of great relevance of which, today, the decimation and interpolation techniques applied to oversampling data converters are more familiar examples. The emergence of other non-digital signal processing technologies, such as charge transport devices and switched-capacitors, which are also discrete-time, although the signal amplitudes are represented in analog form, led to the development of analog multirate signal processing techniques which have found important application areas in the realization of complex filtering systems with very high Q-factors, as well as in high-speed interface and data acquisition systems of which video coders/ decoders and magnetic disk read channel coders are some of the most visible examples. Today, new design solutions are emerging, which combine the benefits of both digital and analog multirate signal processing to achieve high efficiency in silicon and power consumption in modern mixed analog-digital integrated circuits.

This lecture introduces the basic concepts of multirate theory and discusses its practical application to the design of analog sampled-data circuits, both switched capacitors and switched-currents. First, we will show how the ubiquitous switched-capacitors can efficiently realize the signal processing functions needed for analog-digital and digital-analog interfacing, frequency division multiplexing, high-Q filtering and even the currently "hot" subsampling mixers that might be employed in integrated radio receivers. Then, new switched-current realizations of multirate filters will also be shown for very high-frequency video processing applications.



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CMOS Analog-Digital Conversion

Abstract—In a not too distant past, analog-to-digital (A/D) and digital-to-analog (D/A) signal converters were realized as standard components, produced by only a few highly specialized manufacturers worldwide, for assembly in larger boards or maybe even hybrid modules. Today the relentless trend of electronics integration and miniaturization is rapidly changing the way signal converters are used, designed and even produced. Because such converters are being increasingly used as macrocells embedded into larger VLSI mixed-signal systems, rather than standard discrete parts for board assembly, the traditional label of "general purpose" components they used to carry is quickly vanishing to pave the way to "tailor-made" components that can optimally meet target specifications for performance, cost and energy consumption. As a result, their design is no longer the exclusive specialty of a few manufacturers and instead is gaining preeminence also as an integral part of the expertise of the large teams usually involved in the design of those VLSI systems. This, in turn, leads to the fact that their production as part of completed mixed-signal VLSI chips is also shifting from the traditional manufacturers of general-purpose standard components to the ASIC manufacturers. Therefore, the market dominant CMOS technology is also quickly replacing other processing technologies that have been widely used in the past for data converters.

This lecture provides an overview of the most relevant circuit techniques currently employed for designing A/D

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Distinguished Lecturers … continued from Page 31

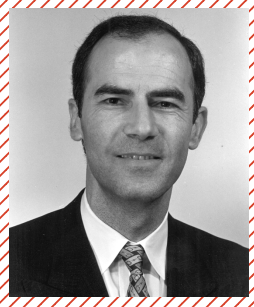
and D/A converters in CMOS technology. Practical examples will be given of about 10 high performance CMOS data converter designs covering a wide range of specifications both in terms of speed and resolution.

High Resolution Pipeline CMOS ADCs

Abstract—Pipelined analog-to-digital converters (ADCs) with specifications ranging from 12 to 14 bits of resolution at 50 to 100 MHz will play a key role in future CMOS integrated systems for portable multimedia and communication applications. Traditional designs of pipelined ADCs, particularly for resolutions up to 10 bits, have considered optimum 1-bit-per-stage architectures yielding maximum speed of operation while minimizing area and power dissipation. For resolutions above 10 bits where self-calibration techniques are required for linearizing inter-stage residue generation and amplification, such design strategy no longer holds and we have to consider instead multibit-per-stage optimization procedures taking into account the constraints introduced by thermal noise, the self-calibration technique employed for accuracy enhancement of capacitor matching as well as the requirements for practical feasibility of the active analog components.

To attack the complex analytical formulation of such a multivariable problem, a systematic computer-assisted methodology has been developed that efficiently handles the critical design issues yielding optimum tradeoffs between power dissipation and area consumption while minimizing stringent requirements of the constituting building blocks and significantly reducing the complexity of the calibration circuitry.

The lecture discusses the practical integrated circuit implementation of such converts, starting with the design of efficient analog-based calibration techniques for the critical high linearity low resolution front-end stages and then going through a systematic computer-assisted methodology that efficiently handles design tradeoffs between power dissipation and area consumption while minimizing stringent requirements of the constituting building blocks. Practical design examples are presented to consolidate the relevant conclusions.



Prof. José E. da Franca

Self-Adjusted Analog-Digital Integrated Circuits

Abstract—Advanced digital CMOS technologies are becoming an increasingly important manufacturing platform for mixed analog-to-digital integrated circuits. Because of its generally acknowledged hostility toward analog circuits, such a technology environment requires that appropriate circuit design techniques are devised to enhance the performance of analog circuits, even when subject to significant accuracy limitations. Among those techniques, digitally self-adjusted circuits are particularly interesting because of their use of inexpensive on-board digital circuitry to assist the operation of analog circuits.

Although several self-adjusted analog circuits have been developed in the past, the underlying basic concepts have been kept quite apart with little or no synergistic interaction between rather different classes of circuit functions (e.g. self-calibrated converters, self-tuned filters, and so forth). In this

lecture we attempt to establish a simple framework for self-adjusted analog-digital RAM and the universal calibrator, which can be used in a wide variety of applications, even those as far apart as filtering and conversion.

Examples given of self-adjusted circuits actually built in CMOS integrated circuit form include several types of data converters, a very high-frequency continuous-time filter, a very low power high-frequency comparator, a switched-current delta-sigma modulator and even a quadrature modulator (I&Q) transmit interface for radio communications.

Professor Yih-Fang Huang

Interference Mitigation for Wireless Communications

Abstract—This lecture addresses applications of adaptive filtering techniques for interference mitigation in modern communication systems. Of particular interest will be wireless CDMA systems, where several forms of interference are present, with the major impairment being multiple access interference. This lecture will address development of practical, appealing multi-user detection schemes that can be deployed for mitigation of multiple access interference. In particular, nonlinear optimum multi-user detection that can be implemented at a practical, acceptable computational cost will be developed.

Novel multi-user detection schemes developed at Notre Dame feature iterative solutions based on optimum multi-stage interference cancellation, such as optimum parallel interference cancellation. Adaptive filtering techniques such as LMS and set-membership filtering play critical roles in such nonlinear multi-user detection, especially relevant to channel estimation. These results lead to a substantial increase in service capacity in wireless communications and can be illustrated with an audio demonstration.

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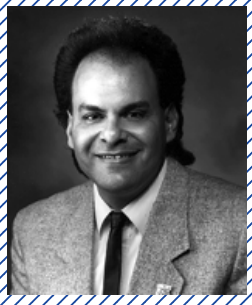

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Professor Mohammed Ismail

Abstract—This lecture will discuss the evolution of the wireless industry and will focus on transceiver architectures and circuit design techniques used in modern cost effective mobile communication systems.

Architectures and design techniques suitable for multi-standard low power transceivers achieving a high level of integration will be presented. The techniques exploit recent developments in submicron CMOS and BiCMOS technologies together with mixed signal design methodologies whereby control of the analog front end is affected directly by digital signals generated from the DSP parts in the baseband. This will pave the way toward efficient implementation of third generation (G3) Universal Mobile Telephone Service (UMTS) and drive an increasingly competitive broadband wireless market even further.

Digitally Programmable RF Front Ends: Toward Universal Mobile Communication Service

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Distinguished Lecturers … continued from Page 33

Recent Developments in CMOS Low Voltage, Low Power VLSI

Abstract—This lecture will cover basic design issues of low voltage (LV), low power (LP) VLSI design and discuss major challenges and state-of-the-art solutions to designing high performance, high yield LV/LPVLSI circuits.

Fabrication and battery technologies as well as circuit and layout design issues are discussed. An introduction to integrated RF in CMOS technology is also given. Emphasis will be placed on robust analog and mixed signal design in CMOS and BiCMOS technologies for mobile/portable applications in areas such as wireless communications and CCD and MOS imager interfaces in digital cameras.

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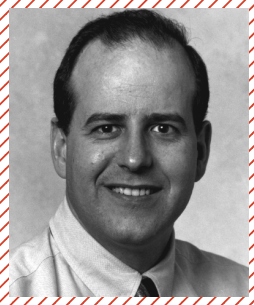
Professor Takao Nishitani

Trends and Perspectives on Multimedia Processors

Abstract—Thanks to LSI progress and well-studied bandwidth compression standards of audio and video, the multimedia world including audio and video are now established among expressions, communications, information processing and database areas in an economical way. Examples can be seen in the Internet carrying video and audio as well as text. Digital audio and video are no more hard media for digital equipment, but it is also true that even compressed audio and video require a lot of digital resources. Therefore, in order to realize this multimedia world in more economical ways, many efforts have been made and are going to be made to develop more powerful processors, called multimedia processors.

In this lecture, after reviewing the brief history of multimedia applications, many multimedia processors now available are segregated into several classes in terms of technical viewpoints. As all classes have strong points as well as weak points, this segregation gives a simple understanding of different chips. Future trends will be estimated through our experience in the consumer market. One big target for future System-on-a-Chip applications will surely be the portable system, and this talk includes such applications based on our experience.



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Professor Fathi M. Salam

Abstract—Inspired by neurobiological experiments on squirrel monkeys to measure how they learn to track objects, we describe the state-of-the-art of architectural connectivity and functionality from an engineering/systems perspective. We show how learning mechanisms can emulate the neurobiological models in simulation. Moreover, micro-electronic circuit architectures are shown to realize these models efficiently into hardware. This process of system investigation is shown to explain new interconnectivities and/or functionality based on performance analysis. The results support more definitively a learning process, which incorporates the brainstem and the flocculus. This interdisciplinary research employs engineering analysis and circuit method-

A Model of Eye Movements and Learning to Track Objects Inspired by the Squirrel Monkey

ologies to create new intelligent circuit and system architectures while supporting better understanding of neurobiology.

Abstract—This lecture describes a framework arising from signal travel through dynamic, non-stationary channels of either room acoustics or free space wireless telecommunications. The framework maps to a unified form of an optimization of a performance index subject to the constraints of a dynamic network, represented in the state space. The performance index is a measure of statistical dependence among the resulting outputs of the network, namely, the relative entropy. The network is represented as (either discrete or continuous time) state space dynamics, including recurrent feedback neural networks. This framework includes the popular models of FIR and IIR network representations. Several adaptive methodologies for general environments are shown, via simulations as well as real-world experiments, to be very effective, and supersede the performance of existing techniques, for example, Noise Cancellation Technologies (NCT).

Blind Signal Separation and Recovery for Speech Denoising and Wireless Communications

Professor Edgar Sánchez-Sinencio

Abstract—This lecture deals with active filters using Operational Transconductance Amplifiers (OTAs). The presentation addresses the inte-

Transconductance Amplifiers, Architectures and Active Filters

grated circuit issues involved in active filters (using CMOS transconductance amplifiers) and the progress in this field in the last fifteen years. CMOS transconductance amplifiers, non-linearized and linearized, as well as frequency limitations and dynamic range considerations, are reviewed. OTA-C filter architectures, current-mode filters, and other potential applications of transconductance amplifiers are discussed.

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E-mail: sanchez@ee.tamu.edu

Abstract—Low voltage (LV) analog circuit design techniques are addressed in this lecture. The following key points are covered: (i) technology considerations; (ii) transistor models

Low Voltage Analog Circuit Design Techniques

capable of providing performance and power trade-offs; (iii) low voltage implementation techniques capable of reducing power supply requirements, such as float gate, bulk driven, and self cascode MOSFETs; (iv) basic LV building blocks; (v) multi-stage frequency compensation topologies; and (vi) fully-differential and fully-balanced systems.

IEEE CAS FELLOW PROFILES 2000

Jaakko Tapio Astola

For contributions to the theory and applications of nonlinear signal processing.

Jaakko T. Astola

Jaakko Astola was born in Helsinki, Finland on May 6, 1949. He received the B.Sc., M.Sc., Licentiate and Ph.D. degrees in mathematics, specializing in error-correcting codes, from Turku University, Finland, in 1972, 1973, 1975, and 1978 respectively. From 1976 to 1977 he was research assistant at the Research Institute for Mathematical Sciences of Kyoto University, Kyoto, Japan. Between 1979 and 1987 he was with the Department of Information Technology, Lappeenranta University of Technology, Lappeenranta, Finland, holding various teaching positions in mathematics, applied mathematics and computer science. In 1984 he worked as visiting scientist in Eindhoven University of Technology, The Netherlands. From 1987 to 1992 he was associate professor in applied mathematics at Tampere University, Tampere, Finland. Currently he is professor of signal processing and head of the Signal Processing Laboratory of Tampere University of Technology and leads a group of about 60 scientists. Based on evaluation by international experts, this laboratory was recently elected as a Centre of Excellence in Research by the Academy of Finland for the years 2000–2005. He is also director of Tampere International Center for Signal Processing, founded 1997, that has already hosted numerous visiting scientists in signal processing as well as organized four workshops. Currently he is coordinating one of the largest graduate schools in Finland: Tampere Graduate School of Information Science and Engineering. He has authored over 200 papers and three textbooks on signal and image processing and has experience in editing books and scientific journals. He has been conference chair of several international conferences.

Kwang-Ting Cheng

For contributions to innovative techniques for testing and synthesis of electronic circuits.

Kwang-Ting Cheng

Kwang-Ting (Tim) Cheng received the B.S. degree in electrical engineering from National Taiwan University in 1983, and the Ph.D. degree in electrical engineering and computer science from the University of California, Berkeley in 1988.

From 1988 to 1993 he worked for AT&T Bell Laboratories in Murray Hill, New Jersey. In 1993 he joined the faculty at the University of California, Santa Barbara where he is currently professor of electrical and computer engineering and director of the computer engineering program. His current research interests include VLSI testing, design synthesis, and design verification. He has published over 150 technical papers, co-authored three books and holds nine U.S. patents in these areas. He has also been working closely with U.S. industry for projects in these areas. He received best paper awards at the 1994 Design Automation Conference, the 1999 Design Automation Conference and the1987 AT&T Conference on Electronic Testing.

He currently serves as associate editor-in-chief for the *IEEE Design and Test of Computers*. He also serves on the editorial boards of the *IEEE Transactions on Computer-Aided Design* and the *Journal of Electronic Testing: Theory and Applications*. He served as general chair and program chair of the IEEE International Test Synthesis Workshop. He has also served on the technical program committees for several international conferences on CAD and testing including DAC, ICCAD, ITCC and VTS.

CIRCUITS AND SYSTEMS SOCIETY MEMBERS

Bogdan M. Wilamowski

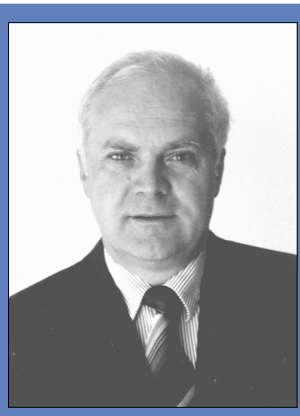
For contributions to industrial electronics and static induction devices.

Bogdan M. Wilamowski received the M.S. in computer engineering in 1966, the Ph.D. in neural computing in 1970, and the Dr.Habil. in integrated circuit design in 1977, all from the Technical University of Gdansk. He received the title of professor from the president of Poland in 1987. He was director of the Institute of Electronics from 1979 to 1981 and chair of the Solid State Electronics Department from 1987 to 1989 at this University. Since 1989 he has been at the University of Wyoming.

Dr. Wilamowski was with the Nishizawa Laboratory at Tohoku University, Japan, from 1968–1970 and he spent one year at the Semiconductor Research Institute, Sendai, Japan, as a JSPS Fellow, in 1975–1976. He was a visiting scholar at Auburn University from 1981–1982 and 1995–1996, and visiting professor at the University of Arizona, Tucson from 1982–1984.

Dr. Wilamowski was, and currently is, a member of organizing/technical committees of several IEEE international conferences: ICIPS'98 (Australia), ISIE'98 (South Africa), ISIE'99 (Slovenia), IECON'99 (USA), ICRAM'99 (Turkey), ICIT'00 (India), IECON'00 (Japan), IIZUKA'00(Japan), ICMNFBS'00 (France), ISIE'01 (Korea), and IECON'02 (Spain). He also serves as general chair of IECON2001 in Denver. He is treasurer of the IEEE Industrial Electronics Society and a member of the IEEE Neural Network Council. He is associate editor of the IEEE *Transactions on Neural Networks*,the *IEEE Transactions on Education*, and the *IEEE Industrial Electronics Newsletter*.

Dr. Wilamowski is author of four textbooks, more than 200 refereed publications, and 27 patents. His main areas of interest are digital hardware, electronics, CAD development, VLSI, network programming, and neuro-fuzzy systems.



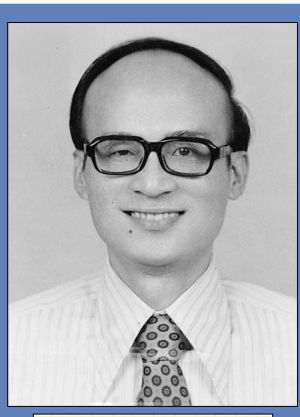
Bogdan M. Wilamowski

Soo-Chang Pei

For contributions to the development of digital eigenfilter design, color image coding and signal compression, and to electrical engineering education in Taiwan.

Soo-Chang Pei was born in Soo-Auo, Taiwan in 1949. He received the BSEE from National Taiwan University in 1970 and the MSEE and Ph.D. degrees from the University of California, Santa Barbara in 1972 and 1975, respectively.

Dr. Pei was engineering officer in the Chinese Navy Shipyard from 1970 to 1971. From 1971 to 1975, he was research assistant at the University of California, Santa Barbara. He was professor and chairman in the Electrical Engineering Department of Tatung Institute of Technology and National Taiwan University, from 1981 to 1983 and 1995 to 1998, respectively. Presently, he is professor of the Electrical Engineering Department at National Taiwan University. His research interests include digital signal processing, image processing, optical information processing, and laser holography. Dr. Pei received the National Sun Yet-Sen Academic Achievement Award in Engineering in 1984, the Distinguished Research Award from the National Science Council from 1990–1998, Outstanding Electrical Engineering Professor Award from the Chinese Institute of Electrical Engineering in 1998; and the Academic Achievement Award in engineering from the Ministry of Education in 1998. He has been president of the Chinese Image Processing and Pattern Recognition Society in Taiwan from 1996–1998, and is a member of the IEEE, Eta Kappa Nu and the Optical Society of America.

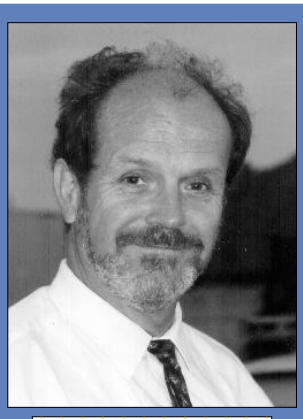


Soo-Chang Pei

IEEE CAS FELLOW PROFILES 2000

Manfred Glesner

For contributions to the development of microelectronic system design and education in microelectronics.



Manfred Glesner

Prof. Dr. Dr.h.c.mult. Manfred Glesner, Darmstadt University of Technology, received the diploma in applied physics and electrical engineering in 1969, and the Ph.D. degree in 1975, both *summa cum laude* from Saarland University in Saarbrücken, Germany. Since 1981 he has been professor for microelectronic systems at Darmstadt University of Technology and teaches courses in circuit design and CAD for microelectronics. In 1981 Manfred Glesner was the first to introduce multi-project chips in university curricula in Germany. He is director of the Graduate College for Intelligent Systems in Information Technology. Manfred Glesner contributed original research to areas of high-level synthesis, physical design, rapid system prototyping and intelligent signal processing. Furthermore, he pioneered research work on developing a design environment for heterogenous real-time systems in an interdisciplinary research program of the German National Science Foundation. He is a member of several national and international organizations and has organized several national and international conferences. From 1997–99 he served as associate editor for the *IEEE Transactions on Circuits and Systems—I*. He has been project consultant for the European Commission and the United Nations Development Organization. He is also serving on the advisory board of several companies. After the political breakdown in Eastern Europe, he built up several microelectronic design centers at eastern European universities with support from the European-Union-based TEMPUS-Program. For his contributions to the field of microelectronics he received two *honoris causa* doctoral degrees, as well as an *honoris causa* professorship.

Yong Ching Lim

For contributions to the design of FIR digital filters.

Yong Ching Lim

Yong Ching Lim received the B.Sc. and Ph.D. degrees in 1977 and 1980, respectively, both in electrical engineering, from Imperial College, London. He was awarded the 1977 IEE prize for the best all-round performance of a final year student in the Electrical Engineering Department of Imperial College.

From 1980 to 1982, he was with the Naval Postgraduate School, California. Since 1982, he has been with the Department of Electrical Engineering, National University of Singapore, where he is currently professor. His research interests include digital signal processing and VLSI circuits and systems design.

Dr. Lim was selected to receive the 1996 IEEE CAS Society's Guillemin-Cauer Award for the paper "Frequency-Response Masking Approach for Digital Filter Design: Complexity Reduction via Masking Filter Factorization" and the 1990 IREE (Australia) Norman Hayes Award for the paper "A New Filtering Scheme for Split-Band Voice Coding".

Dr. Lim served as associate editor for *IEEE Transactions on Circuits and Systems* from 1991 to 1993 and has been serving as associate editor again since 1999. He had also served as associate editor for *CSSP* from 1993 to 2000. He was "digital filters" area editor for *The Circuits and Filters Handbook* jointly published by the IEEE and CRC Press. He chaired the CAS Society's DST TC from 1998 to 2000. He served in the Technical Program Committee's DSP Track as chairman at ISCAS'97 and ISCAS'00 and as co-chairman at ISCAS'99.

CIRCUITS AND SYSTEMS SOCIETY MEMBERS

Wu-Tung Cheng

For contributions to the area of automatic test pattern generation and fault simulation for digital circuits.

Wu-Tung Cheng

Wu-Tung Cheng received the B.S. and M.S. degrees in electrical engineering from National Taiwan University in 1978 and 1982, respectively, and the Ph.D. degree in computer science from the University of Illinois at Urbana-Champaign in 1985.

From 1985 to 1990, he was with AT&T Bell Laboratories developing GENTEST, a test pattern generation system for general sequential circuits. In GENTEST, he created the BACK test generation algorithm, the SPLIT circuit model and the Differential fault simulation algorithm. GENTEST supported stuck-at fault model and IDDQ test methods.

In 1989, he held a visiting position at the University of Illinois where he improved the Differential fault simulation algorithm with the PROOF fault simulation algorithm.

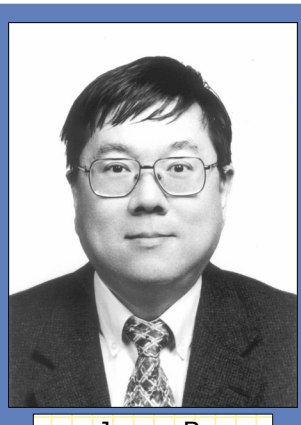
From 1990 to 1993, he was vice president of engineering and cofounder of CheckLogic Systems, Inc. His responsibilities included managing the development team of FastScan (a.k.a. ScanCheck), FlexTest (a.k.a. CyCheck) and DFTAdvisor (a.k.a. DFTMaker) products, and developing software tools of FlexTest and other products in the area of test synthesis, netlist knowledge extraction, design for testability, built-in self test, Boolean verification, and logic minimization.

In 1993, CheckLogic merged with Mentor Graphic Corporation, and since then he has had various technical management positions. His current positions are chief scientist and System-on-Chip test business unit manager. He is continually involved in the development of ATPG and built-in-self-test products.

Dr. Cheng serves as a member of program committees of several DFT related workshops and conferences and he is a member of the IEEE P1500 standard committee.

James B. Kuo

For contributions to modeling CMOS VLSI devices.



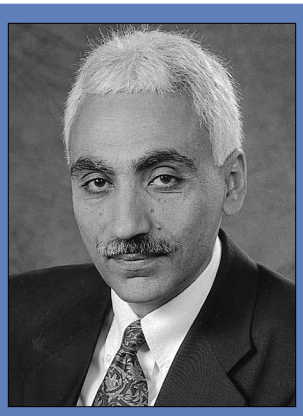
James B. Kuo

James B. Kuo received the BSEE degree from National Taiwan University in 1977, the MSEE degree from The Ohio State University in 1978, and the Ph.D. degree in electrical engineering from Stanford University in 1985. From 1978–1981 he worked in Penril Data Communications, Maryland, and Racal Vadic, California, as a research engineer working on integrating telecommunication modem chips using CMOS technology. From 1985–1987 he was an engineering research associate in the IC Lab of Stanford University, working on BiCMOS devices. From 1987–2000 he was with National Taiwan University. In September 2000, Professor Kuo joined the University of Waterloo, Canada, as a tenured full professor. His research expertise is in the field of low-voltage CMOS VLSI circuits and SPICE compact modeling of deep-submicron bulk and SOI CMOS and BiCMOS VLSI devices. He serves as a member in the international advisory board of the *IEEE Circuits and Devices Magazine* and chair of the membership committee for the IEEE Electron Devices Society. He is a distinguished lecturer of the IEEE Electron Devices Society. He has published over 100 international journal papers and authored eight books including *Low-Voltage CMOS VLSI Circuits* (John Wiley: New York, 1999) and *CMOS VLSI Engineering: Silicon-On-Insulator (SOI)* (Kluwer: Boston, 1998). He has graduated over 35 M.S. and Ph.D. students specialized in CMOS circuit designs and device modeling, currently working in leading US and Taiwan microelectronics companies.

IEEE CAS FELLOW PROFILES 2000

Abbas El Gamal

For pioneering application of probability and statistics to develop new methods for the analysis and design of integrated circuits.



Abbas El Gamal

Abbas El Gamal received the B.S. degree in electrical engineering from Cairo University in 1972, and the M.S. degree in statistics and the Ph.D. degree in electrical engineering from Stanford University in 1977 and 1978, respectively. He was assistant professor of electrical engineering at USC from 1978–1980. In 1980 he joined Stanford University where he is currently professor of electrical engineering. He was on leave from Stanford from 1984–1988 as director of LSI Logic Research Lab, where he developed silicon compilation technology and DSP and image processing ASICs; and then as cofounder and chief scientist of Actel Corporation, a Field Programmable Gate Array supplier, where he developed the first anti-fuse based FPGA and associated design tools. From 1990–1995 he was a cofounder and chief technical officer of Silicon Architects, which is now part of Synopsys, where he developed synthesis optimized libraries and data path synthesis tools. Dr. El Gamal is currently principal investigator on the Stanford Programmable Digital Camera project, an industrially funded research program focused on developing algorithms, architectures, and circuits for single chip CMOS digital imaging systems. He has been a member of the ISSCC Technical Program Committee on Imagers and MEMS since 1997.

Dr. El Gamal's research interests include CMOS image sensors and digital cameras, image processing, FPGAs and mask programmable gate arrays, VLSI CAD, and information theory. He has authored or co-authored over 100 papers and 20 patents in these areas. Dr. El Gamal serves on the board of directors of Numerical Technologies, Lightspeed, and PiXIM, and the advisory boards of several start-up companies including Simplex Solutions, Barcelona Design, and Tspan.

Fellow Nominations Due

Forms must be received by the IEEE Fellow Committee no later than ***March 15, 2001****.*

The IEEE's annual Fellow election begins in early spring. The process begins with the nominator. Any person is eligible to serve as a nominator except members of the IEEE Board of Directors, members of the IEEE Fellow Committee, IEEE Technical Society/Council Fellow Evaluating Committee Chairs, members of IEEE Technical Society/Council Evaluating Committees (only if a nomination will be reviewed by their committee) or IEEE Staff. A candidate is an IEEE Senior Member who has completed five years of service in any grade of membership and is current in their membership dues. The candidate can come from any field, including academia, government and industry. Whatever their careers, candidates must have made an outstanding contribution to the electrical and electronics engineering profession.

The nominator is responsible for the following. Preparation of IEEE Fellow Grade Nomination Form. Solicitation of at least five, but no more than eight, references capable of assessing the candidate's contributions. The references must be IEEE fellows, except in Regions 8, 9, and 10, where they may be senior members. The list of IEEE fellows is available at the website http://services5.ieee.org/about/awards/fellows/fellows.htm. The references cannot be members of the IEEE's Board of Directors, the Fellow Committee, the Society/Council Evaluating Committee or the IEEE Staff. Identification of an IEEE Society/Council whose evaluating committee will assess the

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You can help determine whose picture will be here next year by sending in your suggestion. See the article to the right.

Next Year's Fellow

Governors' Clipboard

MINUTES
of the
CAS BOARD OF GOVERNORS MEETING
Sunday, May 28, 2000
Hotel President Wilson
Geneva, Switzerland

I. **Call to Order and Introduction of Members**. President Bing Sheu called the meeting to order at 12:00 p.m. and asked all in attendance to introduce themselves.

II. **Approval of Previous Minutes**. A motion was made, seconded and voted upon to approve the *Minutes* of the November 7, 1999, Board of Governors meeting. **Approved**.

III. **Review and Adoption of Agenda**. Sheu requested to move reports from Regional VPs toward the end, include the presentation of IEEE past president Ken Laker after the CAS past president's section, and move the VP-Administration section after Laker's report.

The amended agenda was **approved**.

IV. **Report from the President**. Sheu announced that the minutes of the past two ExCom meetings are included in the agenda. Other announcements and reports:

a. **Appointments to IEEE Committees**. President-elect should have enough time to appoint representatives to various IEEE committees for terms beginning January 1 of his/her presidency.

b. **Constitution and Bylaws (C&BL) Committee**. K. Thulasiraman, chair, announced that the C&BL will be revised as follows:

1. Ambiguities will be corrected and inconsistencies clarified which exist in the current C&BL.
2. Past resolutions from past BOG meetings will be incorporated into a proposed version.
3. Conflict of interest areas will be addressed.

Thulasiraman indicated that #1 has been addressed, that he will work with the administrative office on #2, and that he will need assistance/input from ExCom/BOG on #3. He will complete a draft of the document and submit to ExCom by the September meeting.

Sheu emphasized that the C&BL Committee needs to be expanded, and announced that Thulasiraman's appointment had been made by him and past president, George Moschytz.

c. **Other Standing Committees**. The Fellows chair will be replaced in 2000 for 2001. Moschytz is the 2000 Awards Committee chair. The Nominations Committee is chaired by (immediate) past president, Rui de Figueiredo. Discussion on composition of the Nominations Committee took place but no action was taken.

d. **IEEE BOD Meetings**.

1. A Nanotechnology Council is being formed. CASS has been approached to join as a sponsoring society.
2. An IEEE-level Wireless Periodical Working Group has been formed and T. Ng is the CASS representative.
3. System-on-a-Chip Chapter. Davies and Laker will report later.

e. **e-Newsletter in Circuits from IEEE**. A solicitation has been circulated for news items and articles.

f. **Distinguished Lecturers Program (DLP) Subcommittee**. T. Davies, chair, submitted a report (see below) which had been endorsed by the ExCom at its morning meeting. Sheu thanked the *ad-hoc* subcommittee on a job well done, and announced that E. Yoffa has been appointed as the new chair of the DLP.

CAS DLP Subcommittee Report

1. The subcommittee interprets its task as seeking ways to ensure that the DLP covers all CAS areas (as both sources of lecturers and destinations of lecturers) and all "hot" technical areas of the CAS Society.
2. We perceive the DLP objective is to make high quality, stimulating lectures on important CAS topics available to CAS Chapters to enhance their professional development.
3. We suggest that mechanisms needed to enhance the DLP are:
   - more flexibility to add and delete DLs;
   - regular monitoring of the overall situation;
   - promotion of DLP to CAS chapter chairs.
4. We recommend that the DLP should continue to offer 100% funding of reasonable costs for pre-approved visits, subject to a maximum of $1,000 ($2,000 in the case of intercontinental travel). DLP chair should have discretion to increase this in special circumstances.
5. We recommend that the DLP chair should choose the members of the DLP Committee, and be expected to seek the advice of the Regional VPs and chairs of CAS Technical Committees in the se-

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Governors' Clipboard

BOG Report … continued from Page 41

lection of Distinguished Lecturers.

6. We recommend that the DLP be established as a Standing Committee (as opposed to an *ad-hoc* committee) subject to acceptance of #5 above.
7. We anticipate a substantial strengthening of the DLP, to make an increasing impact, and consider this necessary for its survival.

Submitted by: A.C. Davies (chair), B. Shenoi, M. Zaghloul, H. Reddy, [+ E. Yoffa (DLP chair-elect)]
May 27, 2000

g. **Restructuring Committee**. No report is available at this time. President-elect, H. Reddy, will become an additional member of the committee.

h. **Medal Awards Dinner**. A dinner for the CAS and IEEE medal recipients will be held at ISCAS and DAC. Medalists were polled as to where they wished to receive the awards.

i. **Society Growth and Greater Participation**. CAS must seek ways to promote the Society and encourage greater, active participation from its members.

V. **Report from the President-Elect and Regional Activities Division (RAD) – H. Reddy**

a. Promoting CAS in ALL regions has been the RAD's most important goal.

b. There is much potential for new chapters, e.g., Silicon Valley has a large academic and industrial membership, but a CAS chapter does not exist.

c. The DLP needs to be expanded among chapters.

d. There is a decline in membership in Regions 1–6.
   – Sheu commented that that the position of VP-Regions 1–7 had been created to stimulate chapter activity, and hopefully, in return increase membership.

e. Statistics on fluctuations in membership numbers.
   – Moschytz commented that the publications situation, which is now improving under the editorships of M.N.S. Swamy and C. Toumazou, plus the anticipated *CAS Magazine*, should be an attraction to potential members to join.
   – G. Friedman commented that he formed a Rochester (New York) Chapter jointly with EDS four years ago, followed through all the procedures, called "Piscataway", and still has not received approval from Headquarters.
   – Dunlop commented about chapters in Regions 1–7 and the uncertainty of these chapters not knowing where to report, and how the Society plays a role vs. the respective Sections.
   – On a different note, Dunlop suggested that the long RAD reports be limited to electronic format or the WWW. The report in the agenda and the separate RAD report are a duplication of the web site.
   – Gupta suggested that the Society identify which areas are going to be "hot" in the future and work through getting workshops and then turning them into conferences.

VI. **Report from the Past President and Chair, Awards Committee – G. Moschytz**

a. List of Society award recipients for year 2000 distributed as information item. (Published in the June 2000 issue of the *CAS Newsletter*.)

b. Acknowledgment and appreciation to A. Davies and T. Wehner for compiling and distributing the first CAS Society Directory (1999–2000).

c. Announced ("plugged") the next CAS Emerging Technologies Workshop scheduled for Hong Kong in December 2000. Another workshop is being planned for this series by W. Wolf. Encouraged all to submit ideas and continue this program. A Steering Committee for these workshops exists and falls under the purview of the Vice-President for Conferences.

VII. **Report from the IEEE Past President – K. Laker**

A comprehensive report on the status of the IEEE entitled "The Year in Review-1999" was presented by K. Laker. The report showed that IEEE is strong and vital, has enhanced value, and offers many services and products. In addition, a list of 1999 "accomplishments" was presented, all of which can be found on the IEEE web site at http://www.ieee.org.
   – Sheu inquired as to how IEEE field awards can be sponsored. Laker answered that, if CAS is interested, a proposal needs to be submitted to TAB.
   – Sheu also asked how CAS can be more closely aligned with "big" IEEE. Laker emphasized that this must be done through direct participation in TAB meetings by the Society president, and even in observation by the president-elect the year prior to the presidency.
   – Sheu thanked Laker for attending the meeting and giving a very informative presentation.

VIII. **Report from the Vice-President for Administration – I. Hajj**

a. Presented the financial status of the Society.

b. Announced that most of the reserve funds are being invested at cash/money market rate. In 1999, $1.5 million transferred to long-term investments.

Governors' Clipboard

Consulted with IEEE financial advisors and was informed that more can be placed into long-term investments.

Motion: Based on ExCom's recommendation, moved for approval to split the Society's reserves of approximately $7 million into a 50/50 situation ($3.5m cash/money mark and $3.5m long-term investment). **Passed unanimously**.

c. Presented the proposed 2001 budget. Discussion took place to change some line items. Moved to approve the proposed budget for 2001 as revised. **Passed with 2 abstentions.**

d. Announced that the 2001 initiatives of over $50K had to be submitted to IEEE already. They are the (1) production and distribution of annual CAS CD-ROM to all subscribers of at least one CAS transactions, and (2) cost of Newsletter to Magazine conversion. Both are pending FinCom, TAB and BOD approval.

IX. **Report from the Vice-President for Publications – G. De Micheli**

a. Information items:

– IEEE Xplore (up-and-running)

– IEEE Manuscript Central (recommends that all editors use this system)

b. Annual CAS CD-ROM

– The 1999 CD-ROM had been produced this year by Parity Computing.

– It is one CD-ROM for the year, instead of the two IEEE produced in the past.

– Contains the content of the *CAS-I/-II*, *CSVT*, and *CAD Transactions*.

– It is available for sale in year 2000 to subscribers.

The BOG voted in May'99 to give the annual CD-ROM free to members from 2001 on. However, after further research, there needs to be a consistency with the IEEE on-line policy, and also a way to maintain sales of all CAS transactions. Therefore, the issue of a free CD-ROM to all members needed to be revisited and proposed the following motion: Annual CD-ROM will be given free to those CAS members who subscribe to at least one of the CAS transactions, as of 2001 (content of year 2000 transactions). **Passed unanimously**.

c. ***TCAD* CD-ROM Compendium**. The *TCAD* compendium will be similar to the one that the Society already has for CAS, *CAS–I*, *CAS–II* and *CSVT*, and was given as a "gift" to ISCAS'99 attendees. The TCAD compendium is currently being produced by Kathy Preas and will contain all issues from inception to 1998 fitting onto approximately 7 CDs.

Proposed the following motion: Produce 1200 sets of the *TCAD* compendium, and distribute about 900 sets free to ICCAD 2000 attendees. Total estimated cost is $20K. **Passed unanimously**.

d. **CAS Magazine**

– The Society's plan has been to convert its newsletter into a magazine as of January 2001.

– The current newsletter is up to 48 pages per issue and in full color.

– The editor-in-chief of the newsletter is Mike Sain.

– ExCom approved to proceed with the conversion, and to devote $7/member to the CAS magazine (up from $4).

– CAS magazine would be given free to all CAS.

– Issues were raised by IEEE Financial Committee (FinCom) about the proposed budget showing a loss, and also having CAS charge only $7 vs. a typical $19 for societies that include magazines with membership.

– Another concern is the situation with co-sponsorship of the *C&D Magazine*. Sheu will contact the presidents of the other C&D sponsors, namely LEOS and EDS, to discuss the creation of the CAS magazine and how the two would be independent of each other.

After discussion, a 5-part motion was put forth:

1. That *CAS Newsletter* be transformed into a CAS magazine as of January 2001 to be given for free to all CAS members.
2. That $7 of CAS membership would be devoted to the CAS magazine.
3. That CAS would consider to raise membership fees up to $10 in 2002 if this were necessary to reduce CAS magazine deficit.
4. That an Editorial Board be established now, representing all aspects of the Society.
5. That the EIC of the newsletter/magazine would attend the BOG and Publication Division meetings in 2000 and 2001 to report progress, timeliness and format of the magazine, and discuss comments and suggestions from BOG members.

Passed with 4 abstentions.

X. **Regional Reports – A. Davies, J. Cousseau, and T. Ng** Region 8, 9, and 10 reports prepared by A. Davies, J. Cousseau, and T. Ng, respectively, are included in the general RAD Report. T. Ng, VP-Region 10, announced two important upcoming events this year:

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Governors' Clipboard

BOG Report … continued from Page 43

1. CAS Emerging Technologies Workshop – Third Generation Mobile Technologies and Applications, to be held in Hong Kong in December 2000.
2. APCCAS 2000 to be held in Tianjin, China, also in December 2000.

XI. **Report from the Vice-President for Conferences – G. De Veirman**

a. Presented summary of loans and grants approved for 2000 and 2001.

b. Presented summary of conference closures with discussion of penalty structure and fines paid to date.

c. Presented summary of all conferences which still have not closed their books.

d. Announced CAS Society Liaisons to the following conferences:
- ICCAD 2000 – Georges Gielen
- ECCTD 2001 – Hari Reddy
- ISCAS 2001 – Martin Hasler

e. Announced that the Solid-State Circuits Society (SSCS) has approached the DAC Executive Committee to request possible co-sponsorship. De Veirman will form a committee to determine how to best serve the CAD community with DAC surplus in order to provide added value from the CAS Society.

f. Further discussion ensued about concern over loss or reduction of DAC sponsorship. A straw vote was requested by Friedman to determine the BOG's stance on this matter and ensure that the CAS representative to DAC conveys this viewpoint.

g. Sheu suggested providing IEEE member mailing list to DAC to help increase exposure.

h. Society should be able to contribute to expansion of DAC monetarily.

i. **ISCAS Cycle beyond 2000**. Clarification.

Motion 1: Of the two consecutive ***Regions 1–7**** (old: USA)/Open sites, the preference for one of the two years will be given to a qualified proposal from ***Regions 1–7**** (old: USA). **Passed with 1 abstention**. *(* Regions 1–7 include USA **and** Canada.)*

Motion 2: In addition, when the ISCAS Steering Committee makes the selection for the Regions 1–7/Open sites, it is ***mandatory*** that there be a one year presence of ISCAS in Regions 1–7. **Passed unanimously**.

j. Mentioned briefly the Thematic Workshops/Emerging Technologies Workshops. There is interest in holding these. Some areas and organizers have already been identified and others have been suggested. Encouraged all to submit ideas and participate.

k. D. Skellern, ISCAS'01 general co-chair, gave a brief report. Everything is going according to plan. However, a 10% Goods & Services tax is being introduced in Australia, and Skellern warned that at this time the projected figures show the conference will just break even.

XII. **Report from the Vice-President for Technical Activities – M. Zaghloul**

a. Announced that all Technical Committees submitted reports this year; they appear in the Agenda.

b. Announced new initiatives of the TA Division:
- State-of-the-art articles to *CAS Magazine*
- Review of emerging technologies and their relation to CAS Technical Committees (TCs)
- Coordinate TC workshops
- Oversee educational activities

c. TC on Cellular Neural Networks & Array Computing (CNNAC) has proposed a bi-annual Young Researcher Contest.

d. TC on Computer-Aided Network Design (CANDE) submitted a request to the Society to establish an IEEE/CAS ICCAD Best Paper Award in the name of William (Bill) McCalla, one of the co-founders of the conference. The following motions were put forth by Dunlop on behalf of CANDE:

Motion 1: IEEE/CAS to create the William J. McCalla ICCAD Best Paper Award**. Passed with one abstention.**

Motion 2: The Society will establish an endowment at IEEE in the amount of $50K for the McCalla Award. **Passed with two abstentions**.

XIII. **New Business**

a. **Society Awards**. Dunlop moved that the Society double the amount of each of the CAS Society awards due to the amounts being antiquated. **Passed unanimously**.

b. **Nominations Committee**. R. De Figueiredo, chair, announced that nominations are being solicited for both BOG and officer elections.

c. **Next Meeting**. The next meeting of the BOG will be held on Sunday, 5 November 2000, in San José, California, in conjunction with ICCAD.

XIV. **Adjournment**. The meeting adjourned at 6:20 p.m.

Respectfully submitted,
Barbara Wehner
Administrator

Call for Papers and Participation

The 2nd Workshop and Exhibition on MPEG-4

June 18 – 20, 2001 San Jose, California, USA

The first Workshop and Exhibition on MPEG-4 was a great success. To continue this highly successful activity, the Second Workshop and Exhibition on MPEG-4 will be held from June 18 to June 20, 2001, in San Jose, California, U.S.A.

Technical Papers Author's Schedule:

Deadline for Submission of Papers:	January 15, 2001
Notification of Acceptance:	March 15, 2001
Deadline for Submission of Final Papers:	April 15, 2001

Authors should use the following address for electronic submission of papers:
http://www.mpeg4.engr.scu.edu

Demonstration/Exhibition

Prospective contributors should use the following address for electronic submission of their abstracts for demonstration/exhibition by March 15, 2001: **http://www.m4if.org**

Contact Information

For technical papers:	*For exhibitions:*	*For general information:*
Prof. Ming-Ting Sun	Rob Koenen	Weiping Li
Electrical Engineering Dept.	KPN Research	WebCast Technologies, Inc.
University of Washington	P.O.Box 421	257 Castro St. Suite 209
Seattle, Washington 98195	2260 AK Leidchendam	Mountain View, CA 94041
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Phone: (206) 616–8690	Phone: +31 70 332–5310	Phone: (650) 210–9188
Fax: (206) 543–3842	Fax: +31 70 332–5567	Fax: (603) 250–2287

FIRST CALL FOR PAPERS

2001 Midwest Symposium on Circuits and Systems

August 13-17, 2001
Dayton, Ohio

The Midwest Symposium on Circuits and Systems (MWSCAS) is one of the premier IEEE conferences presenting research in all aspects of theory, design, and applications of circuits and systems.

All papers will be reviewed via the Program Committee. Nominations will be solicited for the Myril B. Reed Best Paper Award , and selection and conferring of the best student paper award, and other newly established awards will be celebrated.

Papers must be received no later than March 30, 2001 via electronic submission or at the following address for 5 hardcopies: **Dr. M. Ismail, Ohio State University, 205 Dreese Laboratory, 2015 Neil Avenue, Columbus, OH 43210–1272**.

Deadlines:

Tutorial, Panel, or Industrial Track proposals	March 2, 2001
Special Session proposals	March 2, 2001
Submission of Papers	March 30, 2001
Notification of Acceptance	May 18, 2001
Final Camera-ready paper	June 15, 2001

For further updated information, please see the symposium website:
http://www.ececs.uc.edu/~hcarter/mwscas/

EUROIMAGE 2001

International Conference on Augmented, Virtual Environments and 3D Imaging

May 30–June 1, 2001 Mykonos, Greece
http://www.iti.gr/icav3d/

Call for Papers

The International Conference on Augmented, Virtual Environments and Three-Dimensional Imaging is organized by the European Union IST INTERFACE project in collaboration with the European Association for Speech, Signal and Image Processing (EURASIP). A special session on mixed reality technologies will be organized by the IST ART.LIVE project.

Prospective authors are invited to submit 3 copies of an extended summary of no more than 3 pages to:

Prof. Michael G. Strintzis
Informatics and Telematics Institute
1 Kyvernidou Str.
54639 Thessaloniki, Greece
Tel.: +30.31.996351
Fax: +30.31.996342
E-mail: strintzi@eng.auth.gr

Authors' schedule:

January 10, 2001:	Submission of extended summaries
February 15, 2001:	Notification of acceptance
March 15, 2001:	Receipt of camera-ready paper

Submission may also be accomplished by:

e-mail: postscript file to ICAV3D@iti.gr
ftp: ftp.iti.gr USER:anonymous cd pub/icav3d put <author_name>.ps

CALL FOR PAPERS

ICME2001

IEEE International Conference on Multimedia and Expo

August 22–25, 2001 Waseda University, Tokyo, Japan

International Conference on Multimedia & Expo (ICME) is a major annual international conference organized with the objective of bringing together researchers, developers and practitioners from academia and industry working in all areas in multimedia.

Authors should submit a four-page manuscript in double-column format including authors' names, affiliations and a short abstract. Only electronic submission (in pdf or postscript format) will be accepted. **Electronic submission procedure can be found in the ICME2001 webpage indicated below.**

Important dates:

Submission of Regular Papers:	January 15, 2001
Notification of Acceptance:	On or about April 20, 2001
Camera Ready Copy:	May 31, 2001
Proposals for Special Sessions and Tutorials:	March 1, 2001
Notification of Acceptance (for Proposals):	April 15, 2001

Applications for Exposition: Please contact ICME2001's office at the address indicated below.
Conference Webpage: http://www.giti.waseda.ac.jp/ICME2001/
ICME2001 office: icme2001@giti.waseda.ac.jp

< < Call for Papers > >

Special Issue of *IEEE Transactions on Multimedia* on Multimedia Database

In recent years there has been a large amount of activity in the area of indexing, search, retrieval and manipulation of multimedia data. A variety of techniques from various disciplines such as image and video processing, computer vision, audio and speech processing, statistical pattern recognition, and learning theory and database research have been employed. This research, to a large extent, includes and goes beyond activities of standards committees. Joint multimodal processing by combining multiple modalities such as audio, video, text etc., is also being used.

Original papers are being solicited in the general area of query, search, indexing, retrieval and mining of structured and unstructured multimedia/multimodal information including the areas of authentications and hiding of such data.

Authors should follow the *IEEE Transactions on Multimedia* manuscript format, a description of which is available on the inside back cover of the transactions.

Schedule:

Manuscript submission deadline:April 1, 2001
Acceptance notification:October 1, 2001
Final manuscript due: December 1, 2001
Publication: March 2002

Guest-editors for the special issue are:

Dr. Sankar Basu
IBM T. J. Watson Research Center
Yorktown Heights, New York 10598
sbasu@us.ibm.com

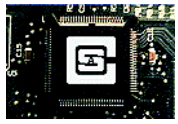
Prof. Alberto Del Bimbo
University of Florence, Italy

Prof. Ahmed Tewfik
University of Minnesota, USA

Dr. Hong-Jiang Zhang
Microsoft Research, P. R. China

Please submit manuscript to Dr. Sankar Basu at the above address.

IEEE 2nd Dallas CAS Workshop on Low Voltage Mixed Signal Circuits and Systems



Monday, 26th March 2001
Dallas, Texas

The IEEE 2nd Dallas CAS Workshop on Low Voltage and Low Power Mixed-Signal Circuits & Systems is being conducted under the aegis of the **IEEE Dallas Section, Circuits & Systems Society**. The workshop will include invited lectures and poster sessions. Leading experts Dr. John Choma, Dr. Randall Geiger, Dr. Franco Maloberti, and Dr. Jaime Ramírez-Angulo will present the latest techniques and challenges involved in low power RF design, low voltage analog circuits, low voltage sigma-delta and nyquist rate data converters. Prospective authors are invited to submit a one-page summary of their posters reporting original work in the area of low voltage/low power mixed-signal design.

General Chair:
Dr. Gabriele Manganaro
gabriele.manganaro@ieee.org

Technical Chair:
Dr. Joseph Varrientos
joseph.varrientos@dalsemi.com

Registration Chair:
Dr. Oscar Moreira-Tamayo
omoreira@ti.com

For further information visit:
http://ewh.ieee.org/soc/cas/dallas/wks2

Dallas

ACM International Symposium on Physical Design

April 1–4, 2001
Sonoma County, California

The International Symposium on Physical Design provides a forum to exchange ideas and promote research on critical areas related to the physical design of VLSI systems. All aspects of physical design, from interactions with synthesis to back-end performance analysis, are within the scope of the Symposium. Following its nine predecessors, the 2001 symposium will highlight key new directions and leading-edge theoretical and experimental contributions to the field.

General Chair
Manfred Wiesel
manfred.wiesel@email.msn.com

Technical Program Chair
Sachin Sapatnekar
sachin@ece.umn.edu

WEB PAGE: **www.ispd.cc**

California

2001 SOUTHWEST SYMPOSIUM ON MIXED-SIGNAL DESIGN

February 25–27, 2001
Austin, Texas, U.S.A.

General Chair
John Choma, Jr.
Univ. of Southern California

General Co-Chair
Jo Dale Carothers
Univ. of Arizona

Program Chair
Franco Maloberti
Texas A&M Univ.

Overview

The 2001 Southwest Symposium on Mixed-Signal Design will bring together researchers in academia, industry, and government from the areas of CAD tools and mixed-signal circuit design. This will allow not only the presentation of the latest developments in each field, but also interaction between the areas in order to expedite the development of improved integrated systems and "systems on a chip".

Further Information

For details on the electronic submission procedure, please go to
http://www.ece.arizona.edu/conferences/ssmsd

Austin

8th IEEE International Conference on Electronics, Circuits and Systems

ICECS'01

September2–5, 2001
The Westin Dragonara Resort, Malta
http://www.eng.um.edu.mt/microelectronics/icecs2001

ICECS 2001, the 8th IEEE International Conference on Electronics, Circuits and Systems is a major international conference which includes regular, special and poster sessions on topics covering analogue circuits and signal processing, general circuits and systems, digital signal processing, VLSI, multimedia and communication, computational methods and optimization, neural systems, control systems, industrial and biomedical applications, and electronic education.

General Chair
Dr. Joseph Micallef
Dept. of Microelectronics
University of Malta
E-mail: jjmica@eng.um.edu.mt

Technical Program Chair
Prof. Franco Maloberti
Dept. of Electrical Engineering
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E-mail: franco@ele.unipv.it

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Malta

38th Design Automation Conference

June 18–22, 2001
Las Vegas
Convention Center
Las Vegas, Nevada

The Design Automation Conference (DAC) is the premier Electronic Design Automation (EDA) and silicon solution event. DAC features over 50 technical sessions covering the latest in design methodologies and EDA tool developments and an Exhibition and Demo Suite area with over 250 of the leading EDA, silicon and IP Providers.

General Chair
Jan Rabaey
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EECS Dept.-Cory Hall
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(510) 666-3111
jan@eecs.berkeley.edu

Exhibits Manager
MP Associates, Inc.
5305 Spine Rd., Ste. A
Boulder, CO 80301
(303) 530-4562
lee@mpassociates.com

Web site:
http://www.dac.com

Las Vegas

Baltimore

2001 IEEE-EURASIP Workshop on NONLINEAR SIGNAL AND IMAGE PROCESSING

June 3–6, 2001
Hyatt Regency Baltimore
Baltimore, Maryland USA
http://www.ece.udel.edu/nsip/

NSIP-01 is the fifth biennial international workshop on nonlinear signal and image processing. Check the web site for up-to-date information on paper proposals and status, workshop registration, special sessions, keynote speakers, and travel information.

Conference Chairs

Kenneth Barner
University of Delaware
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Gonzalo Arce
University of Delaware
Tel: +1–302–831–8030
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"Gh. Asachi" Technical University of Iasi
Bd. Carol 11, Iasi, 6600, ROMANIA

Secretariat:
Phone: +40 32 142283
FAX: +40 32 217720 or +40 32 278628

The Fifth International Symposium on Signals, Circuits and Systems

July 10–11, 2001 **Iasi, Romania**

The fifth edition of the International Symposium on Signals, Circuits and Systems will be held in Iasi at the Faculty of Electronics and Telecommunications, Technical University "Gh. Asachi". Iasi, the oldest academic center of Romania, is located in the North-Eastern part of the country and can be reached from Bucharest by plane or by train. A wine tasting and a one day post symposium trip in the neighboring region, well known for its wonderful monasteries, will be organized.

Other information:
http://www.tuiasi.ro/events/scs2001
http://www-imt.unine.ch/scs2001
lgoras@etc.tuiasi.ro (Prof. Liviu Goras)

Romania

CAS 2001 Election Results

The votes have been counted for the election of Officers and of five members to the IEEE Circuits and Systems Society Board of Governors. The following candidates have been elected.

Officers for a One-Year Term Beginning January 1, 2001

President-Elect	**Josef A. Nossek**

Officers for a Two-Year Term Beginning January 1, 2001

Administrative Vice President	**Ibrahim N. Hajj**
Vice President-Publications	**M. N. S. Swamy**
Vice President-Regions 1–7	**Wasfy B. Mikhael**
Vice President-Region 10	**Nobuo Fujii**

BOG Members for a Three-Year Term Beginning January 1, 2001

Andreas G. Andreou
Robert J. Marks, II
Massoud Pedram
Ljiljana Trajkovic
Ellen Yoffa

We wish the newly elected officers and members of the Board of Governors success and thank all candidates for their willingness to serve and for permitting their names to be included on the ballot.

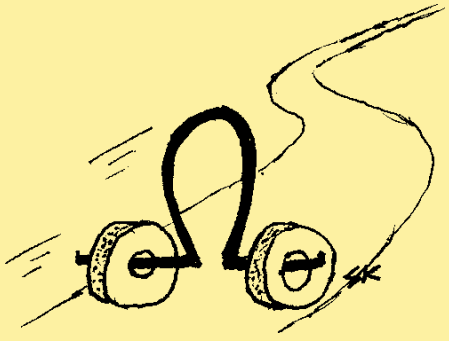
—Mary Ward-Callan, Managing Director
IEEE Technical Activities

$ CAS AWARDS UPGRADE $

Notice: Since the announcement of the call for nominations for the CAS Awards in the *CAS Newsletter*, the IEEE has approved a request to double the cash amount for each of the Awards that include a cash prize, beginning with the awards offered in 2001. Therefore, the cash amount for the Meritorious Service Award, the Technical Achievement Award, the Industrial Pioneer Award, the Education Award, and the Chapter-of-the-Year Award is $1,000. The Mac Van Valkenburg Award cash amount has been raised to $2,000 and the cash prize for the Best Paper Awards are $500 for each author up to a maximum of $2,000.

THE ADVENTURES OF …
…THE 'UMBLE OHM

…Shlomo Karni



Re-tired and going 'ohm.

IEEE CAS Newsletter

The Circuits and Systems Society's homepage web site is: http:// www.ieee-cas.org

IEEE Circuits and Systems Society Newsletter

Fellows Nominations … continued from Page 40

candidate's technical qualifications and contributions. All material is then forwarded in confidence to the IEEE Fellow Committee. The main task of the IEEE Fellow Committee is to recommend candidates to the Board of Directors, in accordance with the following criteria: 1) individual contributions as engineer-scientist originator, technical leader or educator; 2) evaluation by the Society/Council selected by the nominator; 3) evidence of technical accomplishment, such as publications (including internal company reports), patent and peer recognition; 4) confidential opinions of references; 5) service to other professional engineering societies; 6) total years in the profession.

To obtain an IEEE Fellow Nomination Kit, contact the IEEE Fellow Committee via Telephone: (732) 562-3840, Fax (732) 981-9019, or E-mail: fellow-kit@ieee.org. All completed forms for Fellow nominations must be received by the IEEE Fellow Committee no later than March 15, 2001. For more information, see http://www.spectrum.ieee.org/INST/feb97/become.html. The CAS Fellow Awards Committee can also provide information regarding CAS Fellow grade members. Contact Wai-Kai Chen, Chairman, CAS Fellow Awards Committee, University of Illinois at Chicago, Department of Electrical Engineering and Computer Science, Chicago, IL 60607, Tel: (312) 996-2462, Fax: (312) 355-1141, and E-mail: w.chen@ieee.org.

Recent Advances … continued from Page 20

Level Interconnect Prediction, pp. 85–90, April 2000.

[51] OIIC Systems Demonstrator, http://www.elis.rug.ac.be/~jvc/oiic/sysdemo.htm.

2001 IEEE International Symposium on Circuits and Systems

May 6–9, 2001

Sydney Convention and Exhibition Center
Darling Harbor, Sydney, Australia

SYSTEMS of CIRCUITS and MIXED TECHNOLOGY ELEMENTS

The 2001 IEEE International Symposium on Circuits and Systems will be held in Sydney, Australia. The Symposium is sponsored by the IEEE Circuits and Systems Society.

The Symposium will include: regular sessions; plenary sessions on advanced aspects of theory, design and applications of circuits and systems; and short courses/tutorials linked with special sessions on wireless, mixed technology systems engineering, high speed devices and modelling, signal and video processing, and low power high speed VLSI design.

Web Site: http://www.iscas2001.org/

CONFERENCE CO-CHAIRMEN:

Professor David Skellern
Electronics Department (E6A 247)
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