

SWISS ORIGINS OF VERY LOW-POWER INTEGRATED CIRCUITS

(1962-1982)

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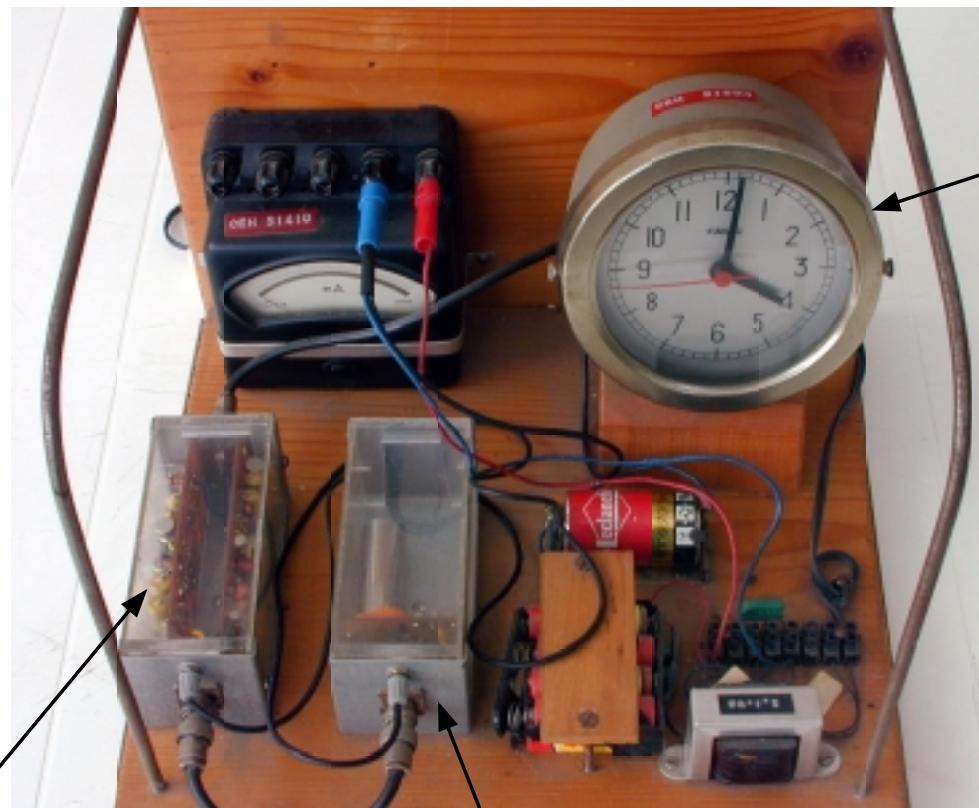
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Gala Special Talk, ESSDERC-ESSCIRC'06, Montreux, Switzerland

1962: FOUNDATION OF CEH

- Objective: Develop an electronic wrist-watch with at least one advantage with respect to existing watches.
- Status:
 - single-transistor battery watches with
 - balance-wheel time base
 - sonic tuning fork (Bulova's Accutron)
 - quartz marine chronometers (1.5 dm^3 , $>100\text{mW}$).
- Challenge for an electronic wrist-watch:
 - reduce volume to 3 cm^3
 - reduce power by factor 10'000 to less than $10 \mu\text{W}$
 - single 1.35 V mercury button cell.

LOW-POWER DEMONSTRATOR (1962)



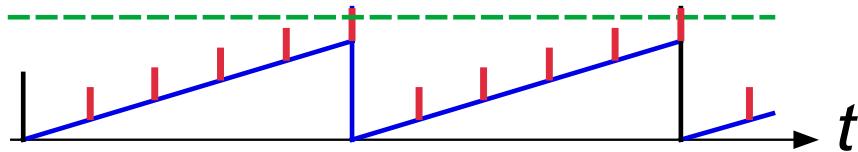
- 4 divide-by-ten stages
(synchronized multivibrators)
 - 10kHz quartz oscillator
- mW-level stepping-motor

FIRST DEVELOPMENTS (1962-1965)

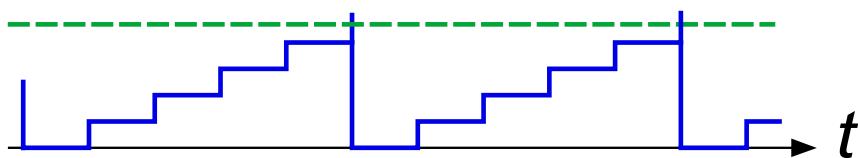
- Building-up of dedicated IC facilities and process.
- Search for adequate time base (precision 10ppm)
 - metallic resonators with tranducers
 - miniaturized quartz resonators.
- Search for adequate display
 - electromechanical (electro-magnetic, piezoelectric).
- Search for **frequency division** techniques
 - analog (low component count)
 - digital.

ANALOG FREQUENCY DIVISION

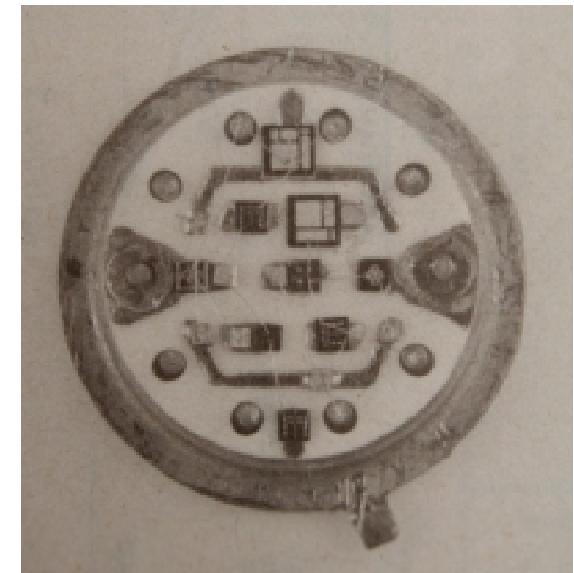
- Synchronized oscillators: $N < 10$



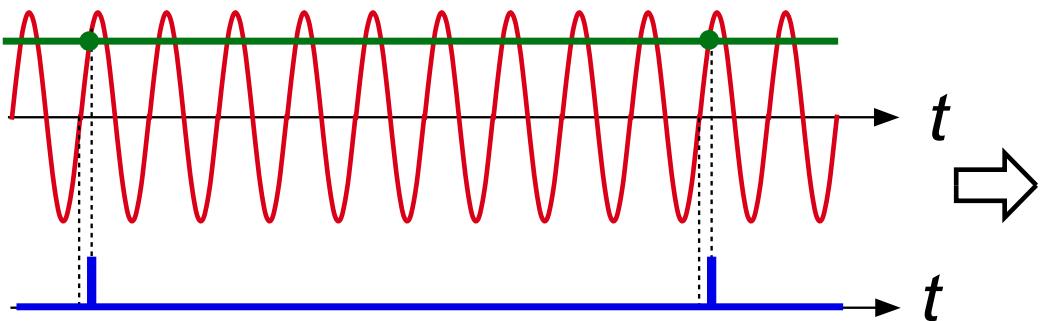
- Accumulation (charge, flux): $N < 10$



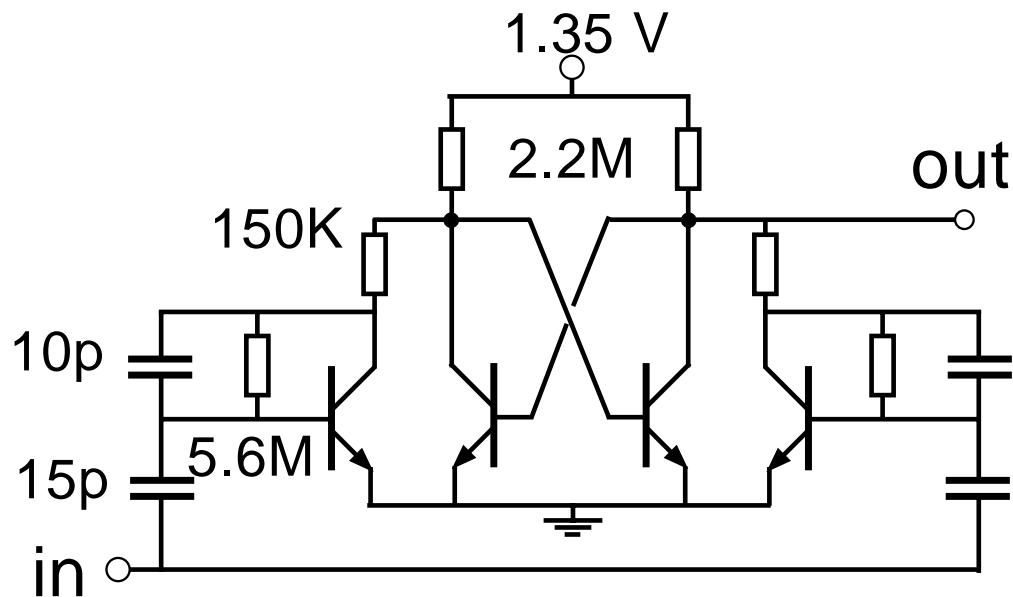
CICC'64



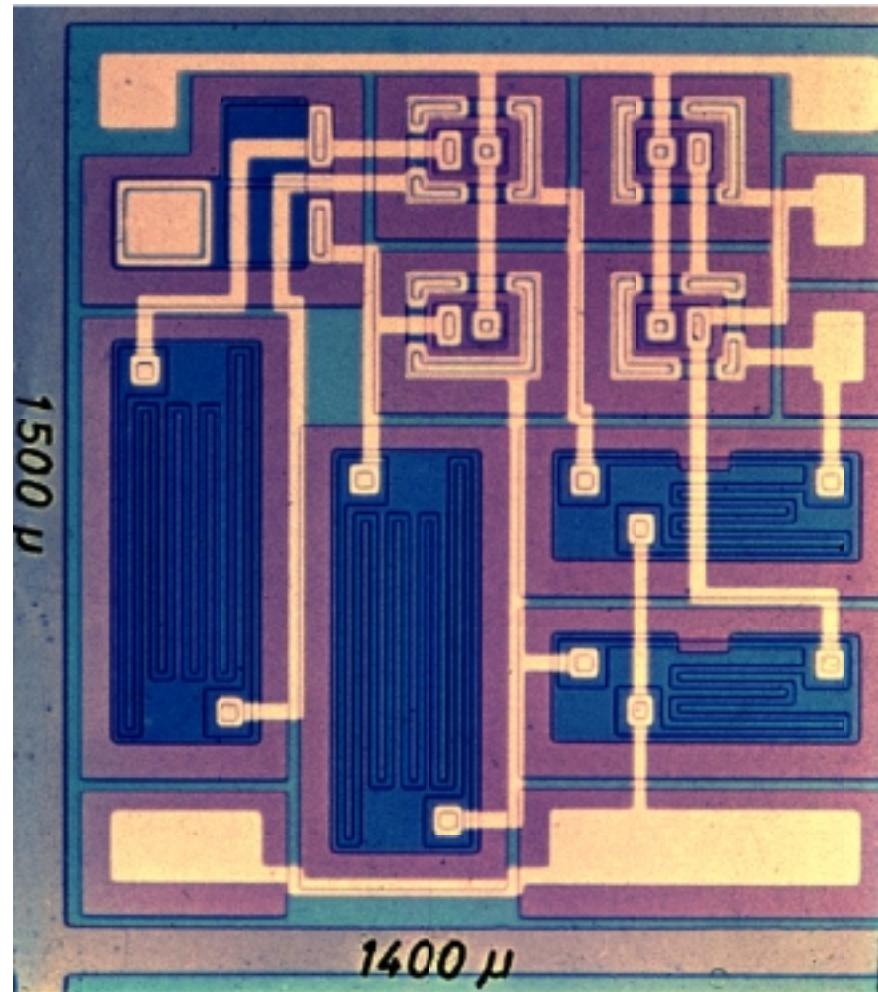
- Phase-lock loop divider: $N=1000$



FIRST DIGITAL FREQUENCY DIVIDERS (1966)

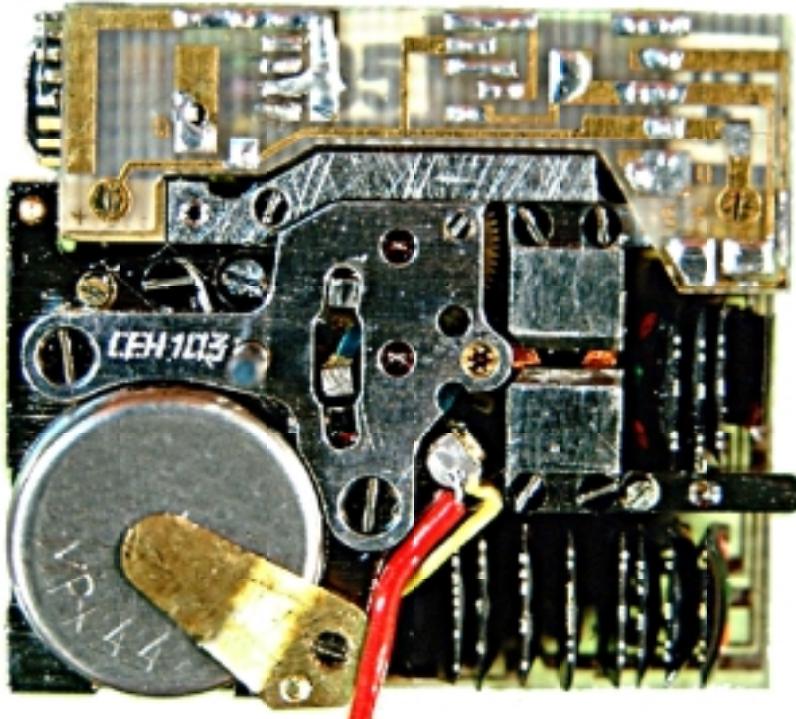


- ~10 micron bipolar process
- bidiffused resistors
- junction capacitors
- $f_{\max} \approx 5 \text{ kHz}$ for $1\mu\text{A}$
- breadboard "simulation".

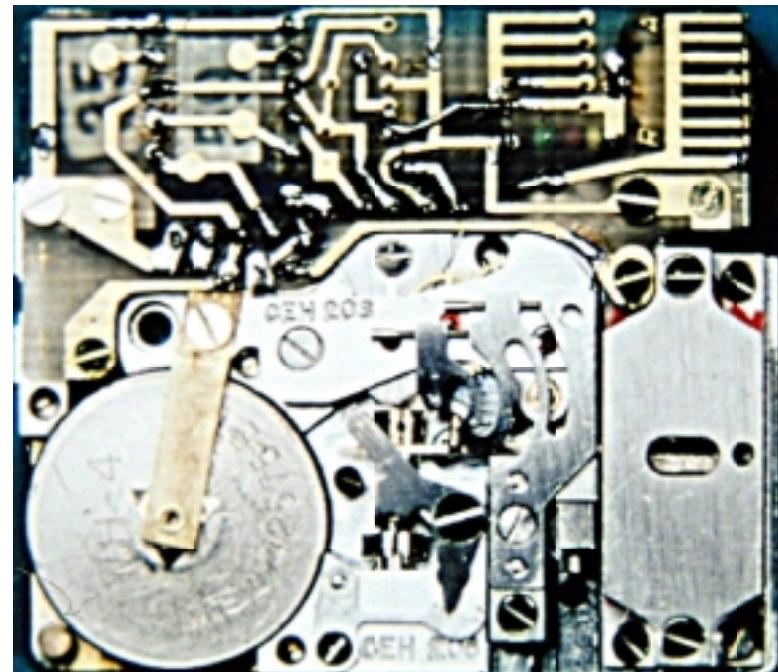


FIRST ELECTRONIC WATCH PROTOTYPES (1967)

- Resonator: quartz cantilever, 8192 Hz



Beta 1

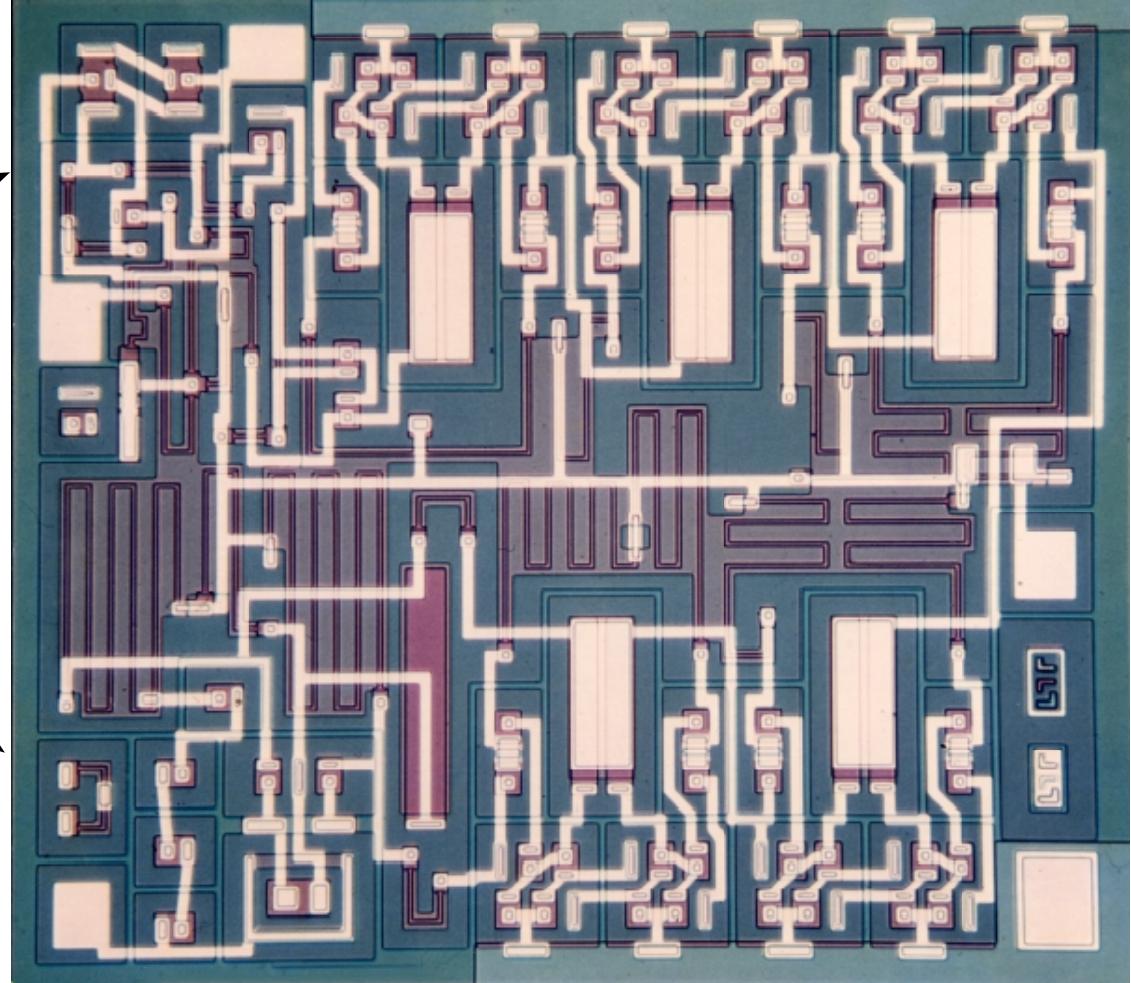


Beta 2

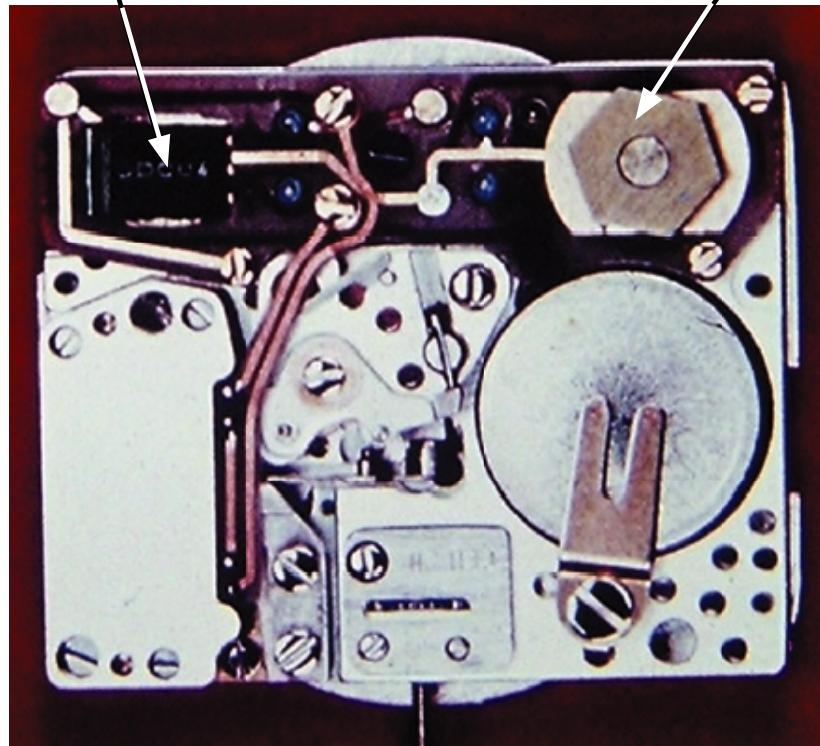
- 13 binary divider stages
- 1 Hz stepping motor.
- Pulverized all records at annual chronometry competition.
- 5 binary divider stages
- 256 Hz vibrating motor+ratchet.

FIRST LSI CIRCUIT FOR A WATCH (1970)

- 8192 Hz oscillator
- 5 stage binary divider
- motor driver
- 110 components
- 8.7 mm^2
- $12\mu\text{A}$ @ 1.3 V.



FIRST PRODUCTION WATCH (1970)



Beta 21



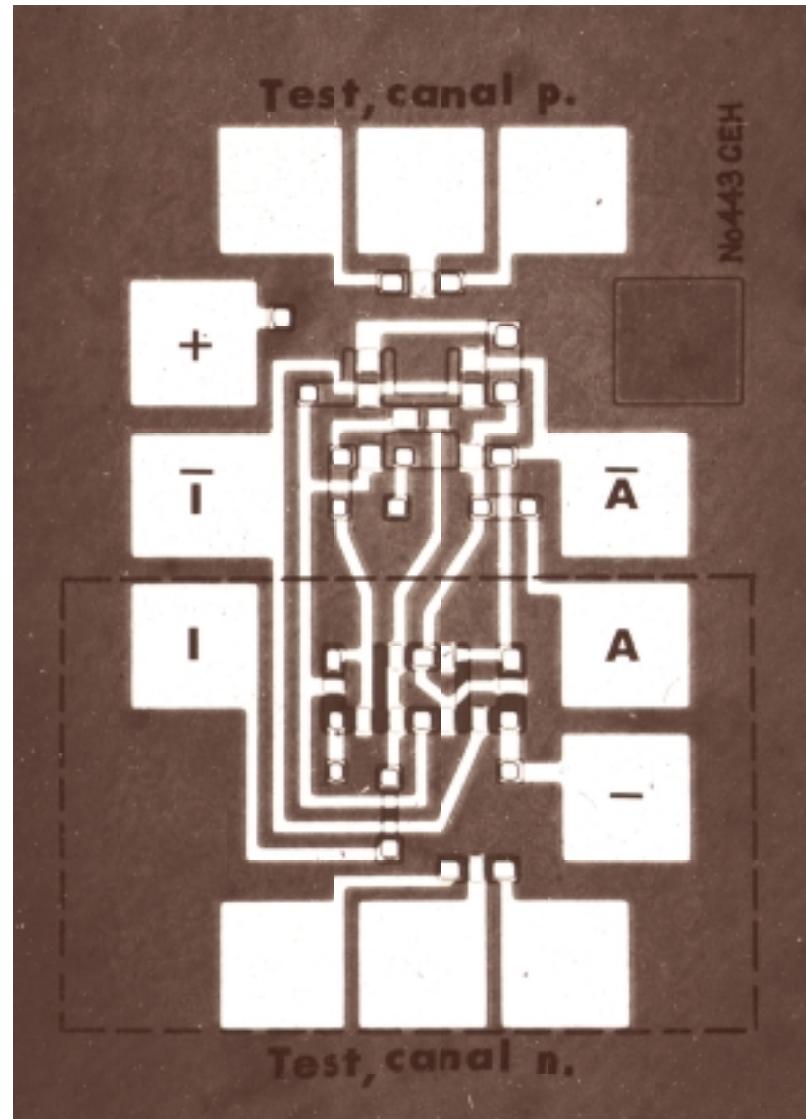
FIRST LOW-VOLTAGE CMOS BINARY DIVIDER (1968)

(F. Leuenberger and E. Vittoz, Proc. IEEE, Sept. 1969)

- 10 μ CMOS process, 7 μ m channel
- etched and refilled p-well
- molybdenum-gold gates
- direct Huffman synthesis by 2-level gates:

$$A = \overline{\overline{B}} \textcolor{red}{I} + \overline{A} \textcolor{red}{\bar{I}}$$
$$B = \overline{\overline{B}} \textcolor{red}{I} + A \textcolor{red}{\bar{I}}$$

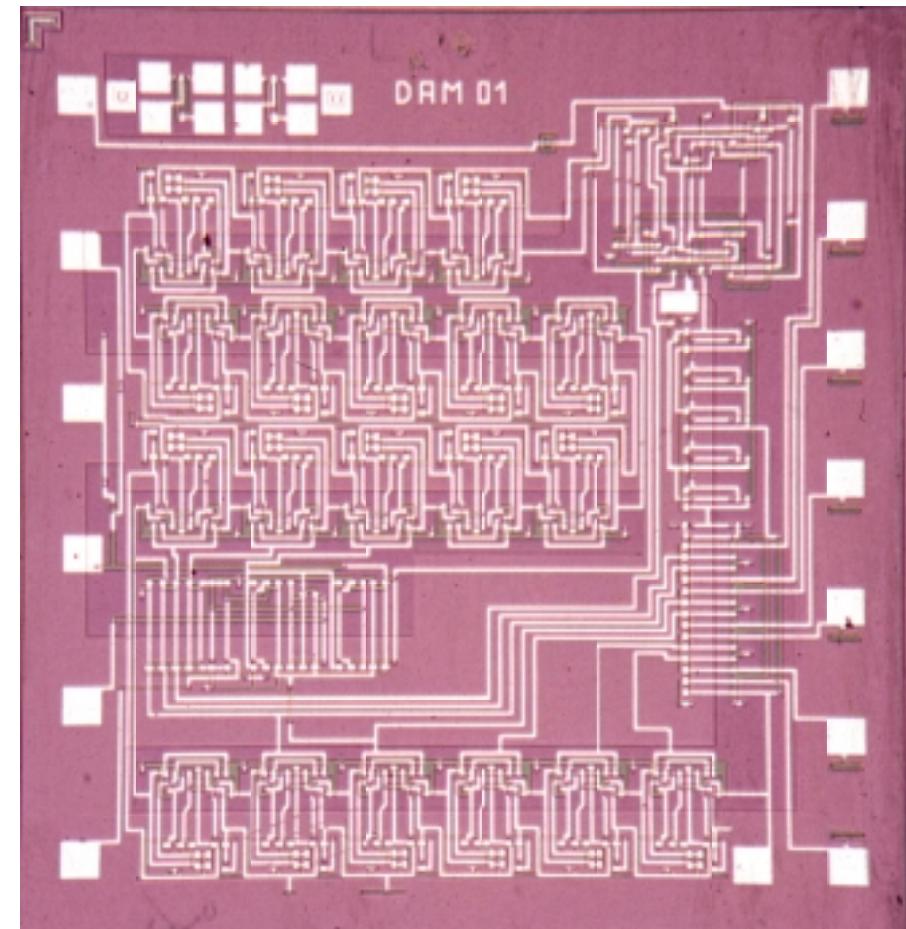
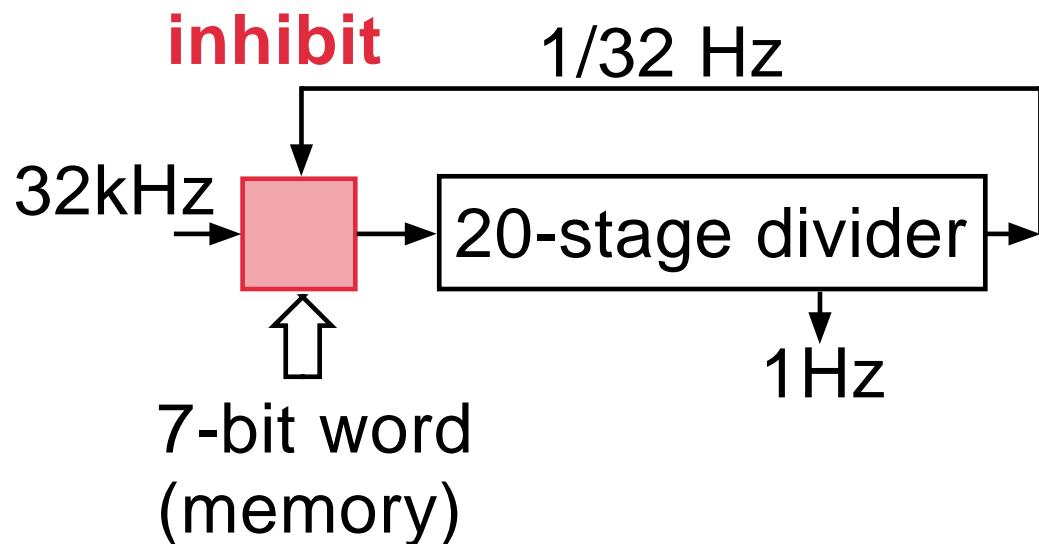
- 16 transistors per stage
- 10nA/kHz , } at 1.35 V.
- $f_{max}=200\text{kHz}$



DIGITAL FREQUENCY ADJUSTEMENT (1971)

("digital tuning")

- Goal: eliminates trimmer

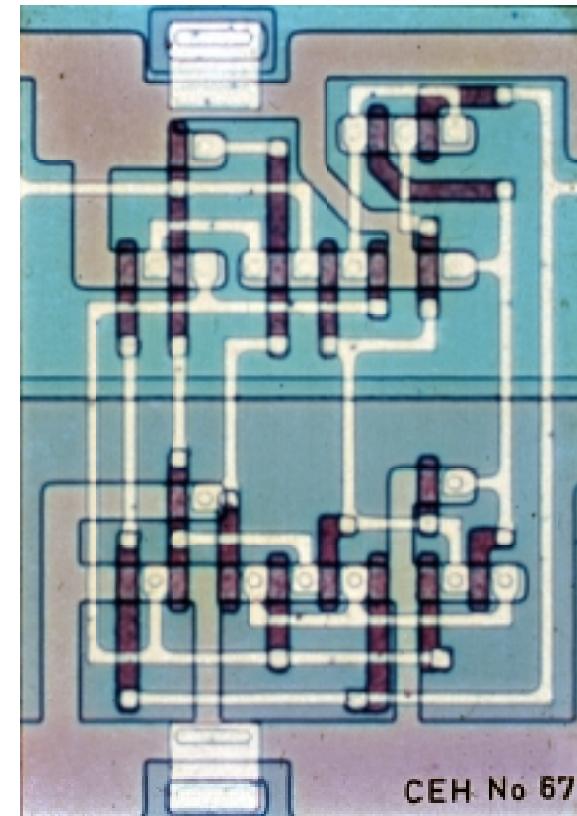


- Manual rubilith cut and peel !!!
- 0.45 μ A at 1.5V.

RACE-FREE DIVIDER CELLS (1972)

- Goals:
 - increase robustness
 - reduce power
 - single input (single clock)
- Systematic computer search
(IBM 1130, punched cards!)
- Result:
 - 1 structure with 4 gates
 - 9 structures with 5 gates
- Best structure:

$$\begin{aligned}A &= \overline{I}\overline{C} \\B &= \overline{A(I+D)} \\C &= \overline{AB} + \overline{IE} \\D &= \overline{B} \\E &= \overline{C}\end{aligned}$$

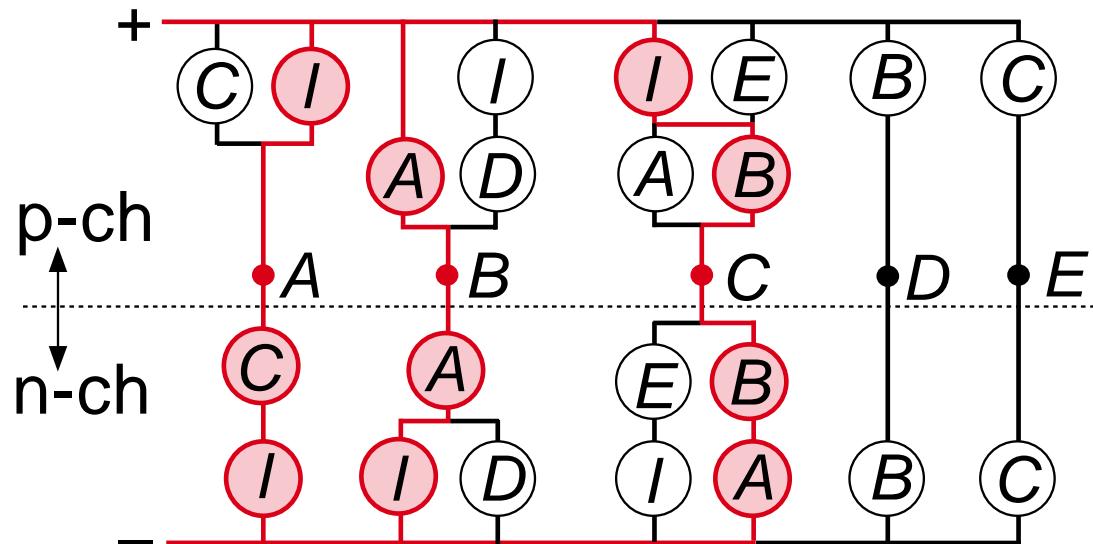


- Si-gate, $L=5\mu\text{m}$
 - 1.2 nA/kHz
 - $f_{max}= 2\text{MHz}$
- } at 1.35 V

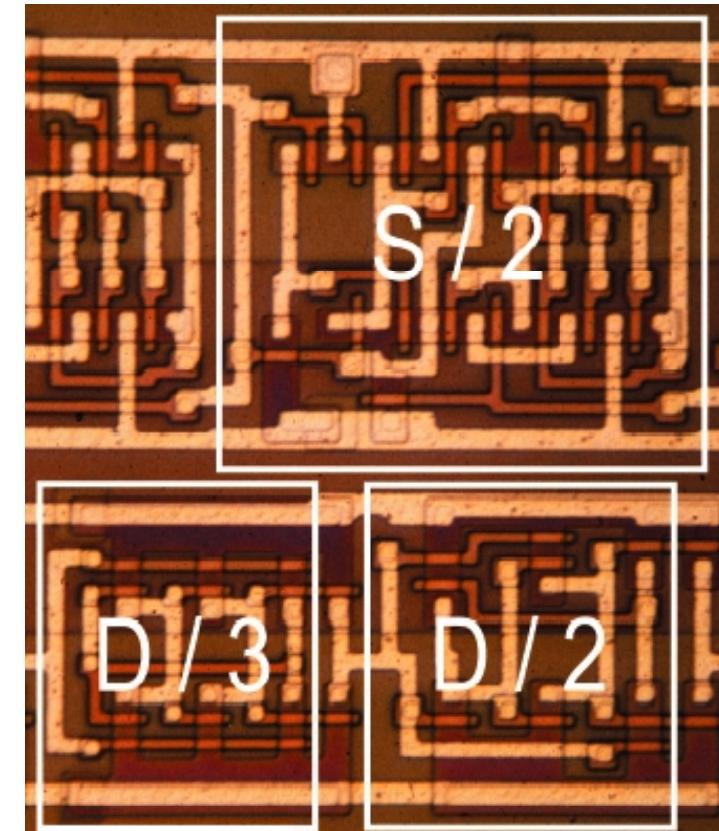
- Synthesis method for race-free cells by Ch. Piguet (late 70's)

COMPLEMENTARY DYNAMIC MOS DIVIDERS

- H. Oguey, 1972: Keep only transistors producing transitions.
- Example of divide-by-two:



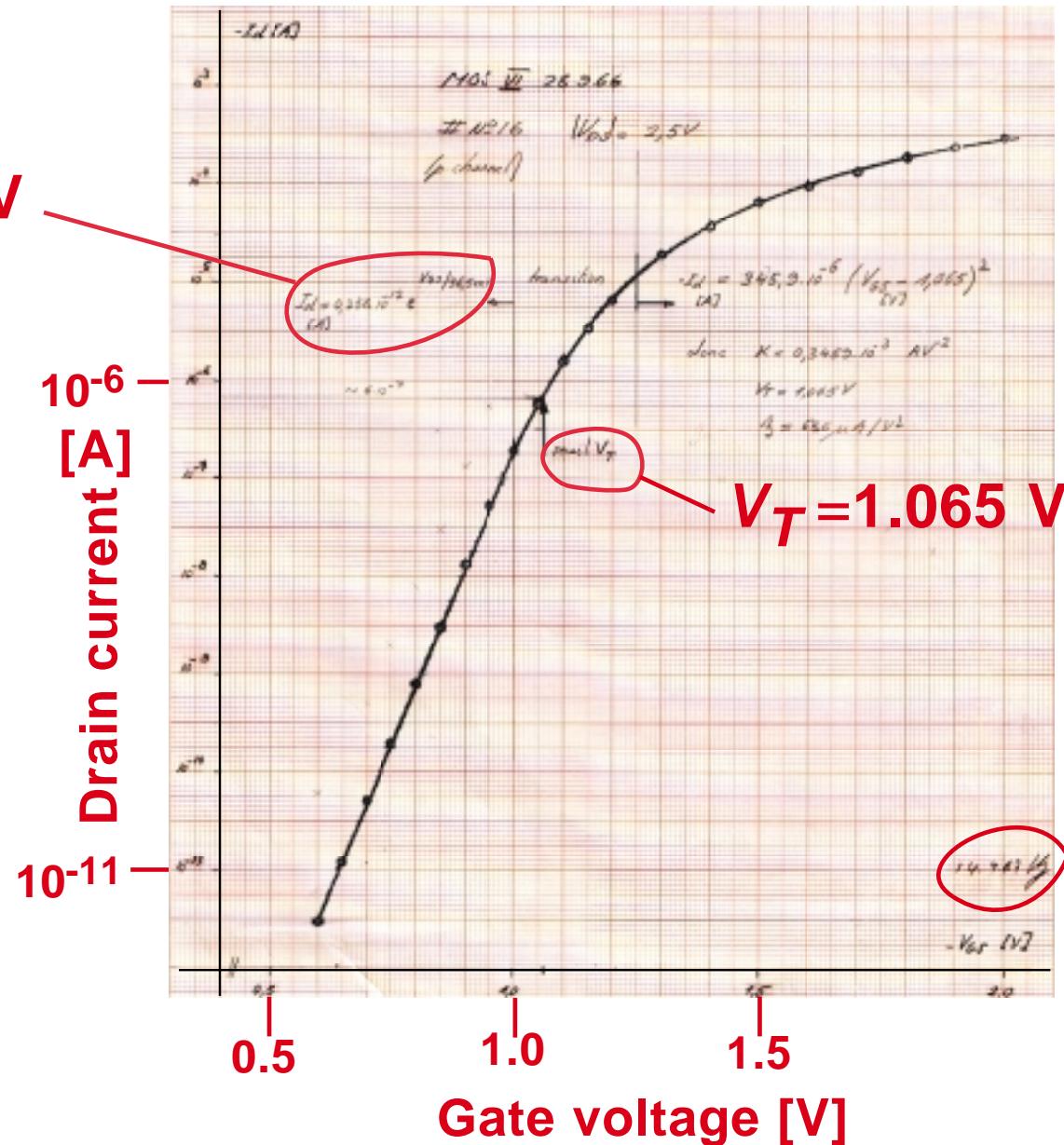
static: 22 transistors
dynamic: 10 transistors



- Systematic synthesis of dynamic dividers.
- Extension to other cells (single-clock D and JK flip-flops).

MOS TRANSISTOR AT VERY LOW CURRENT

$$I_D \propto e^{V_{GS}/36.5\text{mV}}$$



PUBLICATIONS ON WEAK INVERSION (OR SUB-THRESHOLD)

1972: M.B.Barron

1972: R.M. Swanson and J.D. Meindl

1973: R.R. Troutman and S.N.Chakravarti

1973: R.J. Van Overstraeten *et al.*

1974: T.Masuhara *et al.*

1974: R.R.Trotzman

1975: R.R.Trotzman.

COMPACT MODEL IN WEAK INVERSION

$$I_D = \frac{W}{L} I_{D0} e^{\frac{V_G}{nU_T}} \left[\frac{-V_S}{e^{U_T}} - e^{\frac{-V_D}{U_T}} \right]$$

$\underbrace{\phantom{I_{D0} e^{\frac{V_G}{nU_T}}}}$
 $-V_{T0}$

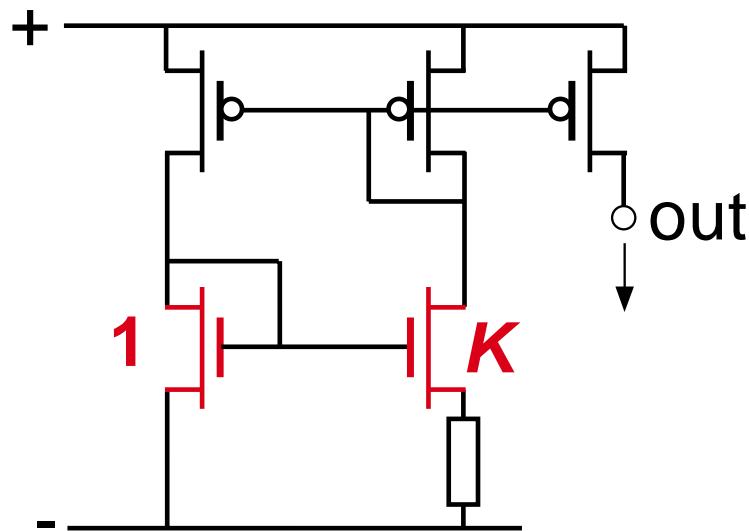
$$I_S e^{\frac{-V_T}{nU_T}} \quad (\text{later in EKV model})$$

- Reference to substrate.
- Source-drain symmetry.
- Slope factor n .
- Similar to Ebers-Moll model of bipolar transistor.

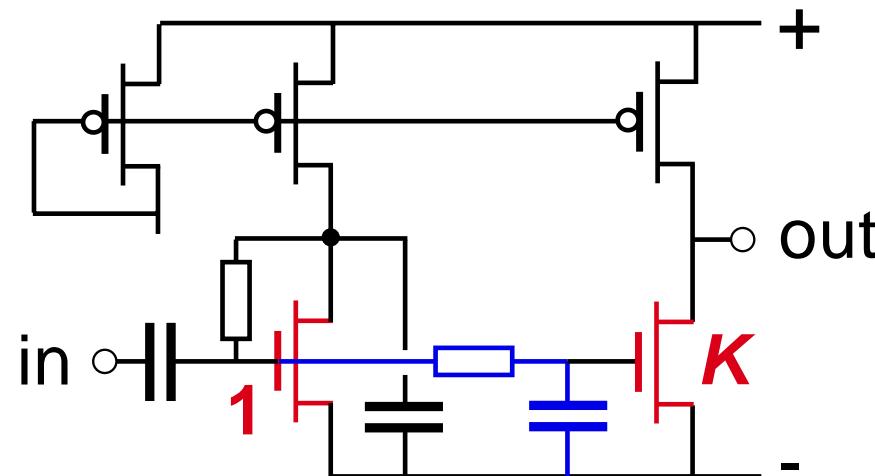
ANALOG CIRCUITS BASED ON WEAK INVERSION

E. Vittoz and J. Fellrath, **ESSCIRC 1976**

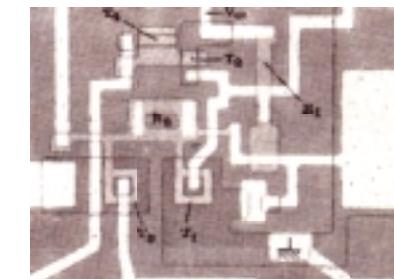
- Current reference:



- Amplitude detector

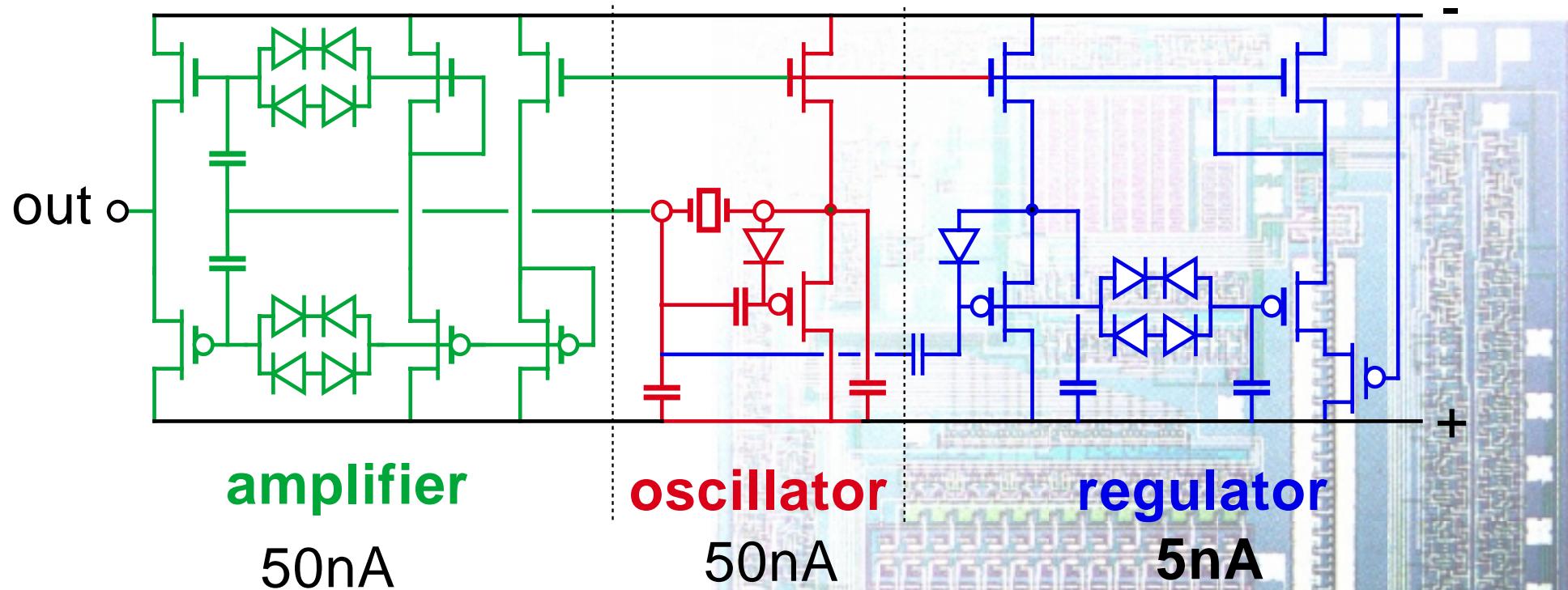


- Crystal oscillator:



- Weak inversion is **not** a "leakage current"!

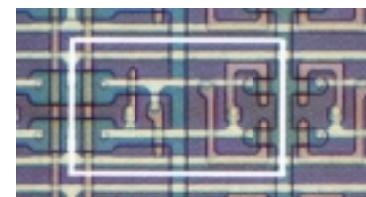
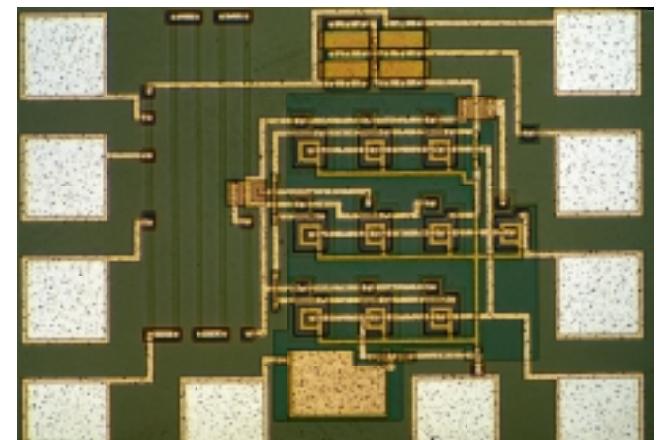
VERY LOW-POWER CRYSTAL OSCILLATOR (1977)



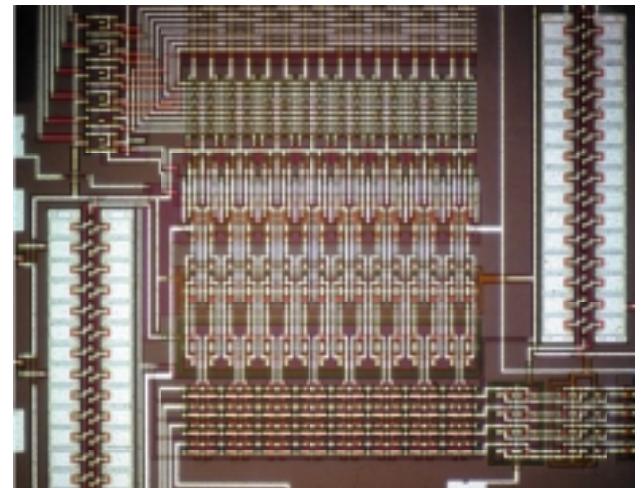
- At 32 KHz: $0.1\mu\text{A}$ from 0.8 to 3 volts
- Use of lateral diodes in polysilicon
(M. Dutoit and F. Sollberger, 1978).

FURTHER DEVELOPMENTS (1975-1982)

- Band gap voltage references
 - S-well-bulk bipolars (ESSCIRC'78)
 - bipol. operated MOS (ESSCIRC'82). 
- Watch microprocessors
(C. Piguet *et al.*).
- Nonvolatile memories for digital tuning
 - read/write from 1.5 volt
(Gerber *et al.*, 1981).
- Extension of MOS model beyond w.i.
(H. Oguey and S. Csereny, 1982).
- Extension to other applications.



RAM cell



WHERE DO THESE EARLY DEVELOPMENTS LEAD TODAY?

- **Watch** building blocks (oscillator, dividers, digital tuning...).
- Compact **model** of MOS transistor $\Rightarrow \Rightarrow \Rightarrow$ EKV model.
- Special compatible **devices** (bipolar, poly-diodes).
- Single-clock sequential **blocks**.
- Low-power, low-voltage circuit **techniques**.
- Micro-processor **architectures** for very low-power.
- Exploitation of **weak inversion** (or sub-threshold).
 - for low-voltage analog
 - for ultimate low-power digital
 - $f_{max} > 100\text{MHz}$ at ultimate low-voltage (100-300 mV)
 - voltage level of brain neurons!

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