# AMD A77E Fusion Controller Hub Databook

| Publication No. | Revision | Date |
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*Advanced Micro Devices*

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# Revision History

| Date | Revision | Change Description |
|---|---|---|
| February 2014 | 3.01 | Modified description in the Power and Ground Pin Descriptions table for VDDBT_RTC_G. |
| October 2013 | 3.00 | Initial Release |

# Chapter 1 Introduction

The A77E FCH, code-named “Bolton-E4” is the third generation fusion controller hub (FCH) from AMD designed to deliver the quality and performance needed for ultimate high end computing, multitasking, and multimedia functionality on performance embedded platforms. The A77E FCH is referred to by it's code name throughout this document.

Supporting AMD accelerated processing units (APUs), Bolton-E4 replaces the traditional two-chip approach with a new, single-chip architecture, reducing power consumption and improving system performance while reducing the overall chipset footprint. Bolton-E4 provides sixSATA 6Gb/s ports and four USB 3.0 ports for expanded I/O connectivity.

# 1.1 Features of Bolton-E4

**Processors Supported**

- Supports AMD Accelerated Processor Units (APUs)

**Unified Media Interface (UMI)**

- 1-, 2-, or 4-lane UMI connecting the FCH with the APU
- Automatic detection of lane configuration on boot-up
- Dynamic lane width up/down configuration on detecting bandwidth requirement
- Supports transfer rate of 2.5 GT/s (2GB/s) or 5 GT/s (5GB/s) per lane
- Clock speed can be locked at 2.5 GHz for power saving

**PCI Express® 2.0 Controller**

- Four-lane PCI Express (PCIe®) 2.0 interface, supporting up to four general purpose (GPP) devices. Supported configurations include:

  1x4

  2x2

  1x2 + 2x1

  4x1
- Supports L0s and L1 link power states for power saving

**USB 3.0/2.0/1.1 Host Controllers**

- 2 xHCI (v.1.0), 3 OHCI, and 2 EHCI host controllers to support:

  4 USB 3.0 ports

  10 USB 2.0 ports

  2 dedicated USB 1.1 ports (for internal devices only)
- Supports xHCI 1.0 features + debug port
- Supports OHCI legacy keyboard/mouse
- Supports wake function in S3 and S4
- Supports USB debug port for EHCI controllers
- Supports port disable with individual control

**SMBus Controller**

- Two SMBus controllers – one is multiplexed on three (3) pairs of SMBus signals while the other controller is dedicated for ASF or a Synaptics InterTouch Touchpad device
- Supports SMBALERT # signal

**Interrupt Controller**

- Supports IOAPIC/X-IO APIC mode for 24 channels of interrupts
- Supports 8259 legacy mode for 15 interrupts
- Supports programmable level/edge triggering on each channels
- Supports serial interrupt on quiet and continuous mode

**DMA Controller**

- Two cascaded 8237 DMA controllers
- Supports LPC DMA

**LPC Host Bus Controller**

- Supports LPC-based super I/O and flash devices
- Three programmable memory windows
- Supports two master/DMA devices
- Supports TPM version 1.1/1.2 devices for enhanced security
- Supports SPI devices at speed up to 66MHz
- Supports a maximum SPI ROM size of 16MB
- Supports single, dual, and quad data SPI

### SATA Controller

- Supports six third-generation SATA ports with transfer rates up to 6 Gbit/s
- Supports SATA first-generation (up to 1.5 Gbit/s) and second-generation (up to 3.0 Gbit/s)-compliant devices
- Complies with SATA 3.0 specification
- Supports three modes of operation:

  IDE emulation mode

  AHCI 1.3 mode
- Any of the ports can be configured to a lower transfer rate of 3.0 or 1.5 Gbit/s for power saving
- Any of the SATA ports can be configured to support second generation e-SATA port (compatible with devices running at 3 Gbit/s and 1.5 Gbit/s)
- AHCI Mode supporting the following features:

  DIPM (Device Initiated Power Management)

  HIPM (Host Initiated Power Management)

  Hot Plug detection and notification

  NCQ (Native Command Queue) mode

  FIS Based Switching Mode

### High Definition Audio

- Four independent output streams (DMA)
- Four independent input streams (DMA)
- Multiple channels of audio output per stream
- Supports up to 4 codecs
- Up to 192kHz sample rate and 32-bit audio
- 64-bit addressing capability for DMA bus master and MSI
- Unified Audio Architecture (UAA) compatible
- HD Audio registers can be located anywhere in the 64-bit address space
- Supports 3.3V/1.5V dual-voltage interface for power saving

### Timers

- 8254-compatible timer
- Microsoft® High Precision Event Timer (HPET)
- ACPI power management timer
- Watchdog timer
- AMD boot timer

### Real Time Clock (RTC)

- 272-byte battery-backed CMOS RAM
- Hardware-supported century rollover
- Hardware-supported day-light saving feature
- RTC battery monitoring feature

### Power Management

- ACPI specification 3.0 compliant power management schemes
- Supports processor C states
- Supports system S0, S3, S4, and S5 states
- Supports the S5 Plus power saving mode.
- Wakeup events for S3, S4, and S5 generated by:

  Any GEVENT pins that are on the S5 domain

  Any GPM pins that are on the S5 domain

  USB (Note: Remote wake from S5 for USB is not supported by the operating systems' USB driver stacks)

  HD modem

  Power Button

  Internal RTC wakeup

  SMI Event

### Consumer IR

- SMM support: generating SMI by power management events, bus transaction (IO, memory, or PCI configuration cycle) trapping, internal controllers, GPIO, timer, management message

- CLKRUN# support for PCI power management
- Low idle power
- Supports STPCLK# control
- ALPM (HIPM) on SATA
- DIPM on SATA

**Integrated Micro-Controller (IMC)**

- 8051 microcontroller:

  4 Kbytes of data memory

  64 Kbytes base instruction plus expanded instruction (beyond 64 KB) support

  Thirteen interrupts, 50 interrupt sources, 4 interrupt priority levels
- 33 MHz operation in S0 state, 16 MHz operation in system sleep state; option to stop clock when idle
- JTAG-based In-Circuit Emulator (ICE) or debugger
- Host I/O interface
- Four general purpose timers/counters
- Hibernation, Watchdog, and RTC timers
- Access to all FCH MMIO resources (e.g. PMIO, RTC, BIOS_RAM registers)

**Consumer IR**

- Media center infrared with wake from all states
- Two transmitters
- IR receiver and wideband learning receiver
- Fully compatible with Microsoft Windows® Vista® and Windows 7 Media Center

**Hardware Monitoring**

- Fan control: IMC-based APU fan control via SB-TSI

**Integrated Clock Generator**

- Provides 25 MHz, 14.3 MHz (frequency is 14.318 MHz on average; cycle-to-cycle variation can be between 14.2857 and 14.8148 MHz), and 48 MHz clocks
- Provides clocks for APU, external graphics, UMI, and nine general purpose PCIe devices

**VGA Translator**

- Provides VGA translation function. Supports a maximum resolution of 1920x1600 at a refresh rate of 60 Hz.
- Auto monitor detection
- Automatic power down for VGA DAC when there is no monitor attached
- Driver can put the VGA DAC into low power mode when a VGA monitor is attached but inactive.

**SD Flash Controller**

- Clock speed up to 50 MHz (high-speed mode)
- Supports both standard (SD) and high-capacity (SDHC) formats
- Supports 1 and 4-bit modes
- For the SDHC format:

  Supports capacity range of 4 to 32 GB, 4 pins @ 50 MHz. **Note:** With Windows 7 (32 or 64 bit) and MS Hotfix KB976422, up to 2 TB is supported.

  Supports speed classes of up to Class 10
- For the SD format:

  Supports capacities of up to 2 GB

**Miscellaneous**

- Access to ACPI features through:

  SMBus

  ASFBus

  GPIO

## 1.2 Branding and Part Numbers


**Figure 1. Bolton-E4 Branding and Part Number**

Notes on branding diagram:

- Branding can be in laser, ink, or mixed laser-and-ink-marking.
- AMD logo image may be in hollow/outline form.
- For the ASIC Name, FCH is used for production parts, while the engineering codename is used for engineering samples.
- For the Date Code, ENG designates engineering sample (it does not appear for production parts).

Figure legends:

ASIC NAME = See table below.
DATE CODE = YYWW (YY = assembly start year, WW = assembly start week)
COO = Country of origin (assembly site)
XXXXXX.XX = Wafer foundry lot number.wafer ID (wafer ID may not appear sometimes)
ZZZ-ZZZZZZZ = AMD part number (see table below)

**Table 1. Bolton-E4 Part Numbers**

| ASIC Name | ASIC Revision | Date Code | AMD Part Number |
|---|---|---|---|
| Bolton-E4 Parts | | | |
| FCH | A1 | YYWW | 218-0844020-00 |

# 1.3 Bolton-E4 Block Diagrams

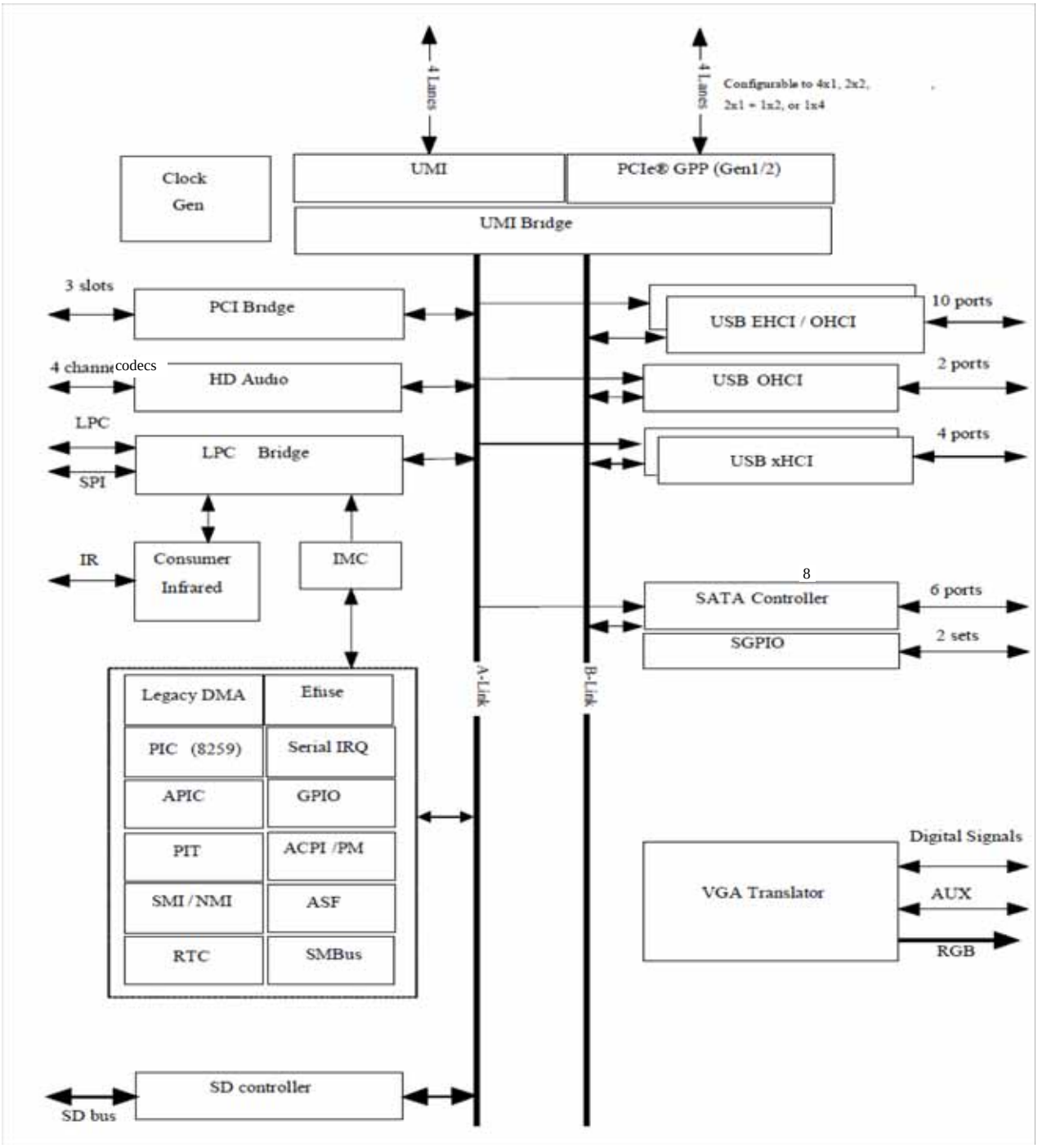



**Figure 2. Bolton-E4 Block Diagram**

# 1.4 Conventions and Notations

The following conventions are used throughout this manual.

## 1.4.1 Pin Names

Pins are identified by their pin names or ball references. All active-low signals are identified by the suffix '#' in their names (e.g., GNT0#).

## 1.4.2 Pin Types

The pins are assigned different codes according to their operational characteristics. These codes are listed below.

**Table 2. Pin Type Codes**

| Code | Pin Type |
|---|---|
| I | Digital Input |
| O | Digital Output |
| OD | Open Drain |
| I/O | Bi-Directional Digital Input or Output |
| I/OD | Digital Input or Open Drain |
| M | Multifunctional |
| PWR | Power |
| GND | Ground |
| A-O | Analog Output |
| A-I | Analog Input |
| A-I/O | Analog Bi-Directional Input/Output |
| A-PWR | Analog Power |
| A-GND | Analog Ground |
| Other | Pin types not included in any of the categories above |

## 1.4.3 Numeric Representation

Hexadecimal numbers are appended with "h" whenever there is a risk of ambiguity. Other numbers are in decimal.

Pins of identical functions but different running integers (e.g., "LAD3," "LAD2," "LAD3") are referred to collectively by specifying their integers in square brackets and with colons (i.e., "LAD[3:0]"). A similar short-hand notation is used to indicate bit occupation in a register. For example, Command[15:10] refers to the bit positions 10 through 15 of the Command register.

### 1.4.4 Register Field

A field of a register is referred to by the format of [Register Name].[Register Field]. For example, “Commad.Memory Space” is the “Memory Space” field of the register “Command.”

### 1.4.5 Acronyms and Abbreviations

The following is a list of the acronyms and abbreviations used in this manual.

**Table 3. Acronyms and Abbreviations**

| Acronym | Full Expression |
|---|---|
| ACPI | Advanced Configuration and Power Interface |
| AHCI | Advanced Host Controller Interface |
| AOAC | Always On Always Connected |
| APU | Accelerated Processor Unit |
| BGA | Ball Grid Array |
| BIOS | Basic Input Output System. Initialization code stored in a ROM or Flash RAM used to start up a system or expansion card. |
| DAC | Digital to Analog Converter |
| DIPM | Device Initiated Interface Power Management |
| DMA | Direct Memory Access |
| EHCI | Enhanced Host Controller Interface |
| EPROM | Erasable Programmable Read Only Memory |
| FCH | Fusion Controller Hub |
| GND | Ground |
| GPIO | General Purpose Input/Output |
| GPM | General Power Management |
| HD | High Definition Audio |
| HIPM | Host Initiated Interface Power Management |
| HPET | High Precision Event Timer |
| $I^2C$ | Inter-Integrated Circuit |
| IDE | Integrated Drive Electronics |
| IMC | Integrated Micro-Controller |
| IR | Infrared |
| ISA | Industry Standard Architecture |
| JTAG | Joint Test Access Group. An IEEE standard. |
| LPC | Low Pin Count |

**Table 3. Acronyms and Abbreviations (Continued)**

| | |
|---|---|
| NC | No Connect |
| NCQ | Native Command Queuing |
| OHCI | Open Host Controller Interface |
| PCI | Peripheral Component Interface |
| PCIe® | PCI Express® |
| PLL | Phase Locked Loop |
| POST | Power On Self Test |
| PD | Pull-down Resistor |
| PU | Pull-up Resistor |
| RAID | Redundant Array of Inexpensive Disks |
| RTC | Real Time Clock |
| SATA | Serial ATA |
| SCI | System Controller Interrupt |
| SGPIO | Serial General Purpose Input/Output |
| SMBus | System Management Bus |
| SMI | System Management Interrupt |
| SPI | Serial Peripheral Interface |
| TBA | To Be Added (the information is not yet available) |
| TPM | Trusted Platform Module |
| UMI | Unified Media Interface |
| USB | Universal Serial Bus |
| xHCI | Extensible Host Controller Interface |

# Chapter 2 Functional Description

## 2.1 USB Controllers

Figure 3 is an internal block diagram for Bolton-E4's USB controllers showing the use of two xHCI, three OHCI and two EHCI controllers to control four USB 3.0, ten USB 2.0, and two dedicated USB 1.1 ports.

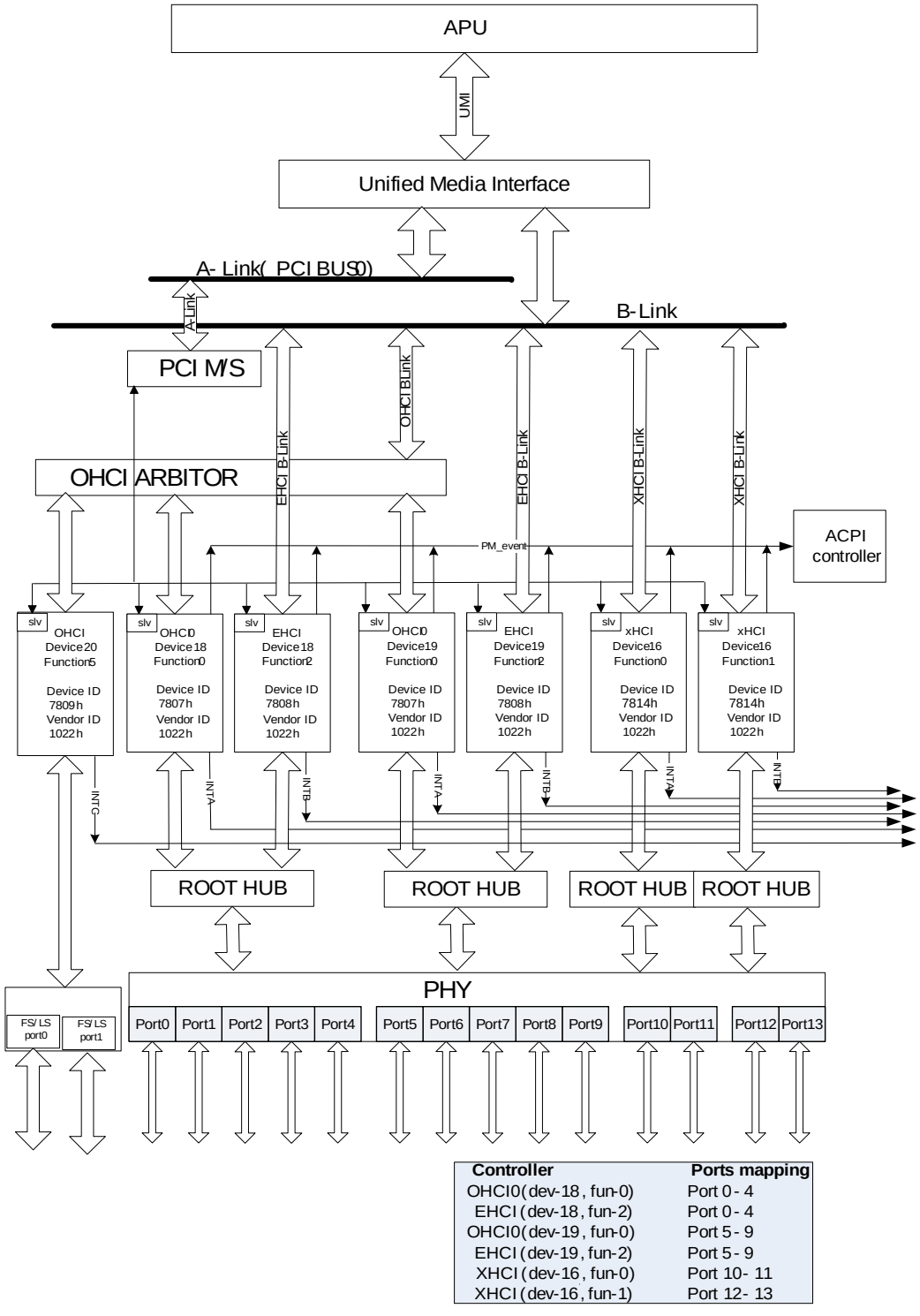



**Figure 3. USB Controller Block Diagram for Bolton-E4**

### 2.1.1 USB Power Management

An advanced power management capability interface compliant with *PCI Bus Power Management Interface Specification Revision 1.1* is incorporated into the EHCI and xHCI controllers. This interface allows the EHCI/xHCI to be placed in various power management states, offering a variety of power savings for a host system.

Table 4 highlights the EHCI/xHCI support for power management states and features supported for each of the power management states. An EHCI/xHCI implementation may internally gate-off USB clocks and suspend the USB transceivers (low power consumption mode) to provide these power savings.

**Table 4. EHCI/xHCI Support for Power Management States**

| PCI Power Management State | State Required / Optional in Specification | Comments |
|---|---|---|
| D0 | Required | Supported.<br>Fully awake backward compatible state. All logic in full power mode. |
| D1 | Optional | **Not supported.**<br>USB Sleep state with EHCI/xHCI bus master capabilities disabled. All USB ports in suspended state. All logic in low latency power savings mode because of low latency returning to D0 state. |
| D2 | Optional | **Not supported.**<br>USB Sleep state with EHCI/xHCI bus master capabilities disabled. All USB ports in suspended state. |
| D3hot | Required | **Supported.**<br>Deep USB Sleep state with EHCI/xHCI bus master capabilities disabled. All USB ports in suspended state. |
| D3cold | Required | **Supported.**<br>Fully asleep backward compatible state. All downstream devices are either suspended or disconnected based on the implementation's capability to supply downstream port power within the power budget. |

The functional and wake-up characteristics for the EHCI/xHCI power states are summarized below.

**Table 5. EHCI/xHCI Power State Summary**

| Power State | Functional Characteristics | Wake-up Characteristics* |
|---|---|---|
| D0 | • Fully functional EHCI/xHCI device state<br>• Unmasked interrupts are fully functional | • Resume detected on suspended port<br>• Connect or Disconnect detected on port<br>• Over Current detected on port |
| D1 | • EHCI/xHCI preserves PCI configuration<br>• EHCI/xHCI preserves USB configuration<br>• Hardware masks functional interrupts<br>• All ports are disabled or suspended | • Resume detected on suspended port<br>• Connect or Disconnect detected on port<br>• Over Current detected on port |
| D2 | • EHCI/xHCI preserves PCI configuration<br>• EHCI/xHCI preserves USB configuration<br>• Hardware masks functional interrupts<br>• All ports are disabled or suspended | • Resume detected on suspended port<br>• Connect or Disconnect detected on port<br>• Over Current detected on port |
| D3hot | • EHCI/xHCI preserves PCI configuration<br>• EHCI/xHCI preserves USB configuration<br>• Hardware masks functional interrupts<br>• All ports are disabled or suspended | • Resume detected on suspended port<br>• Connect or Disconnect detected on port<br>• Over Current detected on port |
| D3cold | • PME Context in PCI Configuration space is preserved<br>• Wake Context in EHCI/xHCI MemorySpace is preserved<br>• All ports are disabled or suspended | • Resume detected on suspended port<br>• Connect or Disconnect detected on port<br>• Over Current detected on port |
| ***Note:*** *******Associated enables must be set.* | | |

# 2.2 LPC ISA Bridge

## 2.2.1 LPC Interface Overview

The Low Pin Count (LPC) bus interface is a cost-efficient, low-speed interface designed to support low bandwidth and legacy devices. The LPC interface essentially eliminates the need of ISA and X-bus in the system. A typical setup of the system with LPC interface is shown in Figure 4. The LPC host controller contains both LPC and Serial Peripheral Interface (SPI) bridge functions. It connects to the internal A-Link bus on one side and the LPC and SPI buses on the other side.

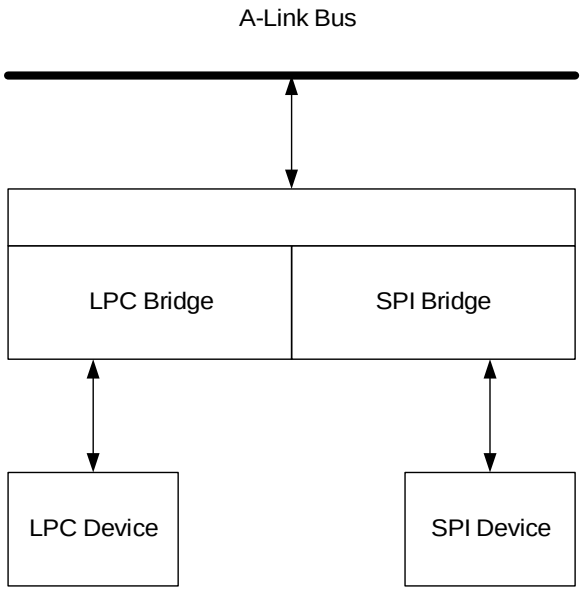



**Figure 4. A Typical LPC Bus System**

Examples of LPC devices include Super I/O, BIOS RAM, audio, Trusted Platform Module (TPM), and system management controller. A BIOS ROM can also be populated on the SPI interface. The FCH can support an LPC or SPI type BIOS ROM. The ROM selection is determined by a strap pin (refer to Table 32 on page 81) during RSMRST# assertion. In addition to the straps, software can change the ROM selection through programming in the PMIO registers.

The host controller supports memory and I/O read/write, Direct Memory Access (DMA) read/write, bus master memory I/O read/write, and TPM read/write. It supports up to two bus masters and seven DMA channels. A bus master or DMA agent uses the LDRQ pin to assert bus master or DMA requests. The host controller uses LFRAME# to indicate the start or termination of a cycle. Table 6 on page 30 shows a list of cycles supported by the host controller, their initiators, data flow directions, and their PCI counterparts.

**Table 6. LPC Cycle List and Data Direction**

| Cycle | Size (bytes) | Initiator | Data Direction | PCI Counterpart |
|---|---|---|---|---|
| Memory read | 1 | Host | P-2-Host | MemRead to LPC range |
| Memory write | 1 | Host | Host-2-P | MemWrit to LPC range |
| I/O read | 1 | Host | P-2-Host | IORead to LPC range |
| I/O write | 1 | Host | Host-2-P | IOWrit to LPC range |
| DMA read | 1, 2, 4 | Peripheral | Host-2-P | DMA control setup; DMA data fetch |
| DMA write | 1, 2, 4 | Peripheral | P-2-Host | DMA control setup; DMA data store |
| BM Memory read | 1, 2, 4 | Peripheral | Host-2-P | DMA control setup; DMA data fetch |
| BM Memory write | 1, 2, 4 | Peripheral | P-2-Host | DMA control setup; DMA data store |
| BM I/O read | 1, 2, 4 | Peripheral | Host-2-P | DMA control setup; I/O data fetch |
| BM I/O write | 1, 2, 4 | Peripheral | P-2-Host | DMA control setup; I/O data store |
| TPM read | 1,2,4 | Host | P-2-Host | TPM read |
| TPM write | 1,2,4 | Host | Host-2-P | TPM write |

The host controller has a SERIRQ (Serial IRQ) pin, which is used by peripherals that require interrupt support. All legacy interrupts are serialized on this pin, decoded by the host controller, and sent to the interrupt controller for processing. Refer to the *Serial IRQ Specification, Version 5.4*, for a detailed description of the Serial IRQ protocol.

# 2.3 Real Time Clock

The Real Time Clock (RTC) updates the computer's time and generates interrupts for periodic events and pre-set alarm. The RTC also makes hardware leap year corrections. The FCH's RTC includes a 272-byte (256 standard bytes plus 16 additional bytes) CMOS RAM, which is used to store the configuration of a computer such as the number and type of disk drive, graphics adapter, base memory, checksum value, etc.

## 2.3.1 Functional Blocks of RTC

The internal RTC is made of two parts—one part is an analog circuit, powered by a battery (VBAT), and the other is a digital circuit, powered by the main power (VDD). Figure 5 shows the block diagram of the internal RTC. The FCH has a hardware-based daylight saving feature, which makes clock adjustments (spring forward or fall back) at the designated dates/times. Both the date and hour for the daylight and standard time are fully programmable, allowing for different daylight saving dates and hours for different parts of the world.

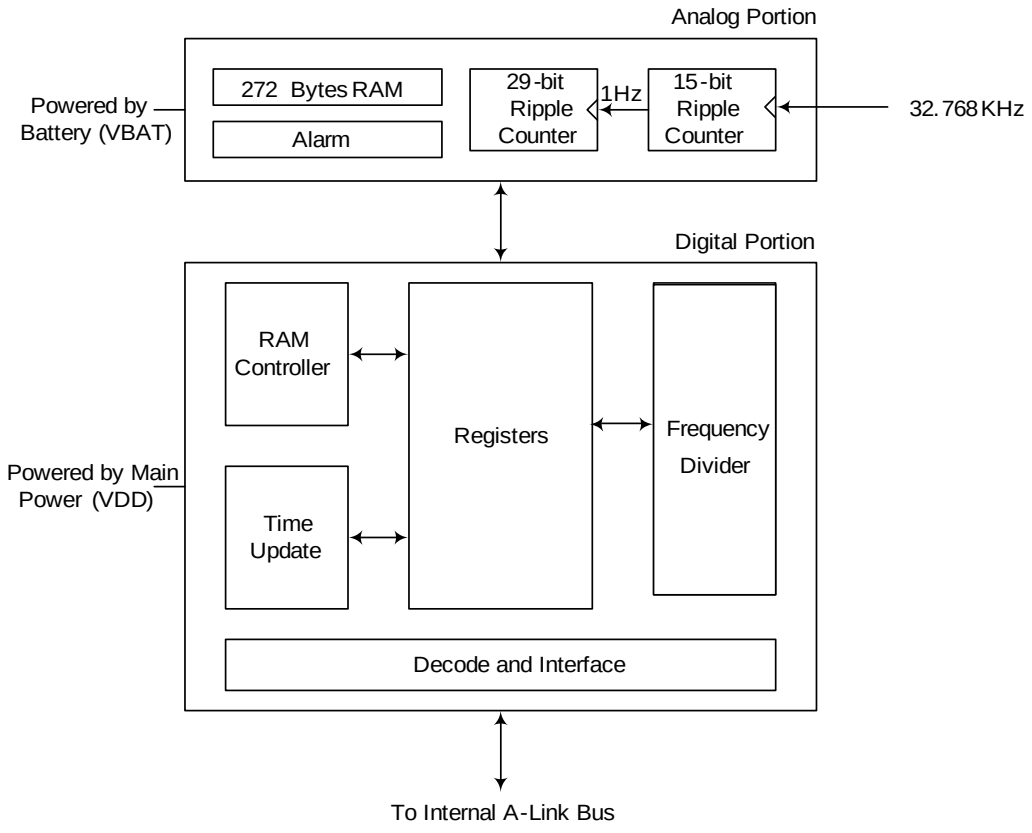



**Figure 5. Block Diagram of Internal RTC**

# 2.4 Serial ATA Controller

The integrated Serial ATA controller processes host commands and transfers data between the host and Serial ATA devices. It supports six independent Serial ATA channels. Each channel has its own Serial ATA bus and supports one Serial ATA device. The SATA controller supports Serial ATA first, second, and third generation transfer rates (up to 1.5 Gbit/s, 3.0 Gbit/s, and 6.0 Gbit/s respectively).

Figure 6 on page 33, and Figure 7 on page 35, are  diagrams for the SATA block. The SATA controller can operate in three modes:

- All six channels configured to SATA AHCI mode.
- All six channels configured to IDE mode. In this configuration, the SATA controller is configured into two IDE controllers, with the programming interface of channel 0 to 3 under the first IDE controller, and that of channel 4 to 5/7 under the second IDE controller.
- Four channels (channel 0 to 3) configured as SATA AHCI and four channels (channel 4 to 5/7) configured as IDE mode. In this configuration, the programming interface of channel 4 to 5/7 is under the IDE controller.

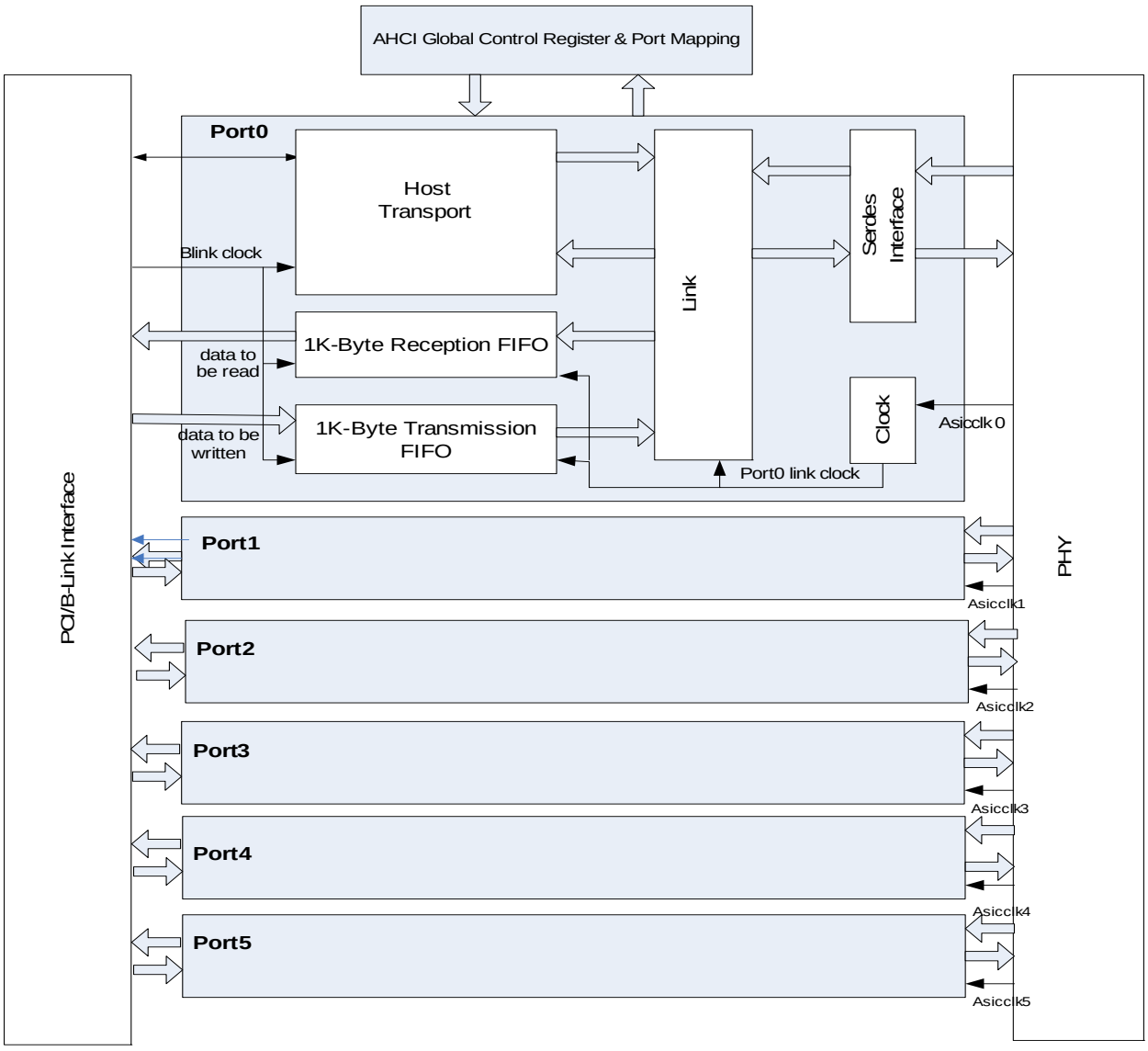



**Figure 6. Block Diagram of the SATA Module of Bolton-E4**

## 2.5 PCI Bridge

The PCI Bridge supports up to three PCI slots. The PCI bridge runs at 33 MHz and can support the CLKRUN# function with individual clock override (option for not stopping specific PCICLK). In addition, it has the capability to hide individual PCI devices.

# 2.6 High Definition Audio

The High Definition (HD) audio controller communicates with external HD audio codec(s) over the HD audio link. The HD audio controller consists of four independent output DMA engines and four independent input DMA engines that are used to move data between system memory and the external codec(s). The controller can support up to four audio or modem codecs in any combinations.

## 2.6.1 HD Audio Codec Connections

Figure 7 shows the HD Audio interface connections to the HD Audio codecs. The FCH can support up to four HD Audio codecs. Each codec has its own AZ_SDIN (data input) for the HD Audio interface. Figure 7 shows the connection for a two-codec configuration.

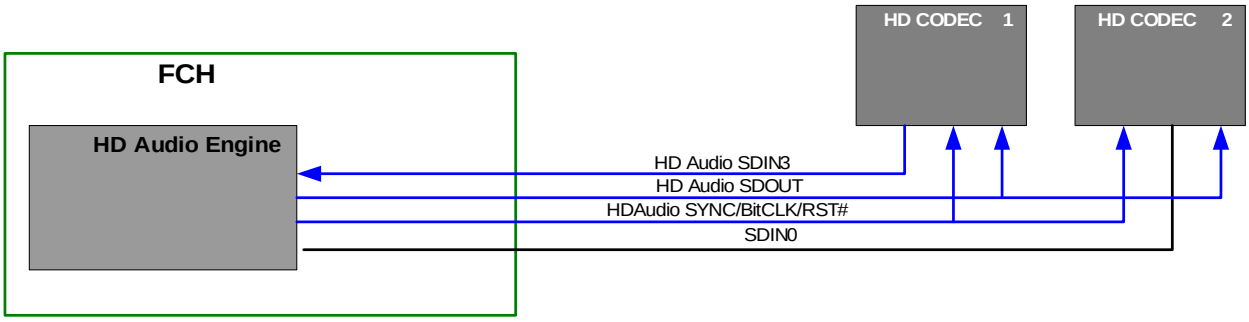



**Figure 7. HD Audio Codec Connections**

# 2.7 Clock Generation

Bolton-E4 has two clock configurations: (1) external clock mode, and (2) integrated clock mode. These are shown in Figure 8 and Figure 9 on page 37, respectively.

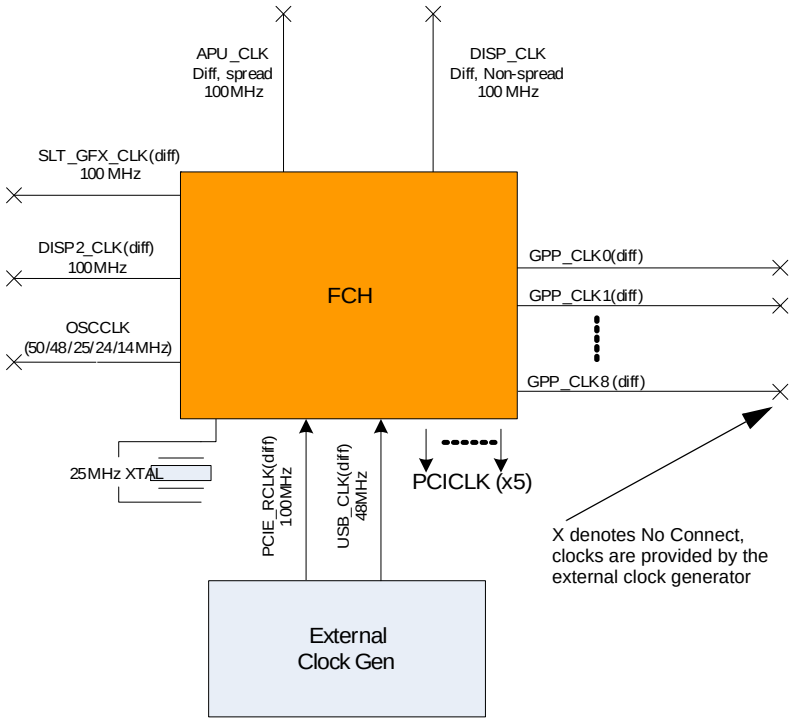



**Figure 8. Bolton-E4 Clock Signals for External Clock Mode**

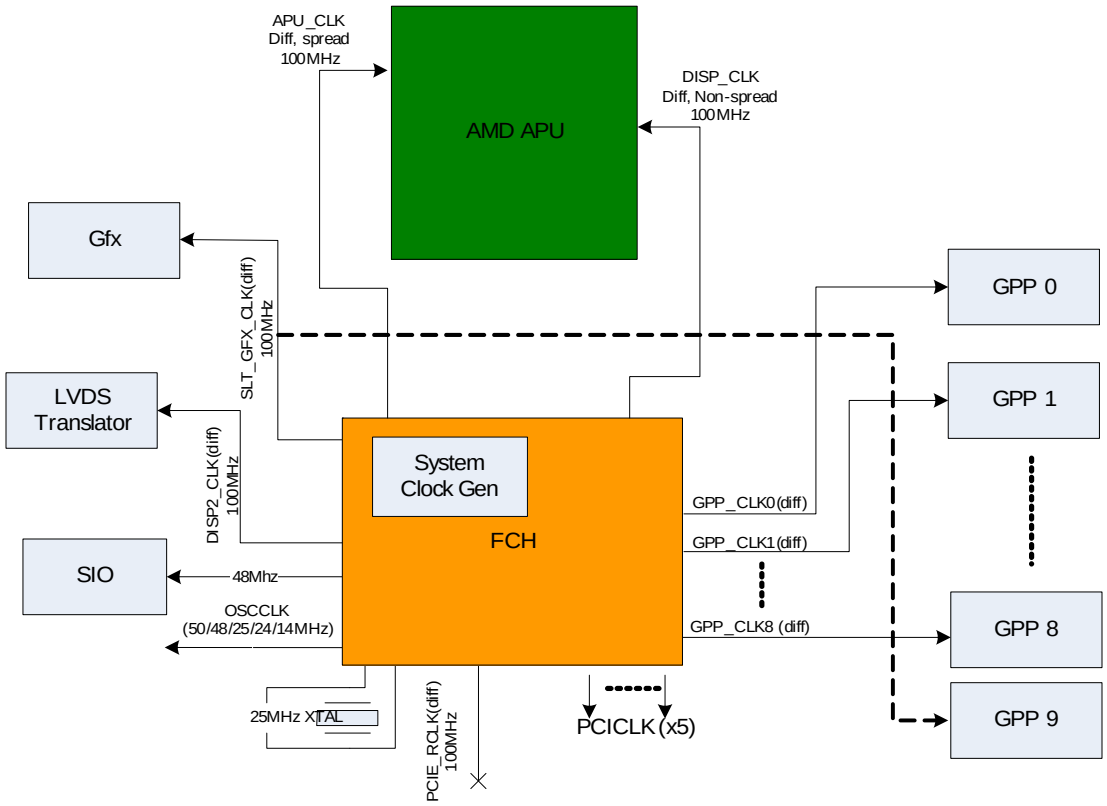



**Figure 9. Bolton-E4 Clock Signals for Internal Clock Mode**

The clock mode is selected by a strap pin. If the FCH is in external clock mode, the clock sources required include a 14.318 MHz source for the timers, a 25MHz clock source for the VGA translator**,** a 32-KHz crystal for the RTC**,** a 100 MHz differential clock pair for the PCIe reference clocks, a 48-MHz clock source for USB, and a 25 MHz single ended or 100 MHz differential pair clock for SATA. In addition to the PCIe® clocks, the FCH also uses the 100 MHz clock to generate various internal clocks, including the PCI 33-MHz clocks.

If integrated clock mode is selected, only a 25 MHz crystal for master reference and a 32 KHz crystal for the RTC are required. The FCH will then generate all of the system clocks needed, including the APU clocks, the external graphics clock, the 25 MHz clock for SATA, and the 48 MHz clocks for USB, and so on.

# 2.8 SMI/SCI Generation

There are a total of 160 sources of events. The first 64 can be mapped to the 32 standard ACPI EVENT bits, which can be used to generate SCI or PME. All of the 160 events can be configured to generate SMI/NMI.

When an event is routed to SMI, an SMI assertion message will be sent by the FCH to the APU. The SMI status remains active until the EOS bit is set and the status bit is cleared. When the EOS is set, an SMI de-assertion message will be sent to the APU. If the event is routed to SCI, BIOS can then route it to any of the legacy interrupts (except IRQ8) or INT21 in the case of IOAPIC.

## 2.8.1 Event Sources for SCI

Table 7 below shows the 160 sources of SCI events, the first 64 of which can be mapped to the 32 event resources of the ACPI EventStatus. The SCI event mapping are controlled through the SciMap* registers in SMI_Reg space. And the SCI Event enable/status is accessed through the EventEnable/ EventStatus registers in SMI_reg space. Refer to the *AMD Bolton Fusion Controller Hub Register Reference Guide* for more details.

**Table 7. SCI Event Sources and Mapping onto ACPI EventStatus**

| Event Number | Event Source |
|---|---|
| 0 ~ 23 | Gevent0 ~ 23 (GEVENT pins) |
| 24 | PME from USB device 18 |
| 25 | PME from USB device 19 |
| 26 | PME from USB device 20 |
| 27 | PME from USB device 22 |
| 28 | PME from GPP device 21, function 0 |
| 29 | PME from GPP device 21, function 1 |
| 30 | PME from GPP device 21, function 2 |
| 31 | PME from GPP device 21, function 3 |
| 32 | Hot plug event from GPP device 21, function 0 |
| 33 | Hot plug event from GPP device 21, function 1 |
| 34 | Hot plug event from GPP device 21, function 2 |
| 35 | Hot plug event from GPP device 21, function 3 |
| 36 | PME from HD Audio device |
| 37 | SATA Gevent 0 |
| 38 | SATA Gevent 1 |
| 39 | PME from Gec |
| 40 | IMC Gevent |

**Table 7. SCI Event Sources and Mapping onto ACPI EventStatus (Continued)**

| | |
|---|---|
| 41 | Reserved |
| 42 | PME from CIR |
| 43 | WAKE# pin |
| 44 | FanThermal Gevent |
| 45 | ASF Master Interrupt event |
| 46 | ASF Slave interrupt event |
| 47 | SMBUS0 interrupt |
| 48 | TWARN event |
| 49 | Traffic Monitor Gevent |
| 50 | iLLB_event50 |
| 51 | PwrButton_event |
| 52 | ProcHot_event |
| 53 | NBHwAssertionMsg |
| 54 | NBSciAssertionMsg |
| 55 | RAS_event |
| 56 | XHC0PME |
| 57 | XHC1PME |
| 57: 63 | Reserved |
| 64 | Reserved |
| 65 | Slp_En_Write |
| 66 | GecRomSmi |
| 67 | SATA_AHCI_Smi |
| 68 | NbGppPme |
| 69 | NbGppHotPlug |
| 70 | RtcIrqEvent |
| 71 | ACPI_Timer_Event |
| 72 | GBL_RLS |
| 73 | BIOS_RLS |
| 74 | PWRBTN |
| 75 | SmiCmdPort |
| 76 | UsiSmi (OHCI legacy support) |
| 77 | SerIrqSmi |
| 78 | SMBus0Intr |

**Table 7. SCI Event Sources and Mapping onto ACPI EventStatus (Continued)**

| | |
|---|---|
| 79 | EcSmi |
| 80 | xHCErr |
| 81 | IntruderAlert |
| 82 | VBATLow |
| 83 | ProcHot |
| 84 | PCI_Serr |
| 85 | SB_Gpp0Serr |
| 86 | SB_Gpp1Serr |
| 87 | SB_Gpp2Serr |
| 88 | SB_Gpp3Serr |
| 89 | ThermalTrip |
| 90 | Emulate64_event90 |
| 91 | Usb_FLR_event91 |
| 92 | Sata_FLR_event92 |
| 93 | Az_FLR_event93 |
| 94 | Gec_FLR_event94 |
| 95 | CmosEraseSts_event95 |
| 96 | IRQ0Trapping_event96 |
| 97 | IRQ1Trapping_event97 |
| 98 | IRQ2Trapping_event98 |
| 99 | IRQ3Trapping_event99 |
| 100 | IRQ4Trapping_event100 |
| 101 | IRQ5Trapping_event101 |
| 102 | IRQ6Trapping_event102 |
| 103 | IRQ7Trapping_event103 |
| 104 | IRQ8Trapping_event104 |
| 105 | IRQ9Trapping_event105 |
| 106 | IRQ10Trapping_event106 |
| 107 | IRQ11Trapping_event107 |
| 108 | IRQ12Trapping_event108 |
| 109 | IRQ13Trapping_event109 |
| 110 | IRQ14Trapping_event110 |
| 111 | IRQ15Trapping_event111 |

**Table 7. SCI Event Sources and Mapping onto ACPI EventStatus (Continued)**

| | |
|---|---|
| 112 | IRQ16Trapping_event112 |
| 113 | IRQ17Trapping_event113 |
| 114 | IRQ18Trapping_event114 |
| 115 | IRQ19Trapping_event115 |
| 116 | IRQ20Trapping_event116 |
| 117 | IRQ21Trapping_event117 |
| 118 | IRQ22Trapping_event118 |
| 119 | IRQ23Trapping_event119 |
| 120 | VIn0Sts_event120 |
| 121 | VIn1Sts_event121 |
| 122 | VIn2Sts_event122 |
| 123 | VIn3Sts_event123 |
| 124 | VIn4Sts_event124 |
| 125 | VIn5Sts_event125 |
| 126 | VIn6Sts_event126 |
| 127 | VIn7Sts_event127 |
| 128 | Temp0Sts_event128 |
| 129 | Temp1Sts_event129 |
| 130 | Temp2Sts_event130 |
| 131 | Temp3Sts_event131 |
| 132 | Temp4Sts_event132 |
| 133 | FanIn0Sts_event133 |
| 134 | FanIn1Sts_event134 |
| 135 | FanIn2Sts_event135 |
| 136 | FanIn3Sts_event136 |
| 137 | FanIn4Sts_event137 |
| 138 | Fake0Sts_event138 |
| 139 | Fake1Sts_event139 |
| 140 | Fake2Sts_event140 |
| 141 | CStateMsg_event141 |
| 142 | ShortTimer_event142 |
| 143 | LongTimer_event143 |
| 144 | AbSmiTrap_event144 |

**Table 7. SCI Event Sources and Mapping onto ACPI EventStatus (Continued)**

| | |
|---|---|
| 145 | SoftReset_event145 |
| 146 | PStateChange_event146 |
| 147 | PStateChange_event147 |
| 148 | IoTrapping0_event148 |
| 149 | IoTrapping1_event149 |
| 150 | IoTrapping2_event150 |
| 151 | IoTrapping3_event151 |
| 152 | MemTrapping0_event152 |
| 153 | MemTrapping1_event153 |
| 154 | MemTrapping2_event154 |
| 155 | MemTrapping3_event155 |
| 156 | CfgTrapping0_event156 |
| 157 | CfgTrapping1_event157 |
| 158 | CfgTrapping2_event158 |
| 159 | CfgTrapping3_event159 |

### 2.8.2 SMI Events

Bolton-E4 supports up to 160 sources to generate SMI. The SMI control/status is accessed through the registers defined in the SMI_Reg space. Refer to the *AMD Bolton Fusion Controller Hub Register Reference Guide, order# 51192* for more details.

### 2.8.3 SMI/SCI Work Flow

Figure 10 on page 43, shows how the SMI/SCI logic works (SmiSciEn bit set to 1).

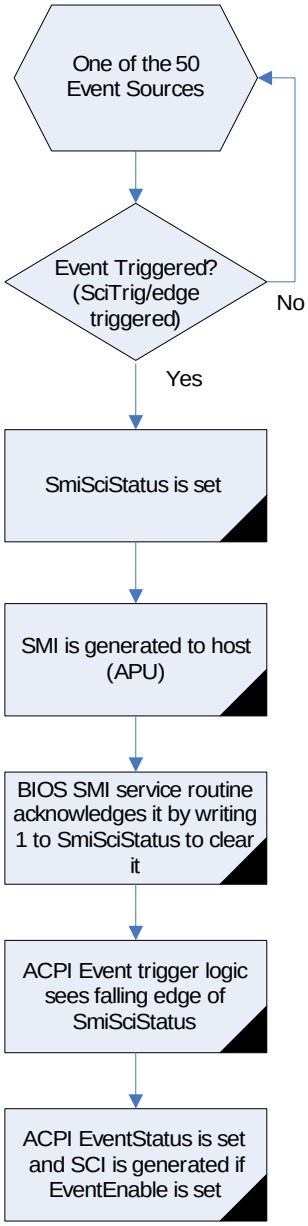
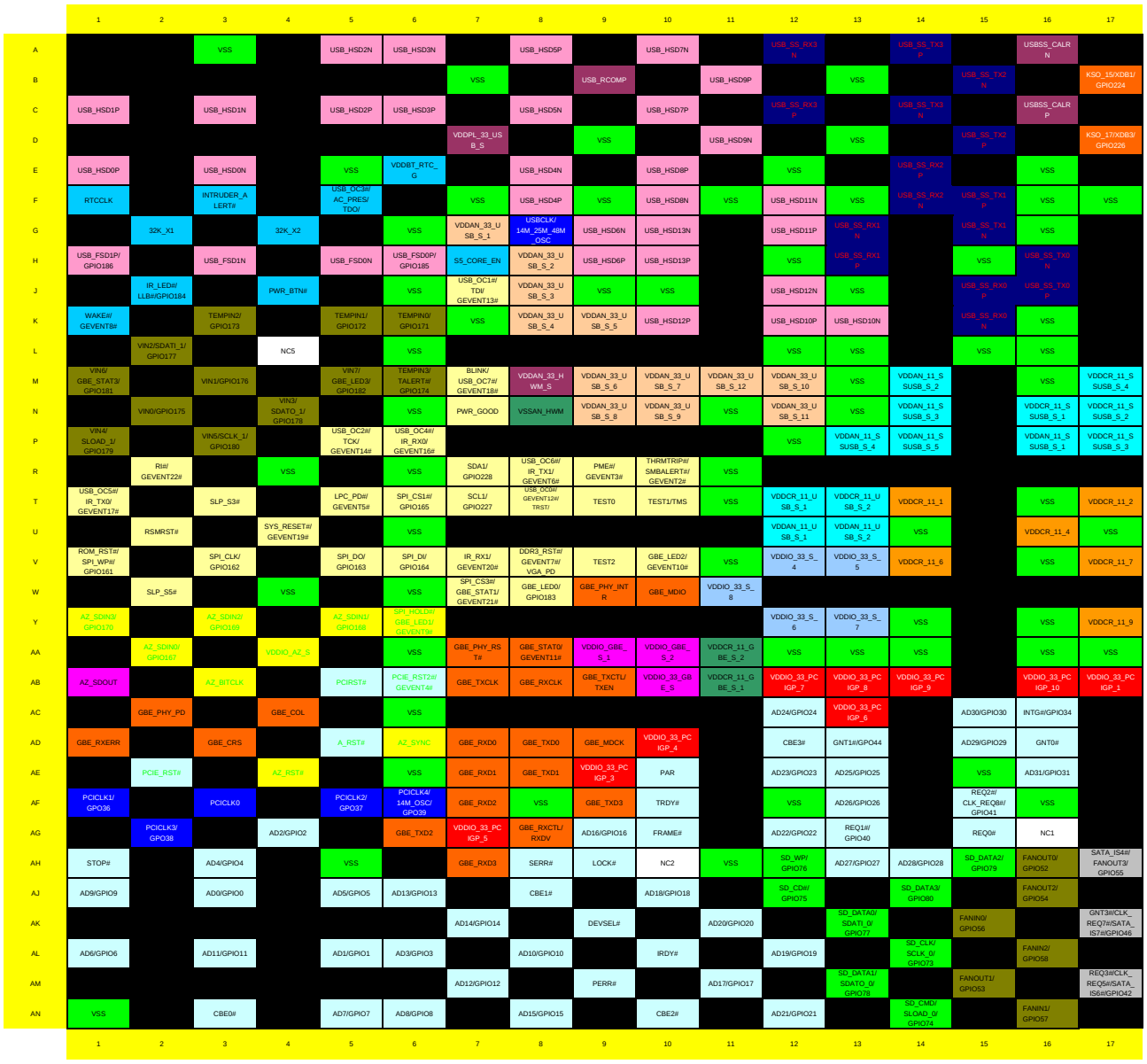



**Figure 10. SMI/SCI Logic of Bolton-E4**

# 2.9 Power Management/ACPI

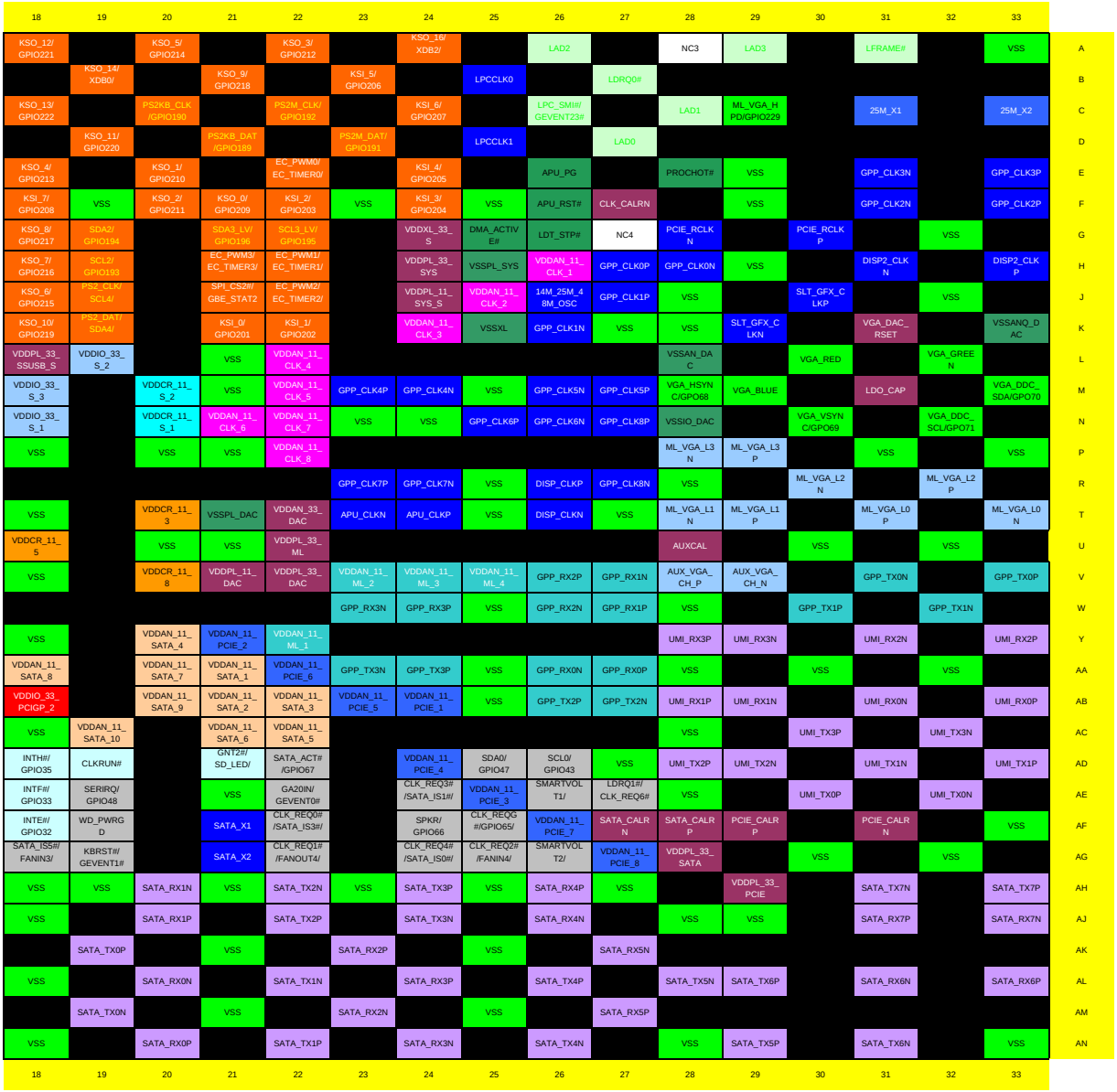
The Bolton-E4 power management/ACPI logic supports both hardware and message-based C1e, stutter mode, and S states.

# Chapter 3 Ballot Assignment



| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | | | VSS | | USB_HSD2N | USB_HSD3N | | USB_HSD5P | | USB_HSD7N | | USB_SS_RX3N | | USB_SS_TX3P | | USBSS_CALRN | |
| B | | | | | | | VSS | | USB_RCOMP | | USB_HSD9P | | VSS | | USB_SS_TX2N | | KSO_15/XDB1/GPIO224 |
| C | USB_HSD1P | | USB_HSD1N | | USB_HSD2P | USB_HSD3P | | USB_HSD5N | | USB_HSD7P | | USB_SS_RX3P | | USB_SS_TX3N | | USBSS_CALRP | |
| D | | | | | | | VDDPL_33_USB_S | | VSS | | USB_HSD9N | | VSS | | USB_SS_TX2P | | KSO_17/XDB3/GPIO226 |
| E | USB_HSD0P | | USB_HSD0N | | VSS | VDDBT_RTC_G | | USB_HSD4N | | USB_HSD8P | | VSS | | USB_SS_RX2P | | VSS | |
| F | RTCCLK | | INTRUDER_ALERT# | | USB_OC3#/AC_PRES/TDO/ | | VSS | USB_HSD4P | VSS | USB_HSD8N | VSS | USB_HSD11N | VSS | USB_SS_RX2N | USB_SS_TX1P | VSS | VSS |
| G | | 32K_X1 | | 32K_X2 | | VSS | VDDAN_33_USB_S_1 | USBCLK/14M_25M_48M_OSC | USB_HSD6N | USB_HSD13N | | USB_HSD11P | USB_SS_RX1N | | USB_SS_TX1N | VSS | |
| H | USB_FSD1P/GPIO186 | | USB_FSD1N | | USB_FSD0N | USB_FSD0P/GPIO185 | S5_CORE_EN | VDDAN_33_USB_S_2 | USB_HSD6P | USB_HSD13P | | VSS | USB_SS_RX1P | | VSS | USB_SS_TX0N | |
| J | | IR_LED#/LLB#/GPIO184 | | PWR_BTN# | | VSS | USB_OC1#/TDI/GEVENT13# | VDDAN_33_USB_S_3 | VSS | VSS | | USB_HSD12N | VSS | | USB_SS_RX0P | USB_SS_TX0P | |
| K | WAKE#/GEVENT8# | | TEMPIN2/GPIO173 | | TEMPIN1/GPIO172 | TEMPIN0/GPIO171 | VSS | VDDAN_33_USB_S_4 | VDDAN_33_USB_S_5 | USB_HSD12P | | USB_HSD10P | USB_HSD10N | | USB_SS_RX0N | VSS | |
| L | | VIN2/SDATI_1/GPIO177 | | NC5 | | VSS | | | | | | VSS | VSS | | VSS | VSS | |
| M | VIN6/GBE_STAT3/GPIO181 | | VIN1/GPIO176 | | VIN7/GBE_LED3/GPIO182 | TEMPIN3/TALERT#/GPIO174 | BLINK/USB_OC7#/GEVENT18# | VDDAN_33_HWM_S | VDDAN_33_USB_S_6 | VDDAN_33_USB_S_7 | VDDAN_33_USB_S_12 | VDDAN_33_USB_S_10 | VSS | VDDAN_11_SUSB_S_2 | | VSS | VDDCR_11_SUSB_S_4 |
| N | | VIN0/GPIO175 | | VIN3/SDATO_1/GPIO178 | | VSS | PWR_GOOD | VSSAN_HWM | VDDAN_33_USB_S_8 | VDDAN_33_USB_S_9 | VSS | VDDAN_33_USB_S_11 | VSS | VDDAN_11_SUSB_S_3 | | VDDCR_11_SUSB_S_1 | VDDCR_11_SUSB_S_2 |
| P | VIN4/SLOAD_1/GPIO179 | | VIN5/SCLK_1/GPIO180 | | USB_OC2#/TCK/GEVENT14# | USB_OC4#/IR_RX0/GEVENT16# | | | | | | VSS | VDDAN_11_SUSB_S_4 | VDDAN_11_SUSB_S_5 | | VDDAN_11_SUSB_S_1 | VDDCR_11_SUSB_S_3 |
| R | | RI#/GEVENT22# | | VSS | | VSS | SDA1/GPIO228 | USB_OC6#/IR_TX1/GEVENT6# | PME#/GEVENT3# | THRMTRIP#/SMBALERT#/GEVENT2# | VSS | | | | | | |
| T | USB_OC5#/IR_TX0/GEVENT17# | | SLP_S3# | | LPC_PD#/GEVENT5# | SPI_CS1#/GPIO165 | SCL1/GPIO227 | USB_OC8#/GEVENT12#/TRST/ | TEST0 | TEST1/TMS | VSS | VDDCR_11_USB_S_1 | VDDCR_11_USB_S_2 | VDDCR_11_1 | | VSS | VDDCR_11_2 |
| U | | RSMRST# | | SYS_RESET#/GEVENT19# | | VSS | | | | | | VDAN_11_USB_S_1 | VDAN_11_USB_S_2 | VSS | | VDDCR_11_4 | VSS |
| V | ROM_RST#/SPI_WP#/GPIO161 | | SPI_CLK/GPIO162 | | SPI_DO/GPIO163 | SPI_DI/GPIO164 | IR_RX1/GEVENT20# | DDR3_RST#/GEVENT7#/VGA_PD | TEST2 | GBE_LED2/GEVENT10# | VSS | VDDIO_33_S_4 | VDDIO_33_S_5 | VDDCR_11_6 | | VSS | VDDCR_11_7 |
| W | | SLP_S5# | | VSS | | VSS | SPI_CS3#/GBE_STAT1/GEVENT21# | GBE_LED0/GPIO183 | GBE_PHY_INTR | GBE_MDIO | VDDIO_33_S_8 | | | | | | |
| Y | AZ_SDIN3/GPIO170 | | AZ_SDIN2/GPIO169 | | AZ_SDIN1/GPIO168 | SPI_HOLD0#/GBE_LED1/GEVENT9# | | | | | | VDDIO_33_S_6 | VDDIO_33_S_7 | VSS | | VSS | VDDCR_11_9 |
| AA | | AZ_SDIN0/GPIO167 | | VDDIO_AZ_S | | VSS | GBE_PHY_RST# | GBE_STAT0/GEVENT11# | VDDIO_GBE_S_1 | VDDIO_GBE_S_2 | VDDCR_11_GBE_S_2 | VSS | VSS | VSS | | VSS | VSS |
| AB | AZ_SDOUT | | AZ_BITCLK | | PCIRST# | PCIE_RST2#/GEVENT4# | GBE_TXCLK | GBE_RXCLK | GBE_TXCTL/TXEN | VDDIO_33_GBE_S | VDDCR_11_GBE_S_1 | VDDIO_33_PCIGP_7 | VDDIO_33_PCIGP_8 | VDDIO_33_PCIGP_9 | | VDDIO_33_PCIGP_10 | VDDIO_33_PCIGP_1 |
| AC | | GBE_PHY_PD | | GBE_COL | | VSS | | | | | | A24/GPIO24 | VDDIO_33_PCIGP_6 | | AD30/GPIO30 | INTG#/GPIO34 | |
| AD | GBE_RXERR | | GBE_CRS | | A_RST# | AZ_SYNC | GBE_RXD0 | GBE_TXD0 | GBE_MDCK | VDDIO_33_PCIGP_4 | | CBE3# | GNT1#/GPO44 | | AD29/GPIO29 | GNT0# | |
| AE | | PCIE_RST# | | AZ_RST# | | VSS | GBE_RXD1 | GBE_TXD1 | VDDIO_33_PCIGP_3 | PAR | | AD23/GPIO23 | AD25/GPIO25 | | VSS | AD31/GPIO31 | |
| AF | PCICLK1/GPO36 | | PCICLK0 | | PCICLK2/GPO37 | PCICLK4/14M_OSC/GPO39 | GBE_RXD2 | VSS | GBE_TXD3 | TRDY# | | VSS | AD26/GPIO26 | | REQ2#/CLK_REQ8#/GPIO41 | VSS | |
| AG | | PCICLK3/GPO38 | | AD2/GPIO2 | | GBE_TXD2 | VDDIO_33_PCIGP_5 | GBE_RXCTL/RXDV | AD16/GPIO16 | FRAME# | | AD22/GPIO22 | REQ1#/GPIO40 | | REQ0# | NC1 | |
| AH | STOP# | | AD4/GPIO4 | | VSS | | GBE_RXD3 | SERR# | LOCK# | NC2 | VSS | SD_WP/GPIO76 | AD27/GPIO27 | AD28/GPIO28 | SD_DATA2/GPIO79 | FANOUT0/GPIO52 | SATA_IS4#/FANOUT3/GPIO55 |
| AJ | AD9/GPIO9 | | AD0/GPIO0 | | AD5/GPIO5 | AD13/GPIO13 | | CBE1# | | AD18/GPIO18 | | SD_CD#/GPIO75 | | SD_DATA3/GPIO80 | | FANOUT2/GPIO54 | |
| AK | | | | | | | AD14/GPIO14 | | DEVSEL# | | AD20/GPIO20 | | SD_DATA0/SDATI_0/GPIO77 | | FANIN0/GPIO56 | | GNT3#/CLK_REQ7#/SATA_IS7#/GPIO46 |
| AL | AD6/GPIO6 | | AD11/GPIO11 | | AD1/GPIO1 | AD3/GPIO3 | | AD10/GPIO10 | | IRDY# | | AD19/GPIO19 | | SD_CLK/SCLK_0/GPIO73 | | FANIN2/GPIO58 | |
| AM | | | | | | | AD12/GPIO12 | | PERR# | | AD17/GPIO17 | | SD_DATA1/SDATO_0/GPIO78 | | FANOUT1/GPIO53 | | REQ3#/CLK_REQ5#/SATA_IS6#/GPIO42 |
| AN | VSS | | CBE0# | | AD7/GPIO7 | AD8/GPIO8 | | AD15/GPIO15 | | CBE2# | | AD21/GPIO21 | | SD_CMD/SLOAD_0/GPIO74 | | FANIN1/GPIO57 | |

**Figure 11. Bolton-E4 Ballout Assignment (Left)**



| 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| KSO_12/ GPIO221 | | KSO_5/ GPIO214 | | KSO_3/ GPIO212 | | KSO_16/ XDB2/ | | LAD2 | | NC3 | LAD3 | | LFRAME# | | VSS | A |
| | KSO_14/ XDB0/ | | KSO_9/ GPIO218 | | KSI_5/ GPIO206 | | LPCCLK0 | | LDRQ0# | | | | | | | B |
| KSO_13/ GPIO222 | | PS2KB_CLK /GPIO190 | | PS2M_CLK/ GPIO192 | | KSI_6/ GPIO207 | | LPC_SMI#/ GEVENT23# | | LAD1 | ML_VGA_H PD/GPIO229 | | 25M_X1 | | 25M_X2 | C |
| | KSO_11/ GPIO220 | | PS2KB_DAT /GPIO189 | | PS2M_DAT/ GPIO191 | | LPCCLK1 | | LAD0 | | | | | | | D |
| KSO_4/ GPIO213 | | KSO_1/ GPIO210 | | EC_PWM0/ EC_TIMER0/ | | KSI_4/ GPIO205 | | APU_PG | | PROCHOT# | VSS | | GPP_CLK3N | | GPP_CLK3P | E |
| KSI_7/ GPIO208 | VSS | KSO_2/ GPIO211 | KSO_0/ GPIO209 | KSI_2/ GPIO203 | VSS | KSI_3/ GPIO204 | VSS | APU_RST# | CLK_CALRN | | VSS | | GPP_CLK2N | | GPP_CLK2P | F |
| KSO_8/ GPIO217 | SDA2/ GPIO194 | | SDA3_LV/ GPIO196 | SCL3_LV/ GPIO195 | | VDDXL_33_ S | DMA_ACTIV E# | LDT_STP# | NC4 | PCIE_RCLK N | | PCIE_RCLK P | | VSS | | G |
| KSO_7/ GPIO216 | SCL2/ GPIO193 | | EC_PWM3/ EC_TIMER3/ | EC_PWM1/ EC_TIMER1/ | | VDDPL_33_ SYS | VSSPL_SYS | VDDAN_11_ CLK_1 | GPP_CLK0P | GPP_CLK0N | VSS | | DISP2_CLK N | | DISP2_CLK P | H |
| KSO_6/ GPIO215 | PS2_CLK/ SCL4/ | | SPI_CS2#/ GBE_STAT2 | EC_PWM2/ EC_TIMER2/ | | VDDPL_11_ SYS_S | VDDAN_11_ CLK_2 | 14M_25M_4 8M_OSC | GPP_CLK1P | VSS | | SLT_GFX_C LKP | | VSS | | J |
| KSO_10/ GPIO219 | PS2_DAT/ SDA4/ | | KSI_0/ GPIO201 | KSI_1/ GPIO202 | | VDDAN_11_ CLK_3 | VSSXL | GPP_CLK1N | VSS | VSS | SLT_GFX_C LKN | | VGA_DAC_ RSET | | VSSANQ_D AC | K |
| VDDPL_33_ SSUSB_S | VDDIO_33_ S_2 | | VSS | VDDAN_11_ CLK_4 | | | | | | VSSAN_DA C | | VGA_RED | | VGA_GREE N | | L |
| VDDIO_33_ S_3 | | VDDCR_11_ S_2 | VSS | VDDAN_11_ CLK_5 | GPP_CLK4P | GPP_CLK4N | VSS | GPP_CLK5N | GPP_CLK5P | VGA_HSYN C/GPO68 | VGA_BLUE | | LDO_CAP | | VGA_DDC_ SDA/GPO70 | M |
| VDDIO_33_ S_1 | | VDDCR_11_ S_1 | VDDAN_11_ CLK_6 | VDDAN_11_ CLK_7 | VSS | VSS | GPP_CLK6P | GPP_CLK6N | GPP_CLK8P | VSSIO_DAC | | VGA_VSYN C/GPO69 | | VGA_DDC_ SCL/GPO71 | | N |
| VSS | | VSS | VSS | VDDAN_11_ CLK_8 | | | | | | ML_VGA_L3 N | ML_VGA_L3 P | | VSS | | VSS | P |
| | | | | | GPP_CLK7P | GPP_CLK7N | VSS | DISP_CLKP | GPP_CLK8N | VSS | | ML_VGA_L2 N | | ML_VGA_L2 P | | | R |
| VSS | | VDDCR_11_ 3 | VSSPL_DAC | VDDAN_33_ DAC | APU_CLKN | APU_CLKP | VSS | DISP_CLKN | VSS | ML_VGA_L1 N | ML_VGA_L1 P | | ML_VGA_L0 P | | ML_VGA_L0 N | T |
| VDDCR_11_ 5 | | VSS | VSS | VDDPL_33_ ML | | | | | | AUXCAL | | VSS | | VSS | | U |
| VSS | | VDDCR_11_ 8 | VDDPL_11_ DAC | VDDPL_33_ DAC | VDDAN_11_ ML_2 | VDDAN_11_ ML_3 | VDDAN_11_ ML_4 | GPP_RX2P | GPP_RX1N | AUX_VGA_ CH_P | AUX_VGA_ CH_N | | GPP_TX0N | | GPP_TX0P | V |
| | | | | | GPP_RX3N | GPP_RX3P | VSS | GPP_RX2N | GPP_RX1P | VSS | | GPP_TX1P | | GPP_TX1N | | W |
| VSS | | VDDAN_11_ SATA_4 | VDDAN_11_ PCIE_2 | VDDAN_11_ ML_1 | | | | | | UMI_RX3P | UMI_RX3N | | UMI_RX2N | | UMI_RX2P | Y |
| VDDAN_11_ SATA_8 | | VDDAN_11_ SATA_7 | VDDAN_11_ SATA_1 | VDDAN_11_ PCIE_6 | GPP_TX3N | GPP_TX3P | VSS | GPP_RX0N | GPP_RX0P | VSS | | VSS | | VSS | | AA |
| VDDIO_33_ PCIGP_2 | | VDDAN_11_ SATA_9 | VDDAN_11_ SATA_2 | VDDAN_11_ SATA_3 | VDDAN_11_ PCIE_5 | VDDAN_11_ PCIE_1 | VSS | GPP_TX2P | GPP_TX2N | UMI_RX1P | UMI_RX1N | | UMI_RX0N | | UMI_RX0P | AB |
| VSS | VDDAN_11_ SATA_10 | | VDDAN_11_ SATA_6 | VDDAN_11_ SATA_5 | | | | | | VSS | | UMI_TX3P | | UMI_TX3N | | AC |
| INTH#/ GPIO35 | CLKRUN# | | GNT2#/ SD_LED/ | SATA_ACT# /GPIO67 | | VDDAN_11_ PCIE_4 | SDA0/ GPIO47 | SCL0/ GPIO43 | VSS | UMI_TX2P | UMI_TX2N | | UMI_TX1N | | UMI_TX1P | AD |
| INTF#/ GPIO33 | SERIRQ/ GPIO48 | | VSS | GA20IN/ GEVENT0# | | CLK_REQ3# /SATA_IS1#/ | VDDAN_11_ PCIE_3 | SMARTVOL T1/ | LDRQ1#/ CLK_REQ6# | VSS | | UMI_TX0P | | UMI_TX0N | | AE |
| INTE#/ GPIO32 | WD_PWRG D | | SATA_X1 | CLK_REQ0# /SATA_IS3#/ | | SPKR/ GPIO66 | CLK_REQG #/GPIO65/ | VDDAN_11_ PCIE_7 | SATA_CALR N | SATA_CALR P | PCIE_CALR P | | PCIE_CALR N | | VSS | AF |
| SATA_IS5#/ FANIN3/ | KBRST#/ GEVENT1# | | SATA_X2 | CLK_REQ1# /FANOUT4/ | | CLK_REQ4# /SATA_IS0#/ | CLK_REQ2# /FANIN4/ | SMARTVOL T2/ | VDDAN_11_ PCIE_8 | VDDPL_33_ SATA | | VSS | | VSS | | AG |
| VSS | VSS | SATA_RX1N | VSS | SATA_TX2N | VSS | SATA_TX3P | VSS | SATA_RX4P | VSS | | VDDPL_33_ PCIE | | SATA_TX7N | | SATA_TX7P | AH |
| VSS | | SATA_RX1P | | SATA_TX2P | | SATA_TX3N | | SATA_RX4N | | VSS | VSS | | SATA_RX7P | | SATA_RX7N | AJ |
| | SATA_TX0P | | VSS | | SATA_RX2P | | VSS | | SATA_RX5N | | | | | | | AK |
| VSS | | SATA_RX0N | | SATA_TX1N | | SATA_RX3P | | SATA_TX4P | | SATA_TX5N | SATA_TX6P | | SATA_RX6N | | SATA_RX6P | AL |
| | SATA_TX0N | | VSS | | SATA_RX2N | | VSS | | SATA_RX5P | | | | | | | AM |
| VSS | | SATA_RX0P | | SATA_TX1P | | SATA_RX3N | | SATA_TX4N | | VSS | SATA_TX5P | | SATA_TX6N | | VSS | AN |
| 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | |

**Figure 12. Bolton-E4 Ballout Assignment (Right)**

# Chapter 4 Pin Descriptions

***Notes:***

*For multi-functional pins, please refer to the relevant section for description of a specific function (e.g., for USB_FSD1P/GPIO186, the USB_FSD1P function is described in* Section 4.6 “USB Interface” on page 51*, and the GPIO186 function is described in* Section 4.21 “General Purpose I/O and General Event Pins” on page 67).

## 4.1 APU Interface

**Table 8. APU Interface Pin Descriptions**

| Pin name | Type | Voltage | Functional Description |
|---|---|---|---|
| DMA_ACTIVE# | In/OD | VDDIO_33_S (0.8V threshold) | DMA_ACTIVE#. See Section 4.14 “Power Management Interface” on page 57 for description. |
| APU_PG | OD | VDDIO_33_S | APU Power Good |
| APU_RST# | OD | VDDIO_33_S | APU Reset. See Section 4.16 “Reset Pins” on page 60 for description. |
| LDT_STP# | OD | VDDIO_33_S | Not used. Leave unconnected. |
| PROCHOT# | I | VDDIO_33_S (0.8V threshold) | Processor Hot: Similar to TALERT#. When it is asserted, it can generate SCI or SMI to OS/BIOS |

## 4.2 LPC Interface

**Table 9. LPC Interface Pin Descriptions**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| CLKRUN# | I/O | VDDIO_33_PCIGP (5V tolerance) | See Section 4.17 “Clock Interface” on page 62 for description. |
| GA20IN/GEVENT0# | I | VDDIO_33_PCIGP (5V tolerance) | A20 Gate Input from SIO / General Event 0 |
| KBRST#/ GEVENT1# | I | VDDIO_33_PCIGP (5V tolerance) | Keyboard reset# / General Event 1 |
| LAD[3:0] | I/O | VDDIO_33_S | Multiplexed Command / Address/Data [3:0] |
| LDRQ0# | I | VDDIO_33_S | Encoded DMA Bus Master Request 0 |
| LDRQ1#/ CLK_REQ6#/ GPIO49 | I/O | VDDIO_33_PCIGP (5V tolerance) | Encoded DMA Bus Master Request 1 / Clock Request 6 / GPIO 49 |
| LFRAME# | O | VDDIO_33_S | LPC Bus Frame. Indicates start of a new cycle or termination of a broken cycle. |
| LPCCLK0 | O | VDDIO_33_S | 33MHz LPCCLK for LPC device such as flash ROM |

**Table 9. LPC Interface Pin Descriptions**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| LPCCLK1 | O | VDDIO_33_S | 33MHz LPCCLK for LPC device such as SIO device |
| LPC_SMI#/ GEVENT23# | I | VDDIO_33_S | LPC SMI / General Event 23 |
| SERIRQ/GPIO48 | I/O | VDDIO_33_PCIGP (5V tolerance) | Serial IRQ / GPIO 48 |
| ***Note:*** *LPCCLK0 can be assigned to any LPC device. This clock can be active during sleep state during initial G3->S5 or when IMC is enabled. LPCCLK1 and PCI clock can be used for additional LPC devices that do not require a clock in S3–S5 states.* | | | |

# 4.3 Unified Media Interface (UMI)

**Table 10. UMI Pin Descriptions**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| UMI_TX[3:0]P | O | VDDAN_11_ PCIE | SCL Lane 3-0 Transmit Positive |
| UMI_TX[3:0]N | O | | SCL Lane 3-0 Transmit Negative |
| UMI_RX[3:0]P | I | | SCL Lane 3-0 Receive Positive |
| UMI_RX[3:0]N | I | | SCL Lane 3-0 Receive Negative |
| PCIE_CALRP | I/O | | Pad connection to an external resistor to VSS on board required for TX impedance calibration. |
| PCIE_CALRN | I/O | | Pad connection to an external resistor to VDDAN_11_PCIE on board required for RX impedance calibration. |

# 4.4 General Purpose PCI Express® Ports Interface

**Table 11. General Purpose PCI Express® Ports Interface Pin Descriptions**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| GPP_TX[3:0]P | O | VDDAN_11_ PCIE | General purpose PCIe® ports Lane 3 to 0 Transmit Positive |
| GPP_TX[3:0]N | O | | General purpose PCIe ports Lane 3 to 0 Transmit Negative |
| GPP_RX[3:0]P | I | | General purpose PCIe ports Lane 3 to 0 Receive Positive |
| GPP_RX[3:0]N | I | | General purpose PCIe ports Lane 3 to 0 Receive Negative |

# 4.5 PCI Interface (PCI Host Bus and Internal PCI/PCI Bridge)

**Table 12. PCI Interface (PCI Host Bus and Internal PCI/PCI Bridge) Pin Description**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| AD[31:0]/ GPIO[31:0] | I/O | VDDIO_33_PCIGP (5V tolerance) | PCI Bus Address/Data [31:0] / GPIO[31:0] |
| CBE[3:0]# | I/O | VDDIO_33_PCIGP (5V tolerance) | Command/Byte Enable[3:0] |
| CLKRUN# | I/O | VDDIO_33_PCIGP (5V tolerance) | See Section 4.17 “Clock Interface” on page 62 for description. |
| DEVSEL# | I/O | VDDIO_33_PCIGP (5V tolerance) | Device Select. Driven by target to indicate it has decoded its address as the target of the current access. |
| FRAME# | I/O | VDDIO_33_PCIGP (5V tolerance) | Cycle Frame. Driven by the current master to indicate the beginning and duration of an access. |
| GNT0# | O | VDDIO_33_PCIGP (5V tolerance) | PCI Bus Grant 0 from the FCH. Indicates to the agent that access to the bus has been granted. |
| GNT1#/GPO44 | O | VDDIO_33_PCIGP (5V tolerance) | PCI Bus Grant 1 from the FCH. Indicates to the agent that access to the bus has been granted. Pin muxed with GPIO44 |
| GNT2#/SD_LED/ GPO45 | O | VDDIO_33_PCIGP (5V tolerance) | PCI Bus Grant 2 from the FCH. Indicates to the agent that access to the bus has been granted. Pin muxed with GPIO45 |
| GNT3#/ CLK_REQ7#/ GPIO46 | I/O | VDDIO_33_PCIGP (5V tolerance) | PCI Bus Grant 3 from the FCH. Indicates to the agent that access to the bus has been granted. Pin muxed with GPIO46 |
| INTH#/GPIO35 | I/O | VDDIO_33_PCIGP (5V tolerance) | PCI Interrupt H / GPIO 35 |
| INTG#/ GPIO34 | I/O | VDDIO_33_PCIGP (5V tolerance) | PCI Interrupt G / GPIO 33 |
| INTF#/GPIO33 | I/O | VDDIO_33_PCIGP (5V tolerance) | PCI Interrupt F / GPIO 33 |
| INTE#/GPIO32 | I/O | VDDIO_33_PCIGP (5V tolerance) | PCI Interrupt E / GPIO 32 |
| IRDY# | I/O | VDDIO_33_PCIGP (5V tolerance) | Initiator Ready: Indicates the initiating agent’s ability to complete the current data phase of the transaction |
| LOCK# | I/OD | VDDIO_33_PCIGP (5V tolerance) | PCI Bus Lock |
| PAR | I/O | VDDIO_33_PCIGP (5V tolerance) | PCI Bus Parity |
| PCICLK0 | O | VDDIO_33_PCIGP (5V tolerance) | 33 MHz PCI clock 0 |

**Table 12. PCI Interface (PCI Host Bus and Internal PCI/PCI Bridge) Pin Description**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| PCICLK[3:1]/ GPO[38:36] | O | VDDIO_33_PCIGP (5V tolerance) | 33 MHz PCI clock [3:1] |
| PCICLK4/ 14M_OSC/GPO39 | O | VDDIO_33_PCIGP (5V tolerance) | 33 MHz PCI clock 4. See Section 4.17 “Clock Interface” on page 62 for description. |
| PCIRST# | O | VDDIO_33_PCIGP (5V tolerance) | Hardware Reset for PCI Slots. See Section 4.16 “Reset Pins” on page 60 for description. |
| A_RST# | O | VDDIO_33_S (5V tolerance) | PCI Host Bus Reset. See Section 4.16 “Reset Pins” on page 60 for description. |
| PERR# | I/O | VDDIO_33_PCIGP (5V tolerance) | Parity Error. Reports data parity errors during all PCI transactions, except in a special cycle. |
| REQ0# | I | VDDIO_33_PCIGP (5V tolerance) | PCI Request 0 Input. Indicates that the agent desires use of the bus. |
| REQ1#/GPIO40 | I | VDDIO_33_PCIGP (5V tolerance) | PCI Request 1 Input. Indicates that the agent desires use of the bus. |
| REQ2#/ CLK_REQ8#/ GPIO41 | I | VDDIO_33_PCIGP (5V tolerance) | Request 2 Input. Indicates that the agent desires use of the bus |
| REQ3#/ CLK_REQ5#/ GPIO42 | I | VDDIO_33_PCIGP (5V tolerance) | Request 3 Input. Indicates that the agent desires use of the bus. |
| SERR# | I/OD | VDDIO_33_PCIGP (5V tolerance) | System Error. For reporting address parity errors and data parity errors on the special cycle command, or any other system error where the result will be catastrophic. |
| STOP# | I/O | VDDIO_33_PCIGP (5V tolerance) | Stop. Indicates the current target is requesting the master to stop the current transaction |
| TRDY# | I/O | VDDIO_33_PCIGP (5V tolerance) | Target Ready. Indicates the target agent’s ability to complete the current data phase of the transaction. |

# 4.6 USB Interface

**Table 13. USB Interface Pin Descriptions**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| USB_SS_TX[3:0]P | I/O | VDDAN_11_SSUSB | USB Super Speed port 3:0 Transmit Positive |
| USB_SS_TX[3:0]N | I/O | VDDAN_11_SSUSB | USB Super Speed port 3:0 Transmit Negative |
| USB_SS_RX[3:0]P | I/O | VDDAN_11_SSUSB | USB Super Speed port 3:0 Receive Positive |
| USB_SS_RX[3:0]N | I/O | VDDAN_11_SSUSB | USB Super Speed port 3:0 Receive Negative |
| USB_HSD[13:0]P | I/O | VDDAN_33_USB | USB Port 13:0 Positive I/O |
| USB_HSD[13:0]N | I/O | VDDAN_33_USB | USB Port 13:0 Negative I/O |
| USB_FSD1P/ GPIO186 | I/O | VDDIO_33_S | USB port 1 (full/low speed) Positive I/O |
| USB_FSD0P/ GPIO185 | I/O | VDDIO_33_S | USB port 0 (full/low speed) Positive I/O |
| USB_FSD[1:0]N | I/O | VDDIO_33_S | USB port 1:0 (full/low speed) Negative I/O |
| USBCLK/ 14M_25M_48M_OSC | I/O | VDDPL_33_USB | See Section 4.16 “Reset Pins” on page 60; Section 4.17 “Clock Interface” on page 62; and Section 4.18 “ATE/JTAG Interface” on page 65 |
| USB_RCOMP | I | VDDPL_33_USB | Compensating resistors input. |
| USB_OC0#/ GEVENT12#/TRST | I/O | VDDIO_33_S | USB Over Current 0# |
| USB_OC1#/TDI/ GEVENT13# | I/O | VDDIO_33_S | USB Over Current 1# |
| USB_OC2#/TCK/ GEVENT14# | I/O | VDDIO_33_S | USB Over Current 2# |
| USB_OC3#/ AC_PRES/TDO/ GEVENT15# | I/O | VDDIO_33_S | USB Over Current 3# |
| USB_OC4#/ IR_RX0/ GEVENT16# | I/O | VDDIO_33_S | USB Over Current 4# |
| USB_OC5#/ IR_TX0/ GEVENT17# | I/O | VDDIO_33_S | USB Over Current 5# |
| USB_OC6#/ IR_TX1/ GEVENT6# | I/O | VDDIO_33_S | USB Over Current 6# |
| BLINK/ USB_OC7#/ GEVENT18# | I/O | VDDIO_33_S | USB Over Current 7# |
| USBSS_CALRP | I | VDDAN_11_SSUSB | Pad connection to an external resistor to VSS (close to USBSS interface) on the motherboard, for TX impedance calibration |

**Table 13. USB Interface Pin Descriptions (Continued)**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| USBSS_CALRN | I | VDDAN_11_SSUSB | Pad connection to an external resistor to VDDAN_11_SSUSB on the motherboard, for RX impedance calibration |

***Note:***

1. *The USB_HSD[13:0]P and USB_HSD[13:0]N signals are used for connecting internal or external USB devices through the USB Port connectors. These ports are handled by users and are subject directly to ESD events to either the connector, the device, or to the pins themselves. The USB_HSDP and USB_HSDN signals that may be exposed to the user through an USB port connection must have ESD protection.*
2. *The USB_FSD[1:0]P and USB _FSD[1:0]N signals are used only for connecting to internal devices. They support only full or low, but not high speed devices.*
3. *The USBCK/14M_25M_48M_OSC pin (G8) as well as the 14M_25M_48M_OSC pin (J26) output a 14.318MHz clock on the first power up if the internal system clock generator mode strap is selected.*

# 4.7 SD Card Interface

**Table 14. SD Card Interface Pin Descriptions**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| SD_CLK/SCLK_0/GPIO73 | O | VDDIO_33_PCIGP | SD Clock |
| SD_CMD/SLOAD_0/GPIO74 | O | | SD Command |
| SD_CD#/GPIO75 | I | | SD Card Detect |
| SD_WP/GPIO76 | O | | SD Write Protect |
| SD_DATA0/SDATI_0/GPIO77 | I/O | | SD Data |
| SD_DATA1/SDATO_0/GPIO78 | I/O | | SD Data 1 |
| SD_DATA2/GPIO79 | I/O | | SD Data 2 |
| SD_DATA3/GPIO80 | I/O | | SD Data 3 |
| GNT2#/SD_LED/GPO45 | O | | SD LED |

# 4.8 Serial ATA Interface

**Table 15. Serial ATA Interface Pin Descriptions**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| SATA_ACT#/GPIO67 | OD | VDDIO_33_PCIGP | SATA Channel Active |
| SATA_CALRP | I | VDDAN_11_SATA | Pad connection to an external resistor to VSS close to the SATA interface on the motherboard, for TX impedance calibration |
| SATA_CALRN | I | VDDAN_11_SATA | Pad connection to an external resistor to VDDAN_11_SATA on the motherboard, for RX impedance calibration |
| SATA_RX[57:0]N | I | VDDAN_11_SATA | SATA Channel[57:0] Receive Negative |
| SATA_RX[57:0]P | I | VDDAN_11_SATA | SATA Channel[57:0] Receive Positive |

**Table 15. Serial ATA Interface Pin Descriptions (Continued)**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| SATA_TX[57:0]N | O | VDDAN_11_SATA | SATA Channel[57:0] Transmit Negative |
| SATA_TX[57:0]P | O | VDDAN_11_SATA | SATA Channel[57:0] Transmit Positive |
| SATA_X1 | I | VDDPL_33_SATA | SATA 25MHz crystal clock input (external clock mode) |
| SATA_X2 | O | VDDPL_33_SATA | SATA 25MHz crystal clock input (external clock mode) |
| CLK_REQ4#/ SATA_IS0#/GPIO64 | I/O | VDDIO_33_PCIGP | SATA Interlock Switch Port 0 (Input) * |
| CLKREQ3#/ SATA_IS1#/GPIO63 | I/O | VDDIO_33_PCIGP | SATA Interlock Switch Port 1 (Input) * |
| SMARTVOLT1/ SATA_IS2#/GPIO50 | I/O | VDDIO_33_PCIGP | SATA Interlock Switch Port 2 (input) * |
| CLKREQ0#/ SATA_IS3#/GPIO60 | I/O | VDDIO_33_PCIGP | SATA Interlock Switch Port 3 (input) * |
| SATA_IS4#/ FANOUT3/GPIO55 | I/O | VDDIO_33_PCIGP | SATA Interlock Switch Port 4 (input) * |
| SATA_IS5#/FANIN3/ GPIO59 | I/O | VDDIO_33_PCIGP | SATA Interlock Switch Port 5 (input) * |
| REQ3#/CLK_REQ5#/ SATA_IS6#/GPIO42 | I/O | VDDIO_33_PCIGP | SATA Interlock Switch Port 6 (input) * |
| GNT3#/CLK_REQ7#/ SATA_IS7#/GPIO46 | I/O | VDDIO_33_PCIGP | SATA Interlock Switch Port 7 (input) * |
| VIN2/SDATI_1/ GPIO177 | I/O | VDDIO_33_S | SGPIO Data In (set 1) ** |
| VIN3/SDATO_1/ GPIO178 | I/O | VDDIO_33_S | SGPIO Data Out (set 1) ** |
| VIN4/SLOAD_1/ GPIO179 | I/O | VDDIO_33_S | SGPIO Load (set 1) ** |
| VIN5/SCLK_1/ GPIO180 | I/O | VDDIO_33_S | SGPIO Clock (set 1) ** |
| SD_CLK/SCLK_0/ GPIO73 | I/O | VDDIO_33_PCIGP | SGPIO Clock (set 0) ** |
| SD_CMD/SLOAD_0/ GPIO74 | I/O | VDDIO_33_PCIGP | SGPIO Load (set 0) ** |
| SD_DATA0/ SDATI_0/GPIO77 | I/O | VDDIO_33_PCIGP | SGPIO Data In (set 0) ** |
| SD_DATA1/ SDATO_0/GPIO78 | I/O | VDDIO_33_PCIGP | SGPIO Data Out (set 0) ** |

***Notes:***

1. ** SATA_ISx#: These are Hot Plug external interlock switches (one for each SATA port). The SATA Hot Plug function support with AMD drivers does not require the use of these signals. Please refer to the Bolton Motherboard Design Guide on how to terminate these signals.*
2. *** Bolton-E4 supports up to two sets of SGPIO.*

# 4.9 HD Audio Interface

**Table 16. HD Audio Interface Pin Descriptions**

| Pin Name | Type | Voltage | Functional description |
|---|---|---|---|
| AZ_BITCLK | O | VDDIO_33_S/VDDIO_AZ_S (1.5V) | HD Audio Interface Bit Clock |
| AZ_RST# | O | VDDIO_33_S/VDDIO_AZ_S (1.5V) | HD Audio Interface Reset |
| AZ_SDIN[3:0]/ GPIO[170:167] | I/O | VDDIO_33_S/VDDIO_AZ_S (1.5V) | HD Audio Serial Data Input from Codec [3:0]/ GPIO [170:167] |
| AZ_SDOUT | O | VDDIO_33_S/VDDIO_AZ_S (1.5V) | HD Audio Serial Data Output to Codec |
| AZ_SYNC | O | VDDIO_33_S/VDDIO_AZ_S (1.5V) | HD Audio Sync signal to Codec |

# 4.10 Real Time Clock Interface

**Table 17. Real Time Clock Interface**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| 32K_X1 | I | VDDIO_33_S/ VDDBT_RTC_G | RTC crystal oscillator input 1 (internal RTC). See Section 4.17 “Clock Interface” on page 62 for description. |
| 32K_X2 | O | VDDIO_33_S/ VDDBT_RTC_G | RTC crystal oscillator input 2 (internal RTC). See Section 4.17 “Clock Interface” on page 62 for description. |
| RTCCLK | I/O | VDDIO_33_S | 32 kHz output for internal RTC. |
| INTRUDER_ALERT# | I | VDDBT_RTC_G | Intruder alert sense input |
| S5_CORE_EN | O | VDDIO_33_S | S5 Core Enable. See Section 4.14 “Power Management Interface” on page 57 for description. |
| USB_OC3#/ AC_PRES/TDO/ GEVENT15# | I/O | VDDIO_33_S | AC Power Present. See Section 4.14 “Power Management Interface” on page 57 for description. |
| WAKE#/ GEVENT8# | I/O | VDDIO_33_S | PCIe® Wake. See Section 4.14 “Power Management Interface” on page 57 for description. |
| IR_LED#/LLB#/ GPIO184 | I/O | VDDIO_33_S | Low Low Battery. Connected to the battery circuit signal output that indicates a battery low condition. When the function is enabled, an assertion of this pin will prevent the system from waking up by any wake event . |

**Table 17. Real Time Clock Interface (Continued)**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| SLP_S3# | O | VDDIO_33_S | S3 Sleep Power plane control. See Section 4.14 “Power Management Interface” on page 57 for description. |
| SLP_S5# | O | VDDIO_33_S | S5 Sleep Power plane control. See Section 4.14 “Power Management Interface” on page 57 for description. |
| PWR_BTN# | I | VDDIO_33_S | Power Button. See Section 4.14 “Power Management Interface” on page 57 for description. |

# 4.11 Hardware Monitor Interface

**Table 18. Hardware Monitor Interface Pin Descriptions**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| CLK_REQ1#/ FANOUT4/GPIO61 | I/O | VDD_IO_33_PCIGP (5V tolerance) | Fan PWM Output 4 |
| CLK_REQ2#/ FANIN4/GPIO62 | I/O | VDD_IO_33_PCIGP (5V tolerance) | Fan Input 4 |
| FANIN[2:0]/ GPIO[58:56] | I/O | VDD_IO_33_PCIGP (5V tolerance) | Fan Tachometer Input [2:0] |
| FANOUT[2:0]/ GPIO[54:52] | I/O | VDD_IO_33_PCIGP (5V tolerance) | Fan PWM Output [2:0] |
| SATA_IS4#/ FANOUT3/GPIO55 | I/O | VDD_IO_33_PCIGP (5V tolerance) | Fan Control Output 3 |
| SATA_IS5#/ FANIN3/GPIO59 | I/O | VDD_IO_33_PCIGP (5V tolerance) | Fan Input 3 |
| TEMPIN[2:0]/ GPIO[173:171] | I/O | VDDIO_33_S | Temperature Monitor Input [2:0] (not supported) |
| TEMPIN3/ TALERT#/GPIO174 | I/O | VDDIO_33_S | Temperature Monitor Input 3 (not supported) / Temperature has reached cautionary state |
| VIN0/GPIO175 | I/O | VDDIO_33_S | Voltage Monitor Input 0 (not supported) |
| VIN1/GPIO176 | I/O | VDDIO_33_S | Voltage Monitor Input 1 (not supported) |
| VIN2/SDATI_1/ GPIO177 | I/O | VDDIO_33_S | Voltage Monitor Input 2 (not supported) |
| VIN3/SDATO_1/ GPIO178 | I/O | VDDIO_33_S | Voltage Monitor Input 3 (not supported) |
| VIN4/SLOAD_1/ GPIO179 | I/O | VDDIO_33_S | Voltage Monitor Input 4 (not supported) |
| VIN5/SCLK_1/ GPIO180 | I/O | VDDIO_33_S | Voltage Monitor Input 5 (not supported) |
| VIN6/GBE_STAT3/ GPIO181 | I/O | VDDIO_33_S | Voltage Monitor Input 6 (not supported) |

**Table 18. Hardware Monitor Interface Pin Descriptions**

| | | | |
|---|---|---|---|
| VIN7/GBE_LED3/ GPIO182 | I/O | VDDIO_33_S | Voltage Monitor Input 7 (not supported) |

# 4.12 VGA Translator Interface

**Table 19. VGA Translator Interface Pin Descriptions**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| ML_VGA_L[3:0]P | I | VDDAN_11_ML | Translator Input [3:0] Positive |
| ML_VGA_L[3:0]N | I | VDDAN_11_ML | Translator Input [3:0] Negative |
| ML_VGA_HPD/ GPIO229 | I/O* | VDDIO_33_S | VGA Hot Plug Detect<br>* Programmed by software to output as required, see Table 28 on page 67, for default I/O state. |
| AUXCAL | I/O | VDDIO_33_PCIGP | AUX Port Calibration |
| AUX_VGA_CH_P | I/O | VDDIO_33_PCIGP | AUX Port Positive |
| AUX_VGA_CH_N | I/O | VDDIO_33_PCIGP | AUX Port Negative |
| VGA_RED | O | LDO_CAP (internally- generated supply) | VGA Red Output |
| VGA_BLUE | O | LDO_CAP | VGA Blue Output |
| VGA_GREEN | O | LDO_CAP | VGA Green Output |
| VGA_HSYNC/ GPO68 | O | VDDIO_33_PCIGP | VGA Horizontal SYNC |
| VGA_VSYNC/ GPO69 | O | VDDIO_33_PCIGP | VGA Veritical SYNC |
| VGA_DAC_RSET | O | VDDIO_33_PCIGP | DAC Reset |
| VGA_DDC_SDA/ GPO70 | I/O | VDDIO_33_PCIGP (5V tolerance) | VGA DDC Data |
| VGA_DDC_SCL/ GPO71 | I/O | VDDIO_33_PCIGP (5V tolerance) | VGA DDC Clock |
| DDR3_RST#/ GEVENT7#/ VGA_PD | O* | VDDIO_33_S | VGA Power Down. This pin is used to power down the VGA DAC regulators when no display is connected.<br>**** Note:** Pin type is OD for DDR_RST#, and I/O for GEVENT7#* |

# 4.13 SPI ROM Interface

SPI ROM is supported up to 66 MHz. The burst read and fast read cycles are not supported. Refer to Section 6.5.3.3 “SPI AC Specifications” on page 107 for timing information.

**Table 20. SPI ROM Interface Pin Descriptions**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| SPI_CS1#/GPIO165 | I/O | VDDIO_33_S | SPI Chip Select1# |
| SPI_CS2#/GBE_STAT2/ GPIO166 | I/O | VDDIO_33_S | SPI Chip Select2# |
| SPI_CS3#/GBE_STAT1/ GEVENT21# | I/O | VDDIO_33_S | SPI Chip Select3# |
| SPI_CLK/GPIO162 | I/O | VDDIO_33_S | SPI Clock |
| SPI_DI/GPIO164 | I/O | VDDIO_33_S | SPI Data In |
| SPI_DO/GPIO163 | I/O | VDDIO_33_S | SPI Data Output |
| SPI_HOLD#/ GBE_LED1/GEVENT9# | I/O | VDDIO_33_S | SPI HOLD#. Assert low to hold the SPI transaction. |
| ROM_RST#/SPI_WP#/ GPIO161 | I/O | VDDIO_33_S | ROM reset (LPC flash) or SPI write protect (active low) |
| LPC_PD#/GEVENT5# | I/O | VDDIO_33_S | LPC power down (negative logic) |

# 4.14 Power Management Interface

**Table 21. Power Management Interface Pin Descriptions**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| DMA_ACTIVE# | In/OD | VDDIO_33_S (0.8V threshold) | DMA active. Bolton-E4 drives the DMA_ACTIVE# to APU to notify DMA activity. This will cause the APU to re-establish the SCL link quicker. |
| PME#/GEVENT3# | I/O | VDDIO_33_S | LPC/PCI PME# Power management signal for LPC/ PCI interface. |
| LPC_SMI#/ GEVENT23# | I/O | VDDIO_33_S | LPC SMI Input |
| PWR_BTN# | I | VDDIO_33_S | Power Button. The Power Button causes an SMI or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWRBTN# is pressed for more than 4 seconds, it will cause an unconditional transition (power button override) to the S5 state with only the PWRBTN# available as a wake event. This signal has an internal pull-up resistor. |

**Table 21. Power Management Interface Pin Descriptions (Continued)**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| PWR_GOOD | I | VDDIO_33_S | Power good input. Assertion of PWR_GOOD by the power good circuit on the motherboard indicates that power supplies to the Bolton-E4 are valid. Assertion takes place sometime after APU Power Good is asserted.<br>Deassertion of PWR_GOOD by the power good circuit indicates that the power supplies to the chip are NOT valid. Deassertion takes place sometime after SLP_S3# or SLP_S5#'s assertion, or after Power Supply Power Good is deasserted. |
| RI#/GEVENT22# | I/O | VDDIO_33_S | Ring Indicator |
| S5_CORE_EN | O | VDDIO_33_S | S5 Core Enable. |
| SMARTVOLT2/ SHUTDOWN#/ GPIO51 | I/O | VDDIO_33_PCIGP (5V tolerance) | System Shutdown.<br>Assertion will cause the Bolton-E4 to assert SLP_S3# and SLP_S5# to force system to transition to S5 immediately, without waiting for the STPGNT message from the APU. |
| SLP_S3# | O | VDDIO_33_S | S3 Sleep Power plane control.<br>Assertion of SLP_S3# shuts off power to non-critical components when system transitions to S3, S4, or S5 states.<br>Deassertion of SLP_S3# turns on power to non-critical components when system transitions from S3, S4, or S5 back to S0. Deassertion takes place sometime after a wake-up event has been triggered. |
| SLP_S5# | O | VDDIO_33_S | S5 Sleep Power plane control.<br>Assertion of SLP_S5# shuts power off to non-critical components when system transitions to S4 or S5 state.<br>Deassertion of SLP_S5# turns on power to non-critical components when transitioning from S4/S5 back to S0 state. Deassertion takes place sometime after a wake-up event is triggered. |
| THRMTRIP#/ SMBALERT#/ GEVENT2# | I/O | VDDIO_33_S | Thermal Trip.<br>Indicates to Bolton E4 that a thermal trip has occurred. Its assertion will cause Bolton E4 to transition the system to S5 immediately, without waiting for the STPGNT message from the processor.<br>***Note:*** *If Thermtrip function is required, the SMBalert function can be mapped to any other available Gevent pin.* |

**Table 21. Power Management Interface Pin Descriptions (Continued)**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| TEMPIN3/ TALERT#/ GPIO174 | I/O | VDDIO_33_S | Thermal Alert.<br>The signal is a thermal alert to the FCH. The FCH can be programmed to generate an SMI, SCI, or IRQ13 through GPE, or generate an SMI without GPE in response to the signal's assertion. See the *AMD Bolton Fusion Controller Hub Register Reference Guide* for details. |
| USB_OC3#/ AC_PRES/TDO/ GEVENT15# | I/O | VDDIO_33_S | AC Power Present. Used by the FCH to check if AC power is present. |
| WAKE#/ GEVENT8# | I/O | VDDIO_33_S | PCIe Wake. WAKE# signal is required for PCIe devices. This signal is routed from the PCIe device/slot to the FCH. Note: the WAKE# is in S5 domain so it is active when the system is in S5 state. Care must be taken when plugging in the PCIe devices: the system should be transitioned into G3 state (S5 Power OFF) before a PCIe device is installed. Plugging in a PCIe device when the system is in S5 state may cause the system to wake up. That is because the WAKE# signal driven by the PCIe device may transition momentarily to active state when the device is installed but has not been initialized to drive the signal in an inactive state. |
| WD_PWRGD | OD | VDDIO_33_PCIGP | The pin is not used by the FCH. Refer to the *AMD Bolton Fusion Controller Hub Motherboard Design Guide* on how to handle the pin. |

# 4.15 SMBus Interface

**Table 22. SMBus Interface Pin Descriptions**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| SCL0/GPIO43 | I/O | VDDIO_33_PCIGP (5V tolerance) | SMBus Clock 0 |
| SDA0/GPIO47 | I/O | VDDIO_33_PCIGP (5V tolerance) | SMBus Data 0 |
| SCL1/GPIO227 | I/O | VDDIO_33_S | SMBus Clock 1. SMBus Clock 1 supports an ASF interface or a Synaptics InterTouch Touchpad. See Note 1 below. |
| SDA1/GPIO228 | I/O | VDDIO_33_S | SMBus Data 1. SMBus Data 1 supports an ASF interface or a Synaptics InterTouch Touchpad. See Note 1 below. |

**Table 22. SMBus Interface Pin Descriptions (Continued)**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| SCL2/GPIO193 | I/O | VDDIO_33_S | SMBus Clock 2 |
| SDA2/GPIO194 | I/O | VDDIO_33_S | SMBus Data 2 |
| SCL3_LV/GPIO195 | I/O | VDDIO_33_S domain (0.8V threshold) | SMBus Clock 3 (typically used for TSI) |
| SDA3_LV/GPIO196 | I/O | VDDIO_33_S domain (0.8V threshold) | SMBus Data 3 (typically used for TSI) |
| PS2_CLK/SCL4/ GPIO188 | I/O | VDDIO_33_S | SMBus Clock 4 |
| PS2_DAT/SDA4/ GPIO187 | I/O | VDDIO_33_S | SMBus Data 4 |
| THRMTRIP#/ SMBALERT#/ GEVENT2# | I/O | VDDIO_33_S | SMBus Alert#. This signal is used to wake the system or generate an SMI. If not used for SMBALERT#, it can be used for thermal trip or as a GEVENT.<br>Note: If this pin is used for Thermtrip function, the SMBalert function can be mapped to any other available Gevent pin. |

***Notes:***

1. *The SDA1 and SCL1 SMBus1 interface is dedicated for ASF devices or a Synaptics InterTouch Touchpad. This SMBus1 interface will not support a connection to both types of devices simultaneously.*
2. *There are only two SMBus controllers. The SCL1/SDA1 pair is controlled by SMBus controller 1. SCL0/SDA0, SCL2/ SDA2, SCL3/SDA3 and SCL4/SDA4 are multiplexed pins that are all controlled by SMBus controller 0, and only 1 pair of those pins can be active at any time.*

# 4.16 Reset Pins

**Table 23. Reset Pin Descriptions**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| A_RST# | O | VDDIO_33_S | PCI Host Bus Reset. Asserted during transition to S3/S4/S5 to reset all devices in the FCH or connected to it, except the ACPI logic in the FCH. |
| AZ_RST# | O | VDDIO_33_S/ VDDIO_AZ_S | HD Audio interface Reset. |
| DDR3_RST#/ GEVENT7#/ VGA_PD | OD | VDDIO_33_S | System Memory Reset |

**Table 23. Reset Pin Descriptions (Continued)**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| APU_RST# | OD | VDDIO_33_S (0.8V threshold) | APU Reset. Reset signal to the APU. Assertion of APU_RST# causes the APU to re-initialize its internal states. Assertion of APU_RST# can occur based on the following:<br>1) whenever there is a S3 or higher sleep state entry;<br>2) deassertion of FCH PWR_GOOD;<br>3) warm reset issued by a software command such as a write to IO 0xCF9;<br>4) hardware reset due to assertion of pins such as RSMRST# or KB_RST# or SYS_RESET#,<br>5) an internal error (sync flood);<br>6) expiration of the watchdog timer.<br>When the above conditions are no longer true, APU_RST# will deassert after a predetermined period of time (see Figure 21 Reset Timing Requirements on page 95) |
| PCIE_RST# | O | VDDIO_33_S | PCIe Reset. Asserted during transition to S3/S4/S5. Same function as A_RST#. |
| PCIE_RST2#/ GEVENT4# | I/O | VDDIO_33_S | Additional PCIe reset for GPP. |
| PCIRST# | O | VDDIO_33_PCI GP (5V tolerance) | Hardware Reset for PCI slots. Asserted (a) at power on, (b) after the system has transitioned into S3/S4/S5, (c) at warm reset, (d) at software initiated reset |
| ROM_RST#/ GPIO161 | I/O | VDDIO_33_S | ROM Reset. Early version of system reset, the deassertion of which is ahead of other system reset signals such as A_RST#, PCIE_RST#, or PCIRST#. Used for resetting the system BIOS flash ROM. |
| RSMRST# | I | VDDIO_33_S | Resume Reset from motherboard. Assertion of RSMRST# resets all FCH registers to their default values. It also causes all reset signals originating from the FCH (A_RST#, PCIRST#, PCIE_RST#, APU_RST#, AZ_RST#, FC_RST#, GBE_PHY_RST#, ROM_RST# and, DDR3_RST#) to be issued. RSRMT# should be asserted when system power is being applied for the first time. RSMRST# should be deasserted sometime after S5 power is up, and should stay deasserted until system power is removed. |
| SYS_RESET#/ GEVENT19# | I/O | VDDIO_33_S | System Reset. Signal coming from the power button circuit signaling a reset for the system. On receiving the signal, the FCH asserts all reset signals that originate from the FCH (A_RST#, PCIRST#, PCIE_RST#, APU_RST#, AZ_RST#, FC_RST#, ROM_RST#, and DDR3_RST#). it also resets all FCH registers to their default values. |

# 4.17 Clock Interface

**Table 24. Clock Interface Pin Descriptions**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| 25M_X1 | I | 3.3V (VDDXL_33_S) | 25 MHz crystal clock or external reference clock. Clock source for FCH internal core PLLs. |
| 25M_X2 | O | 3.3V (VDDXL_33_S) | 25 MHz crystal clock output. |
| 32K_X1 | I | VDDIO_33_S/ VDDBT_RTC_G | RTC crystal oscillator input 1 (internal RTC). Must be active at all time. |
| 32K_X2 | O | VDDIO_33_S/ VDDBT_RTC_G | RTC crystal oscillator input 2 (internal RTC). Must be active at all time. |
| 14M_25M_48M_OSC | O | VDDIO_33_S | 14MHz / 24MHz / 25MHz / 48MHz /50MHz clock output.<br>Note: This pin outputs a 14.318MHz clock on the first power up if the internal system clock generator mode strap is selected. |
| PCICLK0 | O | 3.3V (5V tolerance) | 33 MHz PCI clock 0 |
| PCICLK1/GPO36 | O | 3.3V (5V tolerance) | 33 MHz PCI clock 1 |
| PCICLK2/GPO37 | O | 3.3V (5V tolerance) | 33 MHz PCI clock 2 |
| PCICLK3/GPO38 | O | 3.3V (5V tolerance) | 33 MHz PCI clock 3 |
| PCICLK4/ 14M_OSC/GPO39 | O | 3.3V | 33 MHz PCI Clock 4 / 14.318 MHz clock output.<br>**For external clock generator mode**: 33 MHz PCI clock output.<br>**For internal clock generator mode:** 14.318 MHz clock output for internal clock generator mode.<br>The function is selected by the pin strap “CLKGEN” (pin LPCCLK1). Refer to Table 32 on page 81. |
| CLKRUN# | I/O | 3.3V (5V tolerance) | Clock running is deasserted by the clock provider to indicate the system is about to shut down the PCI or LPC clock. When it is driven low by other agents, it means the agent is requesting the clock provider not to deactivate the clock. |
| USBCLK/ 14M_25M_48M_OSC | I/O | VDDIO_33_S | 48 MHz clock input used for USB / 14.318 MHz or 25 MHz or 48 MHz output. |

**Table 24. Clock Interface Pin Descriptions (Continued)**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| APU_CLKP | O | VDDAN_11_CLK | Positive phase of 100 MHz APU reference clock. Spread capable. |
| APU_CLKN | O | VDDAN_11_CLK | Negative phase of 100 MHz APU reference clock. Spread capable. |
| GPP_CLK[8:0]P | O | VDDAN_11_CLK | Positive phase of 100 MHz reference clock for PCIe device(s). Spread capable. |
| GPP_CLK[8:0]N | O | VDDAN_11_CLK | Negative phase of 100 MHz reference clock for PCIe device(s). Spread capable. |
| PCIE_RCLKP | I | VDDAN_11_CLK | **For external clock generator mode:** Positive phase of 100-MHz reference clock for the FCH. Spread capable.<br>**For internal clock generator mode:** Not used. Left unconnected.<br>The function is selected by the pin strap “CLKGEN” (pin LPCCLK1). Refer to Table 32 on page 81. |
| PCIE_RCLKN | I | VDDAN_11_CLK | **For external clock generator mode:** Negative phase of 100-MHz reference clock for the FCH. Spread capable.<br>**For internal clock generator mode:** Not used. Left unconnected.<br>The function is selected by the pin strap “CLKGEN” (pin LPCCLK1). Refer to Table 32 on page 81. |
| DISP_CLKP | O | VDDAN_11_CLK | Positive phase of 100-MHz reference clock for APU’s display engine. Not spread capable. |
| DISP_CLKN | O | VDDAN_11_CLK | Negative phase of 100-MHz reference clock for APU’s display engine. Not spread capable. |
| DISP2_CLKP | O | VDDAN_11_CLK | Positive phase of 100-MHz LVDS translator reference clock. Not spread capable. |
| DISP2_CLKN | O | VDDAN_11_CLK | Negative phase of 100-MHz LVDS translator reference clock. Not spread capable. |
| SLT_GFX_CLKP | O | VDDAN_11_CLK | Positive phase of 100 MHz reference clock for external discrete graphics device. Spread capable. |
| SLT_GFX_CLKN | O | VDDAN_11_CLK | Negative phase of 100 MHz reference clock for external discrete graphics device. Spread capable. |
| CLK_REQ0#/ SATA_IS3#/GPIO60 | I/O | VDDIO_33_PCIGP (5V tolerance) | PCIe® Clock Request 0 |

**Table 24. Clock Interface Pin Descriptions (Continued)**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| CLK_REQ1#/ FANOUT4/GPIO61 | I/O | VDDIO_33_PCIGP (5V tolerance) | PCIe Clock Request 1 |
| CLK_REQ2#/ FANIN4/GPIO62 | I/O | VDDIO_33_PCIGP (5V tolerance) | PCIe Clock Request 2 |
| CLK_REQ3#/ SATA_IS1#/GPIO63 | I/O | VDDIO_33_PCIGP (5V tolerance) | PCIe Clock Request 3 |
| CLK_REQ4#/ SATA_IS0#/GPIO64 | I/O | VDDIO_33_PCIGP (5V tolerance) | PCIe Clock Request 4 |
| REQ3#/ CLK_REQ5#/ GPIO42 | I | VDDIO_33_PCIGP (5V tolerance) | PCIe Clock Request 5 |
| LDRQ1#/ CLK_REQ6#/ GPIO49 | I/O | VDDIO_33_PCIGP (5V tolerance) | PCIe Clock Request 6 |
| GNT3#/ CLK_REQ7#/ GPIO46 | I/O | VDDIO_33_PCIGP (5V tolerance) | PCIe Clock Request 7 |
| REQ2#/ CLK_REQ8#/ GPIO41 | I | VDDIO_33_PCIGP (5V tolerance) | PCIe Clock Request 8 |
| CLK_REQG#/ GPIO65/OSCIN/ IDLEEXIT# | I | VDDIO_33_PCIGP (5V tolerance) | Clock Request by PCIe Graphics / 14.318 MHz clock input<br>**For external clock generator mode:** 14.318 MHz OSC clock input pin.<br>**For internal clock generator mode:** Used as GPIO or left unconnected. |
| RTCCLK | I/O | VDDIO_33_S | 32 kHz output for internal RTC. |
| CLK_CALRN | I | VDDAN_11_CLK | Pad connection to an external resistor to VDDAN_11_CLK on the motherboard, for impedance calibration |

# 4.18 ATE/JTAG Interface

**Table 25. ATE/JTAG Interface Pin Descriptions**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| TEST0 | I | VDDIO_33_S | ATE Test 0 |
| TEST1/TMS | I | VDDIO_33_S | ATE Test 1/ JTAG TMS |
| TEST2 | I | VDDIO_33_S | ATE Test 2 |
| USB_OC0#/ GEVENT12#/TRST | I/O | VDDIO_33_S | JTAG Reset |
| USB_OC1#/TDI/GEVENT13# | I/O | VDDIO_33_S | JTAG Data In |
| USB_OC2#/TCK/GEVENT14# | I/O | VDDIO_33_S | JTAG Clock |
| USB_OC3#/AC_PRES/TDO/ GEVENT15# | I/O | VDDIO_33_S | JTAG Data Out |

# 4.19 Integrated Micro-Controller (IMC) Interface

**Table 26. Integrated Micro-Controller Interface Pin Descriptions**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| EC_PWM0/ EC_TIMER0/ GPIO197 | I/O | VDDIO_33_S | IMC PWM 0 |
| EC_PWM1/ EC_TIMER1/ GPIO198 | I/O | VDDIO_33_S | IMC PWM 1 |
| EC_PWM2/ EC_TIMER2/ WOL_EN/ GPIO199 | I/O | VDDIO_33_S | IMC PWM 2 |
| EC_PWM3/ EC_TIMER3/ GPIO200 | I/O | VDDIO_33_S | IMC PWM 3 |

# 4.20 Consumer Infrared Interface

**Table 27. Consumer Infrared Interface Pin Description**

| Pin Name | Type | Voltage | Functional Description |
|---|---|---|---|
| USB_OC4#/IR_RX0/ GEVENT16# | I/O | VDDIO_33_S | Infrared Receive 0. Connection to wideband CIR receiver. |
| IR_RX1/GEVENT20# | I/O | VDDIO_33_S | Infrared Receive 1. Connection to long-range CIR receiver. |
| USB_OC5#/IR_TX0/ GEVENT17# | I/O | VDDIO_33_S | Infrared Transmit 0 |
| USB_OC6#/IR_TX1/ GEVENT6# | I/O | VDDIO_33_S | Infrared Transmit 1 |
| IR_LED#/LLB#/ GPIO184 | I/O | VDDIO_33_S | Infrared LED |
| *The following are the possible configurations for CIR*<br>***No CIR**:*<br>*CIR not used*<br>***CIR RX with TX0**:*<br>*One RX pin used with TX0*<br>***CIR RX with TX1**:*<br>*One RX pin used with TX1*<br>***CIR RX with TX0 and TX1**:*<br>*One RX pin used with TX0 and TX1*<br>*RX can be RX0 or RX1 except when using wideband CIR, in which case both RX pins need to be used.* | | | |

# 4.21 General Purpose I/O and General Event Pins

The GPIO and GEVENT pins of the FCH are multiplexed with other functions. For information on how to configure the GPIO pins for the desired functions, see the *AMD Bolton Fusion Controller Hub Register Reference Guide.*

Table 28 lists all the GPIO and GEVENT pins on the FCH. The Default I/O State column shows the direction and the state of the pin after the core power has become stable (VDDCR > ~0.8V). The integrated resistor column shows the default status of the internal integrated pull-up/pull-down resistor on the pin after the PCI host bus reset (A_RST#) is deasserted. The integrated resistor can be enabled/disabled by the system BIOS after boot up.

**Table 28. General Purpose I/O and General Event Pin Descriptions**

| Pin Name | Type | Level | Default Muxed Function | Default I/O State | Integrated Resistor | Functional Descriptions |
|---|---|---|---|---|---|---|
| **General Events** | | | | | | |
| GA20IN/ GEVENT0# | I | VDDIO_33_PCIGP (5V tolerance) | null | Input, PU | 8.2k PU | General Event 0 |
| KBRST#/ GEVENT1# | I | VDDIO_33_PCIGP (5V tolerance) | KBRST# | Input, PU | 8.2k PU | General Event 1<br>***Note:*** *On G3 to S5 transition, the BIOS will not be able to program this pin as Gevent1#. If the pin is used as Gevent1#, the design should ensure that the pin remains in logical high during the G3 → S5 → S0 transition. BIOS can then program this pin as Gevent1# when it is posting.* |
| THRMTRIP#/ SMBALERT#/ GEVENT2# | I/O | VDDIO_33_S | THRM TRIP# | Input | 10K PU | General Event 2 |
| PME#/ GEVENT3# | I/O | VDDIO_33_S | null | Input, PU | 10K PU | General Event 3 |

**Table 28. General Purpose I/O and General Event Pin Descriptions (Continued)**

| Pin Name | Type | Level | Default Muxed Function | Default I/O State | Integrated Resistor | Functional Descriptions |
|---|---|---|---|---|---|---|
| PCIE_RST2#/ GEVENT4# | I/O | VDDIO_33_S | null | Input, PU | 10k PU | General Event 4 |
| LPC_PD#/ GEVENT5# | I/O | VDDIO_33_S | GEVENT 5# | Input, PU | 10k PU | General Event 5 |
| USB_OC6#/ IR_TX1/ GEVENT6# | I/O | VDDIO_33_S | null | Input, PU | 10k PU | General Event 6 |
| DDR3_RST#/ GEVENT7#/ VGA_PD | I/O | VDDIO_33_S | DDR3_ RST# | Output LOW | 10k PU for GEVENT, OD for DDR3_RST#, push-pull and no integrated PU/PD for VGA_PD | General Event 7 |
| WAKE#/ GEVENT8# | I/O | VDDIO_33_S | null | Input, PU | 10k PU | General Event 8 |
| SPI_HOLD#/ GBE_LED1/ GEVENT9# | I/O | VDDIO_33_S | null | Input, PU | 10k PU | General Event 9 |
| GBE_LED2/ GEVENT10# | I/O | VDDIO_33_S | null | Input, PU | 10k PU | General Event 10 |
| GBE_STAT0/ GEVENT11# | I/O | VDDIO_33_S | null | Input, PU | 10k PU | General Event 11 |
| USB_OC0#/ GEVENT12#/ TRST | I/O | VDDIO_33_S | GEVENT 12# | Input, PU* | 10k PU* | General Event 12<br>***Note:*** **Integrated PU is not supported when the pin is configured for USB over current function.* |
| USB_OC1#/ TDI/ GEVENT13# | I/O | VDDIO_33_S | null | Input, PU* | 10k PU* | General Event 13<br>***Note:*** **Integrated PU is not supported when the pin is configured for USB over current function.* |

**Table 28. General Purpose I/O and General Event Pin Descriptions (Continued)**

| Pin Name | Type | Level | Default Muxed Function | Default I/O State | Integrated Resistor | Functional Descriptions |
|---|---|---|---|---|---|---|
| USB_OC2#/ TCK/ GEVENT14# | I/O | VDDIO_33_S | null | Input, PU* | 10k PU* | General Event 14<br>***Note:*** *******Integrated PU is not supported when the pin is configured for USB over current function.* |
| USB_OC3#/ AC_PRES/ TDO/ GEVENT15# | I/O | VDDIO_33_S | null | Input, PU* | 10k PU* | General Event 15<br>***Note:*** *******Integrated PU is not supported when the pin is configured for USB over current function.* |
| USB_OC4#/ IR_RX0/ GEVENT16# | I/O | VDDIO_33_S | null | Input, PU* | 10k PU* | General Event 16<br>***Note:*** *******Integrated PU is not supported when the pin is configured for USB over current function.* |
| USB_OC5#/ IR_TX0/ GEVENT17# | I/O | VDDIO_33_S | null | Input, PU* | 10k PU* | General Event 17<br>***Note:*** ** Integrated PU is not supported when the pin is configured for USB over current function.* |
| BLINK/ USB_OC7#/ GEVENT18# | I/O | VDDIO_33_S | null | Input, PU* | 10k PU* | General Event 18<br>***Note:*** **Integrated PU is not supported when the pin is configured for USB over current function.* |
| SYS_RESET#/ GEVENT19# | I/O | VDDIO_33_S | null | Input, PU | 10k PU | General Event 19 |
| IR_RX1/ GEVENT20# | I/O | VDDIO_33_S | null | Input, PU | 10k PU | General Event 20 |
| SPI_CS3#/ GBE_STAT1/ GEVENT21# | I/O | VDDIO_33_S | null | Input, PU | 10k PU | General Event 21 |

**Table 28. General Purpose I/O and General Event Pin Descriptions (Continued)**

| Pin Name | Type | Level | Default Muxed Function | Default I/O State | Integrated Resistor | Functional Descriptions |
|---|---|---|---|---|---|---|
| RI#/ GEVENT22# | I/O | VDDIO_33_S | null | Input, PU | 10k PU | General Event 22 |
| LPC_SMI#/ GEVENT23# | I/O | VDDIO_33_S | null | Input, PU | 8.2k PU | General Event 23 |
| S0-domain General Purpose I/O | | | | | | |
| AD[31:0]/ GPIO[31:0] | I/O | VDDIO_33_PCIGP (5V tolerance) | PCI | Output HIGH | - | GPIO [31:0] |
| INTE#/GPIO32 | I/O | VDDIO_33_PCIGP (5V tolerance) | PCI | Input, PU | 8.2k PU | GPIO 32 |
| INTF#/GPIO33 | I/O | VDDIO_33_PCIGP (5V tolerance) | PCI | Input, PU | 8.2k PU | GPIO 33 |
| INTG#/GPIO34 | I/O | VDDIO_33_PCIGP (5V tolerance) | PCI | Input, PU | 8.2k PU | GPIO 34 |
| INTH#/GPIO35 | I/O | VDDIO_33_PCIGP (5V tolerance) | PCI | Input, PU | 8.2k PU | GPIO 35 |
| PCICLK1/ GPO36 | O | VDDIO_33_PCIGP (5V tolerance) | PCICLK | Output 33MHz | - | GPO 36 |
| PCICLK2/ GPO37 | O | VDDIO_33_PCIGP (5V tolerance) | PCICLK | Output 33MHz | - | GPO 37 |
| PCICLK3/ GPO38 | O | VDDIO_33_PCIGP (5V tolerance) | PCICLK | Output 33MHz | - | GPO 38 |
| PCICLK4/ 14M_OSC/ GPO39 | O | VDDIO_33_PCIGP (5V tolerance) | PCICLK | Output 14MHz (internal CLKGEN) or 33MHz (external CLKGEN) | - | GPO 39 |

**Table 28. General Purpose I/O and General Event Pin Descriptions (Continued)**

| Pin Name | Type | Level | Default Muxed Function | Default I/O State | Integrated Resistor | Functional Descriptions |
|---|---|---|---|---|---|---|
| REQ1#/GPIO40 | I | VDDIO_33_PCIGP (5V tolerance) | PCI | Input, PU | 15k PU | GPIO 40 |
| REQ2#/ CLK_REQ8#/ GPIO41 | I | VDDIO_33_PCIGP (5V tolerance) | PCI | Input, PU | 15k PU | GPIO 41 |
| REQ3#/ CLK_REQ5#/ GPIO42 | I | VDDIO_33_PCIGP (5V tolerance) | PCI | Input, PU | 15k PU | GPIO 42 |
| SCL0/GPIO43 | I/O | VDDIO_33_PCIGP (5V tolerance) | null | Input, Tri-State | - | GPIO 43 |
| GNT1#/GPO44 | O | VDDIO_33_PCIGP (5V tolerance) | PCI | Output HIGH | - | GPO 44 |
| GNT2#/ SD_LED/ GPO45 | O | VDDIO_33_PCIGP (5V tolerance) | PCI | Output HIGH | - | GPO 45 |
| GNT3#/ CLK_REQ7#/ GPIO46 | I/O | VDDIO_33_PCIGP (5V tolerance) | null | Input, PU | 8.2k PU | GPIO 46 |
| SDA0/GPIO47 | I/O | VDDIO_33_PCIGP (5V tolerance) | null | Input, Tri-State | - | GPIO 47 |
| SERIRQ/ GPIO48 | I/O | VDDIO_33_PCIGP (5V tolerance) | null | Input, PU | 8.2k PU | GPIO 48 |
| LDRQ1#/ CLK_REQ6#/ GPIO49 | I | VDDIO_33_PCIGP (5V tolerance) | null | Input, PU | 8.2k PU | GPIO 49 |
| SMARTVOLT1/ SATA_IS2#/ GPIO50 | I/O | VDDIO_33_PCIGP (5V tolerance) | null | Input, PU | 8.2k PU | GPIO 50 |
| SMARTVOLT2/ SHUTDOWN#/ GPIO51 | I/O | VDDIO_33_PCIGP (5V tolerance) | null | Input, PU | 8.2k PU | GPIO 51 |

**Table 28. General Purpose I/O and General Event Pin Descriptions (Continued)**

| Pin Name | Type | Level | Default Muxed Function | Default I/O State | Integrated Resistor | Functional Descriptions |
|---|---|---|---|---|---|---|
| FANOUT0/ GPIO52 | I/O | VDDIO_33_ PCIGP (5V tolerance) | null | Input, PU | 8.2k PU | GPIO 52 |
| FANOUT1/ GPIO53 | I/O | VDDIO_33_ PCIGP (5V tolerance) | null | Input, PU | 8.2k PU | GPIO 53 |
| FANOUT2/ GPIO54 | I/O | VDDIO_33_ PCIGP (5V tolerance) | null | Input, PU | 8.2k PU | GPIO 54 |
| SATA_IS4#/ FANOUT3/ GPIO55 | I/O | VDDIO_33_ PCIGP (5V tolerance) | null | Input, PU | 8.2k PU | GPIO 55 |
| FANIN[2:0]/ GPIO[58:56] | I/O | VDDIO_33_ PCIGP (5V tolerance) | null | Input, PU | 8.2k PU | GPIO [58:56] |
| SATA_IS5#/ FANIN3/ GPIO59 | I/O | VDDIO_33_ PCIGP (5V tolerance) | null | Input, PU | 8.2k PU | GPIO 59 |
| CLK_REQ0#/ SATA_IS3#/ GPIO60 | I/O | VDDIO_33_ PCIGP (5V tolerance) | null | Input, PU | 8.2k PU | GPIO60 |
| CLK_REQ1#/ FANOUT4/ GPIO61 | I/O | VDDIO_33_ PCIGP (5V tolerance) | null | Input, PU | 8.2k PU | GPIO 61 |
| CLK_REQ2#/ FANIN4/ GPIO62 | I/O | VDDIO_33_ PCIGP (5V tolerance) | null | Input, PU | 8.2k PU | GPIO 62 |
| CLK_REQ3#/ SATA_IS1#/ GPIO63 | I/O | VDDIO_33_ PCIGP (5V tolerance) | null | Input, PU | 8.2k PU | GPIO 63 |
| CLK_REQ4#/ SATA_IS0#/ GPIO64 | I/O | VDDIO_33_ PCIGP (5V tolerance) | null | Input, PU | 8.2k PU | GPIO 64 |
| CLK_REQG#/ GPIO65/ OSCIN/ IDLEEXIT# | I | VDDIO_33_ PCIGP (5V tolerance) | null | Input, PU | 8.2k PU | GPIO 65 |

**Table 28. General Purpose I/O and General Event Pin Descriptions (Continued)**

| Pin Name | Type | Level | Default Muxed Function | Default I/O State | Integrated Resistor | Functional Descriptions |
|---|---|---|---|---|---|---|
| SPKR/GPIO66 | I/O | VDDIO_33_PCIGP (5V tolerance) | null | Input, Tri-State | - | GPIO 66 |
| SATA_ACT#/ GPIO67 | OD | VDDIO_33_PCIGP (5V tolerance) | null | Input, Tri-State | - | GPIO 67 |
| VGA_HSYNC/ GPO68 | O | VDDIO_33_PCIGP | VGA_HSYNC | Tri-State during reset then output low | - | GPO 68 |
| VGA_VSYNC/ GPO69 | O | VDDIO_33_PCIGP | VGA_VSYNC | Tri-State during reset then output low | - | GPO 69 |
| VGA_DDC_SDA/GPO70 | I/O | VDDIO_33_PCIGP (5V tolerance) | VGA_DDC_SDA | Tri-State | - | GPO70 |
| VGA_DDC_SCL/GPO71 | O | VDDIO_33_PCIGP (5V tolerance) | VGA_DDC_SCL | Tri-State | - | GPO 71 |
| SD_CLK/ SCLK_0/ GPIO73 | I/O | VDDIO_33_PCIGP | null | Input, PU | 8.2k PU | GPIO 73 |
| SD_CMD/ SLOAD_0/ GPIO74 | I/O | VDDIO_33_PCIGP | null | Input, PU | 8.2k PU | GPIO 74 |
| SD_CD#/ GPIO75 | I/O | VDDIO_33_PCIGP | null | Input, PU | 8.2k PU | GPIO 75 |
| SD_WP/ GPIO76 | I/O | VDDIO_33_PCIGP | null | Input, PU | 8.2k PU | GPIO 76 |
| SD_DATA0/ SDATI_0/ GPIO77 | I/O | VDDIO_33_PCIGP | null | Input, PU | 8.2k PU | GPIO 77 |
| SD_DATA1/ SDATO_0/ GPIO78 | I/O | VDDIO_33_PCIGP | null | Input, PU | 8.2k PU | GPIO 78 |
| SD_DATA2/ GPIO79 | I/O | VDDIO_33_PCIGP | null | Input, PU | 8.2k PU | GPIO 79 |

**Table 28. General Purpose I/O and General Event Pin Descriptions (Continued)**

| Pin Name | Type | Level | Default Muxed Function | Default I/O State | Integrated Resistor | Functional Descriptions |
|---|---|---|---|---|---|---|
| SD_DATA3/ GPIO80 | I/O | VDDIO_33_ PCIGP | null | Input, PU | 8.2k PU | GPIO 80 |
| **S5-Domain General Purpose I/O** | | | | | | |
| ROM_RST#/ SPI_WP#/ GPIO161 | I/O | VDDIO_33_S | ROM_RST# | Output LOW | - | GPIO 161 |
| SPI_CLK/ GPIO162 | I/O | VDDIO_33_S | null or SPI (strap depen-dent) | Input, PD | 10k PD | GPIO 162 |
| SPI_DO/ GPIO163 | I/O | VDDIO_33_S | null or SPI (strap depen-dent) | Input, PD | 10k PD | GPIO 163 |
| SPI_DI/ GPIO164 | I/O | VDDIO_33_S | null or SPI (strap depen-dent) | Input, PD | 10k PD | GPIO 164 |
| SPI_CS1#/ GPIO165 | I/O | VDDIO_33_S | null or SPI (strap depen-dent) | Input, PU | 10k PU | GPIO 165 |
| SPI_CS2#/ GBE_STAT2/ GPIO166 | I/O | VDDIO_33_S | null or SPI (strap depen-dent) | Input, PU | 10k PU | GPIO 166 |
| AZ_SDIN[3:0]/ GPIO[170:167] | I/O | VDDIO_33_S /1.5V_S5 | AZ | Input, PD | 50k PD | GPIO [17:167] |
| TEMPIN[2:0]/ GPIO[173:171] | I/O | VDDIO_33_S | null | Input | - | GPIO [173:171] |
| TEMPIN3/ TALERT#/ GPIO174 | I/O | VDDIO_33_S | null | Input | - | GPIO 174 |
| VIN[5:0]/ GPIO[180:175] | I/O | VDDIO_33_S | null | Input | 10k PU/PD (disabled by default) | GPIO [180:175] |

**Table 28. General Purpose I/O and General Event Pin Descriptions (Continued)**

| Pin Name | Type | Level | Default Muxed Function | Default I/O State | Integrated Resistor | Functional Descriptions |
|---|---|---|---|---|---|---|
| VIN6/ GBE_STAT3/ GPIO181 | I/O | VDDIO_33_S | null | Input | - | GPIO 181 |
| VIN7/ GBE_LED3/ GPIO182 | I/O | VDDIO_33_S | null | Input | - | GPIO 182 |
| GBE_LED0/ GPIO183 | I/O | VDDIO_33_S | null | Input | 10k PU | GPIO 183 |
| IR_LED#/ LLB#/GPIO184 | I/O | VDDIO_33_S | null | Input, PU | 10k PU | GPIO 184 |
| USB_FSD0P/ GPIO185 | I/O | VDDIO_33_S | USB | Input, PD | 15k PD | GPIO 185 |
| USB_FSD1P/ GPIO186 | I/O | VDDIO_33_S | USB | Input, PD | 15k PD | GPIO 186 |
| PS2_DAT/ SDA4/GPIO187 | I/O | VDDIO_33_S (5V tolerance) | null | Input, PU | 10k PU | GPIO 187 |
| PS2_CLK/ SCL4/GPIO188 | I/O | VDDIO_33_S (5V tolerance) | null | Input, PU | 10k PU | GPIO 188 |
| PS2KB_DAT/ GPIO189 | I/O | VDDIO_33_S (5V tolerance) | null | Input, PU | 10k PU | GPIO 189 |
| PS2KB_CLK/ GPIO190 | I/O | VDDIO_33_S (5V tolerance) | null | Input, PU | 10k PU | GPIO 190 |
| PS2M_DAT/ GPIO191 | I/O | VDDIO_33_S (5V tolerance) | null | Input, PU | 10k PU | GPIO 191 |
| PS2M_CLK/ GPIO192 | I/O | VDDIO_33_S (5V tolerance) | null | Input, PU | 10k PU | GPIO 192 |
| SCL2/GPIO193 | I/O | VDDIO_33_S (5V tolerance) | null | Input, Tri-State | - | GPIO 193 |
| SDA2/GPIO194 | I/O | VDDIO_33_S (5V tolerance) | null | Input, Tri-State | - | GPIO 194 |
| SCL3_LV/ GPIO195 | I/O | 0.8V threshold, VDDIO_33_S domain | null | Input, Tri-State | - | GPIO 195 |

**Table 28. General Purpose I/O and General Event Pin Descriptions (Continued)**

| Pin Name | Type | Level | Default Muxed Function | Default I/O State | Integrated Resistor | Functional Descriptions |
|---|---|---|---|---|---|---|
| SDA3_LV/ GPIO196 | I/O | 0.8V threshold, VDDIO_33_S domain | null | Input, Tri-State | - | GPIO 196 |
| EC_PWM0/ EC_TIMER0/ GPIO197 | I/O | VDDIO_33_S | null | Input, PU | 10k PU | GPIO 197 |
| EC_PWM1/ EC_TIMER1/ GPIO198 | I/O | VDDIO_33_S | null | Input, PU | 10k PU | GPIO 198 |
| EC_PWM2/ EC_TIMER2/ GPIO199 | I/O | VDDIO_33_S (5V tolerance) | null | Input, PU | 10k PU | GPIO 199 |
| EC_PWM3/ EC_TIMER3/ GPIO200 | I/O | VDDIO_33_S (5V tolerance) | null | Input, PU | 10k PU | GPIO 200 |
| KSI_[7:0]/ GPIO[208:201] | I/O | VDDIO_33_S | null | Input, PU | 10k PU | GPIO [208:201] |
| KSO_[13:0]/ GPIO[222:209] | I/O | VDDIO_33_S | null | Input, PU | 10k PU | GPIO [222:209] |
| KSO_14/XDB0/ GPIO223 | I/O | VDDIO_33_S | null | Input, PU | 10k PU | GPIO 223 |
| KSO_15/XDB1/ GPIO224 | I/O | VDDIO_33_S | null | Input, PU | 10k PU | GPIO 224 |
| KSO_16/XDB2/ GPIO225 | I/O | VDDIO_33_S | null | Input, PU | 10k PU | GPIO 225 |
| KSO_17/XDB3/ GPIO226 | I/O | VDDIO_33_S | null | Input, PU | 10k PU | GPIO 226 |
| SCL1/GPIO227 | I/O | VDDIO_33_S (5V tolerance) | null | Input, Tri-State | - | GPIO 227 |
| SDA1/GPIO228 | I/O | VDDIO_33_S (5V tolerance) | null | Input, Tri-State | - | GPIO 228 |
| ML_VGA_HPD /GPIO229 | I/O | VDDIO_33_S | HPD | Output high | - | GPIO 229 |

# 4.22 Power and Ground Pins

For more information on the power domain, grouping, and power-up sequencing for the power rails, please refer to Section 5.2 “Power Rail Power-up/down Sequence” on page 90.

**Table 29. Power and Ground Pin Descriptions**

| Signal Name | Voltage /GND | GND Reference | Note | Description |
|---|---|---|---|---|
| VDDCR_11_[9:1] | 1.1V | VSS | - | Core power |
| VDDCR_11_S_[2:1] | 1.1V | VSS | - | S5 core power |
| VDDIO_33_S_[8:1] | 3.3V | VSS | - | S5 IO power |
| VDDIO_33_PCIGP[10:1] | 3.3V | VSS | - | IO power |
| VDDIO_AZ_S | 1.5V/ 3.3V | VSS | - | HD Audio Interface IO power |
| VDDXL_33_S | 3.3V | VSSXL | 1 | 25MHz XTAL IO power |
| VDDPL_33_SYS | 3.3V | VSSPLL_ SYS | 2 | System clock generator PLLs analog power |
| VDDPL_11_SYS_S | 1.1V | VSSPL_ SYS | 2 | System clock generator PLLs analog power |
| VDDAN_11_CLK_[8:1] | 1.1V | VSS | 2 | System clock generator analog/output power |
| VDDAN_11_ML_[4:1] | 1.1V | VSS | - | VGA translator input 1.1V analog power |
| VDDPL_33_ML | 3.3V | VSSPL_ SYS | - | VGA translator input 3.3V analog power |
| VDDPL_33_PCIE | 3.3V | VSS | 2 | SCL /PCI Express PLL power |
| VDDAN_11_PCIE_[8:1] | 1.1V | VSS | 2 | SCL / PCI Express analog power |
| VDDPL_33_SATA | 3.3V | VSS | 2 | SATA PHY PLL power |
| VDDAN_11_SATA_[10:1] | 1.1V | VSS | 2 | SATA PHY analog/IO power |

**Table 29. Power and Ground Pin Descriptions (Continued)**

| Signal Name | Voltage /GND | GND Reference | Note | Description |
|---|---|---|---|---|
| VDDBT_RTC_G | 2.5 – 3.6V BAT | VSS | - | RTC/CMOS backup power. Must be present at all time.<br>***Notes:***<br>*1. If the VBAT voltage falls below 1.65V, the CMOS CLR status bit will be set.*<br>*2. To force CMOS clear status bit to be set and still maintain the contents of the CMOS the voltage cannot be lowered past 1.55V.*<br>*3. If the foltage falls below 1.3V, then all of the contents of the RAM and Real Time Clock is invalid.*<br>*4. If the contents of CMOS are not required to be maintained, then the VBAT input of the SOC can be grounded momentarily after the rest of the SOC power rail (S5 and S0) are turned off.* |
| VDDPL_33_USB_S | 3.3V | VSS | 2, 3, 4 | USB PHY PLL analog power |
| VDDAN_33_USB_S_[12:1] | 3.3V | VSS | 2, 3, 4 | USB PHY analog/IO power |
| VDDAN_11_USB_S_[2:1] | 1.1V | VSS | 2, 3, 5 | USB PHY DLL analog power |
| VDDCR_11_USB_S_[2:1] | 1.1V | VSS | 3, 5 | USB PHY core power |
| VDDPL_33_SSUSB_S | 3.3V | VSS | 2, 3, 4 | PLL power for super speed USB |
| VDDAN_11_SSUSB_S_[5:1] | 1.1V | VSS | 2, 3, 5 | Super speed USB analog power |
| VDDCR_11_SSUSB_S_[4:1] | 1.1V | VSS | 3, 5 | Super speed USB core power |
| VDDAN_33_HWM_S | 3.3V | VSSAN_HWM | - | Hardware monitor interface analog/IO power |
| VDDAN_33_DAC | 3.3V | VSSPL_DAC | - | DAC 3.3V analog power |
| VDDPL_33_DAC | 3.3V | VSSPL_DAC | - | DAC 3.3V PLL power |
| VDDPL_11_DAC | 1.1V | VSSPL_DAC | - | DAC 1.1V PLL power |
| LDO_CAP | 1.8V | VSSPL_DAC | - | Internally generated 1.8V supply for the RGB outputs |
| VSS | GND | - | - | Digital ground (plane) |
| VSSXL | GND | - | - | 25MHz XTAL ground |
| VSSPL_SYS | GND | - | - | System clock generator PLLs common ground |

**Table 29. Power and Ground Pin Descriptions (Continued)**

| Signal Name | Voltage /GND | GND Reference | Note | Description |
|---|---|---|---|---|
| VSSAN_HWM | GND | - | - | Hardware monitor interface analog ground |
| VSSIO_DAC | GND | - | - | DAC IO ground |
| VSSAN_DAC | GND | - | - | DAC analog ground |
| VSSANQ_DAC | GND | - | - | DAC analog bias ground |
| VSSPL_DAC | GND | - | - | DAC PLL ground |

***Notes:***

1. *These power rails can be tied to S0-S5 or S0-S3, depending on whether WakeOnLan, USB 3.0 Wakemode is supported. See Table 37.*
2. *These power rails should be filtered.*
3. *These power rails can be tied to S0-S5 or S0-S3 power depending on whether wake from S4/S5 is supported or not.*
4. *VDDPL_33_USB_S and VDDAN_33_USB_S_[12:1] should be sourced from the same voltage regulator and have traces routed close together to minimize voltage droop difference.*
5. *VDDAN_11_USB_S_[2:1] and VDDCR_11_USB_S_[2:1] should be sourced from the same voltage regulator and have traces routed close together to minimize voltage drop difference.*

# 4.23 Miscellaneous Pins

**Table 30. Miscellaneous Pin Descriptions**

| Pin Name | Functional Description |
|---|---|
| NC[x] | No Connect |
| ***Note:*** *GbE is not supported. The greyed out pins below are not used and must be connected or not connected as described.* | |
| GBE_COL | No Connect |
| GBE_CRS | No Connect |
| GBE_MDCK | No Connect |
| GBE_MDIO | No Connect |
| GBE_RXCLK | No Connect |
| GBE_RXD[3:0] | No Connect |
| GBE_RXCTL/RXDV | No Connect |
| GBE_RXERR | No Connect |
| GBE_TXCLK | No Connect |
| GBE_TXD[3:0] | No Connect |

**Table 30. Miscellaneous Pin Descriptions (Continued)**

| | |
|---|---|
| GBE_TXCTL/TXEN | No Connect |
| GBE_PHY_PD | No Connect |
| GBE_PHY_RST# | No Connect |
| GBE_PHY_INTR | Not used. Terminate as per the *AMD Bolton Fusion Controller Hub Motherboard Design Guide*, order# 51206 |
| VDDIO_GBE_S[2:1] | Not used. Terminate as per the *AMD Bolton Fusion Controller Hub Motherboard Design Guide*, order# 51206 |
| VDDIO_33_GBE_S | Not used. Terminate as per the *AMD Bolton Fusion Controller Hub Motherboard Design Guide*, order# 51206 |
| VDDCR_11_GBE_S[2:1] | Not used. Terminate as per the *AMD Bolton Fusion Controller Hub Motherboard Design Guide*, order# 51206 |

# 4.24 Integrated Resistors

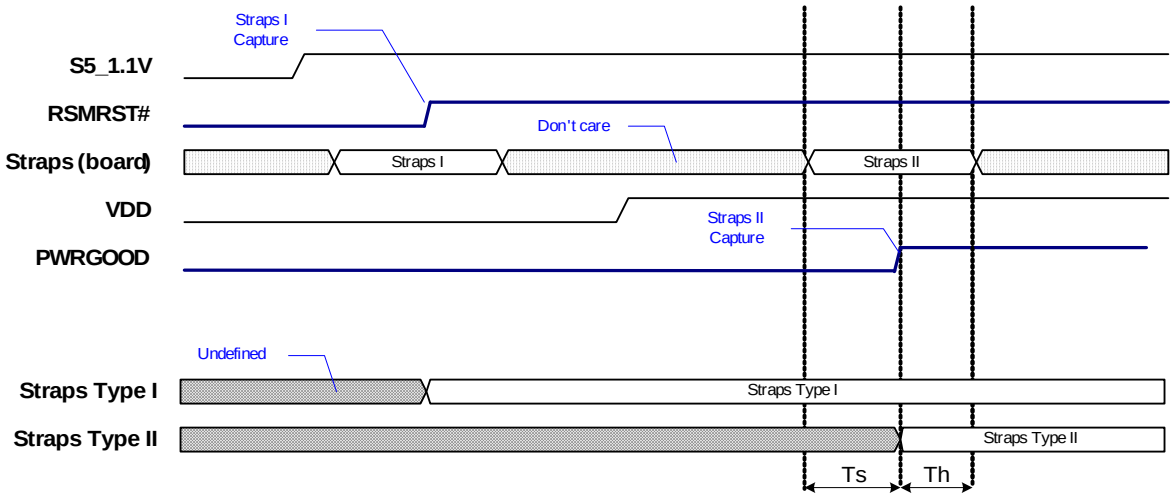
Table 31 shows the pins that have an integrated resistor on their pad and the resistor's nature (pull-up or pull-down) and value. In general, the integrated resistors are enabled by default, but can be changed by programming. The table does NOT include information for any GPIO or GEVENT pins, for which one should refer to Table 28 in Section 4.21 "General Purpose I/O and General Event Pins" on page 67.

**Table 31. Pins with Integrated Resistors (Excluding GPIO/GEVENT Pins)**

| Interface | Pin | Resistor Type/Requirement |
|---|---|---|
| LPC | LAD[3:0] | 10k pull up |
| | LDRQ0# | 10k pull up |
| | CLKRUN# | 7.5k pull up |
| | DEVSEL# | 7.5k pull up |
| | FRAME# | 7.5k pull up |
| | IRDY# | 7.5k pull up |
| | LOCK# | 7.5k pull up |
| | PERR# | 7.5k pull up |
| | REQ[3:0]# | 15k pull up |
| | SERR# | 7.5k pull up |
| | STOP# | 7.5k pull up |
| | TRDY# | 7.5k pull up |
| RTC | RTCCLK | 10k pull up |
| | RSMRST# | 10k pull up (cannot be disabled) |

# 4.25 Strap Information

Two types of straps are captured on the rising edge of RSMRST# and PWR_GOOD—Type I and Type II. Type I straps become valid immediately after capture on the rising edge of RSMRST#. Modules in the S5 power well use this type of straps, which are captured only once when power is first applied to the chip. All other straps (type II) become valid after PWR_GOOD is asserted in order to prevent the strap logic that resides in the standby power well from being driven by un-powered logic. Type II straps are captured every time the system powers up from the S5 state. A transition from S3 to S0 does not trigger capture.




| T | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| Ts | Setup Time for capture | 0 | | ns |
| Th | Hold Time for capture | | 1310.5 | ns |

**Figure 13. Straps Capture Timing**

Straps are also classified into two groups—standard and debug. Standard straps are required for selecting different chip options at power-up. Debug straps are used for debugging purposes only and do not require population for production boards. However, provisions for connecting pull-ups or pull-downs on the debug strap signals should be made if they are not used for normal system operation.

Table 32 and Table 33 show the function of every strap signal in the design. All straps are defined such that in the most likely scenario of operation, they will be set to the recommended (or safest) values by default. The values shown in the Description column are the external board strap values, with 3.3V being a pull up and 0V a pull down.

**Table 32. Standard Straps**

| Ball Name* | Strap Name | Type | Default Value | Description |
|---|---|---|---|---|
| LPCCLK0 | ECEnableStrap | I | - | Enable Integrated Micro-Controller<br>0V – Disable<br>3.3V – Enable<br>This strap has to be enabled to support enhanced hardware monitor features. |
| EC_PWM2 | {ROMTYPE_0 } | I | - | ROMTYPE_0ROM Type<br>0VSPI ROM<br>3.3VLPC ROM |
| RTCCLK | S5 Plus Mode | I | - | Set S5 Plus Mode<br>0V – Enable<br>3.3V – Disable |
| LPCCLK1 | CLKGEN | II | - | Defines clock generator.<br>0V – External clock mode: Use 100 MHz PCIe® clock as reference clock and generate internal clocks only.<br>3.3V – Integrated clock mode: Use 25MHz crystal clock and generate both internal and external clocks. |
| PCICLK1 | BIF_GEN2_COMPLIANCE_Strap | II | - | Set PCIe to Gen II mode.<br>0V – Force PCIe interface at Gen I mode.<br>3.3V – PCIe interfacce is at Gen II mode. |
| PCICLK3 | DefaultStrapMode | II | - | Default Debug Straps<br>0V – Disable Debug Straps.<br>3.3V – Select external Debug Straps (see Table 33). |
| PCICLK4 | CPUClkSel | II | - | APU_CLKP/N and DISP_CLKP/N Clock Selection<br>0V – Required setting for integrated clock mode.<br>3.3V – Reserved.<br>This strap is not used if the strap CLKGEN is configured for external clock generator mode. |

***Note:*** ** For clarity's sake, ball names for strap pins given in this table are truncated to show only the beginning parts. Refer to the pins lists in Appendix A for the complete ball names.*

**Table 33. Debug Straps**

| Ball Name | Strap Name | Type | Default Value | Description |
|---|---|---|---|---|
| AD27 | PciPllByp | II | 3.3V (Internal PU of 15kΩ) | Bypass PCI PLL (used in functional test at tester)<br>0V– Bypass internal PLL clock.<br>Use xSPciReqB_1_ as SPCI33 bypass clock.<br>Use xSPciReqB_2_as A-Link bypass clock. Use xSPciGntB_1_as B-Link bypass clock. Use xSPciGntB_0_ as B-Link266 bypass clock.<br>3.3V – Use internal PLL-generated PLL CLK. |
| AD24 | I2CRomEn | II | 3.3V (Internal PU of 15kΩ) | I2C ROM enable. Load the settings for SCL/PLL/ misc control from I2C ROM.<br>0V – Getting the value from I2C EPROM.<br>I2C EPROM ADDRESS set to all zeroes. Use REQ3# as SDA.<br>Use GNT3# as SCL.<br>3.3V – Disable I2C ROM |
| AD23 | PCI_ROM_ BOOT | II | 3.3V (Internal PU of 15kΩ) | Booting from PCI memory<br>0V – Route ROM fetch to PCI bus on the very first boot. Use ROMTYPE to determine the ROM type on subsequent boots.<br>3.3V – Use ROMTYPE straps to determine the ROM type. |

# Chapter 5 Power Sequence and Timing

This chapter describes the power-on sequences and other timing data for the Bolton-E4 FCH.

## 5.1 Power-up/down Sequence

Figure 14 on page 85 and Figure 15 on page 86 illustrate respectively the power-up/down sequences for ACPI S5-to- S0 -to- S5 and S3-to- S0-to-S3 transitions.

Table 34, Table 35, and Table 36 give the timing values.

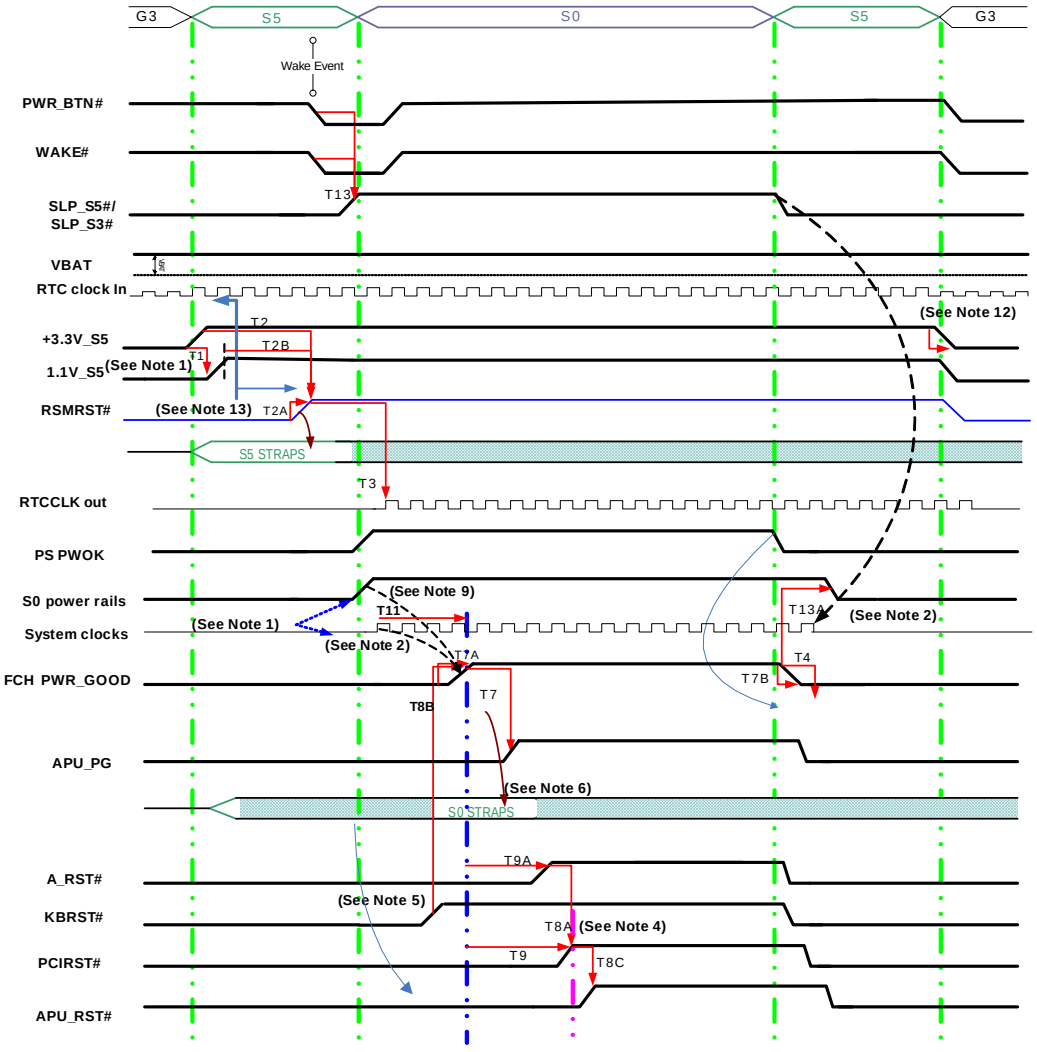



**Figure 14. FCH Power Sequence (S5-to-S0-to-S5)**

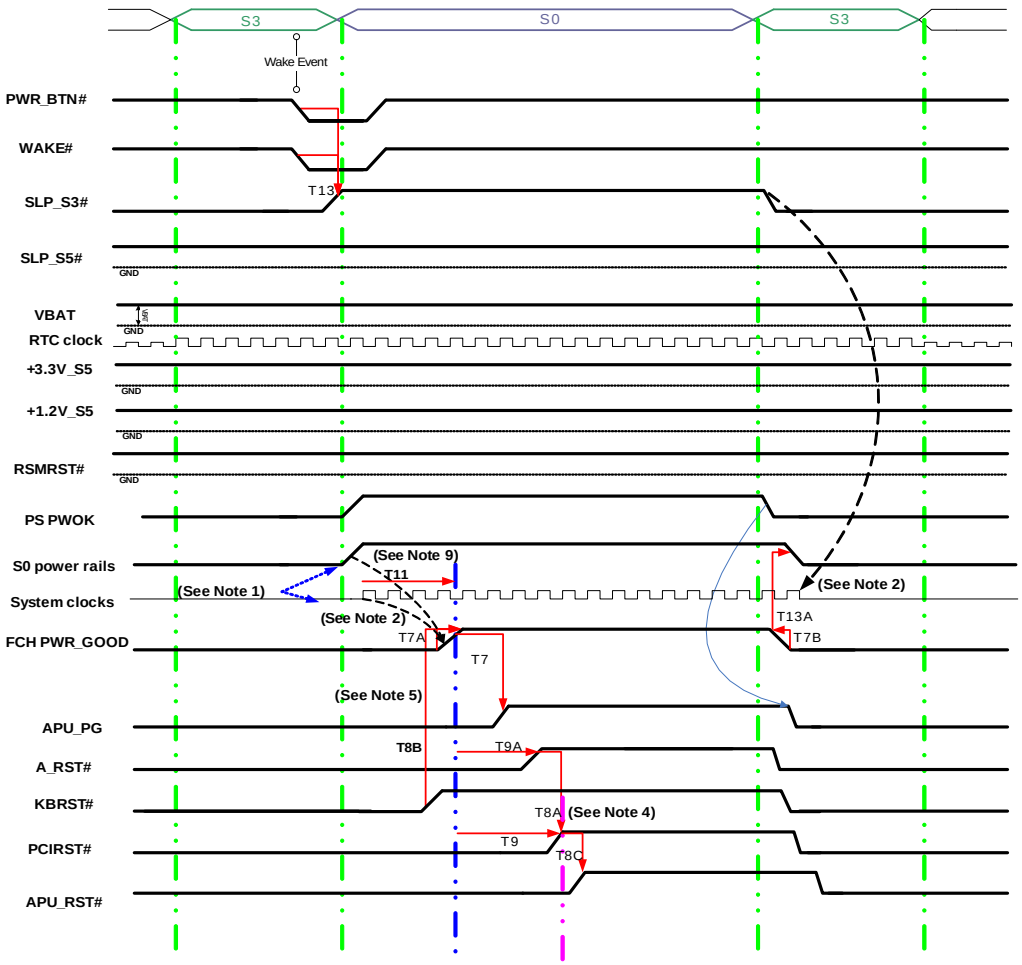



**Figure 15. FCH Power Sequence (S3 to S0 to S3)**

**Table 34. Power Sequence Timing**

| Symbol | Minimum | Maximum | Description |
|---|---|---|---|
| T1 | Note 1 of Section 5.1.1 | | +3.3V_S5 to +1.1V_S5 |
| T2 | 10 ms | – | +3.3V_S5 to resume reset (RSMRST#) |
| T2B | (See Description) | | +1.1V_S5 should ramp up to nominal voltage before resume reset (RSMRST#) is de-asserted. |
| T2A | – | 50 ms | Resume reset (RSMRST#) rise time (10% to 90%). See Note 11 of Section 5.1.1. |
| T3 | 16 ms | – | RSMRST# de-asserted to start of RTCCLK output from the FCH. |

**Table 34. Power Sequence Timing (Continued)**

| Symbol | Minimum | Maximum | Description |
|---|---|---|---|
| T7 | | | See Table 35 and Table 36 on page 88 . |
| T7A | – | 50 ms | FCH PWR_GOOD rise time (10% to 90 %). See Note 3 of Section 5.1.1 “Power up Sequence Timing Notes” on page 88. |
| T7B | – | 1 ms | FCH PWR_GOOD fall time. |
| T8A | 0 ns<br>Note 4 of Section 5.1.1 | 100 ns | A_RST# (PCI host bus reset) to PCIRST#. |
| T8B | – | Note 5 of Section 5.1.1 | KBRST# to FCH PWR_GOOD. |
| T8C | 1.0 ms | 2.3 ms | PCIRST# to APU_RST#. |
| T9 | 101 ms | 113 ms | FCH PWR_GOOD to PCIRST#. |
| T9A | 101 ms | 113 ms | FCH PWR_GOOD to A_RST# (T9-T8A). |
| T13 | – | 15 ns | Wake Event (except PwrButton) to SLP_S3# / SLP_S5# de-assertion.<br>See Note 14 of Section 5.1.1 “Power up Sequence Timing Notes” on page 88. |
| | | 16 ms | Wake Event (PwrButton) to SLP_S3# / SLP_S5# de-assertion. |
| T13A | 80 ns | – | FCH PWR_GOOD must be de-asserted before VDD (PS PWOK) drops more than 5% off the nominal value. See Note 9 of Section 5.1.1 “Power up Sequence Timing Notes” on page 88. |
| T14 | 1 ns | – | FCH PWR_GOOD de-assertion to Resume Reset (RSMRST#) assertion. See Note 10 of Section 5.1.1 “Power up Sequence Timing Notes” on page 88. |
| T15 | 5 s | – | [Not illustrated] VBAT to +3.3V_S5 to +1.1V_S5. Must be greater than 5 seconds to allow start time for the internal RTC. |
| T16A | 40 µs | – | [Not illustrated] APU_STP# assertion to APU_RST# assertion. |
| T16B | 4 µs | – | [Not illustrated] APU_RST# assertion to SLP_S3# assertion. |

**Table 35. FCH PWR_GOOD and System Clock Timing (Internal Clock Mode Only)**

| Symbol | Minimum | Maximum | Description |
|---|---|---|---|
| T7 | 98 ms | 150 ms | FCH PWR_GOOD assertion to APU_PG assertion delay. |
| T11B | – | 39 ms | [Not illustrated] FCH PWR_GOOD to clock out stable. |

**Table 36. FCH PWR_GOOD and System Clock Timing (External Clock Mode Only)**

| Symbol | Min. | Max. | Description |
|---|---|---|---|
| T7 | 77 ms | 108 ms | FCH PWR_GOOD assertion to APU_PWRGD assertion delay when using the FCH APU_PG output. |
| T11 | – | Note 2 of Section 5.1.1 | [Not illustrated] Stable system clocks (25MHz, SRC (PCIe), OSC, 48MHz) to FCH PWR_GOOD when using external clock generator. |

## 5.1.1 Power up Sequence Timing Notes

***Notes:***

1. *Refer to Section 5.2 "Power Rail Power-up/down Sequence" on page 90 for the power rail power-up/down requirements.*
2. *All system clocks should be stable before the assertion of FCH PWR_GOOD. Refer to the external clock specification for the timing $T_{STAB}$, the time it takes for the external clock chip to provide stable clocks after valid power is applied. If the FCH and the external clock chip share power rails, this parameter needs to be taken into account when considering the FCH PWR_GOOD assertion timing. Typical value for $T_{STAB}$ is 1.8 ms. All system clocks should be stopped after SLP_S3# is asserted when transitioning to sleep states; clock generator power-down sequencing should be adjusted accordingly to meet this requirement.*
3. *The FCH will latch the straps after rising edge of FCH PWR_GOOD only once. With de-bouncing of FCH PWR_GOOD, the latching of strap will occur at approximately ~10ms after the rising edge of FCH PWR_GOOD.*
4. *Typical time between A_RST# and PCIRST# is 75 ns. The measurement should be performed at 10% of both signals. Loading on the motherboard may cause the measurement at 90% to be more than the specified value.*
5. *The KBRST# should be de-asserted before FCH PWR_GOOD is de-asserted.*
6. *Type II Standard and Debug straps will be latched after FCH PWR_GOOD is asserted. Type I straps are latched on resume reset rising edge.*
7. *FCH PWR_GOOD Assertion: The FCH PWR_GOOD should be asserted after all S0 power rails have ramped up to 90% of their nominal value. FCH PWR_GOOD de-assertion: The FCH will monitor internally the power down events and protect the internal circuit during the power down event. This includes power down during the S3, S4, and S5 states. During an unexpected power failure or G3 state, the relationship between the +1.1 V (VDDCR) and FCH PWR_GOOD should be maintained to protect the internal logic of the FCH.*
8. *The following figure shows the timing of FCH PWR_GOOD de-asserted to RSMRST# de-asserted during a power down sequence. However, this timing only applies to S0-to-G3 state transition, because G3 state is where both signals are inactivated.*

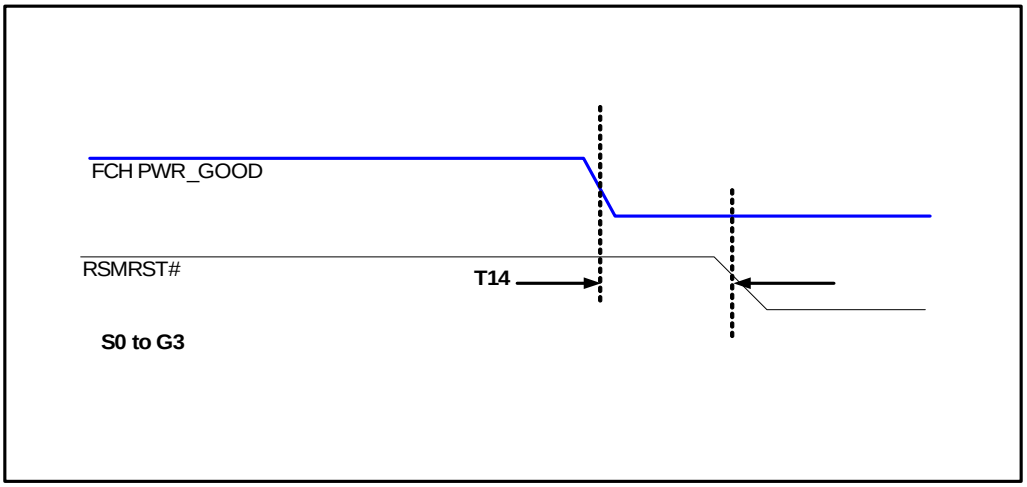



**Figure 16. Timing for FCH PWR_GOOD De-asserted to RSMRST# De-asserted**

9. *When measuring the RSMRST# timing T2A, the loading of the motherboard PCB trace may cause a slow rise time, which should be taken in account. See Figure 17 below.*

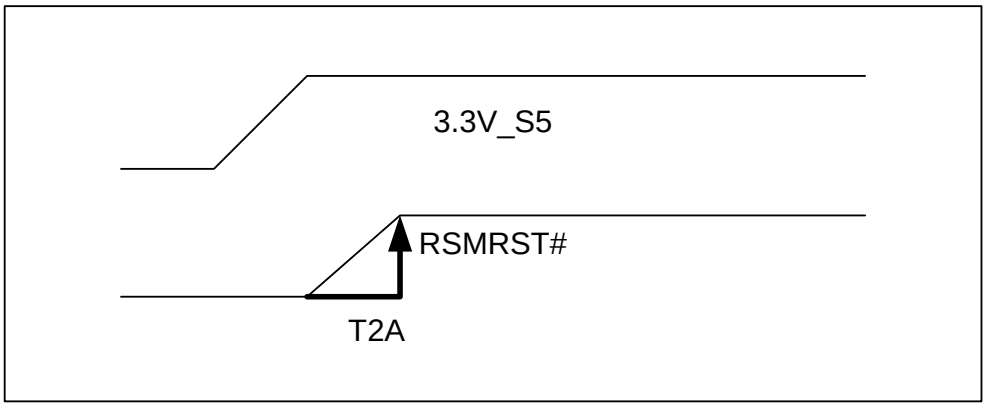



**Figure 17. Measurement for RSMRST# Timing (T2A)**

10. *The ramp down rate of the 3.3V_S5 rail should not be faster than (-) 8 mV/µS. See Figure 18 on page 90 .*

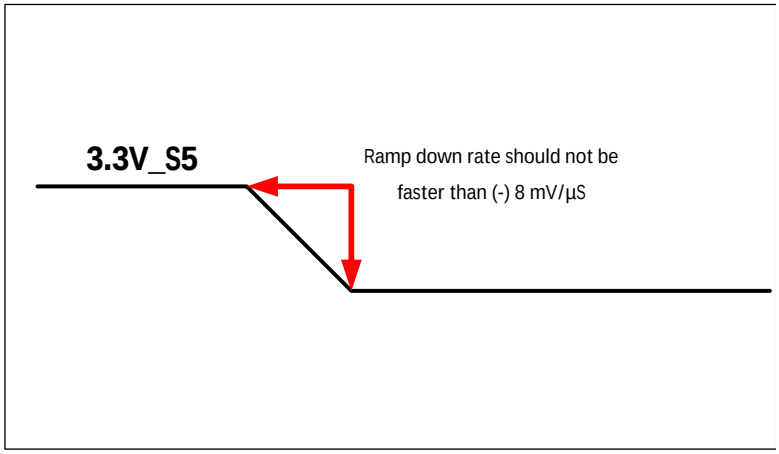



**Figure 18. 3.3V_S5 Power-down Sequence Requirement**

11. *VBAT powers the RTC clock input to the FCH. The RTC clock must be functional before de-assertion of RSMRST#; therefore, the VBAT power ramp up time relative to RSMRST# may need to be controlled. Typical start time is 5 seconds, but the value varies with different crystals.*
12. *The maximum time represents the time FCH's internal logic will take to start driving SLP_S3# / SLP_S5#. The net delay time may be dominated by onboard loading which can be far greater than the silicon intrinsic delay.*

# 5.2 Power Rail Power-up/down Sequence

The Bolton-E4 FCH power rails can be broadly divided into the following two groups:

- + 3.3V and +1.1 V voltage rails that are ON in S0 to S5 states. Rails in this group have the suffix "_S" at the end of their names.
- +3.3V and +1.1V voltage rails that are ON in S0 state but turned OFF in S3 to S5 states. Rails in this group do not have the suffix "_S" at the end of their names.

Table 37 shows how the FCH voltage rails are divided into these two groups. Some of the "_S" domain voltage rails can be connected to "non-_S" domain voltage rails depending on the feature set supported, as explained in the "Note" column.

**Table 37. FCH Voltage Rail Grouping**

| Voltage Rail | +3.3/1.1V_S5 | +3.3/1.1V_S0 | Note |
|---|---|---|---|
| VDDIO_33_S | x | | - |
| VDDAN_33_USB_S | x | | - |
| VDDAN_33_HWM_S | x | | - |
| VDDPL_33_USB_S | x | | -. |

**Table 37. FCH Voltage Rail Grouping**

| Voltage Rail | +3.3/1.1V_S5 | +3.3/1.1V_S0 | Note |
|---|---|---|---|
| VDDPL_33_SSUSB_S | x | x | VDDPL_33_SSUSB_S should be tied to +3.3V_S5 rail if USB 3.0 Wake is supported; otherwise, it can be tied to +3.3V_S0 rail. If USB 3.0 is not used at all, it can be tied to GND. |
| VDDXL_33_S | x | x | VDDXL_33_S should be tied to +3.3V_S5 rail if USB 3.0 Wake is supported; otherwise, it can be tied to +3.3V_S0 rail. |
| VDDIO_33_PCIGP | | x | - |
| VDDPL_33_SYS | | x | - |
| VDDPL_33_PCIE | | x | - |
| VDDPL_33_SATA | | x | - |
| VDDPL_33_DAC | | x | VDDPL_33_DAC, VDDPL_33_ML, VDDAN_33_DAC should be tied to +3.3V_S0 rail if the VGA translator function is supported. If the VGA translator is not used at all, these power rails can be tied to GND. |
| VDDPL_33_ML | | x | |
| VDDAN_33_DAC | | x | |
| VDDCR_11_S | x | | - |
| VDDCR_11_USB_S | x | | - |
| VDDPL_11_SYS_S | x | x | VDDPL_11_SYS_S should be tied to +1.1V_S5 rail if USB 3.0 Wake is supported; otherwise, it can be tied to +1.1V_S0 rail. |
| VDDCR_11_SSUSB_S | x | x | VDDCR_11_SSUSB_S should be tied to +1.1V_S5 rail if USB 3.0 Wake is supported; otherwise, it can be tied to +1.1V_S0 rail. If USB 3.0 is not used at all, it can be tied to GND. |
| VDDCR_11 | | x | - |
| VDDAN_11_SATA | | x | - |
| VDDAN_11_PCIE | | x | - |
| VDDAN_11_CLK | | x | - |

**Table 37. FCH Voltage Rail Grouping**

| Voltage Rail | +3.3/1.1V_S5 | +3.3/1.1V_S0 | Note |
|---|---|---|---|
| VDDAN_11_ML | | x | Tie to GND if VGA interface is not enabled. |
| VDDAN_11_SSUSB_S | x | x | VDDAN_11_SSUSB_S should be tied to +1.1V_S5 rail if USB 3.0 Wake is supported; otherwise, it can be tied to +1.1V_S0 rail. If USB 3.0 is not used at all, it can be tied to GND. |
| VDDPL_11_DAC | | x | Tie to GND if VGA interface is not enabled. |
| VDDIO_AZ_S | x | x | Though the rail's voltage is 3.3V/1.5V, it follows the same power-rail power-up/down requirements for the 3.3V/1.1V rails as described in this section. It is thus classified here as belonging to either the 3.3V/1.1V_S5 or the 3.3V/1.1V_S0 rail group with respect to the power-up/down requirements, according to the following conditions:<br>**Wake on Ring supported:** Tie to +3.3/ 1.5V_S5 rail, and treat like a 3.3/1.1V_S5 rail.<br>**Wake on Ring not supported:** Tie to +3.3/ 1.5V_S0 rail, and treat like a 3.3/1.1V S0 rail. |

Within each of the +3.3 /1.1 V_S5 or +3.3 /1.1 V_S0 power rail groups, rails of the same voltage (3.3 V or 1.1 V) should be powered up at the same time. However, there are no required sequencing relationships between the 3.3-V rails and the 1.1-V rails.

Although there are no power rail sequencing requirements between any specific power rail groups (except for VBAT—see explanations below), customers can use the power rail power-up sequence shown in Figure 19 and Table 38 below as a reference. All of the AMD Bolton-E4 reference platforms are designed to follow that reference power-up sequence.

For power-down sequence, power rails on reference platforms should either be powered-down at the same time or in the reverse order of the power-up sequence shown below.

The only mandatory requirement for power rail sequencing is that VBAT (VDDBT_RTC_G) must ramp at least 5 seconds before the S5 rails to allow start time for the external RTC crystal.

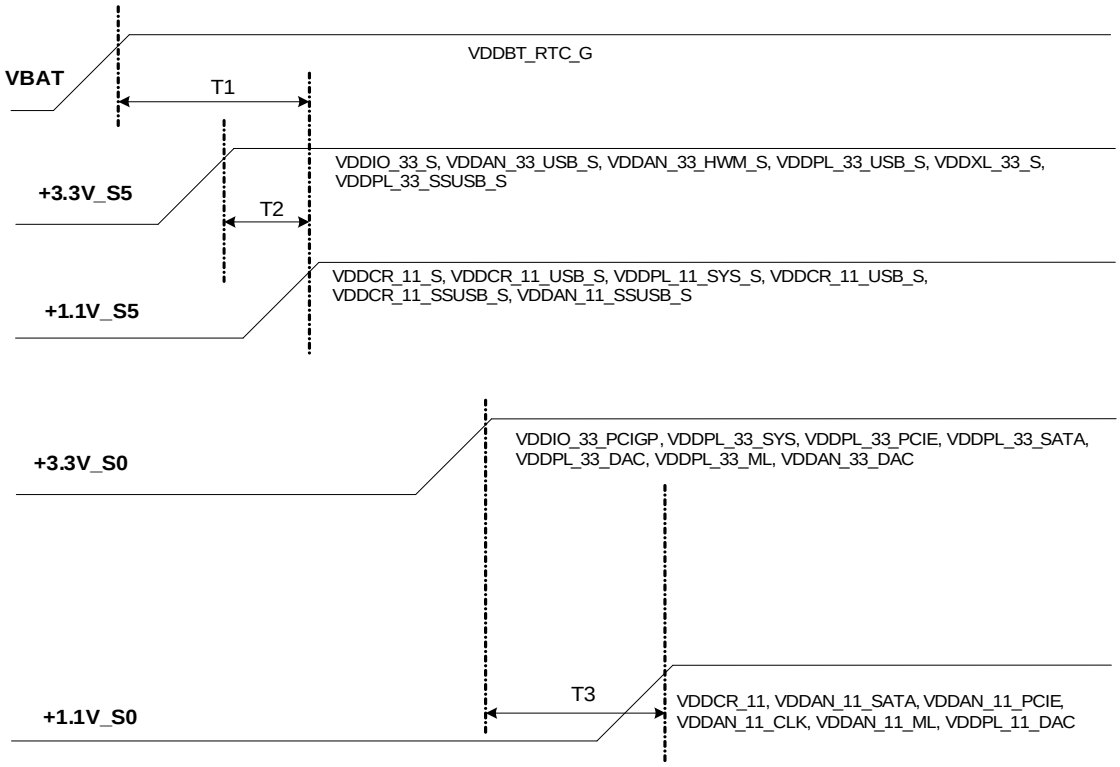



**Figure 19. Power Rail Power-up Sequence Requirements**

**Table 38. Power Rail Power-up Sequence Requirements**

| Symbol | Parameter | Voltage Difference during Ramping | |
|---|---|---|---|
| | | Minimum (V) | Maximum (V) |
| T1 | VBAT to the S5 rails | VDDBT_RTC_G must ramp at least 5 seconds before the S5 rails. | No restrictions |
| T2 | +3.3V_S5 rails ramp high relative to +1.1V_S5 rails | 0 | No restrictions* |
| T3 | +3.3V_S0 rails ramp high relative to +1.1V_S0 rails | 0 | No restrictions* |
| **Note:* *Power rails from the same group are assumed to be generated from the same regulator; however, they can be generated from different regulators as long as they come up at the same time.* | | | |

# 5.3 Reset Timings

The FCH controls the system reset signal timings, which are provided in this section. ROMRST# timing is shown with respect to RSMRST# and A_RST# signals in Figure 20 (a) and (b). ROM_RST can be generated on the system board using either the RSMRST# or A_RST# signal depending on the platform configurations, and Table 40 on page 95, indicates the timing figure and label that apply in each situation.

**Table 39. ROM Reset Timing Figure for Various Platform Configurations**

| IMC Enabled | ROM Reset Timing Figure |
|---|---|
| Y | Figure 20 (a) |
| N | Figure 20 (b) |

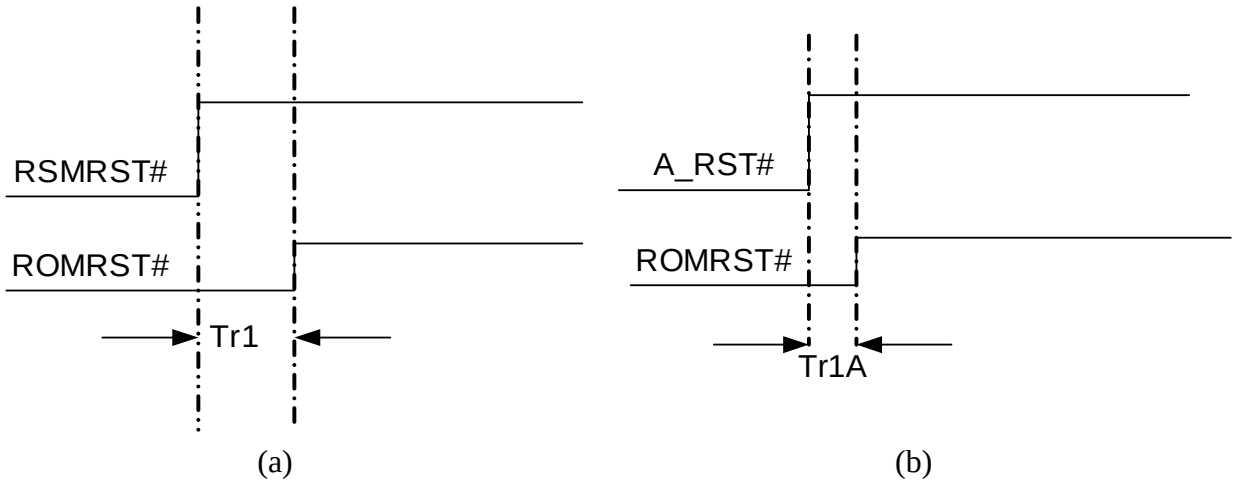



**Figure 20. ROM Reset Timing**

Figure 21 on page 95 shows the timing of APU_RST#, APU_PG, A_RST#, and PCI_RST# with respect to the SYS_RST# signal when SYS_RST# is used to force a system reset. SYS_RST# and RSMRST# signals are input to the FCH and are generated on the system board.

Table 40 on page 95 shows the values of all the timing labels.

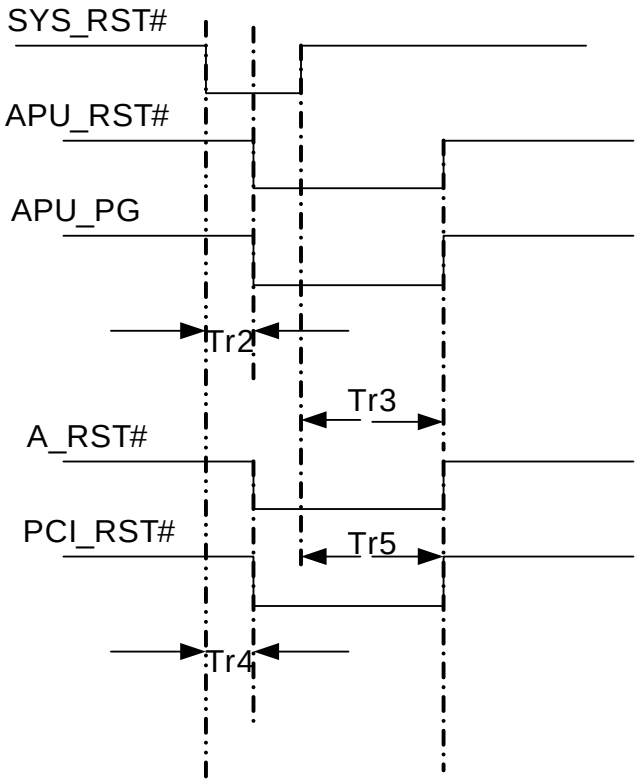


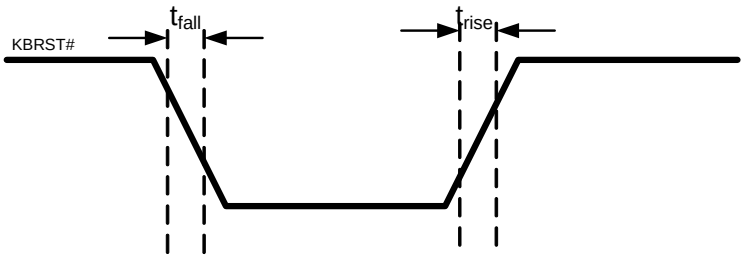

**Figure 21. Reset Timing Requirements**

**Table 40. Reset Timing Requirements**

| Symbol | Parameter | Min | Typical | Max |
|---|---|---|---|---|
| Tr1 | RSMRST# to ROMRST#<br>(ROMRST# is generated from RSMRST#.) | 48 ms | - | 58 ms |
| Tr1A | A_RST# to ROMRST#<br>(ROMRST# is generated from A_RST#) | - | - | 100 ns |
| Tr2 | SYS_RESET# assertion to APU_RST# assertion | - | 8 ms | - |
| | SYS_RESET# assertion to APU_PG de-assertion | - | 8 ms | - |
| Tr3 | SYS_RESET# de-assertion to A-RST# de-assertion | - | 230 ms | - |
| Tr4 | SYS_RESET# assertion to A_RST# assertion | - | 8.05 ms | - |
| | SYS_RESET# assertion to PCI_RST# assertion | - | 8.1 ms | - |
| Tr5 | SYS_RESET# de-assertion to PCI_RST# de-assertion | - | 231 ms | |

### 5.3.1 KBRST# Timing Requirements

KBRST# rise and fall time requirements are shown in Figure 22 .




$t_{rise}$ = 500ns max (10 - 90 %)
$t_{fall}$ = 500ns max (10 - 90 %)

**Figure 22. Timing Requirements for KBRST#**

# 5.4 Power Button Timing

Figure 23 illustrates various timing values related to the assertion and de-assertion of the power button.

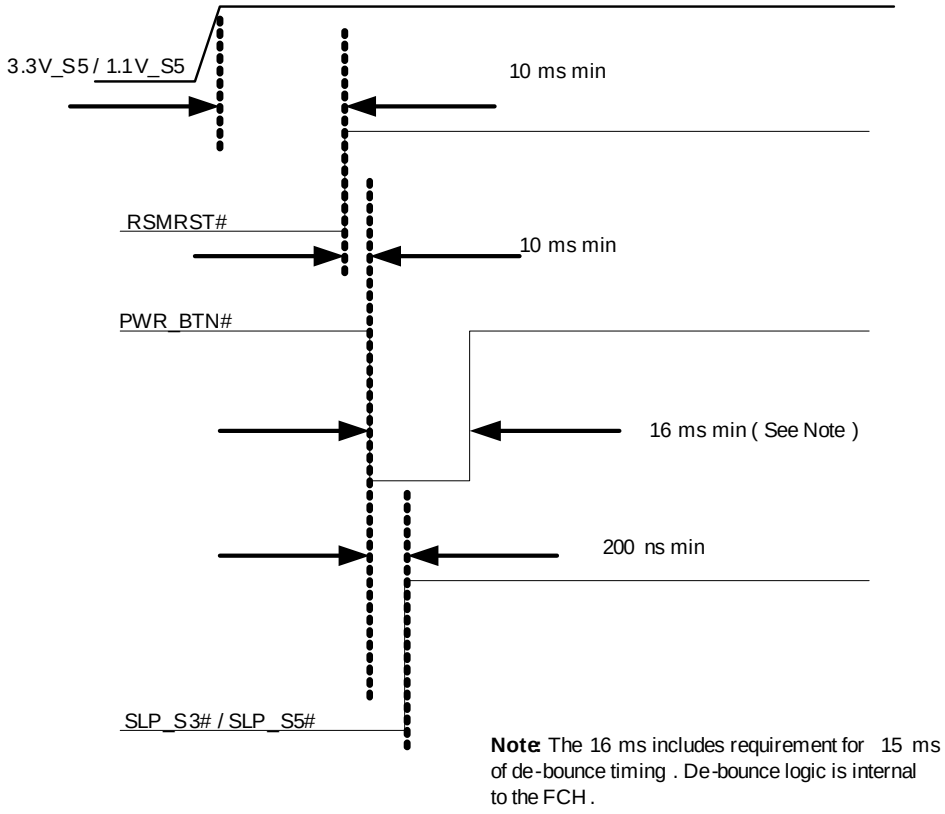



**Figure 23. Power Button Timing**

# Chapter 6 Electrical Characteristics

***Note:*** *Values quoted in this section are preliminary and require further verification.*

## 6.1 Power Rail Specifications

### 6.1.1 Absolute Ratings

To prevent damage to the ASIC, the voltage applied to each power rail should not exceed 10% of its nominal voltage, nor should it fall below -0.5V with respect to VSS.

### 6.1.2 Operating Range

For proper operation of the ASIC, voltages of all power rails should stay within +/- 5% of their nominal values. Voltages, measured at the ball of the ASIC, must stay within the range of tolerance in spite of any DC transients or AC noises of frequencies less than 2 MHz.

## 6.2 DC Characteristics

**Table 41. DC Characteristics of the GPIO Pins**

| Symbol | Parameter | Minimum | Maximum | Unit | Condition |
|---|---|---|---|---|---|
| VDDQ | I/O power | 3.0 | 3.46 | V | |
| VIL | Input Low Voltage | - | 1.5 | V | |
| VIH | Input High Voltage | 1.5 | - | V | |
| VOL | Output Low Voltage | - | 0.4 | V | IOL = 8.0 mA (Note 1) |
| VOH | Output High Voltage | 2.4 | - | V | IOH = 8.0 mA (Note 1, 2) |
| ILI | Input Leakage Current | - | 10 | µA | Only applicable when the integrated resistors are not enabled. |
| CIN | Input Capacitance | - | 10 | pF | Only applicable when the integrated resistors are not enabled. |

***Notes:***

1. *For the GEVENT9# and GEVENT10# pads, the IOL and IOH are programmable to values between 4 and 8 mA.*
2. *VOH specifications are not applicable to I/OD or OD signals.*

**Table 42. DC Characteristics of the PCI Interface**

| Symbol | Parameter | Minimum | Maximum | Unit | Condition |
|---|---|---|---|---|---|
| VDDQ | I/O power | 3.0 | 3.46 | V | |
| VIL | Input Low Threshold | - | 0.3VDD | V | |
| VIH | Input High Threshold | 0.3VDD | - | V | |
| VOL | Output Low Voltage | - | 0.4 | V | IOL = 4.0 mA to 12 .0 mA |
| VOH* | Output High Voltage | 2.4 | - | V | IOH = -4.0 mA to 12 mA |
| ILI | Input Leakage Current | - | 10 | µA | Only applicable when the integrated resistors are not enabled. |
| CIN | Input Capacitance | - | 10 | pF | Only applicable when the integrated resistors are not enabled. |
| ***Note:*** **VOH specifications are not applicable to I/OD or OD signals.* | | | | | |

**Table 43. DC Characteristics of the APU Interface**

| Symbol | Parameter | Minimum | Maximum | Unit | Condition |
|---|---|---|---|---|---|
| **DMA_ACTIVE#** | | | | | |
| VCPU_IO | CPU IO Voltage | - | - | V | OD signal |
| VOL | Output Low Voltage | - | 0.4 | V | IOL = 8.0 mA |
| **APU_PG, APU_RST#** | | | | | |
| VDDQ | I/O power | | | V | OD signal |
| VOL | Output Low Voltage | - | 0.4 | V | IOL = 8.0 mA |

**Table 44. DC Characteristics of RSMRST#**

| Symbol | Parameter | Minimum | Maximum | Unit | Condition |
|---|---|---|---|---|---|
| 3.3V_S5 | Core standby power | 3.0 | 3.46 | V | |
| VIL | Input Low Voltage | - | 1.5 | V | |
| VIH | Input High Voltage | 1.5 | - | V | |
| ILI | Input Leakage Current | - | 10 | µA | |
| CIN | Input Capacitance | - | 10 | pf | |

**Table 45. DC Characteristics of PWR_GOOD**

| Symbol | Parameter | Minimum | Maximum | Unit | Condition |
|---|---|---|---|---|---|
| VDDQ | I/O power | 3.0 | 3.46 | V | |
| VIL | Input Low Voltage | - | 1.5 | V | |
| VIH | Input High Voltage | 1.5 | - | V | |
| ILI | Input Leakage Current | - | 10 | µA | |
| CIN | Input Capacitance | - | 10 | pf | |

**Table 46. DC Characteristics of the LPC Interface**

| Symbol | Parameter | Minimum | Maximum | Unit | Condition |
|---|---|---|---|---|---|
| VDDQ | I/O power | 3.0 | 3.46 | V | |
| VIL | Input Low Threshold | - | 0.3VDD | V | |
| VIH | Input High Threshold | 0.3VDD | - | V | |
| VOL | Output Low Voltage | - | 0.4 | V | IOL = 4.0 mA to 12 .0 mA |
| VOH | Output High Voltage | 2.4 | - | V | IOH = -4.0 mA to 12 mA |
| ILI | Input Leakage Current | - | 10 | µA | Only applicable when the integrated resistors are not enabled. Not applicable to LDRQ[1:0]#. |
| CIN | Input Capacitance | - | 10 | pF | Only applicable when the integrated resistors are not enabled. Not applicable to LDRQ[1:0]#. |

# 6.3 RTC Battery Current Consumption

The RTC battery current consumption is estimated as follows:

**Table 47. RTC Battery Current Consumption (Preliminary Estimates)**

| Power State | RTC Battery Current | |
|---|---|---|
| | Typical | Maximum |
| G3 (Off) | < 3 µA | < 4.5 µA |
| S0-S5 | < 0.2 µA | - |

The RTC battery life is calculated using the rated capacity of the battery and the typical current numbers. The typical batteries used for the RTC are normally rated for 170 mAh, and the worst case current consumption for the FCH is 4.5 µA, according to Table 47 on page 101. Thus, the minimum life of the battery can be calculated as follows:

170,000 µAh / 4.5 µA = 38,000 h ≅ 4.3 years

# 6.4 States of Power Rails during ACPI S3 to S5 States

Please refer to Section 5.2 “Power Rail Power-up/down Sequence” on page 90.

# 6.5 System Clock Specifications

## 6.5.1 System Clock Descriptions

**Table 48. System Clock Input Source Descriptions**

| Clock Domain | Frequency | Source | Usage |
|---|---|---|---|
| 25M_X1, 25M_X2 | 25 MHz | 25-MHz Crystal | Master reference clock for the FCH for internal clock mode |
| PCIE_RCLKP, PCIE_RCLKN | 100 MHz | Main clock generator | Reference clock for the FCH for external clock mode. |
| SATA_X1, SATA_X2 | 25 MHz | 25-MHz Crystal | For SATA Controllers |
| 32K_X1, 32K_X2 | 32 KHz | 32-KHz Crystal | For RTC |
| USBCLK | 48 MHz | 48-MHz OSC or internal USB 48-MHz PLL | For USB Controllers and HD Audio |

## 6.5.2 System Clock Input Frequency Specifications

**Table 49. System Clock Input Frequency Specifications**

| Clock | Frequency |
|---|---|
| 25M_X1, 25M_X2 | 25.000 MHz ± 50 ppm |
| USBCLK | 48.000 MHz ± 100 ppm |
| SATA_X1, SATA_X2 | 25.000 MHz ± 50 ppm |

## 6.5.3 AC Specifications

### 6.5.3.1 System Clock Output AC Specifications

**GPP_CLKP/N, SLT_GFX_CLKP/N, and DISP2_CLKP/N**: These clocks are compliant with the PCI Express® Specification 2.0. Please refer to the *PCI Express CEM 2.0 Specification* for the clocks' AC and DC specifications for the clocks.

**Table 50. DISP_CLKP/N AC Specifications: (Non-Spread Clock)**

| Symbol | Parameter | 100 MHz Input | | Unit |
|---|---|---|---|---|
| | | Minimum | Maximum | |
| $V_{IH}$ | Differential Input High Voltage | +150 | - | mV |
| $V_{IL}$ | Differential Input Low Voltage | - | –150 | mV |
| $V_{CROSS}$ | Absolute crossing point voltage | +250 | +550 | mV |
| $T_{PERIOD\ AVG}$ | Average Clock Period Accuracy | –300 | +300 | ppm |
| $T_{CCJITTER}$ | Cycle to Cycle Jitter | - | 150 | ps |
| Tdc | Reference Duty Cycle | 40 | 60 | % |
| Rising Edge Rate | Rising Edge Rate | 0.6 | 4.0 | V/ns |
| Falling Edge Rate | Falling Edge Rate | –4.0 | –0.6 | V/ns |

**Table 51. APU_CLKP/N AC Specifications**

| Symbol | Parameter | 200/100 MHz Output | | Unit |
|---|---|---|---|---|
| | | Minimum | Maximum | |
| $V_{OH}$ | Differential Output High Voltage | +150 | - | mV |
| $V_{OL}$ | Differential Output Low Voltage | - | –150 | mV |
| $V_{CROSS}$ | Absolute crossing point voltage | +250 | +550 | mV |
| $V_{CROSS\ DELTA}$ | Variation of VCROSS over all rising clock edges | - | +140 | mV |
| $T_{PERIOD\ AVG}$ | Average Clock Period Accuracy | –300 | +300 | ppm |
| Rising Edge Rate | Rising Edge Rate | 0.6 | 4.0 | V/ns |
| Falling Edge Rate | Falling Edge Rate | –4.0 | –0.6 | V/ns |
| $T_{CCJITTER}$ | Cycle to Cycle jitter | - | 150 | ps |
| Duty Cycle | Duty Cycle | 40 | 60 | % |

**Table 52. 14MHz/25MHz/48MHz Auxiliary Clock AC Specifications**

| Symbol | Parameter | Value | | | Unit | Note |
|---|---|---|---|---|---|---|
| | | Minimum | Typical | Maximum | | |
| 14M | 14 MHz Clock Frequency | 14.2146 | 14.31818 | 14.8920 | MHz | - |
| 24M | 24 MHz Clock Frequency | TBA | 24 | TBA | MHz | |
| 25M | 25 MHz Clock Frequency | 24.875 | 25 | 25.125 | MHz | - |
| 48M | 48 MHz Clock Frequency | 47.55 | 48 | 48.47 | MHz | - |
| 50M | 50 MHz Clock Frequency | TBA | 50 | TBA | MHz | - |
| VOL | Output low voltage | - | - | 0.4 | V | IOL=4.0 mA when highdrive = 0<br>IOL = 8.0 mA when highdrive = 1 |
| VOH | Output high voltage | 2.4 | - | - | V | IOH = -4.0 mA when highdrive = 0<br>IOH = 8.0 mA when highdrive = 1 |
| Rising Slew Rate | Rising Slew Rate | 1.0 | - | 4.0 | V/ns | 50pf load |
| Falling Slew Rate | Falling Slew Rate | 1.0 | - | 4.0 | V/ns | 50pf load |
| Tdc | Duty Cycle | 40 | - | 60 | % | |

***Note:*** *In integrated clock mode this pin will output 14.318 MHz clock. The output frequency varies from cycle to cycle, with an average frequency of 14.318MHz. This clock is available for customers to use on the system board if it meets the requirements of target device.* ***AMD has not validated this clock on any specific applications.*** *Since this clock is averaged at 14.318 MHz, AMD does not recommend this clock to be used for devices that use an Internal PLL. The output will generate 12 MHz on power up until after the FCH PWR_GOOD is asserted. After the FCH PWR_GOOD assertion, the clock output will be 14MHz. After power up, this pin can be configured to output a 24-MHz, 25-MHz, 48-MHz, or 50-MHz clock.*

**Table 53. PCI Clock AC Specifications**

| Symbol | Parameter | Value | | | Unit | Note |
|---|---|---|---|---|---|---|
| | | Minimum | Typical | Maximum | | |
| Tperiod | Clock period | 30 | - | 33.3 | MHz | |
| VOL | Output low voltage | - | - | 0.4 | V | IOL = 4.0 mA |
| VOH | Output high voltage | 2.4 | - | - | V | IOH = –4.0 mA |
| Rising Slew Rate | Rising Slew Rate | 1.0 | - | 4.0 | V/ns | 50pf load |
| Falling Slew Rate | Falling Slew Rate | 1.0 | - | 4.0 | V/ns | 50pf load |

### 6.5.3.2 AC Specification of External Reference Clock for 25M_X1

***Note:*** *The specification below applies at the input of the 25M_X1 pad only, it does not apply to the output of the external clock chip.*

**Table 54. AC Specification of External Reference Clock for 25M_X1**

| Symbol | Parameter | Minimum | Typical | Maximum | Unit | Notes |
|---|---|---|---|---|---|---|
| VIH | Input High Level | 2.97 | -- | -- | V | 1 |
| Vin Max | Maximum Voltage IN | | -- | 3.3 | V | 2 |
| VIL | Input Low Voltage | 0 | -- | 0.33 | V | |
| TIP | 25MHZ Clock Period | -- | 40 | -- | ns | 3 |
| FTOL | Frequency Tolerance | –25 | -- | 25 | ppm | |
| DC | Duty Cycle | 45 | 50 | 55 | % | |
| TIR | 25MHz Slew Rate (Rise) | 1 | -- | -- | V/ns | 4, 5 |
| TIF | 25MHz Slew Rate (Fall) | 1 | -- | -- | V/ns | 4, 5 |
| TSHORT | Short Term Peak-to-Peak Jitter | -- | -- | 200 | ps | 3 |
| TIJLT | 25MHz Long Term Jitter Requirement (10 µs after scope trigger) | -- | -- | 250 | ps | |

**Table 54. AC Specification of External Reference Clock for 25M_X1**

***Notes:***

1. *Minimum voltage required to guarantee a High level detection.*
2. *25M_X1 input should not exceed Vin Max during normal operation.*
3. *Time intervals measured at 50% threshold point.*
4. *Rise Time and Fall Time measurements should be measured at 10%-90% thresholds.*
5. *For acceptable duty-cycle performance, TIR and TIF should be kept to within 10% of each other.*

### 6.5.3.3 SPI AC Specifications

Figure 24 and Figure 25 show the timing requirements for the SPI ROM controller setup.

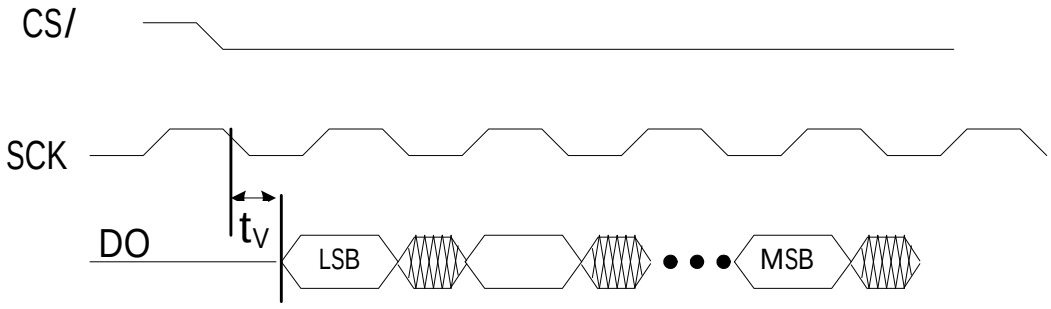



**Figure 24. SPI Output Timing Diagram**

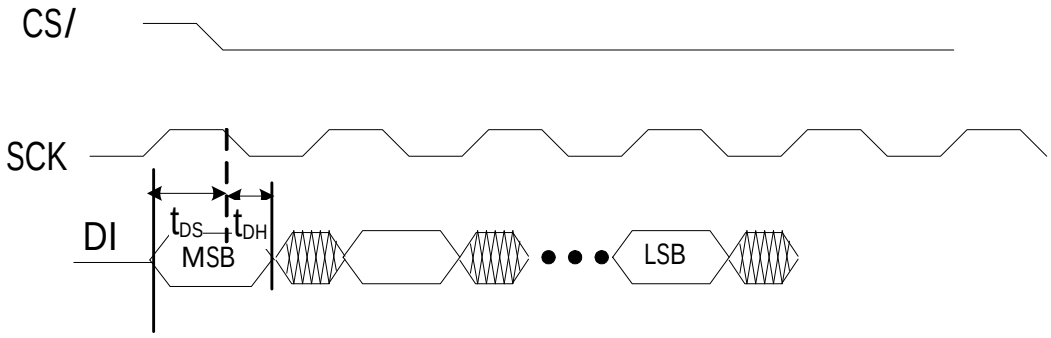



**Figure 25. SPI Iutput Timing Diagram**

**Table 55. SPI Timing Parameters**

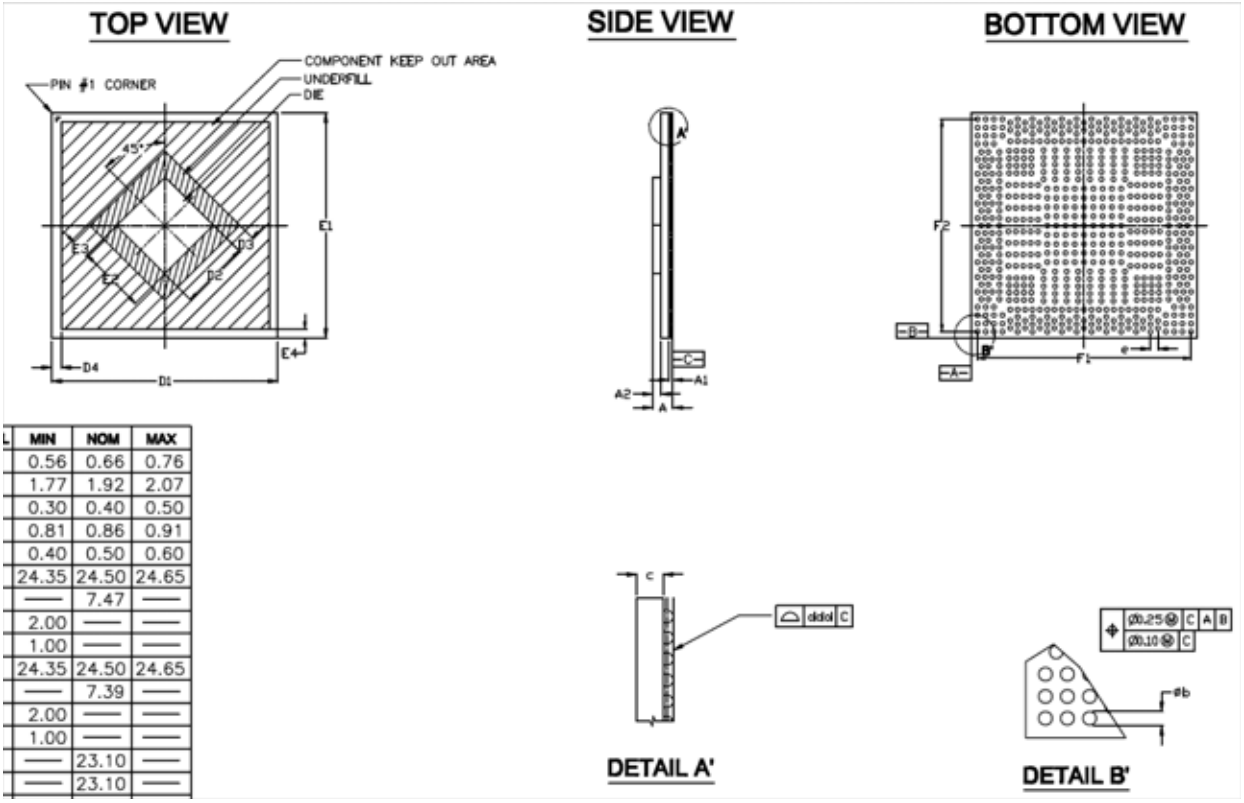
| Symbol | Parameter | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| $t_V$ | Output valid time | | 4 | ns | @ output load of 10 pf and timing measured from the falling edge of the clock |
| $t_{DS}$ | Data in setup | 5.5 | | ns | Timing measured from the falling edge of the clock |
| $t_{DH}$ | Data in hold | 0 | | ns | |
| $t_V$ (quad mode) | Output valid time | | 6 | ns | @ output load of 10 pf and timing measured from thefalling edge of the clock |
| $t_{DS}$ (quad mode) | Data in setup | 6 | | ns | Timing measured from the falling edge of the clock |
| $t_{DH}$ (quad mode) | Data in hold | 0 | | ns | |

**Table 56. SPI Serial Clock Timing (Supported frequencies: 16.5, 22, 33 and 66 MHz)**

| | **Minimum** | **Typical** | **Maximum** |
|---|---|---|---|
| Clock Frequency for READ instructions (fR) | 16.34 MHz | 16.50 MHz | 16.67 MHz |
| Clock High Time (tCLH) | 26.1 ns | 30.3 ns | 34.5 ns |
| Clock Low Time (tCLL) | 26.1 ns | 30.3 ns | 34.5 ns |
| Clock Rise Time (tCLCH) | 0.10 V/ns | | |
| Clock Fall Time (tCHCL) | 0.10 V/ns | | |
| | | | |
| | **Minimum** | **Typical** | **Maximum** |
| Clock Frequency for READ instructions (fR) | 21.78 MHz | 22.00 MHz | 22.22 MHz |
| Clock High Time (tCLH) | 12.9 ns | 15.0 ns | 17.1 ns |
| Clock Low Time (tCLL) | 25.8 ns | 30.0 ns | 34.2 ns |
| Clock Rise Time (tCLCH) | 0.10 V/ns | | |
| Clock Fall Time (tCHCL) | 0.10 V/ns | | |
| | | | |
| | **Minimum** | **Typical** | **Maximum** |
| Clock Frequency for READ instructions (fR) | 32.67 MHz | 33.00 MHz | 33.33 MHz |
| Clock High Time (tCLH) | 13.0 ns | 15.2 ns | 17.3 ns |
| Clock Low Time (tCLL) | 13.0 ns | 15.2 ns | 17.3 ns |
| Clock Rise Time (tCLCH) | 0.10 V/ns | | |
| Clock Fall Time (tCHCL) | 0.10 V/ns | | |
| | | | |
| | **Min** | **Typical** | **Max** |
| Clock Frequency for READ instructions (fR) | 65.34 MHz | 66.00 MHz | 66.66 MHz |
| Clock High Time (tCLH) | 6.5 ns | 7.6 ns | 8.6 ns |
| Clock Low Time (tCLL) | 6.5 ns | 7.6 ns | 8.6 ns |
| Clock Rise Time (tCLCH) | 0.10 V/ns | | |
| Clock Fall Time (tCHCL) | 0.10 V/ns | | |

# Chapter 7 Package Information

## 7.1 Physical Dimensions




| MIN | NOM | MAX |
|---|---|---|
| 0.56 | 0.66 | 0.76 |
| 1.77 | 1.92 | 2.07 |
| 0.30 | 0.40 | 0.50 |
| 0.81 | 0.86 | 0.91 |
| 0.40 | 0.50 | 0.60 |
| 24.35 | 24.50 | 24.65 |
| — | 7.47 | — |
| 2.00 | — | — |
| 1.00 | — | — |
| 24.35 | 24.50 | 24.65 |
| — | 7.39 | — |
| 2.00 | — | — |
| 1.00 | — | — |
| — | 23.10 | — |
| — | 23.10 | — |

**Figure 26. Bolton-E4 24.5 mm x 24.5 mm 0.8 mm Pitch 656-FCBGA Package Outline**

**Table 57. Bolton-E4 24.5 mm x 24.5 mm 0.8 mm Pitch 656-FCBGA Physical Dimensions**

| Reference | Minimum (mm) | Nominal (mm) | Maximum (mm) |
|---|---|---|---|
| c | 0.56 | 0.66 | 0.76 |
| A | 1.77 | 1.92 | 2.07 |
| A1 | 0.30 | 0.40 | 0.50 |
| A2 | 0.81 | 0.86 | 0.91 |
| ϕb | 0.40 | 0.50 | 0.60 |
| D1 | 24.35 | 24.50 | 24.65 |

**Table 57. Bolton-E4 24.5 mm x 24.5 mm 0.8 mm Pitch 656-FCBGA Physical Dimensions**

| Reference | Minimum (mm) | Nominal (mm) | Maximum (mm) |
|---|---|---|---|
| D2 | - | 6.84 | - |
| D3 | 2.00 | - | - |
| D4 | 1.00 | - | - |
| E1 | 24.35 | 24.50 | 24.65 |
| E2 | - | 7.20 | - |
| E3 | 2.00 | - | - |
| E4 | 1.00 | - | - |
| F1 | - | 23.10 | - |
| F2 | - | 23.10 | - |
| e (min. pitch) | - | 0.80 | - |
| ddd | - | - | 0.20 |

## 7.2 Pressure Specification

To avoid damages to the ASIC (die or solder ball joint cracks) caused by improper mechanical assembly of the cooling device, follow the recommendations below:

- It is recommended that the maximum load that is evenly applied across the contact area between the thermal management device and the die do not exceed 6 lbf. Note that a total load of 4-6 lbf is adequate to secure the thermal management device and achieve the lowest thermal contact resistance with a temperature drop across the thermal interface material of no more than 3°C. Also, the surface flatness of the metal spreader should be 0.001 inch/1 inch or better.
- Pre-test the assembly fixture with a strain gauge to make sure that the flexing of the final assembled board and the pressure applied around the ASIC package will not exceed 600 micro-strains under any circumstances.
- Ensure that any distortion (bow or twist) of the board after SMT and cooling device assembly is within industry guidelines (IPC/EIA J-STD-001). For measurement method, refer to the industry approved technique described in the manual *IPC-TM-650, section 2.4.22*.

# 7.3 Thermal Information

This section describes some key thermal parameters of Bolton-E4. For a detailed discussion on these parameters and other thermal design descriptions including package level thermal data and analysis, please consult the *Thermal Design and Analysis Guidelines for the Bolton Fusion Controller Hub, order# 51209.*

**Table 58. Bolton-E4 Thermal Limits**

| Parameter | Minimum | Nominal | Maximum | Unit | Note |
|---|---|---|---|---|---|
| Operating Case Temperature | 0 | — | 105 | °C | 1 |
| Absolute Rated Junction Temperature | — | — | 125 | °C | 2 |
| Storage Temperature | –40 | — | 60 | °C | |
| Ambient Temperature | 0 | — | 45 | °C | 3 |
| Thermal Design Power | — | See Table 59 | — | W | 4 |

***Notes:***

1. *The maximum operating case temperature is the die geometric top-center temperature measured through proper thermal contact to the back side of the die based on the methodology given in the document Thermal Design and Analysis Guidelines for the Bolton Fusion Controller Hub, order# 51209(Chapter 1). This is the temperature at which the functionality of the chip is qualified.*
2. *The maximum absolute rated junction temperature is the junction temperature at which the device can operate without causing damage to the ASIC.*
3. *The ambient temperature is defined as the temperature of the local intake air to the thermal management device. The maximum ambient temperature is dependent on the heat sink's local ambient conditions as well as the chassis' external ambient, and the value given here is based on the AMD reference Desktop heat sink solution for the FCH. Refer to Chapter 5 in the Thermal Design and Analysis Guidelines for the Bolton Fusion Controller Hub, order# 51209, for heat sink and thermal design guidelines. Refer to Chapter 6 of the above mentioned document for details of ambient conditions.*
4. *Thermal Design Power (TDP) is defined as the highest power dissipated while running currently available worst case applications at nominal voltages. The core voltage was raised to 5% above its nominal value for measuring the ASIC power. Since the core power of modern ASICs using 65nm and smaller process technology can vary significantly, parts specifically screened for higher core power were used for TDP measurement. The TDP is intended only as a design reference, and the value given here is preliminary.*

**Table 59. Bolton-E4 TDP Values and Configurations**

| | **Bolton-E4** |
|---|---|
| Clock Gen | Y |
| SATA | 8 x 6Gb/s |
| RAID | not supported |
| FIS-Based Switching | Y |
| HD Audio | Y |
| x1 PCIe GPP | 4 Gen 2 |
| Unified Media Interface | X4 Gen 2 |
| USB 3.0 + 2.0 + 1.1 Ports | 4 + 10 +2 |
| APU Fan Control | Y |
| Consumer IR | Y |
| SD Controller | Y |
| VGA DAC | Y |
| TDP (105 °C) | 7.8W |

# 7.4 Reflow Profile

A reference reflow profile is given below. Please note the following when using RoHS/lead-free solder (SAC105/305/405 Tin-Silver-Cu):

- The final reflow temperature profile will depend on the type of solder paste and chemistry of flux used in the SMT process. Modifications to the reference reflow profile may be required in order to accommodate the requirements of the other components in the application.
- An oven with 10 heating zones or above is recommended.
- To ensure that the reflow profile meets the target specification on both sides of the board, a different profile and oven recipe for the first and second reflow may be required.
- Mechanical stiffening can be used to minimize board warpage during reflow.
- It is suggested to decrease temperature cooling rate to minimize board warpage.
- This reflow profile applies only to RoHS/lead-free (high temperature) soldering process and it should not be used for eutectic solder packages. Damage may result if this condition is violated.
- Maximum 3 reflows are allowed on the same part.

**Table 60. Recommended Board Solder Reflow Profile - RoHS/Lead-Free Solder**

| Profiling Stage | Temperature | Process Range |
|---|---|---|
| Overall Preheat | Room temp to 220°C | 2 mins to 4 mins |
| Soaking Time | 130°C to 170°C | Typical 60 – 80 seconds |
| Liquidus | 220°C | Typical 60 – 80 seconds |
| Ramp Rate | Ramp up and Cooling | <2°C / second |
| Peak | Max. 245°C | 235°C ±5 °C |
| Temperature at peak within 5°C | 240°C to 245°C | 10 – 30 seconds |

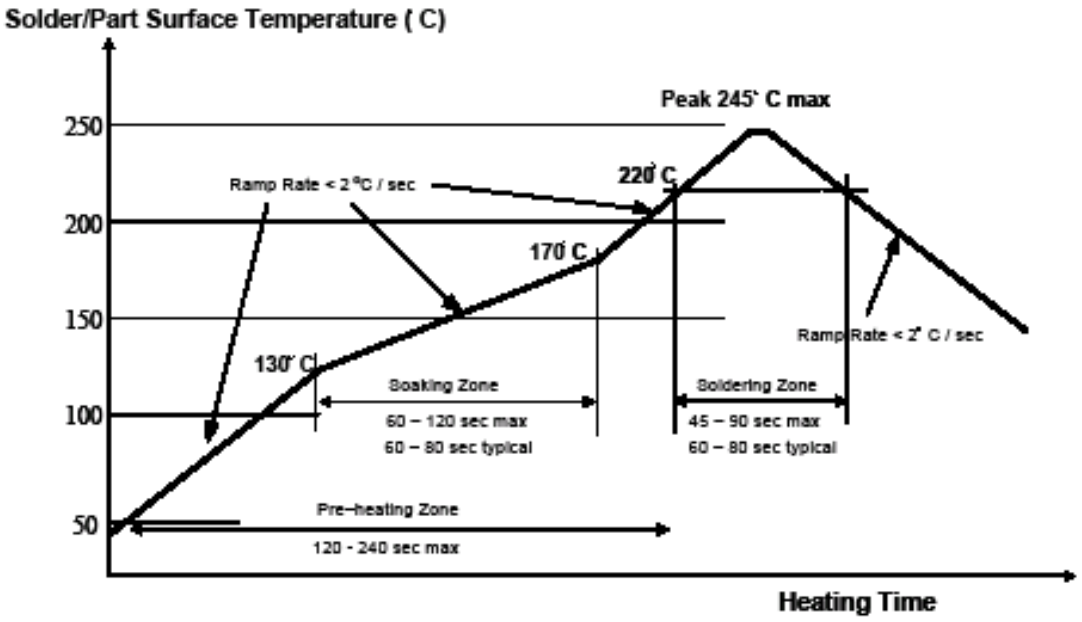



**Figure 27. RoHS/Lead-Free Solder (SAC305/405 Tin-Silver-Copper) Reflow Profile**

# Chapter 8 Testability

## 8.1 XOR Chain Test Mode

### 8.1.1 Test Control Signals

Table 61 shows the signals used for the integrated test controller of Bolton-E4.

**Table 61. Signals for the Test Controller of Bolton-E4**

| Signal Name | Description |
|---|---|
| 25M_X1, 25M_X2 | 25-MHz Reference Clock |
| TEST0 | Test0 input |
| TEST1 | Test1 input |
| TEST2 | Test2 input |

Table 62 shows how Test[2:0] are used to select the normal operation, ASIC debug, or test mode.

**Table 62. Test Mode Signals**

| TEST2 | TEST1 | TEST0 | Test Mode | Description |
|---|---|---|---|---|
| 0 | 0 | 0 | None | Normal operation |
| 0 | 0 | 1 | Reserved | Reserved for ASIC debug |
| 0 | 1 | X | Test Mode | EnableTest Mode |
| 1 | X | X | Reserved | Reserved for ASIC debug |

When TEST2 is low, a low on TEST1 will reset all test logic and allow TEST0 to choose between normal operation and the reserved debug mode. A high on TEST1 should be followed by a bit sequence on TEST0 to define the test mode into which Bolton-E4 will enter. A new test mode can be entered when a new bit sequence is transmitted. In addition to resetting the test controller asynchronously with TEST1, a bit sequence can also be used to synchronously change the test mode. Table 63 on page 116 shows the legal bit sequences for TEST0.

***Note:*** *Once the Test mode or Test mode and sub test mode is entered, Test2 and Test1 should be kept at 0 and 1 respectively until the requirement for the Test Mode is completed.*

**Table 63. TEST0 Bit Sequence**

| TEST0 bit sequence | Test Mode |
|---|---|
| 11111 | Look for first 0 to define a new test mode |
| 00000 | Reserved |
| 00001 | Alt Pull High Test |
| 00010 | Pull Outputs High |
| 00011 | Pull Outputs Low |
| 00100 | Pull Outputs to Z |
| 00101 | XOR Test Mode |

Figure 28 illustrates the data timing for the test signals with respect to the OSC clock. Any timing reference referred in this section is assumed to be based on OSC clock running at 25 MHz. The OSC clock can be slowed down to 1 MHz as long as the bit stream applied on TEST0 pin is also in sync with this clock. The 25-MHz OSC clock should be disconnected first. For setting any Test 0 bit sequence, the OSC clock is required only up-to the time the mode set is completed. After this the clock can be stopped and as long as TEST1 and Test2 pins are set to {1, 0} respectively to maintain the selected mode to be active. Note that once TEST1 is set to one, TEST0 needs to be asserted to one for at least 8 clocks before transmitting the test mode bit sequence. The rising of “Internal Test Mode” in the diagram indicates the time when Huhdson-2 enters into test mode.

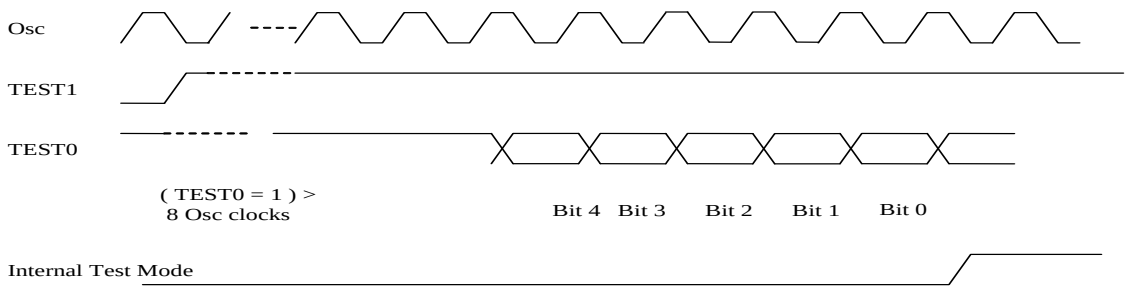



**Figure 28. Test Mode Capturing Sequence Timing**

## 8.1.2 Brief Description of an XOR Chain

A sample of a generic XOR chain is shown in the figure below.

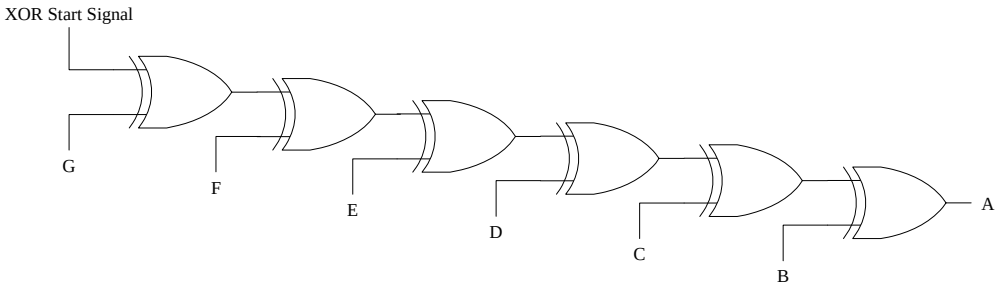



**Figure 29. A Generic XOR Chain**

Pin A is assigned to the output direction, and pins B through F are assigned to the input direction. After all pins from B to F are assigned to logic 0 or 1, a logic change in any one of these pins will toggle the output pin A.

Table 64 is the truth table for the XOR tree shown in Figure 29. The XOR start signal is assumed to be logic 1. The start signal is an internal signal to the ASIC and is not part of the XOR tree pins listed in Table 64.

Once the inputs are set to their respective values, the output pin will reflect the correct value within 200ns. Note: OSC clock is not required to be running after the mode is set and the pads are exercised in XOR tree function.

**Table 64. Truth Table for an XOR Chain**

| Test Vector Number | Input Pin G | Input Pin F | Input Pin E | Input Pin D | Input Pin C | Input Pin B | Output Pin A |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 4 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 5 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 6 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 7 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

# 8.2 Description of the Bolton-E4 XOR Chain

During XOR chain test mode, most of the chip pads on Bolton-E4 are connected together using XOR gates as shown in Figure 30. The first input of the chain is connected to a logic level high (internal connection), and all pads (listed in Table 65) are configured as inputs except for the last pad in the chain, which is configured as an output. Table 65 lists all pads that are on the Bolton-E4 XOR chain, as well as and their order of connection. Pads are chained together in the shown order, i.e., pad number 1 is the first pad on the XOR chain, pad number 2 the second, and so on.

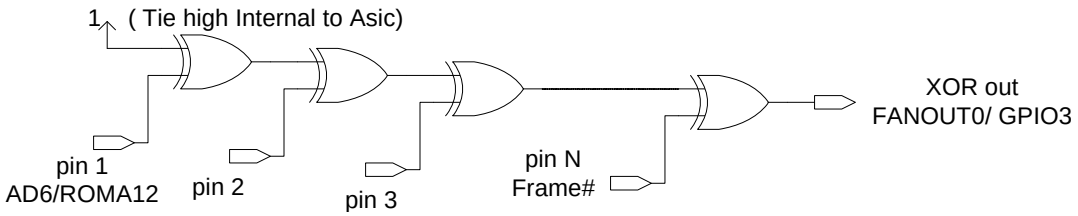



**Figure 30. On-chip XOR Chain Connectivity**

**Table 65. Connection Order of Bolton-E4 XOR Chain Pins**

| XOR# | Ball Ref | Pin Name |
|---|---|---|
| 1 | A31 | LFRAME# |
| 2 | C29 | ML_VGA_HPD/GPIO229 |
| 3 | A29 | LAD3 |
| 4 | E28 | PROCHOT# |
| 5 | C28 | LAD1 |
| 6 | D27 | LAD0 |
| 7 | B27 | LDRQ0# |
| 8 | G26 | LDT_STP# |
| 9 | F26 | LDT_RST# |
| 10 | E26 | LDT_PG |
| 11 | C26 | LPC_SMI#/GEVENT23# |
| 12 | A26 | LAD2 |
| 13 | G25 | DMA_ACTIVE# |
| 14 | D25 | LPCCLK1 |
| 15 | B25 | LPCCLK0 |
| 16 | F24 | KSI_3/GPIO204 |
| 17 | E24 | KSI_4/GPIO205 |
| 18 | C24 | KSI_6/GPIO207 |
| 19 | A24 | KSO_16/XDB2/GPIO225 |
| 20 | D23 | PS2M_DAT/GPIO191 |
| 21 | B23 | KSI_5/GPIO206 |
| 22 | K22 | KSI_1/GPIO202 |
| 23 | J22 | EC_PWM2/EC_TIMER2/ WOL_EN/GPIO199 |
| 24 | H22 | EC_PWM1/EC_TIMER1/ GPIO198 |
| 25 | G22 | SCL3_LV/GPIO195 |
| 26 | F22 | KSI_2/GPIO203 |
| 27 | E22 | EC_PWM0/EC_TIMER0/ GPIO197 |
| 28 | C22 | PS2M_CLK/GPIO192 |

| XOR# | Ball Ref | Pin Name |
|---|---|---|
| 29 | A22 | KSO_3/GPIO212 |
| 30 | K21 | KSI_0/GPIO201 |
| 31 | J21 | SPI_CS2#/GBE_STAT2/ GPIO166 |
| 32 | H21 | EC_PWM3/EC_TIMER3/ GPIO200 |
| 33 | G21 | SDA3_LV/GPIO196 |
| 34 | F21 | KSO_0/GPIO209 |
| 35 | D21 | PS2KB_DAT/GPIO189 |
| 36 | B21 | KSO_9/GPIO218 |
| 37 | F20 | KSO_2/GPIO211 |
| 38 | E20 | KSO_1/GPIO210 |
| 39 | C20 | PS2KB_CLK/GPIO190 |
| 40 | A20 | KSO_5/GPIO214 |
| 41 | K19 | PS2_DAT/SDA4/GPIO187 |
| 42 | J19 | PS2_CLK/SCL4/GPIO188 |
| 43 | H19 | SCL2/GPIO193 |
| 44 | G19 | SDA2/GPIO194 |
| 45 | D19 | KSO_11/GPIO220 |
| 46 | B19 | KSO_14/XDB0/GPIO223 |
| 47 | K18 | KSO_10/GPIO219 |
| 48 | J18 | KSO_6/GPIO215 |
| 49 | H18 | KSO_7/GPIO216 |
| 50 | G18 | KSO_8/GPIO217 |
| 51 | F18 | KSI_7/GPIO208 |
| 52 | E18 | KSO_4/GPIO213 |
| 53 | C18 | KSO_13/GPIO222 |
| 54 | A18 | KSO_12/GPIO221 |
| 55 | B17 | KSO_15/XDB1/GPIO224 |
| 56 | D17 | KSO_17/XDB3/GPIO226 |
| 57 | H5 | USB_FSD0N |
| 58 | H3 | USB_FSD1N |
| 59 | J4 | PWR_BTN# |

| XOR# | Ball Ref | Pin Name |
|---|---|---|
| 60 | F5 | USB_OC3#/AC_PRES/TDO/ GEVENT15# |
| 61 | K1 | WAKE#/GEVENT8# |
| 62 | J2 | IR_LED#/LLB#/GPIO184 |
| 63 | M5 | VIN7/GBE_LED3/ GPIO182 |
| 64 | P3 | VIN5/SCLK_1/GPIO180 |
| 65 | M1 | VIN6/GBE_STAT3/GPIO181 |
| 66 | P1 | VIN4/SLOAD_1/GPIO179 |
| 67 | K6 | TEMPIN0/GPIO171 |
| 68 | K5 | TEMPIN1/GPIO172 |
| 69 | K3 | TEMPIN2/GPIO173 |
| 70 | M6 | TEMPIN3/TALERT#/ GPIO174 |
| 71 | J7 | USB_OC1#/TDI/GEVENT13# |
| 72 | L2 | VIN2/SDATI_1/GPIO177 |
| 73 | N2 | VIN0/GPIO175 |
| 74 | M3 | VIN1/GPIO176 |
| 75 | N4 | VIN3/SDATO_1/GPIO178 |
| 76 | M7 | BLINK/USB_OC7#/ GEVENT18# |
| 77 | P5 | USB_OC2#/TCK/ GEVENT14# |
| 78 | P6 | USB_OC4#/IR_RX0/ GEVENT16# |
| 79 | R2 | RI#/GEVENT22# |
| 80 | R7 | SDA1/GPIO228 |
| 81 | R8 | USB_OC6#/IR_TX1/ GEVENT6# |
| 82 | R9 | PME#/GEVENT3# |
| 83 | R10 | THRMTRIP#/SMBALERT#/ GEVENT2# |
| 84 | T1 | USB_OC5#/IR_TX0/ GEVENT17# |
| 85 | T5 | LPC_PD#/GEVENT5# |

| XOR# | Ball Ref | Pin Name |
|---|---|---|
| 86 | T7 | SCL1/GPIO227 |
| 87 | T8 | USB_OC0#/ GEVENT12#/ TRST/SPI_TPM_CS# |
| 88 | T6 | SPI_CS1#/GPIO165 |
| 89 | V1 | ROM_RST#/SPI_WP#/ GPIO161 |
| 90 | U4 | SYS_RESET#/GEVENT19# |
| 91 | V3 | SPI_CLK/GPIO162 |
| 92 | V5 | SPI_DO/GPIO163 |
| 93 | V8 | DDR3_RST#/GEVENT7#/ VGA_PD |
| 94 | V7 | IR_RX1/GEVENT20# |
| 95 | V10 | GBE_LED2/ GEVENT10# |
| 96 | V6 | SPI_DI/GPIO164 |
| 97 | Y6 | SPI_HOLD#/ GBE_LED1/GEVENT9# |
| 98 | W8 | GBE_LED0/GPIO183 |
| 99 | W9 | GBE_PHY_INTR |
| 100 | AC2 | GBE_PHY_PD |
| 101 | W7 | SPI_CS3#/GBE_STAT1/ GEVENT21# |
| 102 | AA7 | GBE_PHY_RST# |
| 103 | AA8 | GBE_STAT0/GEVENT11# |
| 104 | W10 | GBE_MDIO |
| 105 | AC4 | GBE_COL |
| 106 | AD1 | GBE_RXERR |
| 107 | AD3 | GBE_CRS |
| 108 | AD9 | GBE_MDCK |
| 109 | AE2 | PCIE_RST# |
| 110 | AD5 | A_RST# |
| 111 | AB5 | PCIRST# |
| 112 | AB6 | PCIE_RST2#/GEVENT4# |
| 113 | Y1 | AZ_SDIN3/GPIO170 |

| XOR# | Ball Ref | Pin Name |
|---|---|---|
| 114 | Y3 | AZ_SDIN2/GPIO169 |
| 115 | Y5 | AZ_SDIN1/GPIO168 |
| 116 | AA2 | AZ_SDIN0/GPIO167 |
| 117 | AB3 | AZ_BITCLK |
| 118 | AB1 | AZ_SDOUT |
| 119 | AE4 | AZ_RST# |
| 120 | AD6 | AZ_SYNC |
| 121 | AB7 | GBE_TXCLK |
| 122 | AB8 | GBE_RXCLK |
| 123 | AB9 | GBE_TXCTL/TXEN |
| 124 | AD7 | GBE_RXD0 |
| 125 | AD8 | GBE_TXD0 |
| 126 | AE7 | GBE_RXD1 |
| 127 | AE8 | GBE_TXD1 |
| 128 | AF7 | GBE_RXD2 |
| 129 | AF9 | GBE_TXD3 |
| 130 | AG6 | GBE_TXD2 |
| 131 | AG8 | GBE_RXCTL/RXDV |
| 132 | AH7 | GBE_RXD3 |
| 133 | AF1 | PCICLK1/GPO36 |
| 134 | AF3 | PCICLK0 |
| 135 | AF5 | PCICLK2/GPO37 |
| 136 | AF6 | PCICLK4/14M_OSC/GPO39 |
| 137 | AG2 | PCICLK3/GPO38 |
| 138 | AL1 | AD6/GPIO6 |
| 139 | AJ1 | AD9/GPIO9 |
| 140 | AH1 | STOP# |
| 141 | AN3 | CBE0# |
| 142 | AL3 | AD11/GPIO11 |
| 143 | AJ3 | AD0/GPIO0 |
| 144 | AH3 | AD4/GPIO4 |
| 145 | AG4 | AD2/GPIO2 |
| 146 | AN5 | AD7/GPIO7 |

| XOR# | Ball Ref | Pin Name |
|---|---|---|
| 147 | AL5 | AD1/GPIO1 |
| 148 | AJ5 | AD5/GPIO5 |
| 149 | AN6 | AD8/GPIO8 |
| 150 | AL6 | AD3/GPIO3 |
| 151 | AJ6 | AD13/GPIO13 |
| 152 | AM7 | AD12/GPIO12 |
| 153 | AK7 | AD14/GPIO14 |
| 154 | AN8 | AD15/GPIO15 |
| 155 | AL8 | AD10/GPIO10 |
| 156 | AJ8 | CBE1# |
| 157 | AH8 | SERR# |
| 158 | AM9 | PERR# |
| 159 | AK9 | DEVSEL# |
| 160 | AH9 | LOCK# |
| 161 | AG9 | AD16/GPIO16 |
| 162 | AN10 | CBE2# |
| 163 | AL10 | IRDY# |
| 164 | AJ10 | AD18/GPIO18 |
| 165 | AG10 | FRAME# |
| 166 | AF10 | TRDY# |
| 167 | AE10 | PAR |
| 168 | AM11 | AD17/GPIO17 |
| 169 | AK11 | AD20/GPIO20 |
| 170 | AN12 | AD21/GPIO21 |
| 171 | AL12 | AD19/GPIO19 |
| 172 | AG12 | AD22/GPIO22 |
| 173 | AE12 | AD23/GPIO23 |
| 174 | AE16 | AD31/GPIO31 |
| 175 | AG15 | REQ0# |
| 176 | AD13 | GNT1#/GPO44 |
| 177 | AD12 | CBE3# |
| 178 | AC12 | AD24/GPIO24 |
| 179 | AD18 | INTH#/GPIO35 |

| XOR# | Ball Ref | Pin Name |
|---|---|---|
| 180 | AD21 | GNT2#/SD_LED/GPO45 |
| 181 | AD16 | GNT0# |
| 182 | AC16 | INTG#/GPIO34 |
| 183 | AG13 | REQ1#/GPIO40 |
| 184 | AE13 | AD25/GPIO25 |
| 185 | AF13 | AD26/GPIO26 |
| 186 | AH13 | AD27/GPIO27 |
| 187 | AH14 | AD28/GPIO28 |
| 188 | AD15 | AD29/GPIO29 |
| 189 | AC15 | AD30/GPIO30 |
| 190 | AD19 | CLKRUN# |
| 191 | AF15 | REQ2#/CLK_REQ8#/GPIO41 |
| 192 | AE18 | INTF#/GPIO33 |
| 193 | AF18 | INTE#/GPIO32 |
| 194 | AK17 | GNT3#/CLK_REQ7#/ SATA_IS7#/GPIO46 |
| 195 | AM17 | REQ3#/CLK_REQ5#/ SATA_IS6#/GPIO42 |
| 196 | AL16 | FANIN2/GPIO58 |
| 197 | AN16 | FANIN1/GPIO57 |
| 198 | AJ16 | FANOUT2/GPIO54 |
| 199 | AM15 | FANOUT1/GPIO53 |
| 200 | AH16 | FANOUT0/GPIO52 |
| 201 | AK15 | FANIN0/GPIO56 |
| 202 | AE19 | SERIRQ/GPIO48 |
| 203 | AD22 | SATA_ACT#/GPIO67 |
| 204 | AH17 | SATA_IS4#/FANOUT3/ GPIO55 |
| 205 | AG18 | SATA_IS5#/FANIN3/ GPIO59 |
| 206 | AF25 | CLK_REQG#/GPIO65/ OSCIN/IDLEEXIT# |
| 207 | AF19 | NB_PWRGD |
| 208 | AG19 | KBRST#/GEVENT1# |

| XOR# | Ball Ref | Pin Name |
|---|---|---|
| 209 | AE22 | GA20IN/GEVENT0# |
| 210 | AE24 | CLK_REQ3#/SATA_IS1#/ GPIO63 |
| 211 | AG26 | SMARTVOLT2/ SHUTDOWN#/GPIO51 |
| 212 | AG24 | CLK_REQ4#/SATA_IS0#/ GPIO64 |
| 213 | AD25 | SDA0/GPIO47 |
| 214 | AG25 | CLK_REQ2#/FANIN4/ GPIO62 |
| 215 | AG22 | CLK_REQ1#/FANOUT4/ GPIO61 |
| 216 | AF24 | SPKR/GPIO66 |
| 217 | AD26 | SCL0/GPIO43 |
| 218 | AE26 | SMARTVOLT1/SATA_IS2#/ GPIO50 |
| 219 | AF22 | CLK_REQ0#/SATA_IS3#/ GPIO60 |
| 220 | AE27 | LDRQ1#/CLK_REQ6#/ GPIO49 |
| 221 | AH12 | SD_WP/GPIO76 |
| 222 | AN14 | SD_CMD/SLOAD_0/ GPIO74 |
| 223 | AL14 | SD_CLK/SCLK_0/ GPIO73 |
| 224 | AJ12 | SD_CD#/GPIO75 |
| 225 | AJ14 | SD_DATA3/GPIO80 |
| 226 | AK13 | SD_DATA0/SDATI_0/ GPIO77 |
| 227 | AM13 | SD_DATA1/SDATO_0/ GPIO78 |
| 228 | AH15 | SD_DATA2/GPIO79 |
| 229 | N32 | VGA_DDC_SCL/GPO71 |
| 230 | M33 | VGA_DDC_SDA/GPO70 |
| 231 | M28 | VGA_HSYNC/GPO68 |
| 232 | N30 | VGA_VSYNC/GPO69 |

### 8.2.1 Unused Pins

The pins that are part of the XOR chain (see Table 65 on page 118) but are not used for testing must be pulled up or down before the XOR chain is activated. No pins in the XOR chain should be left floating. All digital or analog pins not included in Table 65 on page 118 are not part of the XOR chain and can be left floating during an XOR test.

# Appendix A Pin Listing

This appendix contains pin listings for the Bolton-E4 sorted in two different ways. To go to the listing of interest, click on the linked cross-references below:

- "Pin List by Pin Name" on page 126
- "Pin List by Ball Number" on page 143

# A.1 Pin List by Pin Name

**Table A-1 Pin Listing by Pin Name**

| Pin Name | Ball # |
|---|---|
| 14M_25M_48M_OSC | J26 |
| 25M_X1 | C31 |
| 25M_X2 | C33 |
| 32K_X1 | G2 |
| 32K_X2 | G4 |
| A_RST# | AD5 |
| AD0/GPIO0 | AJ3 |
| AD1/GPIO1 | AL5 |
| AD10/GPIO10 | AL8 |
| AD11/GPIO11 | AL3 |
| AD12/GPIO12 | AM7 |
| AD13/GPIO13 | AJ6 |
| AD14/GPIO14 | AK7 |
| AD15/GPIO15 | AN8 |
| AD16/GPIO16 | AG9 |
| AD17/GPIO17 | AM11 |
| AD18/GPIO18 | AJ10 |
| AD19/GPIO19 | AL12 |
| AD2/GPIO2 | AG4 |
| AD20/GPIO20 | AK11 |
| AD21/GPIO21 | AN12 |
| AD22/GPIO22 | AG12 |
| AD23/GPIO23 | AE12 |
| AD24/GPIO24 | AC12 |
| AD25/GPIO25 | AE13 |
| AD26/GPIO26 | AF13 |
| AD27/GPIO27 | AH13 |
| AD28/GPIO28 | AH14 |
| AD29/GPIO29 | AD15 |
| AD3/GPIO3 | AL6 |
| AD30/GPIO30 | AC15 |
| AD31/GPIO31 | AE16 |
| AD4/GPIO4 | AH3 |
| AD5/GPIO5 | AJ5 |
| AD6/GPIO6 | AL1 |
| AD7/GPIO7 | AN5 |
| AD8/GPIO8 | AN6 |
| AD9/GPIO9 | AJ1 |
| APU_CLKN | T23 |
| APU_CLKP | T24 |
| APU_PG | E26 |

| Pin Name | Ball # |
|---|---|
| APU_RST# | F26 |
| AUX_VGA_CH_N | V29 |
| AUX_VGA_CH_P | V28 |
| AUXCAL | U28 |
| AZ_BITCLK | AB3 |
| AZ_RST# | AE4 |
| AZ_SDIN0/GPIO167 | AA2 |
| AZ_SDIN1/GPIO168 | Y5 |
| AZ_SDIN2/GPIO169 | Y3 |
| AZ_SDIN3/GPIO170 | Y1 |
| AZ_SDOUT | AB1 |
| AZ_SYNC | AD6 |
| BLINK/USB_OC7#/ GEVENT18# | M7 |
| CBE0# | AN3 |
| CBE1# | AJ8 |
| CBE2# | AN10 |
| CBE3# | AD12 |
| CLK_CALRN | F27 |
| CLK_REQ0#/ SATA_IS3#/GPIO60 | AF22 |
| CLK_REQ1#/ FANOUT4/GPIO61 | AG22 |
| CLK_REQ2#/FANIN4/ GPIO62 | AG25 |
| CLK_REQ3#/ SATA_IS1#/GPIO63 | AE24 |
| CLK_REQ4#/ SATA_IS0#/GPIO64 | AG24 |
| CLK_REQG#/GPIO65/ OSCIN/IDLEEXIT# | AF25 |
| CLKRUN# | AD19 |
| DDR3_RST#/ GEVENT7#/VGA_PD | V8 |
| DEVSEL# | AK9 |
| DISP_CLKN | T26 |
| DISP_CLKP | R26 |
| DISP2_CLKN | H31 |
| DISP2_CLKP | H33 |
| DMA_ACTIVE# | G25 |
| EC_PWM0/ EC_TIMER0/GPIO197 | E22 |
| EC_PWM1/ EC_TIMER1/GPIO198 | H22 |
| EC_PWM2/ EC_TIMER2/WOL_EN/ GPIO199 | J22 |

| Pin Name | Ball # |
|---|---|
| EC_PWM3/ EC_TIMER3/GPIO200 | H21 |
| FANIN0/GPIO56 | AK15 |
| FANIN1/GPIO57 | AN16 |
| FANIN2/GPIO58 | AL16 |
| FANOUT0/GPIO52 | AH16 |
| FANOUT1/GPIO53 | AM15 |
| FANOUT2/GPIO54 | AJ16 |
| FRAME# | AG10 |
| GA20IN/GEVENT0# | AE22 |
| GBE_COL | AC4 |
| GBE_CRS | AD3 |
| GBE_LED0/GPIO183 | W8 |
| GBE_LED2/ GEVENT10# | V10 |
| GBE_MDCK | AD9 |
| GBE_MDIO | W10 |
| GBE_PHY_INTR | W9 |
| GBE_PHY_PD | AC2 |
| GBE_PHY_RST# | AA7 |
| GBE_RXCLK | AB8 |
| GBE_RXCTL/RXDV | AG8 |
| GBE_RXD0 | AD7 |
| GBE_RXD1 | AE7 |
| GBE_RXD2 | AF7 |
| GBE_RXD3 | AH7 |
| GBE_RXERR | AD1 |
| GBE_STAT0/ GEVENT11# | AA8 |
| GBE_TXCLK | AB7 |
| GBE_TXCTL/TXEN | AB9 |
| GBE_TXD0 | AD8 |
| GBE_TXD1 | AE8 |
| GBE_TXD2 | AG6 |
| GBE_TXD3 | AF9 |
| GNT0# | AD16 |
| GNT1#/GPO44 | AD13 |
| GNT2#/SD_LED/ GPO45 | AD21 |
| GNT3#/CLK_REQ7#/ SATA_IS7#/GPIO46 (Note: SATA_IS7# applies to | AK17 |
| GPP_CLK0N | H28 |
| GPP_CLK0P | H27 |
| GPP_CLK1N | K26 |
| GPP_CLK1P | J27 |

| Pin Name | Ball # |
|---|---|
| GPP_CLK2N | F31 |
| GPP_CLK2P | F33 |
| GPP_CLK3N | E31 |
| GPP_CLK3P | E33 |
| GPP_CLK4N | M24 |
| GPP_CLK4P | M23 |
| GPP_CLK5N | M26 |
| GPP_CLK5P | M27 |
| GPP_CLK6N | N26 |
| GPP_CLK6P | N25 |
| GPP_CLK7N | R24 |
| GPP_CLK7P | R23 |
| GPP_CLK8N | R27 |
| GPP_CLK8P | N27 |
| GPP_RX0N | AA26 |
| GPP_RX0P | AA27 |
| GPP_RX1N | V27 |
| GPP_RX1P | W27 |
| GPP_RX2N | W26 |
| GPP_RX2P | V26 |
| GPP_RX3N | W23 |
| GPP_RX3P | W24 |
| GPP_TX0N | V31 |
| GPP_TX0P | V33 |
| GPP_TX1N | W32 |
| GPP_TX1P | W30 |
| GPP_TX2N | AB27 |
| GPP_TX2P | AB26 |
| GPP_TX3N | AA23 |
| GPP_TX3P | AA24 |
| INTE#/GPIO32 | AF18 |
| INTF#/GPIO33 | AE18 |
| INTG#/GPIO34 | AC16 |
| INTH#/GPIO35 | AD18 |
| INTRUDER_ALERT# | F3 |
| IR_LED#/LLB#/ GPIO184 | J2 |
| IR_RX1/GEVENT20# | V7 |
| IRDY# | AL10 |
| KBRST#/GEVENT1# | AG19 |
| KSI_0/GPIO201 | K21 |
| KSI_1/GPIO202 | K22 |
| KSI_2/GPIO203 | F22 |
| KSI_3/GPIO204 | F24 |
| KSI_4/GPIO205 | E24 |
| KSI_5/GPIO206 | B23 |

| Pin Name | Ball # |
|---|---|
| KSI_6/GPIO207 | C24 |
| KSI_7/GPIO208 | F18 |
| KSO_0/GPIO209 | F21 |
| KSO_1/GPIO210 | E20 |
| KSO_10/GPIO219 | K18 |
| KSO_11/GPIO220 | D19 |
| KSO_12/GPIO221 | A18 |
| KSO_13/GPIO222 | C18 |
| KSO_14/XDB0/ GPIO223 | B19 |
| KSO_15/XDB1/ GPIO224 | B17 |
| KSO_16/XDB2/ GPIO225 | A24 |
| KSO_17/XDB3/ GPIO226 | D17 |
| KSO_2/GPIO211 | F20 |
| KSO_3/GPIO212 | A22 |
| KSO_4/GPIO213 | E18 |
| KSO_5/GPIO214 | A20 |
| KSO_6/GPIO215 | J18 |
| KSO_7/GPIO216 | H18 |
| KSO_8/GPIO217 | G18 |
| KSO_9/GPIO218 | B21 |
| LAD0 | D27 |
| LAD1 | C28 |
| LAD2 | A26 |
| LAD3 | A29 |
| LDO_CAP | M31 |
| LDRQ0# | B27 |
| LDRQ1#/CLK_REQ6#/ GPIO49 | AE27 |
| LDT_STP# | G26 |
| LFRAME# | A31 |
| LOCK# | AH9 |
| LPC_PD#/GEVENT5# | T5 |
| LPC_SMI#/ GEVENT23# | C26 |
| LPCCLK0 | B25 |
| LPCCLK1 | D25 |
| ML_VGA_HPD/ GPIO229 | C29 |
| ML_VGA_L0N | T33 |
| ML_VGA_L0P | T31 |
| ML_VGA_L1N | T28 |
| ML_VGA_L1P | T29 |
| ML_VGA_L2N | R30 |

| Pin Name | Ball # |
|---|---|
| ML_VGA_L2P | R32 |
| ML_VGA_L3N | P28 |
| ML_VGA_L3P | P29 |
| NC1 | AG16 |
| NC10 | AH33 |
| NC11 | AH31 |
| NC12 | AJ33 |
| NC13 | AJ31 |
| NC2 | AH10 |
| NC3 | A28 |
| NC4 | G27 |
| NC5 | L4 |
| NC6 | AL29 |
| NC7 | AN31 |
| NC8 | AL31 |
| NC9 | AL33 |
| PAR | AE10 |
| PCICLK0 | AF3 |
| PCICLK1/GPO36 | AF1 |
| PCICLK2/GPO37 | AF5 |
| PCICLK3/GPO38 | AG2 |
| PCICLK4/14M_OSC/ GPO39 | AF6 |
| PCIE_CALRN | AF31 |
| PCIE_CALRP | AF29 |
| PCIE_RCLKN | G28 |
| PCIE_RCLKP | G30 |
| PCIE_RST# | AE2 |
| PCIE_RST2#/ GEVENT4# | AB6 |
| PCIRST# | AB5 |
| PERR# | AM9 |
| PME#/GEVENT3# | R9 |
| PROCHOT# | E28 |
| PS2_CLK/SCL4/ GPIO188 | J19 |
| PS2_DAT/SDA4/ GPIO187 | K19 |
| PS2KB_CLK/GPIO190 | C20 |
| PS2KB_DAT/GPIO189 | D21 |
| PS2M_CLK/GPIO192 | C22 |
| PS2M_DAT/GPIO191 | D23 |
| PWR_BTN# | J4 |
| PWR_GOOD | N7 |
| REQ0# | AG15 |
| REQ1#/GPIO40 | AG13 |

| Pin Name | Ball # |
|---|---|
| REQ2#/CLK_REQ8#/ GPIO41 | AF15 |
| REQ3#/CLK_REQ5#/ SATA_IS6#/GPIO42 | AM17 |
| RI#/GEVENT22# | R2 |
| ROM_RST#/SPI_WP#/ GPIO161 | V1 |
| RSMRST# | U2 |
| RTCCLK | F1 |
| S5_CORE_EN | H7 |
| SATA_ACT#/GPIO67 | AD22 |
| SATA_CALRN | AF27 |
| SATA_CALRP | AF28 |
| SATA_IS4#/FANOUT3/ GPIO55 | AH17 |
| SATA_IS5#/FANIN3/ GPIO59 | AG18 |
| SATA_RX0N | AL20 |
| SATA_RX0P | AN20 |
| SATA_RX1N | AH20 |
| SATA_RX1P | AJ20 |
| SATA_RX2N | AM23 |
| SATA_RX2P | AK23 |
| SATA_RX3N | AN24 |
| SATA_RX3P | AL24 |
| SATA_RX4N | AJ26 |
| SATA_RX4P | AH26 |
| SATA_RX5N | AK27 |
| SATA_RX5P | AM27 |
| SATA_RX6N | AL31 |
| SATA_RX6P | AL33 |
| SATA_RX7N | AJ33 |
| SATA_RX7P | AJ31 |
| SATA_TX0N | AM19 |
| SATA_TX0P | AK19 |
| SATA_TX1N | AL22 |
| SATA_TX1P | AN22 |
| SATA_TX2N | AH22 |
| SATA_TX2P | AJ22 |
| SATA_TX3N | AJ24 |
| SATA_TX3P | AH24 |
| SATA_TX4N | AN26 |
| SATA_TX4P | AL26 |
| SATA_TX5N | AL28 |
| SATA_TX5P | AN29 |
| SATA_TX6N | AN31 |
| SATA_TX6P | AL29 |

| Pin Name | Ball # |
|---|---|
| SATA_TX7N | AH31 |
| SATA_TX7P | AH33 |
| SATA_X1 | AF21 |
| SATA_X2 | AG21 |
| SCL0/GPIO43 | AD26 |
| SCL1/GPIO227 | T7 |
| SCL2/GPIO193 | H19 |
| SCL3_LV/GPIO195 | G22 |
| SD_CD#/GPIO75 | AJ12 |
| SD_CLK/SCLK_0/ GPIO73 | AL14 |
| SD_CMD/SLOAD_0/ GPIO74 | AN14 |
| SD_DATA0/SDATI_0/ GPIO77 | AK13 |
| SD_DATA1/SDATO_0/ GPIO78 | AM13 |
| SD_DATA2/GPIO79 | AH15 |
| SD_DATA3/GPIO80 | AJ14 |
| SD_WP/GPIO76 | AH12 |
| SDA0/GPIO47 | AD25 |
| SDA1/GPIO228 | R7 |
| SDA2/GPIO194 | G19 |
| SDA3_LV/GPIO196 | G21 |
| SERIRQ/GPIO48 | AE19 |
| SERR# | AH8 |
| SLP_S3# | T3 |
| SLP_S5# | W2 |
| SLT_GFX_CLKN | K29 |
| SLT_GFX_CLKP | J30 |
| SMARTVOLT1/ SATA_IS2#/GPIO50 | AE26 |
| SMARTVOLT2/ SHUTDOWN#/GPIO51 | AG26 |
| SPI_CLK/GPIO162 | V3 |
| SPI_CS1#/GPIO165 | T6 |
| SPI_CS2#/ GBE_STAT2/GPIO166 | J21 |
| SPI_CS3#/ GBE_STAT1/ GEVENT21# | W7 |
| SPI_DI/GPIO164 | V6 |
| SPI_DO/GPIO163 | V5 |
| SPI_HOLD#/ GBE_LED1/GEVENT9# | Y6 |
| SPKR/GPIO66 | AF24 |
| STOP# | AH1 |

| Pin Name | Ball # |
|---|---|
| SYS_RESET#/ GEVENT19# | U4 |
| TEMPIN0/GPIO171 | K6 |
| TEMPIN1/GPIO172 | K5 |
| TEMPIN2/GPIO173 | K3 |
| TEMPIN3/TALERT#/ GPIO174 | M6 |
| TEST0 | T9 |
| TEST1/TMS | T10 |
| TEST2 | V9 |
| THRMTRIP#/ SMBALERT#/ GEVENT2# | R10 |
| TRDY# | AF10 |
| UMI_RX0N | AB31 |
| UMI_RX0P | AB33 |
| UMI_RX1N | AB29 |
| UMI_RX1P | AB28 |
| UMI_RX2N | Y31 |
| UMI_RX2P | Y33 |
| UMI_RX3N | Y29 |
| UMI_RX3P | Y28 |
| UMI_TX0N | AE32 |
| UMI_TX0P | AE30 |
| UMI_TX1N | AD31 |
| UMI_TX1P | AD33 |
| UMI_TX2N | AD29 |
| UMI_TX2P | AD28 |
| UMI_TX3N | AC32 |
| UMI_TX3P | AC30 |
| USB_FSD0N | H5 |
| USB_FSD0P/GPIO185 | H6 |
| USB_FSD1N | H3 |
| USB_FSD1P/GPIO186 | H1 |
| USB_HSD0N | E3 |
| USB_HSD0P | E1 |
| USB_HSD10N | K13 |
| USB_HSD10P | K12 |
| USB_HSD11N | F12 |
| USB_HSD11P | G12 |
| USB_HSD12N | J12 |
| USB_HSD12P | K10 |
| USB_HSD13N | G10 |
| USB_HSD13P | H10 |
| USB_HSD1N | C3 |
| USB_HSD1P | C1 |

| Pin Name | Ball # |
|---|---|
| USB_HSD2N | A5 |
| USB_HSD2P | C5 |
| USB_HSD3N | A6 |
| USB_HSD3P | C6 |
| USB_HSD4N | E8 |
| USB_HSD4P | F8 |
| USB_HSD5N | C8 |
| USB_HSD5P | A8 |
| USB_HSD6N | G9 |
| USB_HSD6P | H9 |
| USB_HSD7N | A10 |
| USB_HSD7P | C10 |
| USB_HSD8N | F10 |
| USB_HSD8P | E10 |
| USB_HSD9N | D11 |
| USB_HSD9P | B11 |
| USB_OC0#/ GEVENT12#/TRST | T8 |
| USB_OC1#/TDI/ GEVENT13# | J7 |
| USB_OC2#/TCK/ GEVENT14# | P5 |
| USB_OC3#/AC_PRES/ TDO/GEVENT15# | F5 |
| USB_OC4#/IR_RX0/ GEVENT16# | P6 |
| USB_OC5#/IR_TX0/ GEVENT17# | T1 |
| USB_OC6#/IR_TX1/ GEVENT6# | R8 |
| USB_RCOMP | B9 |
| USB_SS_RX0N | K15 |
| USB_SS_RX0P | J15 |
| USB_SS_RX1N | G13 |
| USB_SS_RX1P | H13 |
| USB_SS_RX2N | F14 |
| USB_SS_RX2P | E14 |
| USB_SS_RX3N | A12 |
| USB_SS_RX3P | C12 |
| USB_SS_TX0N | H16 |
| USB_SS_TX0P | J16 |
| USB_SS_TX1N | G15 |
| USB_SS_TX1P | F15 |
| USB_SS_TX2N | B15 |
| USB_SS_TX2P | D15 |
| USB_SS_TX3N | C14 |
| USB_SS_TX3P | A14 |

| Pin Name | Ball # |
|---|---|
| USBCLK/ 14M_25M_48M_OSC | G8 |
| USBSS_CALRN | A16 |
| USBSS_CALRP | C16 |
| VDDAN_11_CLK_1 | H26 |
| VDDAN_11_CLK_2 | J25 |
| VDDAN_11_CLK_3 | K24 |
| VDDAN_11_CLK_4 | L22 |
| VDDAN_11_CLK_5 | M22 |
| VDDAN_11_CLK_6 | N21 |
| VDDAN_11_CLK_7 | N22 |
| VDDAN_11_CLK_8 | P22 |
| VDDAN_11_ML_1 | Y22 |
| VDDAN_11_ML_2 | V23 |
| VDDAN_11_ML_3 | V24 |
| VDDAN_11_ML_4 | V25 |
| VDDAN_11_PCIE_1 | AB24 |
| VDDAN_11_PCIE_2 | Y21 |
| VDDAN_11_PCIE_3 | AE25 |
| VDDAN_11_PCIE_4 | AD24 |
| VDDAN_11_PCIE_5 | AB23 |
| VDDAN_11_PCIE_6 | AA22 |
| VDDAN_11_PCIE_7 | AF26 |
| VDDAN_11_PCIE_8 | AG27 |
| VDDAN_11_SATA_1 | AA21 |
| VDDAN_11_SATA_10 | AC19 |
| VDDAN_11_SATA_2 | AB21 |
| VDDAN_11_SATA_3 | AB22 |
| VDDAN_11_SATA_4 | Y20 |
| VDDAN_11_SATA_5 | AC22 |
| VDDAN_11_SATA_6 | AC21 |
| VDDAN_11_SATA_7 | AA20 |
| VDDAN_11_SATA_8 | AA18 |
| VDDAN_11_SATA_9 | AB20 |
| VDDAN_11_SSUSB_S_1 | P16 |
| VDDAN_11_SSUSB_S_2 | M14 |
| VDDAN_11_SSUSB_S_3 | N14 |
| VDDAN_11_SSUSB_S_4 | P13 |
| VDDAN_11_SSUSB_S_5 | P14 |
| VDDAN_11_USB_S_1 | U12 |
| VDDAN_11_USB_S_2 | U13 |
| VDDAN_33_DAC | T22 |

| Pin Name | Ball # |
|---|---|
| VDDAN_33_HWM_S | M8 |
| VDDAN_33_USB_S_1 | G7 |
| VDDAN_33_USB_S_10 | M12 |
| VDDAN_33_USB_S_11 | N12 |
| VDDAN_33_USB_S_12 | M11 |
| VDDAN_33_USB_S_2 | H8 |
| VDDAN_33_USB_S_3 | J8 |
| VDDAN_33_USB_S_4 | K8 |
| VDDAN_33_USB_S_5 | K9 |
| VDDAN_33_USB_S_6 | M9 |
| VDDAN_33_USB_S_7 | M10 |
| VDDAN_33_USB_S_8 | N9 |
| VDDAN_33_USB_S_9 | N10 |
| VDDBT_RTC_G | E6 |
| VDDCR_11_1 | T14 |
| VDDCR_11_2 | T17 |
| VDDCR_11_3 | T20 |
| VDDCR_11_4 | U16 |
| VDDCR_11_5 | U18 |
| VDDCR_11_6 | V14 |
| VDDCR_11_7 | V17 |
| VDDCR_11_8 | V20 |
| VDDCR_11_9 | Y17 |
| VDDCR_11_GBE_S_1 | AB11 |
| VDDCR_11_GBE_S_2 | AA11 |
| VDDCR_11_S_1 | N20 |
| VDDCR_11_S_2 | M20 |
| VDDCR_11_SSUSB_S_1 | N16 |
| VDDCR_11_SSUSB_S_2 | N17 |
| VDDCR_11_SSUSB_S_3 | P17 |
| VDDCR_11_SSUSB_S_4 | M17 |
| VDDCR_11_USB_S_1 | T12 |
| VDDCR_11_USB_S_2 | T13 |
| VDDIO_33_GBE_S | AB10 |
| VDDIO_33_PCIGP_1 | AB17 |
| VDDIO_33_PCIGP_10 | AB16 |
| VDDIO_33_PCIGP_2 | AB18 |
| VDDIO_33_PCIGP_3 | AE9 |
| VDDIO_33_PCIGP_4 | AD10 |
| VDDIO_33_PCIGP_5 | AG7 |
| VDDIO_33_PCIGP_6 | AC13 |
| VDDIO_33_PCIGP_7 | AB12 |

| Pin Name | Ball # |
|---|---|
| VDDIO_33_PCIGP_8 | AB13 |
| VDDIO_33_PCIGP_9 | AB14 |
| VDDIO_33_S_1 | N18 |
| VDDIO_33_S_2 | L19 |
| VDDIO_33_S_3 | M18 |
| VDDIO_33_S_4 | V12 |
| VDDIO_33_S_5 | V13 |
| VDDIO_33_S_6 | Y12 |
| VDDIO_33_S_7 | Y13 |
| VDDIO_33_S_8 | W11 |
| VDDIO_AZ_S | AA4 |
| VDDIO_GBE_S_1 | AA9 |
| VDDIO_GBE_S_2 | AA10 |
| VDDPL_11_DAC | V21 |
| VDDPL_11_SYS_S | J24 |
| VDDPL_33_DAC | V22 |
| VDDPL_33_ML | U22 |
| VDDPL_33_PCIE | AH29 |
| VDDPL_33_SATA | AG28 |
| VDDPL_33_SSUSB_S | L18 |
| VDDPL_33_SYS | H24 |
| VDDPL_33_USB_S | D7 |
| VDDXL_33_S | G24 |
| VGA_BLUE | M29 |
| VGA_DAC_RSET | K31 |
| VGA_DDC_SCL/ GPO71 | N32 |
| VGA_DDC_SDA/ GPO70 | M33 |
| VGA_GREEN | L32 |
| VGA_HSYNC/GPO68 | M28 |
| VGA_RED | L30 |
| VGA_VSYNC/GPO69 | N30 |
| VIN0/GPIO175 | N2 |
| VIN1/GPIO176 | M3 |
| VIN2/SDATI_1/ GPIO177 | L2 |
| VIN3/SDATO_1/ GPIO178 | N4 |
| VIN4/SLOAD_1/ GPIO179 | P1 |
| VIN5/SCLK_1/GPIO180 | P3 |
| VIN6/GBE_STAT3/ GPIO181 | M1 |
| VIN7/GBE_LED3/ GPIO182 | M5 |
| VSS | A3 |

| Pin Name | Ball # |
|---|---|
| VSS | A33 |
| VSS | AA12 |
| VSS | AA13 |
| VSS | AA14 |
| VSS | AA16 |
| VSS | AA17 |
| VSS | AA25 |
| VSS | AA28 |
| VSS | AA30 |
| VSS | AA32 |
| VSS | AA6 |
| VSS | AB25 |
| VSS | AC18 |
| VSS | AC28 |
| VSS | AC6 |
| VSS | AD27 |
| VSS | AE15 |
| VSS | AE21 |
| VSS | AE28 |
| VSS | AE6 |
| VSS | AF12 |
| VSS | AF16 |
| VSS | AF33 |
| VSS | AF8 |
| VSS | AG30 |
| VSS | AG32 |
| VSS | AH11 |
| VSS | AH18 |
| VSS | AH19 |
| VSS | AH21 |
| VSS | AH23 |
| VSS | AH25 |
| VSS | AH27 |
| VSS | AH5 |
| VSS | AJ18 |
| VSS | AJ28 |
| VSS | AJ29 |
| VSS | AK21 |
| VSS | AK25 |
| VSS | AL18 |
| VSS | AM21 |
| VSS | AM25 |
| VSS | AN1 |
| VSS | AN18 |
| VSS | AN28 |
| VSS | AN33 |

| Pin Name | Ball # |
|---|---|
| VSS | B13 |
| VSS | B7 |
| VSS | D13 |
| VSS | D9 |
| VSS | E12 |
| VSS | E16 |
| VSS | E29 |
| VSS | E5 |
| VSS | F11 |
| VSS | F13 |
| VSS | F16 |
| VSS | F17 |
| VSS | F19 |
| VSS | F23 |
| VSS | F25 |
| VSS | F29 |
| VSS | F7 |
| VSS | F9 |
| VSS | G16 |
| VSS | G32 |
| VSS | G6 |
| VSS | H12 |
| VSS | H15 |
| VSS | H29 |
| VSS | J10 |
| VSS | J13 |
| VSS | J28 |
| VSS | J32 |
| VSS | J6 |
| VSS | J9 |
| VSS | K16 |
| VSS | K27 |
| VSS | K28 |
| VSS | K7 |
| VSS | L12 |
| VSS | L13 |
| VSS | L15 |
| VSS | L16 |
| VSS | L21 |
| VSS | L6 |
| VSS | M13 |
| VSS | M16 |
| VSS | M21 |
| VSS | M25 |
| VSS | N11 |
| VSS | N13 |

| Pin Name | Ball # |
|---|---|
| VSS | N23 |
| VSS | N24 |
| VSS | N6 |
| VSS | P12 |
| VSS | P18 |
| VSS | P20 |
| VSS | P21 |
| VSS | P31 |
| VSS | P33 |
| VSS | R11 |
| VSS | R25 |
| VSS | R28 |
| VSS | R4 |
| VSS | R6 |
| VSS | T11 |
| VSS | T16 |
| VSS | T18 |
| VSS | T25 |
| VSS | T27 |
| VSS | U14 |
| VSS | U17 |
| VSS | U20 |
| VSS | U21 |
| VSS | U30 |
| VSS | U32 |
| VSS | U6 |
| VSS | V11 |
| VSS | V16 |
| VSS | V18 |
| VSS | W25 |
| VSS | W28 |
| VSS | W4 |
| VSS | W6 |
| VSS | Y14 |
| VSS | Y16 |
| VSS | Y18 |
| VSSAN_DAC | L28 |
| VSSAN_HWM | N8 |
| VSSANQ_DAC | K33 |
| VSSIO_DAC | N28 |
| VSSPL_DAC | T21 |
| VSSPL_SYS | H25 |
| VSSXL | K25 |
| WAKE#/GEVENT8# | K1 |
| WD_PWRGD | AF19 |

# A.2 Pin List by Ball Number

**Table A-2 Pin List by Ball Number**

| Ball # | Pin Name |
|---|---|
| A10 | USB_HSD7N |
| A12 | USB_SS_RX3N |
| A14 | USB_SS_TX3P |
| A16 | USBSS_CALRN |
| A18 | KSO_12/GPIO221 |
| A20 | KSO_5/GPIO214 |
| A22 | KSO_3/GPIO212 |
| A24 | KSO_16/XDB2/ GPIO225 |
| A26 | LAD2 |
| A28 | NC3 |
| A29 | LAD3 |
| A3 | VSS |
| A31 | LFRAME# |
| A33 | VSS |
| A5 | USB_HSD2N |
| A6 | USB_HSD3N |
| A8 | USB_HSD5P |
| AA10 | VDDIO_GBE_S_2 |
| AA11 | VDDCR_11_GBE_S_2 |
| AA12 | VSS |
| AA13 | VSS |
| AA14 | VSS |
| AA16 | VSS |
| AA17 | VSS |
| AA18 | VDDAN_11_SATA_8 |
| AA2 | AZ_SDIN0/GPIO167 |
| AA20 | VDDAN_11_SATA_7 |
| AA21 | VDDAN_11_SATA_1 |
| AA22 | VDDAN_11_PCIE_6 |
| AA23 | GPP_TX3N |
| AA24 | GPP_TX3P |
| AA25 | VSS |
| AA26 | GPP_RX0N |
| AA27 | GPP_RX0P |
| AA28 | VSS |
| AA30 | VSS |
| AA32 | VSS |
| AA4 | VDDIO_AZ_S |
| AA6 | VSS |
| AA7 | GBE_PHY_RST# |

| Ball # | Pin Name |
|---|---|
| AA8 | GBE_STAT0/ GEVENT11# |
| AA9 | VDDIO_GBE_S_1 |
| AB1 | AZ_SDOUT |
| AB10 | VDDIO_33_GBE_S |
| AB11 | VDDCR_11_GBE_S_1 |
| AB12 | VDDIO_33_PCIGP_7 |
| AB13 | VDDIO_33_PCIGP_8 |
| AB14 | VDDIO_33_PCIGP_9 |
| AB16 | VDDIO_33_PCIGP_10 |
| AB17 | VDDIO_33_PCIGP_1 |
| AB18 | VDDIO_33_PCIGP_2 |
| AB20 | VDDAN_11_SATA_9 |
| AB21 | VDDAN_11_SATA_2 |
| AB22 | VDDAN_11_SATA_3 |
| AB23 | VDDAN_11_PCIE_5 |
| AB24 | VDDAN_11_PCIE_1 |
| AB25 | VSS |
| AB26 | GPP_TX2P |
| AB27 | GPP_TX2N |
| AB28 | UMI_RX1P |
| AB29 | UMI_RX1N |
| AB3 | AZ_BITCLK |
| AB31 | UMI_RX0N |
| AB33 | UMI_RX0P |
| AB5 | PCIRST# |
| AB6 | PCIE_RST2#/ GEVENT4# |
| AB7 | GBE_TXCLK |
| AB8 | GBE_RXCLK |
| AB9 | GBE_TXCTL/TXEN |
| AC12 | AD24/GPIO24 |
| AC13 | VDDIO_33_PCIGP_6 |
| AC15 | AD30/GPIO30 |
| AC16 | INTG#/GPIO34 |
| AC18 | VSS |
| AC19 | VDDAN_11_SATA_10 |
| AC2 | GBE_PHY_PD |
| AC21 | VDDAN_11_SATA_6 |
| AC22 | VDDAN_11_SATA_5 |
| AC28 | VSS |
| AC30 | UMI_TX3P |
| AC32 | UMI_TX3N |
| AC4 | GBE_COL |
| AC6 | VSS |
| AD1 | GBE_RXERR |

| Ball # | Pin Name |
|---|---|
| AD10 | VDDIO_33_PCIGP_4 |
| AD12 | CBE3# |
| AD13 | GNT1#/GPO44 |
| AD15 | AD29/GPIO29 |
| AD16 | GNT0# |
| AD18 | INTH#/GPIO35 |
| AD19 | CLKRUN# |
| AD21 | GNT2#/SD_LED/ GPO45 |
| AD22 | SATA_ACT#/GPIO67 |
| AD24 | VDDAN_11_PCIE_4 |
| AD25 | SDA0/GPIO47 |
| AD26 | SCL0/GPIO43 |
| AD27 | VSS |
| AD28 | UMI_TX2P |
| AD29 | UMI_TX2N |
| AD3 | GBE_CRS |
| AD31 | UMI_TX1N |
| AD33 | UMI_TX1P |
| AD5 | A_RST# |
| AD6 | AZ_SYNC |
| AD7 | GBE_RXD0 |
| AD8 | GBE_TXD0 |
| AD9 | GBE_MDCK |
| AE10 | PAR |
| AE12 | AD23/GPIO23 |
| AE13 | AD25/GPIO25 |
| AE15 | VSS |
| AE16 | AD31/GPIO31 |
| AE18 | INTF#/GPIO33 |
| AE19 | SERIRQ/GPIO48 |
| AE2 | PCIE_RST# |
| AE21 | VSS |
| AE22 | GA20IN/GEVENT0# |
| AE24 | CLK_REQ3#/ SATA_IS1#/GPIO63 |
| AE25 | VDDAN_11_PCIE_3 |
| AE26 | SMARTVOLT1/ SATA_IS2#/GPIO50 |
| AE27 | LDRQ1#/CLK_REQ6#/ GPIO49 |
| AE28 | VSS |
| AE30 | UMI_TX0P |
| AE32 | UMI_TX0N |
| AE4 | AZ_RST# |
| AE6 | VSS |

| Ball # | Pin Name |
|---|---|
| AE7 | GBE_RXD1 |
| AE8 | GBE_TXD1 |
| AE9 | VDDIO_33_PCIGP_3 |
| AF1 | PCICLK1/GPO36 |
| AF10 | TRDY# |
| AF12 | VSS |
| AF13 | AD26/GPIO26 |
| AF15 | REQ2#/CLK_REQ8#/ GPIO41 |
| AF16 | VSS |
| AF18 | INTE#/GPIO32 |
| AF19 | WD_PWRGD |
| AF21 | SATA_X1 |
| AF22 | CLK_REQ0#/ SATA_IS3#/GPIO60 |
| AF24 | SPKR/GPIO66 |
| AF25 | CLK_REQG#/GPIO65/ OSCIN/IDLEEXIT# |
| AF26 | VDDAN_11_PCIE_7 |
| AF27 | SATA_CALRN |
| AF28 | SATA_CALRP |
| AF29 | PCIE_CALRP |
| AF3 | PCICLK0 |
| AF31 | PCIE_CALRN |
| AF33 | VSS |
| AF5 | PCICLK2/GPO37 |
| AF6 | PCICLK4/14M_OSC/ GPO39 |
| AF7 | GBE_RXD2 |
| AF8 | VSS |
| AF9 | GBE_TXD3 |
| AG10 | FRAME# |
| AG12 | AD22/GPIO22 |
| AG13 | REQ1#/GPIO40 |
| AG15 | REQ0# |
| AG16 | NC1 |
| AG18 | SATA_IS5#/FANIN3/ GPIO59 |
| AG19 | KBRST#/GEVENT1# |
| AG2 | PCICLK3/GPO38 |
| AG21 | SATA_X2 |
| AG22 | CLK_REQ1#/ FANOUT4/GPIO61 |
| AG24 | CLK_REQ4#/ SATA_IS0#/GPIO64 |
| AG25 | CLK_REQ2#/FANIN4/ GPIO62 |

| Ball # | Pin Name |
|---|---|
| AG26 | SMARTVOLT2/ SHUTDOWN#/GPIO51 |
| AG27 | VDDAN_11_PCIE_8 |
| AG28 | VDDPL_33_SATA |
| AG30 | VSS |
| AG32 | VSS |
| AG4 | AD2/GPIO2 |
| AG6 | GBE_TXD2 |
| AG7 | VDDIO_33_PCIGP_5 |
| AG8 | GBE_RXCTL/RXDV |
| AG9 | AD16/GPIO16 |
| AH1 | STOP# |
| AH10 | NC2 |
| AH11 | VSS |
| AH12 | SD_WP/GPIO76 |
| AH13 | AD27/GPIO27 |
| AH14 | AD28/GPIO28 |
| AH15 | SD_DATA2/GPIO79 |
| AH16 | FANOUT0/GPIO52 |
| AH17 | SATA_IS4#/FANOUT3/ GPIO55 |
| AH18 | VSS |
| AH19 | VSS |
| AH20 | SATA_RX1N |
| AH21 | VSS |
| AH22 | SATA_TX2N |
| AH23 | VSS |
| AH24 | SATA_TX3P |
| AH25 | VSS |
| AH26 | SATA_RX4P |
| AH27 | VSS |
| AH29 | VDDPL_33_PCIE |
| AH3 | AD4/GPIO4 |
| AH31 | NC11 (D3 only) |
| AH31 | SATA_TX7N |
| AH33 | NC10 (D3 only) |
| AH33 | SATA_TX7P |
| AH5 | VSS |
| AH7 | GBE_RXD3 |
| AH8 | SERR# |
| AH9 | LOCK# |
| AJ1 | AD9/GPIO9 |
| AJ10 | AD18/GPIO18 |
| AJ12 | SD_CD#/GPIO75 |
| AJ14 | SD_DATA3/GPIO80 |
| AJ16 | FANOUT2/GPIO54 |

| Ball # | Pin Name |
|---|---|
| AJ18 | VSS |
| AJ20 | SATA_RX1P |
| AJ22 | SATA_TX2P |
| AJ24 | SATA_TX3N |
| AJ26 | SATA_RX4N |
| AJ28 | VSS |
| AJ29 | VSS |
| AJ3 | AD0/GPIO0 |
| AJ31 | NC13 (D3 only) |
| AJ31 | SATA_RX7P |
| AJ33 | NC12 (D3 only) |
| AJ33 | SATA_RX7N |
| AJ5 | AD5/GPIO5 |
| AJ6 | AD13/GPIO13 |
| AJ8 | CBE1# |
| AK11 | AD20/GPIO20 |
| AK13 | SD_DATA0/SDATI_0/ GPIO77 |
| AK15 | FANIN0/GPIO56 |
| AK17 | GNT3#/CLK_REQ7#/ SATA_IS7#/GPIO46 (Note: SATA_IS7# applies to |
| AK19 | SATA_TX0P |
| AK21 | VSS |
| AK23 | SATA_RX2P |
| AK25 | VSS |
| AK27 | SATA_RX5N |
| AK7 | AD14/GPIO14 |
| AK9 | DEVSEL# |
| AL1 | AD6/GPIO6 |
| AL10 | IRDY# |
| AL12 | AD19/GPIO19 |
| AL14 | SD_CLK/SCLK_0/ GPIO73 |
| AL16 | FANIN2/GPIO58 |
| AL18 | VSS |
| AL20 | SATA_RX0N |
| AL22 | SATA_TX1N |
| AL24 | SATA_RX3P |
| AL26 | SATA_TX4P |
| AL28 | SATA_TX5N |
| AL29 | NC6 (D3 only) |
| AL29 | SATA_TX6P |
| AL3 | AD11/GPIO11 |
| AL31 | NC8 (D3 only) |
| AL31 | SATA_RX6N |

| Ball # | Pin Name |
|---|---|
| AL33 | NC9 (D3 only) |
| AL33 | SATA_RX6P ( |
| AL5 | AD1/GPIO1 |
| AL6 | AD3/GPIO3 |
| AL8 | AD10/GPIO10 |
| AM11 | AD17/GPIO17 |
| AM13 | SD_DATA1/SDATO_0/ GPIO78 |
| AM15 | FANOUT1/GPIO53 |
| AM17 | REQ3#/CLK_REQ5#/ SATA_IS6#/GPIO42 |
| AM19 | SATA_TX0N |
| AM21 | VSS |
| AM23 | SATA_RX2N |
| AM25 | VSS |
| AM27 | SATA_RX5P |
| AM7 | AD12/GPIO12 |
| AM9 | PERR# |
| AN1 | VSS |
| AN10 | CBE2# |
| AN12 | AD21/GPIO21 |
| AN14 | SD_CMD/SLOAD_0/ GPIO74 |
| AN16 | FANIN1/GPIO57 |
| AN18 | VSS |
| AN20 | SATA_RX0P |
| AN22 | SATA_TX1P |
| AN24 | SATA_RX3N |
| AN26 | SATA_TX4N |
| AN28 | VSS |
| AN29 | SATA_TX5P |
| AN3 | CBE0# |
| AN31 | NC7 (D3 only) |
| AN31 | SATA_TX6N |
| AN33 | VSS |
| AN5 | AD7/GPIO7 |
| AN6 | AD8/GPIO8 |
| AN8 | AD15/GPIO15 |
| B11 | USB_HSD9P |
| B13 | VSS |
| B15 | USB_SS_TX2N |
| B17 | KSO_15/XDB1/ GPIO224 |
| B19 | KSO_14/XDB0/ GPIO223 |
| B21 | KSO_9/GPIO218 |

| Ball # | Pin Name |
|---|---|
| B23 | KSI_5/GPIO206 |
| B25 | LPCCLK0 |
| B27 | LDRQ0# |
| B7 | VSS |
| B9 | USB_RCOMP |
| C1 | USB_HSD1P |
| C10 | USB_HSD7P |
| C12 | USB_SS_RX3P |
| C14 | USB_SS_TX3N |
| C16 | USBSS_CALRP |
| C18 | KSO_13/GPIO222 |
| C20 | PS2KB_CLK/GPIO190 |
| C22 | PS2M_CLK/GPIO192 |
| C24 | KSI_6/GPIO207 |
| C26 | LPC_SMI#/ GEVENT23# |
| C28 | LAD1 |
| C29 | ML_VGA_HPD/ GPIO229 |
| C3 | USB_HSD1N |
| C31 | 25M_X1 |
| C33 | 25M_X2 |
| C5 | USB_HSD2P |
| C6 | USB_HSD3P |
| C8 | USB_HSD5N |
| D11 | USB_HSD9N |
| D13 | VSS |
| D15 | USB_SS_TX2P |
| D17 | KSO_17/XDB3/ GPIO226 |
| D19 | KSO_11/GPIO220 |
| D21 | PS2KB_DAT/GPIO189 |
| D23 | PS2M_DAT/GPIO191 |
| D25 | LPCCLK1 |
| D27 | LAD0 |
| D7 | VDDPL_33_USB_S |
| D9 | VSS |
| E1 | USB_HSD0P |
| E10 | USB_HSD8P |
| E12 | VSS |
| E14 | USB_SS_RX2P |
| E16 | VSS |
| E18 | KSO_4/GPIO213 |
| E20 | KSO_1/GPIO210 |
| E22 | EC_PWM0/ EC_TIMER0/GPIO197 |

| Ball # | Pin Name |
|---|---|
| E24 | KSI_4/GPIO205 |
| E26 | APU_PG |
| E28 | PROCHOT# |
| E29 | VSS |
| E3 | USB_HSD0N |
| E31 | GPP_CLK3N |
| E33 | GPP_CLK3P |
| E5 | VSS |
| E6 | VDDBT_RTC_G |
| E8 | USB_HSD4N |
| F1 | RTCCLK |
| F10 | USB_HSD8N |
| F11 | VSS |
| F12 | USB_HSD11N |
| F13 | VSS |
| F14 | USB_SS_RX2N |
| F15 | USB_SS_TX1P |
| F16 | VSS |
| F17 | VSS |
| F18 | KSI_7/GPIO208 |
| F19 | VSS |
| F20 | KSO_2/GPIO211 |
| F21 | KSO_0/GPIO209 |
| F22 | KSI_2/GPIO203 |
| F23 | VSS |
| F24 | KSI_3/GPIO204 |
| F25 | VSS |
| F26 | APU_RST# |
| F27 | CLK_CALRN |
| F29 | VSS |
| F3 | INTRUDER_ALERT# |
| F31 | GPP_CLK2N |
| F33 | GPP_CLK2P |
| F5 | USB_OC3#/AC_PRES/ TDO/GEVENT15# |
| F7 | VSS |
| F8 | USB_HSD4P |
| F9 | VSS |
| G10 | USB_HSD13N |
| G12 | USB_HSD11P |
| G13 | USB_SS_RX1N |
| G15 | USB_SS_TX1N |
| G16 | VSS |
| G18 | KSO_8/GPIO217 |
| G19 | SDA2/GPIO194 |
| G2 | 32K_X1 |

| Ball # | Pin Name |
|---|---|
| G21 | SDA3_LV/GPIO196 |
| G22 | SCL3_LV/GPIO195 |
| G24 | VDDXL_33_S |
| G25 | DMA_ACTIVE# |
| G26 | LDT_STP# |
| G27 | NC4 |
| G28 | PCIE_RCLKN |
| G30 | PCIE_RCLKP |
| G32 | VSS |
| G4 | 32K_X2 |
| G6 | VSS |
| G7 | VDDAN_33_USB_S_1 |
| G8 | USBCLK/ 14M_25M_48M_OSC |
| G9 | USB_HSD6N |
| H1 | USB_FSD1P/GPIO186 |
| H10 | USB_HSD13P |
| H12 | VSS |
| H13 | USB_SS_RX1P |
| H15 | VSS |
| H16 | USB_SS_TX0N |
| H18 | KSO_7/GPIO216 |
| H19 | SCL2/GPIO193 |
| H21 | EC_PWM3/ EC_TIMER3/GPIO200 |
| H22 | EC_PWM1/ EC_TIMER1/GPIO198 |
| H24 | VDDPL_33_SYS |
| H25 | VSSPL_SYS |
| H26 | VDDAN_11_CLK_1 |
| H27 | GPP_CLK0P |
| H28 | GPP_CLK0N |
| H29 | VSS |
| H3 | USB_FSD1N |
| H31 | DISP2_CLKN |
| H33 | DISP2_CLKP |
| H5 | USB_FSD0N |
| H6 | USB_FSD0P/GPIO185 |
| H7 | S5_CORE_EN |
| H8 | VDDAN_33_USB_S_2 |
| H9 | USB_HSD6P |
| J10 | VSS |
| J12 | USB_HSD12N |
| J13 | VSS |
| J15 | USB_SS_RX0P |
| J16 | USB_SS_TX0P |

| Ball # | Pin Name |
|---|---|
| J18 | KSO_6/GPIO215 |
| J19 | PS2_CLK/SCL4/ GPIO188 |
| J2 | IR_LED#/LLB#/ GPIO184 |
| J21 | SPI_CS2#/ GBE_STAT2/GPIO166 |
| J22 | EC_PWM2/ EC_TIMER2/WOL_EN/ GPIO199 |
| J24 | VDDPL_11_SYS_S |
| J25 | VDDAN_11_CLK_2 |
| J26 | 14M_25M_48M_OSC |
| J27 | GPP_CLK1P |
| J28 | VSS |
| J30 | SLT_GFX_CLKP |
| J32 | VSS |
| J4 | PWR_BTN# |
| J6 | VSS |
| J7 | USB_OC1#/TDI/ GEVENT13# |
| J8 | VDDAN_33_USB_S_3 |
| J9 | VSS |
| K1 | WAKE#/GEVENT8# |
| K10 | USB_HSD12P |
| K12 | USB_HSD10P |
| K13 | USB_HSD10N |
| K15 | USB_SS_RX0N |
| K16 | VSS |
| K18 | KSO_10/GPIO219 |
| K19 | PS2_DAT/SDA4/ GPIO187 |
| K21 | KSI_0/GPIO201 |
| K22 | KSI_1/GPIO202 |
| K24 | VDDAN_11_CLK_3 |
| K25 | VSSXL |
| K26 | GPP_CLK1N |
| K27 | VSS |
| K28 | VSS |
| K29 | SLT_GFX_CLKN |
| K3 | TEMPIN2/GPIO173 |
| K31 | VGA_DAC_RSET |
| K33 | VSSANQ_DAC |
| K5 | TEMPIN1/GPIO172 |
| K6 | TEMPIN0/GPIO171 |
| K7 | VSS |
| K8 | VDDAN_33_USB_S_4 |

| Ball # | Pin Name |
|---|---|
| K9 | VDDAN_33_USB_S_5 |
| L12 | VSS |
| L13 | VSS |
| L15 | VSS |
| L16 | VSS |
| L18 | VDDPL_33_SSUSB_S |
| L19 | VDDIO_33_S_2 |
| L2 | VIN2/SDATI_1/ GPIO177 |
| L21 | VSS |
| L22 | VDDAN_11_CLK_4 |
| L28 | VSSAN_DAC |
| L30 | VGA_RED |
| L32 | VGA_GREEN |
| L4 | NC5 |
| L6 | VSS |
| M1 | VIN6/GBE_STAT3/ GPIO181 |
| M10 | VDDAN_33_USB_S_7 |
| M11 | VDDAN_33_USB_S_12 |
| M12 | VDDAN_33_USB_S_10 |
| M13 | VSS |
| M14 | VDDAN_11_SSUSB_S _2 |
| M16 | VSS |
| M17 | VDDCR_11_SSUSB_S _4 |
| M18 | VDDIO_33_S_3 |
| M20 | VDDCR_11_S_2 |
| M21 | VSS |
| M22 | VDDAN_11_CLK_5 |
| M23 | GPP_CLK4P |
| M24 | GPP_CLK4N |
| M25 | VSS |
| M26 | GPP_CLK5N |
| M27 | GPP_CLK5P |
| M28 | VGA_HSYNC/GPO68 |
| M29 | VGA_BLUE |
| M3 | VIN1/GPIO176 |
| M31 | LDO_CAP |
| M33 | VGA_DDC_SDA/ GPO70 |
| M5 | VIN7/GBE_LED3/ GPIO182 |
| M6 | TEMPIN3/TALERT#/ GPIO174 |

| Ball # | Pin Name |
|---|---|
| M7 | BLINK/USB_OC7#/ GEVENT18# |
| M8 | VDDAN_33_HWM_S |
| M9 | VDDAN_33_USB_S_6 |
| N10 | VDDAN_33_USB_S_9 |
| N11 | VSS |
| N12 | VDDAN_33_USB_S_11 |
| N13 | VSS |
| N14 | VDDAN_11_SSUSB_S_3 |
| N16 | VDDCR_11_SSUSB_S_1 |
| N17 | VDDCR_11_SSUSB_S_2 |
| N18 | VDDIO_33_S_1 |
| N2 | VIN0/GPIO175 |
| N20 | VDDCR_11_S_1 |
| N21 | VDDAN_11_CLK_6 |
| N22 | VDDAN_11_CLK_7 |
| N23 | VSS |
| N24 | VSS |
| N25 | GPP_CLK6P |
| N26 | GPP_CLK6N |
| N27 | GPP_CLK8P |
| N28 | VSSIO_DAC |
| N30 | VGA_VSYNC/GPO69 |
| N32 | VGA_DDC_SCL/ GPO71 |
| N4 | VIN3/SDATO_1/ GPIO178 |
| N6 | VSS |
| N7 | PWR_GOOD |
| N8 | VSSAN_HWM |
| N9 | VDDAN_33_USB_S_8 |
| P1 | VIN4/SLOAD_1/ GPIO179 |
| P12 | VSS |
| P13 | VDDAN_11_SSUSB_S_4 |
| P14 | VDDAN_11_SSUSB_S_5 |
| P16 | VDDAN_11_SSUSB_S_1 |
| P17 | VDDCR_11_SSUSB_S_3 |
| P18 | VSS |
| P20 | VSS |

| Ball # | Pin Name |
|---|---|
| P21 | VSS |
| P22 | VDDAN_11_CLK_8 |
| P28 | ML_VGA_L3N |
| P29 | ML_VGA_L3P |
| P3 | VIN5/SCLK_1/GPIO180 |
| P31 | VSS |
| P33 | VSS |
| P5 | USB_OC2#/TCK/ GEVENT14# |
| P6 | USB_OC4#/IR_RX0/ GEVENT16# |
| R10 | THRMTRIP#/ SMBALERT#/ GEVENT2# |
| R11 | VSS |
| R2 | RI#/GEVENT22# |
| R23 | GPP_CLK7P |
| R24 | GPP_CLK7N |
| R25 | VSS |
| R26 | DISP_CLKP |
| R27 | GPP_CLK8N |
| R28 | VSS |
| R30 | ML_VGA_L2N |
| R32 | ML_VGA_L2P |
| R4 | VSS |
| R6 | VSS |
| R7 | SDA1/GPIO228 |
| R8 | USB_OC6#/IR_TX1/ GEVENT6# |
| R9 | PME#/GEVENT3# |
| T1 | USB_OC5#/IR_TX0/ GEVENT17# |
| T10 | TEST1/TMS |
| T11 | VSS |
| T12 | VDDCR_11_USB_S_1 |
| T13 | VDDCR_11_USB_S_2 |
| T14 | VDDCR_11_1 |
| T16 | VSS |
| T17 | VDDCR_11_2 |
| T18 | VSS |
| T20 | VDDCR_11_3 |
| T21 | VSSPL_DAC |
| T22 | VDDAN_33_DAC |
| T23 | APU_CLKN |
| T24 | APU_CLKP |
| T25 | VSS |
| T26 | DISP_CLKN |

| Ball # | Pin Name |
|---|---|
| T27 | VSS |
| T28 | ML_VGA_L1N |
| T29 | ML_VGA_L1P |
| T3 | SLP_S3# |
| T31 | ML_VGA_L0P |
| T33 | ML_VGA_L0N |
| T5 | LPC_PD#/GEVENT5# |
| T6 | SPI_CS1#/GPIO165 |
| T7 | SCL1/GPIO227 |
| T8 | USB_OC0#/ GEVENT12#/TRST |
| T9 | TEST0 |
| U12 | VDDAN_11_USB_S_1 |
| U13 | VDDAN_11_USB_S_2 |
| U14 | VSS |
| U16 | VDDCR_11_4 |
| U17 | VSS |
| U18 | VDDCR_11_5 |
| U2 | RSMRST# |
| U20 | VSS |
| U21 | VSS |
| U22 | VDDPL_33_ML |
| U28 | AUXCAL |
| U30 | VSS |
| U32 | VSS |
| U4 | SYS_RESET#/ GEVENT19# |
| U6 | VSS |
| V1 | ROM_RST#/SPI_WP#/ GPIO161 |
| V10 | GBE_LED2/ GEVENT10# |
| V11 | VSS |
| V12 | VDDIO_33_S_4 |
| V13 | VDDIO_33_S_5 |
| V14 | VDDCR_11_6 |
| V16 | VSS |
| V17 | VDDCR_11_7 |
| V18 | VSS |
| V20 | VDDCR_11_8 |
| V21 | VDDPL_11_DAC |
| V22 | VDDPL_33_DAC |
| V23 | VDDAN_11_ML_2 |
| V24 | VDDAN_11_ML_3 |
| V25 | VDDAN_11_ML_4 |
| V26 | GPP_RX2P |

| Ball # | Pin Name |
|---|---|
| V27 | GPP_RX1N |
| V28 | AUX_VGA_CH_P |
| V29 | AUX_VGA_CH_N |
| V3 | SPI_CLK/GPIO162 |
| V31 | GPP_TX0N |
| V33 | GPP_TX0P |
| V5 | SPI_DO/GPIO163 |
| V6 | SPI_DI/GPIO164 |
| V7 | IR_RX1/GEVENT20# |
| V8 | DDR3_RST#/ GEVENT7#/VGA_PD |
| V9 | TEST2 |
| W10 | GBE_MDIO |
| W11 | VDDIO_33_S_8 |
| W2 | SLP_S5# |
| W23 | GPP_RX3N |
| W24 | GPP_RX3P |
| W25 | VSS |
| W26 | GPP_RX2N |
| W27 | GPP_RX1P |
| W28 | VSS |
| W30 | GPP_TX1P |
| W32 | GPP_TX1N |
| W4 | VSS |
| W6 | VSS |
| W7 | SPI_CS3#/ GBE_STAT1/ GEVENT21# |
| W8 | GBE_LED0/GPIO183 |
| W9 | GBE_PHY_INTR |
| Y1 | AZ_SDIN3/GPIO170 |
| Y12 | VDDIO_33_S_6 |
| Y13 | VDDIO_33_S_7 |
| Y14 | VSS |
| Y16 | VSS |
| Y17 | VDDCR_11_9 |
| Y18 | VSS |
| Y20 | VDDAN_11_SATA_4 |
| Y21 | VDDAN_11_PCIE_2 |
| Y22 | VDDAN_11_ML_1 |
| Y28 | UMI_RX3P |
| Y29 | UMI_RX3N |
| Y3 | AZ_SDIN2/GPIO169 |
| Y31 | UMI_RX2N |
| Y33 | UMI_RX2P |
| Y5 | AZ_SDIN1/GPIO168 |

| Ball # | Pin Name |
|---|---|
| Y6 | SPI_HOLD#/<br>GBE_LED1/GEVENT9# |