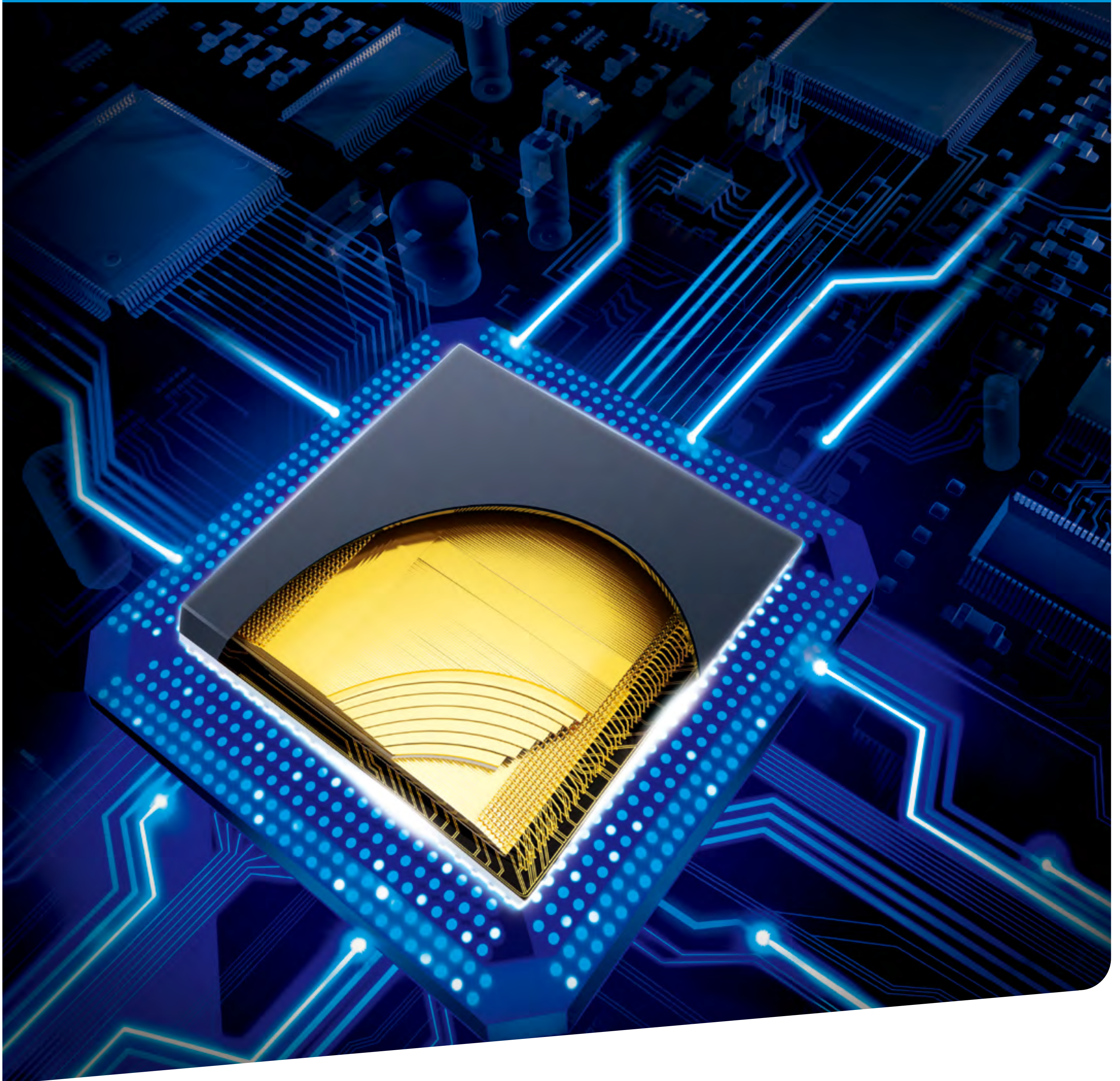
White Paper

Samsung V-NAND technology

Yield more capacity, performance, endurance and power efficiency



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Meet today's data demands with Samsung's revolutionary 3D V-NAND technology

Executive summary

The explosive worldwide growth in data traffic is pushing the limits of NAND flash memory. Current 2D planar NAND technology has intrinsic limitations, inhibiting capacity expansion without critically compromising performance and reliability. As a result of the inability of 2D planar NAND to effectively scale capacity to meet increasing data demands, new solutions must be found. Samsung has developed an innovative solution to satisfy rising data demands with its cutting-edge 3D vertical-NAND (V-NAND) flash memory technology. By stacking memory cells vertically in a three-dimensional structure, new potential for 3D memory capacities are created, eliminating performance and reliability issues from capacity limitations.

Yield superb performance and reliability with Samsung 3D V-NAND flash memory

In order to keep up with this incredible growth, a new era of flash memory is required at the datacenter level, as well as the client level. NAND flash memory is at the core of this process. From the moment the image or video is captured, then sent to the datacenter and, in turn, distributed to the millions or billions of other users, NAND flash is part of that infrastructure every step of the way.

Samsung 3D V-NAND technology delivers reliable performance at lower costs for today's demanding, data-centric world. This innovative architecture improves memory in the following essential areas:

- **More capacity.** Fit more memory cells in a NAND chip in less space for significantly more capacity
- **Better performance.** Write data much faster by virtually eliminating cell-to-cell interference
- **Outstanding endurance.** Experience less stress with insulators more resistant to wear for greater endurance
- **Superb power efficiency.** Reduce power consumption by reducing the number of programming steps

This white paper explains how Samsung 3D V-NAND flash memory differs from, and is superior to, 2D planar NAND memory.

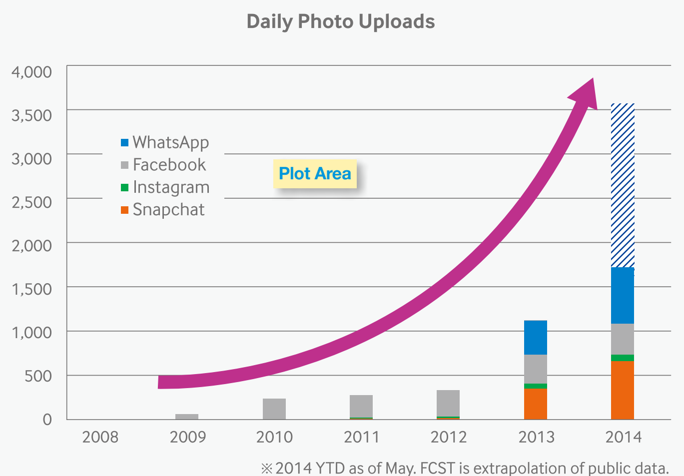
Industry trends

Right now the world is experiencing the data explosion era as larger numbers of people and devices connect to the Internet. By some predictions, the exponential growth will likely exceed 50 billion connected devices by 2020.

Mobile data traffic is also booming, growing in staggering numbers with more connections, faster speeds, more videos and more users. Social media is largely responsible for this astounding growth.

YouTube™ and social networking have turned everyone from content consumers to content creators. To put this growth into perspective, more videos are uploaded to YouTube in one month than were created by the three major networks in sixty years. WhatsApp® handles 50 billion messages per day, Twitter® experiences more than 500 million tweets per day and mobile phones are checked 100 billion times a day.

On average, in 2014, 3.6 billion photos are uploaded a day. More than 100 million selfies alone are shared every day and, when they go viral, they are causing IT challenges in moving the data around. In total, social networking activities account for 91 percent of mobile data consumption.



Figurine 1: Social media comprises 91 percent of mobile Internet access.

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Go beyond traditional planar NAND capacity with an advanced cell-stacking configuration

Discover the advantages of V-NAND compared with planar NAND

The architectural changes that have been made to Samsung V-NAND flash memory in comparison to planar NAND include tripling the number of pages and the block size. In addition, dual-page programming has been adopted to improve the program bandwidth, as well as reduce strong electron correlation effects and bit errors.

Features	21nm planar 64Gb	V1 128Gb
Voltage Supply (Typ)	VCC: 3.3V, VCCQ: 1.8V/3.3V	VCC: 3.3V, VCCQ: 1.8V only
Page Size within a Block	(8K+640) Bytes	(8K+896) Bytes
Number of Pages per Block	128 Pages	384 Pages
Block Size	(1M+80K) Bytes	(3M+336K) Bytes
Number of Planes	4	2
Page Program per Plane	(8K+640) Bytes	2 x (8K+896) Bytes[1]
Page Program Time (tPROG)	2.0ms	0.6ms
Page Read per Plane	(8K+640) Bytes	(8K+896) Bytes
Random Read Time (tR)[2]	52µs	49µs
Date Transfer Rate	400Mbps	533Mbps
Block Erase Time (tBERS)	5ms	4ms

Table 1. Key features of the 35K V-NAND flash memory versus the 10K planar flash memory
Note 1. Dual page program / Note 2. 8KB read case

In addition, the 1st Generation V-NAND technology has increased the capacity in the unit size to twice that of 21nm planar NAND. Improvements also include 24-Word Line (WL) stacked layers, 64Gb array in multiples of two planes, a one-sided page buffer equaling an 8KBx2 page size and an asynchronous double data rate (DDR) interface at a speed of 533 megabits per second (Mbps) using eight-stacked dies.

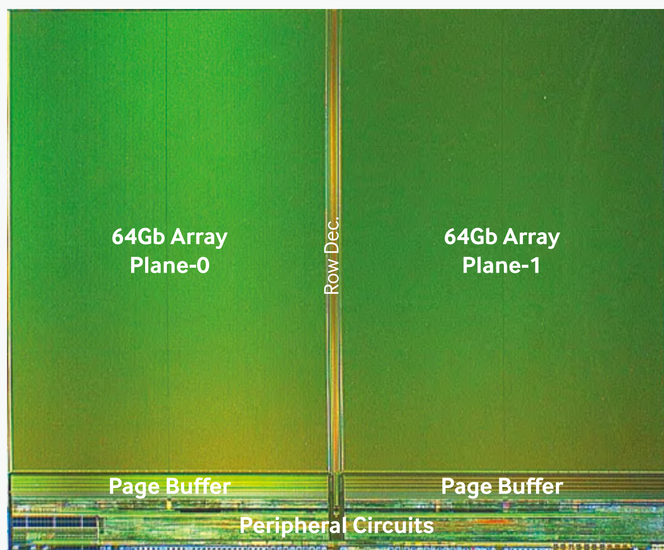

Figure 2. A die microphotograph of a 1st Generation 128Gb 2bit memory

Overcome the limitations of patterning with vertical architecture

In an effort to shrink cells to fit more cells in less space in 2D planar NAND flash memory, it becomes difficult or impossible for light to penetrate the mask to transfer the pattern to a photoresist. The reduction in light constricts the patterning process or prevents the process from taking place. This inherit obstacle limits the use of 2D planar NAND flash memory in today's demanding memory environment.

However, Samsung's 3D V-NAND design stacks cells vertically, resulting in a wider gap between each cell, overcoming patterning limitations. The cell-to-cell space in a planar 1Ynm NAND typically ranges from 15 nanometers (nm) to 16nm, but Samsung V-NAND flash has 30nm to 40nm of space between cells, creating a NAND technology breakthrough.

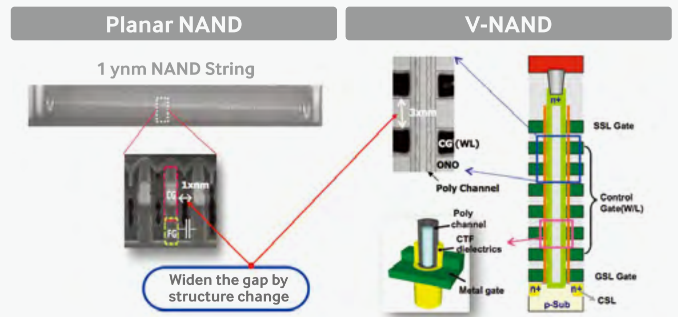

Figure 3. The V-NAND design widens the gap between cells to overcome patterning limitations and cross interference.

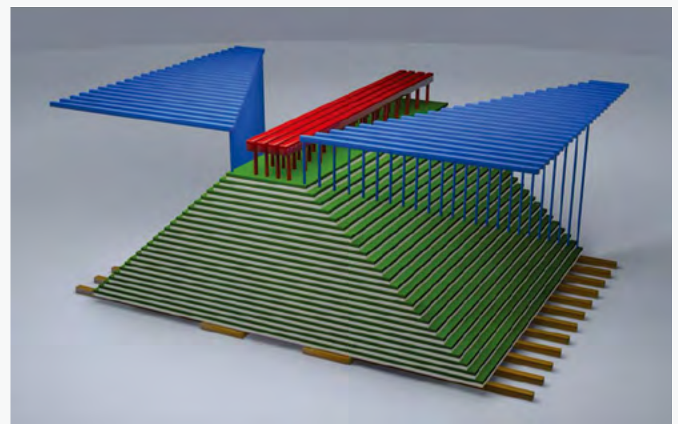

Figure 4. A bird's-eye view of the V-NAND structure

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Maximize cell density with a smaller footprint and innovative material and structure

Another technical challenge that arises from continually shrinking cells in 2D planar NAND technology is the creation of cell-to-cell interference, which leads to data corruption.
And when a cell size goes below 20nm, the chance for interference drastically increases, inevitably making the cell unreliable. Samsung has addressed that issue by adopting Charge Trap Flash (CTF) technology that results in a cell-to-cell interference-free structure.

In planar NAND memory, the cell stores the electron in the conductor. With V-NAND memory, the conductor is replaced by an insulator, which has a lower height and, thereby lowers the coupling. In addition, the V-NAND memory has a larger channel area than planar NAND memory, which improves the initial electron dispersion, creating an almost coupling-free cell structure.

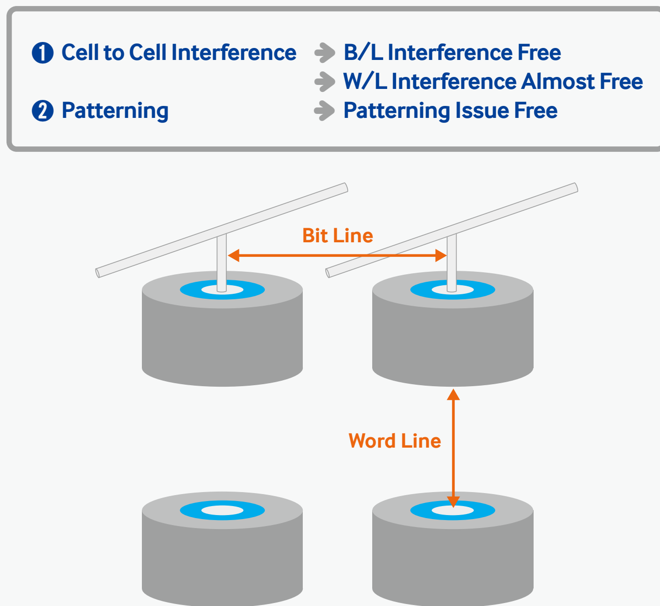
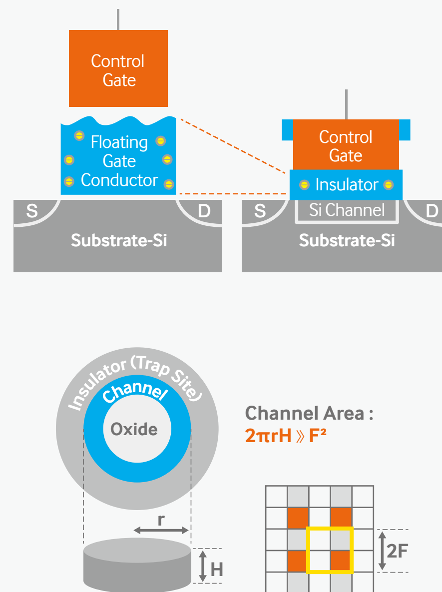


Figure 5. The V-NAND cell-to-cell interference-free structure



Realize superior cell characteristics with advanced CTF technology

Samsung's revolutionary 3D V-NAND technology features a unique design that stacks 24 layers of cells on top of one another instead of trying to decrease the cells' length and width to fit into today's ever-shrinking form factors. Using this new 3D V-NAND architecture creates two times the density of a traditional 2D planar NAND in a smaller footprint.

This innovative design eliminates pattern limitations while achieving a much larger scalable capacity to satisfy present and future data demands. 3D V-NAND's unique design is achieved by disruptive innovation of material, structure and integration.

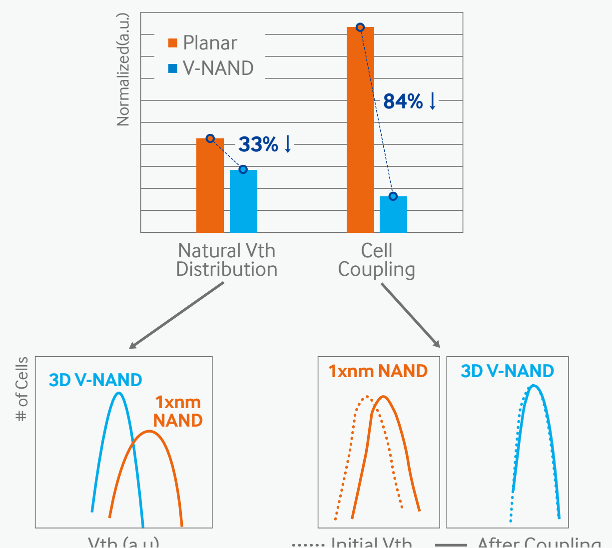


Figure 6. Cell characteristics of the V-NAND versus planar NAND memory

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Streamline page assignments and programming tasks for more efficient performance

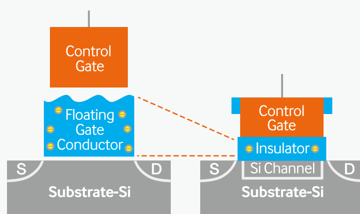
Material innovation

Using advanced CTF technology, Samsung's 3D V-NAND flash memory boasts a cell-to-cell interference-free structure. CTF technology uses a non-conductive layer of silicon nitride (SiN), which temporarily traps electrical charges to maintain cell integrity. This non-conductive layer is modified into a three-dimensional form to wrap around the control gate of the cell, acting as an insulator that holds charges to prevent data corruption caused by cell-to-cell cross interference.

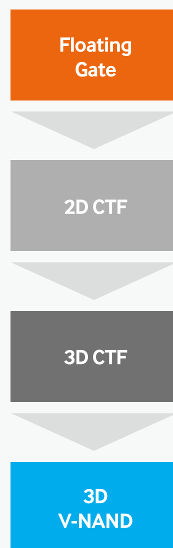
Structural innovation and integration

To create the vertical integration of 3D V-NAND cell layers, Channel Hole Technology is used. This technology enables cells to connect vertically with one another through a cylindrical channel that runs through each column of stacked cells and rotates 90 degrees. The 24-layer stacks of cells are connected to over 2 billion channel holes that are etched from the top layer of the NAND to the bottom layer. Looking from a top-down view, all the holes can be seen on a 128Gb NAND chip that is the size of a fingernail. The cylindrical channels enable seamless integration of the vertical layers of cells.

❶ Innovation Material (2003)



❷ Innovation Structure (2008)



❸ Innovation Integration (2008)

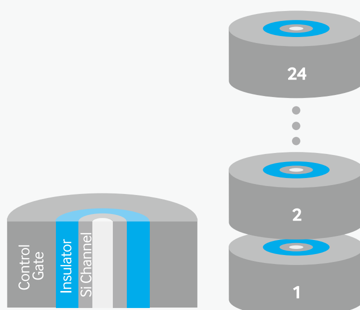


Figure 7. The disruptive innovation of structure in V-NAND flash memory

Satisfy compatibility issues with planar NAND flash memory

As stated earlier, Samsung 3D V-NAND flash memory is composed of vertically stacked cell strings as opposed to planar NAND, which is arranged in a cell string on a single plane. Although the architecture is quite different, the Samsung V-NAND flash memory page operation is compatible with existing planar flash. However, what makes V-NAND unique is that it solves the limitation issues inherent in planar flash memory. In addition, V-NAND cells can share the same Word Line (WL) and String Select Line (SSL) split.

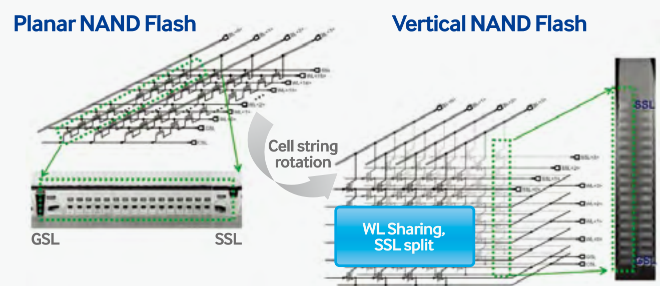


Figure 8. Cell array architecture compatibility with planar NAND

Samsung V-NAND flash has adopted sequential page assignment, eliminating the back-and-forth assignments required by planar NAND flash. Plus, program status failures do not corrupt the pages that have already been written.

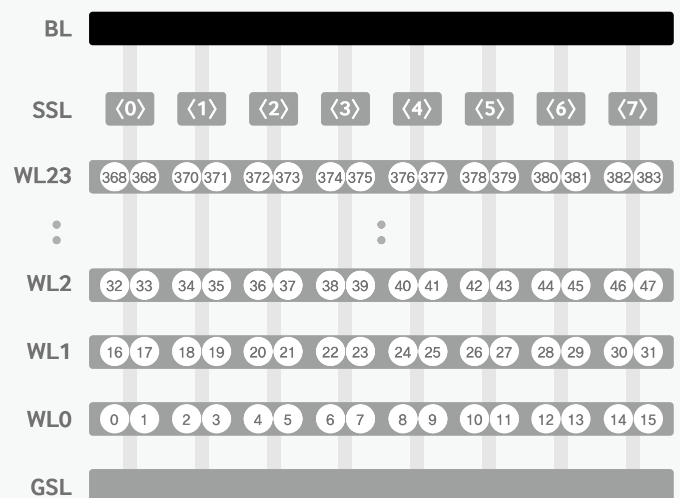


Figure 9. A 2bit page assignment

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Boost performance and endurance with Samsung 2nd Generation V-NAND memory

Program bits simultaneously for enhanced performance

Planar NAND memory must separate the program by the Least Significant Bit (LSB) and the Most Significant Bit (MSB) and operate twice. V-NAND flash, on the other hand, features a dual-page program, which has a virtually coupling-free structure. This feature enables V-NAND memory to program the bits all at once, improving the bandwidth for enhanced performance.

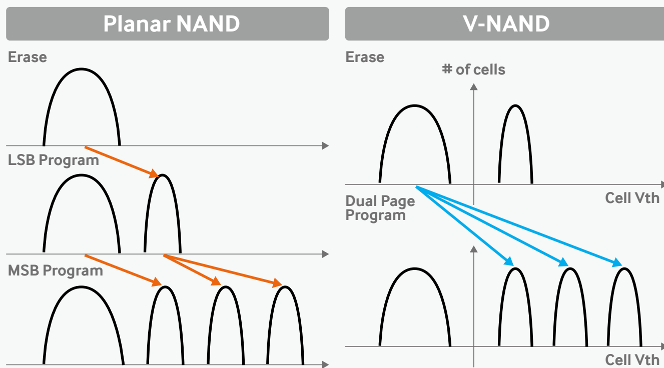


Figure 10. V-NAND dual-page programming improves program bandwidth for enhanced performance.

By programing the LSB and MSB simultaneously, programming time is significantly reduced. When compared with 21 nm planar NAND memory, Samsung V-NAND memory power consumption is substantially lowerd by up to 40 percent.

V-NAND cells are employ CTF-based insulators, enabling it to hold more electrical charges, making it more resistant to wear and reducing the risk of cell-to-cell interference. Its superb voltage distribution reduces overlaps, which directly improves the bit error rate. As a result, the V-NAND flash memory experiences less stress, thereby improving its endurance, enabling higher reliability over a longer duration than planar NAND.

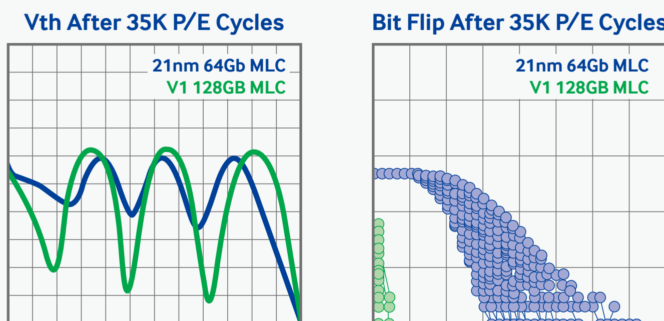
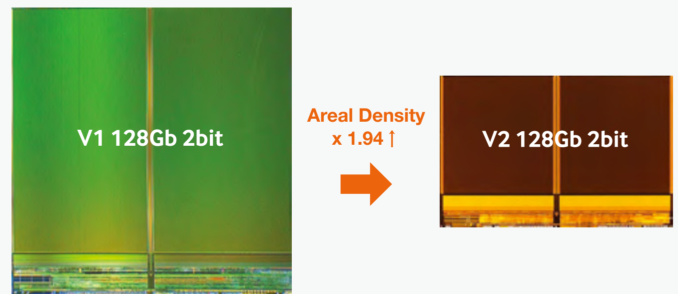


Figure 10. The endurance characteristics of V-NAND compared with 21nm planar NAND at six blocks per die.

Discover Samsung's 2nd Generation V-NAND flash memory

Samsung's revolutionary 2nd Generation 2bit 3D V-NAND technology features a unique design that stacks 32 layers of 2bit cells on top of one another instead of trying to decrease the cells' length and width to fit into technology's increasingly smaller form factors. Its page size has increased from 8K to 16K and performance is also enhanced using an improved program/read alogrithm. Using this new 3D V-NAND architecture creates much greater density compared with traditional 2D planar NAND in a smaller footprint.



Features	V1 128Gb 2bit	V2 128Gb 2bit
Voltage Supply (Typ)	VCC: 3.3V, VCCQ: 1.8V only	VCC: 3.3V, VCCQ: 1.8V only
Page Size within a Block	(8K+896) Bytes	(16K+1536) Bytes
Number of Pages per Block	384 Pages	384 Pages
Block Size	(3M+336K) Bytes	(4M+384K) Bytes
Number of Planes	2	2
Page Program per Plane	2 x (8K+896) Bytes[1]	2 x (16K+1536) Bytes[1]
Page Program Time (tPROG)	0.6ms	0.39ms
Page Read per Plane	(8K+896) Bytes	(16K+1536) Bytes
Random Read Time (tR)[2]	49μs	35μs
Date Transfer Rate	533Mbps	667Mbps
Block Erase Time (tBERS)	4ms	4ms

Table 2. The comparison between Samsung's 1st and 2nd Generation 2bit V-NAND flash memory
Note 1. Dual page program / Note 2. 8KB read case

Compared to Samsung's 2bit 32-layer V-NAND technology, the 3bit V-NAND flash has crossed the threshold of costs in dollars per gigabit by being able to store 3bits per cell over 2bits per cell. This disruptive density 3bit technology brings costs down, yet still offers better endurance for consumer and enterprise applications. By delivering cost, value and density, it enables Samsung to increase the level of support for next-generation interfaces, advancing the SSD market.

Virtually eliminate structural failures with unmatched cycle test performance results

Observe the parallels in qualification tests between V-NAND and planar NAND

When tested against the planar NAND flash, the V-NAND flash memory passed all the qualifications tests, concluding that the V-NAND tested the same as planar NAND. However, the cycle test, in particular, showed the V-NAND well surpassed the planar NAND with thirty-five thousand cycles compared with merely ten thousand cycles for the planar NAND, indicating much higher endurance.

Items	Condition	S/S	21nm 64Gb MLC	V1 128Gb MLC
Enderance	VCC=3.6V / Ta=85°C	231	18K Cycle	35K Cycle
	VCC=3.6V / Ta25°C	231		
High Temperrature Date Retention	13hr@85°C	231	Pass(@18K)	Pass(@35K)
Low Temperrature Date Retention	500hr@25°C	231	Pass(@18K)	Pass(@35K)
Read Disturb	Ta=25°C / 1E4 Times	231	Pass(@18K)	Pass(@35K)
High Temperrature Operation	Ta=125°C Dynamic Stress	1000	Pass(@168hr)	←
		387	Pass(1000hr)	←
High Temperrature Storage	Ta=150°C, Storage	231	Pass(@1000hr)	←
THB	85°C / 85%RH, 3.3V, Static Stress	116	Pass(@1000hr)	←
uHAST	130°C, 85%RH, 1atm	116	Pass(@168hr)	←
TC	-55°C~125°C Cycling	116	Pass(@1000hr)	←
Electro Static Discharge	HBM (Human Body Model)	200	>2000V Pass	←
	CDM (Charged Device Model)	40	>500V Pass	←
Latch-up	V-Test	20	>8V	←
	I-Test	60	>200mA	←

Table 3. Qualifications test results showing V-NAND equaled planar NAND, except in endurance where it excelled

There are four major structural failures that can occur in NAND flash memory, the WL to WL bridge, the WL to channel bridge, the WL to Common Source Line (CSL) bridge and the hole not open. In the WL to WL bridge failure, the mold profile becomes defective due to a particle causing the WL to WL bridge and program speed of the shortened two WLs to slow down. By improving the inner Fab (Fablication facility), the structural failure is diminished.

The WL to channel bridge failure is caused by some holes forming abnormally due to a defective photon or particles from the process. A WL to CSL bridge failure happens when the Gound Select Line (GSL) WL profiles become defective by the particle and it shortens the GSL and CSL. The fourth major structural failure can occur as the result of a defective photo or etch, which is distinguished by an abnormal Vth.

1) WL to WL Bridge

2) WL to Ch. Bridge

3) WL to CSL Bridge

Channel Holes

Figure 12. The major structural failures that can occur in NAND flash memory

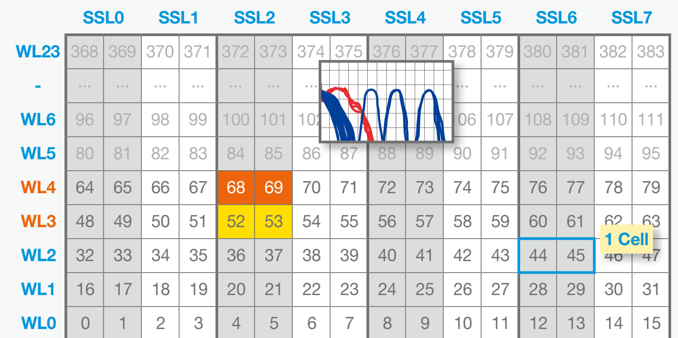


Figure 13. A WL to WL bridge status failure requiring a back-up operation to be performed on every WL

Figure 13 illustrates the WL to WL bridge that can occur between two WLs. WL 4 is bridged to WL 3 during the program operation, dropping the program level, thereby preventing the operation from completing in pages 68 and 69. As a result, a status failure occurs and victim pages 52 and 53 are disturbed, requiring a back-up operation to be performed on every WL. To prevent this failure from occuring, the WL to WL bridge occurances are screened and monitored by increasing the erase dispersion.

The String Selected line (SSL) is the same as a charge trap-based cell, therefore, there is the possibility that an SSL can accumulate or lose its charge, resulting in threshold voltage changes.

However, extensive test screening will eliminate any defects, but error prediction and data recovery tech-niques are still being developed. However, Samsung V-NAND flash memory has thoroughly screened out these failures by achieving a thirty-five thousand cycle, SSD-grade Defective Parts Per Minute (DPPM) test result.

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Improve performance and lifespan with power-efficient 3D V-NAND flash memory

Conclusion

Samsung 3D V-NAND flash memory fundamentally changes the architecture of flash memory. By vertically stacking each cell, more cells can fit within a smaller footprint for higher capacity. The block size is also larger compared with planar NAND memory, which reduces the coupling and cell-to-cell interference issues, enabling data to be written significantly faster for superb performance. Because Samsung's 3D V-NAND technology has eliminated the issue of interference, the number of programming steps has been vastly reduced. Hence, substantially lowered power consumption is achieved.

Its structural innovation also enables the adoption of the dual-page programming method for improved bandwidth and a reduction of strong electron correlation and bit errors. With the addition of CTF technology, the insulators surrounding the control gate are more resistant to wear, providing greater endurance.

V-NAND flash memory excelled in the qualifications tests when compared with planar flash memory, confirming that Samsung V-NAND provides high endurance.

Overall, Samsung 3D V-NAND flash memory delivers better performance, a longer lifespan and substantial energy savings over 2D planar NAND flash memory.

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For more information

For more information about the Samsung 3D V-NAND flash memory, visit www.samsung.com/semiconductor/ssd

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Samsung Electronics Co., Ltd.
416, Maetan 3-dong, Yeongtong-gu, Suwon-si, Gyeonggi-do 443-772, Korea

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