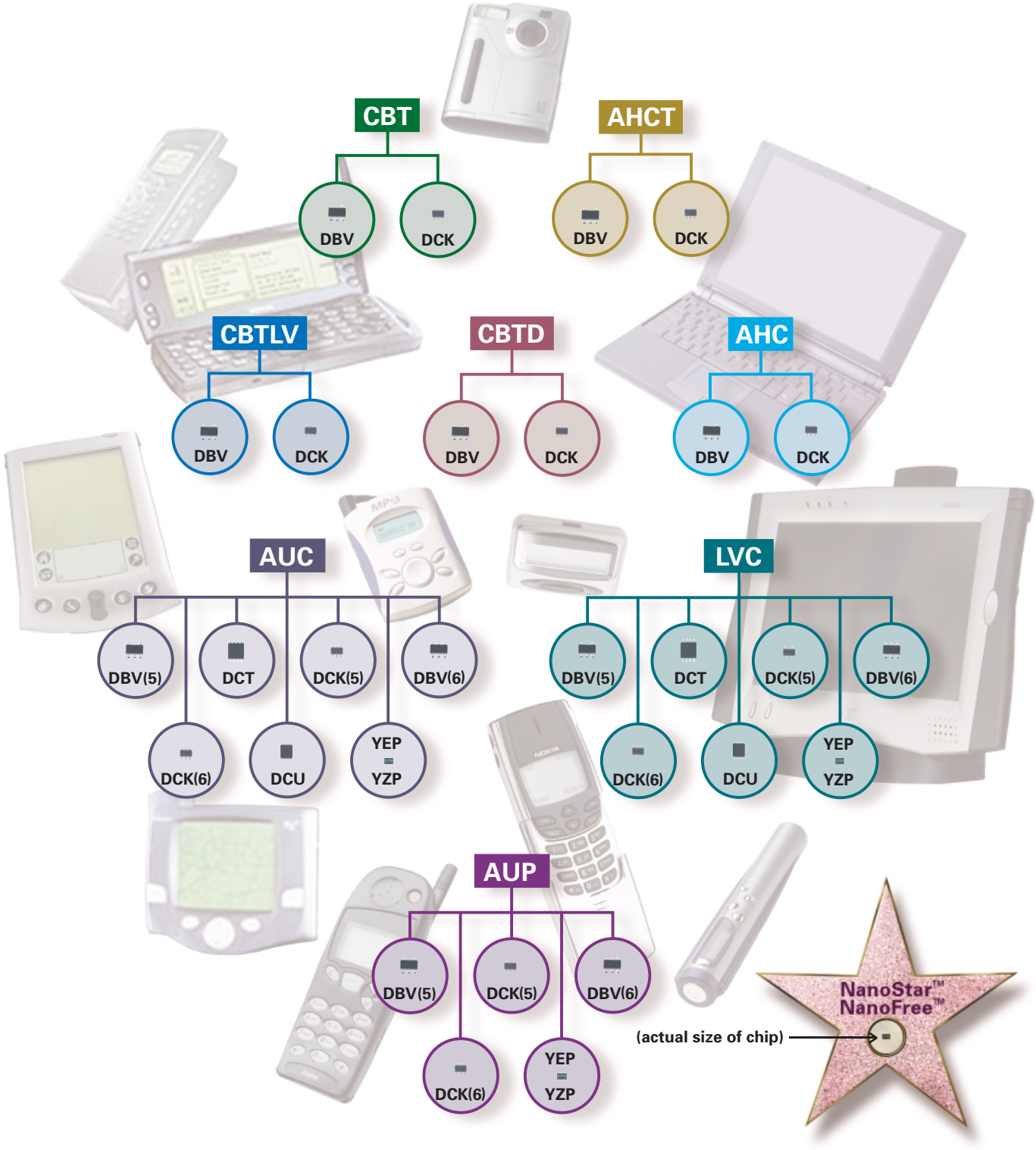
LITTLE LOGIC SELECTION GUIDE



2Q 2004

A WINNING DESIGN IS LIKE A PUZZLE. TEXAS INSTRUMENTS GIVES YOU THE RIGHT PIECES.

Little Logic devices from Texas Instruments (TI) are the pieces that help complete the design puzzle. Their extremely small size gives designers the ability to greatly simplify design routing and maximize ASIC design development. Little Logic devices in 5-pin SOT-23, 5-pin SC-70, 6-pin SOT-23, 6-pin SC-70, 8-pin SM-8, 8-pin US-8 and the NanoStar™ and NanoFree™ packages allow designers to place a particular gate function close to related circuitry, shortening and simplifying routes on a board. This represents a major advance over multiple-gate devices, which require the routing of multiple etches from distinct partitions on a printed circuit board (PCB) through one logic device. In addition, TI's Little Logic devices also allow designers to alter the output of an ASIC without redesign and manufacture, effectively extending the life of the device and maximizing design investment. TI's growing line of Little Logic products is helping designers in almost every end-equipment build more simple, powerful and cost-effective designs. If you would like more information on how TI's Little Logic can help you put all your design pieces together, call your local TI Field Sales office or your authorized TI distributor. Or visit our Web site at: **www.ti.com/littlelogic**

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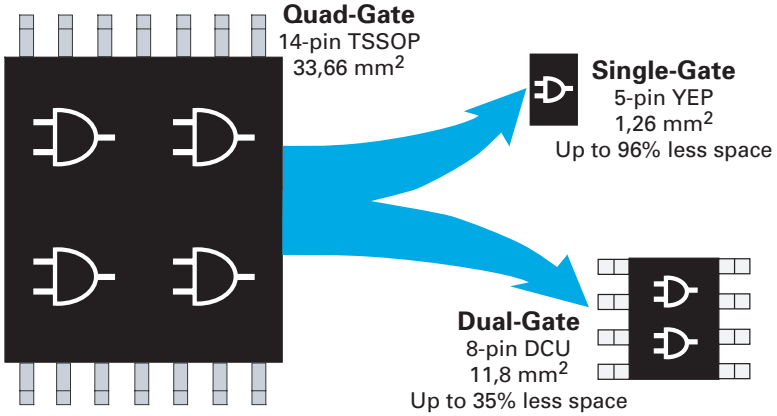
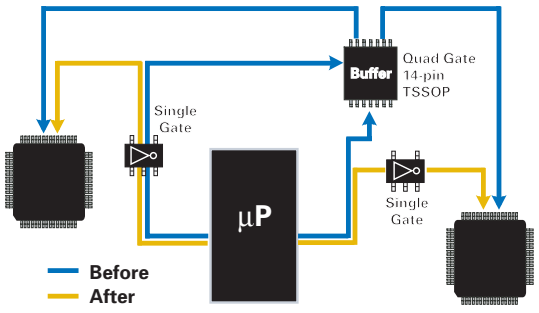
Space-Saving Package Options

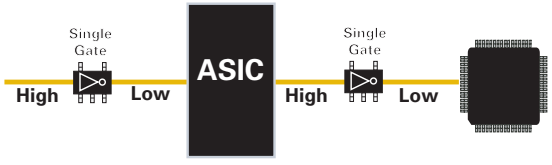


Little Logic Technology Simplifies Board Layout and Offers Better Overall Performance

Simplified Routing



Quick Fixes for ASICs



LITTLE LOGIC PRODUCTS BY PERFORMANCE

Performance Comparisons

Family	Operating Voltage Range (V)	Optimized Voltage (V)	Propagation Delay - t_{pd} (typ) (ns)	Output Drive (mA)	Input Tolerance (V)	I_{OFF} Protection
AUP	0.8 to 3.6	3.3	3.5	4	3.6	Yes
AUC	0.8 to 2.7	1.8	2.0	8	3.6	Yes
LVC	1.65 to 5.5	3.3	3.0	24	5.5	Yes
AHC	2.0 to 5.5	5.0	5.0	8	5.5	No
AHCT	4.5 to 5.5	5.0	5.0	8	5.5	No
CBT	4.5 to 5.5	5.0	0.25†	–‡	5.5	Yes
CBTD	4.5 to 5.5	5.0	0.25†	–‡	5.5	Yes
CBTLV	2.3 to 3.6	3.3	0.25†	–‡	3.6	Yes

†The progagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance). The value listed is a maximum.

‡The FET switch has no output drive. The drive current at the output terminal is determined by the drive current of the device connected at the input terminal of the FET switch.

AHC (Advanced High-Speed CMOS)

- Operating range: 2 to 5.5-V V_{CC}
- 5-ns typical t_{pd}

SN74AHC1G00
SN74AHC1G02
SN74AHC1G04
SN74AHC1GU04
SN74AHC1G08
SN74AHC1G14
SN74AHC1G32
SN74AHC1G86
SN74AHC1G125
SN74AHC1G126

AHCT (Advanced High-Speed CMOS)

- Operating range: 4.5 to 5.5-V V_{CC}
- 5.0-ns typical t_{pd}

SN74AHCT1G00
SN74AHCT1G02
SN74AHCT1G04
SN74AHCT1G08
SN74AHCT1G14
SN74AHCT1G32
SN74AHCT1G86
SN74AHCT1G125
SN74AHCT1G126

AUP (Advanced Ultra-Low-Power CMOS)

- Operating range: 0.8 to 3.6-V V_{CC}
- 3.5-ns typical t_{pd}

SN74AUP1G08
SN74AUP1G57
SN74AUP1G58
SN74AUP1G97
SN74AUP1G98

LVC (Low-Voltage CMOS)

- Operating range: 1.65 to 5.5-V V_{CC}
- 3.0-ns typical t_{pd}

SN74LVC1G00
SN74LVC1G02
SN74LVC1G04
SN74LVC1GU04
SN74LVC1G06
SN74LVC1G07
SN74LVC1G08
SN74LVC1G10
SN74LVC1G11
SN74LVC1G14
SN74LVC1G17
SN74LVC1G18
SN74LVC1G19
SN74LVC1G27
SN74LVC1G32
SN74LVC1G34
SN74LVC1G38
SN74LVC1G57
SN74LVC1G58
SN74LVC1G66
SN74LVC1G79
SN74LVC1G80
SN74LVC1G86
SN74LVC1G97
SN74LVC1G98
SN74LVC1G125
SN74LVC1G126
SN74LVC1G240
SN74LVC1G332
SN74LVC1G373
SN74LVC1G374
SN74LVC1G3157
SN74LVC1T45
SN74LVC2G00
SN74LVC2G02
SN74LVC2G04
SN74LVC2GU04
SN74LVC2G06
SN74LVC2G07
SN74LVC2G08
SN74LVC2G14
SN74LVC2G17
SN74LVC2G32
SN74LVC2G34
SN74LVC2G53
SN74LVC2G66
SN74LVC2G74
SN74LVC2G79
SN74LVC2G80
SN74LVC2G86
SN74LVC2G125
SN74LVC2G126
SN74LVC2G157
SN74LVC2G240
SN74LVC2G241
SN74LVC2T45
SN74LVC3G04
SN74LVC3GU04
SN74LVC3G06
SN74LVC3G07
SN74LVC3G14
SN74LVC3G17
SN74LVC3G34

AUC (Advanced Ultra-Low-Voltage CMOS)

- Operating range: 0.8 to 2.7-V V_{CC}
- 2.0-ns typical t_{pd}

SN74AUC1G00
SN74AUC1G02
SN74AUC1G04
SN74AUC1GU04
SN74AUC1G06
SN74AUC1G07
SN74AUC1G08
SN74AUC1G14
SN74AUC1G17
SN74AUC1G32
SN74AUC1G66
SN74AUC1G74
SN74AUC1G79
SN74AUC1G80
SN74AUC1G86
SN74AUC1G125
SN74AUC1G126
SN74AUC1G240
SN74AUC2G00
SN74AUC2G02
SN74AUC2G04
SN74AUC2GU04
SN74AUC2G06
SN74AUC2G07
SN74AUC2G08
SN74AUC2G14
SN74AUC2G17
SN74AUC2G32
SN74AUC2G34
SN74AUC2G53
SN74AUC2G66
SN74AUC2G74
SN74AUC2G79
SN74AUC2G80
SN74AUC2G86
SN74AUC2G125
SN74AUC2G126
SN74AUC2G157
SN74AUC2G240
SN74AUC2G241
SN74AUC3G04
SN74AUC3GU04
SN74AUC3G06
SN74AUC3G07
SN74AUC3G14
SN74AUC3G17
SN74AUC3G34

LITTLE LOGIC SIGNAL SWITCHES

CBT (Bus Switch)
- Operating range: 4-V to 5.5-V V_{CC}
- 0.25-ns typical t_{pd}

SN74CBT1G125 SN74CBT1G384
SN74CBTD1G125 SN74CBTD1G384

CBTLV (Low-Voltage Bus Switch)
- Operating range: 2.3-V to 3.6-V V_{CC}
- 0.25-ns typical t_{pd}

SN74CBTLV1G125

CB3T (Low-Voltage Translation Bus Switch)
- Operating range: 2.3-V to 3.6-V V_{CC}
- 0.25-ns typical t_{pd}

SN74CB3T1G125

LVC (Low-Voltage CMOS)
- Operating range: 1.8-V to 5.5-V V_{CC}
- 3.0-ns typical t_{pd}

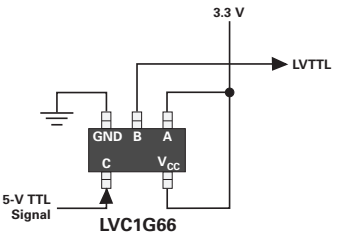
SN74LVC1G66 SN74LVC2G53
SN74LVC1G3157 SN74LVC2G66

AUC (Advanced Ultra-Low-Voltage CMOS)
- Operating range: 0.8-V to 2.7-V V_{CC}
- 2.0-ns typical t_{pd}

SN74AUC1G66 SN74AUC2G66
SN74AUC2G53

LVC1G66 TTL-to-LVTTL Level Shifter

The LVC1G66 can be used for simple translation from 5-V TTL levels to LVTTL. The control pin is tolerant to 5.5 V and, with a maximum r_{on} of 15 W at V_{CC} = 3.3 V, the voltage drop across the switch is only 0.36 V with 24 mA of through current.



Visit **www.ti.com/signalswitches** for the Application Report, *Selecting the Right TI Signal Switch*.

LITTLE LOGIC CONFIGURABLES

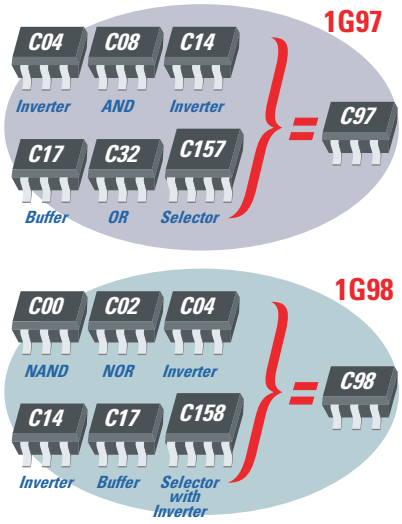
AUP (Advanced Ultra-Low-Power CMOS)
- Operating range: 0.8-V to 3.6-V V_{CC}
- 3.5-ns typical t_{pd}

SN74AUP1G57 SN74AUP1G58
SN74AUP1G97 SN74AUP1G98

LVC (Low-Voltage CMOS)
- Operating range: 1.8-V to 5.5-V V_{CC}
- 3.0-ns typical t_{pd}

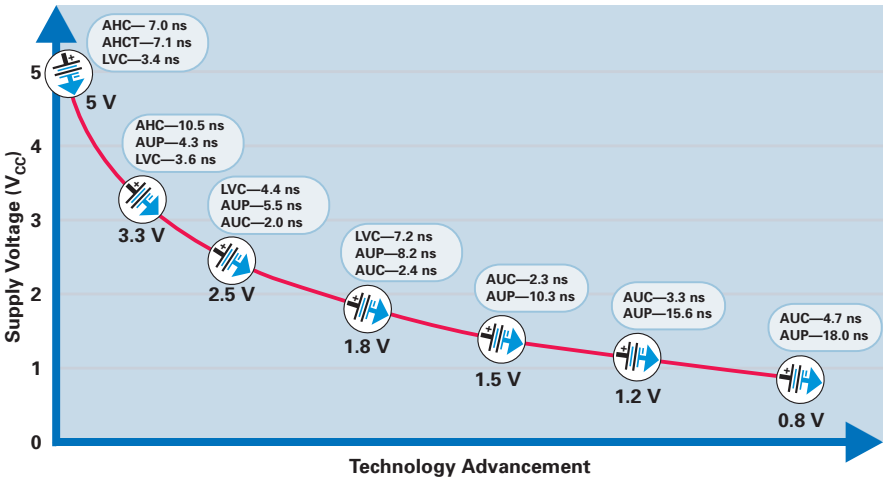
SN74LVC1G57 SN74LVC1G58
SN74LVC1G97 SN74LVC1G98

The next-generation configurable devices in the Little Logic portfolio are the 1G97/98 functions in both the LVC and AUP technologies. By providing nine single-gate logic solutions in one device, the 1G97/98 allows reductions in device inventory and simplifies part management.



LOGIC MIGRATION TO 3.3-V FUTURE

As portable electronics designers look to extend battery life, operating voltages decrease. TI makes the migration to lower operating system voltages simple by offering numerous logic technologies with mixed voltage operation from 5.0-V to 0.8-V. The graph represents TI's logic technology offering in Little Logic at various operating voltages and propagation delays.



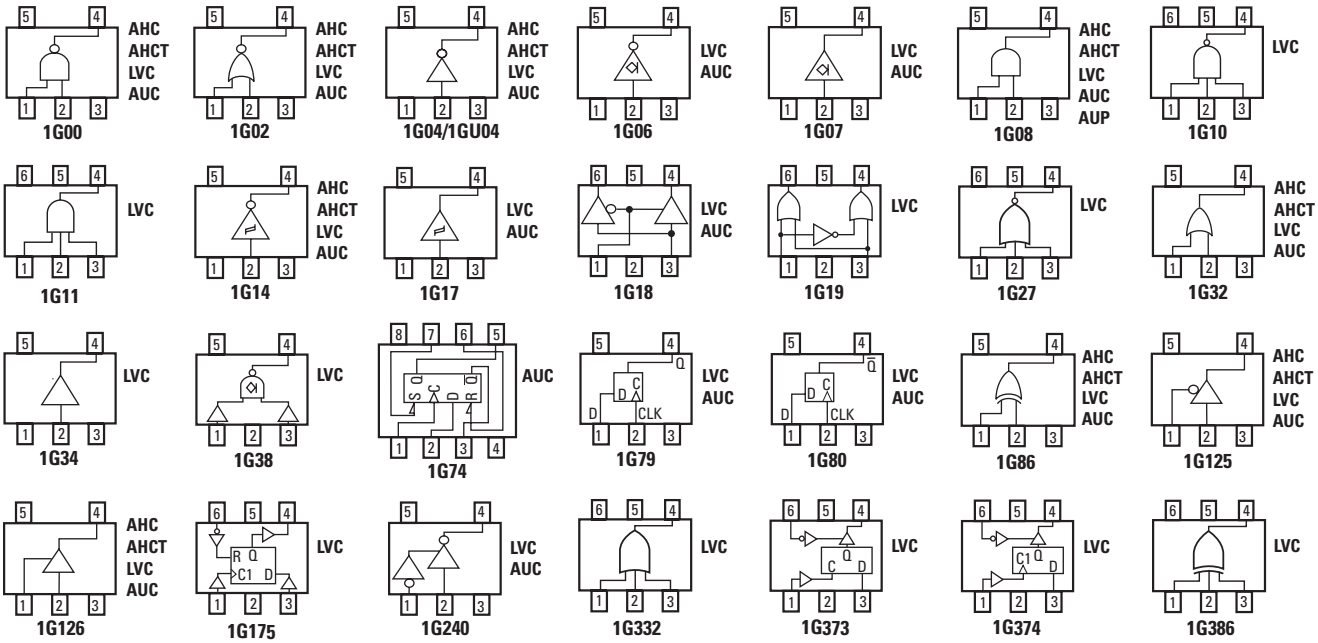
SINGLE-GATE FUNCTIONS

Function	Description	Performance					Package					
		AHC	AHCT	LVC	AUC	AUP	DBV	DCK	DCT	DCU	YEP	YZP*
1G00	Single 2 Input NAND Gate	A	A	A	A		A	A			A	A
1G02	Single 2 Input NOR Gate	A	A	A	A		A	A			A	A
1G04	Single Inverter	A	A	A	A		A	A			A	A
1GU04	Single Unbuffered Inverter	A	A	A	A		A	A			A	A
1G06	Single Inverter Buffer/Driver w/Open Drain Output			A	A		A	A			A	A
1G07	Single Buffer/Driver w/Open Drain Output			A	A		A	A			A	A
1G08	Single 2-Input AND Gate	A	A	A	A	A	A	A			A	A
1G10	Single 3-Input NAND Gate			A			A	A			A	A
1G11	Single 3-Input AND Gate			A			A	A			A	A
1G14	Single Schmitt Trigger Inverter	A	A	A	A		A	A			A	A
1G17	Single Schmitt Trigger Buffer			A	A		A	A			A	A
1G18	1 of 2 Non-Inverting Mux			A	P		A	A			A	A
1G19	1 of 2 Decoder/Demultiplexer			A			A	A			A	A
1G27	Singel 3-Input NOR Gate			A			A	A			A	A
1G32	Single 2-Input OR Gate	A	A	A	A		A	A			A	A
1G34	Single Buffer Gate			A			A	A				
1G38	Single 2-Input NAND Gate w/Open Drain Output			P			P	P				
1G74	Single Positive-Edge-Triggered D-Type Flip-Flop				A				A	A	A	A
1G79	Single D-Type Flip-Flop			A	A		A	A			A	A
1G80	Single D-Type Flip-Flop			A	A		A	A			A	A
1G86	Single 2-Input Exclusive-OR Gate	A	A	A	A		A	A			A	A
1G125	Single Bus Buffer Gate w/3-State Output	A	A	A	A		A	A			A	A
1G126	Single Bus Buffer Gate w/3-State Output	A	A	A	A		A	A			A	A
1G175	Single D-Type Flip-Flop w/Asynch Clr			A			A	A			P	P
1G240	Single Buffer/Driver w/3-State Output			A	A		A	A			A	A
1G332	Single 3-Input OR Gate			A			A	A			A	A
1G373	Single D-Type Latch w/3-State Output			A			A	A			P	P
1G374	Single D-Type Flip-Flop w/3-State Output			A			A	A			P	P
1G386	Single 3-Input Exclusive-OR Gate			A			A	A			A	A

*YZP (NanoFree) is the Pb-Free version of NanoStar. A = Available P = Planned

NOTE: Visit **www.ti.com/littlelogic** for product release updates. Information above valid as of April 2004.

Single-Gate Diagrams



DUAL-GATE FUNCTIONS

Function	Description	Performance		Package					
		LVC	AUC	DBV (6)	DCK (6)	DCT	DCU	YEP	YZP*
2G00	Dual 2-Input NAND Gate	A	A			A	A	A	A
2G02	Dual 2-Input NOR Gate	A	A			A	A	A	A
2G04	Dual Inverter	A	A	A	A	P	P	A	A
2GU04	Dual Unbuffered Inverter	A	A	A	A			A	A
2G06	Dual Inverter w/Open Drain Output	A	A	A	A			A	A
2G07	Dual Non-Inverter w/Open Drain Output	A	A	A	A			A	A
2G08	Dual 2-Input AND Gate	A	A			A	A	A	A
2G14	Dual Schmitt Inverter	A	P	A	A			A	A
2G17	Dual Schmitt Trigger Input Buffers	A		A	A			A	A
2G32	Dual 2-input OR Gate	A	A			A	A	A	A
2G34	Dual Non-Inverter	A	A	A	A			A	A
2G38	Dual 2-Input NAND Gate w/Open Drain Output	A				A	A		
2G53	2:1 Analog Multiplexer/Demultiplexer	A	A			A	A	A	A
2G74	Single Positive Edge Triggered D-Type Flip Flop w/Clear & Reset	A				A	A	A	A
2G79	Dual Positive-Edge-Triggered D-Type Flip-Flop	P	A			A	A	A	A
2G80	Dual Positive-Edge-Triggered D-Type Flip-Flop	P	A			A	A	A	A
2G86	Dual 2-Input Exclusive-OR Gate	A	A			A	A	A	A
2G125	Dual Bus Buffer Gate w/3-State Outputs	A	A			A	A	A	A
2G126	Dual Bus Buffer Gate w/3-State Outputs	A	A			A	A	A	A
2G157	Single 2 Line to 1 Line Data Selector/Multiplexer	A	P			A	A	A	A
2G240	Dual Bus Buffer Gate w/3-State Outputs	A	A			A	A	A	A
2G241	Dual Buffer/Driver w/3-State Outputs	A	A			A	A	A	A

*YZP (NanoFree) is the Pb-Free version of NanoStar. A = Available P = Planned

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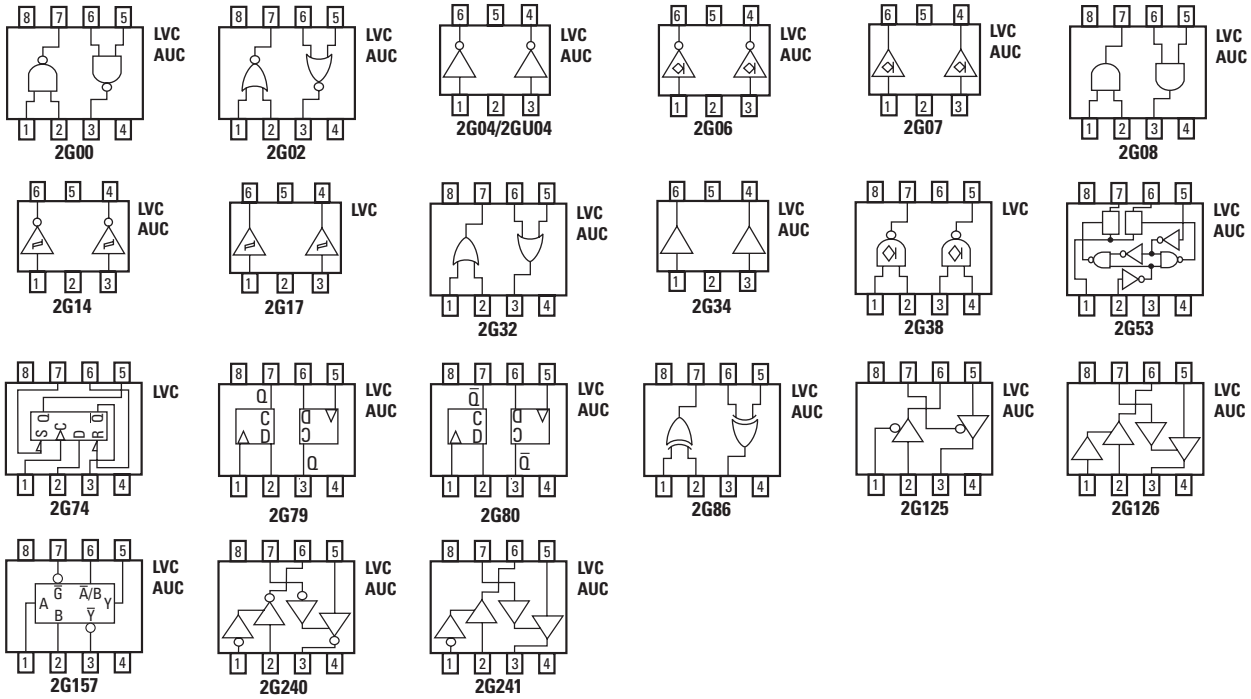
Dual-Gate Diagrams



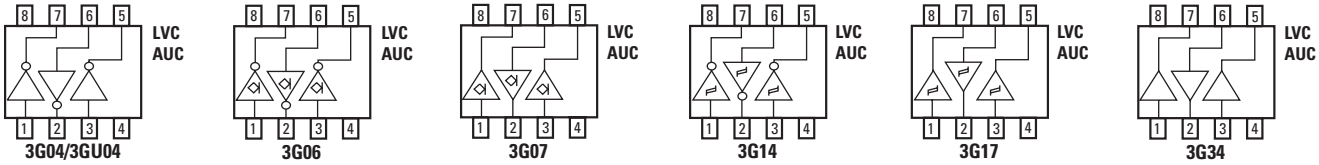
TRIPLE-GATE FUNCTIONS

Function	Description	Performance		Package			
		LVC	AUC	DCT	DCU	YEP	YZP*
3G04	Triple Inverter Gate	A	P	A	A	A	A
3GU04	Triple Inverter Gate (Unbuffered)	A	P	A	A	A	A
3G06	Triple Inverter Buffer/Driver w/Open Drain Output	A	P	A	A	A	A
3G07	Triple Buffer/Driver w/Open Drain Output	A	P	A	A	A	A
3G14	Triple Schmitt Trigger Inverter	A	P	A	A	A	A
3G17	Triple Schmitt Trigger Buffer	A	P	A	A	A	A
3G34	Triple Buffer Gate	A	P	A	A	A	A

*YZP (NanoFree) is the Pb-Free version of NanoStar. A = Available P = Planned

NOTE: Visit **www.ti.com/littlelogic** for product release updates. Information above valid as of April 2004.

Triple-Gate Diagrams



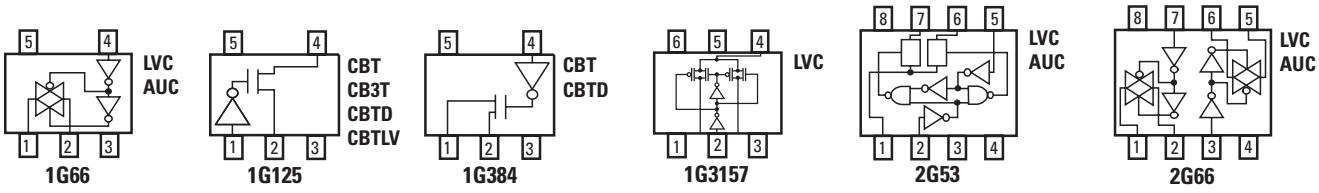
SIGNAL-SWITCH FUNCTIONS

Function	Description	Performance						Packaging							
		CBT	CB3T	CBTD	CBTLV	LVC	AUC	DBV (5)	DCK (5)	DBV (6)	DCK (6)	DCT	DCU	YEP	YZP*
1G66	Single Analog Switch					A	A	A	A					A	A
1G125	Single FET Bus Switch	A	A	A	A			A	A					P	P
1G384	Single FET Bus Switch	A		A				A	A					P	P
1G3157	Single-Pole, Double-Throw (SPDT) Analog Switch					A				A	A			A	A
2G53	Single-Pole, Double-Throw (SPDT) Analog Switch					A	A					A	A	A	A
2G66	Dual Analog Switch					A	A					A	A	A	A

*YZP (NanoFree) is the Pb-Free version of NanoStar. A = Available P = Planned

NOTE: Visit **www.ti.com/littlelogic** for product release updates. Information above valid as of April 2004.

Signal-Switch Diagrams



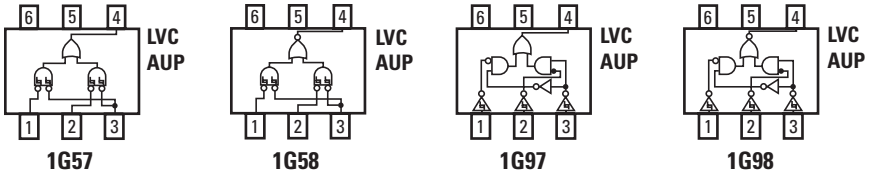
CONFIGURABLE FUNCTIONS

Function	Description	Performance		Package			
		LVC	AUP	DBV	DCK	YEP	YZP*
1G57	Configurable Multiple-Function Gate	A	A	A	A	A	A
1G58	Configurable Multiple-Function Gate	A	A	A	A	A	A
1G97	Configurable Multiple-Function Gate	A	A	A	A	A	A
1G98	Configurable Multiple-Function Gate	A	A	A	A	A	A

*YZP (NanoFree) is the Pb-Free version of NanoStar. A = Available P = Planned

NOTE: Visit **www.ti.com/littlelogic** for product release updates. Information above valid as of April 2004.

Configurable Diagrams



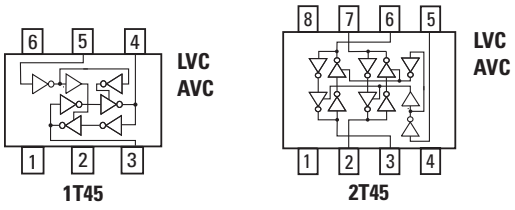
TRANSLATION FUNCTIONS

Function	Description	Performance		Package					
		LVC	AVC	DBV	DCK	DCT	DCU	YEP	YZP*
1T45	Single-Bit Dual-Supply Transceiver w/Configurable Voltage Translation and 3-State Outputs	A	P	A	A			P	P
2T45	Dual-Bit Dual-Supply Transceiver w/Configurable Voltage Translation and 3-State Outputs	A	P			A	A	P	P

*YZP (NanoFree) is the Pb-Free version of NanoStar. A = Available P = Planned

NOTE: Visit **www.ti.com/littlelogic** for product release updates. Information above valid as of April 2004.

Translation Diagrams



COMPETITOR CROSS-REFERENCE

AHC Devices (5-pin, unless noted)

For up-to-date cross-reference information, visit **www.ti.com/littlelogic**

Function	Company (Prefix):	TI (AHC)	Toshiba (TC7S/W)	Fairchild (NC7S)	ON (VHC)	STMicro (V1G)	Philips
1G00	Single 2-Input NAND Gate	SN74AHC1G00	TC7SH00	NC7S00	MC74VHC1G00	74V1G00	74AHC1G00
1G02	Single 2-Input NOR	SN74AHC1G02	TC7SH02	NC7S02	MC74VHC1G02	74V1G02	74AHC1G02
1G04	Single Inverter	SN74AHC1G04	TC7SH04	NC7S04	MC74VHC1G04	74V1G04	74AHC1G04
1GU04	Single Inverter (Unbuffered)	SN74AHC1GU04	TC7SHU04	NC7SU04	MC74VHC1GU04	74V1GU04	74AHC1GU04
1G08	Single 2-Input AND	SN74AHC1G08	TC7SH08	NC7S08	MC74VHC1G08	74V1G08	74AHC1G08
1G14	Single Inverter w/Schmitt Trigger	SN74AHC1G14	TC7SH14	NC7S14	MC74VHC1G14	74V1G14	74AHC1G14
1G32	Single 2-Input OR	SN74AHC1G32	TC7SH32	NC7S32	MC74VHC1G32	74V1G32	74AHC1G32
1G86	Single 2-Input Exclusive-OR	SN74AHC1G86	TC7SH86	NC7S86	MC74VHC1G86	74V1G86	74AHC1G86
1G125	Single Bus Buffer Gate w/3-State	SN74AHC1G125			MC74VHC1G125	74V1G125	74AHC1G125
1G126	Single Bus Buffer Gate w/3-State	SN74AHC1G126			MC74VHC1G126	74V1G126	74AHC1G126

AHCT Devices (5-pin, unless noted)

Function	Company (Prefix):	TI (AHCT)	Toshiba (TC7SE/WT)	Fairchild (NC7ST)	ON (VHC1GT)	STMicro (V1T)	Philips
1G00	Single 2-Input NAND	SN74AHCT1G00	TC7SET00	NC7ST00	MC74VHC1GT00	74V1T00	74AHCT1G00
1G02	Single 2-Input NOR	SN74AHCT1G02	TC7SET02	NC7ST02	MC74VHC1GT02	74V1T02	74AHCT1G02
1G04	Single Inverter	SN74AHCT1G04	TC7SET04	NC7ST04	MC74VCH1GT04	74V1T04	74AHCT1G04
1G08	Single 2-Input AND	SN74AHCT1G08	TC7SET08	NC7ST08	MC74VHC1GT08	74V1T08	74AHCT1G08
1G14	Single Inverter w/Schmitt Trigger	SN74AHCT1G14			MC74VHC1GT14	74V1T14	74AHCT1G14
1G32	Single 2-Input OR	SN74AHCT1G32	TC7SET32	NC7ST32	MC74VHC1GT32	74V1T32	74AHCT1G32
1G86	Single 2-Input Exclusive-OR	SN74AHCT1G86	TC7SET86	NC7ST86	MC74VHC1GT86	74V1T86	74AHCT1G86
1G125	Single Bus Buffer Gate w/3-State	SN74AHCT1G125			MC74VHC1GT125	74V1T125	74AHCT1G125
1G126	Single Bus Buffer Gate w/3-State	SN74AHTC1G126			MC74VHC1GT126	74V1T126	74AHCT1G126

LVC Devices

Function	Company (Prefix):	TI (LVC)	Fairchild (NC7S/WZ)	ON (SZ)	Toshiba (TC7S/WZ)	Philips (LVC)	Pericom (STX)	STMicro (LX)	IDT (LVC)
Single Gate (5-pin, unless noted)									
1G00	Single 2-Input NAND	SN74LVC1G00	NC7SZ00	NL17SZ00	TC7SZ00	74LVC1G00	PI74STX1G00	74LX1G00	IDT74LVC1G00A
1G02	Single 2-Input NOR	SN74LVC1G02	NC7SZ02	NL17SZ02	TC7SZ02	74LVC1G02	PI74STX1G02	74LX1G02	IDT74LVC1G02
1G04	Single Inverter	SN74LVC1G04	NC7SZ04	NL17SZ04	TC7SZ04	74LVC1G04	PI74STX1G04	74LX1G04	IDT74LVC1G04A
1GU04	Single Inverter (Unbuffered)	SN74LVC1GU04	NC7SZU04	NL17SZU04	TC7SZU04	74LVC1GU04	PI74STX1GU04	74LX1GU04	IDT74LVC1GU04A
1GX04	Crystal Driver	SN74LVC1GX04[1]				74LVC1GX04			
1G06	Single Inverter Buffer/Driver w/Open Drain	SN74LVC1G06		NL17SZ06		74LVC1G06			IDT74LVC1G06A
1G07	Single Buffer/Driver w/Open Drain	SN74LVC1G07		NL17SZ07		74LVC1G07		74LX1G07	IDT74LVC1G07A
1G08	Single 2-Input AND	SN74LVC1G08	NC7SZ08	NL17SZ08	TC7SZ08	74LVC1G08	PI74STX1G08	74LX1G08	IDT74LVC1G08A
1G10	Single 3-Input NAND	SN74LVC1G10	NC7SZ10[2]						
1G11	Single 3-Input AND	SN74LVC1G11[2]	NC7SZ11[2]						

[1]Preview [2]6-pin package

COMPETITOR CROSS-REFERENCE (Continued)

LVC Devices

Function	Company (Prefix):	TI (LVC)	Fairchild (NC7S/WZ)	ON (SZ)	Toshiba (TC7S/WZ)	Philips (LVC)	Pericom (STX)	STMicro (LX)	IDT (LVC)
Single Gate (5-pin, unless noted) (Continued)									
1G14	Single Inverter w/Schmitt Trigger	SN74LVC1G14	NC7SZ14	NL17SZ14		74LVC1G14	PI74STX1G14	74LX1G14	
1G17	Single Buffer w/Schmitt Trigger	SN74LVC1G17		NL17SZ17		74LVC1G17			
1G18	1 of 2 Non-Inverting Mux	SN74LVC1G18[2]	NC7SZ18[2]	NL7SZ18[2]		74LVC1G18[2]			
1G19	1 of 2 Decoder	SN74LVC1G19[2]	NC7SZ19[2]	NL7SZ19[2]		74LVC1G19[2]			
1G27	Single 3-Input NOR	SN74LVC1G27[2]	NC7SZ27[2]						
1G32	Single 2-Input OR	SN74LVC1G32	NC7SZ32	NL17SZ32	TC7SZ32	74LVC1G32	PI74STX1G32	74LX1G32	IDT74LVC1G32A
1G34	Single Buffer Gate	SN74LVC1G34		NL17SZ16					
1G38	Single 2-Input NAND w/Open Drain	SN74LVC1G38[1]	NC7SZ38						
1G79	Single D-Type Flip-Flop	SN74LVC1G79				74LVC1G79	PI74STX1G79		IDT74LVC1G79A
1G80	Single D-Type Flip-Flop	SN74LVC1G80				74LVC1G80			
1G86	Single 2-Input EX-OR	SN74LVC1G86	NC7SZ86	NL17SZ86	TC7SZ86	74LVC1G86	PI74STX1G86	74LX1G86	IDT74LVC1G86A
1G125	Single Bus Buffer Gate w/3-State	SN74LVC1G125	NC7SZ125	NL17SZ125	TC7SZ125	74LVC1G125	PI74STX1G125	74LX1G125	IDT74LVC1G125A
1G126	Single Bus Buffer Gate w/3-State	SN74LVC1G126	NC7SZ126	NL17SZ126	TC7SZ126	74LVC1G126	PI74STX1G126	74LX1G126	IDT74LVC1G126A
1G132	Single 2-Input NAND w/Schmitt Trigger	SN74LVC1G132[1]						74LX1G132	
1G157	2-input Non-Inverting Mux	SN74LVC1G157[2]	NC7SZ157[2]						
1G175	Single D-Type Flip-Flop w/Asynch Clr	SN74LVC1G175[2]	NC7SZ175[2]						
1G240	Single bus Buffer Gate w/3-state	SN74LVC1G240							
1G332	Single 3-Input OR	SN74LVC1G332[2]	NC7SZ332[2]						
1G373	Single D-Type Latch w/3-State	SN74LVC1G373[2]	NC7SZ373[2]						
1G374	Single D-Type Flip-Flop w/3-State	SN74LVC1G374[2]	NC7SZ374[2]						
1G386	Single 3-Input Exclusive-OR	SN74LVC1G386[2]	NC7SZ386[2]			74LVC1G386			
Dual Gate (8-pin, unless noted)									
2G00	Dual 2-Input NAND	SN74LVC2G00	NC7WZ00	NL27WZ00	TC7WZ00	74LVC2G00	PI74STX2G00		
2G02	Dual 2-Input NOR	SN74LVC2G02	NC7WZ02	NL27WZ02	TC7WZ02	74LVC2G02	PI74STX2G02		
2G04	Dual Inverter	SN74LVC2G04[2]	NC7WZ04[2]	NL27WZ04[2]	TC7WZ04	74LVC2G04[2]	PI74STX2G04		
2GU04	Dual Inverter (Unbuffered)	SN74LVC2GU04	NC7WZU04[2]	NL27WZU04[2]	TC7WZU04	74LVC2GU04[2]	PI74STX2GU04		
2G06	Dual Inverter Buffer/Driver w/Open Drain	SN74LVC2G06[2]		NL27WZ06[2]		74LVC2G06			
2G07	Dual BufferDriver w/Open Drain Output	SN74LVC2G07[2]	NC7WZ07[2]	NL27WZ07[2]		74LVC2G07[2]			
2G08	Dual 2-Input AND	SN74LVC2G08	NC7WZ08	NL27WZ08	TC7WZ08	74LVC2G08	PI74STX2G08		
2G14	Dual Inverter w/Schmitt Trigger	SN74LVC2G14[2]	NC7WZ14[2]	NL27WZ14[2]	TC7WZ14	74LVC2G14[2]	PI74STX2G14		
2G17	Dual Buffer w/Schmitt Trigger Input	SN74LVC2G17[2]	NC7WZ17[2]	NL27WZ17[2]		74LVC2G17[2]			
2G32	Dual 2-Input OR	SN74LVC2G32	NCWZ32	NL27WZ32	TC7WZ32	74LVC2G32	PI74STX2G32		
2G34	Dual Buffer Gate	SN74LVC2G34[2]	NC7WZ16[2]	NL27WZ16[2]	TC7WZ34	74LVC2G34[2]			
2G38	Dual 2-Input NAND w/Open Drain	SN74LVC2G38[1]	NCWZ38		TC7WZ38	74LVC2G38			
2G74	D-Type Flip-Flop w/Pre & CLR	SN74LVC2G74	NC7SZ74	NL17SZ74	TC7WZ74		PI74STX2G74		
2G79	Dual D-Type Flip-Flop	SN74LVC2G79					PI74STX2G79		

[1]Preview [2]6-pin package

COMPETITOR CROSS-REFERENCE (Continued)

LVC Devices (Continued)

Function	Company (Prefix):	TI (LVC)	Fairchild (NC7S/WZ)	ON (SZ)	Toshiba (TC7S/WZ)	Philips (LVC)	Pericom (STX)	STMicro (LX)	IDT (LVC)
Dual Gate (8-pin, unless noted) (Continued)									
2G80	Dual D-Type Flip-Flop	SN74LVC2G80							
2G86	Dual 2-Input Exclusive-OR	SN74LVC2G86	NC7WZ86	NL27WZ86		74LVC2G86	PI74STX2G86		
2G125	Dual Bus Buffer Gate w/3-State	SN74LVC2G125	NC7WZ125	NL27WZ125		74LVC2G125	PI74STX2G125		
2G126	Dual Bus Buffer Gate w/3-State	SN74LVC2G126	NC7WZ126	NL27WZ126		74LVC2G126	PI74STX2G126		
2G132	Dual 2-Input NAND w/Schmitt Trigger Input	SN74LVC2G132[1]	NC7WZ132						
2G157	2-input Non-Inverting Mux	SN74LVC2G157							
2G240	Dual Bus Buffer Gate w/3-State	SN74LVC2G240	NC7WZ240			74LVC2G240			
2G241	Dual Bus Buffer Gate w/3-State	SN74LVC2G241	NC7WZ241			74LVC2G241			
Triple Gate (8-pin, unless noted)									
3G04	Triple Inverter	SN74LVC3G04	NC7NZ04	NL37WZ04	TC7WZ04		PI74STX3G04		
3GU04	Triple Inverter (Unbuffered)	SN74LVC3GU04[1]	NC7NZU04		TC7WZU04		PI74STX3GU04		
3G06	Triple Inverter Buffer/Driver w/Open Drain	SN74LVC3G06		NL37WZ06					
3G07	Triple Buffer/Driver w/Open Drain	SN74LVC3G07		NL37WZ07					
3G14	Triple Inverter w/Schmitt Trigger	SN74LVC3G14	NC7NZ14	NL37WZ14	TC7WZ14		PI74STX3G14		
3G17	Triple Buffer w/Schmitt Trigger	SN74LVC3G17	NC7NZ17	NL37WZ17					
3G34	Triple Buffer	SN74LVC3G34	NC7NZ34	NL37WZ16	TC7WZ34				

[1]Preview [2]6-pin package

COMPETITOR CROSS-REFERENCE (Continued)

AUC Devices

Function	Company (Prefix):	TI (AUC)	Fairchild (NC7SV)	ON (SV)
Single Gate (5-pin, unless noted)				
1G1G00	Single 2-Input NAND	SN74AUC1G00	NC7SV00	NL17SV00
1G02	Single 2-Input NOR	SN74AUC1G02	NC7SV02	NL17SV02
1G04	Single Inverter	SN74AUC1G04	NC7SV04	NL17SV04
1GU04	Single Inverter (Unbuffered)	SN74AUC1GU04	NC7SVU04	
1G06	Single Inverter Buffer/Driver w/Open Drain	SN74AUC1G06		
1G07	Single Buffer/Driver w/Open Drain	SN74AUC1G07		
1G08	Single 2-Input AND	SN74AUC1G08	NC7SV08	NL17SV08
1G11	Single 3-Input AND	SN74AUC1G11[1]	NC7SV11	
1G14	Single Inverter w/Schmitt Trigger	SN74AUC1G14	NC7SV14	
1G17	Single Buffer w/Schmitt Trigger	SN74AUC1G17	NC7SV17	
1G32	Single 2-Input OR	SN74AUC1G32	NC7SV32	NL17SV32
1G74	D-Type Flip-Flop w/Pre & CLR	SN74AUC1G74	NC7SV74	
1G79	Single D-Type Flip-Flop	SN74AUC1G79		
1G80	Single D-Type Flip-Flop	SN74AUC1G80		
1G86	Single 2-Input Exclusive-OR	SN74AUC1G86	NC7SV86	
1G125	Single Bus Buffer Gate w/3-State	SN74AUC1G125	NC7SV125	
1G126	Single Bus Buffer Gate w/3-State	SN74AUC1G126	NC7SV126	
1G240	Single Bus Buffer Gate w/3-State	SN74AUC1G240		
Dual Gate (8-pin, unless noted)				
2G00	Dual 2-Input NAND	SN74AUC2G00		
2G02	Dual 2-Input NOR	SN74AUC2G02		
2G04	Dual Inverter	SN74AUC2G04[2]	NC7WV04	
2GU04	Dual Inverter (Unbuffered)	SN74AUC2GU04		
2G06	Dual Inverter Buffer/Driver w/Open Drain Output	SN74AUC2G06[2]		
2G07	Dual Buffer/Driver w/Open Drain Output	SN74AUC2G07[2]	NC7WV07	
2G08	Dual 2-Input AND	SN74AUC2G08		
2G14	Dual Inverter w/Schmitt Trigger	SN74AUC2G14[1]	NC7WV14	
2G17	Dual Buffer w/Schmitt Trigger Input	SN74AUC2G17[1]	NC7WV17	
2G32	Dual 2-Input OR	SN74AUC2G32		
2G34	Dual Buffer	SN74AUC2G34[2]	NC7WV16	
2G79	Dual D-Type Flip-Flop	SN74AUC2G79		
2G80	Dual D-Type Flip-Flop	SN74AUC2G80		
2G86	Dual 2-Input Exclusive-OR	SN74AUC2G86		
2G125	Dual Bus Buffer Gate w/3-State	SN74AUC2G125	NC7WV125	
2G126	Dual Bus Buffer Gate w/3-State	SN74AUC2G126		
2G240	Dual Bus Buffer Gate w/3-State	SN74AUC2G240		
2G241	Dual Bus Buffer Gate w/3-State	SN74AUC2G241		

[1]Preview [2]6-pin package

COMPETITOR CROSS-REFERENCE (Continued)

AUP Devices (5-pin, unless noted)

Function	Company (Prefix):	TI (AUC)	Fairchild (NC7SV)
1G00	Single 2-Input NAND	SN74AUP1G00[1]	NC7SP00
1G02	Single 2-Input NOR	SN74AUP1G02[1]	NC7SP02
1G04	Single Inverter	SN74AUP1G04[1]	NC7SP04
1G06	Single Inverter Buffer/Driver w/Open Drain	SN74AUP1G06[1]	
1G07	Single Buffer/Driver w/Open Drain	SN74AUP1G07[1]	
1G08	Single 2-input AND	SN74AUP1G08	NC7SP08
1G14	Single Inverter w/Schmitt Trigger	SN74AUP1G14[1]	NC7SP14
1G17	Single Buffer w/Schmitt Trigger	SN74AUP1G17[1]	NC7SP17
1G32	Single 2-Input OR	SN74AUP1G32[1]	NC7SP32
1G34	Single Buffer	SN74AUP1G34[1]	NC7SP34
1G79	Single D-Type Flip-Flop	SN74AUP1G79[1]	
1G80	Single D-Type Flip-Flop	SN74AUP1G80[1]	
1G125	Single Bus Buffer Gate w/3-State	SN74AUP1G125[1]	NC7SP125
1G126	Single Bus Buffer Gate w/3-State	SN74AUP1G126[1]	NC7SP126
1G240	Single Bus Buffer Gate w/3-State	SN74AUP1G240[1]	

[1]Preview

Signal-Switch Devices

Function	Company:	TI	Toshiba	Fairchild	Philips	Pericom
CBT1G125	Single FET Bus Switch	SN74CBT1G125				P15A125
CBTD1G125	Single FET Bus Switch	SN74CBTD1G125				
CBT1G384	Single Low Power Bus Switch	SN74CBT1G384	TC7SB384	NC7SZ384		
CBTD1G384	384 Function w/Level Shifting	SN74CBTD1G384	TC7SBD384	NC7SZD384		
CBTLV1G125	Single LV FET Bus Switch	SN74CBTLV1G125				P13A125
AUC1G66	Single Analog Switch	SN74AUC1G66				
AUC2G53	SPDT Analog Switch	SN74AUC2G53	TC7PA53			
AUC2G66	Dual Analog Switch	SN74AUC2G66				
LVC1G66	Single Analog Switch	SN74LVC1G66		NC7SZ66	74LVC1G66	
LVC1G3157	SPDT Analog Switch	SN74LVC1G3157		NC7SB3157		
LVC2G53	SPDT Analog Switch	SN74LVC2G53				
LVC2G66	Dual Analog Switch	SN74LVC2G66		NC7WB66		

Configurable Devices

Function	Company:	TI	Fairchild
LVC1G57	Single Configurable (5 functions)	SN74LVC1G57	NC7SZ57
LVC1G58	Single Configurable (5 functions)	SN74LVC1G58	NC7SZ58
LVC1G97	Single Configurable (9 functions)	SN74LVC1G97	
LVC1G98	Single Configurable (9 functions)	SN74LVC1G98	
AUP1G57	Single Configurable (5 functions)	SN74AUP1G57	NC7SP57
AUP1G58	Single Configurable (5 functions)	SN74AUP1G58	NC7SP58
AUP1G97	Single Configurable (9 functions)	SN74AUP1G97	
AUP1G98	Single Configurable (9 functions)	SN74AUP1G98	
AUC1G57	Single Configurable (5 functions)	SN74AUC1G57[1]	NC7SV57
AUC1G58	Single Configurable (5 functions)	SN74AUC1G58[1]	NC7SV58

[1]Preview

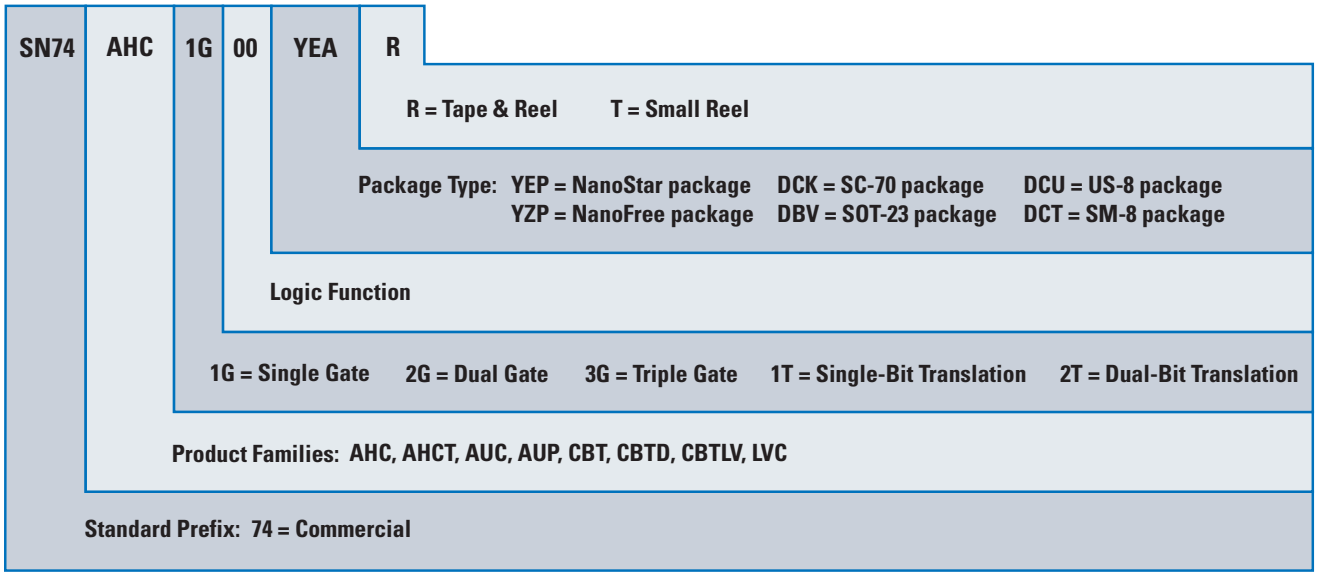
Translation Devices

Function	Company:	TI	Fairchild	Pericom	IDT
LVC1T45	Single-Bit	SN74LVC1T45			
LVC2T45	Dual-Bit	SN74LVC2T45			
AVC1T45	Single-Bit	SN74AVC1T45[1]			
AVC2T45	Dual-Bit	SN74AVC2T45[1]			
AVCH1T45	Single-Bit (w/Bus Hold)	SN74AVCH1T45[1]			
AVCH2T45	Dual-Bit (w/Bus Hold)	SN74AVCH2T45[1]			

All devices are Dual-Supply Bus Transceivers w/Configurable Voltage Translation and 3-State Outputs

[1]Preview

PART NUMBER DEFINITION



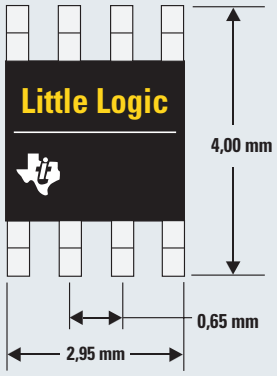
COMPETITOR PART PREFIXES

TI	Toshiba	Fairchild	ON	STMicro	Philips	IDT	Pericom
Little Logic							
SN74AHC1G	TC7S	NC7S	MC74VHC1G	74V1G	74AHC1G		
SN74AHCT1G	TC7SET	NC7ST	MC74VHC1GT	74V1T	74AHCT1G		
SN74AUC1G		NC7SV	NL17SV				
SN74AUC2G		NC7WV					
SN74AUP1G		NC7SP					
SN74LVC1G	TC7SZ	NC7SZ	NL17SZ	74LX1G	74LVC1G	IDT74LVC1G	P174STX1G
SN74LVC2G	TC7WZ	NC7WZ	NL27WZ		74LVC2G		P174STX2G
SN74LVC3G	TC7WZ	NC7NZ	NL37WZ				P174STX3G
Little Logic Signal Switches							
SN74AUC2G	TC7PA						
SN74CBT1G	TC7SB	NC7SZ					P15A
SN74CBTD1G	TC7SBD	NC7SZD					
SN74CBTLV1G	TC7SBL						P13A
SN74LVC1G66		NC7SZ66			74LVC1G66		
SN74LVC2G66		NC7WB66					
Little Logic Configurables							
SN74AUP1G57		NC7SP57					
SN74AUP1G58		NC7SP58					
SN74LVC1G57		NC7SZ57					
SN74LVC1G58		NC7SZ58					
Little Logic Translation							
SN74LVC1T45							
SN74LVC2T45							

LITTLE LOGIC PACKAGING AND MECHANICAL DATA

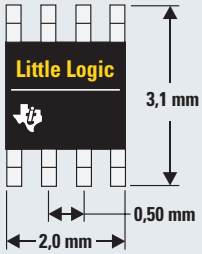
DCT (SM-8)

(Actual Size)



DCU (US-8)

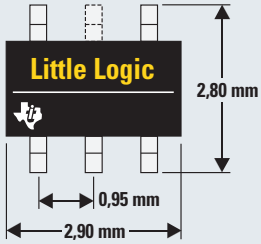
(Actual Size)



DBV (SOT-23)

5-pin or 6-pin

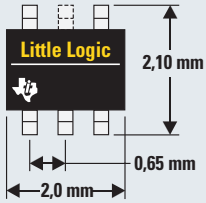
(Actual Size)



DCK (SC-70)

5-pin or 6-pin

(Actual Size)

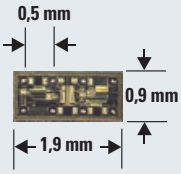


NanoStar (YEP)

8-pin

(Actual Size)

NanoFree (YZP)

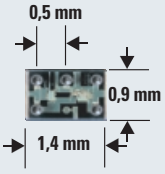


NanoStar (YEP)

5-pin or 6-pin

(Actual Size)

NanoFree (YZP)



Package Data	DCT 8-pin	DCU 8-pin	DBV 5- or 6-pin	DCK 5- or 6-pin	YEP/YZP 5- or 6-pin	YEP/YZP 8-pin
Length (mm)	2,95 ± 0,20	2,0 ± 0,1	2,90 ± 0,1	2,00 ± 0,15	1,40 ± 0,05	1,90 ± 0,05
Width (mm)	4,00 ± 0,25	3,1 ± 0,1	2,80 ± 0,2	2,10 ± 0,2	0,90 ± 0,05	0,90 ± 0,05
Height (mm)	1,30	0,90	1,20	0,95	0,50	0,50
Footprint Area (mm^2)	11,80	6,20	8,12	4,20	1,26	1,71
Weight (gm)	0,0206	0,0095	0,0135	0,006	≤ 0,001	0,0013

LITTLE LOGIC PACKAGE CROSS-REFERENCE

	TI	Fairchild	ON	Toshiba	Philips	IDT	Pericom	STMicro
NanoStar	YEP	L6*						
NanoFree	YZP							
SOT-23 (5-pin)	DBV	M5	DT	F	GV		TX	ST
SC-70 (5-pin)	DCK	P5	DF	FU	GW	DY	CX	CT
SOT-23 (6-pin)	DBV	DT			GV			
SC-70 (6-pin)	DCK	P6	DF		DW			
SM-8 (8-pin)	DCT			FU				
US-8 (8-pin)	DCU	K8	US	FK	DC			

**Nanostar measures smaller than L6 package.*

Note: Pb-Free, NanoFree classified per J-STD-020B MSL-1 rated.

www.ti.com/nanostar

TI Package Suffix Decoder

YEP is NanoStar
YZP is NanoFree, Pb-Free
DBV is 5 and 6-pin leadframe

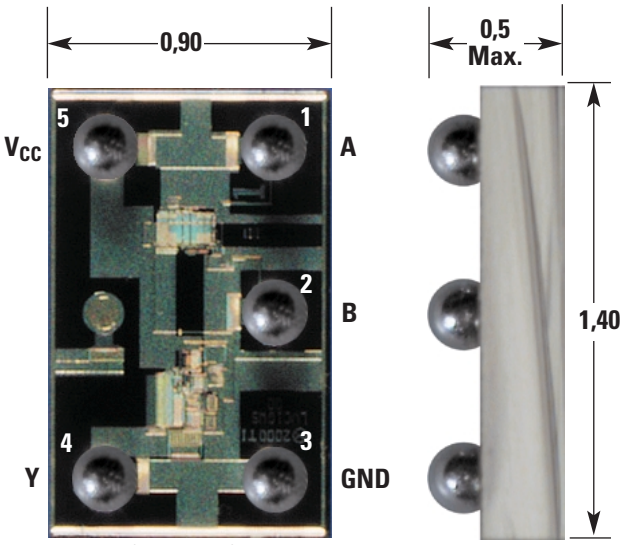
DCK is 5 and 6-pin leadframe, slightly smaller than DBV
DBV is 5 and 6-pin leadframe

DCK is 5 and 6-pin leadframe, slightly smaller than DBV
DCT is 8-pin leadframe

DCU is 8-pin leadframe, slightly smaller than DCT

INTRODUCTION TO NanoStar AND NanoFree

As the marketplace continues to demand size reductions in various consumer electronic products such as cell phones, PDAs, MP3/CD players and other portable devices, the need for smaller logic packaging becomes paramount. The major challenge of today's digital processing industry is the overall system cost reduction as complexity and functionality increase. These marketplace forces have resulted in circuit integration and board miniaturization becoming a necessary trend for successful competition. To address these rapidly evolving customer requirements, TI has defined the latest innovation in logic packaging: NanoStar and NanoFree. This is a wafer-chip-scale package (WCSP) and, to date, is the world's smallest 5-, 6- and 8-pin logic solution for Little Logic functions. NanoStar and NanoFree are registered under JEDEC MO-211, and are the only wafer-level logic solutions available to date. NanoStar uses an eutectic SnPb ball, and NanoFree uses a Pb-Free (SnAgCu) ball. Other than ball metallurgy, there is no difference between NanoStar (YEA) and NanoFree (YZA). TI offers both a small ball and a large ball version of the WCSP.



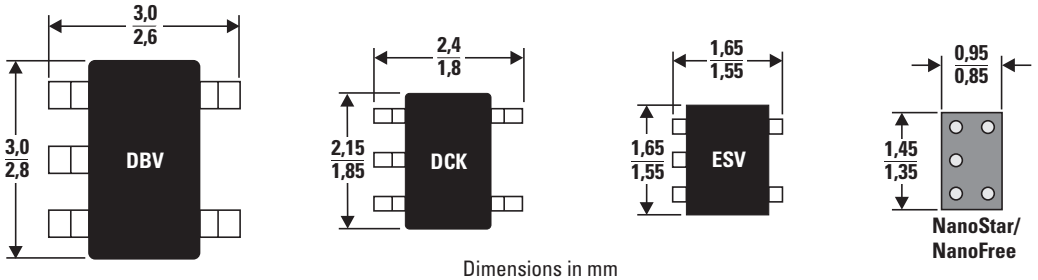
(Bottom view)
Dimensions in millimeters (mm)

Package Designators
YEP = SnPb Large Ball
YZP = Pb-Free Large Ball

NanoFree™

Pb-FREE

PACKAGE DATA



Dimensions in mm

Package Comparisons

Package Data	SOT-23 (5-pin) TI – DBV	SC-70 (5-pin) TI – DCK	ESV*	WCSP (5-/6-pin) TI – YEP/YZP
Length (mm)	2,90 ± 0,10	2,00 ± 0,15	1,60 ± 0,05	1,40 ± 0,05
Width (mm)	2,80 ± 0,20	2,10 ± 0,30	1,60 ± 0,05	0,90 ± 0,05
Height Max (mm)	1,45	1,10	0,60	0,50
Footprint Area (mm^2)	8,12	4,20	2,56	1,26
Approx. Weight (g)	0,0135	0,006	0,003	≤0,00113

*Available 3Q 2004.

PACKAGE DATA (Continued)

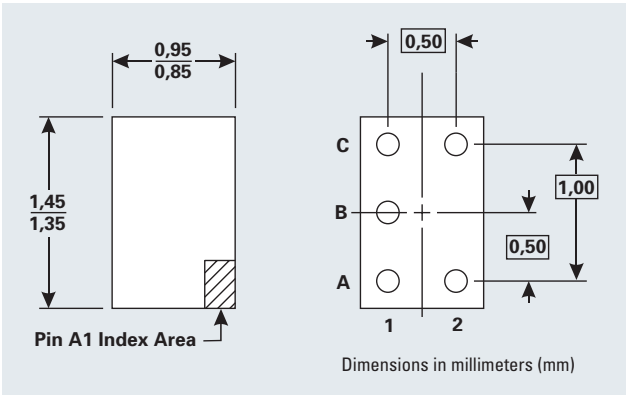
Dual-/Triple-Gate Comparisons

	SOT-23 (6-pin)	SC-70 (6-pin)	SSOP (8-pin)	VSOP (8-pin)	WCSP (8-pin)
Package Data	**TI – DBV**	**TI – DCK**	**TI – DCT**	**TI – DCU**	**TI – YEP/YZP**
Length (mm)	2,90 ± 0,10	2,00 ± 0,15	2,95 ± 0,20	2,0 ± 0,10	1,90 ± 0,05
Width (mm)	2,80 ± 0,20	2,10 ± 0,30	4,0 ± 0,25	3,10 ± 0,10	0,90 ± 0,05
Height (mm)	1,20 ± 0,25	0,95 ± 0,15	1,30 max	0,90 max	0,50 max
Footprint Area (mm^2)	8,12	4,20	11,80	6,20	1,71
Weight (g)	0,0135	0,006	0,0206	0,0095	0,00153

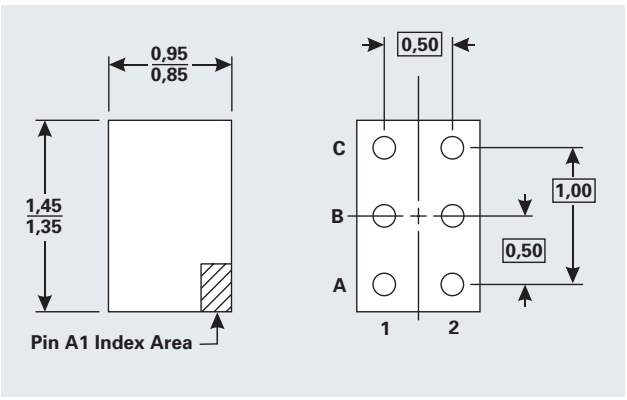
Package Attributes

Attribute	5-Ball	6-Ball	8-Ball
Ball Pitch (mm)	0,5	0,5	0,5
Ball Diameter (mm)	Small Ball = 0,17 Large Ball = 0,23	Small Ball = 0,17 Large Ball = 0,23	Small Ball = 0,17 Large Ball = 0,23
Package Length (mm)	1,4	1,4	1,9
Package Width (mm)	0,9	0,9	0,9
Package Height (mm)	0,5 max	0,5 max	0,5 max
Ball Matrix (rows, columns)	3 x 2, depopulate 1	3 x 2	4 x 2
Weight (mg)	Small Ball = 0,995 Large Ball = 1,07	Small Ball = 0,998 Large Ball = 1,13	Small Ball = 1,30 Large Ball = 1,53
Ball Metallurgy	SnPb or Pb-Free	SnPb or Pb-Free	SnPb or Pb-Free
Moisture Level	Level 1 @ 260°C	Level 1 @ 260°C	Level 1 @ 260°C

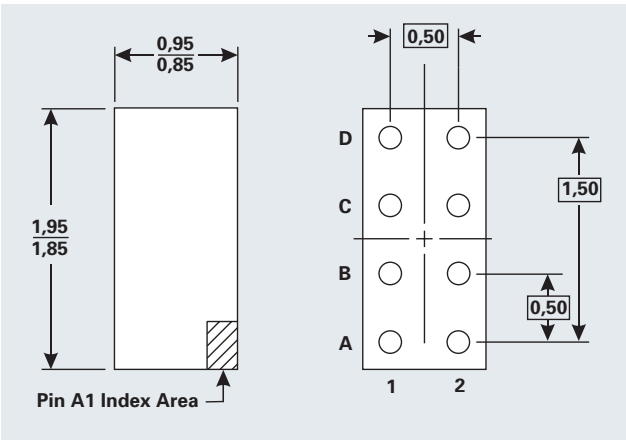
5-Ball Package



6-Ball Package

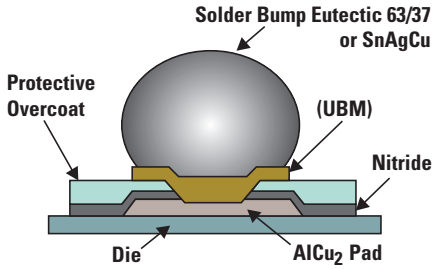


8-Ball Package

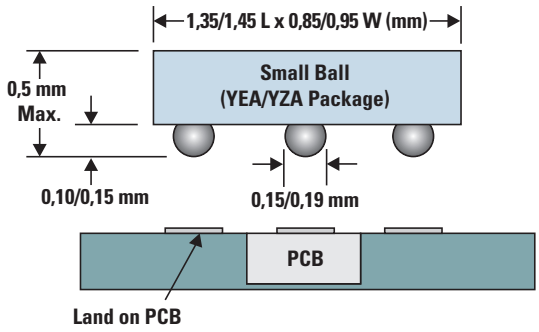


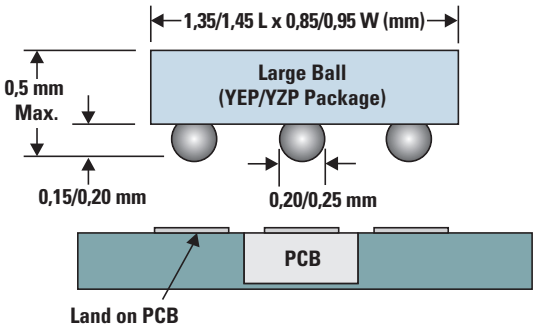
PCB DESIGN GUIDELINES

Solder Ball Composition

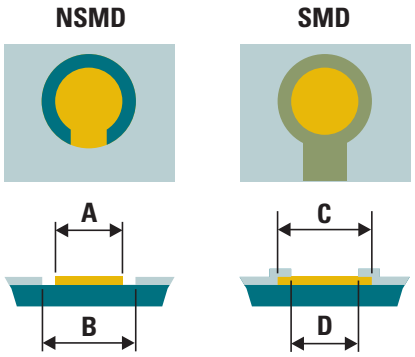


Package Area Configuration (0,5-mm Ball Pitch)



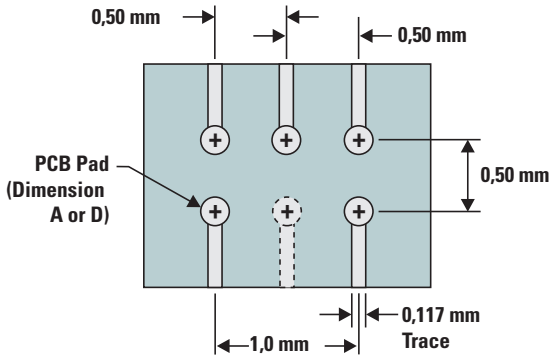


PCB Design

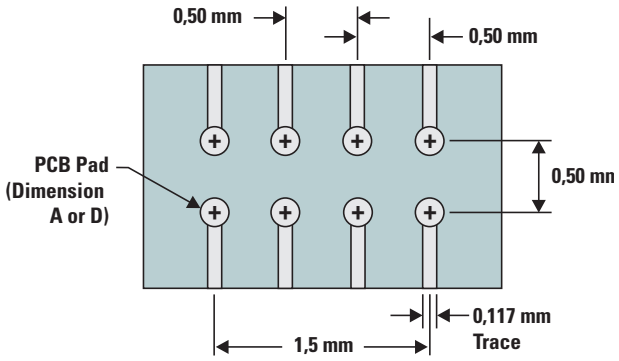


Non-Solder Mask Defined (NSMD) Preferred Method		Solder Mask Defined (SMD)	
Copper Pad	Solder Mask Opening	Copper Pad	Solder Mask Opening
"A"	"B"	"C"	"D"
Small Ball (YEA, YZA)			
0,175 mm + 0,0/–0,025 mm	0,350 mm ± 0,025 mm	0,350 mm ± 0,025 mm	0,175 mm + 0,0/–0,025 mm
Large Ball (YEP, YZP)			
0,225 mm ± 0,025 mm	0,350 mm ± 0,025 mm	0,350 mm ± 0,025 mm	0,225 mm ± 0,025 mm

5-/6-Ball PCB Pattern



8-Ball PCB Pattern



Note: Trace width shall be ≤ $\frac{2}{3}$ pad diameter.

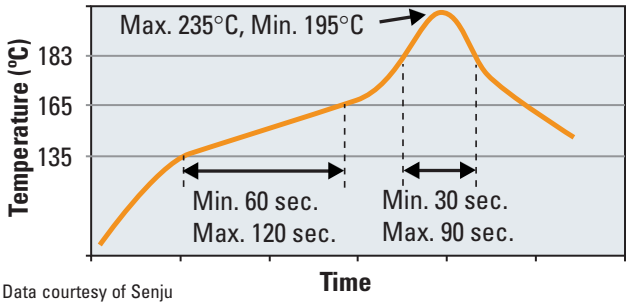
IR REFLOW PROFILE

Reflow Parameters

	Pb Assy	Pb-Free
Ramp Rate:	3°C/sec. Max.	3°C/sec. Max.
Preheat	135 to 165°C	150 to 180°C
	60 to 120 sec.	60 to 120 sec.
Time Above Liquidus:	183°C	220°C
	30 to 90 sec.	30 to 90 sec.
Peak Temp.	235°C ±5°C	255°C ±5°C
Time Within 5°C Peak Temp.	20 to 40 sec.	20 to 40 sec.
Ramp Down Rate	6°C/sec. Max.	6°C/sec. Max.

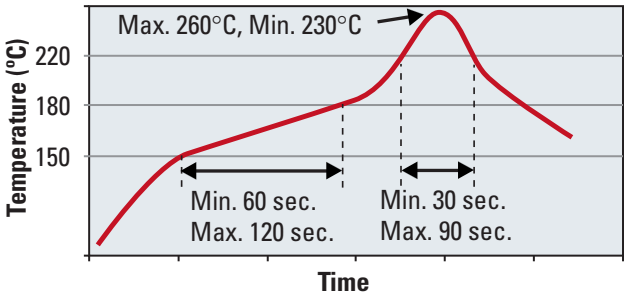
Note: These are ideal profiles, and actual conditions obtained in any specified reflow oven will vary. The profiles are based on convection or RF plus forced convection heating.

SnPb Eutectic (AT-Alloy and S2062) Recommended Temperature Profile



Data courtesy of Senju

Pb-Free Ball NanoFree Recommended Temperature Profile



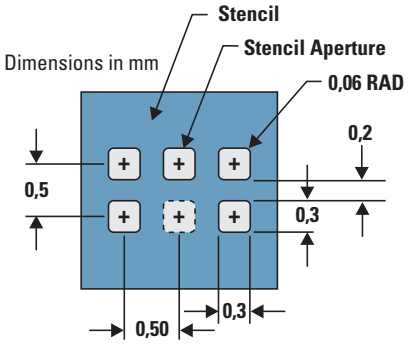
STENCIL VITALS

Solder Paste

TI recommends the use of type 3 or finer solder paste when mounting the WCSP. The use of paste offers the following advantages:

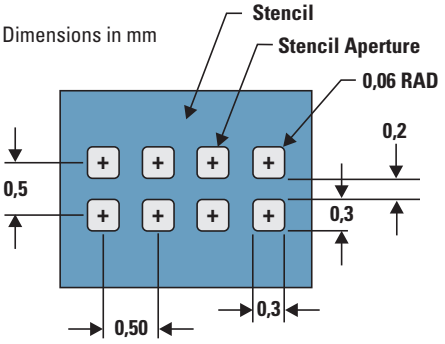
- Paste aids wetting of the solder ball to the PCB land.
- The adhesive properties of the paste will hold the component in place during reflow.
- Paste contributes to the final volume of solder in the joint, and thus allows this volume to be varied to give an optimum joint.
- Paste selection is normally driven by overall system assembly requirements. In general, the "no clean" compositions are preferred due to the difficulty in cleaning under the mounted components.

5-/6-Ball Solder Stencil (Small/Large Ball)



Stencil Thickness = 0,125 mm

8-Ball Solder Stencil (Small/Large Ball)



Stencil Thickness = 0,125 mm

THERMAL CHARACTERISTICS

Thermal Impedance Values at Various Airflow Rates (Model data per JESD 51-7 and JESD 51-3)

Package		Thermal Impedance	Airflow (linear ft/minute)			
			0	150	250	500
Small Ball						
5-Ball	1S0P	$R_{\theta JA}$ (°C/W)	251.66	233.62	224.28	211.12
		$R_{\theta JC}$ (°C/W)	21.4	—	—	—
	1S2P	$R_{\theta JA}$ (°C/W)	154.32	152.05	150.73	148.72
		$R_{\theta JC}$ (°C/W)	18.75	—	—	—
6-Ball	1S0P	$R_{\theta JA}$ (°C/W)	236.83	219.01	210.02	197.39
		$R_{\theta JC}$ (°C/W)	21.03	—	—	—
	1S2P	$R_{\theta JA}$ (°C/W)	143.47	141.14	139.87	137.93
		$R_{\theta JC}$ (°C/W)	18.48	—	—	—
8-Ball	1S0P	$R_{\theta JA}$ (°C/W)	236.59	218.76	209.46	196.32
		$R_{\theta JC}$ (°C/W)	16.45	—	—	—
	1S2P	$R_{\theta JA}$ (°C/W)	139.87	137.69	136.34	134.34
		$R_{\theta JC}$ (°C/W)	14.80	—	—	—
Large Ball						
5-Ball	1S2P	$R_{\theta JA}$ (°C/W)	131.56	129.26	128	126.08
		$R_{\theta JC}$ (°C/W)	18.0	—	—	—
6-Ball	1S2P	$R_{\theta JA}$ (°C/W)	123.36	121.03	119.8	119.3
		$R_{\theta JC}$ (°C/W)	17.6	—	—	—
8-Ball	1S2P	$R_{\theta JA}$ (°C/W)	101.92	99.69	98.5	96.75
		$R_{\theta JC}$ (°C/W)	13.79	—	—	—

BOARD-LEVEL RELIABILITY DATA

Board-Level Reliability N_1 (cycles to first failure)	
NanoStar/NanoFree (YEA/YZA)	>1000 cycles

No underfill or adhesive was used, nor is required for these packages.

Test Parameters:
2 cycles/hr: –40 to +125°C
0.8-mm thick FR4 epoxy board
per IPC-9701, TC3, NTC-C

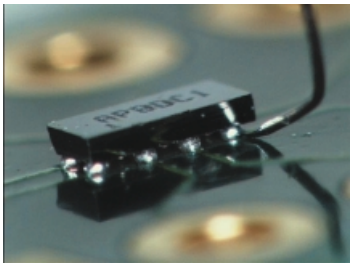
BOARD-MOUNTING PICK-UP TOOLS

Due to the package size and configuration, a rectangular or circular shaped pick-up tool is recommended. It is also recommended the tool have an outside diameter smaller than the package body, with a compliant tip. Recommended placement force is 200 gF.

WCSP TESTABILITY

Solder Balls Provide Easy Access

Due to the ideal placement of the solder balls along the outside of the package along with sufficient ball height, probe tips can easily create a dedicated contact to the individual pins.



ELECTRICAL CHARACTERISTICS

WCSP (YEA/YZA)

	R (Ω)	L (nH)	C (pF)		
			5-Ball	6-Ball	8-Ball
Mean	0.001	0.021	0.046	0.046	0.043

Note: Electrical package parasitic was achieved through electrical modeling and is based on a 3D model. Actual electrical data may differ slightly from simulated results.

Little Logic Product Portfolio Electrical Performance

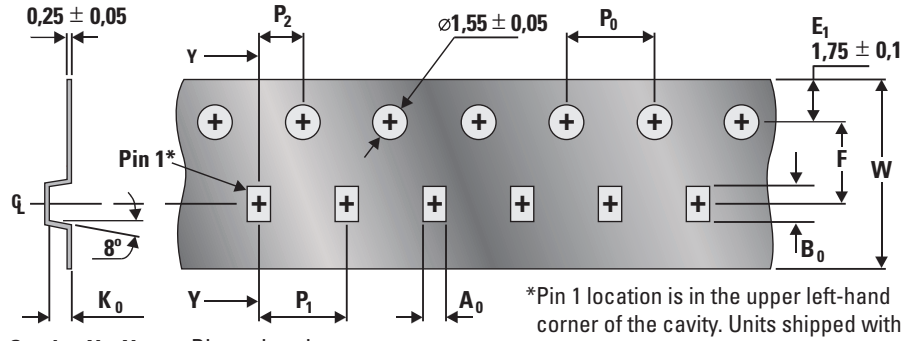
Family	Operating Voltage Range (V)	Optimized Voltage (V)	Propagation Delay (typ) (ns)	Output Drive (mA)	Input Tolerance (V)	I_{OFF} Protection
AUC	0.8 to 2.7	1.8	2.0	8	3.6	Yes
LVC	1.65 to 5.5	3.3	3.0	24	5.5	Yes
AHC	2.0 to 5.5	5	5.0	8	5.5	No
AHCT	4.5 to 5.5	5	5.0	8	5.5	No
CBT	4.5 to 5.5	5	0.25*	—**	5.5	Yes
CBTD	4.5 to 5.5	5	0.25*	—**	5.5	Yes
CBTLV	2.3 to 3.6	3.3	0.25*	—**	3.6	Yes

*The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance). The value listed is a maximum.

**The FET switch has no output drive. The drive current at the output terminal is determined by the drive current of the device connected at the input terminal of the FET switch.

PACKAGING TAPE AND REEL

Reel Tape Configuration (Small/Large Ball)



*Pin 1 location is in the upper left-hand corner of the cavity. Units shipped with balls down.

Dimensions	5- and 6-Ball	8-Ball
Pocket Width, A_0 (mm)	1,10 ± 0,05	1,10 ± 0,05
Pocket Length, B_0 (mm)	1,60 ± 0,05	2,10 ± 0,05
Pocket Depth, K_0 (mm)	0,56 ± 0,05	0,56 ± 0,05
Pocket Pitch, P_1 (mm)	4,0 ± 0,1	4,0 ± 0,1
Sprocket Hole-to-Pocket Centerline, F (mm)	3,50 ± 0,05	3,50 ± 0,05
Sprocket Hole-to-Pocket Offset, P_2 (mm)	2,0 ± 0,05	2,0 ± 0,05
Sprocket Hole Pitch, P_0 (mm)	4.,00 ± 0,1	4,00 ± 0,1
Tape Width, W (mm)	8,00 ± 0,3	8,00 ± 0,3
Reel Diameter (mm) Max.	178	178

REWORK PROCEDURE

There are several rework equipment vendors in the market offering well designed equipment and established processes. Air-Vac Engineering (www.air-vac-eng.com) has established NanoStar reflow profiles for both convection and contact heat (conduction) rework processes. A typical process for the convection using DRS-24NC equipment for a 0.056-inch thick FR4 board can be:

Eutectic Balls

1) Apply flux to component using Auto Flux feature of DRS24
2) Align device over pads
3) Place device on board
4) Raise nozzle .050"
5) Preheat board to 90°C, nozzle warming up 20% air flow, 100°C
6) Soak Stage—20% air flow, 200°C, 90 seconds
7) Ramp Stage—20% air flow, 300°C, 30 seconds
8) Reflow Stage—25% air flow, 325°C, 55 seconds
9) Cooldown Stage—40% air flow, 25°C, 30 seconds

Pb-Free Balls

Apply flux to component using Auto Flux feature of DRS24:

1) Align device over pads
2) Place device on board
3) Raise nozzle .050"
4) Preheat board to 90°C, nozzle warming up 20% air flow, 125°C
5) Soak Stage—20% air flow, 225°C, 90 seconds
6) Ramp Stage—20% air flow, 335°C, 30 seconds
7) Reflow Stage—25% air flow, 370°C, 65 seconds
8) Cooldown Stage—40% air flow, 25°C, 50 seconds

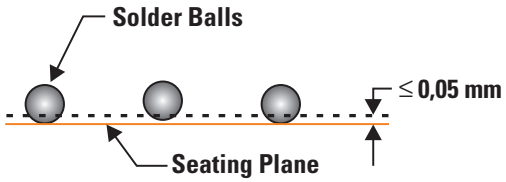
The recommended tooling for both the convection and conduction processes is:

Process	Nozzle Description	Nozzle Part Number	Tray
Hot Gas	NanoStar .0365" x .0560" x .0155" 5-ball	N09DVG-7	A04DVG06
Contact	NanoStar .0365" x .0560" x .0155" 5-ball	CE037-056TI	A0201X8-OX

GEOMETRIC DIMENSIONAL TOLERANCES

Coplanarity

This package meets a coplanarity of 0,05 mm as shown. Coplanarity is defined as a unilateral tolerance zone measured upward from the seating plane. (Reference ASME Y14.5M - 1994)



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LITERATURE

Selection Guides	**Lit. Number**
Logic Selection Guide	SDYU001*
Advanced Bus Interface Logic Selection Guide	SCYT126*
Design Considerations for Logic Products, Volume 3	SDYA019

Data Books

Little Logic Data Book	SCED010*
Logic Pocket Data Book	SCYD013*
Signal Switch Data Book	SCDD003*
AHC/AHCT Data Book	SCLD003B

Application Notes

Application of the Texas Instruments AUC Sub-1-V Little Logic Devices	SCEA027*
Selecting the Right Texas Instruments Signal Switch	SZZA030*

Brochures/Product Bulletins	**Lit. Number**
Logic Reference Guide	SCYB004
AUC Product Brochure	SCEB011
Bus Switches (CBT & CBTLV) Product Bulletin	SCDB002A

Application/Product Clips

1G97/98 Configurable Multi-Function Devices Product Clip	SCYB010*
NanoStar/NanoFree Product Clip	SCYB011
LVC1G3157 & LVC2G53 Analog Switches Application Clip	SCYB014*

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