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INTEL DEVELOPER FORUM

Silicon Technology Leadership for the Mobility Era

Mark Bohr, Intel Senior Fellow

SPCS008

Agenda

- Transistor Scaling Trends
- 32 nm SoC Technology
- 22 nm CPU Technology
- 22 nm SoC Technology

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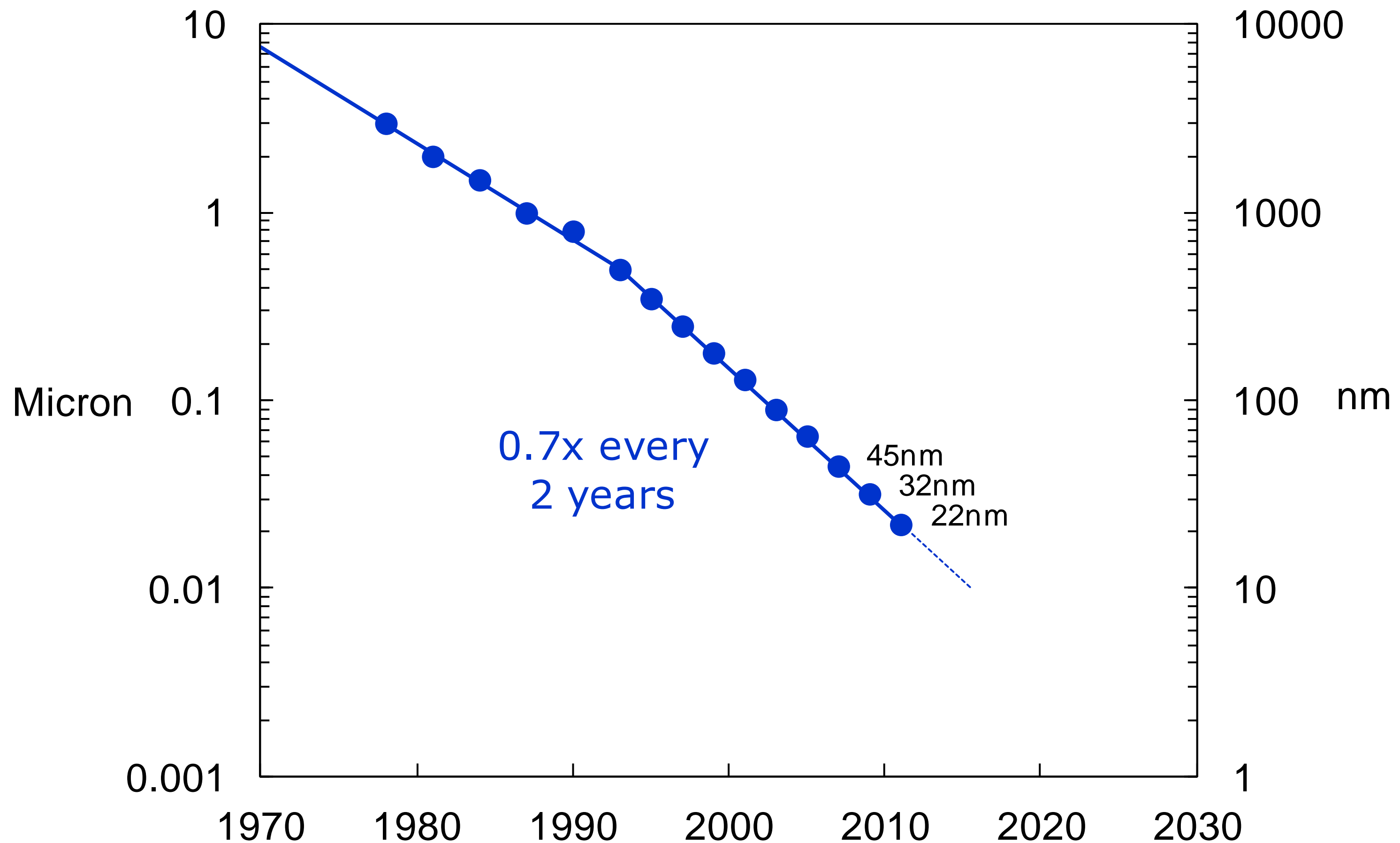
Agenda

- Transistor Scaling Trends
- 32 nm SoC Technology
- 22 nm CPU Technology
- 22 nm SoC Technology

Transistor Scaling



Transistor dimensions scale to improve performance, reduce power and reduce cost per transistor

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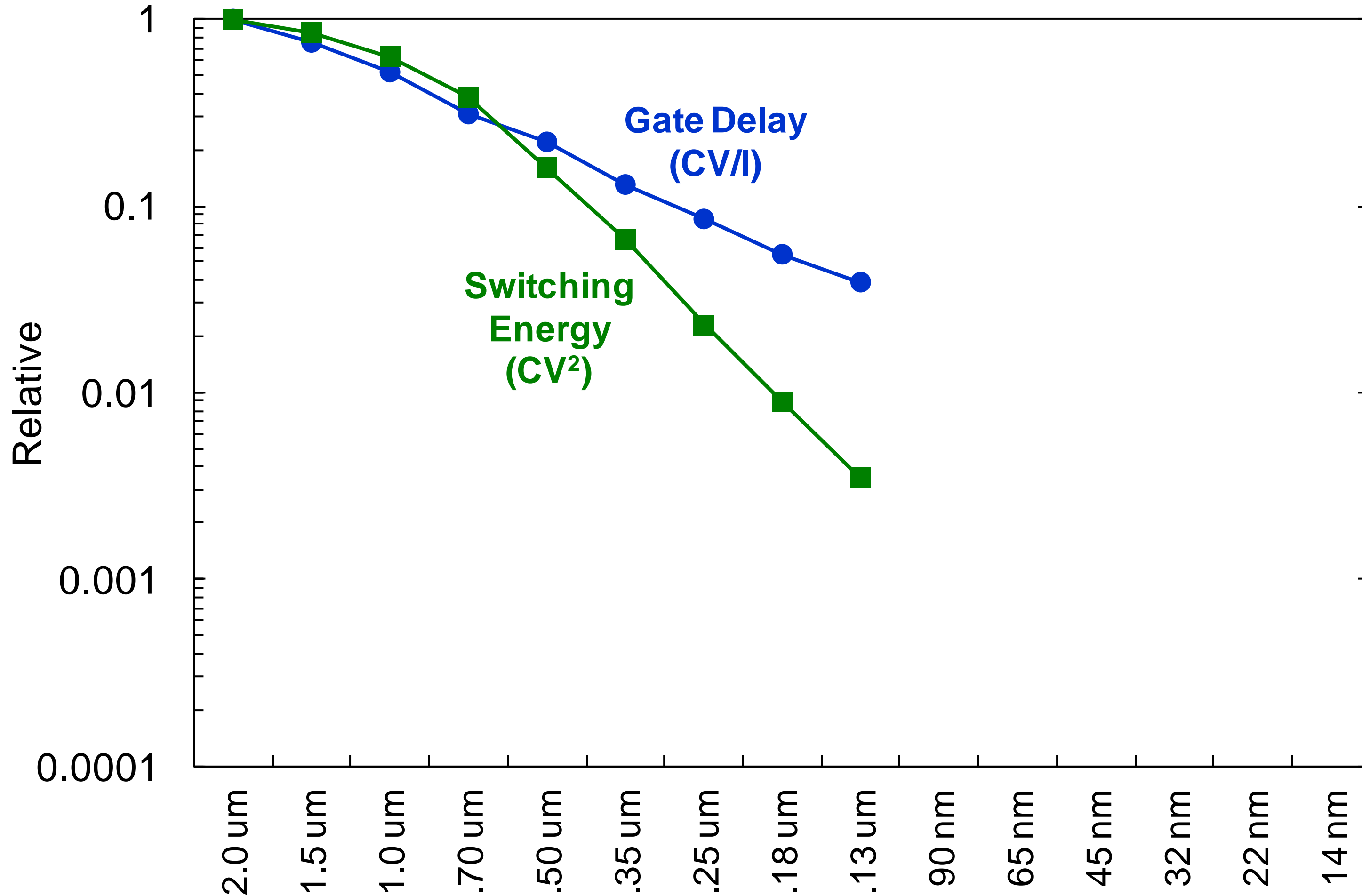
Transistor Performance and Power



"Classical" transistor scaling provided improvements in performance (gate delay) and active power (switching energy)

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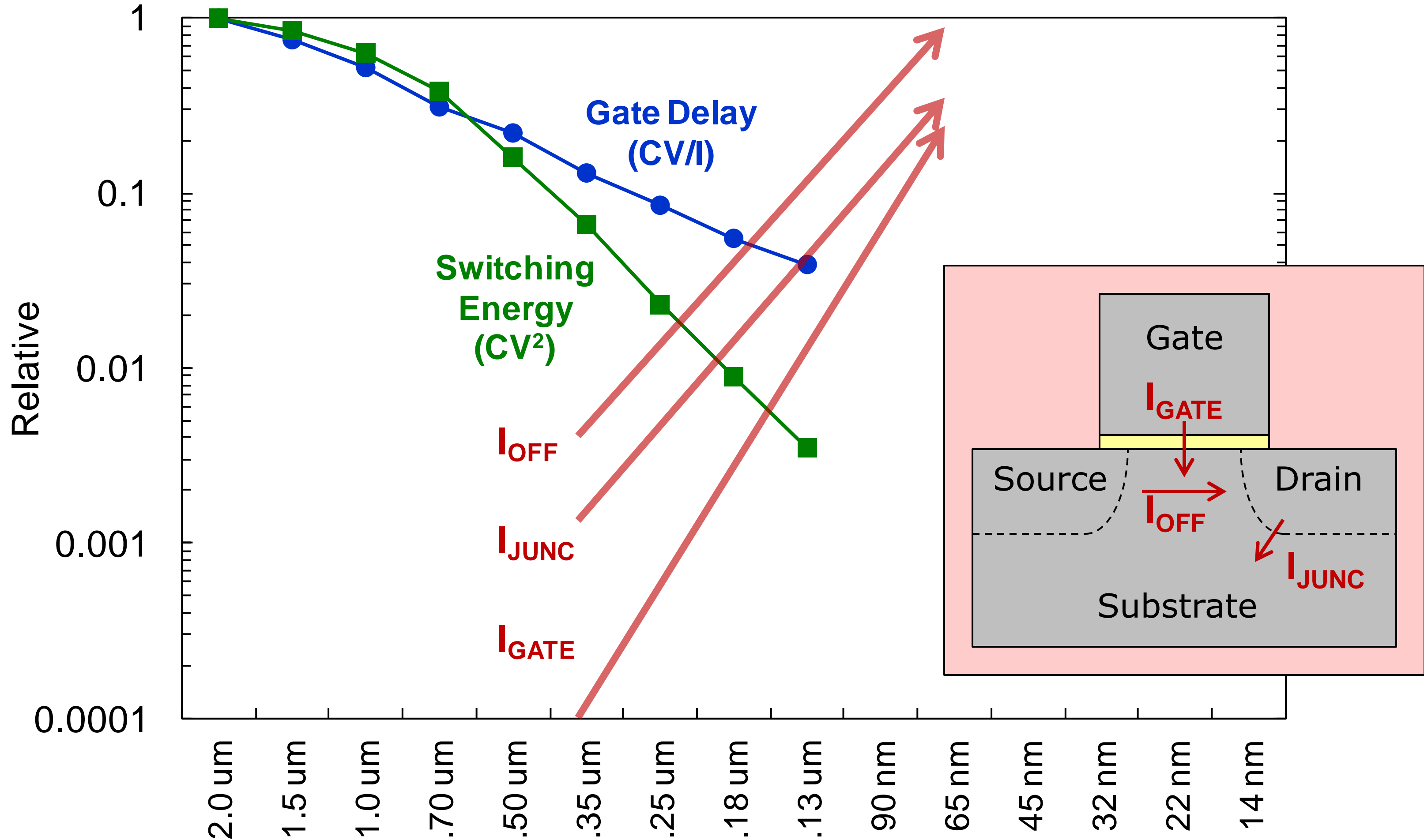
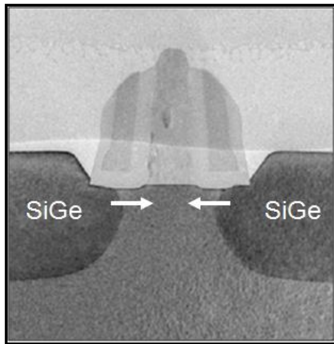
Transistor Performance and Power

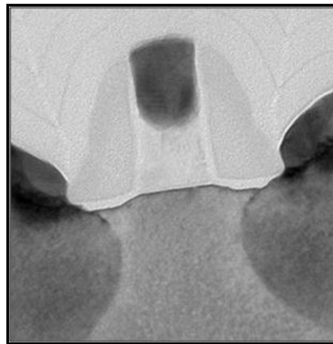


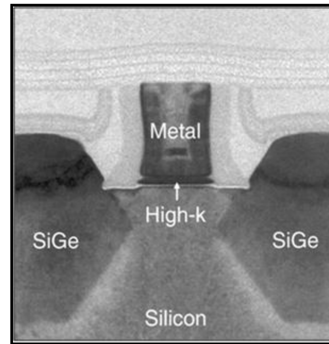
... but at the expense of increased leakage current

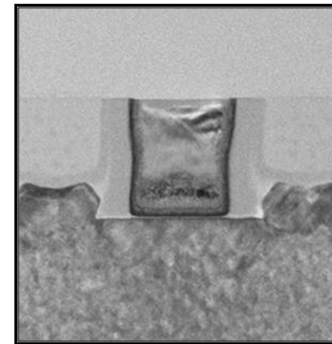
Non-Classical Scaling

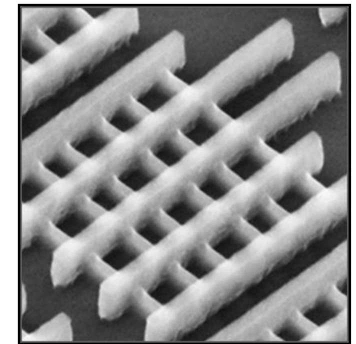
90 nm	65 nm	45 nm	32 nm	22 nm
2003	2005	2007	2009	2011











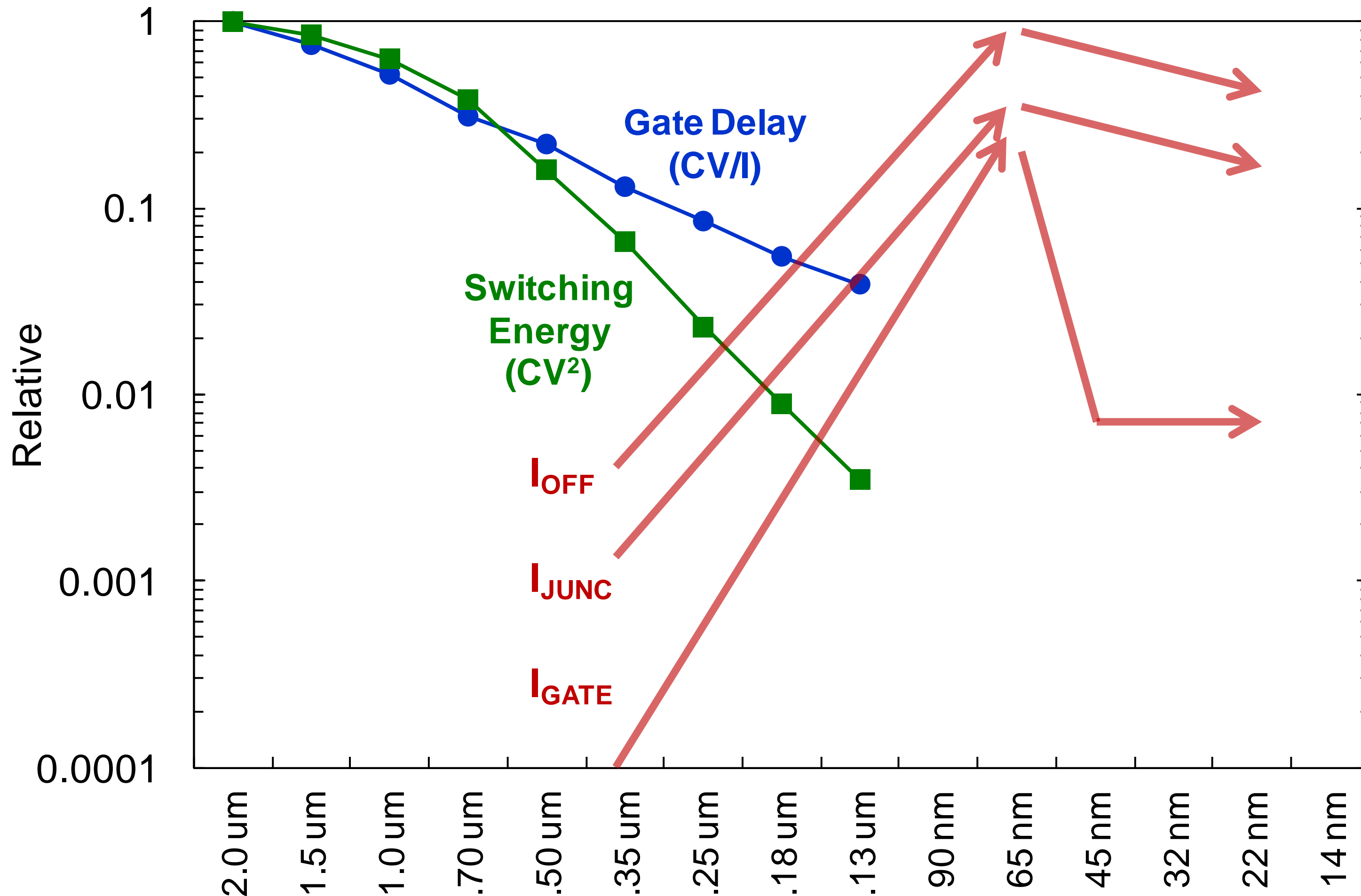
Strained Silicon

High-k Metal Gate

Tri-Gate

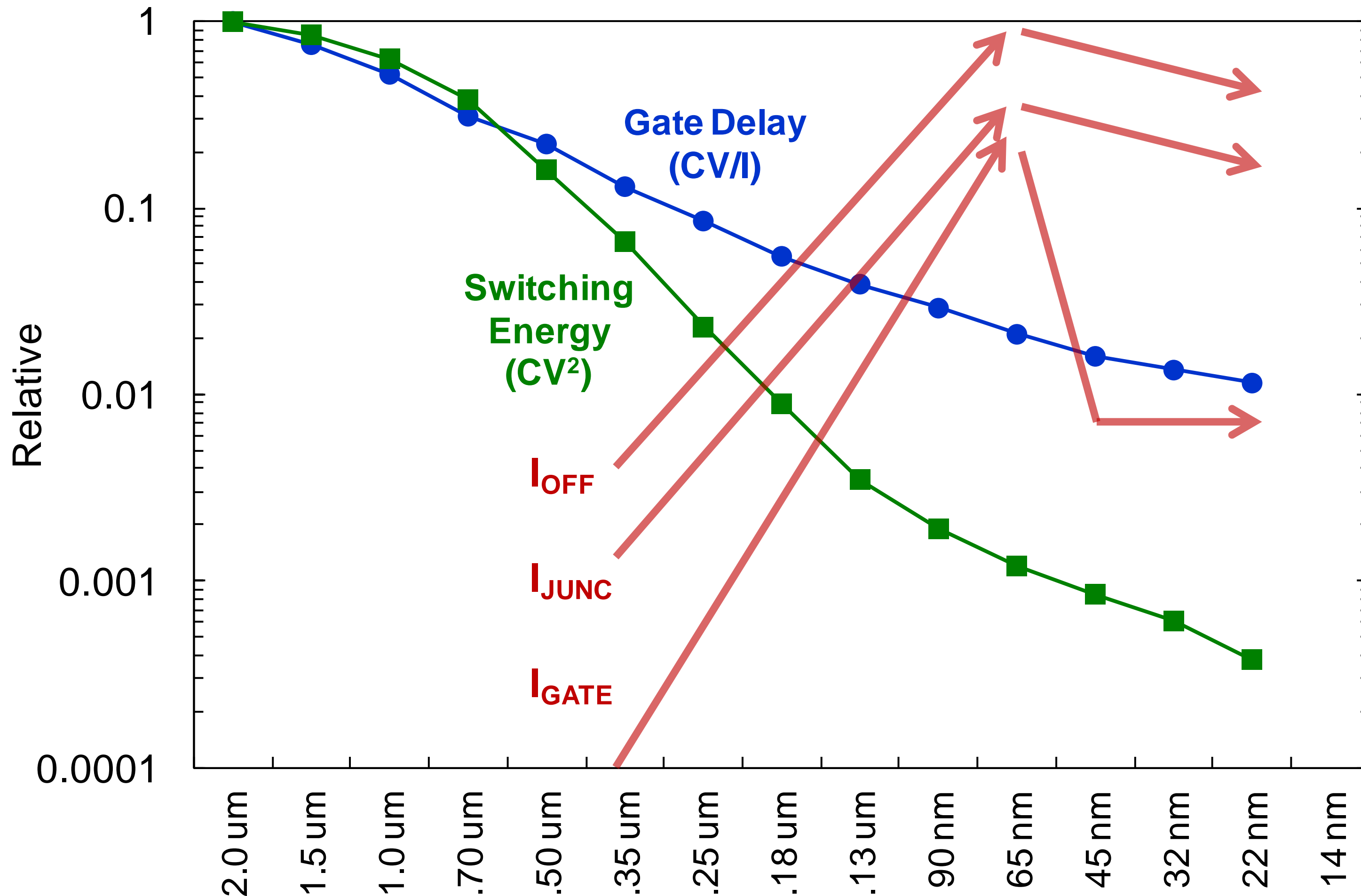
Scaling now requires continual innovations in transistor structure and materials

Transistor Performance and Power



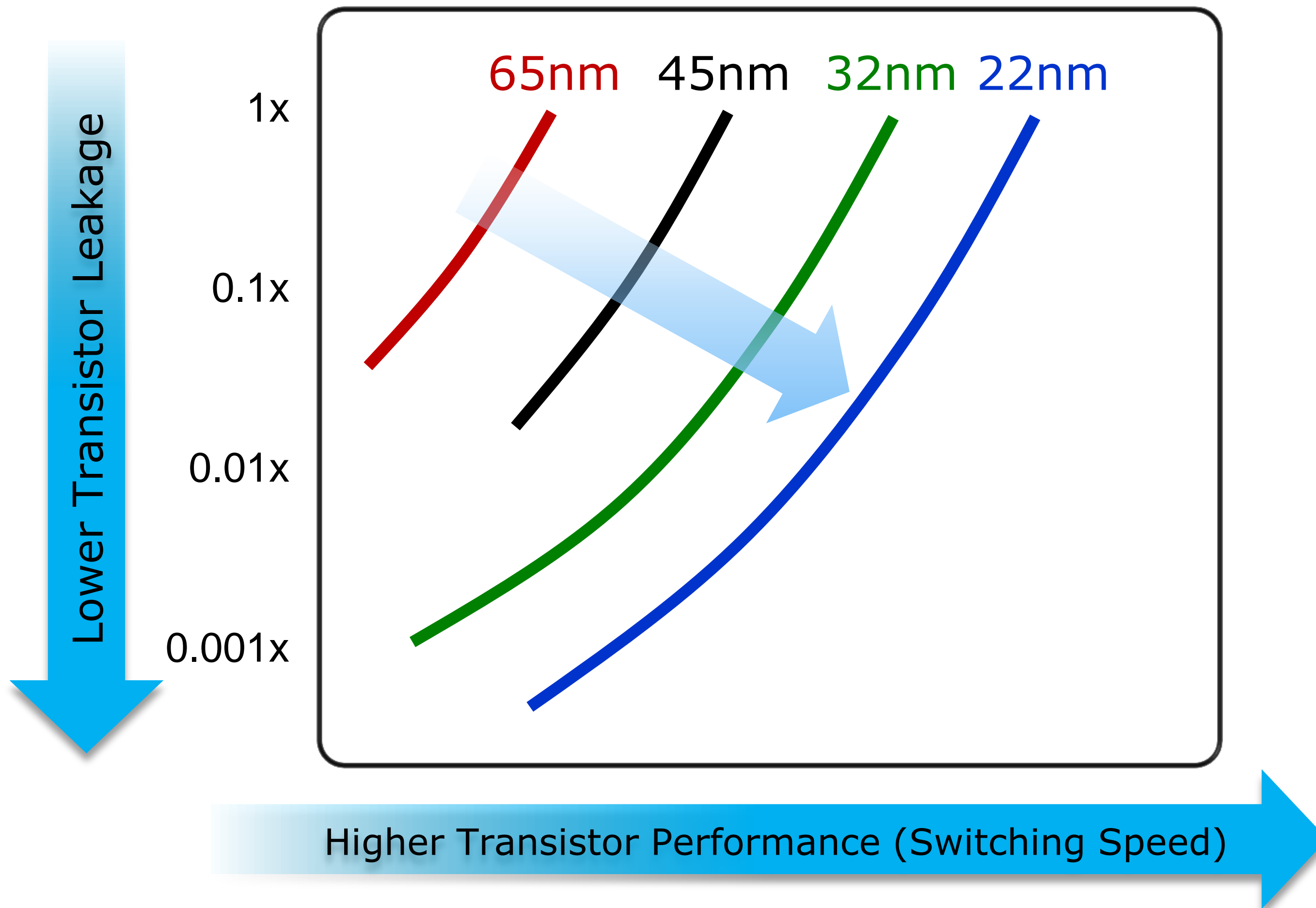
Transistor scaling now focuses on reducing leakage

Transistor Performance and Power



… and continues to improve performance and power

Transistor Performance vs. Leakage



Transistors now improve on both performance and leakage vectors

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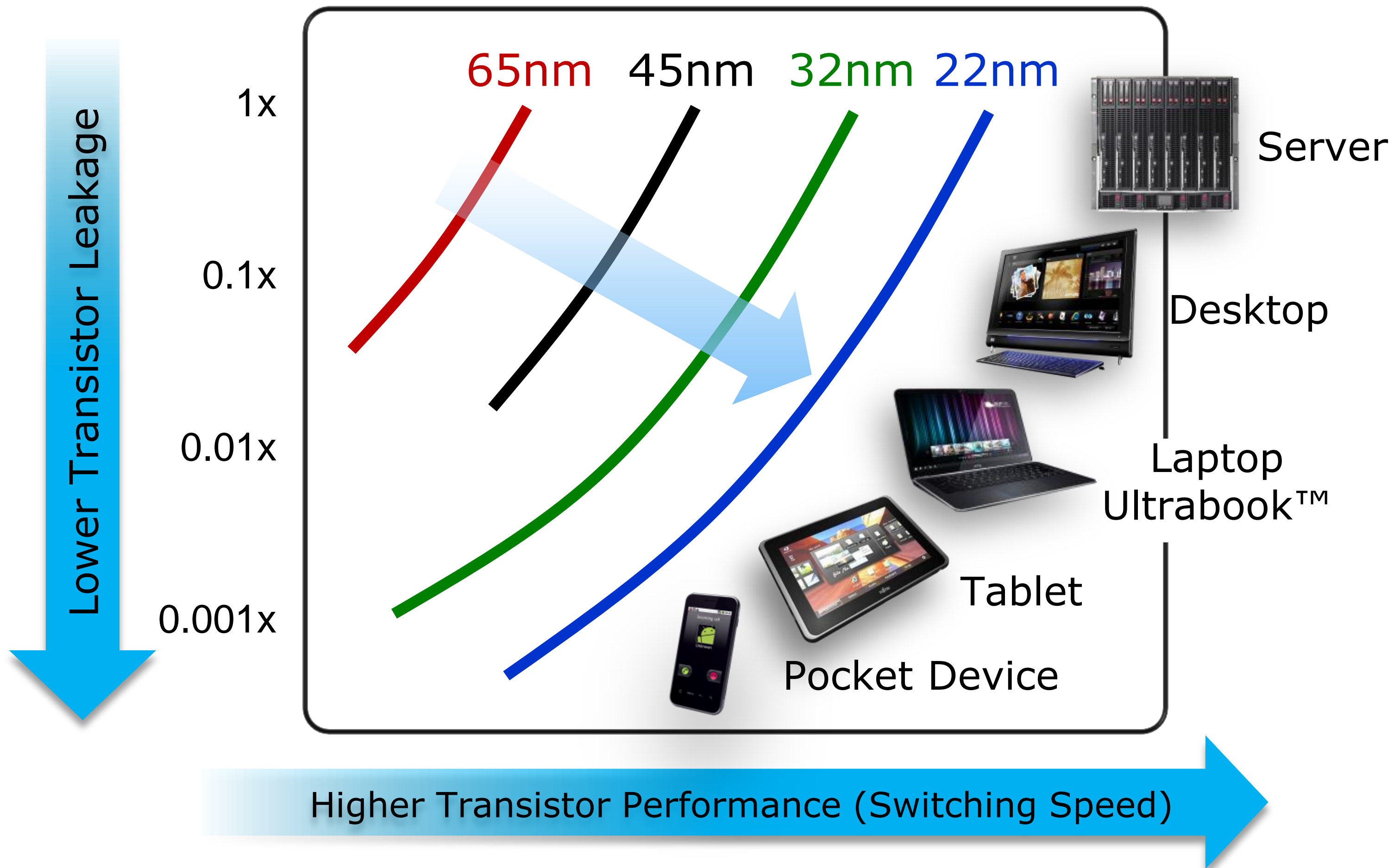
Transistor Performance vs. Leakage



Wider range of transistors to support a wider range of products

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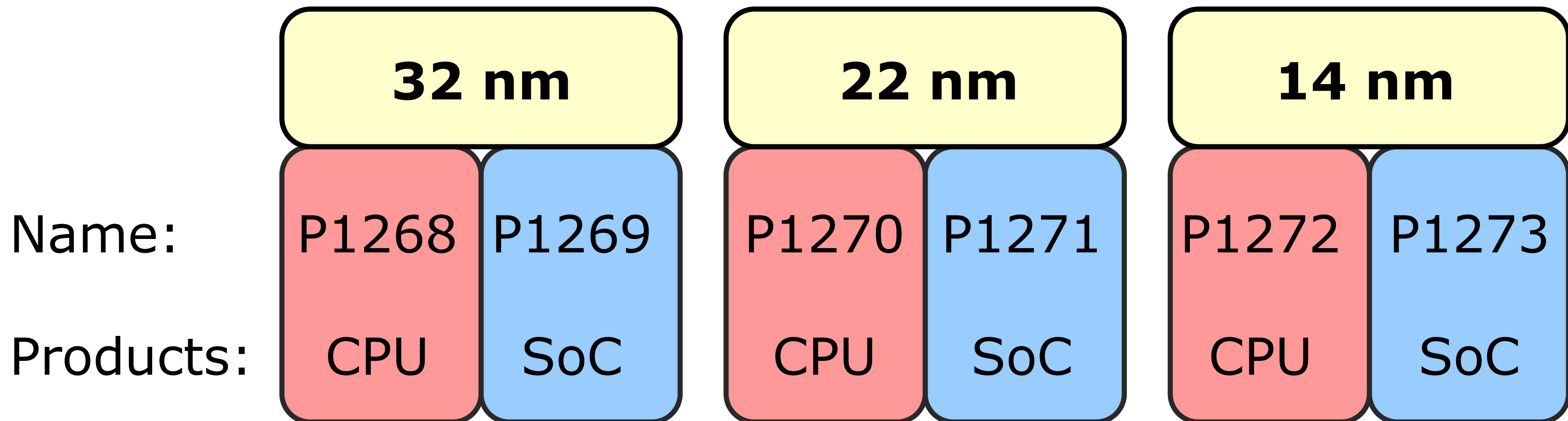
Intel® Technology Roadmap



Intel develops both CPU and SoC versions of each generation

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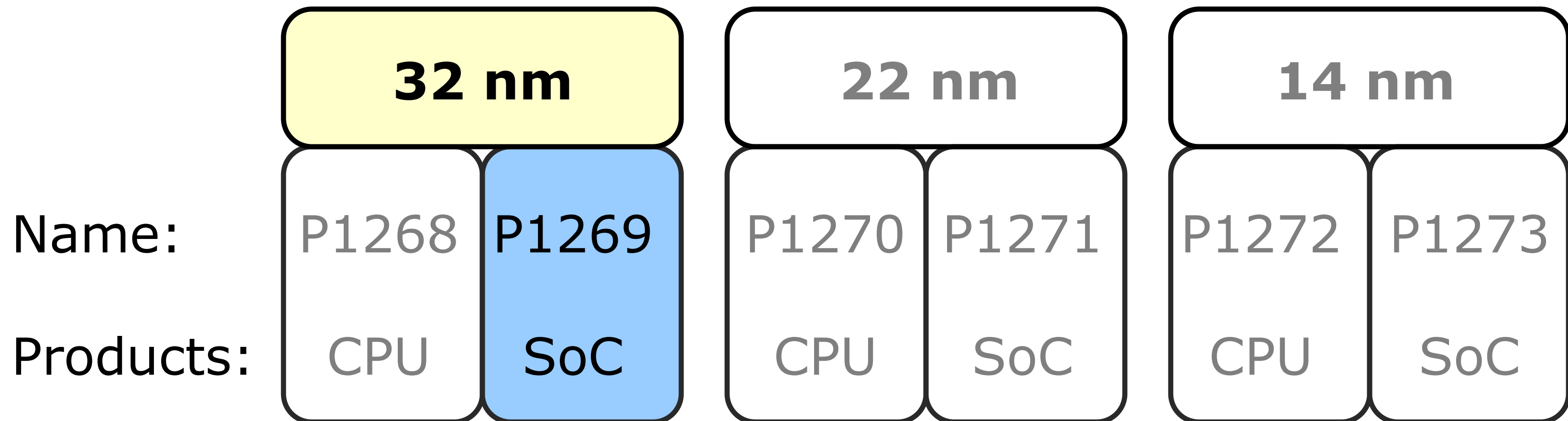
Intel® Technology Roadmap



Intel develops both CPU and SoC versions of each generation

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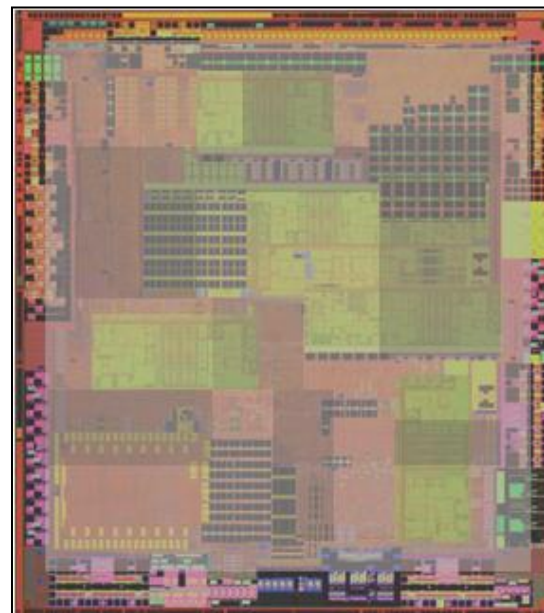
Low Power Smartphone Products

Medfield Phone



32 nm Intel® Atom™ processor (Medfield) SoC

432 million transistors, 64 mm^2

Low Power Smartphone Products

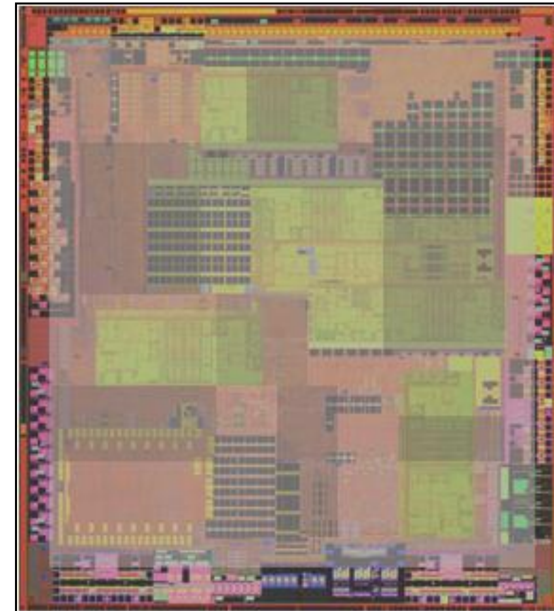
32 nm SoC Technology Feature Menu

Logic Transistor	I/O Trans Voltage	Metal	Advanced Passives	Embedded Memory
High Performance	1.2V Low Power	9 Layer High Perf	Precision Resistor	Dense SRAM
Std Performance	1.8V Thick Gate	7-11 Layer Hi Dense	Precision Capacitor	Low Voltage SRAM
Low Power	3.3V Thick Gate		High Q Inductor	High Speed SRAM

32 nm SoC process offers a rich mix-and-match feature set

Intel Developer Forum, Sep. 2009

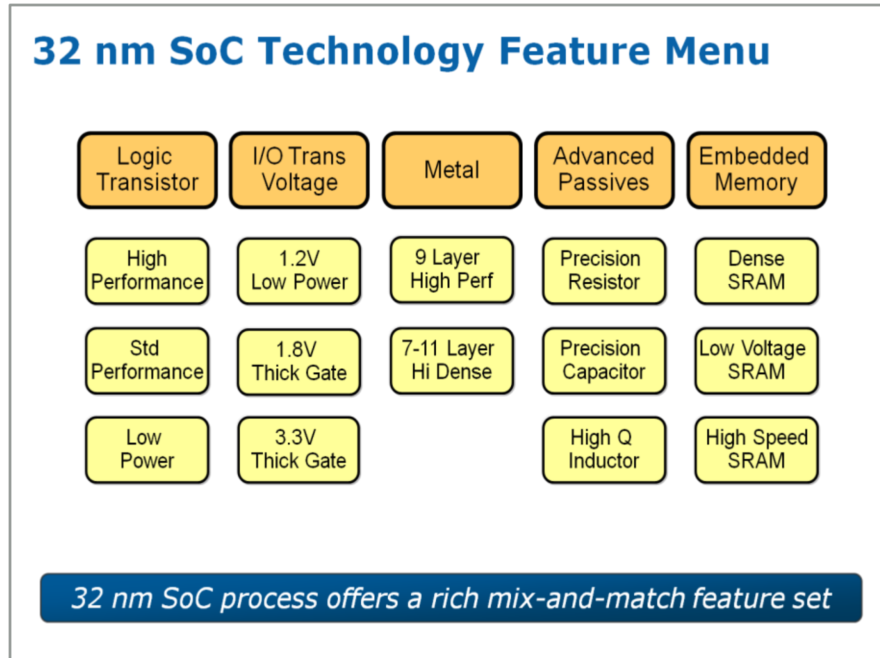
32 nm SoC Technology



32 nm Intel® Atom™ processor (Medfield) SoC

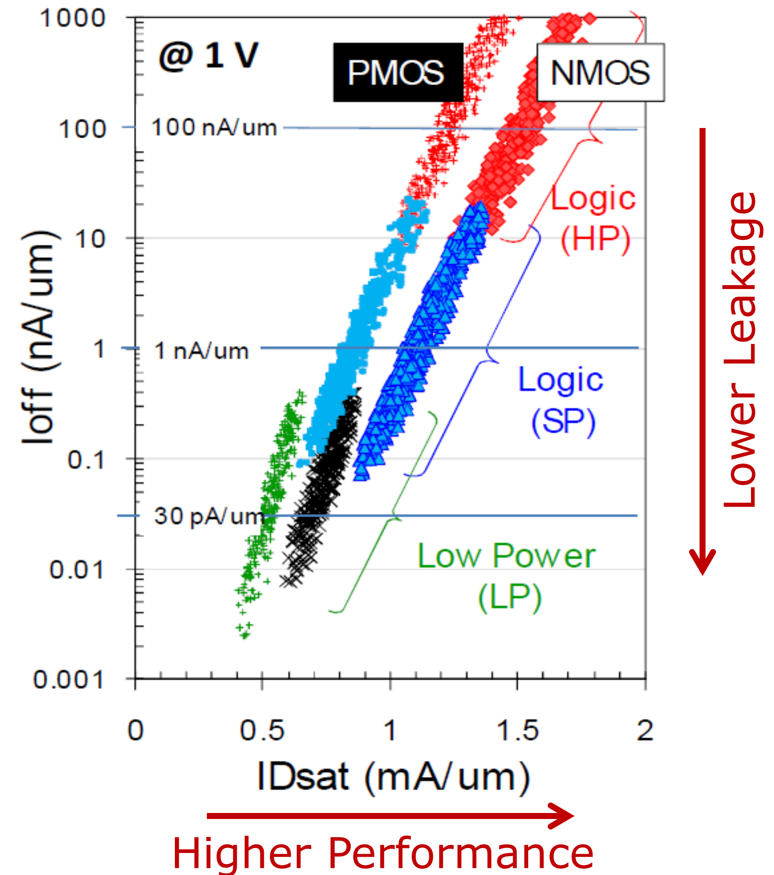
432 million transistors, 64 mm^2

Low Power Smartphone Products



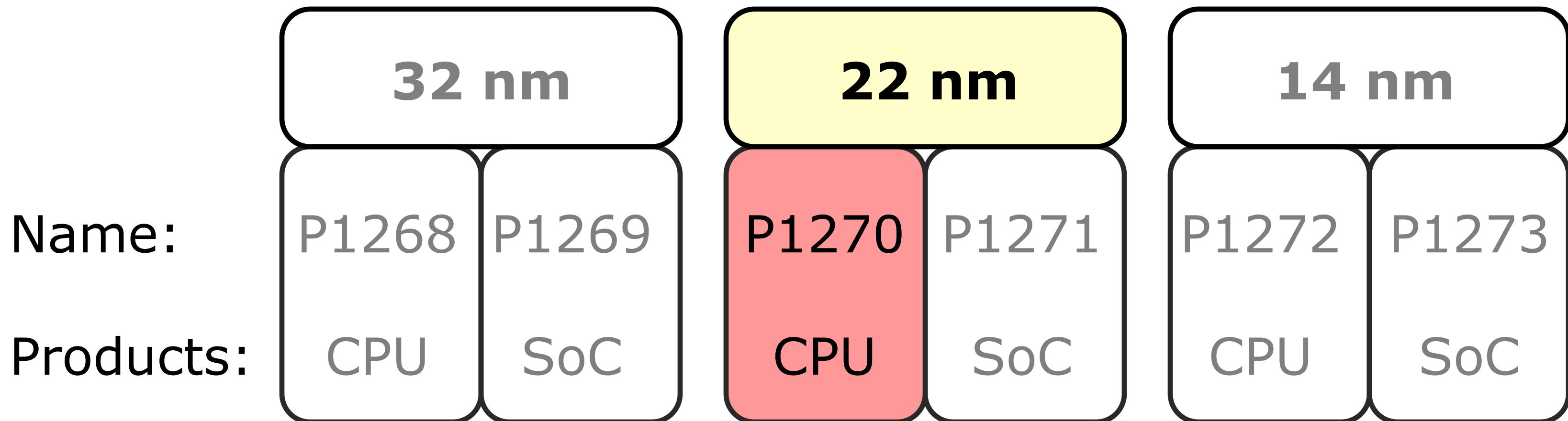
Intel Developer Forum, Sep. 2009

32 nm SoC Technology



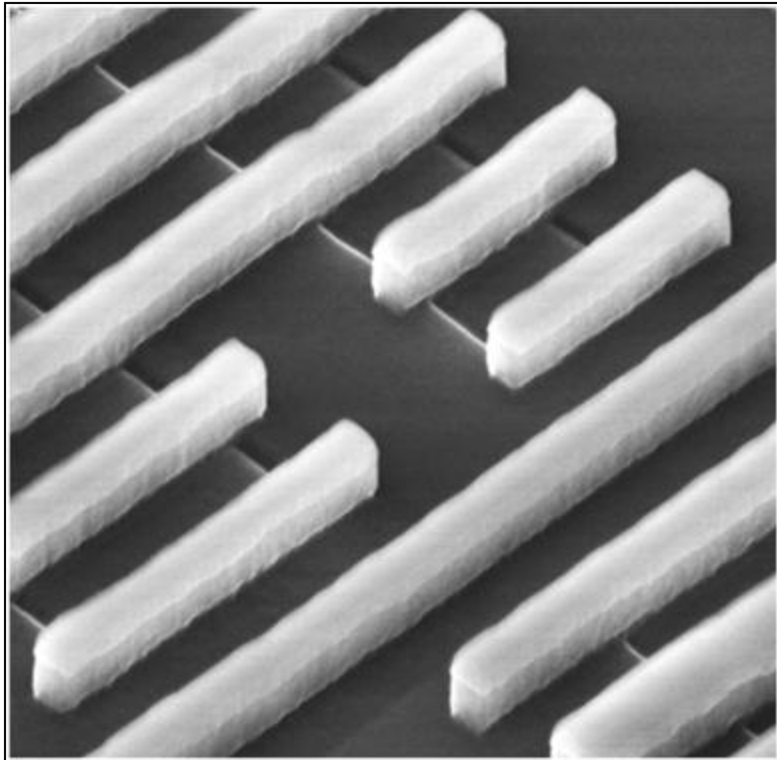
32 nm SoC transistors range from high performance to low power

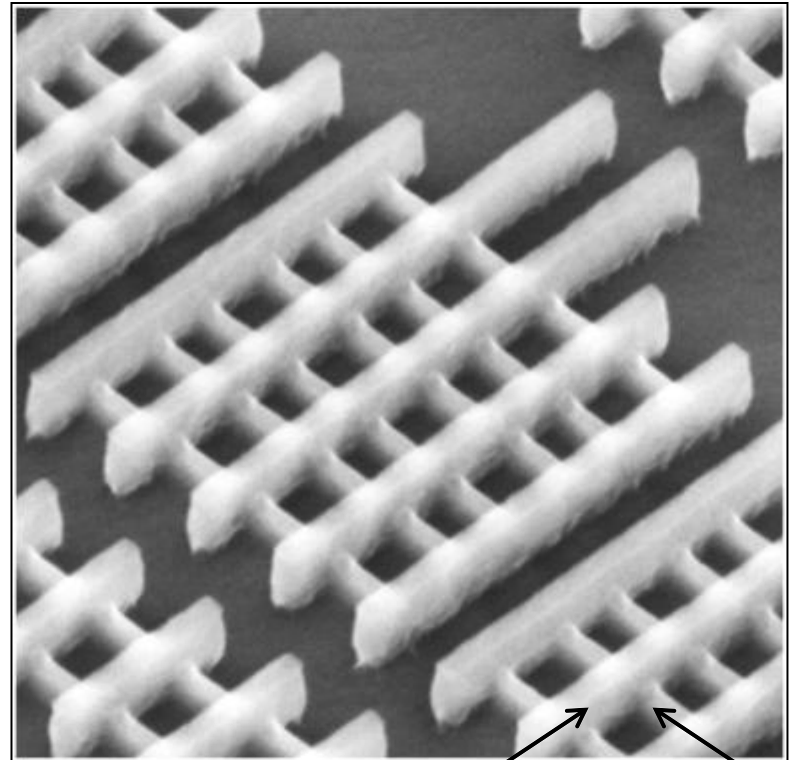
Intel® Technology Roadmap



32 nm Planar Transistors

22 nm Tri-Gate Transistors





22 nm generation introduces revolutionary 3-D Tri-Gate transistors

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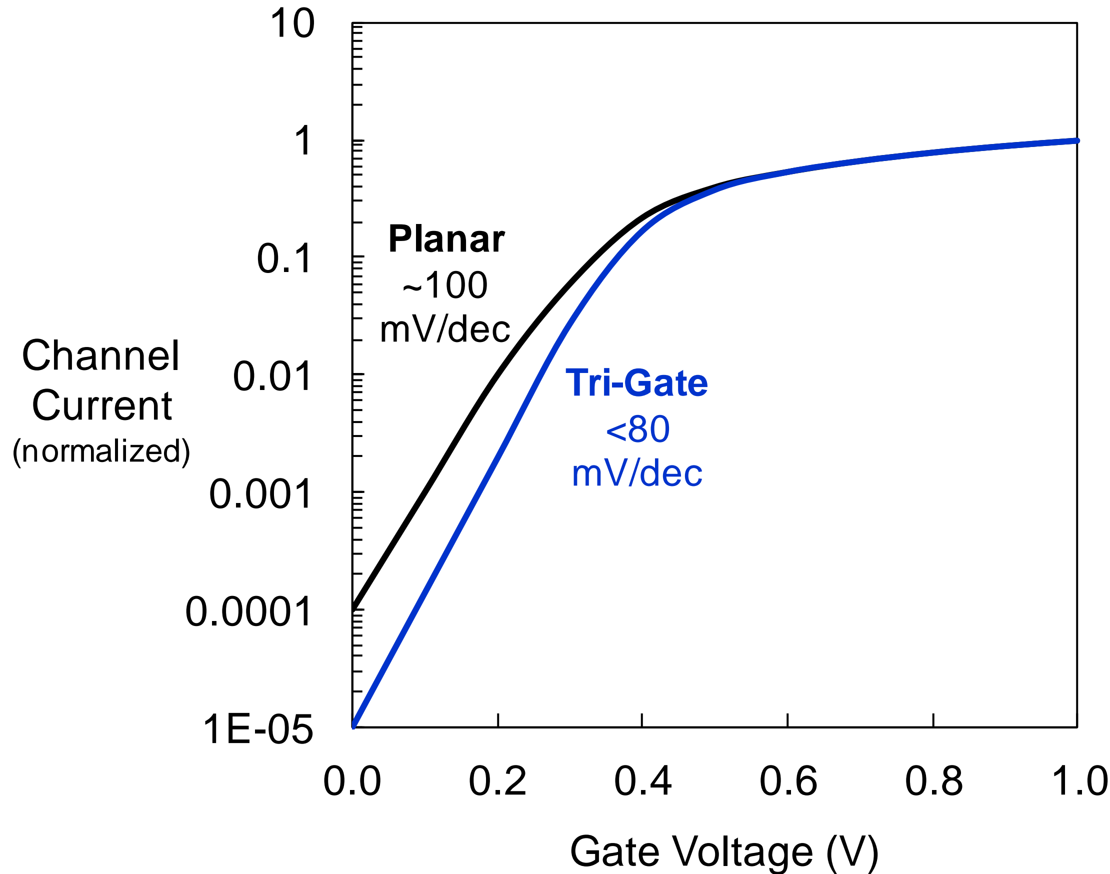
Fully Depleted Device



Tri-Gate transistors are fully depleted devices offering a steeper sub-threshold slope

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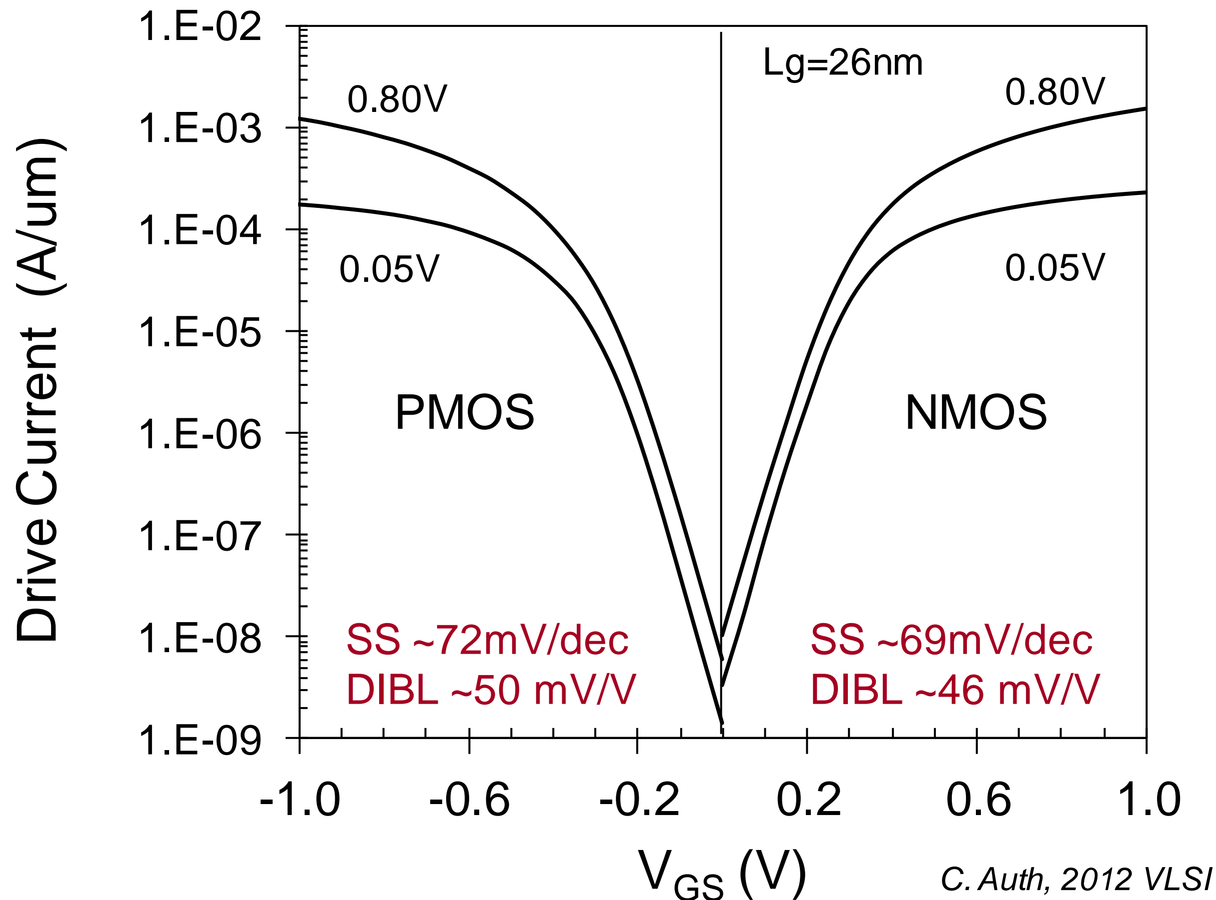
22 nm Tri-Gate I-V Curves



Tri-Gate provides steepest sub-threshold slope and best short channel (DIBL) values of any technology in manufacturing

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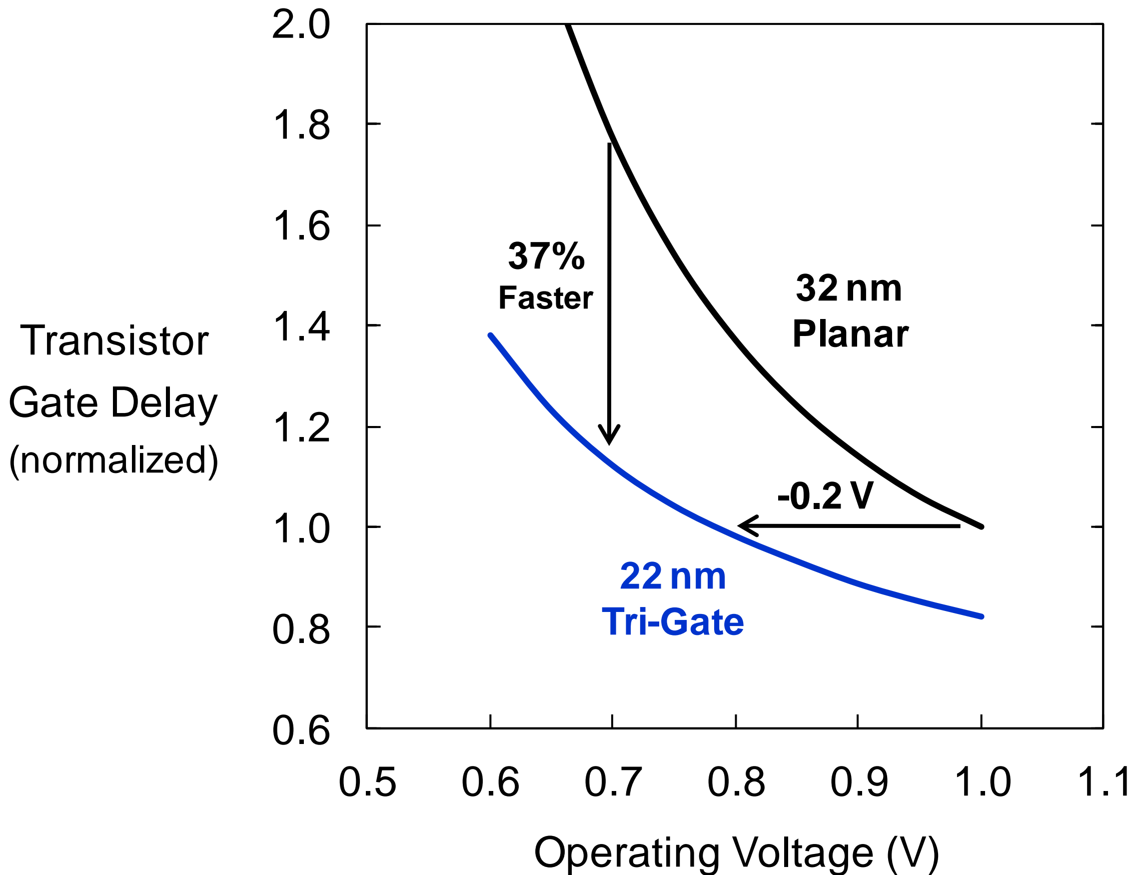
Performance/Power Benefits



Tri-Gate provides 37% speed up at low voltage or 50% active power reduction at same performance

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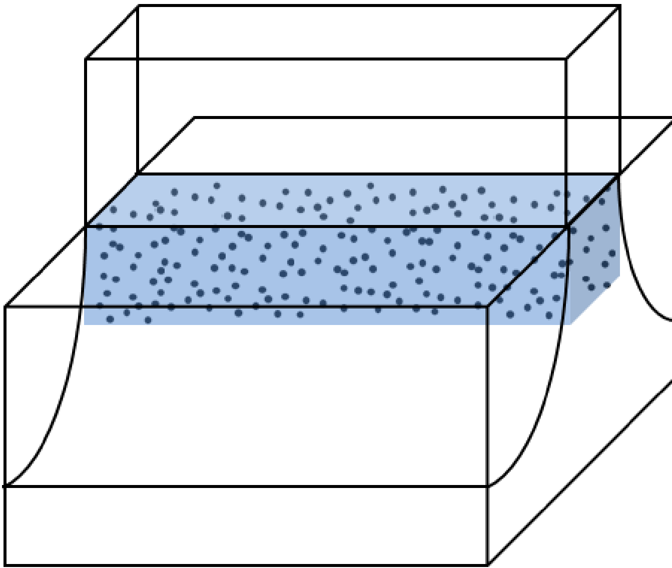
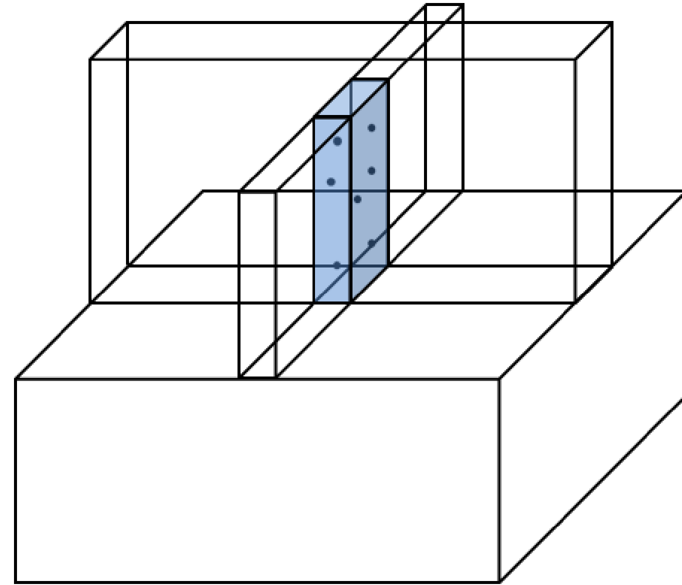
Reduced Channel Doping

Planar

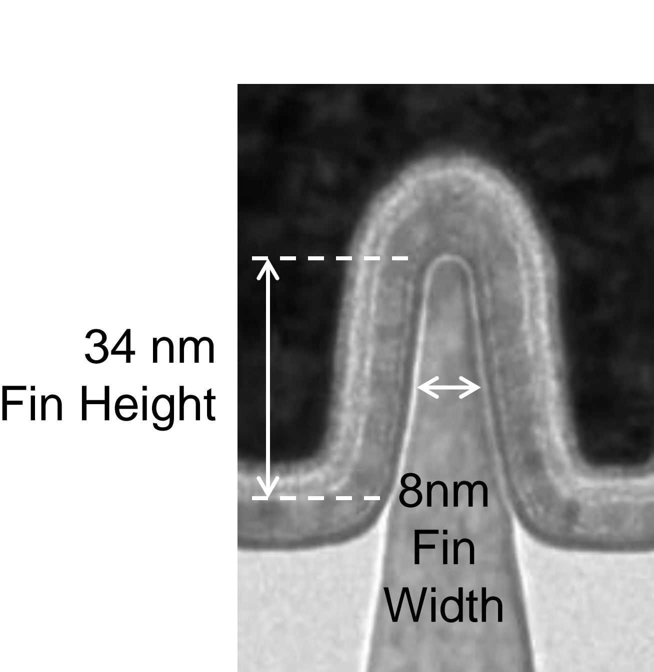


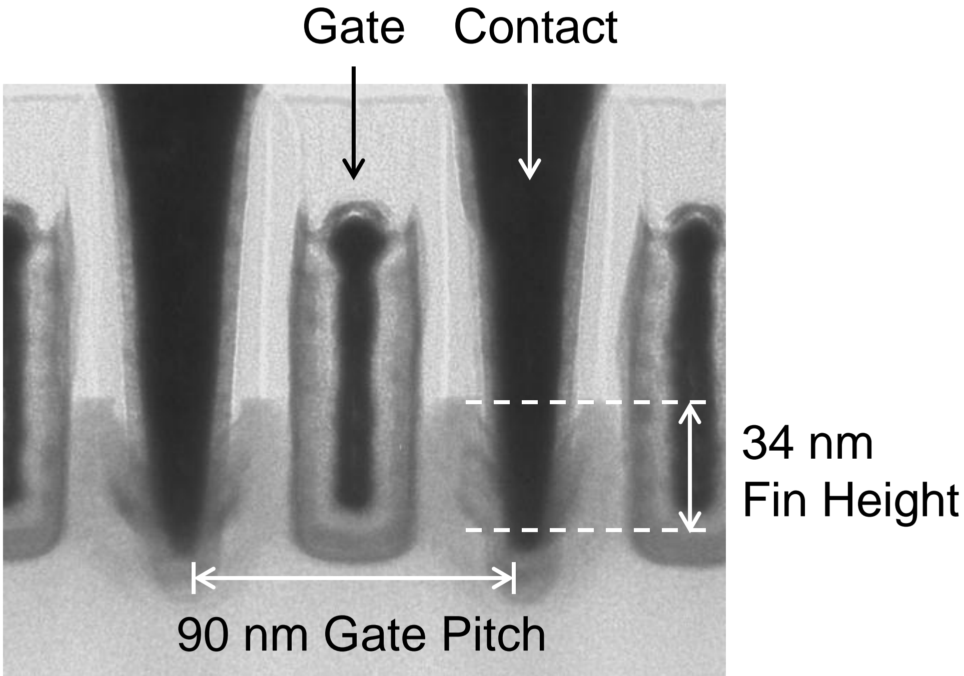
Tri-Gate



Fully depleted Tri-Gate structure has reduced channel doping, providing improved performance and reduced variability

22 nm Tri-Gate Transistors





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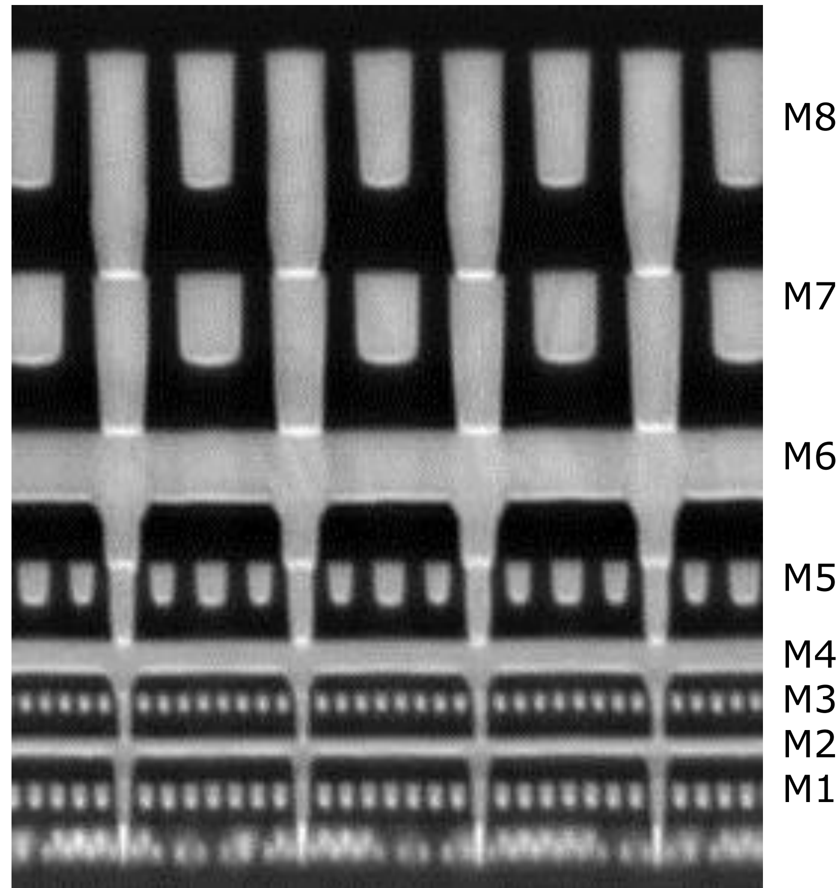
22 nm Interconnects

Layer	Pitch
TM	14 um
M8	360 nm
M7	320 nm
M6	240 nm
M5	160 nm
M4	112 nm
M3	80 nm
M2	80 nm
M1	90 nm



Minimum pitch scaled ~0.7x from 32 nm for ~2x transistor density improvement

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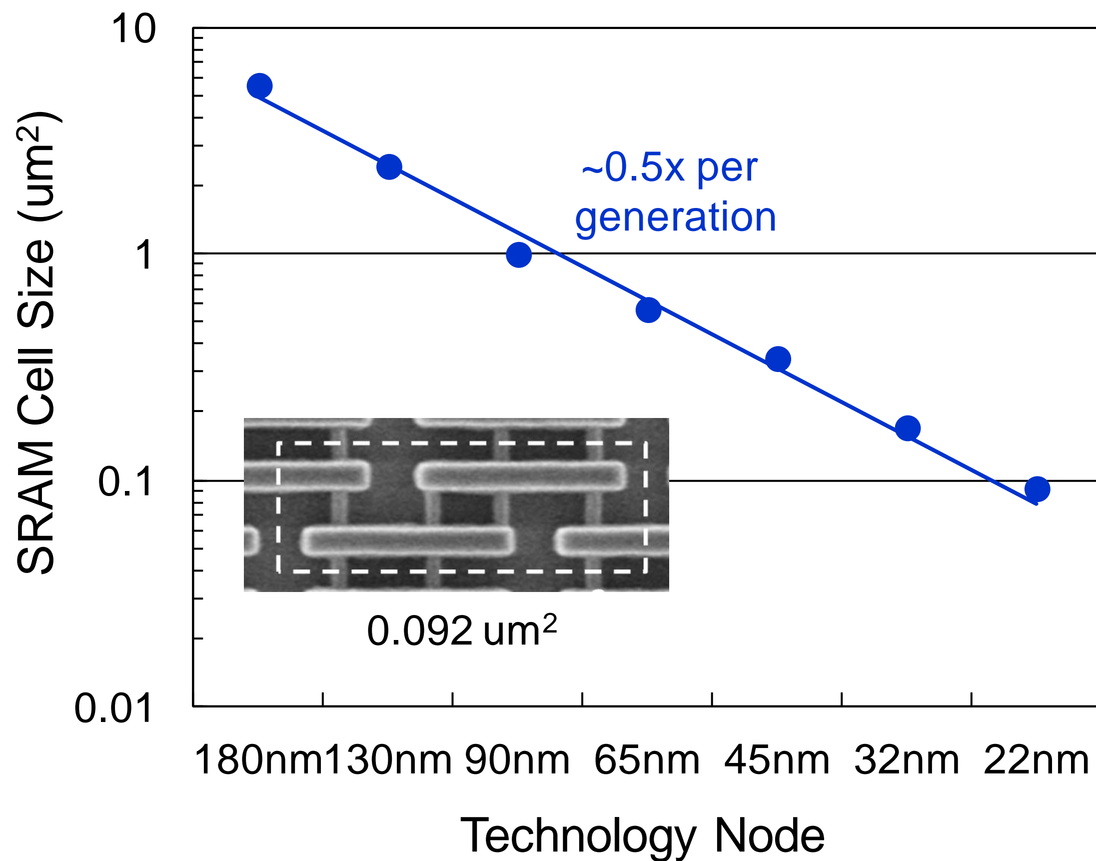
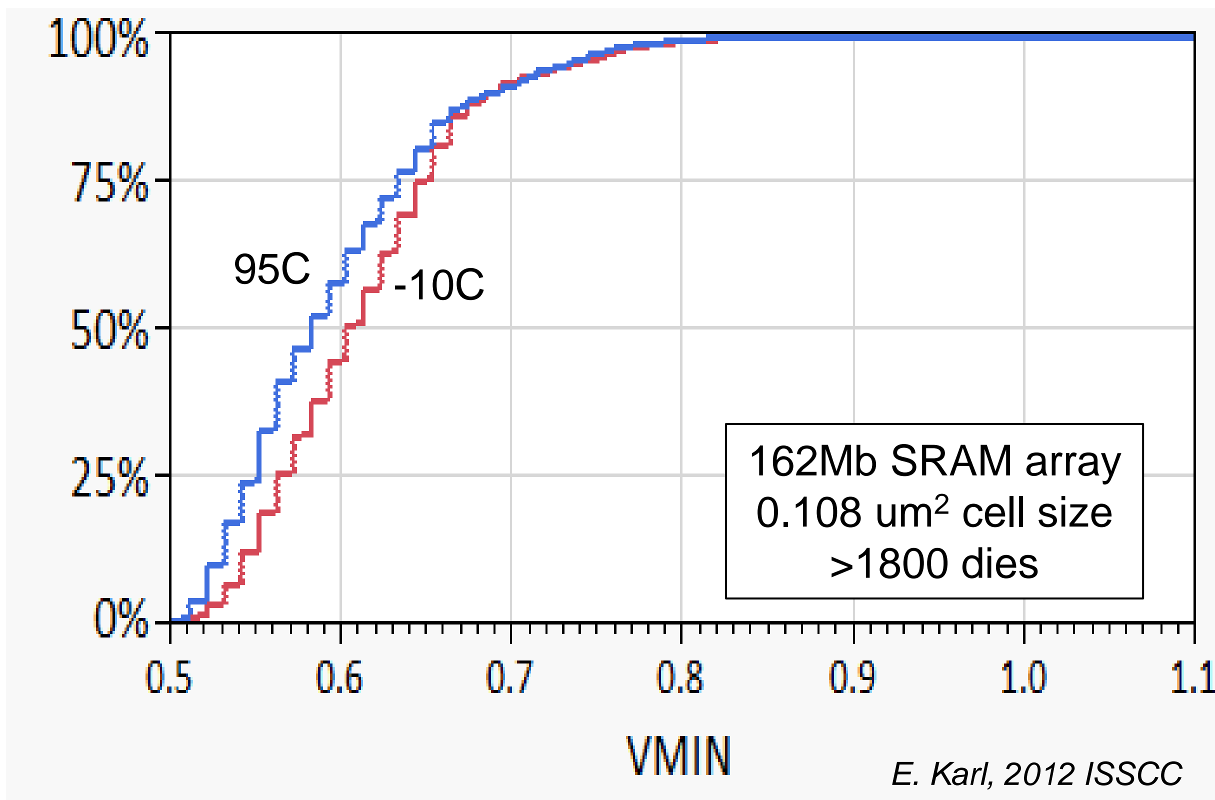
SRAM Cells



0.092 um² and 0.108 um² SRAM cells optimized for density and performance/power

SRAM Array V_{MIN}



0.60V medium active V_{MIN} for low power applications

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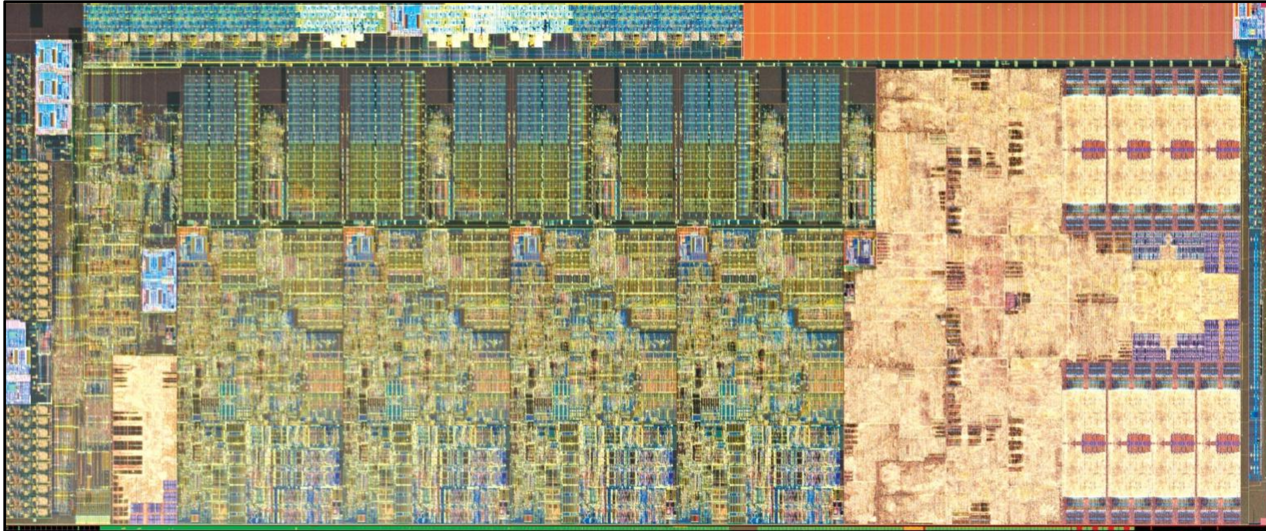
3RD Generation Intel® Core™ Processor

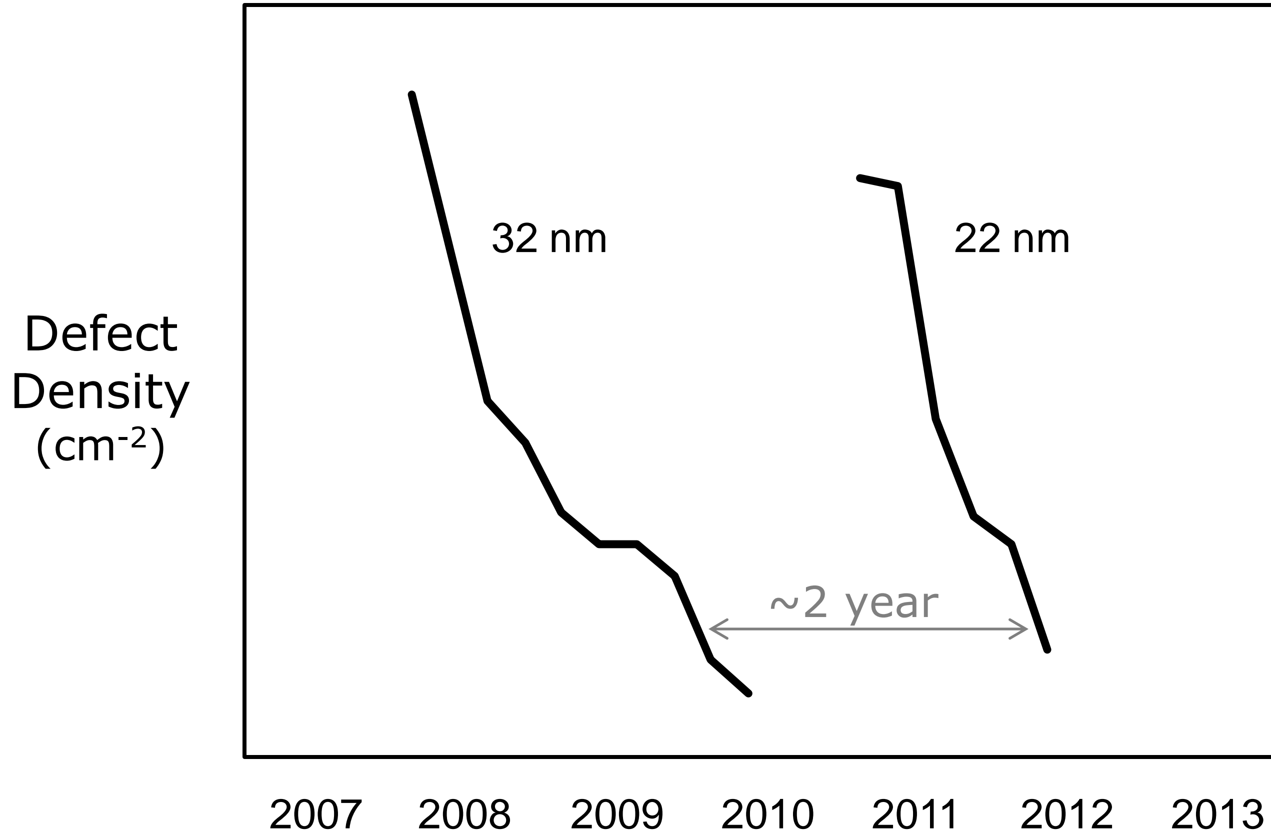


22 nm Tri-Gate Technology

4 Cores + Integrated Graphics

1.4 Billion Transistors, 160 mm^2

22 nm Defect Density Trend



22 nm defect density now at low levels needed for volume manufacturing

22 nm Manufacturing Fabs

D1D Oregon ✓

D1C Oregon

Fab 32 Arizona ✓

Fab 28 Israel ✓

Fab 12 Arizona

✓ In production 2Q '12

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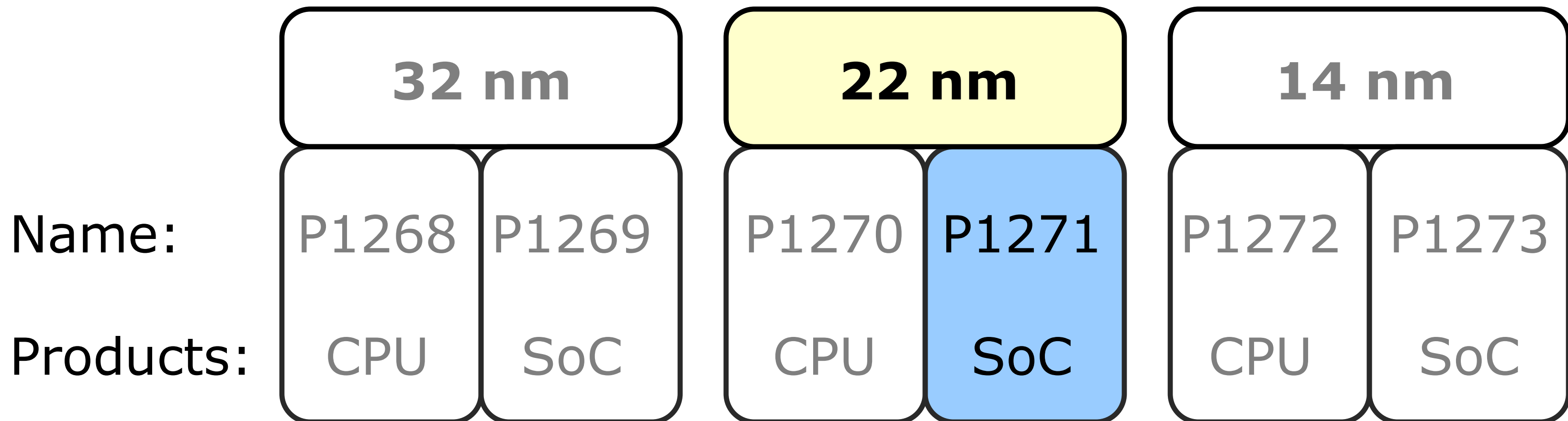
Intel® Technology Roadmap



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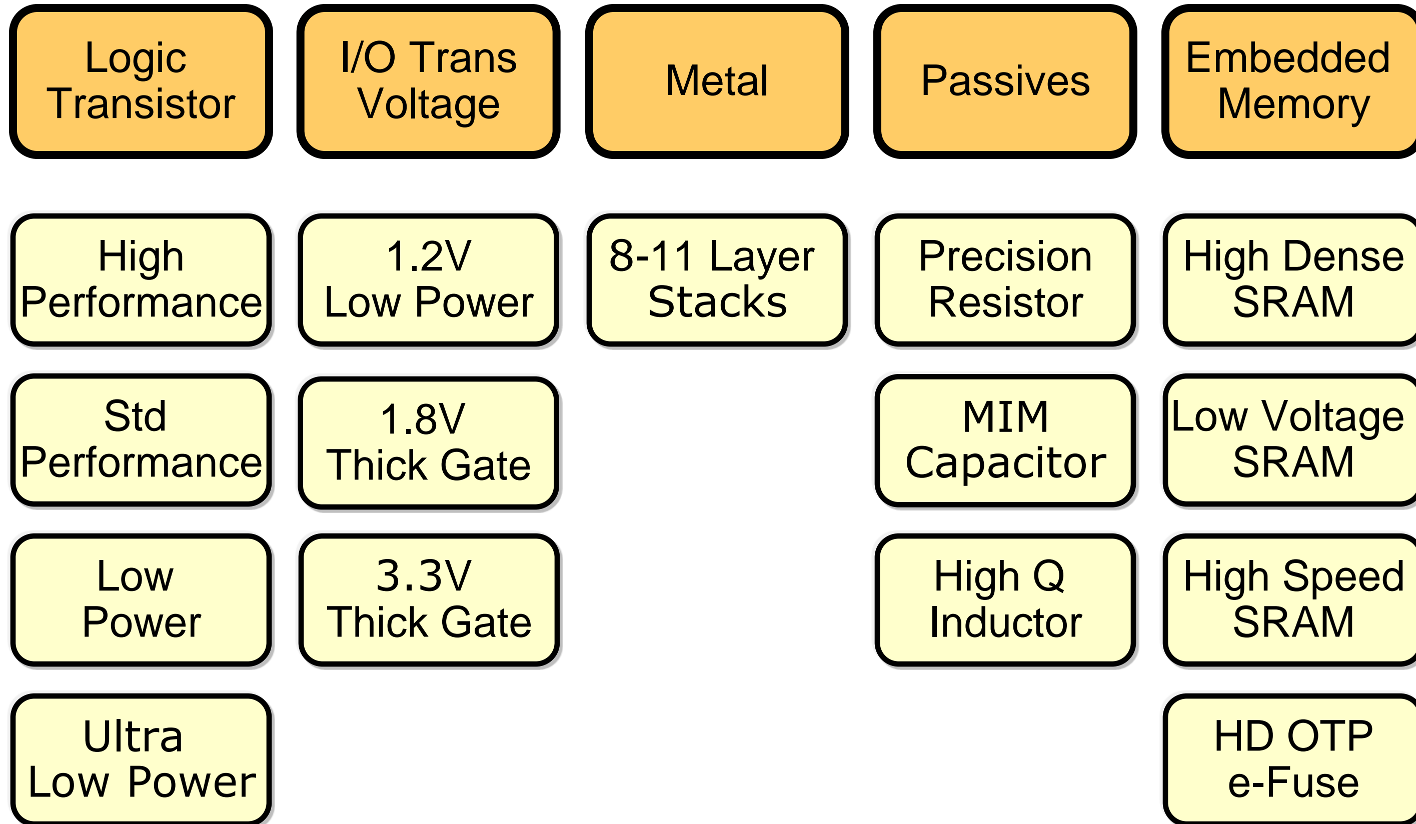
CPU vs. SoC Technology Comparison

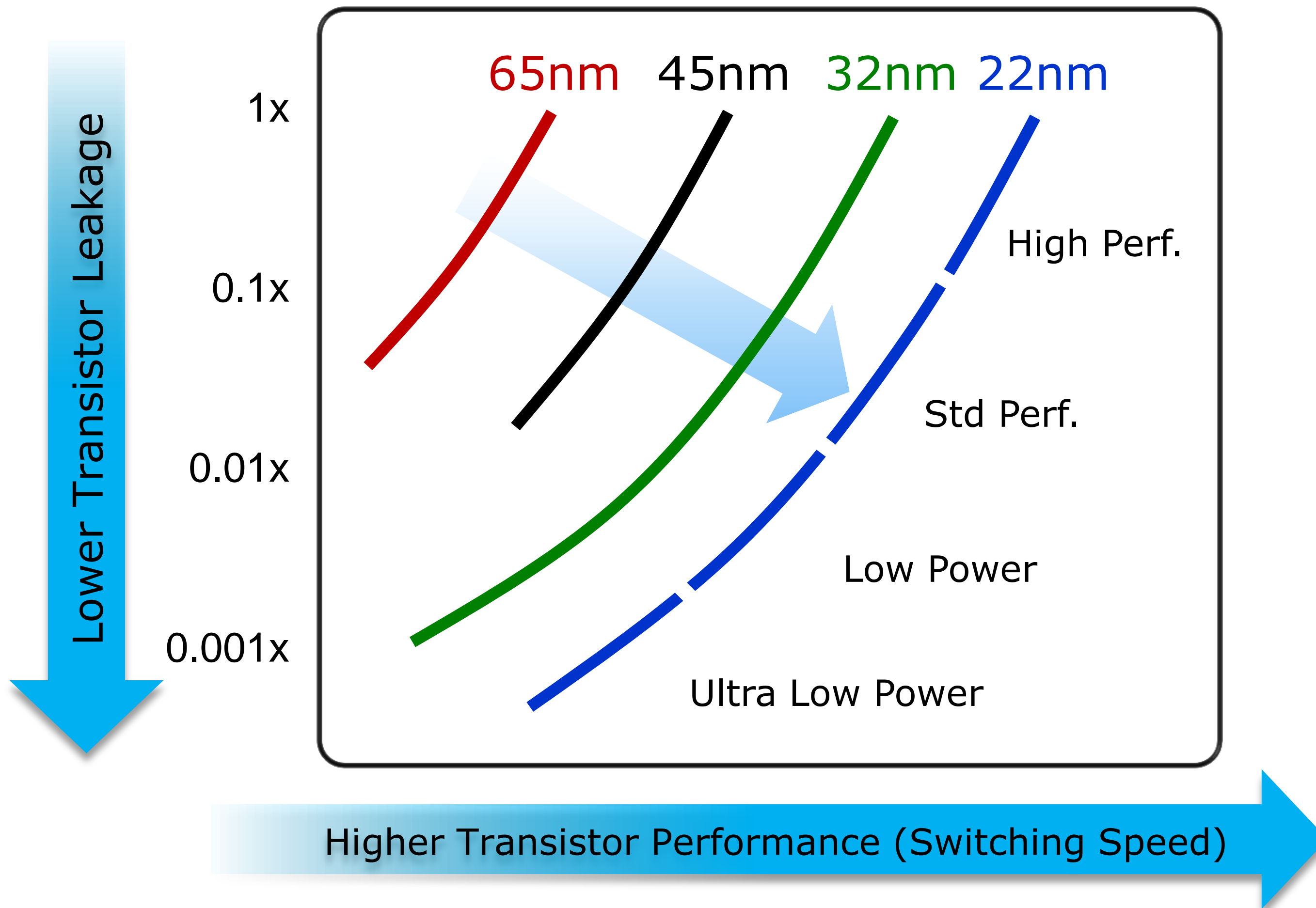
	CPU (P1270)	SoC (P1271)
Similarities		
Tri-Gate Structure	Same	Same
Tight Transistor Pitch	Same	Same
Dense SRAM Cell	Same	Same
Lower Level Interconnects	Same	Same
Fab Process Equipment	Same	Same
Differences		
Logic Transistors	High Speed	Low Leakage
I/O Transistors	Std Voltage	Std and High Volt
Upper Level Interconnects	High Speed	Dense
Precision Passives	None	R, C and L

22 nm SoC Technology Features



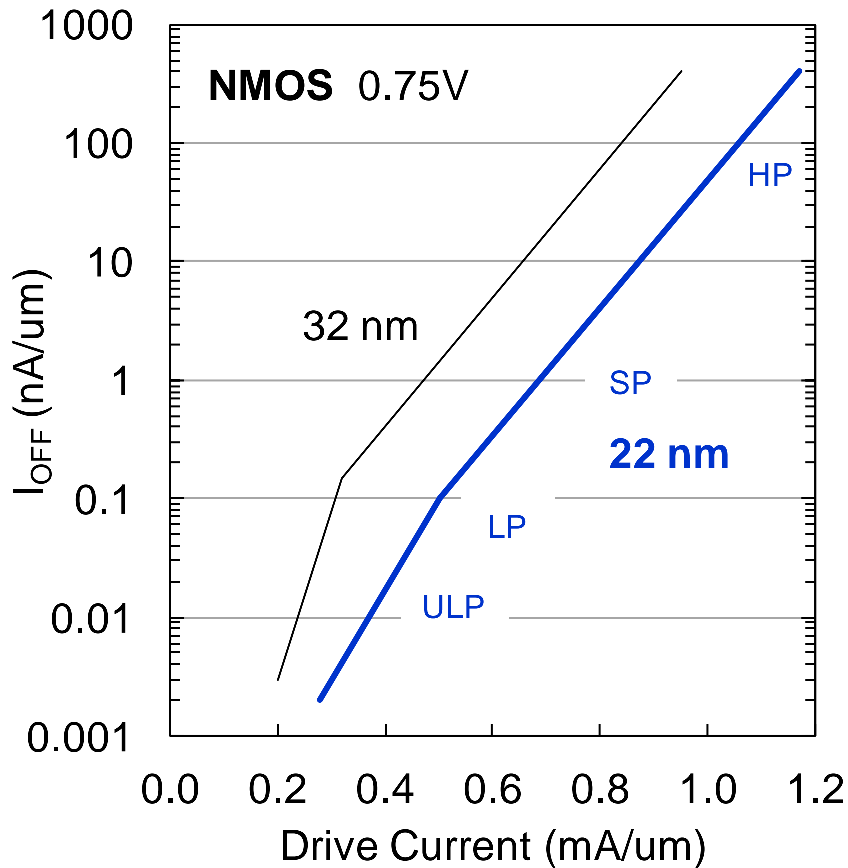
22 nm SoC technology offers a rich menu of feature options

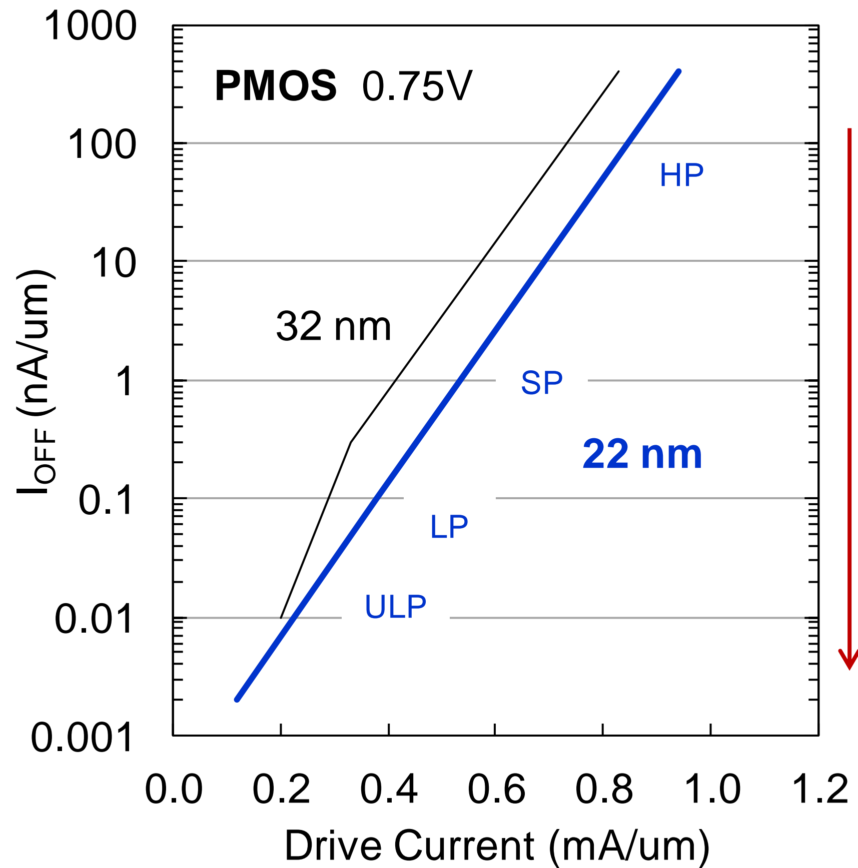
Transistor Performance vs. Leakage



22 nm SoC technology offers a wide range of transistors

Transistor Performance vs. Leakage





22 nm SoC technology offers a wide range of transistors

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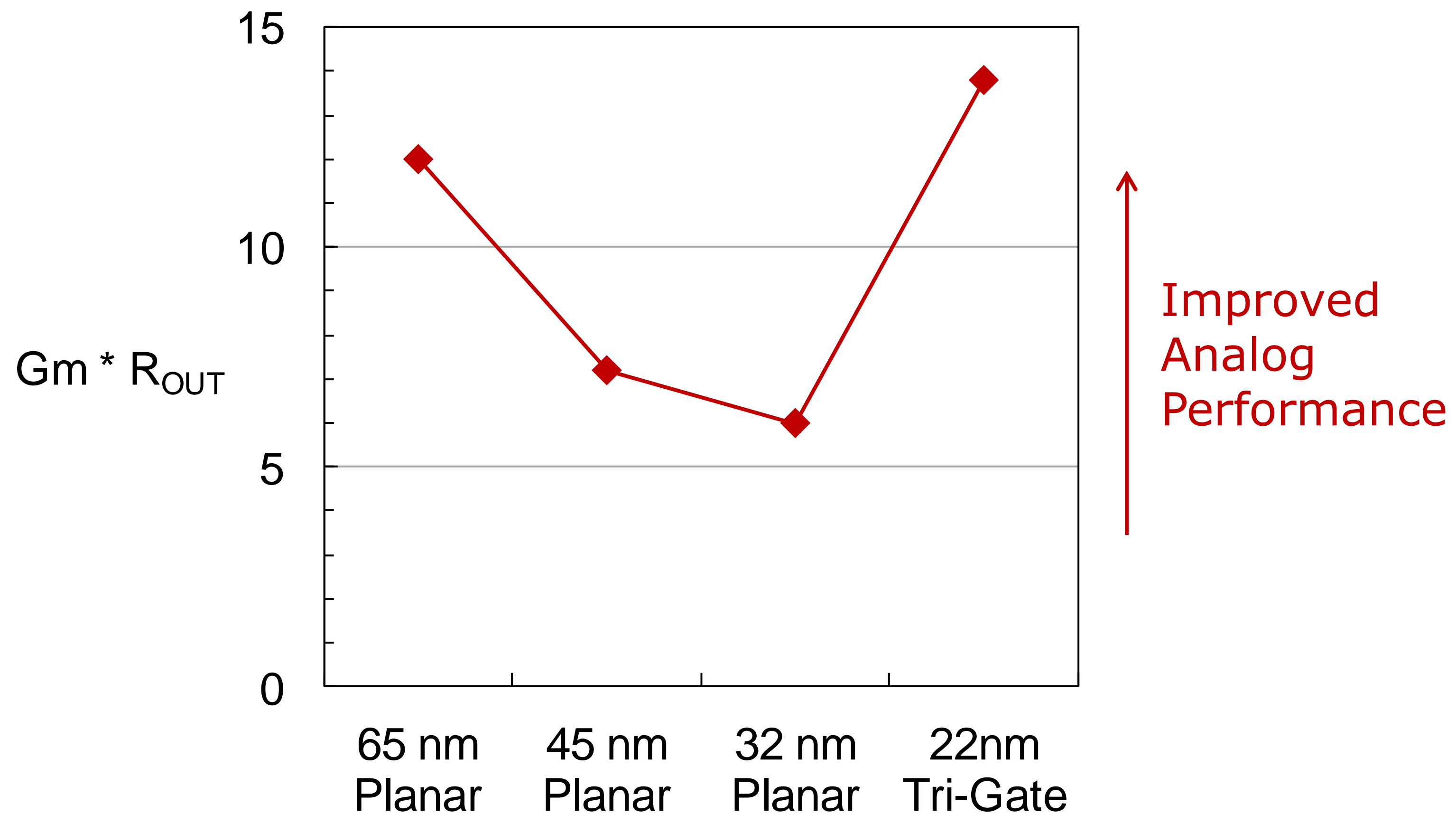
Analog Device Characteristics



22 nm Tri-Gate transistors provide improved Gm * R_{OUT} for improved analog circuit performance

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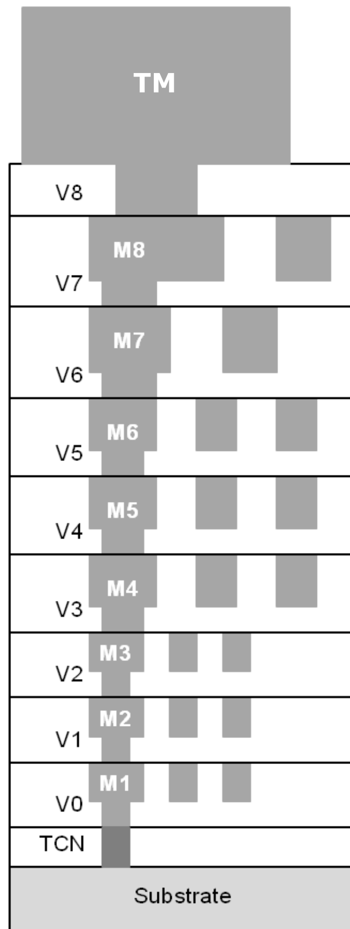
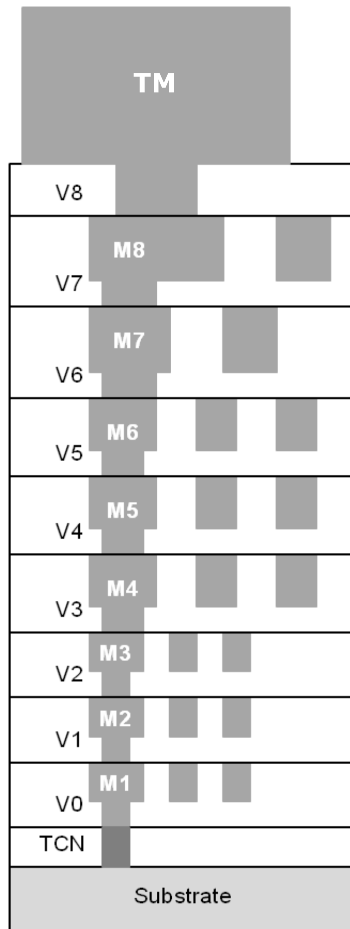
22 nm SoC Interconnect Options



Layer	A	B	C	
TM	14	14	14	um
M10	-	-	360	nm
M9	-	360	360	nm
M8	360	240	160	nm
M7	240	160	108	nm
M6	160	108	80	nm
M5	108	80	80	nm
M4	80	80	80	nm
M3	80	80	80	nm
M2	80	80	80	nm
M1	90	90	90	nm

Range of SoC interconnect options for low cost or high density

22 nm SoC Interconnect Options



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M7	240	160	108	nm
M6	160	108	80	nm
M5	108	80	80	nm
M4	80	80	80	nm
M3	80	80	80	nm
M2	80	80	80	nm
M1	90	90	90	nm

80 nm pitch is done with single patterning, thus an optimal pitch to use for this generation

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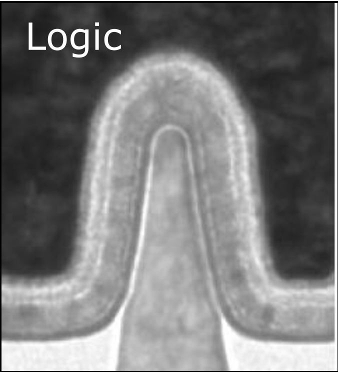
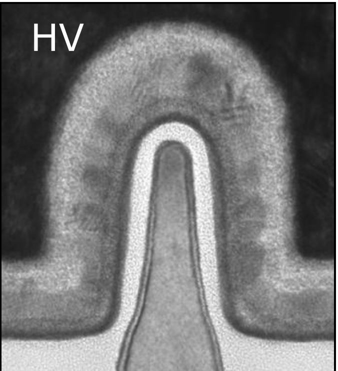
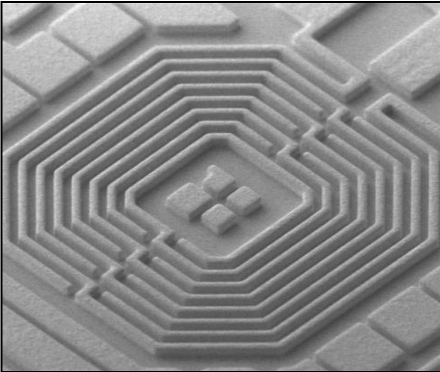
22 nm SoC Device Features

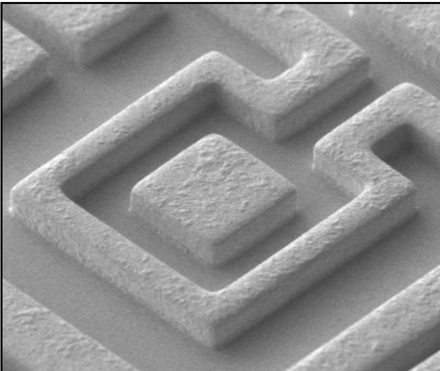
High Voltage I/O Transistors



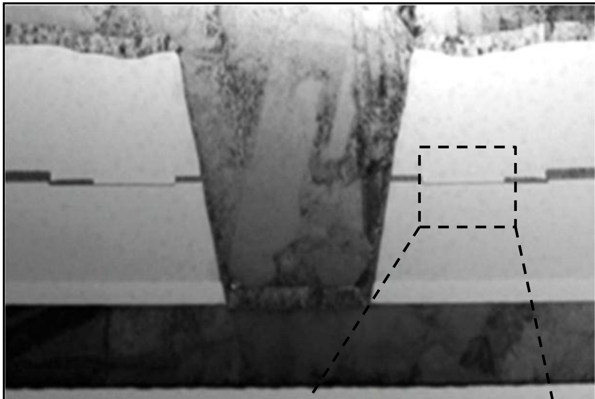


Inductors

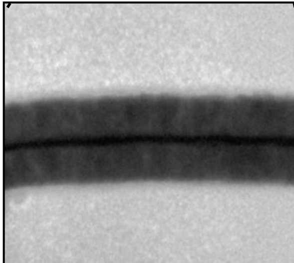




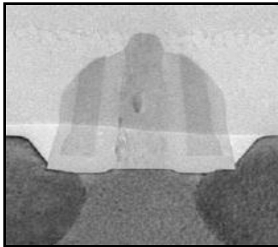
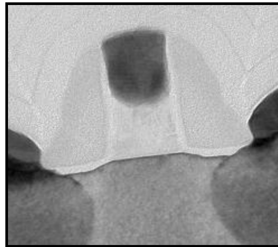
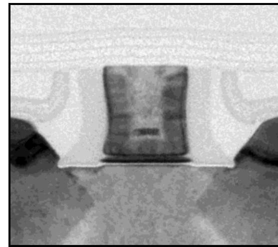
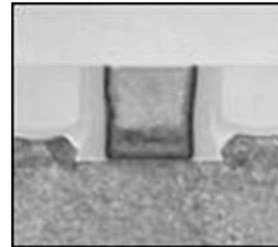
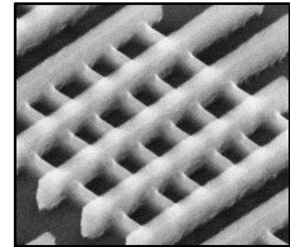
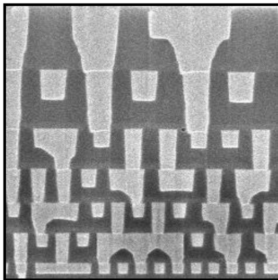
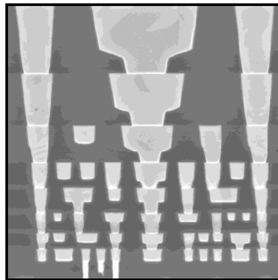
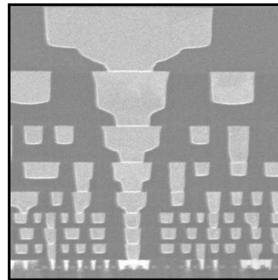
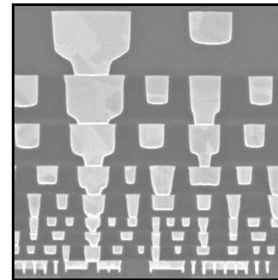
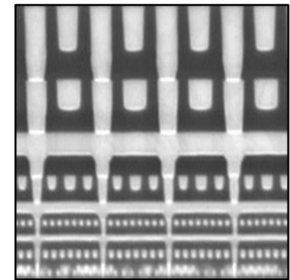
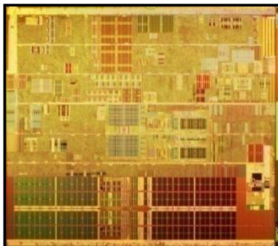
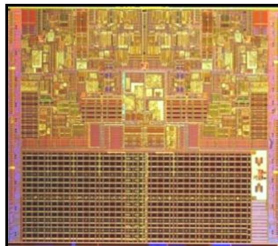
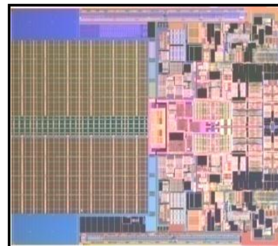
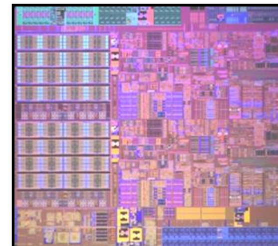
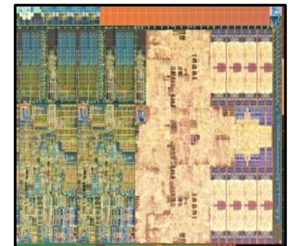
MIM Capacitor



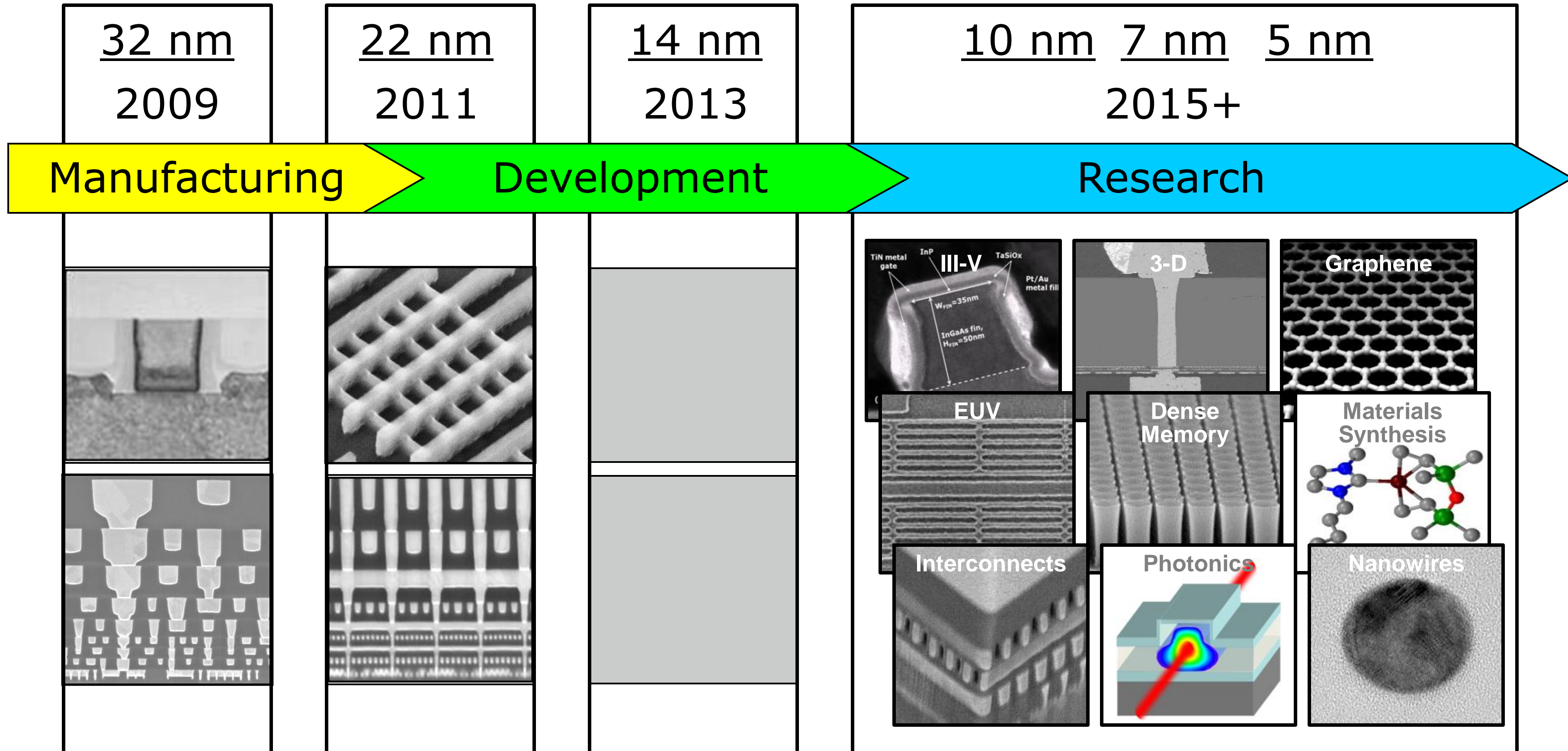
Metal
Insulator
Metal



2 Year Technology Cycles

90 nm	65 nm	45 nm	32 nm	22 nm
2003	2005	2007	2009	2011
				
				
				

Innovation Enabled Technology Pipeline



Future options subject to change

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Advantage of an Integrated Device Manufacturer

Research

Equipment Vendors
Industry Consortia
Universities
Government Labs

- **Identify innovative technologies**

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Advantage of an Integrated Device Manufacturer

Research

Components Research

Equipment Vendors
Industry Consortia
Universities
Government Labs

- **Identify innovative technologies**

Development

Product Design

Logic Technology Development

Design Tools
Photo Masks
Packaging

- **Co-optimize process+product**
- **Design for manufacturing**

Advantage of an Integrated Device Manufacturer

Research	Development	Manufacturing
Components Research	**Product Design** **Logic Technology Development**	**Wafer Manufacturing Fabs**
Equipment Vendors Industry Consortia Universities Government Labs	Design Tools Photo Masks Packaging	Oregon Arizona New Mexico Israel Ireland China
• **Identify innovative technologies**	• **Co-optimize process+product** • **Design for manufacturing**	• **Early product ramp** • **Rapid yield learning**

Summary

- Transistor scaling continues to provide improvements in performance, power and cost, but now with greater focus on power reduction
- Scaling no longer follows a “classical” path and requires continued innovations in materials and structures
- A highly integrated approach is needed to successfully bring innovative technologies from the research phase to high volume manufacturing
- Low power System-on-Chip technologies are increasingly important to support the wide range of features needed on mobile computing devices

Additional Sources of Information on This Topic:

More web based info:

www.intel.com/technology/architecture-silicon

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