Determine Buck Converter Efficiency in PFM Mode

By Jingdong Chen, Staff Application Engineer, National Semiconductor, Santa Clara, Calif.

By analyzing the light-load efficiency of a synchronous buck operating under pulse-frequency modulation control, designers can predict efficiency over the converter's full load range and maximize battery life in portable applications.

Because of the widespread use of pulse-width modulation (PWM), the efficiency of a synchronous buck converter operating in this mode is well understood. However, relatively few designers understand how to predict the efficiency of a buck converter when it operates under pulse-frequency modulation (PFM), a mode that is widely used in portable applications to improve efficiency at light loads. Therefore, an efficiency analysis of PFM mode operation is quite useful, especially when using buck regulators that allow automatic switching between PFM and PWM modes.

To calculate the efficiency of a regulator operating in PFM mode, it is first necessary to identify and characterize the mechanisms that generate losses for this mode. This information may then be combined with a standard analysis of buck converter efficiency in PWM mode to predict system efficiency over the full operating range of the converter. The validity of this analysis can be verified by comparing predicted system efficiency with the measured efficiency for a synchronous buck converter capable of operating in both PWM and PFM modes.

Efficiency Analysis of a Buck Converter

In portable applications, efficiency, especially at light loads, has a significant impact on battery life. Normal PWM-mode operation can optimize efficiency at mid to full load, but this is usually at the expense of light-load efficiency. This could reduce overall efficiency in a system that frequently operates at light load. To maintain high efficiency across the entire load range, it is necessary to operate in PFM mode for light loads. System-level efficiency is further enhanced when the converter automatically selects between the two modes to give the best efficiency for any given load.

A typical synchronous buck converter is shown in **Fig. 1**. For PWM operation, losses of a synchronous buck converter can be grouped into two categories, dc losses and ac losses. The dc losses are determined mainly by on-resistance ($R_{DS_{ON}}$) in the low-side and high-side MOSFETs, and by the series dc resistance (DCR) of the inductor. The ac losses consist mainly of switching losses, gate-drive losses of both FETs and dead-time losses. The ac losses are proportional to the MOSFET switching frequency.

There are different approaches to improve the operating efficiency for different load ranges. Normally, dc losses dominate at heavy load, so lowering $R_{DS_{ON}}$ and DCR would effectively improve efficiency at heavy loads. However, at light loads, conduction losses become insignificant as the ac losses dominate, so decreasing the switching frequency effectively improves efficiency.

Another design consideration when synchronous buck converters operate at light loads is negative inductor current during synchronous operation. When the load becomes smaller and smaller, inductor current can change from positive to partially negative. This negative inductor current discharges the output capacitor and causes additional losses. Therefore, efficiency can be further increased by operating the converter in a nonsynchronous mode, in which a zero-crossing detection circuit would turn off the low-side n-type FET (NFET) when the inductor current goes negative.

PFM is a nonlinear operation in which a series of inductor current pulses are applied to the load and output capacitor to maintain the output voltage within preset boundaries. This mode effectively lowers the frequency of the switching-cycle events, thereby lowering the switching losses in the converter. There are several variations on PFM, such as single-pulse PFM, multipulse PFM and burst-mode PFM. However, all operate according to the basic principle of initiating switching cycles only as needed to maintain the output voltage.

PFM Burst and Pulse Frequencies

Typical inductor current and output-voltage waveforms during PFM mode are shown in **Fig. 2**. During PFM opera-

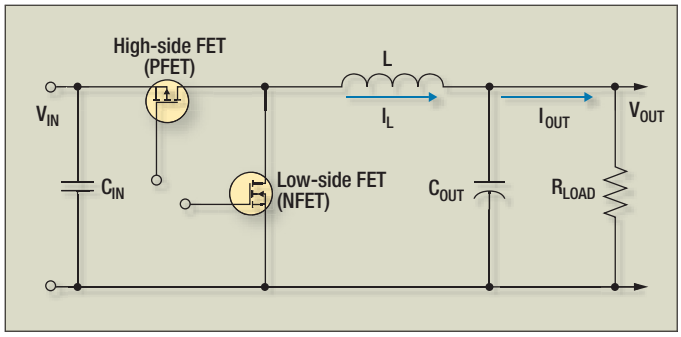

Fig. 1. *To optimize the operating efficiency of the synchronous-buck-converter topology in portable applications, it is necessary to use different switching-modulation modes for nominal and light loads.*

tion, a nonlinear bang-bang control is applied. In this control scheme, four boundary conditions regulate the output voltage: peak inductor current, zero-crossing detection of the inductor current, V_{OUT} upper threshold and V_{OUT} lower threshold.

When the p-type FET (PFET) in the **Fig. 1** circuit turns on, inductor current will increase for time interval dt1 until it reaches the current limit. It is important to note that this current limit is set specifically for PFM mode, and is different from the overcurrent-protection threshold of the regulator.

$$dt1 = \frac{I_{PEAK_{PFM}} \times L}{V_{IN} - V_{OUT}}, \quad \text{Eq. 1}$$

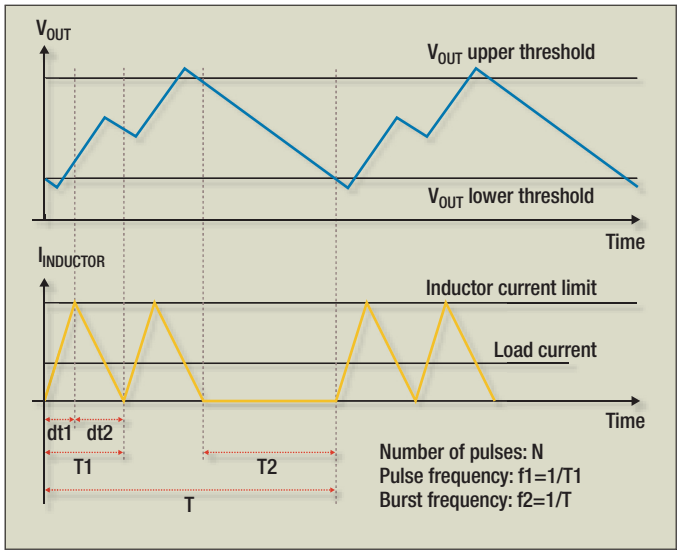

Fig. 2. *PFM-mode waveforms are characterized by two different frequency components: the pulse frequency, which defines the switching frequency of the FETs, and the burst frequency, which indicates how often the FET switching action goes active after an idle state.*

where $I_{PFM_{PEAK}}$ is the peak inductor current during PFM mode, V_{IN} is the input voltage, V_{OUT} is the output voltage and L is the inductance of the inductor. When the PFET turns off, the NFET turns on and inductor current decreases for time

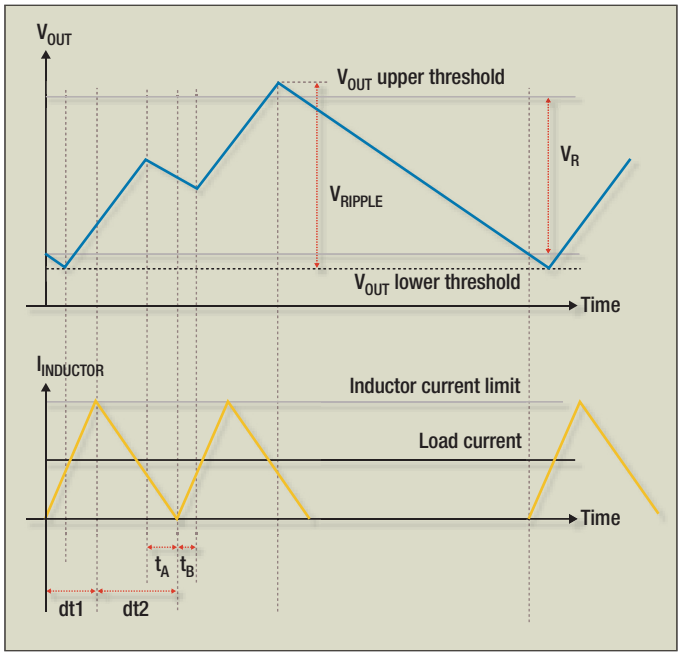

Fig. 3. *The actual ripple on V_{OUT} in PFM mode is determined by voltage overshoot and undershoot outside established upper and lower control thresholds for V_{OUT}.*

interval dt2 until it reaches zero. This action is described by the following equation:

$$dt2 = \frac{I_{PEAK_{PFM}} \times L}{V_{OUT}}. \quad \text{Eq. 2}$$

Therefore, the pulse frequency (f1) is determined as:

$$f1 = \frac{1}{dt1 + dt2} = \frac{1}{T1} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{I_{PEAK_{PFM}} \times L \times V_{IN}}. \quad \text{Eq. 3}$$

The charge provided by the inductor pulses and the charge supplied by the output capacitor (C_{OUT}) to the load should be equal within a single burst period to maintain a stable dc output voltage across C_{OUT} in the **Fig. 1** circuit. Therefore, the burst frequency (f2) is determined by:

$$f2 = \frac{1}{T} = \frac{1}{N \times T1 + T2} = \frac{2 \times I_{OUT} \times \left(\frac{I_{PEAK_{PFM}}}{2} - I_{OUT} \right)}{V_R \times C_{OUT} \times I_{PEAK_{PFM}}}, \quad \text{Eq. 4}$$

where C_{OUT} is the capacitance of the output capacitor, T2 is the dead time, I_{OUT} is the output current drawn by the load, and V_R is the ideal ripple voltage of the output as defined by the upper and lower control thresholds.

PFM Efficiency

Inductor conduction loss ($P_{CONDUCTION_{INDUCTOR}}$) is calculated as follows:

$$P_{L_{CONDUCTION}} = R_L \times \frac{2}{3} \times I_{OUT} \times I_{PEAK_{PFM}}. \quad \text{Eq. 5}$$

The inductor ac losses ($P_{AC_{INDUCTOR}}$) can be computed by the product of the inductor's ac-equivalent resistance ($R_{AC_{INDUCTOR}}$) and the root-mean-square (rms) value of the inductor current:

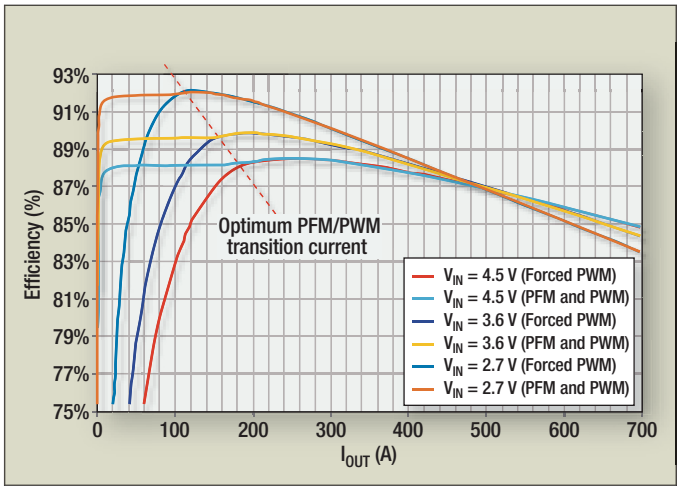

Fig. 4. *The optimum transition point between PWM and PFM modes in the Fig. 1 circuit is a function of input voltage and load current.*

$$P_{L_{AC}} = \frac{1}{6} \times R_{L_{AC}} \times I_{OUT} \times I_{PEAK_{PFM}}. \quad \text{Eq. 6}$$

High-side PFET conduction losses ($P_{CONDUCTION_{PFET}}$) can be estimated as:

$$P_{PFET_{CONDUCTION}} = R_{DS_P} \times \frac{2}{3} \times I_{OUT} \times I_{PEAK_{PFM}} \times \frac{V_{OUT}}{V_{IN}}. \quad \text{Eq. 7}$$

Because of the zero-crossing detection capability, when the high-side PFET in the **Fig. 1** circuit turns on, inductor current is zero, which eliminates the turn-on loss. Therefore, only the turn-off loss for the PFET ($P_{TURN\ OFF_{PFET}}$) is considered:

$$P_{PFET_{TURN\ OFF}} = V_{IN} \times I_{OUT} \times \left[\frac{V_{OUT} \times (V_{IN} - V_{OUT})}{I_{PEAK_{PFM}} \times L \times V_{IN}} \right] \times T_{OFF}, \quad \text{Eq. 8}$$

where $T_{TURN\ OFF_{PFET}}$ is the turn-off switching time for the PFET. Gate-drive loss for the high-side PFET ($P_{GATE\ DRIVE_{PFET}}$) is determined by gate-to-source capacitance ($C_{GS_{PFET}}$), input and output voltage, load current and the PFM preset current limit as follows:

$$P_{GATE\ DRIVE_P} = C_{GS_P} \times V^2_{IN} \times \frac{2 \times I_{OUT} \times V_{OUT} \times (V_{IN} - V_{OUT})}{I^2_{PEAK_{PFM}} \times L \times V_{IN}}. \quad \text{Eq. 9}$$

Conduction loss of the low-side NFET in the **Fig. 1** circuit ($P_{CONDUCTION_{NFET}}$) is calculated by the on-resistance of the NFET ($R_{DS_{NFET}}$) and the rms current through the NFET.

$$P_{NET_{CONDUCTION}} = R_{DS_N} \times \frac{2}{3} \times I_{OUT} \times I_{PEAK_{PFM}} \times \frac{(V_{IN} - V_{OUT})}{V_{IN}}. \quad \text{Eq. 10}$$

The gate-drive loss of the low-side NFET ($P_{GATE\ DRIVE_{NFET}}$) is obtained by:

$$P_{GATE\ DRIVE_N} = C_{GS_N} \times V^2_{IN} \times \frac{2 \times I_{OUT} \times V_{OUT} \times (V_{IN} - V_{OUT})}{I^2_{PEAK_{PFM}} \times L \times V_{IN}}. \quad \text{Eq. 11}$$

Because of the dead time (T2 in **Fig. 2**), the shoot-through losses in the NFET and PFET are avoided, as well as the switching loss of the low-side NFET. Moreover, zero-crossing

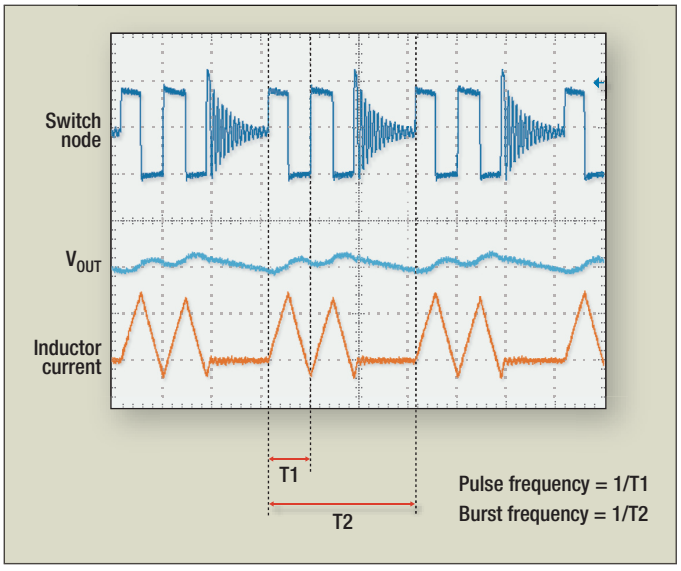

Fig. 5. *PFM-mode waveforms for a synchronous buck regulator implemented with the LM3677TL controller clearly show the regions of no switching activity, greatly reducing switching losses. Using the topology in Fig. 1, Channel 1 shows the switch node, Channel 2 shows the output voltage, and Channel 3 displays the inductor current.*

detection removes the turn-off switching losses and reduces the freewheeling current losses in the low-side NFET. So, the turn-on diode loss of the NFET ($P_{DIODE\ LOSS_{NFET}}$) is the only loss generated during the dead time of the PFM cycle:

$$P_{NFET_{DIODE}} = V_{DIODE_{DROP}} \times T_{DEAD\ TIME} \times \frac{2 \times I_{OUT} \times V_{OUT} \times (V_{IN} - V_{OUT})}{I^2_{PEAK_{PFM}} \times L \times V_{IN}}, \quad \text{Eq. 12}$$

where $V_{DIODE_{NFET}}$ is the forward-voltage drop of the NFET body diode. The ESR loss related to the output capacitor ($P_{ESR_{CAPACITOR}}$) and quiescent current losses (P_{IQ}) are calculated using Eqs. 13 and 14, respectively:

$$P_{ESR_{CAPACITOR}} = ESR_{CAPACITOR} \times \frac{1}{6} \times I_{OUT} \times I_{PEAK_{PFM}} \quad \text{Eq. 13}$$

$$P_{I_Q} = I_Q \times V_{IN}, \quad \text{Eq. 14}$$

where $ESR_{CAPACITOR}$ is the ESR of the output capcacitor and I_Q is the quiescent current. The reductions in losses at light loads give the PFM-mode operation of the **Fig. 1** circuit much higher efficiency than the forced PWM-mode operation.

Output Ripple

One important parameter in PFM mode is the output ripple. Referring to **Fig. 3**, the time intervals that affect output ripple (t_A and t_B) are defined as follows:

$$t_A = \frac{I_{OUT} \times L}{V_{OUT}} \quad \text{Eq. 15}$$

$$t_B = \frac{I_{OUT} \times L}{V_{IN} - V_{OUT}}. \quad \text{Eq. 16}$$

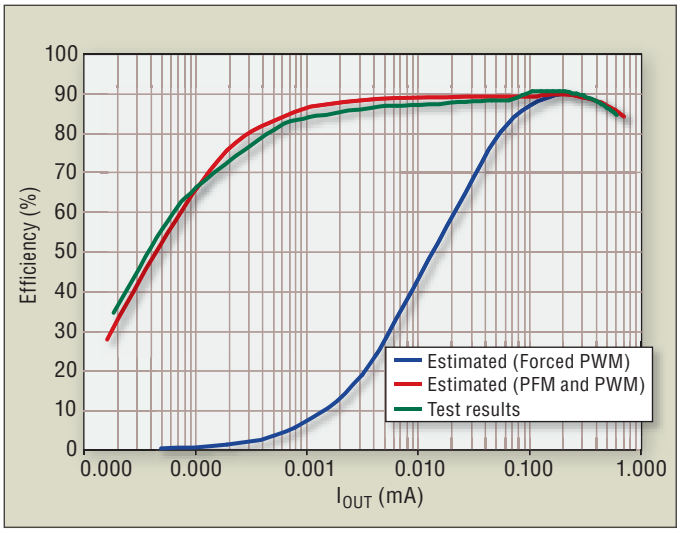

Fig. 6. *The predicted and measured efficiency curves for combined PWM and PFM operation reveal the benefits of being able to switch PFM mode for light loads.*

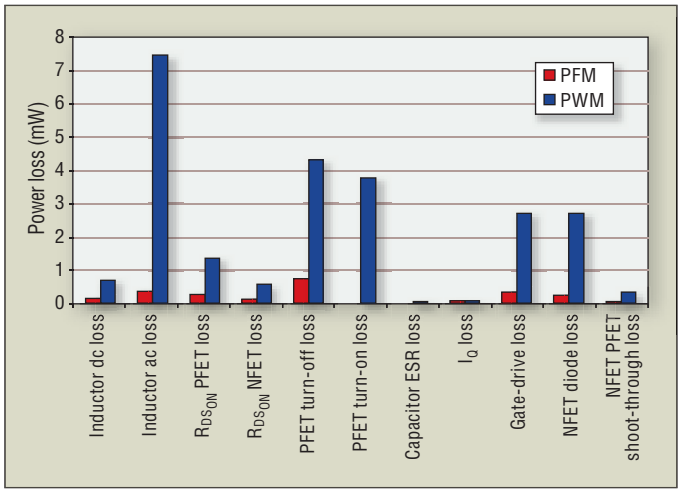

Fig. 7. *This loss comparison between forced-PWM mode, and the automatically switched PFM and PWM modes, show how the individual loss reductions of PFM mode contribute to the system-level gains in efficiency.*

Because of the charging balance of the output capacitor needed to maintain a constant value for V_{OUT}:

$$V_{RIPPLE} \times C_{OUT} = N \times \frac{I_{PEAK_{PFM}} - I_{OUT}}{2} \times (dt1 + dt2 - t_A - t_B) - (N-1) \times \frac{I_{OUT}}{2} \times (t_A + t_B), \quad \text{Eq. 17}$$

where V_{RIPPLE} is the actual ripple voltage on V_{OUT}. Note that V_{RIPPLE} is greater than V_R. This is true because even when the output voltage reaches the upper threshold for V_{OUT} and the PFET is off, the converter has no further control over V_{OUT}. The output capacitor will continue to charge until the inductor current decays to the value of the load current. Therefore, the actual output peak is always higher than the upper threshold for V_{OUT}.

Additionally, when V_{OUT} reaches the lower threshold, the PFET turns on to pull V_{OUT} up. The output voltage continues to decrease until the inductor current builds up to the value of the load current. Therefore, the actual minimum value for V_{OUT} is less than the lower threshold for V_{OUT}. Again, the cumulative result of these two control limitations is that V_{RIPPLE} is greater than V_R, affecting the number of switching cycles in a burst (N) as follows:

$$N > \frac{V_R \times C_{OUT} - \frac{I_{OUT}}{2} \times t_A}{\frac{I_{PEAK_{PFM}} - I_{OUT}}{2} \times (dt1 + dt2) - \frac{I_{PEAK_{PFM}}}{2} \times (t_A + t_B)}. \quad \text{Eq. 18}$$

Rounding up the resulting N from Eq. 18 to the next-highest integer, output ripple is then given by:

$$V_{RIPPLE} = \frac{1}{C_{OUT}} \times \left[N \times \frac{I_{PEAK_{PFM}} - I_{OUT}}{2} \times (dt1 + dt2) - N \times \frac{I_{PEAK_{PFM}}}{2} \times (t_A + t_B) + \frac{I_{OUT}}{2} \times (t_A + t_B) \right]. \quad \text{Eq. 19}$$

Test conditions V_{IN} = 3.6 V, V_{OUT} = 1.8 V, I_{OUT} = 20 mA	Pulse frequency (MHz)	Burst frequency (MHz)
Estimated	545.5	4.08
Measurement	550.0	4.12

Table. *Comparison of estimated and measured PFM-mode operating frequency in a buck regulator using the LM3677TL.*

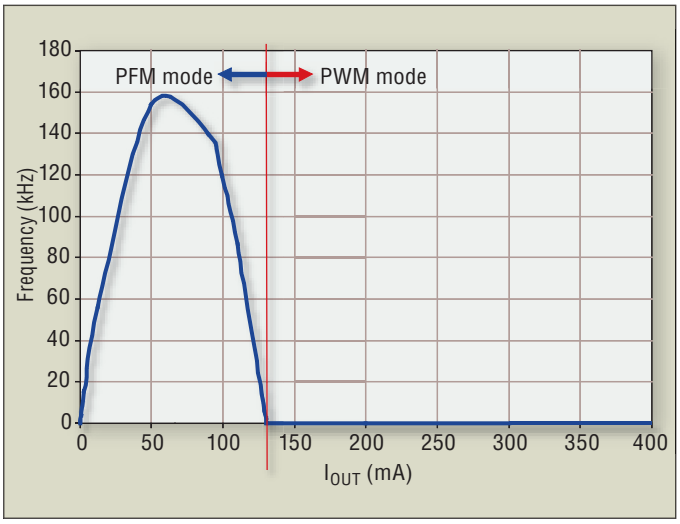

Fig. 8. *The burst frequency of PFM operation peaks at approximately 50% of the maximum load current supported by the PFM operation.*

Transition Between PFM and PWM

To optimize the system-level efficiency of the converter, it is best to change between PFM and PWM operating modes at the peak of the forced PWM efficiency curve. Then the combined PFM and PWM efficiency curve would be the

profile of the higher efficiency between the two modes for each value of load current. Because input voltage has a strong effect on the PWM efficiency curve (**Fig. 4**), the value for the load current giving peak PWM efficiency decreases as input voltage decreases. Therefore, it is desirable to set different transition points for different input voltages. In general, the lower the input voltage, the lower the value of the transitional load current between PFM and PWM operating modes.

Performance Verification

National's LM3677TL can be used to implement a buck regulator that automatically switches between PFM and PWM in the manner described previously. It is a 3-MHz buck regulator with 600-mA load capacity. **Fig. 5** shows typical waveforms of this implementation in PFM-mode operation, implementing the following values for the buck topology shown in **Fig. 1**: V_{IN} = 3.6 V, V_{OUT} = 1.8 V, F = 3 MHz, L = 1 µH, C_{IN} = 4.7 µF and C_{OUT} = 10 µF.

The **table** shows a sample comparison between the estimated and measured frequencies of PFM mode at V_{IN} = 3.6 V, V_{OUT} = 1.8 V and I_{OUT} = 20 mA.

Fig. 6 shows an efficiency comparison between forced-PWM, and PFM and PWM operating modes. Good agreement is observed between measured and estimated results for the latter operating mode. The efficiency improvement using PFM mode is also illustrated clearly in this graph. For example, when the load current is 1 mA, PWM mode can only provide 8% efficiency. However, PFM mode can provide a substantial improvement, with 84% efficiency.

Fig. 7 illustrates the weighting of the various losses contributed by PFM mode and forced-PWM mode for a 10-mA load. Because of the low rms current in PFM mode, ac losses in the inductor are greatly reduced, and the high-side PFET turn-on loss is totally removed. As indicated in **Fig. 7**, PFET turn-on and turn-off losses, gate-drive loss and dead-time loss are also significantly reduced in PFM mode. It is all because of switching events.

Fig. 8 shows the burst-frequency change with the change of load. At no load, burst frequency approaches zero. As the load current increases, the burst frequency starts increasing and peaks at about half the maximum load current that PFM mode can support. Then burst frequency decreases to zero, at which point the device operates in PWM mode. This mechanism indicates that the PFM-mode operation results in an output voltage with very rich harmonics.

The increase in efficiency gained by using PFM mode is substantial and directly translates to longer battery life in portable applications. As demonstrated by the LM3677 design example, the efficiency of a synchronous buck regulator operating in both PFM and PWM modes can be predicted with a high level of accuracy. **PETech**