

# MOS fabrication process

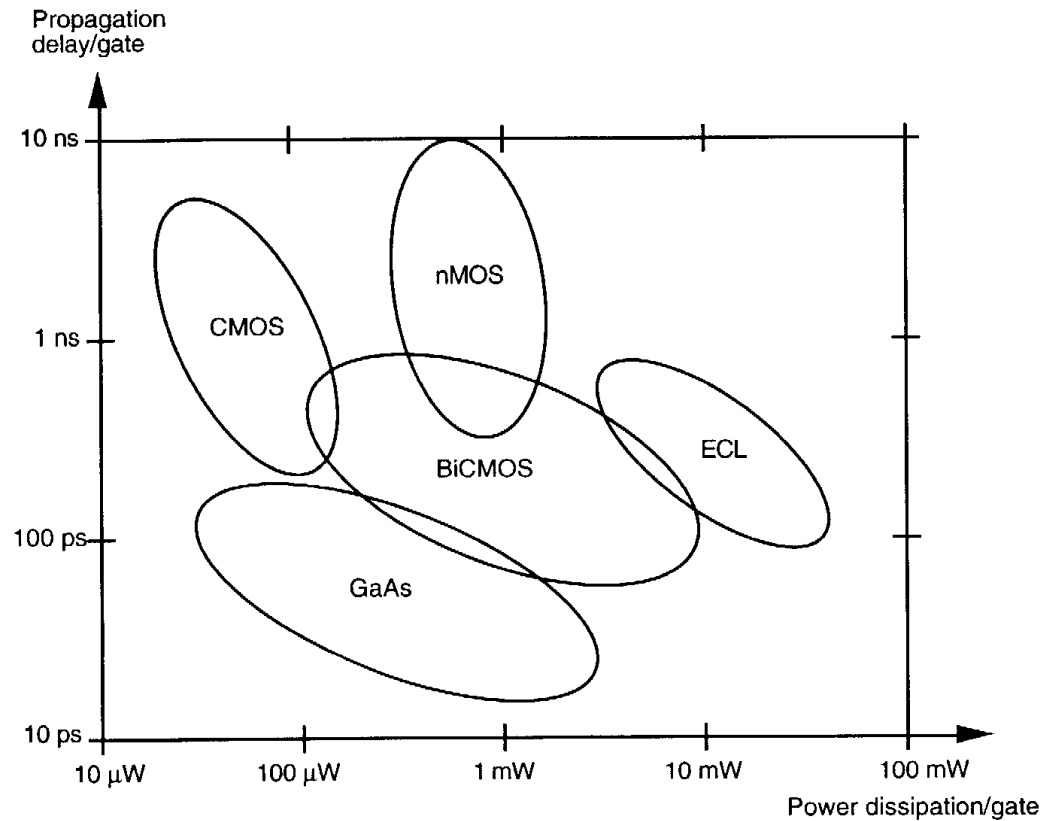
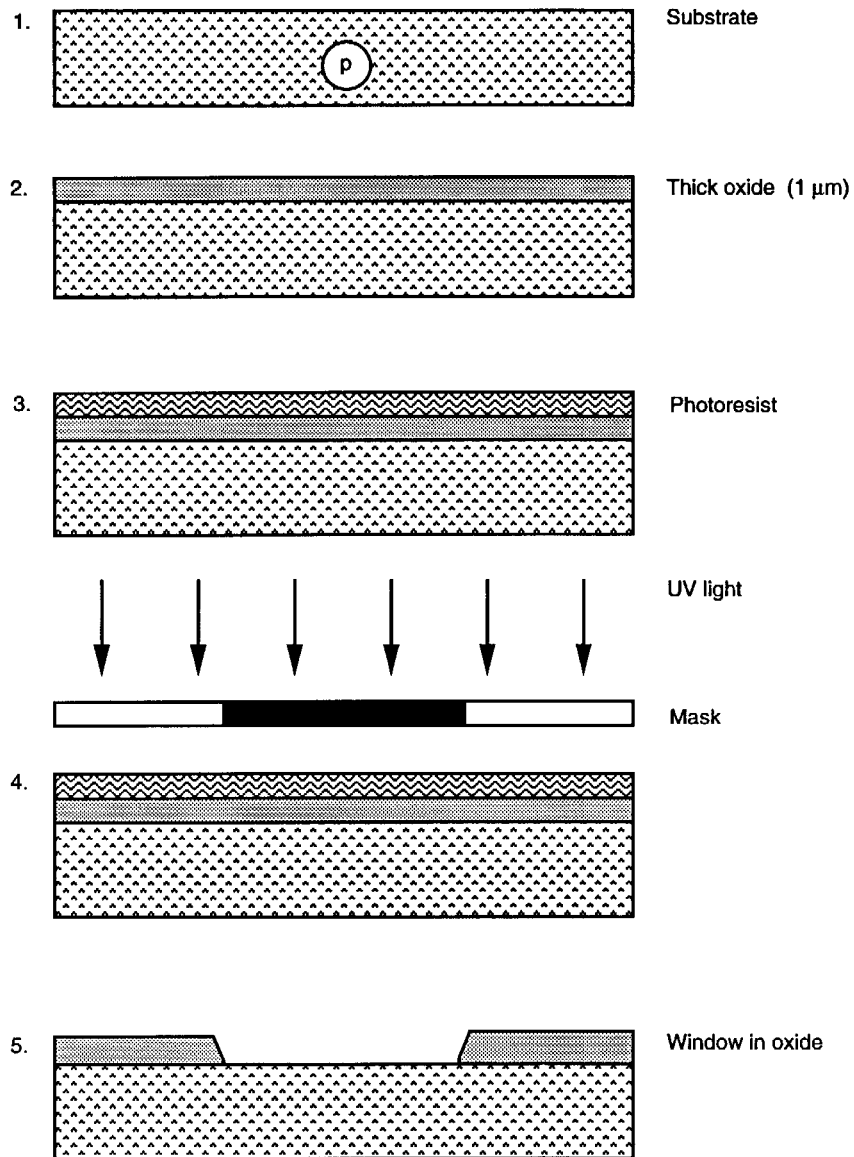


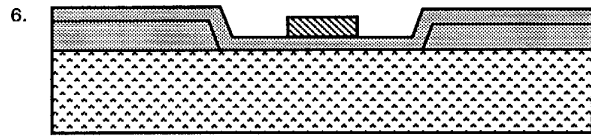
Figure 1-2 Speed/power performance of available technologies

- nMOS
- CMOS for logic
- BiCMOS for I/O and driver circuit

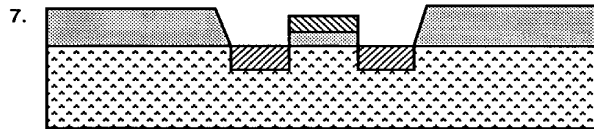
# nMOS fabrication



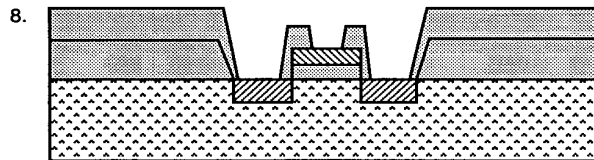
1. Processing is carried out on a thin wafer cut from a single crystal of silicon of high purity into which the required p-impurities are introduced as the crystal is grown. Such wafers are typically 75 to 150 mm in diameter and 0.4 mm thick and are doped with, say, boron to impurity concentrations of  $10^{15}/\text{cm}^3$  to  $10^{16}/\text{cm}^3$ , giving resistivity in the approximate range 25 ohm cm to 2 ohm cm.
2. A layer of silicon dioxide ( $\text{SiO}_2$ ), typically  $1\ \mu\text{m}$  thick, is grown all over the surface of the wafer to protect the surface, act as a barrier to dopants during processing, and provide a generally insulating substrate onto which other layers may be deposited and patterned.
3. The surface is now covered with a photoresist which is deposited onto the wafer and spun to achieve an even distribution of the required thickness.
4. The photoresist layer is then exposed to ultraviolet light through a mask which defines those regions into which diffusion is to take place together with transistor channels. Assume, for example, that those areas exposed to ultraviolet radiation are polymerized (hardened), but that the areas required for diffusion are shielded by the mask and remain unaffected.
5. These areas are subsequently readily etched away together with the underlying silicon dioxide so that the wafer surface is exposed in the window defined by the mask.



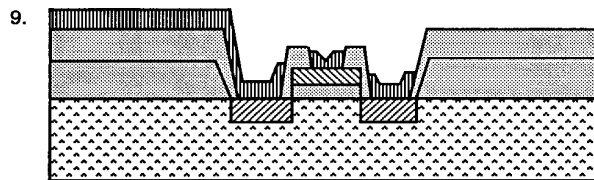
6. Patterned poly. (1–2 μm)  
on thin oxide (800–1000 Å)



7. n<sup>+</sup> diffusion (1 μm deep)



8. Contact holes (cuts)



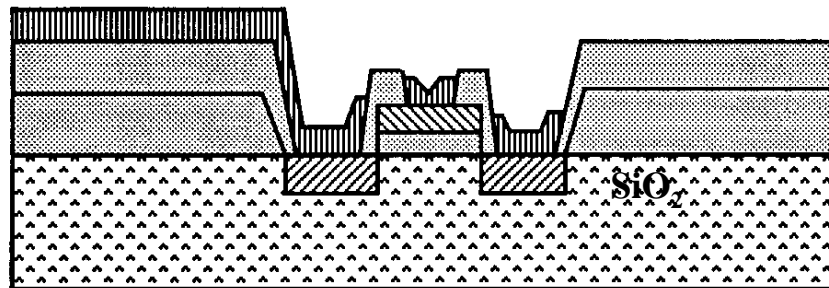
9. Patterned metallization  
(aluminum 1 μm)

6. The remaining photoresist is removed and a thin layer of SiO<sub>2</sub> (0.1 μm typical) is grown over the entire chip surface and then polysilicon is deposited on top of this to form the gate structure. The polysilicon layer consists of heavily doped polysilicon deposited by chemical vapor deposition (CVD). In the fabrication of fine pattern devices, precise control of thickness, impurity concentration, and resistivity is necessary.
7. Further photoresist coating and masking allows the polysilicon to be patterned (as shown in Step 6), and then the thin oxide is removed to expose areas into which n-type impurities are to be diffused to form the source and drain as shown. Diffusion is achieved by heating the wafer to a high temperature and passing a gas containing the desired n-type impurity (for example, phosphorus) over the surface as indicated in Figure 1–8. Note that the polysilicon with underlying thin oxide and the thick oxide act as masks during diffusion — the process is self-aligning.
8. Thick oxide (SiO<sub>2</sub>) is grown over all again and is then masked with photoresist and etched to expose selected areas of the polysilicon gate and the drain and source areas where connections (i.e. contact cuts) are to be made.
9. The whole chip then has metal (aluminum) deposited over its surface to a thickness typically of 1 μm. This metal layer is then masked and etched to form the required interconnection pattern.

# Summary of an nMOS process

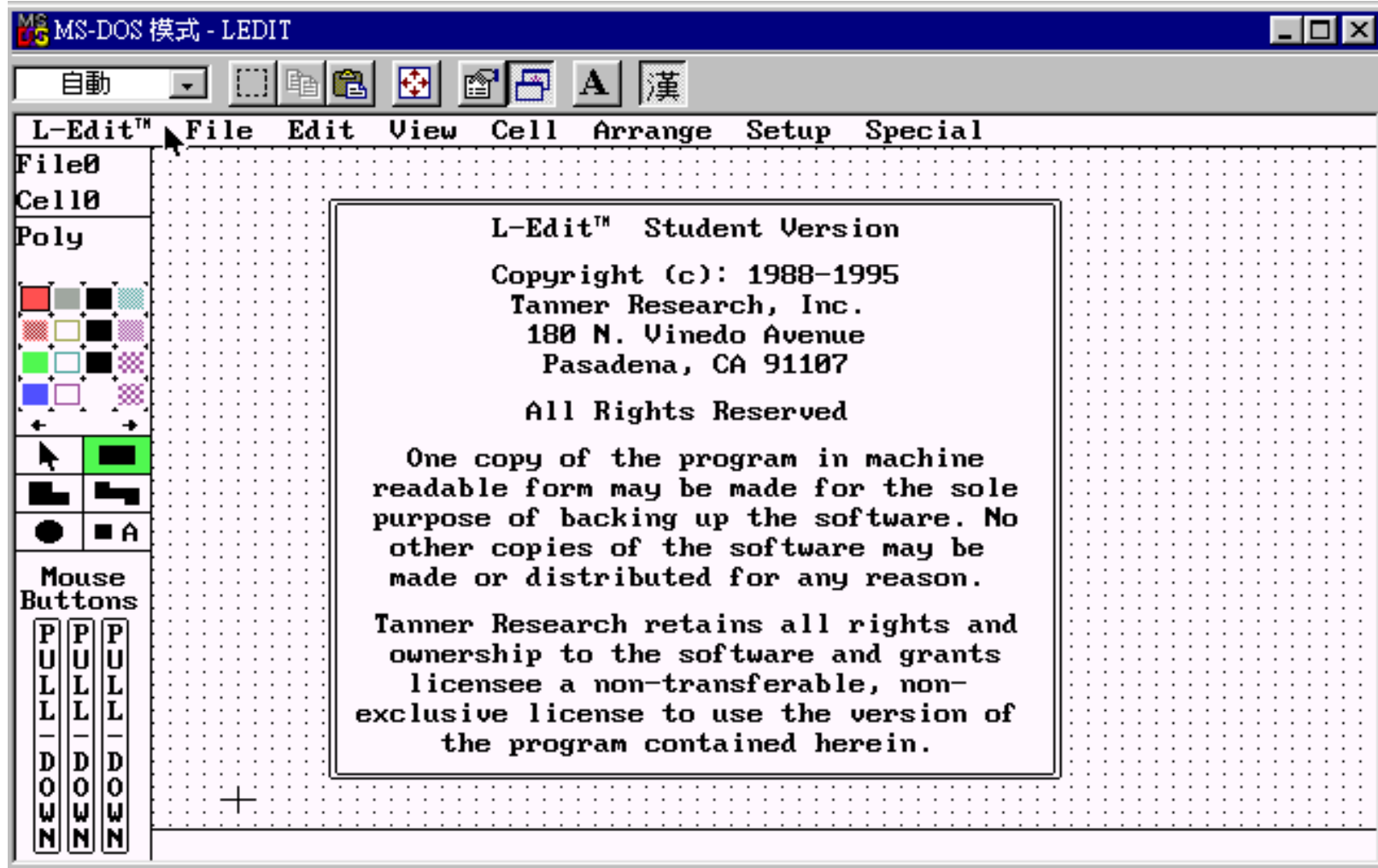
- Processing takes place on a p-doped silicon crystal wafer on which is grown a 'thick' layer of  $\text{SiO}_2$ .
- *Mask 1* — Pattern  $\text{SiO}_2$  to expose the silicon surface in areas where paths in the diffusion layer or source, drain or gate areas of transistors are required. Deposit thin oxide over all. For this reason, this mask is often known as the '*thinox*' mask but some texts refer to it as the *diffusion mask*.
- *Mask 2* — Pattern the ion implantation within the thinox region where depletion mode devices are to be produced — *self-aligning*. ←
- *Mask 3* — Deposit polysilicon over all ( $1.5\ \mu\text{m}$  thick typically), then pattern using Mask 3. Using the same mask, remove thin oxide layer where it is not covered by polysilicon.
- Diffuse  $\text{n}^+$  regions into areas where thin oxide has been removed. Transistor drains and sources are thus self-aligning with respect to the gate structures.
- *Mask 4* — Grow thick oxide over all and then etch for contact cuts.
- *Mask 5* — Deposit metal and pattern with Mask 5.
- *Mask 6* — Would be required for the overglassing process step.

Depletion mode only



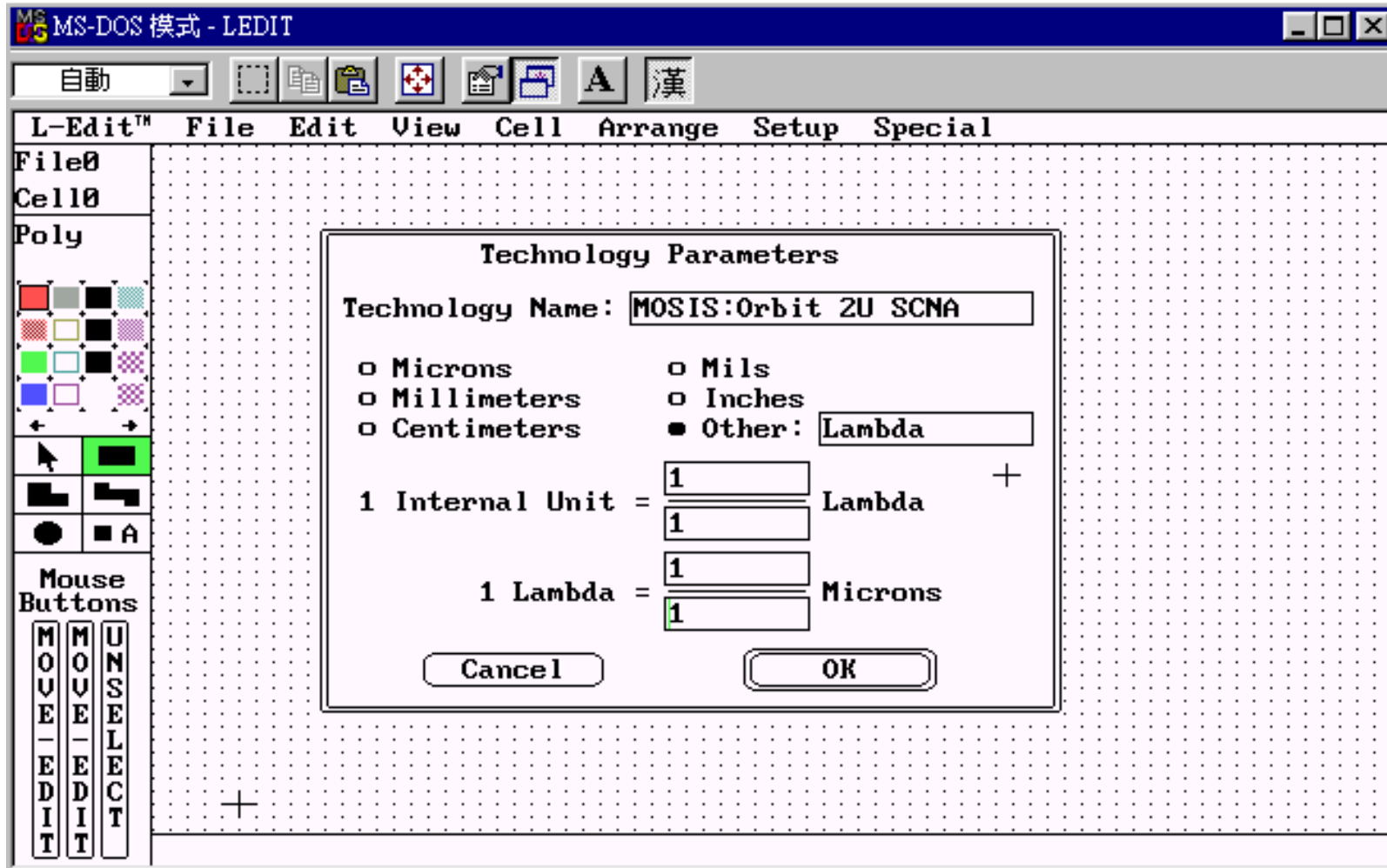
# Mask Layout

## L-Edit layout program



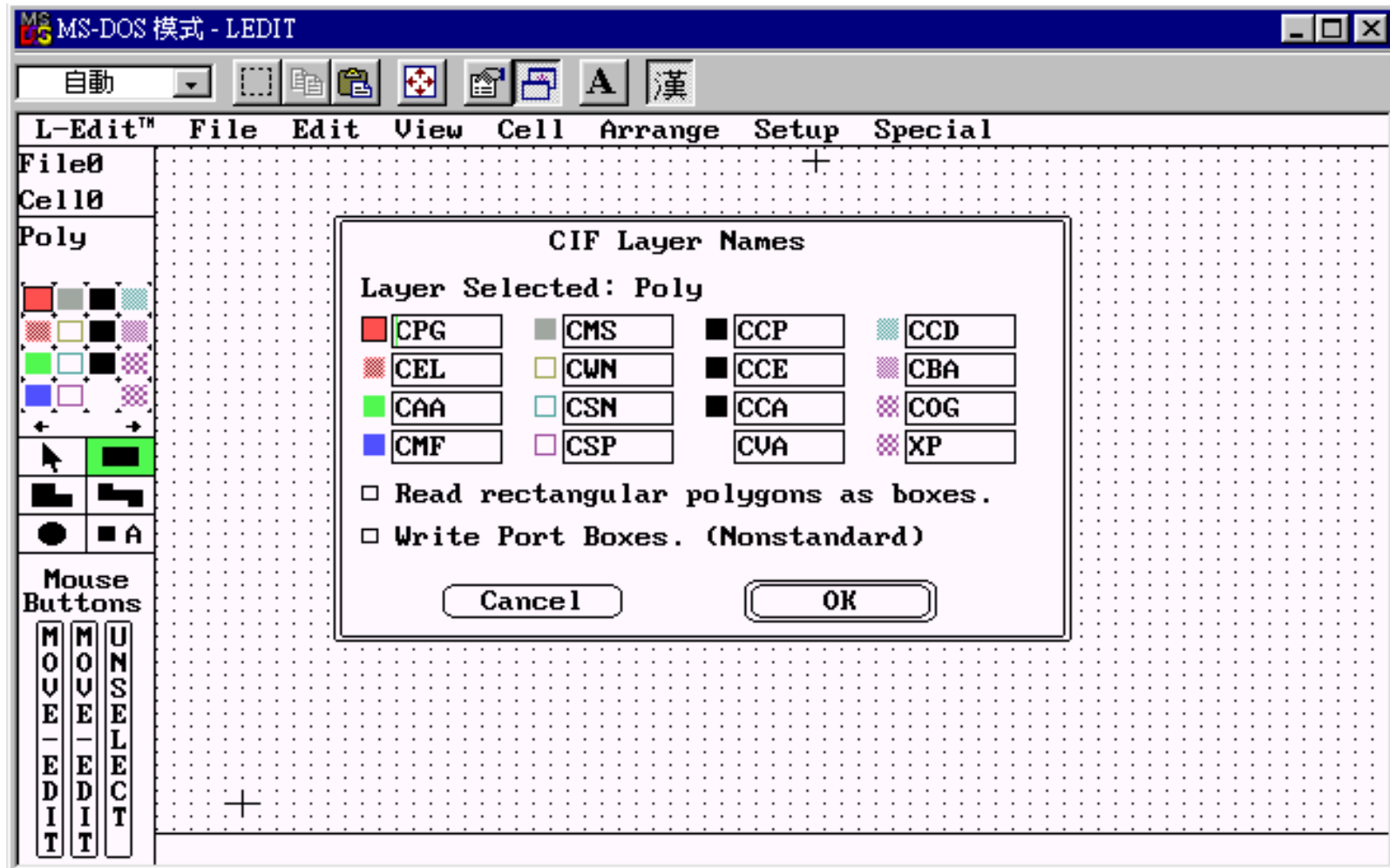
# Technology Setup

- Setup > Technology > MOSIS: Orbit 2U SCNA



















# CIF Layers

- Setup > CIF



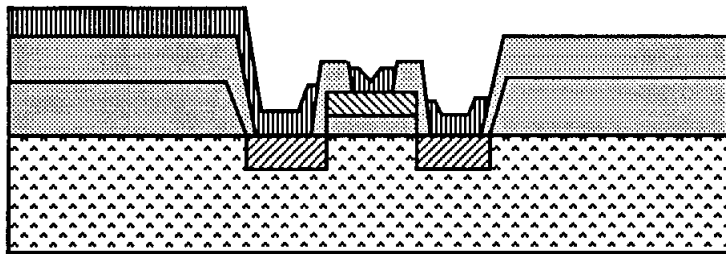
# CIF Layer Names

	<b>CPG</b>	<b>CMOS Poly Gate (CPF)</b>	<b>Poly (Poly1)</b>
	<b>CEL</b>	<b>CMOS Electrode (CPS)</b>	<b>(Poly2)</b>
	<b>CAA</b>	<b>CMOS Active Area</b>	<b>Active (Thinox=n-diff + transistor channel)</b>
	<b>CMF</b>	<b>CMOS Metal First</b>	<b>Metal 1</b>
	<b>CMS</b>	<b>CMOS Metal Second</b>	<b>Metal 2</b>
	<b>CWN</b>	<b>CMOS Well N-diff</b>	<b>N well</b>
	<b>CSN</b>	<b>CMOS Select N</b>	<b>N select</b>
	<b>CSP</b>	<b>CMOS Select P</b>	<b>P select</b>
	<b>CCP</b>	<b>CMOS Contact Poly</b>	<b>Poly contact</b>
	<b>CCE</b>	<b>CMOS Contact Electrode</b>	<b>Poly2 contact</b>
	<b>CCA</b>	<b>CMOS Contact Active</b>	<b>Active contact</b>
	<b>CVA</b>	<b>CMOS Via</b>	<b>Via</b>
	<b>CCD</b>		
	<b>CBA</b>		
	<b>COG</b>	<b>CMOS Overglass</b>	<b>Overglass</b>
	<b>XP</b>		











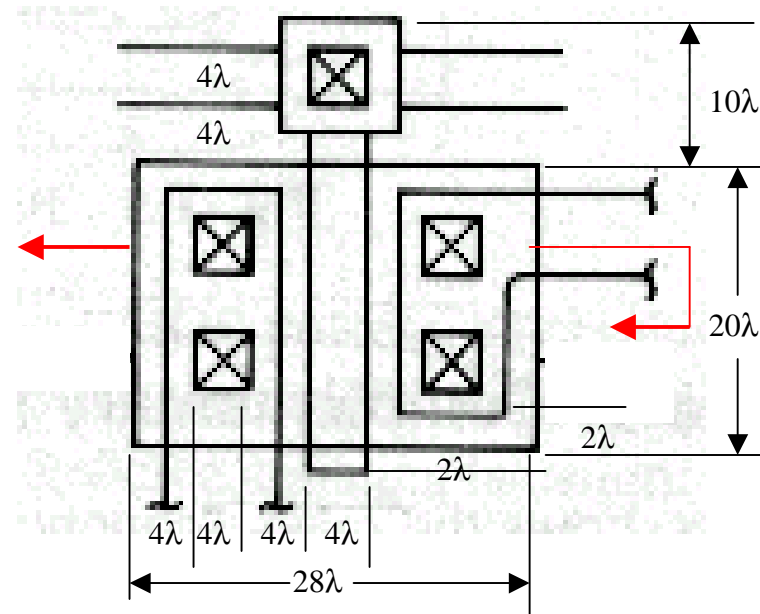
# Enhancement Mode NMOS Mask Layout

(1) Use Layout program (L-Edit) to draw 6 masks of an enhancement mode nMOS process by using L-edit and Orbit 2 $\mu\text{m}$  double metal, double poly, CMOS technology.

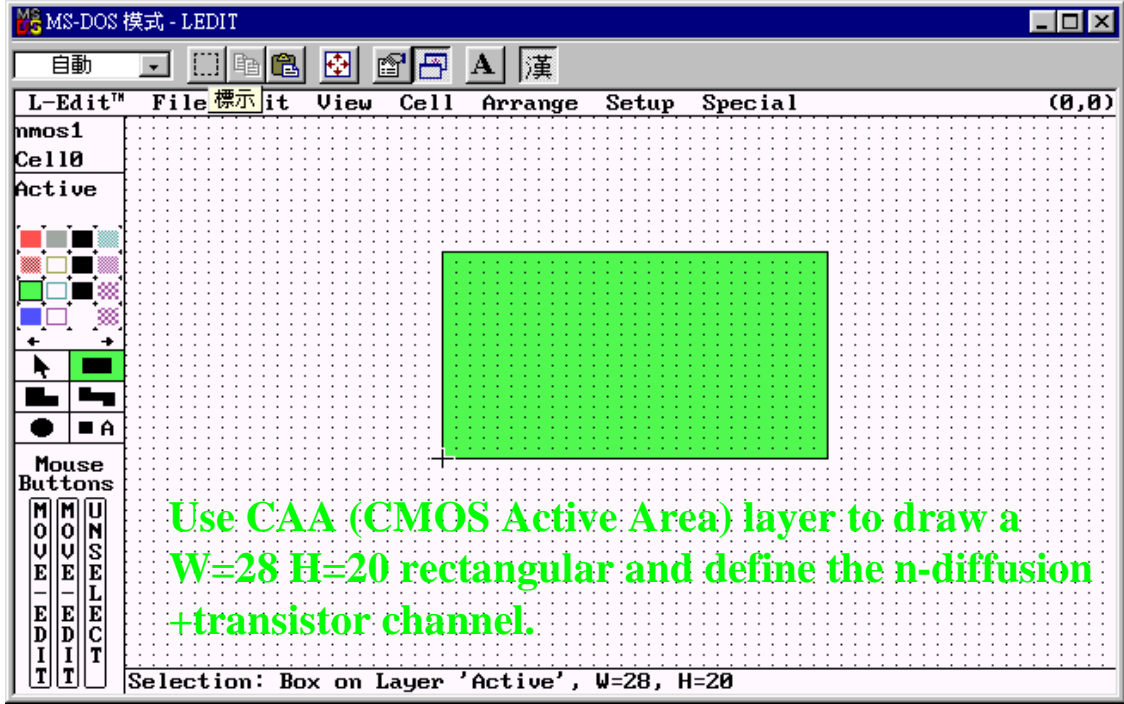
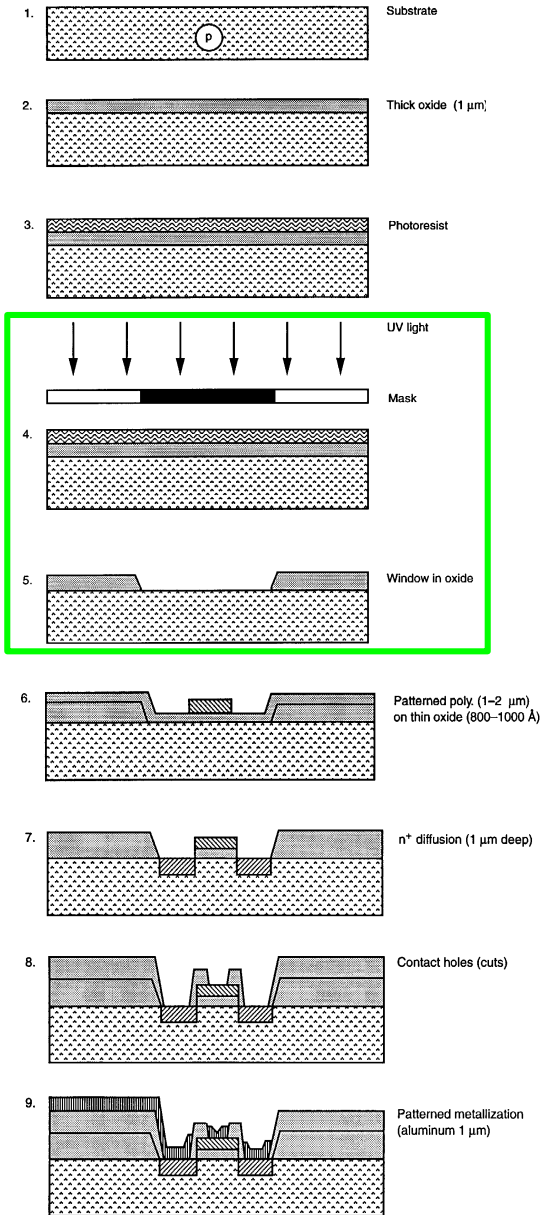


## KEY

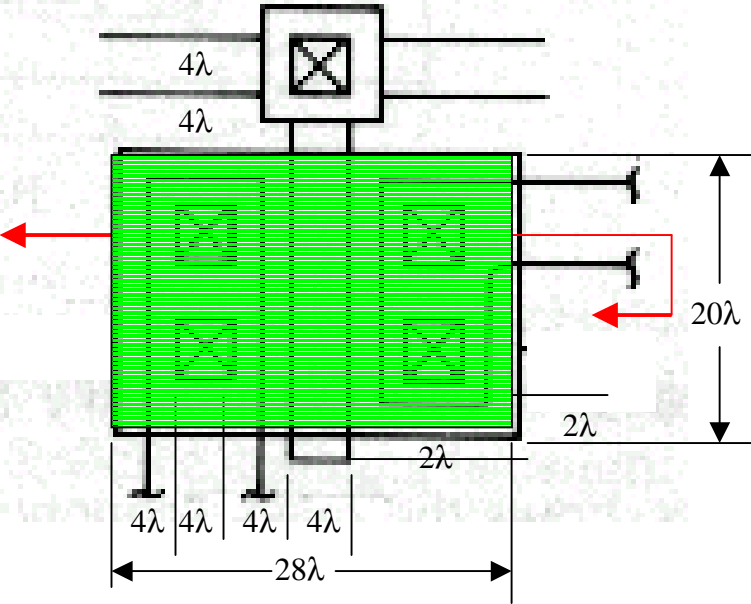
	Metal
	Polysilicon
	Oxide
	n-diffusion
	p-diffusion
	p-substrate
	n-substrate
	Depletion



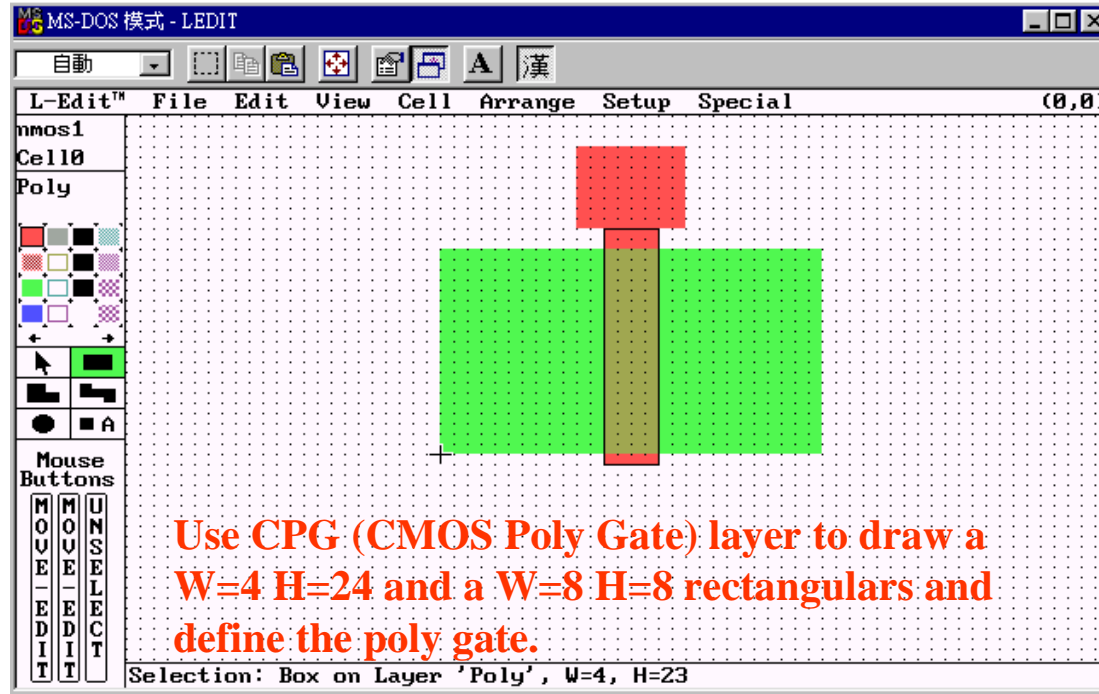
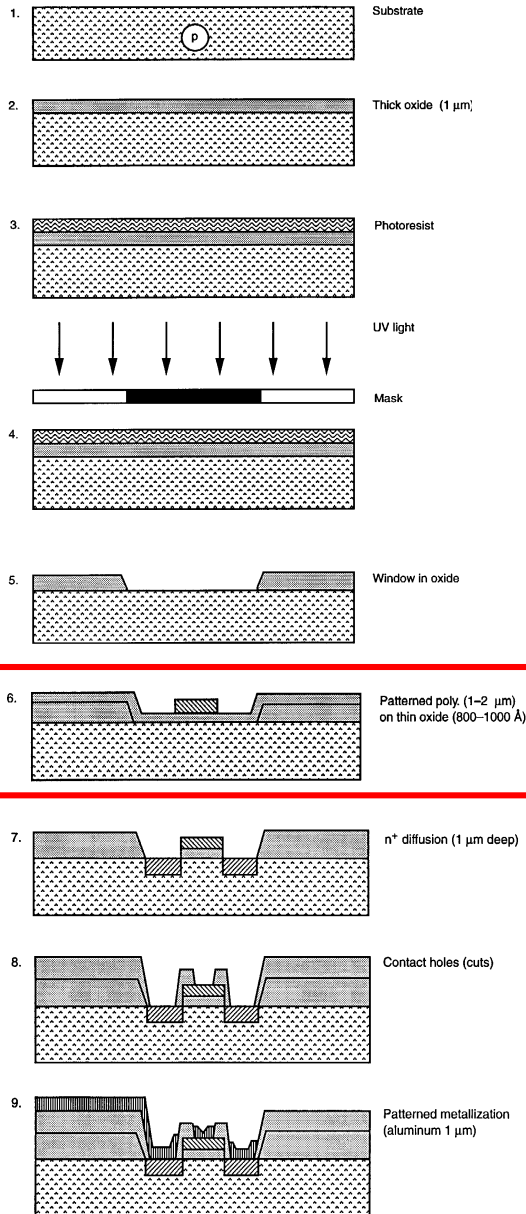
# Mask #1- CAA



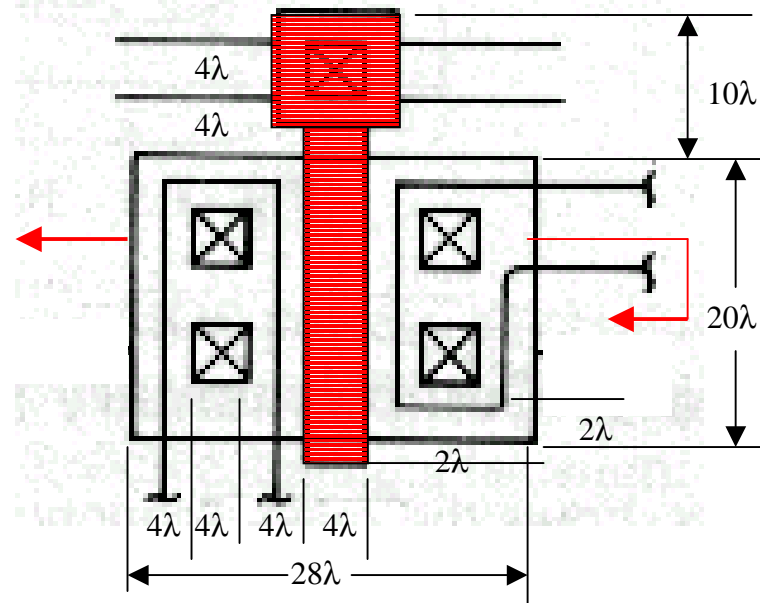
Use CAA (CMOS Active Area) layer to draw a W=28 H=20 rectangular and define the n-diffusion + transistor channel.



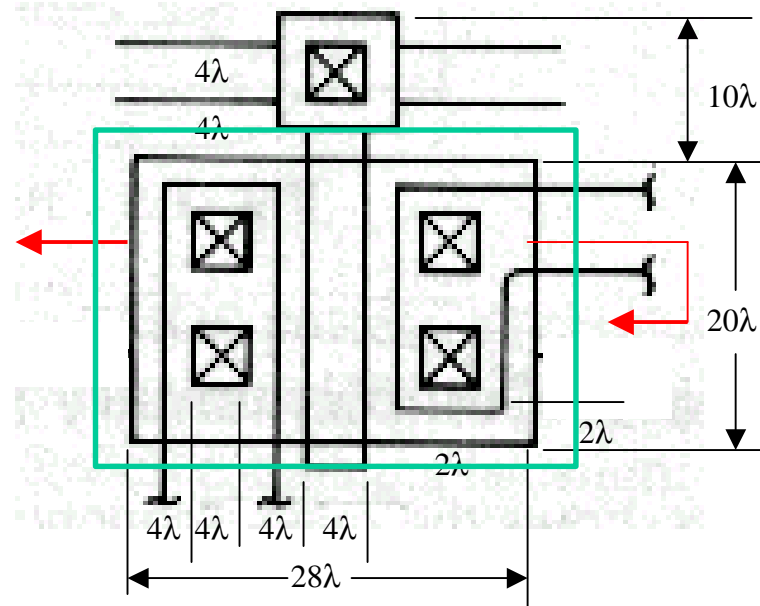
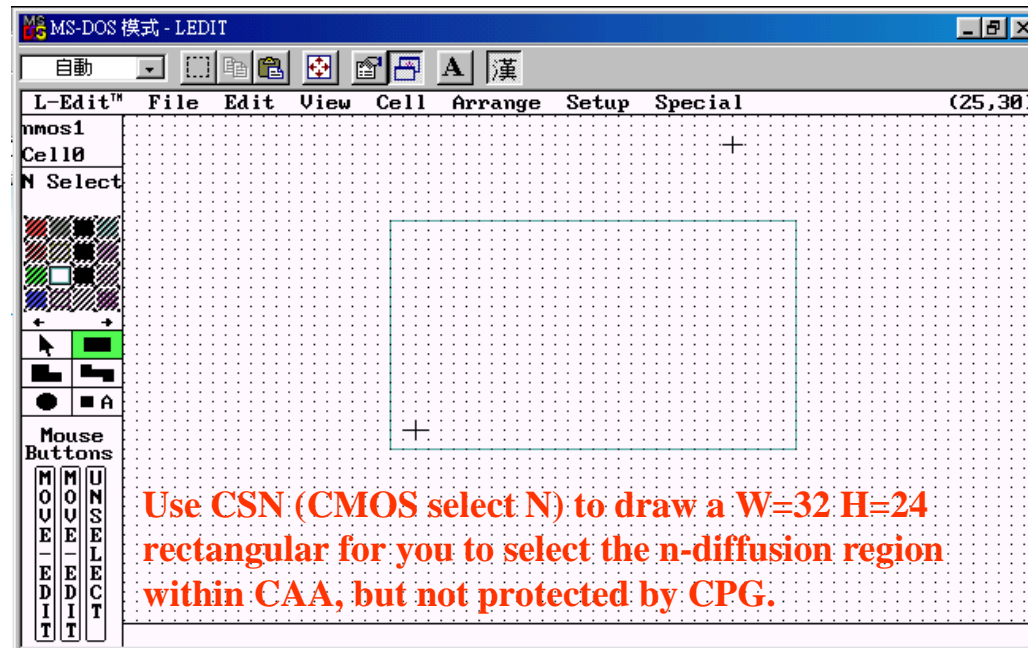
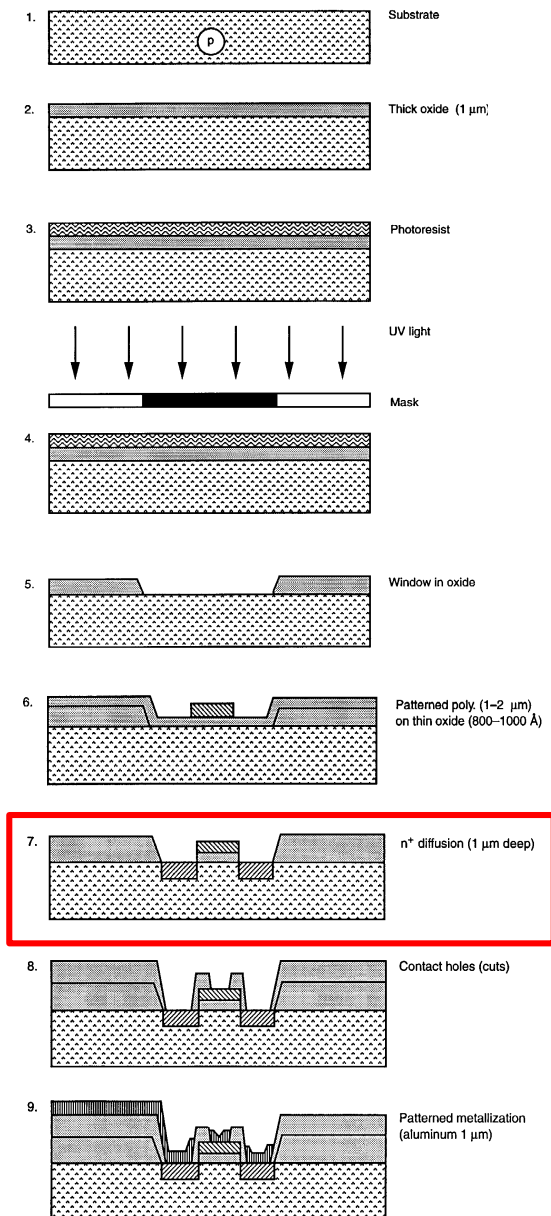
# Mask #2- CPG



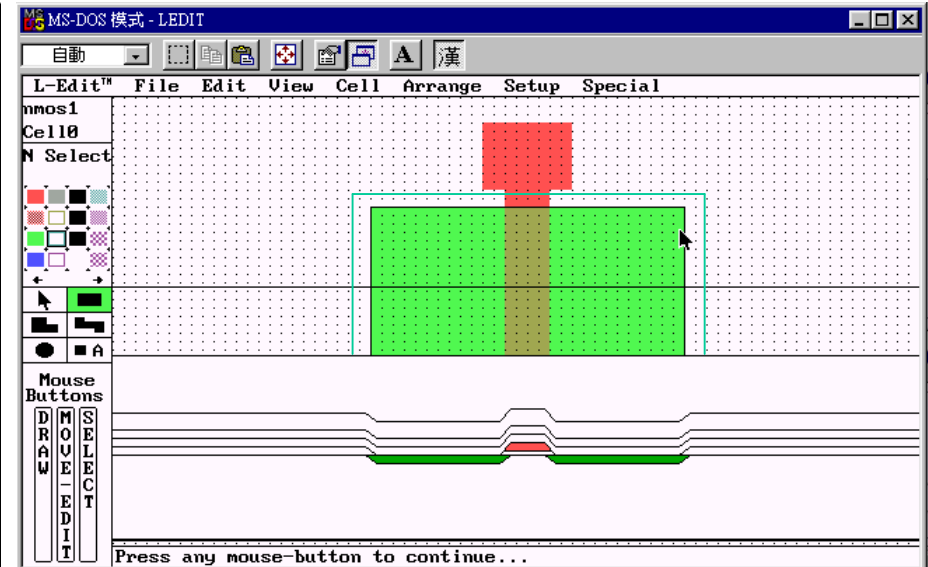
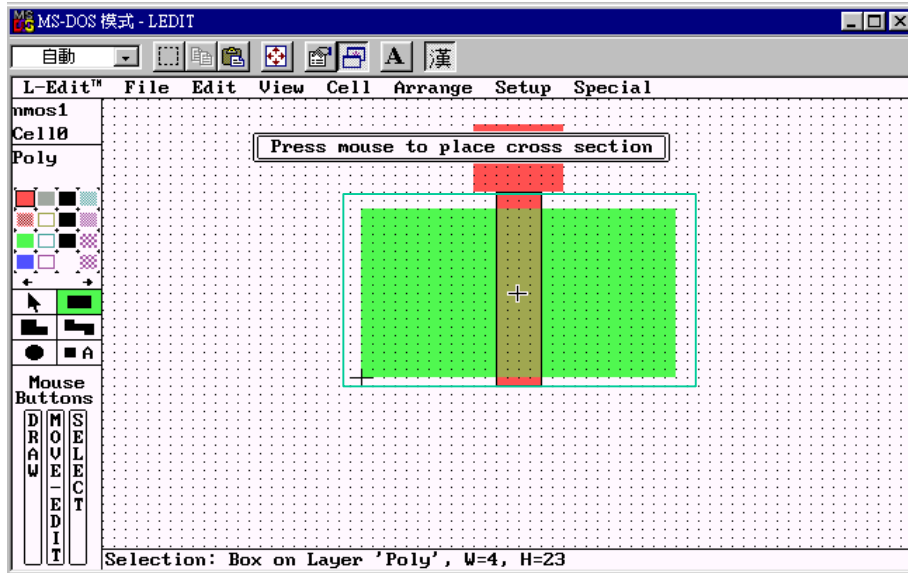
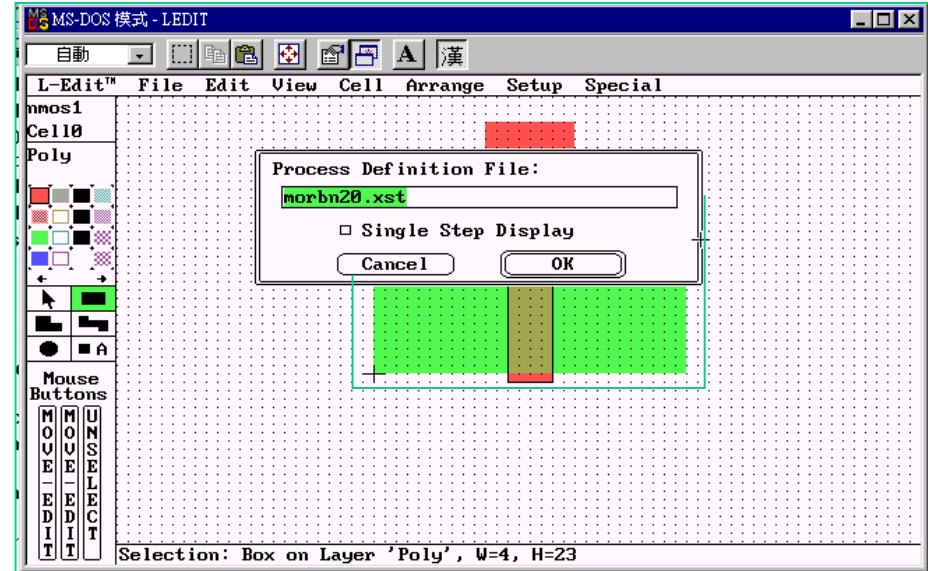
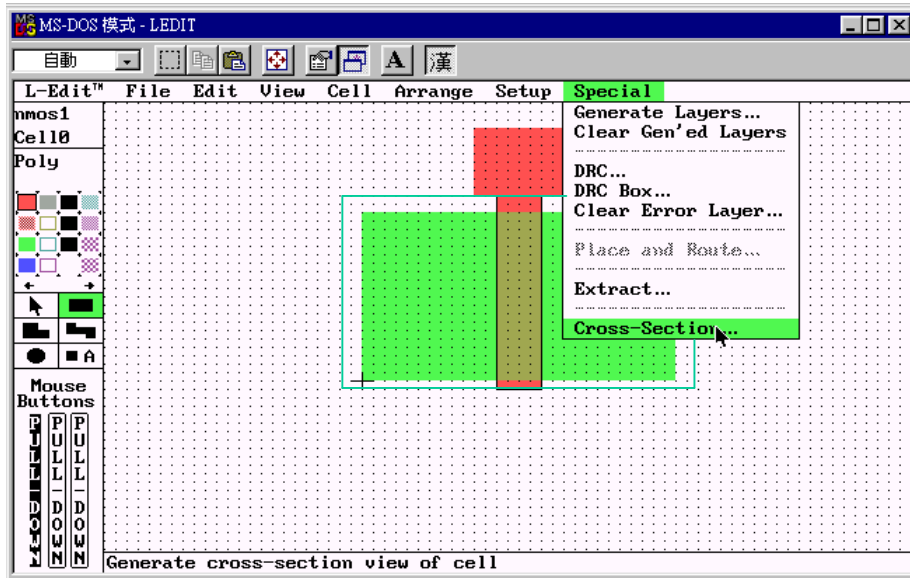
Use CPG (CMOS Poly Gate) layer to draw a  $W=4\ H=24$  and a  $W=8\ H=8$  rectangulars and define the poly gate.



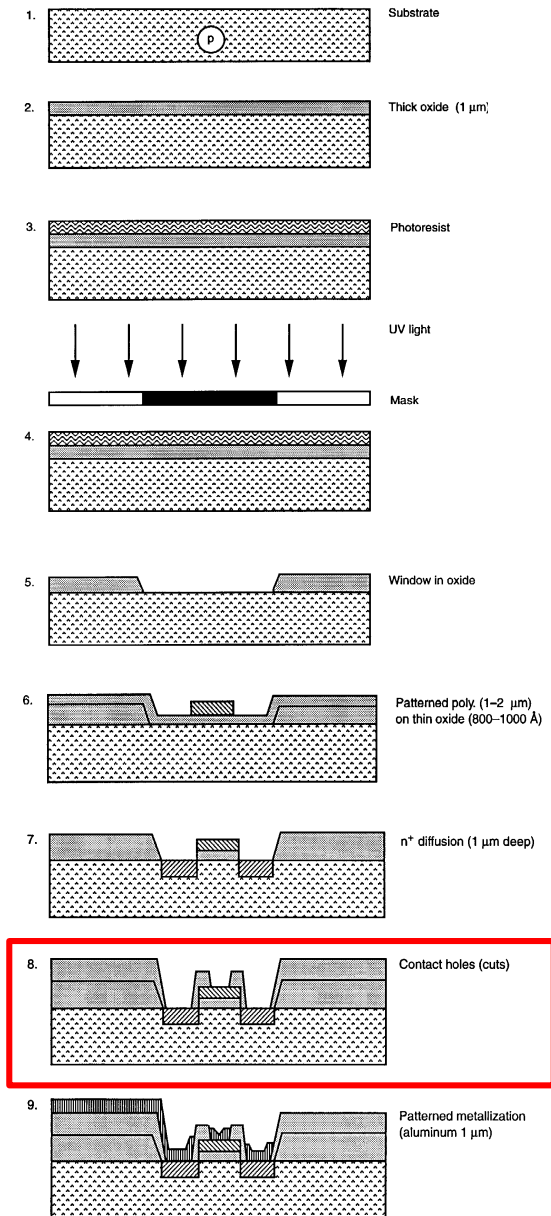
# Mask #2 again for n<sup>+</sup>-diffusion (CSN)



# Cross-Section



# Mask #3- CCP & CCA



MS-DOS 模式 - LEDIT

L-Edit™ File Edit View Cell Arrange Setup Special (0,0)

nmos1  
Cell10  
Poly Contact

CCP

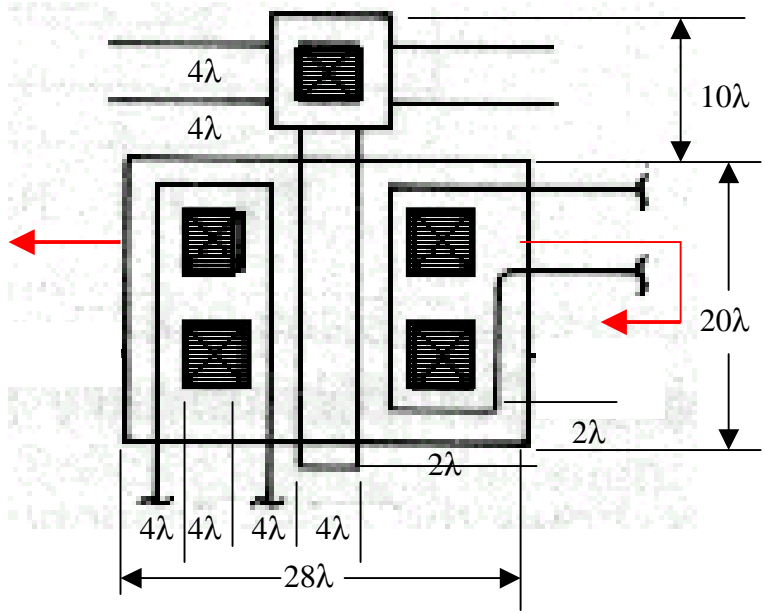
CCA

CCA

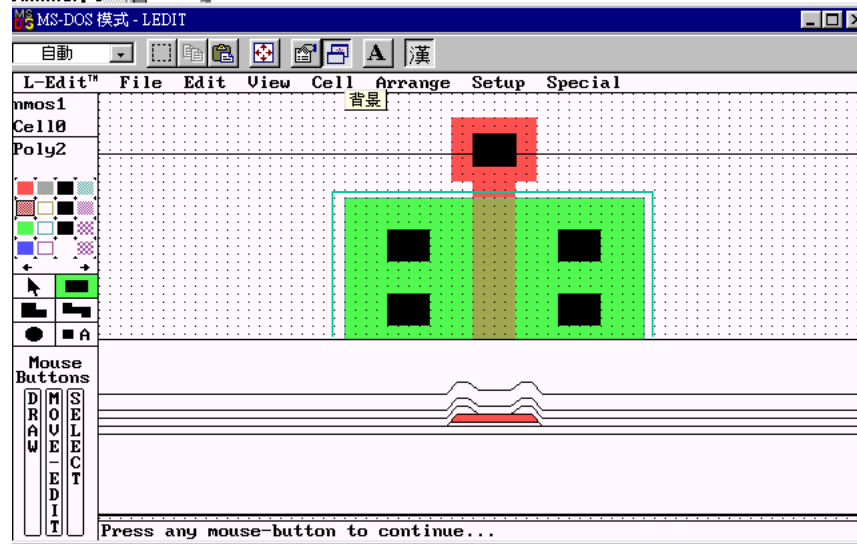
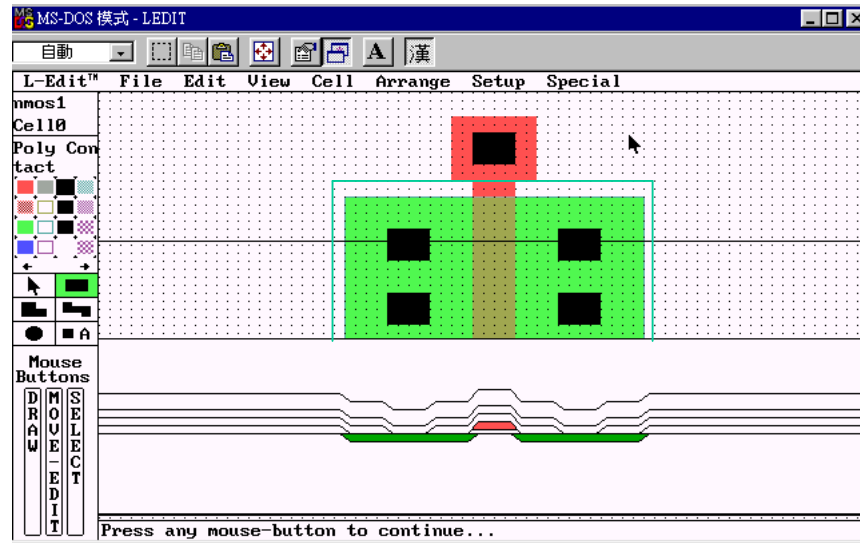
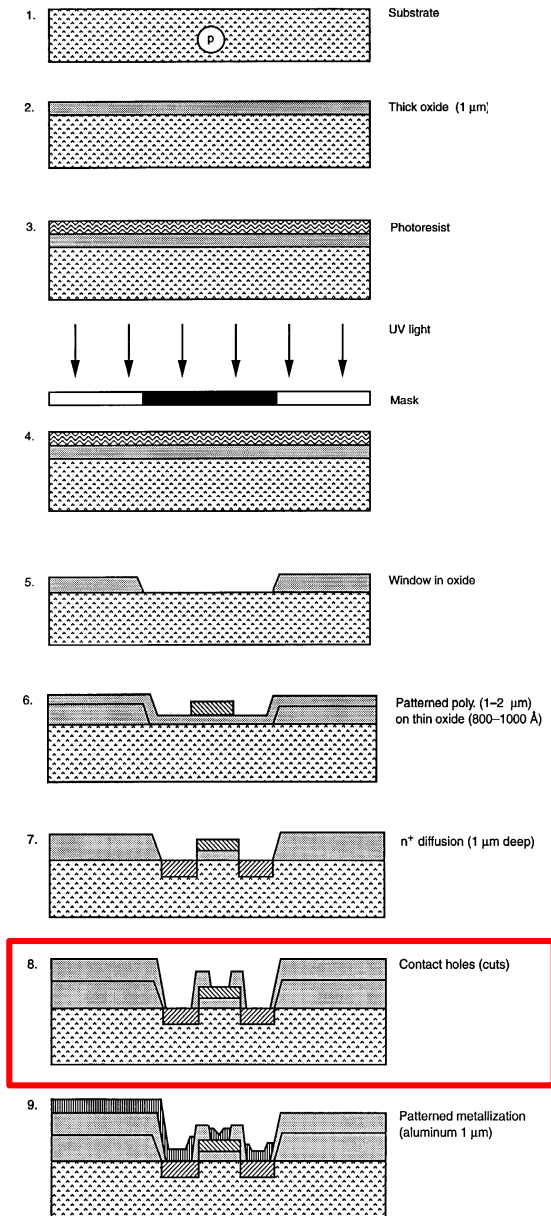
Mouse Buttons  
MOVE EDIT UNSELECT

Use CCP (CMOS Contact Poly) and CCA (CMOS Contact Active) to draw 5 W=4 H=4 rectangular to open the poly contacts through thick OX

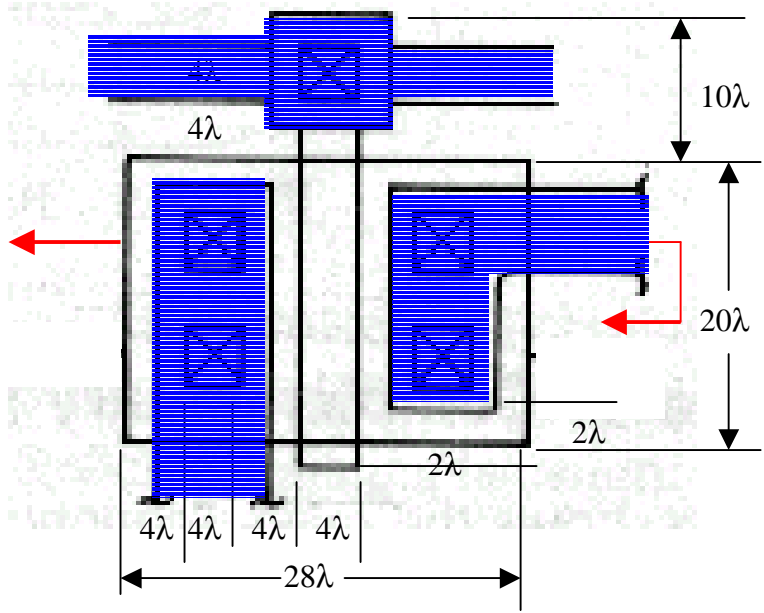
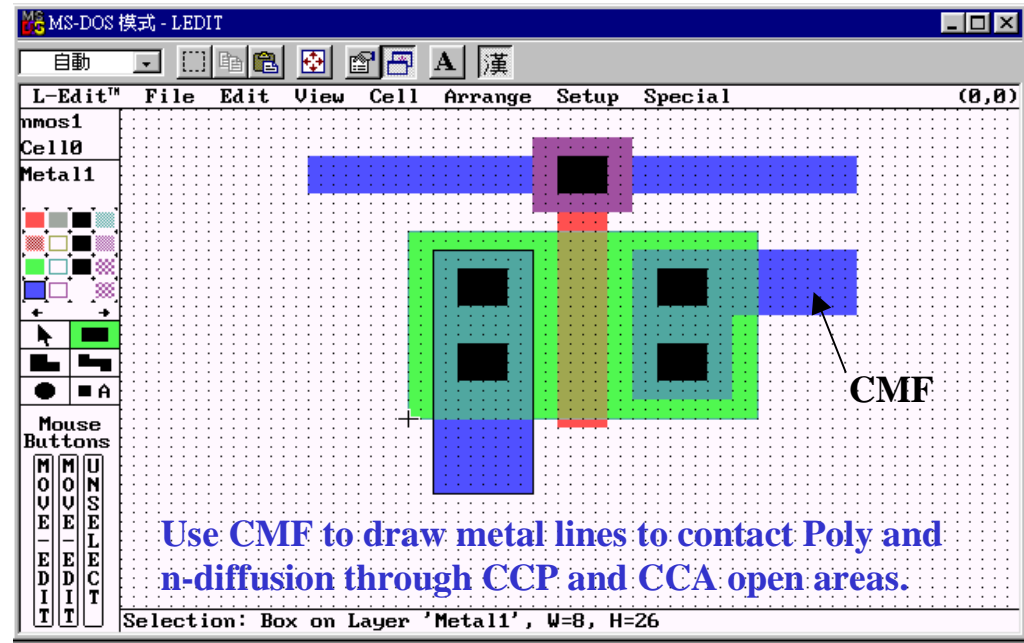
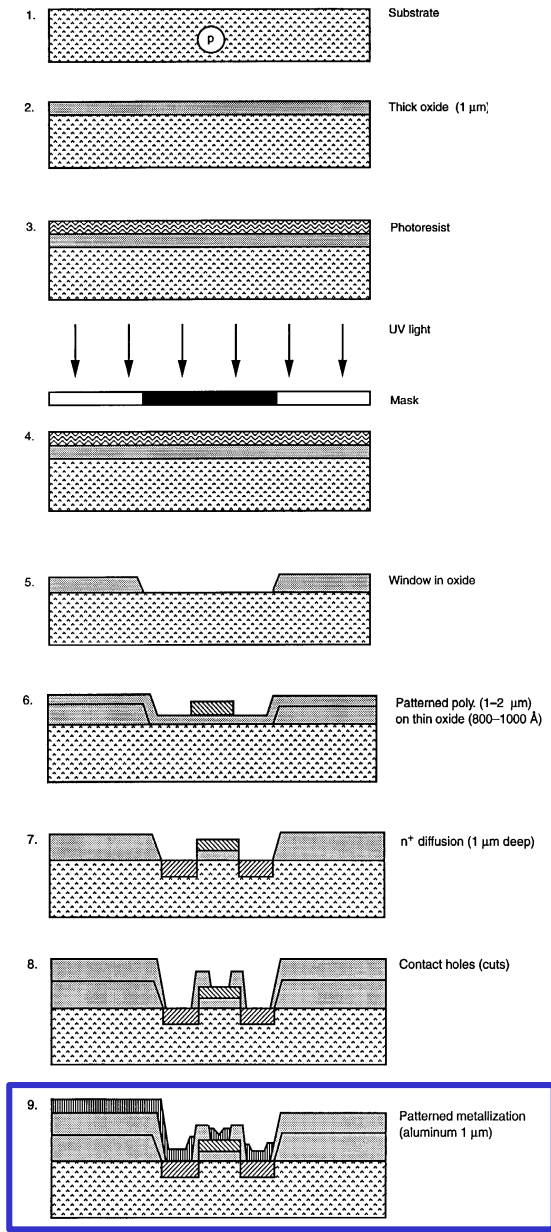
Selection: Box on Layer 'Poly Contact', W=4, H=4



# Cross Section after Mask #3

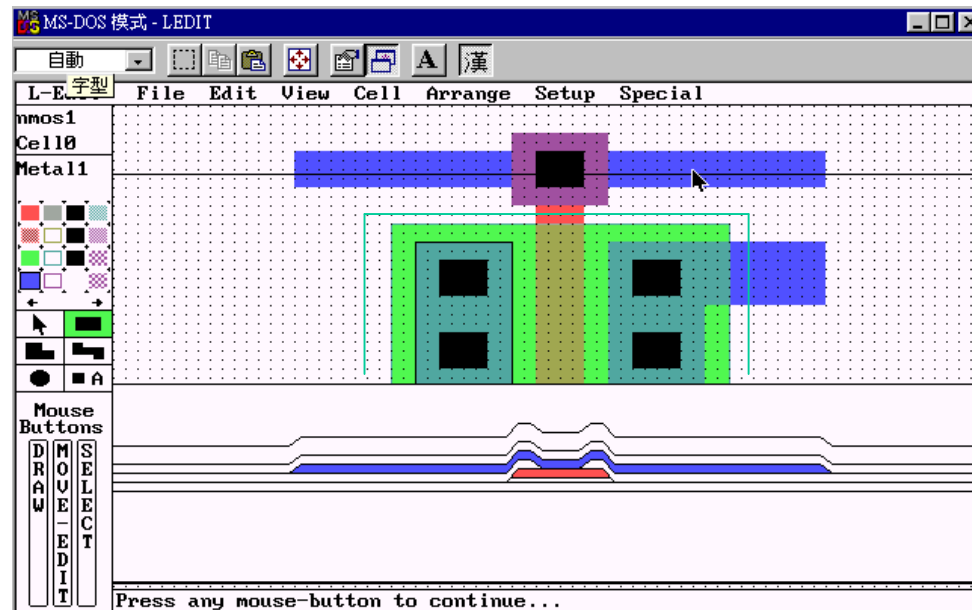
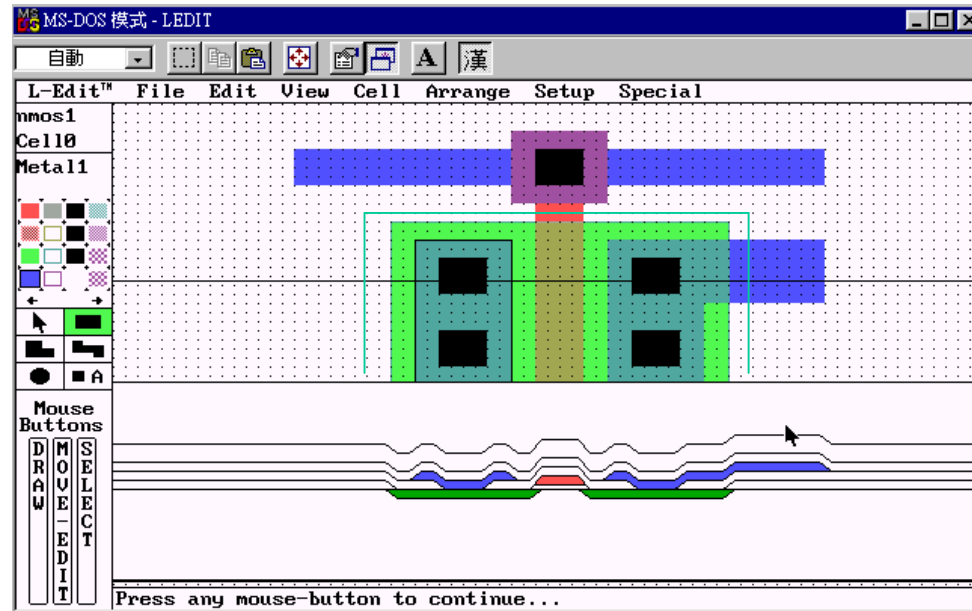
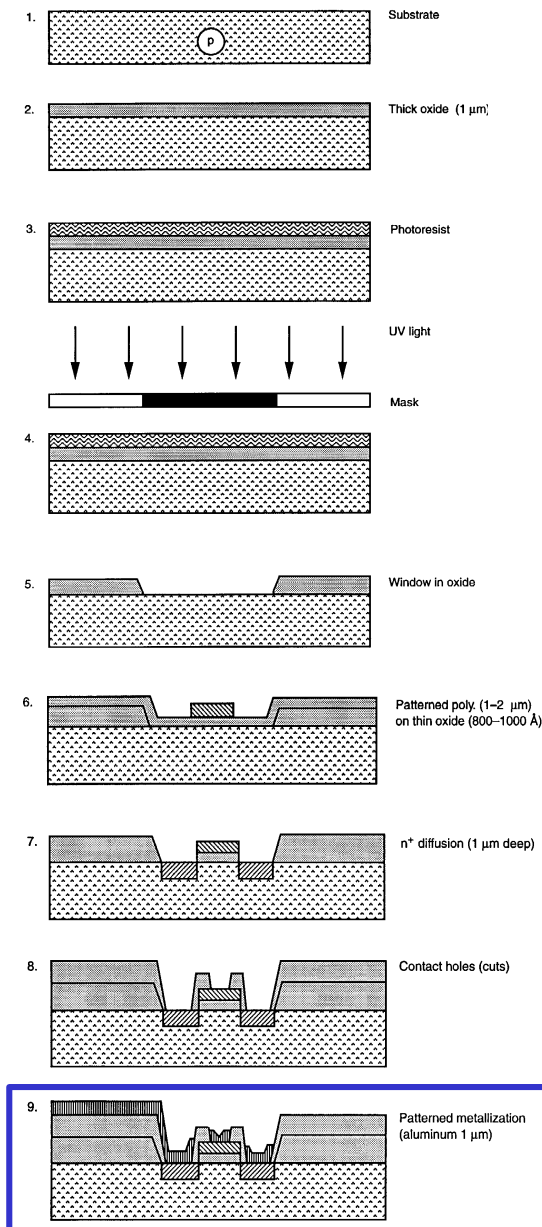


# Mask #4 - CMF

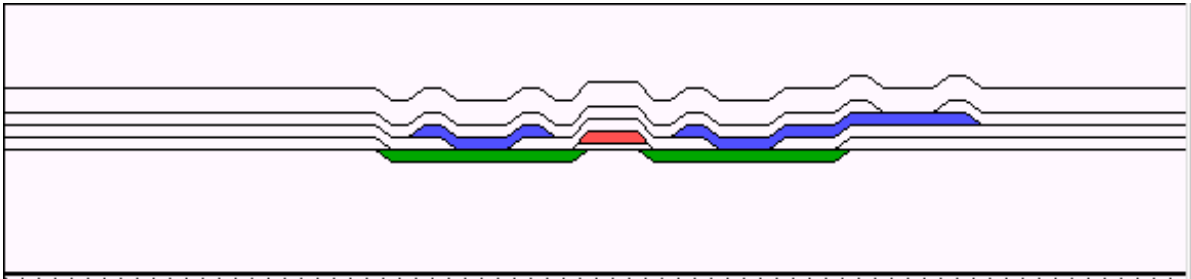
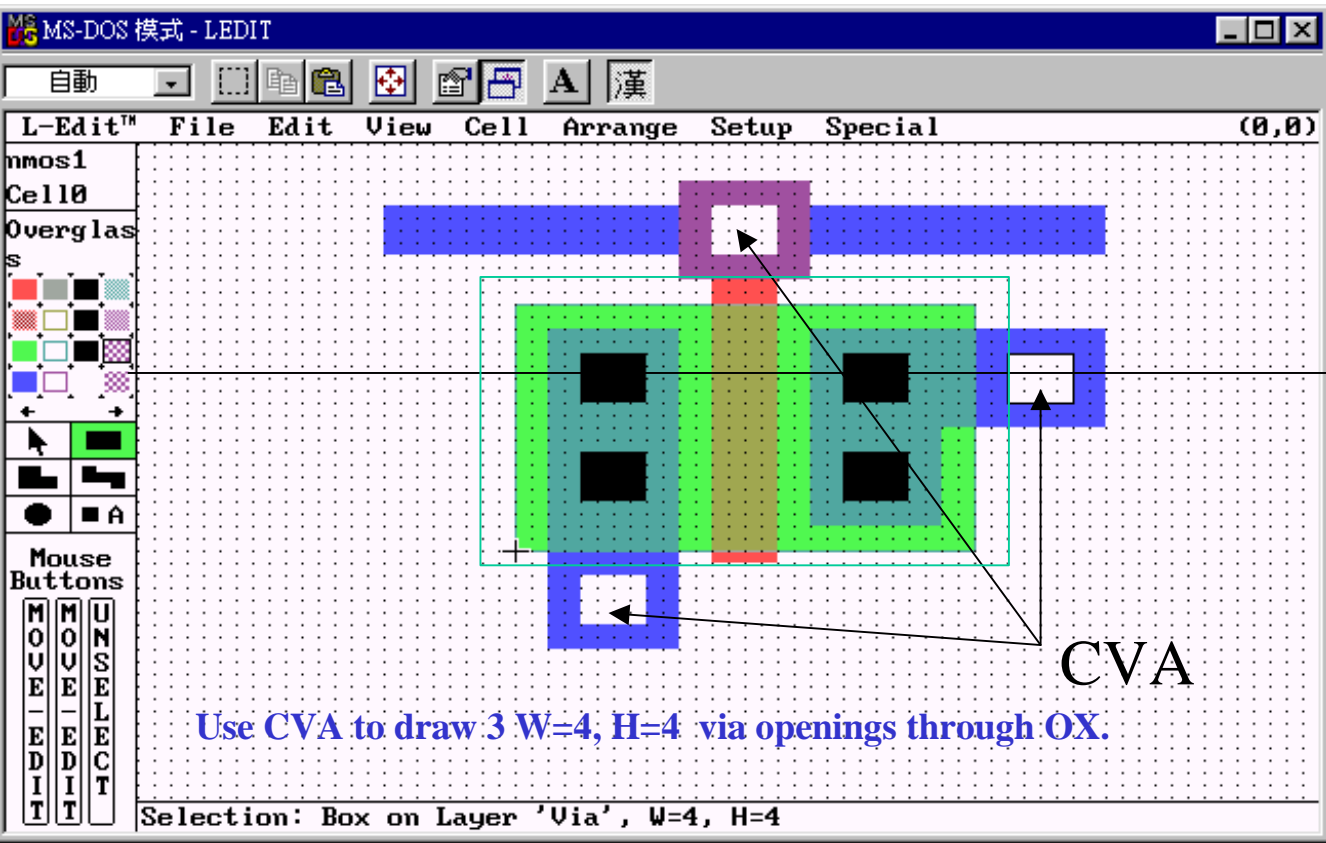




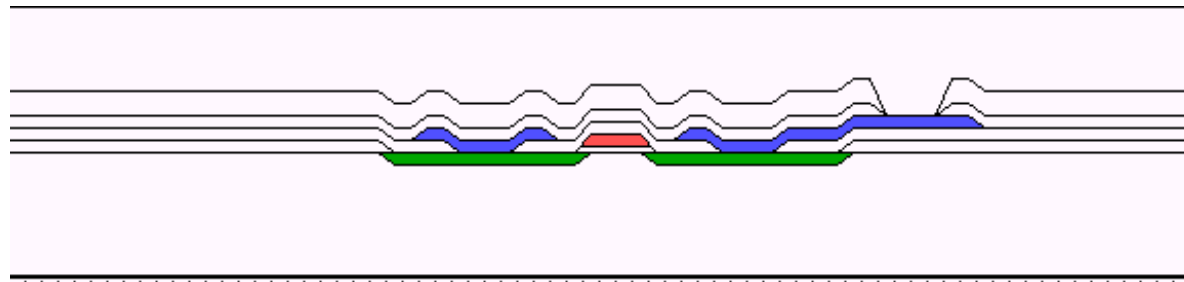
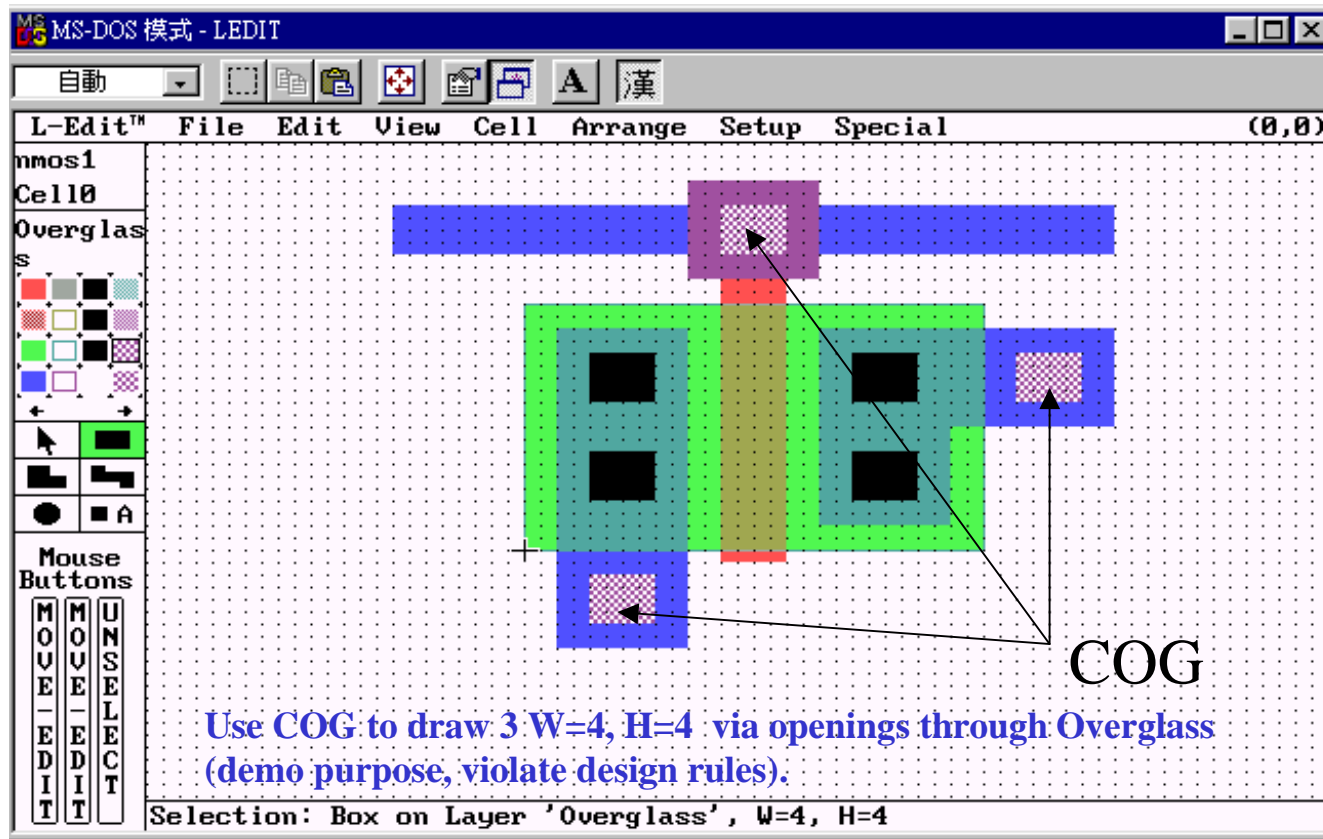
# Cross Section after Mask #4



# Mask #5 – Via layer



# Mask #6 – Overglass Opening



# Summary of nMOS Layers

