MIT Haystack Observatory Technology Development Center

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Abstract Technology development at MIT Haystack Observatory was focused on the following three areas in 2014: (1) KPGO 12-m Signal Chain, (2) VLBI Data Acquisition Module, and (3) Mark 6. In this report, we outline the three main sub-systems comprising the KPGO signal chain and describe a new generic/open-source monitor and control module possessing a small, modular form factor. Lastly, we describe the latest refinements applied to the Mark 6 16 Gbps recorder software suite.

1 KPGO 12-m VGOS Signal Chain

MIT Haystack Observatory is responsible for the design, fabrication, and installation of the signal chain for the new KPGO 12-m VGOS system scheduled for installation at Kokee Park, HI, in September 2015. This signal chain is comprised of three separate subsystems: (1.1) frontend, (1.2), backend, and (1.3) calibration.

1.1 Frontend Sub-system

The frontend subsystem contains the very sensitive low noise electronics and radio telescope feed necessary to achieve a system equivalent flux density of 2,500 Jy when integrated with the Intertronics Solutions Inc. 12-m antenna. The frontend also includes all supporting infrastructure (e.g. networking, power supply distribution, and monitor/control) necessary to operate the dual-linearly polarized cryogenic receiver frontend. Furthermore, a phase/noise calibration signal is injected directly into the frontend to provide a mechanism for instrumental delay/gain correction in post-correlation processing. Within the frontend, the power levels amplified are such that they are suitable to drive the high-band, microwave-over-fiber link that is used to downlink these signals to the backend sub-systems. To conserve dynamic range in the high-band link, the RFI afflicted S-band portion of the frontend frequency range is downlinked separately over a coaxial downlink which possesses significantly more dynamic range to support observing in this frequency band. A block diagram of the signal chain frontend sub-system is shown in Figure 1.

1.2 Backend Sub-system

The backend sub-system receives the microwave signals downlinked from the frontend sub-system for further processing. A block diagram of this backend subsystem is shown in Figure 2.

Both low and high band signals from the frontend subsystem can be distributed to four independently tunable 2—14 GHz UDCs. This UDC supports 2 GHz baseband output with fine LO tuning resolution (< 1 Hz) to accommodate compatibility with other VGOS frequency conversion schemes. These features are provided by the next generation UDC V2.0, which incorporates an additional downconversion stage not included in its predecessor. The fine tunability of this design is made possible by a custom LO that was de-

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signed at Haystack and incorporates a finely tunable DDS. Figure 3 displays a layout of the custom LO circuitry.

In the KPGO implementation, 512 MHz Nyquist zone filters are incorporated in the UDCs to support the sample rate of the RDBE (1024 MHz). Following PFB processing by the RDBE, the digitized data are recorded onto hard disk by a single Mark 6 recorder capable of sustaining the 8 Gbps data rate onto a single disk module.

1.3 Calibration Sub-system

The calibration sub-system is physically split between the frontend (on the antenna) and backend (in the control room). This sub-system is responsible for generating phase and noise calibration signals in the frontend sub-system. In this frontend, these signals are injected into the receiver to facilitate correction of instrumental delay and gain variations in the radio source (e.g., quasar) signal path.

Accurate correction of the instrumental delay variations in this signal path is somewhat complicated by the need to uplink the timing reference (i.e., 5 MHz MASER reference) to the frontend. The complication arises because the delay in this timing reference is subject to variations that are independent of the variation in the quasar signal path downlink. A primary source of these variations is mechanical stress fluctuations imparted on the reference cable by the motion of the antenna. Hence, the calibration sub-system must monitor variations in this reference cable delay so that they may be removed from the phase variations extracted by the correlator.

The resultant instrumental phase estimate represents that imparted on the quasar signal as it propagates through the signal chain. A proof-of-concept cable delay measurement system has been developed and is currently being tested to address this requirement. The calibration signal generator (i.e., the antenna unit) is being redesigned to integrate this new capability. This effort is expected to be complete in the first quarter of 2015.

2 VLBI Data Acquisition Module

MIT Haystack Observatory has developed the VLBI Data AcQuistion (VDAQ) module as an open source hardware development to address general purpose monitor and control requirements at the generic VLBI station. As a modular instrument, the VDAQ makes dual use of Ethernet infrastructure, using the Ethernet backbone to provide both communication and power interfaces into the module. This feature of the VDAQ serves to provide a small form factor (13x10x2.5 cm) and allows it to be deployed to space-limited locations where MCI is needed. Figure 4 presents a 3D CAD model rendering of the VDAQ module.

This modular concept also serves to minimize issues related to signal integrity because sensors and signal monitors can be placed in close proximity to the module which can also serve as a distributed power source. The following provides a breakdown of the interfaces that the VDAQ module will support:

- Digital Communications
  - RS232
  - I^2C
  - SPI
  - Ethernet
- Isolated DC Power Sources
- 16 Analog Monitors
  - Single-ended or Differential
  - Isolated or Non-Isolated
  - Configurable signal conditioning
- 40 Digital Monitors or Controls
  - 10 Isolated Monitors
  - 10 Isolated Controls
  - 20 Non-isolated Monitors and/or Controls

3 Mark 6 Developments

In 2014, the software utility *vdifuse* was commited to the DiFX repository. *vdifuse* mounts the disk modules as local directories readable by the Mark 6 OS and performs the pointer mathematics necessary to navigate the scattered nature of the Mark 6 recording methodology. In this way, *vdifuse* allows the Mark 6 user to

interact with scans recorded on the Mark 6 disk module(s) as if they were contiguous files within the *vdifuse*-mounted directories. Using this utility, it is possibe to copy entire (and partial) scans from the mounted disk modules to the OS (or external, e.g., USB) disk. It is also possible to read these virtual files using standard Linux commands such as *ls*, *more*, *head*, and *tail*. It is not possible to utilize *vdifuse* to perform write operations on these mounted directories (e.g., the Linux delete *rm* command).

Lastly, Mark 6 software v1.2d was developed to resolve an IRQ bug that was discovered through testing. This bug introduced a loss of data at 16 Gbps data rate due to a non-uniform distribution of record processing load across the available CPUs. This software release is available through the EHT wiki at the following address: *http://eht-wiki.haystack.mit.edu*. Login credentials are required to obtain the package and can be obtained by contacting the EHT wiki webmaster at the aforementioned Web link.

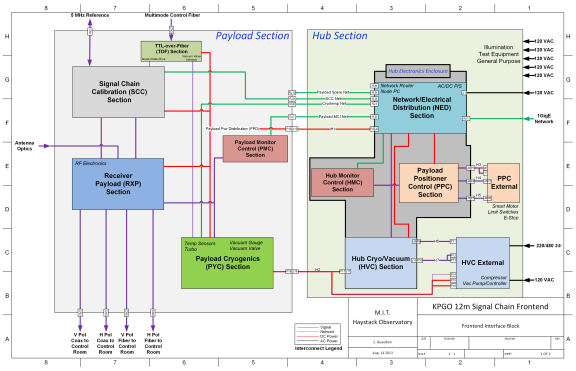

Fig. 1 Block diagram of the signal chain frontend sub-system. External connections into the frontend from the top/bottom represent those to the backend/calibration sub-systems. External connections into the frontend from the left/right represent those from the site's general infrastructure (not provided by Haystack).

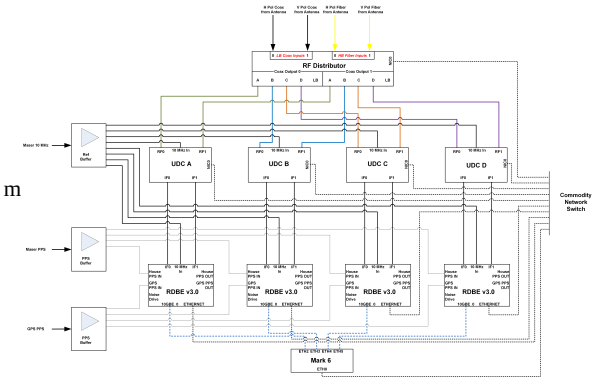

Fig. 2 Block diagram of the signal chain backend sub-system. External connections into the backend from the top represent those to the frontend sub-system. External connections into the frontend from the left/right represent those from the site's general infrastructure (not provided by Haystack).

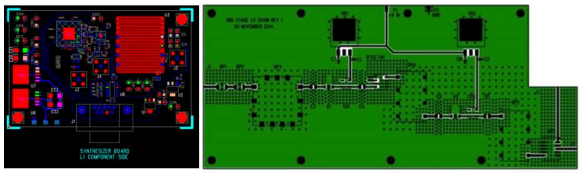

Fig. 3 PCB layouts of electronics designed for custom LO circuitry in UDC third downconversion stage.

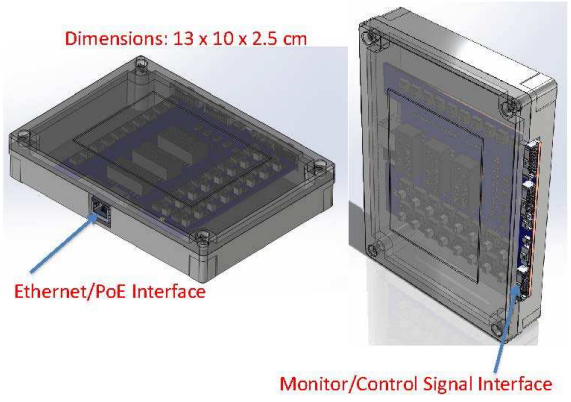

Fig. 4 3D CAD model rendering of the VDAQ module identifying its physical interfaces.