Tutorial 3 : Insert Scan Chain using Design Compiler
Authors: Bibhas Ghoshal & Subhadip Kundu

Objectives:

1. How to insert scan chain into a design .
2. Compare the area of synthesized netlist and scan inserted netlist.

1. Create a folder named dft in the project folder s27

>> mkdir dft

2. Invoke DftCompiler

Dft Compiler is actually embedded in the Design Compiler thus to invoke Dft Compiler, invoke design_vision

>> design_vision (GUI mode)

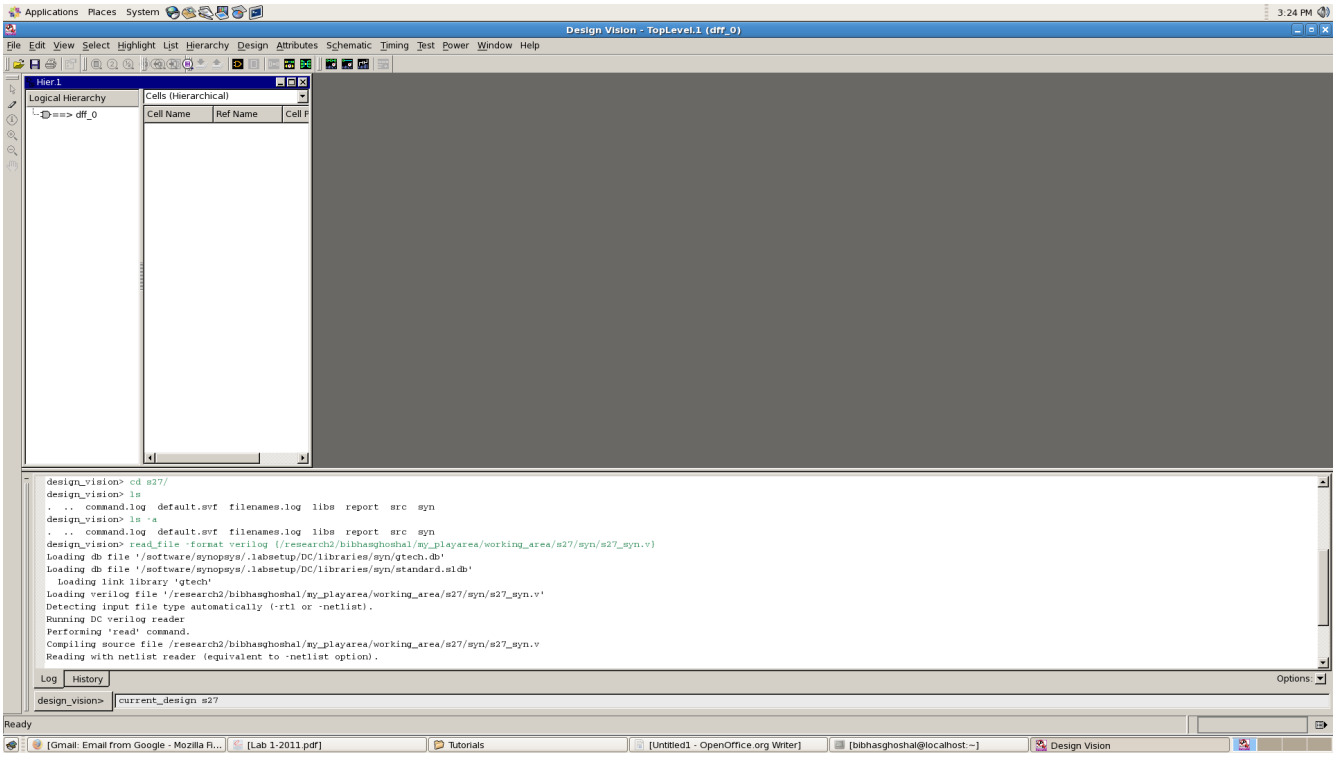
3.Read Input Netlist

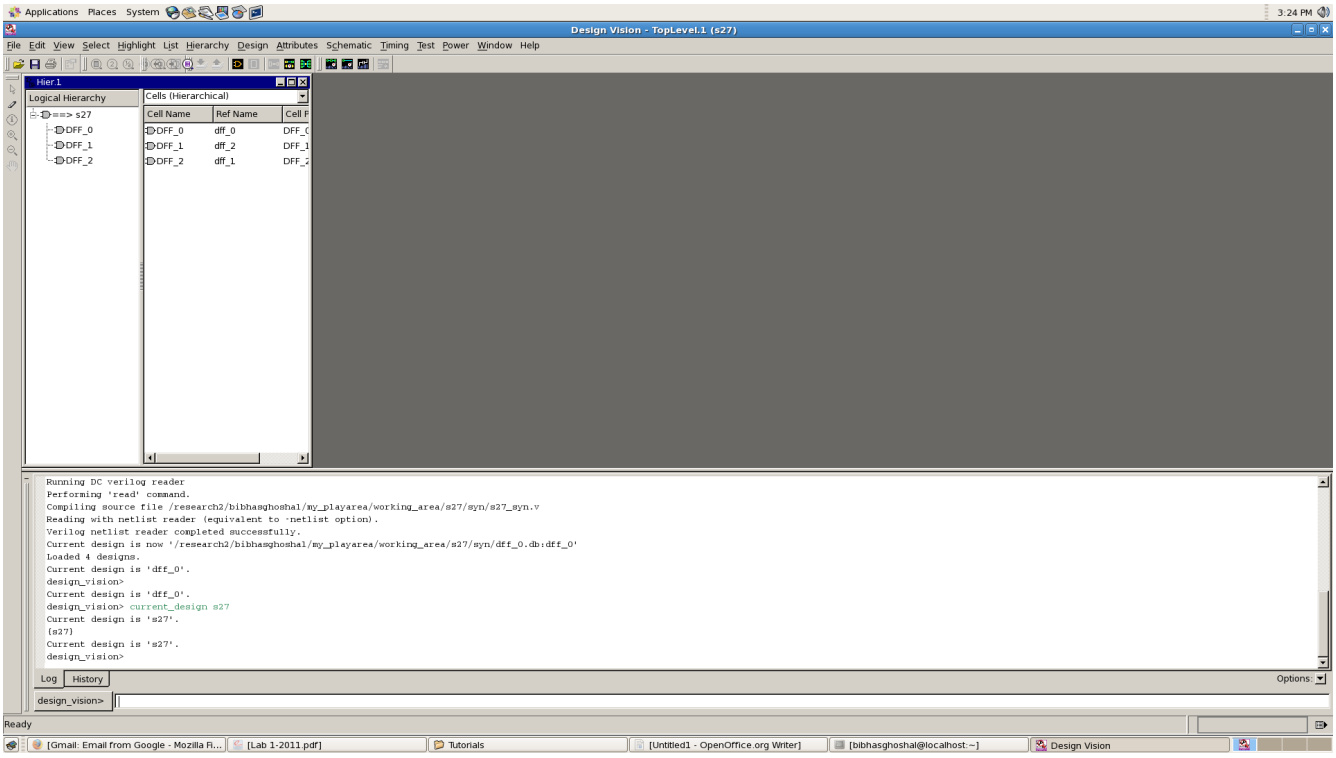
Read the synthesized netlist s27_syn.v created in Tutorial 2(b) from the syn folder of your project directory.
File-> Read (read s27_syn.v)

On reading the netlist, check whether the top level design is s27. If not then you can do either of the following:

i. current_design 27 at the command prompt of design_vision window

The screenshots below show the current design after the netlist is read and after current_deisgn command is typed.


Applications Places System
3:24 PM
Design Vision - TopLevel.1 (dff_0)
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power Window Help
Hier.1
Logical Hierarchy
==> dff_0
Cells (Hierarchical)
Cell Name
Ref Name
Cell F
design_vision> cd s27/
design_vision> ls
. .. command.log default.svf filenames.log libs report src syn
design_vision> ls -a
. .. command.log default.svf filenames.log libs report src syn
design_vision> read_file -format verilog {/research2/bibhasghoshal/my_playarea/working_area/s27/syn/s27_syn.v}
Loading db file '/software/synopsys/.labsetup/DC/libraries/syn/gtech.db'
Loading db file '/software/synopsys/.labsetup/DC/libraries/syn/standard.sldb'
Loading link library 'gtech'
Loading verilog file '/research2/bibhasghoshal/my_playarea/working_area/s27/syn/s27_syn.v'
Detecting input file type automatically (-rtl or -netlist).
Running DC verilog reader
Performing 'read' command.
Compiling source file /research2/bibhasghoshal/my_playarea/working_area/s27/syn/s27_syn.v
Reading with netlist reader (equivalent to -netlist option).
Log
History
Options:
design_vision>
current_design s27
Ready
[Gmail: Email from Google - Mozilla Fi...
[Lab 1-2011.pdf]
Tutorials
[Untitled1 - OpenOffice.org Writer]
[bibhasghoshal@localhost:~]
Design Vision


Applications Places System
3:24 PM
Design Vision - TopLevel.1 (s27)
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power Window Help
Hier.1
Logical Hierarchy
==> s27
DFF_0
DFF_1
DFF_2
Cells (Hierarchical)
Cell Name
Ref Name
Cell F
DFF_0 dff_0
DFF_1 dff_2
DFF_2 dff_1
Running DC verilog reader
Performing 'read' command.
Compiling source file /research2/bibhasghoshal/my_playarea/working_area/s27/syn/s27_syn.v
Reading with netlist reader (equivalent to -netlist option).
Verilog netlist reader completed successfully.
Current design is now '/research2/bibhasghoshal/my_playarea/working_area/s27/syn/dff_0.db:dff_0'
Loaded 4 designs.
Current design is 'dff_0'.
design_vision>
Current design is 'dff_0'.
design_vision> current_design s27
Current design is 's27'.
{s27}
Current design is 's27'.
design_vision>
Log
History
Options:
design_vision>
Ready
[Gmail: Email from Google - Mozilla Fi...
[Lab 1-2011.pdf]
Tutorials
[Untitled1 - OpenOffice.org Writer]
[bibhasghoshal@localhost:~]
Design Vision

ii. Open the s27_syn.v in a text editor. Cut the verilog module s27 (at the end of the file) and paste it at the top of the file. Save the file and exit the editor.
Read the netlist again. This time you can see s27 as the top level module.

4. Scan Ready Synthesis :

Although you have done the synthesis before, you did not use the –scan option.
This compilation (with –scan option) considers the impact of scan insertion on mission mode constraints during optimization. This –scan option causes the command to replace all sequential elements during optimization. Type these lines.

```
-----------------------------------------------------------------
set_scan_configuration –style multiplexed_flip_flop
compile –scan

-----------------------------------------------------------------
```

5. ATE configuration

To create a test clock waveform, type

```
-------------------------------------------------------------------------------------------------
set_dft_signal -view existing_dft -type ScanClock -port CK -timing [list 40 60]
-------------------------------------------------------------------------------------------------
```

To create a test default ports, type

```
---------------------------------------
create_test_protocol
---------------------------------------
```

6. Pre-scan Check

This command checks if your follow the gate-level scan design rule. Type

```
---------------------------------------
dft_drc
---------------------------------------
```

7. Scan specification

This step tells the Dft Compiler how many scan chains you want. You can also specify the names of scan related pins (scan_enable, scan_in, scan_out). We will let Dft Compiler to choose the pin names for us.

---

set_scan_configuration -chain_count 1

8.Scan preview

This step checks your scan specification for consistency.

---

preview_dft

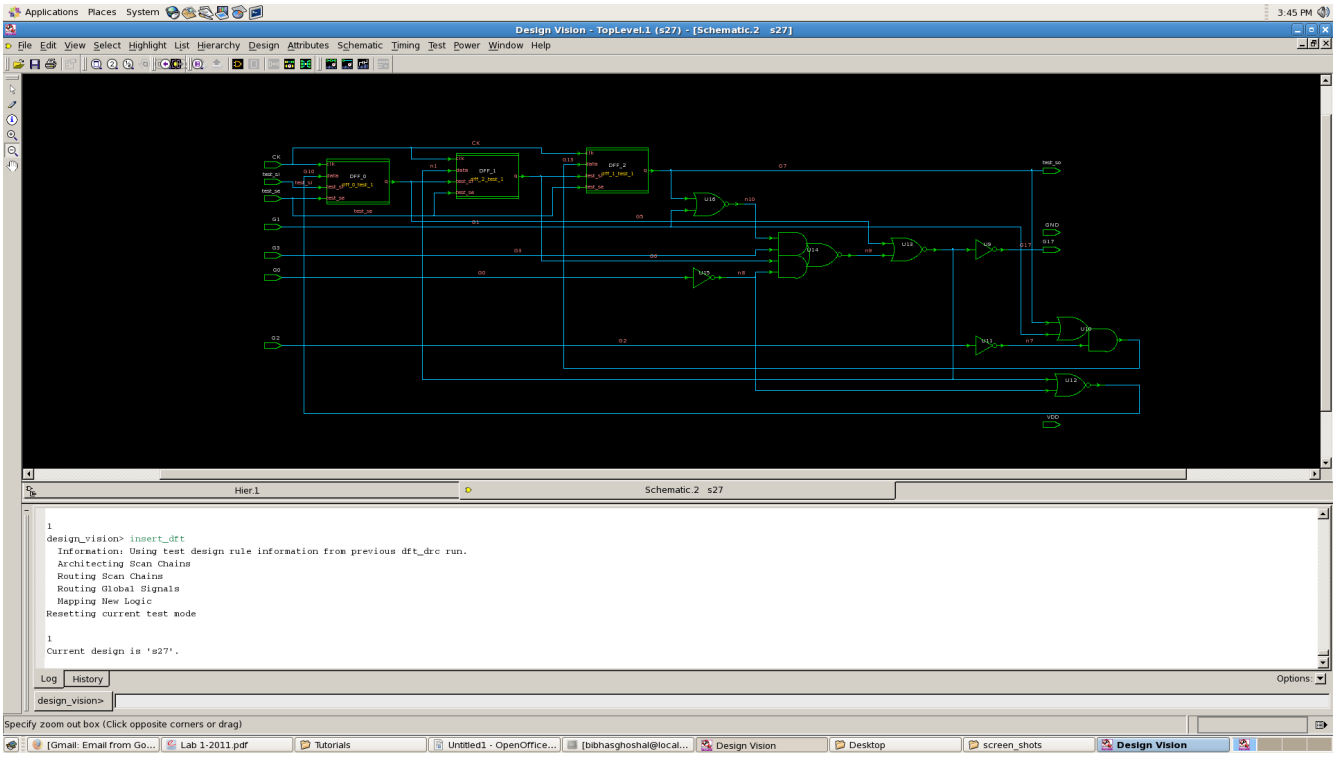
---

9. Scan chain synthesis : stitch your scan cells into a chain.

---

insert_dft

You should get the schematic view as shown in following screenshot.



10. Save your scan inserted netlist in the folder dft

---

write -format verilog -hierarchy -output s27_dft.v

---

11. Report Area of your scan inserted netlist