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15 February 1970

SPACE SYSTEMS

POWER CONDITIONING EQUIPMENT FOR A THERMOELECTRIC OUTER PLANET SPACECRAFT

QUARTERLY TECHNICAL REPORT

FOR FOURTH QUARTER, 1969

JPL CONTRACT NO. 952536

GENERAL ELECTRIC

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"THIS WORK WAS PERFORMED FOR THE JET PROPULSION LABORATORY, CALIFORNIA INSTITUTE OF TECHNOLOGY, AS SPONSORED BY THE NATIONAL AERONAUTICS AND SPACE ADMINISTRATION UNDER CONTRACT NAS 7-100."

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ABSTRACT

This report covers activities performed from October through December, 1969 under JPL Contract No. 952536. This contract pertains to the design and development of the electrical system and the power conditioning equipment for the TOPS (Thermoelectric Outer Planet Spacecraft) program. During this reporting period a number of breadboard circuits were built and tested including quad redundant switching devices, quad redundant shunt regulators, high voltage conversion for TWT's, and microcircuit packaging. Power system studies have resulted in the tentative selection of DC distribution on a single bus with overcurrent and undervoltage protection features.

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SECTION 1. INTRODUCTION AND SUMMARY

This report covers activities performed under JPL Contract No. 952536 for the period 1 October 1969 through 31 December 1969.

The effort of this contract is directed at designing and developing the PCE (power conditioning equipment) for the TOPS concept. The function of this equipment is to receive power from RTG (Radioisotope Thermoelectric Generator) power sources and to condition, distribute and control this power for the spacecraft loads. The TOPS mission, aimed at a tour of the outer planets, will operate for an estimated 12 year period. Unique design characteristics required for the power conditioning equipment result from the long mission time and the need for autonomous on-board operations due to large communications distances and the associated time delays of ground initiated actions.

The TOPS program was specifically initiated as a means for evaluating the status of various subsystem technologies for extended outer planet missions. This particular power conditioning equipment contract is being conducted within this context. Near term objectives are to develop subsystem concepts, conduct trade studies and identify and proceed with necessary technology developments. Specific trade studies are concerned with the use of AC or DC distributed power, the need for batteries, and the selection of bus configurations which yield a high probability of mission success. Technology developments pertain principally to techniques for increasing the life of power equipment and devices. These include examinations of such items as circuit redundancy and the possible replacement of life limited mechanical relays by solid state switching devices.

Long-term goals will be aimed at designing; building and testing power conditioning equipment against detailed design requirements resulting from the near-term studies and integration with the overall TOPS concept.

The principal accomplishments during this period are as follows:

- Principal emphasis has been placed on a single bus DC distribution system with overcurrent and undervoltage protective features.
- Present weight estimates for the power conditioning equipment are as follows:

  PCE within power system - 36.5 lbs.

  PCE in other subsystems - 66.5 lbs.
- Thermal loading within the PCE equipment bay appears excessive; alternative shunt configurations are being considered.
- Relay and semiconductor switches in quad redundancy configurations were built and successfully tested.
- A quad redundant shunt regulator was built and successfully tested.
- Several transformer configurations have been built and tested for the TWT converter. Operation appears satisfactory though efficiency is low.
- "Flat pack" thick film microcircuitry assemblies have been built and tested, demonstrating their applicability for DC to DC converters.
- A two-phase inverter was fabricated, tested and delivered to JPL.

SECTION 2. STUDY APPROACH

Original goals in the TOPS-PCE program were to establish component requirements early in the contract period with the objective of designing, fabricating and testing three engineering model sets of the PCE for delivery to JPL by July 1970. As the result of reevaluation and extension of the overall TOPS program schedule, the original goals have been modified as follows. Greater emphasis is to be placed on power system requirements and definition, with particular attention given to the interplay and interdependence with other TOPS subsystems. As presently planned, only one breadboard set of PCE will be fabricated, tested and delivered by July, 1970.

A Work Plan reflecting this change in emphasis is shown on Figure 2-1. The activities have been divided into five categories relating to: (1) Power System Requirements; (2) Power System Design; (3) Trade Studies; (4) Technology Development; and (5) Program Management. A detailed description of tasks within each category is provided in Table 2-1.

TABLE 2-1 - TASK DESCRIPTIONS

NO.	TASK	SCOPE
1.0	Subsystem Requirements	Establish load profiles, mission constraints, technical interfaces, environments, etc. through liaison with JPL.
2.0	Subsystem Design	Develop design of the subsystem through definition of the following:
	2.1 System Description	Electrical Configuration - Block diagrams, types of power, power level limitations, transient behavior
		Physical Configuration - Size, volume, weight, thermal characteristics, location
		Interfaces - computer, telemetry, command, attitude control, etc.
	2.2 Operational Procedures	Test, ground checkout, flight operations
	2.3 Load Management	Power margin analysis
	2.4 Reliability	Design status evaluation, where and how redundancy should be applied.
3.0	Trade Studies	Evaluation of principal design alternatives
	3.1 Distribution Studies	Select the best distribution method from the point of view of efficiency, flexibility, experience, reliability and any other pertinent factors.
	3.2 Energy Storage Study	Synthesize two power systems with and without batteries. Compare these systems on the basis of weight and reliability. Provide recommendations as to preferred TOPS-PCE approach.
	3.3 Bus Configuration Study	Evaluate several practical bus configurations from the point of view of tolerance to source and/or load failures and the degree to which service can be restored.
	3.4 Shunt Regulation Study	Evaluate shunt regulation concepts from point of view of RTG protection, reliability, thermal load and electrical performance characteristics.
4.0	Technology Development	Identify required development items and proceed with design & breadboard development.
	4.1 Power Distribution Assembly	
	4.2 Shunt Regulator Assembly	
	4.3 TWT Converter	
	4.4 Two Phase Inverter Assembly	
	4.5 AC Power Conditioners	
	4.6 DC Power Conditioners	
	4.7 Power Source & Logic Assembly	
	4.8 Subsystem tests	Combine development components into a subsystem configuration & perform tests.
	4.9 Bench Test Equipment	Design and build equipment for component and subsystem tests.
	4.10 Advanced Circuit Development	Development of new and unique circuit concepts.
5.0	Program Management	Manage manpower resources, finances, schedules.

FOLDOUT FRAME 1

FOLDOUT FRAME 2

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SECTION 3. PROGRAM STATUS

This section reports on each of the task items listed in Table 2-1.

Task 1.0 Power System Requirements

Design guidelines for the TOPS Power Conditioning Equipment have been developing in conjunction with overall system design guidelines for the TOPS mission. At this point in the program, load estimates and sequence profiles are of a preliminary nature as are interface definitions with the numerous spacecraft subsystems. Some of the more important guideline factors used for concept development and initial sizing purposes are described below:

- Power source - 4 RTG's, each rated at 150 watts at beginning of mission and 110 watts at end of mission.
- Life - 12 years.
- No batteries to be used unless higher reliability and/or mission advantages can be demonstrated.
- Reliability shall be a strong factor in the PCE design, and shall be achieved through judicious part selection, use of redundancy, etc. No single component failure shall cause catastrophic failure of the PCE. No failure in the power source shall impair operation of the PCE. Additionally, redundant power supplies shall be used for all mission critical subsystems.
- On/off switching shall be provided for all non-mission critical subsystems.

- All power on/off switches and all primary/standby unit switches shall be commandable by both a primary source in the Central Computer and Sequencer (CC&S) and a backup source by ground command through the flight command subsystem.
- Telemetry points shall be incorporated in the PCE to provide the CC&S with information on the performance of the PCE, so that in the event of PCE failures the CC&S can take corrective action (switch to a standby unit, remove a faulted load from the bus, etc.)
- Some capability will exist in the PCE to detect faulted loads or PCE failures, and to remove faulted loads or switch to standby PCE units in the event that the CC&S is unable to perform these functions.
- Short circuit protection in the form of circuit breakers that may be reset by CC&S or ground command shall be provided for bus protection at the front end of PCE power supplies:
  a) As a series element for all subsystems which are not mission critical;
  b) Where necessary to insure that a secondary mode of operation is obtainable by either on-board logic or ground command in the event of a failure in an element of the primary mode.
- Circuitry shall be provided to minimize power switching transients and to limit current in the event of a load or power supply fault.
- Non-toggle switching shall be used so that knowledge of switch status is not required and so that multiple commands can be sent.

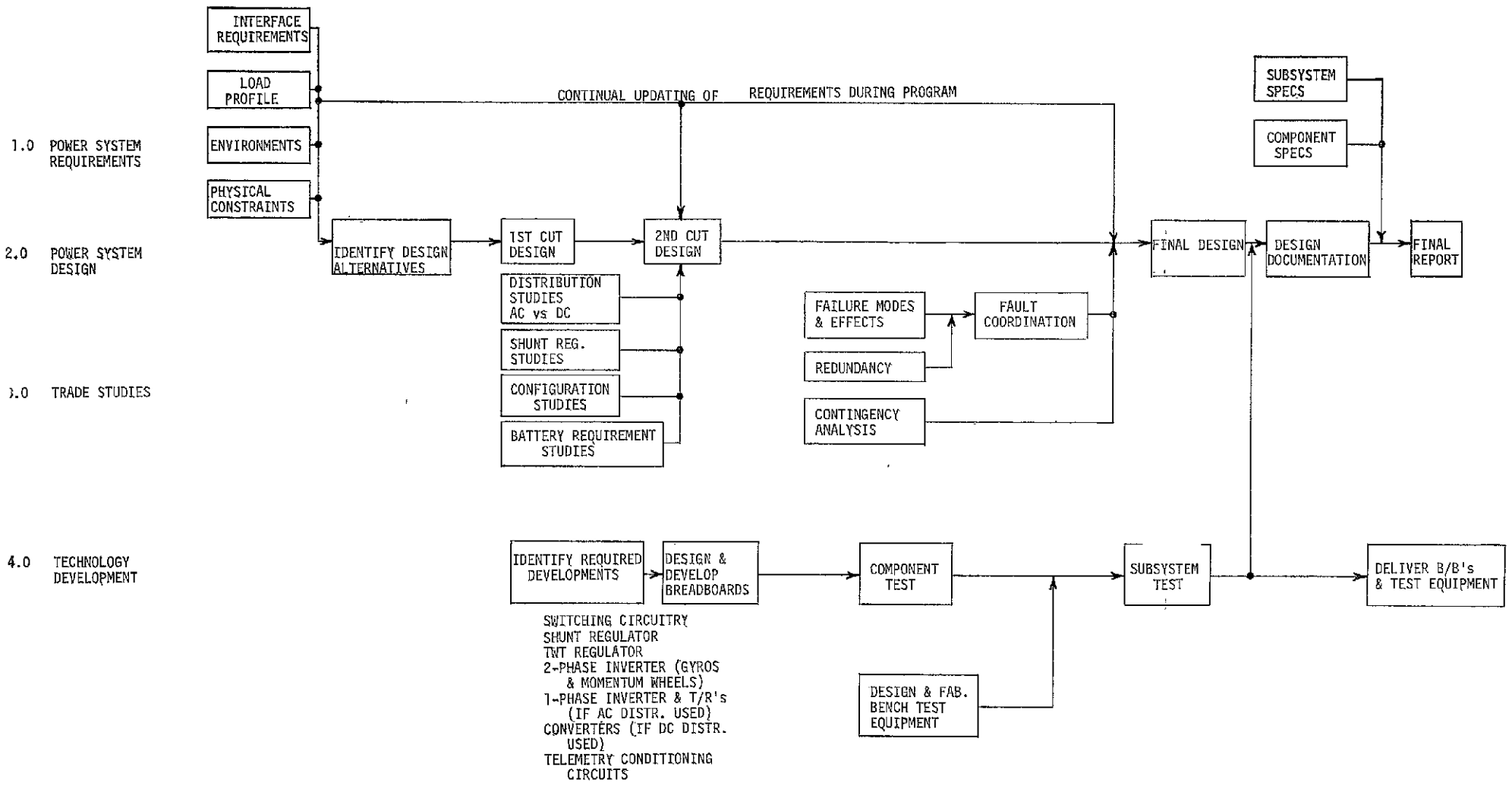

FIGURE 2-1 WORK FLOW DIAGRAM

FOLDOUT FRAME 1

FOLDOUT FRAME 2

- Main inverters and DC to DC converters shall be capable of free-running should the sync signal be lost.
- Weight and volume of the PCE shall be minimized.
- Power efficiency of the PCE, including inverters, converters, switches, etc., shall be maximized.
- Power consumption by the power switching control circuitry shall be minimized.
- Immunity to spurious switch operation shall be provided.
- The type approval temperature range shall be -20°C to +80°C as measured at the shear plate of the power bay.
- The regulation of the shunt regulator shall be traded off against the required regulation of the power supplies, and an optimization in terms of efficiency shall be reached.
- The nominal frequency of the two phase gyro inverter shall be between 1584 Hz and 1616 Hz. The frequency tolerance of this inverter shall be $\pm$ 0.01%. The frequency of the two phase momentum wheel inverter shall be 400 $\pm$ 5% Hz.
- If an AC distribution system is used, the frequency tolerance shall be $\pm$5%.
- Load requirements as a function of mission phase are summarized on Figure 3-1.

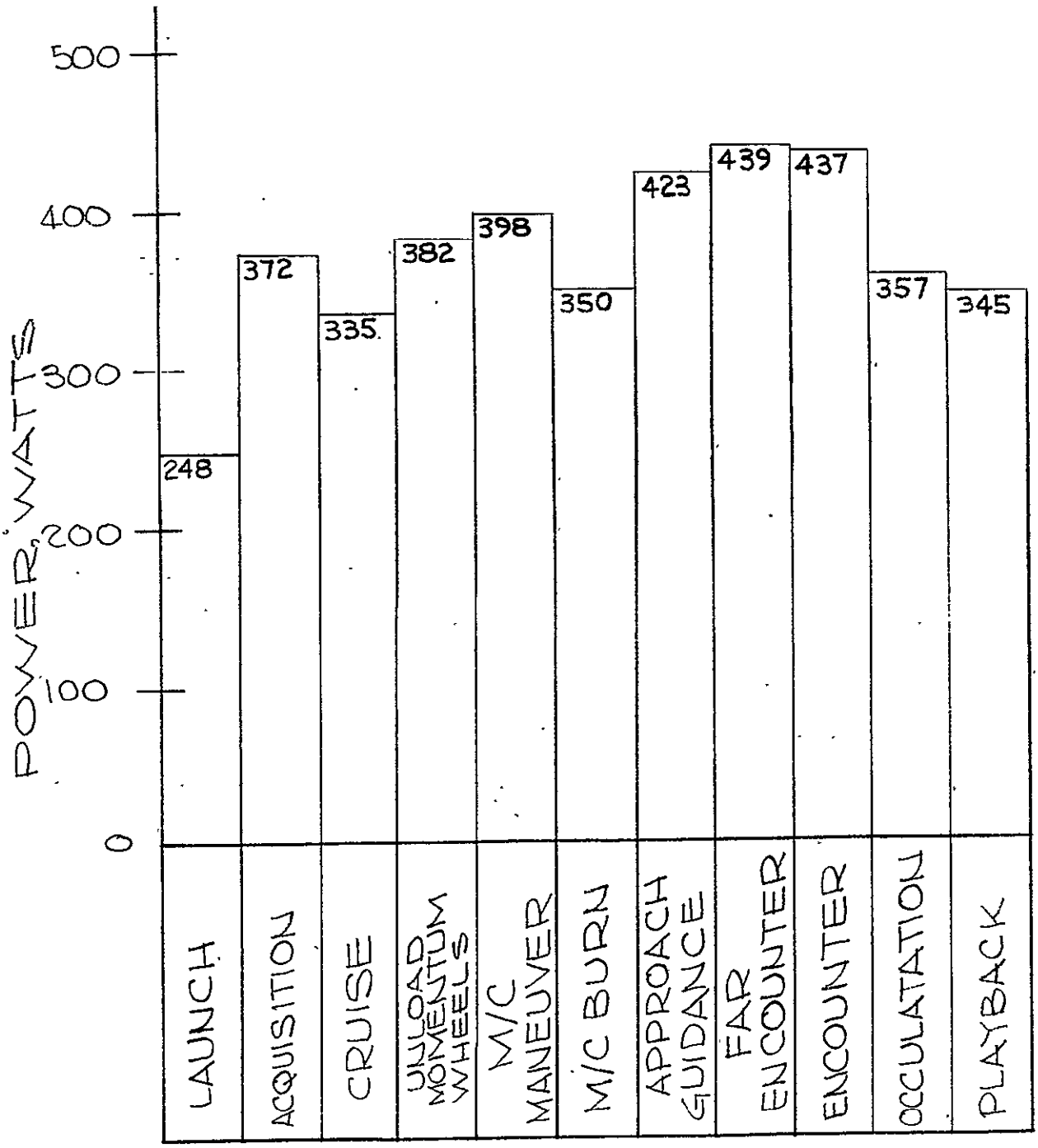

FIGURE 3-1. RTG POWER REQUIREMENTS

Task 2.0 Subsystem Design

2.1 System Description

Based on preliminary trade study indications, a tentative selection has been made of a DC distribution system. Its principal features are described below:

2.1.1 Electrical Configuration

A block diagram of the system is shown on Figure 3-2. Four RTG's are used, estimated to provide an initial output of 600 watts (150 watts each) and a conservative end of life power (after about 12 years) of 440 watts (110 watts each). The RTG outputs are combined through isolation diodes to a shunt regulated 30 VDC bus. The shunt regulator maintains constant load conditions on the RTG's and is of a quad redundant configuration permitting a short or open failure in any of its sections.

The regulated DC power is distributed to the various loads through current protection devices (which operate only as a result of load short failures) and power control switches. Converters, located at the loads, condition the power to the particular user voltage requirements. Individual converters may serve from one to several loads depending on functional and physical considerations.

The shunt regulator can dissipate only a portion of the largest amount of excess RTG power expected during the mission. Auxiliary loads operated by command or automatic on-off controls are used to absorb any excess power above that dissipated in the shunt regulator. These

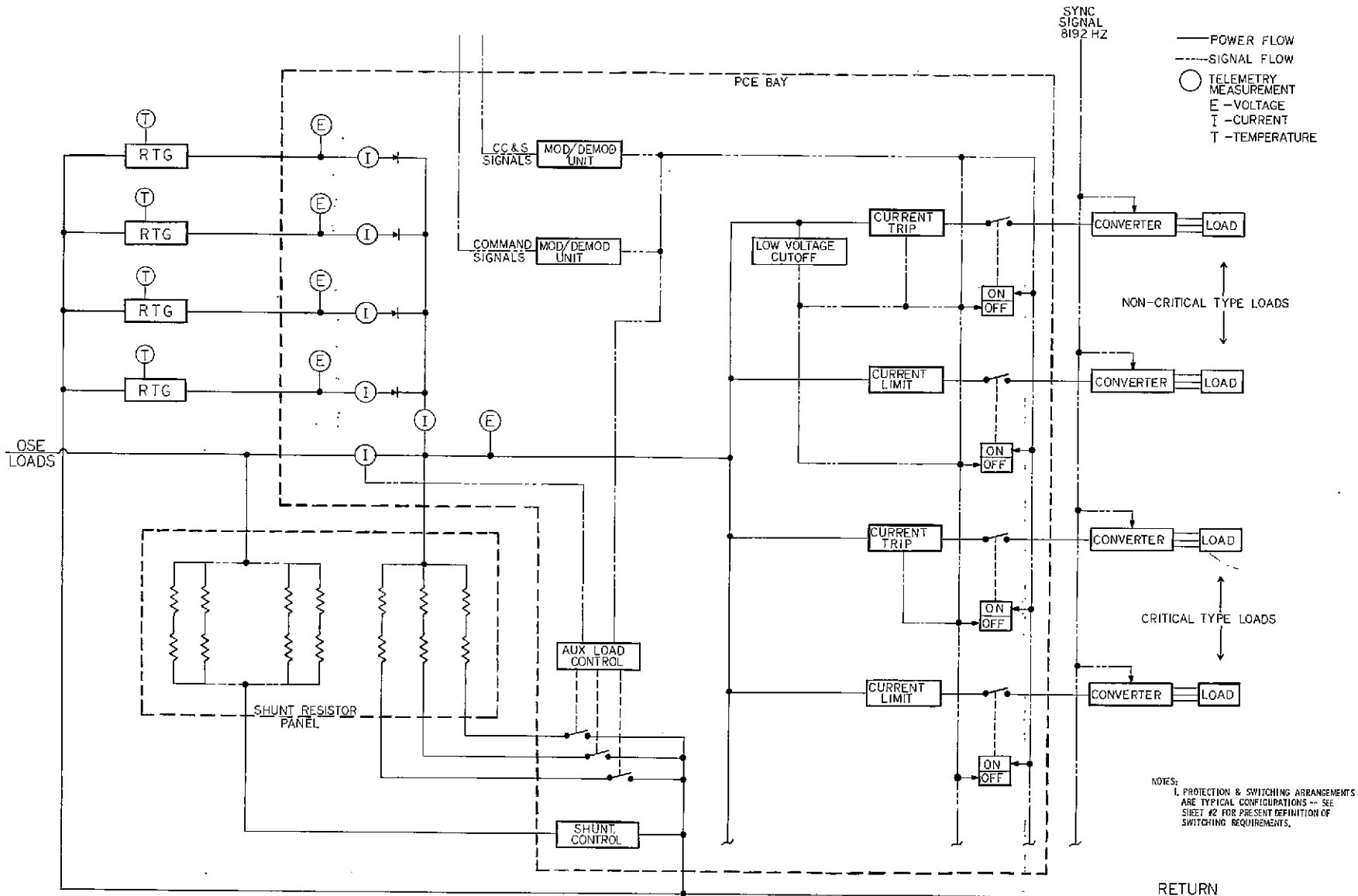

FIG. 3-2 TOPS POWER SYSTEM BLOCK DIAGRAM

SHEET NO.1

FOLDOUT FRAME 1

FOLDOUT FRAME 2

auxiliary loads will be active principally early in the mission when RTG output is highest.

Load management will be accomplished by control of the on-off switches at each load. The CC&S will be the principal source of signals controlling these switches in accordance with the mission sequence. A more thorough discussion of the load management concept using the CC&S is provided under Task 2.3.

Load faults and/or overload conditions are handled in several ways. First, if a specific load fails in short circuit, a current limiter on the input line limits the current to a preset level, or the overcurrent condition can be used to trip the control switch removing power from the load. Which of the two methods should be used for particular loads has not as yet been resolved. If a severe overload condition occurs, possibly as a result of a fault in a load that is not current limited, the system reacts through the initiation of a low voltage cutoff circuit. When the system voltage is depressed to some pre-established level, this circuit opens the control switches of designated non-critical loads. Power is sequentially reapplied to these loads by the CC&S. By comparing the change in shunt current as power is restored to each load with prestored data concerning each load, the CC&S can identify the load which has caused a failure and either bypass this load or substitute a standby unit.

Figure 3-2, Sheet 2, shows the latest definition of loads and assigned power control switches.

2.1.2 Physical Characteristics

Physically the power system consists of four RTG's, a single bay assembly containing the power conditioning equipment and a Shunt Resistor Panel (SRP), which contains the resistors of the shunt regulator and the auxiliary dissipation loads. DC to DC converters for the detailed conditioning of load power are considered to be part of the load subsystems. However, for comparing the system described here with other candidate configurations, the converters are included as part of the power system.

Figure 3-3 shows the physical breakdown of assemblies comprising the power system. Weight, size and volume estimates for the PCE, SRP and DC to DC converters are shown in Figure 3-4.

A preliminary thermal evaluation of the PCE bay assembly is shown on Figure 3-5. This evaluation is based on limiting the dissipation from the bay to 100 watts or less. As a result of discussions at JPL, it was determined that the bay thermal dissipation area will be about 225 square inches and can dissipate up to 50 watts for an average equipment temperature of 70°F. It was indicated that by utilizing other lateral regions on the equipment bay, it will be feasible to dissipate around 100 watts and still maintain equipment temperatures at 70°F. This is the basis for the thermal breakdown shown in Figure 3-5. With the 100 watt dissipation constraint, it is necessary to remove a large portion of the potential shunt

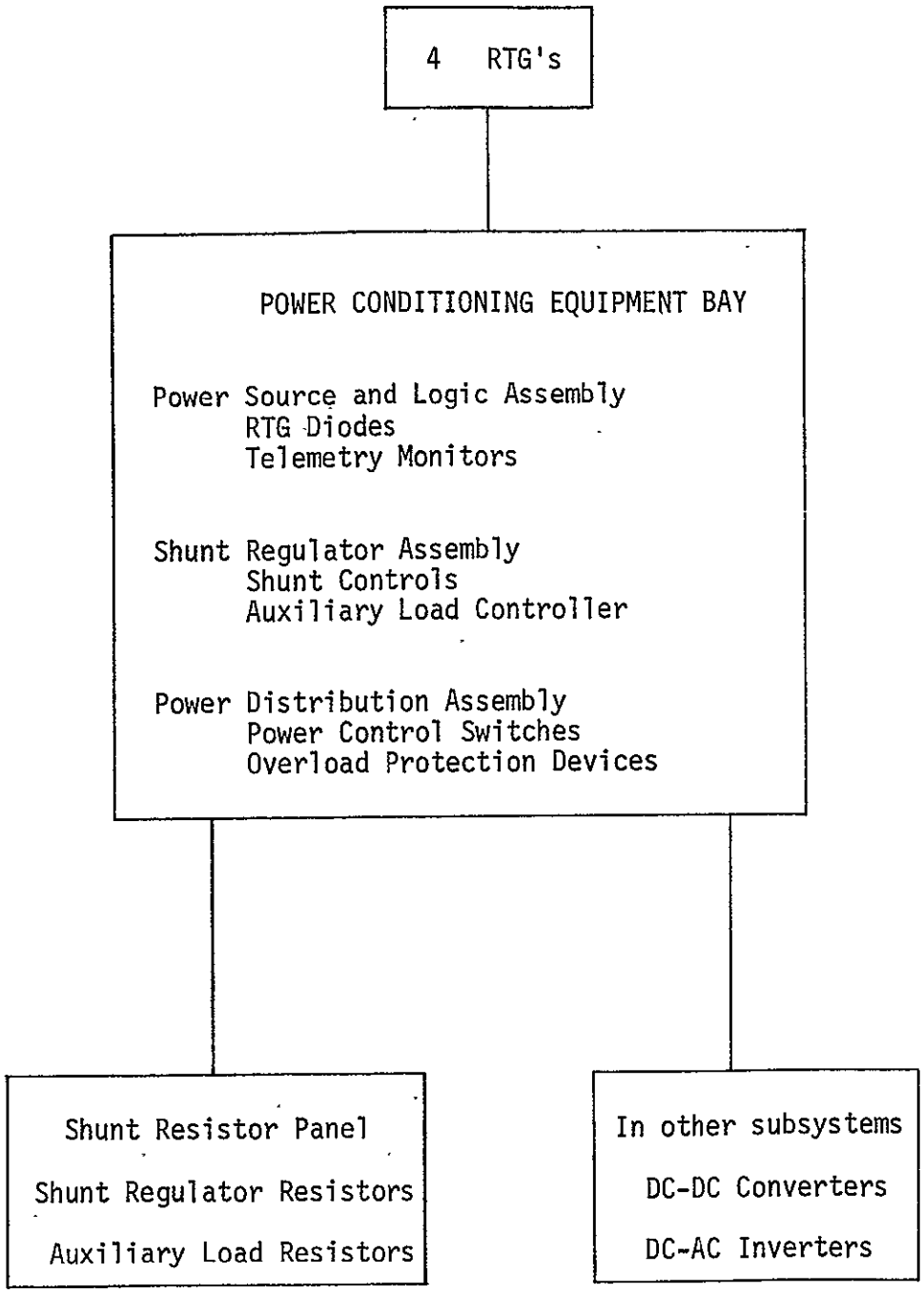

FIGURE 3-3 POWER SUBSYSTEM BREAKDOWN

	VOLUME, cu in.	WEIGHT, lbs.
PCE Bay Assembly		
Power Distribution Assembly	780	20.0
Shunt Regulator Assembly	220	3.5
Power Source and Logic Assembly	120	3.0
Chassis, wiring	220	5.5
Subtotal	1340	32.0
Shunt Resistor Panel Assembly	650 *	4.5
Subtotal	650	4.5
Conversion Equipment (In other subsystems)		
TWT Converter	200	6.5
Two-Phase Inverters (8)	480	14.0
All other converters (41)	1400	46.0
Subtotal	2080	66.5
TOTALS		
Without Conversion Equipment	1990	36.5
With Conversion Equipment	4070	103.0

* Required radiating area: 4.5 square feet

FIGURE 3-4 PHYSICAL CHARACTERISTICS SUMMARY

	Max Thermal Dissipation, Watts
Power Conditioning Equipment Bay	
Power Source and Logic	
Diodes	16
Telemetry Monitors	4
Shunt Regulator Assembly	
Transistors	40
Controls	negligible
Power Distribution Assembly	
Switches	40
Protection Devices	negligible
PCE Total	100
Shunt Resistor Panel	
Active Shunt Resistors	111
Auxiliary Loads	300
SRP Total	411

FIGURE 3-5 THERMAL STATUS

regulator dissipation to another location. This is done by locating the shunt resistor elements outside of the PCE bay - specifically on the Shunt Resistor Panel. Because of other fixed dissipation within the PCE bay, it is necessary to limit the shunt transistor dissipation to 40 watts. This maximum transistor dissipation occurs when the transistor voltage drop is equal to the resistor voltage drop, which at 15 volts and 40 watts is equivalent to a resistance of 5.625 ohms. When greater overall shunt dissipation is required, the transistor drop is decreased to a minimum of 5 volts, established by the particular shunt regulator design approach. At this point the respective transistor and resistor dissipations are 22 watts and 111 watts for a maximum total of 133 watts.

A rough survey of the load profile indicates that the load may be as low as 250 watts. With an RTG output of 600 watts, it would be necessary to dissipate 350 watts. Since the active shunt with this thermal constraint cannot handle more than 133 watts, auxiliary parasitic loads of about 220 watts are required. Allowing for some margin, three auxiliary loads of 100 watts each are tentatively selected. The resistors for these loads are located on the Shunt Resistor Panel (SRP) along with the active shunt resistors for a maximum dissipation capacity of 300 + 111 = 411 watts. Assuming an average panel temperature of 100°C and an emissivity of 0.9, the required panel area is 4.5 square feet, assuming radiation from only one panel surface.

2.1.3 Interfaces

Some preliminary interface considerations with the power system are discussed below:

A. Telemetry

The general concept for handling measurement data for telemetry purposes will be to condition all signals to a 0 to 5 volt analog signal corresponding to the measurement range. Signal source impedance will be 5000 ohms or less. Depending on the number of measurements, it is possible that they will be multiplexed and transmitted from the subsystem through a single coax cable as shown in Figure 3-6. This approach would also be used to route signals to and from the CC&S and command subsystems. If this concept is adopted, the required multiplexing and modulation/demodulation equipment would be supplied for inclusion in the PCE equipment bay. Table 3-1 is a preliminary breakdown of telemetry measurements.

B. Command

A preliminary breakdown of command requirements is shown on Table 3-2.

C. CC&S

Generally the CC&S interaction with the power system will be to control the power applied to the various loads. This control will depend on the particular mission sequence and the power margin status. As long as sufficient margin is available, operations can proceed according to planned sequences. If margins are insufficient,

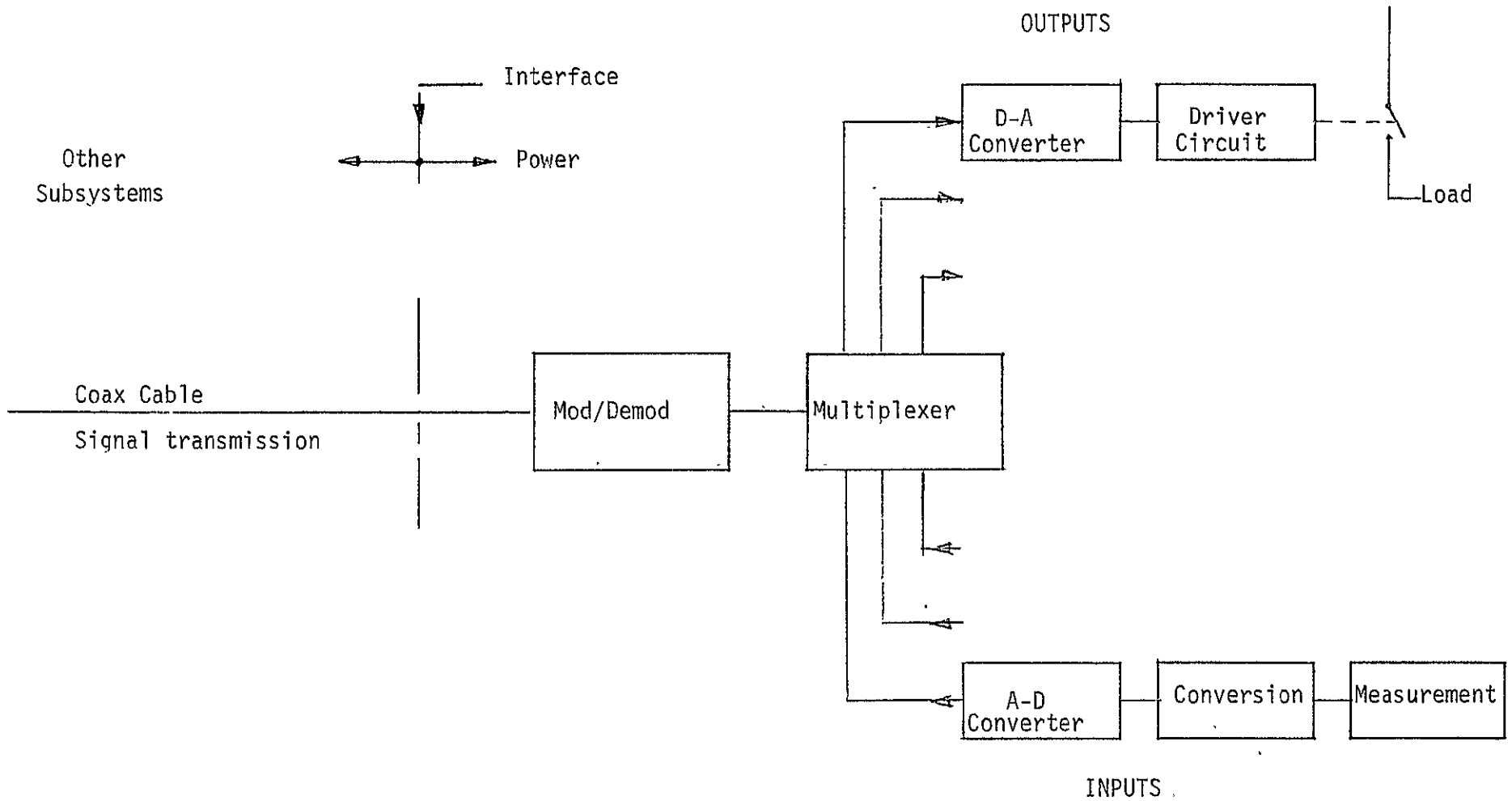

FIGURE 3-6 SIGNAL INTERFACE DIAGRAM

TABLE 3-1 TELEMETRY MEASUREMENTS

QUANTITY	MEASUREMENT	RANGE
4	RTG output voltage	0 to 60 volts
4	RTG output current	0 to 10 amperes
1	Shunt regulator current	0 to 5 amperes
1	Main bus current	0 to 20 amperes
1	Main bus voltage	27.5 to 32.5 volts
8	RTG temperature	Later
3	Auxiliary load switch on-off state	
80	User load switch on-off state	

TABLE 3-2 COMMAND REQUIREMENTS

QUANTITY	COMMAND FUNCTION
3	Turn on auxiliary loads
3	Turn off auxiliary loads
Later	Turn on user loads
Later	Turn off user loads

the CC&S, through stored instructions, withholds power according to some priority criterion. As presently visualized, status information for margin determination will be multiplexed and distributed in a manner similar to the telemetry information.

2.2 Operational Procedures

This section will concern test, ground checkout, flight operation, and associated equipment. There is no significant data to report at this time.

2.3 Load Management

This task will continually assess the margin status of the power system by comparing its capability against power requirements. The margin evaluation will take the following factors into account:

- Load profile information
- RTG time degradation
- Conditioning losses
- Contingency allowance
- Transient overshoot

Based on the latest information pertaining to these factors, Figure 3-7 shows the present estimate of margin status at the planet encounter times.

2.4 Reliability

Summary

Using a TOPS PCE reliability goal of 0.95, an apportionment was performed to allocate reliability objectives to the five major assemblies. Results of the apportionment are as follows:

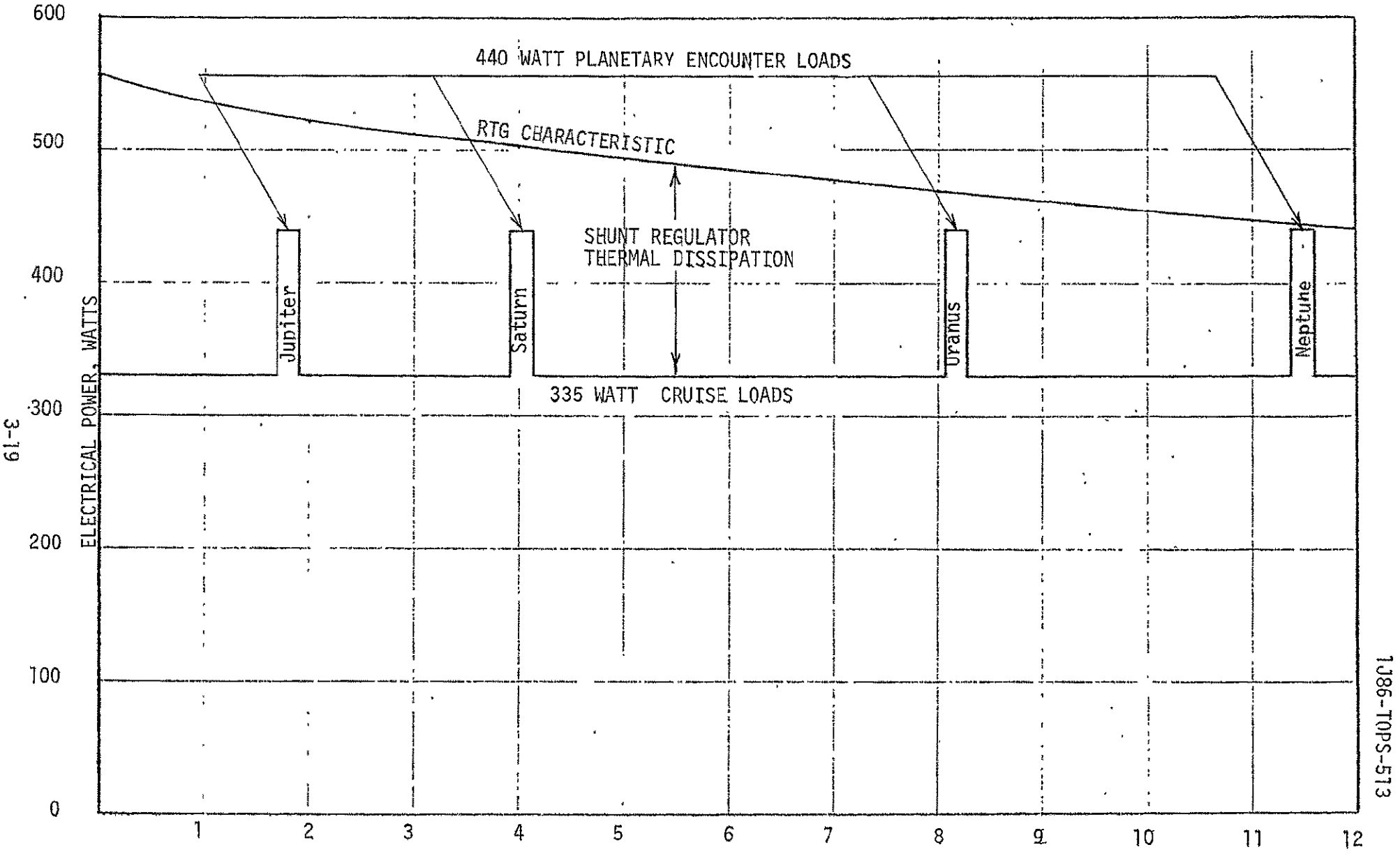

FIGURE 3-7 POWER MARGIN STATUS

TABLE 3-3 RELIABILITY APPORTIONMENT

ASSEMBLY	RELIABILITY OBJECTIVE
Power Source and Logic	.991
Shunt Regulator	.989
Main Inverter	.991
Power Distribution	.987
Two-Phase Inverter	.991

The above values will be updated when more detailed design definition of the assemblies permits a reevaluation of the factors used for computing the apportionment. The apportionment method is discussed in Appendix A.

Task 3. Trade Studies

The status of trade studies effecting system design selection is presented below:

3.1 Distribution Studies

This trade study concerns the question of whether AC or DC is the preferred form of power distribution. Results thus far favor the DC distribution option because of lower weight and higher efficiency. These differences arise principally from the additional stage of transformation required with the AC distribution method. There are additional factors to be studied before a final selection is made. These concern the following:

A. Redundancy

When the spacecraft loads are more firmly established, including the intended use of load redundancies, it will be possible to more accurately determine the number of converters that would be required for a DC distribution approach. Practical considerations of operating several loads from a common converter will be considered in establishing this number. Standby or functional redundancy will be taken into account where this approach is not practical. The AC distribution method will be similarly evaluated. From these more developed AC and DC distribution models, reliability, weight and efficiency factors will be reevaluated.

B. Design Flexibility

Probably the greatest merit of the AC distribution method lies in its insensitivity to load design changes, i.e., its flexibility in adapting to changed load requirements. The effect of user changes

are usually limited to the transformer/rectifier serving the particular user. With the DC distribution method, load changes will also generally affect only one converter. Since converters contain more circuitry than transformer-rectifiers, the effect of load changes may be more involved. In studying possible converter configurations for the TOPS-PCE, it is believed that the design can be modularized to use standard assemblies with the exception of the transformer and rectifier elements. Since these are the identical elements affected by changes in the AC system, it is believed that the standard module approach for DC to DC converters will permit changes to be accommodated with similar ease. These ideas are being evaluated presently.

3.2 Energy Storage Study

One of the guidelines used on TOPS is to design the spacecraft and mission sequences without dependence on battery energy storage. This is largely due to uncertainties in predicting battery performance over a 12 year period.

The purpose of this study task is to review constraints relative to battery requirements, develop power system designs with and without batteries, evaluate their impact on the spacecraft and mission design, and thereby determine whether the no-battery guideline is valid.

The study approach will be as follows:

Develop sufficient understanding of the mission to determine when and how battery power would be used.

Develop power system design concepts with and without batteries. Regarding battery design, analyze the range of possible configurations considering the number of series cells and ampere-hour sizes or reliability.

Compare the power system designs with and without batteries in terms of general physical and electrical characteristics and estimate their impact on mission capability.

Effort so far on this study has been principally devoted to Item C above concerning battery design. Battery reliability trades are discussed in Appendix B.

3.3 Bus Configuration Study

Several evaluations have been completed and others are underway concerning the bus configuration selection. A variety of RTG/bus arrangements are considered in Appendix C. The general conclusion is that a single bus configuration provides the most suitable arrangement. Appendix D considers the merits of RTG diode protection and indicates under what conditions the use of diodes is desirable.

The results of other subtasks are too preliminary other than to report their general objectives. Based on the single bus conclusion, a reliability study is proceeding to evaluate two basic single bus variations. One uses current limiting devices at all loads as a means of providing load fault protection; a second approach considers the use of only several current limit devices to assure the provision of power to the CC&S under load fault conditions.

3.4 Shunt Regulation Study

The purpose of this study is to determine the most effective means for accommodating the RTG's by assuring proper load conditions for the expected modes of operation. The name of the study results from the fact that linear shunt regulation appears to be the best method for providing the desired operating conditions. This conclusion is the result of comparing several methods as described in Appendix E.

The equipment bay constraints being considered for the TOPS-PCE will not allow the use of a fully integrated linear shunt regulator for the expected range of thermal dissipation.

This problem was discussed earlier under Task 2.1 and related to the maximum transistor dissipation that could be accommodated within the equipment bay. For long-life goals it is desirable to locate transistors within a temperature controlled region. Resistors are not as critical in this regard and therefore the approach is to accommodate resistor dissipation on a separate environmentally exposed panel, thereby reducing the thermal burden on the PCE bay. In spite of this alleviation, the transistor dissipation would still be excessive. For this reason it was necessary to reduce the active shunt capability and add auxiliary loads to maintain the overall system dissipation capability. The auxiliary load resistors would also be located on an exposed panel and would be controlled by switches located in the PCE bay. Since such switches (solid state or relay types) are either fully on or off, they dissipate negligible power.

The auxiliary load approach requires some control method for determining when the auxiliary loads should be applied or removed. It may be possible to implement this control by ground command or, knowing the load profile and RTG performance in advance, it may be feasible to program these loads with the CC&S. An alternative method of control may be to switch in each auxiliary load at discrete levels within the band of main bus voltage regulation. At the highest

error level all auxiliary loads would be switched in with the active shunt load also near its highest value. As the voltage decreases because of higher power demands, the active shunt is gradually unloaded. At some discrete level, one of the auxiliary loads is abruptly interrupted and the active shunt readjusts to absorb this incremented power. As the voltage decreases further because of higher demands, the active shunt is again gradually unloaded, the second auxiliary load is interrupted, and so on through the additional auxiliary loads. Some deadband will be required to avoid instabilities that might result with turning the auxiliary loads on or off.

Circuit concepts and general system implications of the above possibilities will be examined in this coming period.

Appendix F presents some supporting data on the thermal performance of shunt regulator elements.

Task 4.0 Technology Development

The following sections report on the status of technology developments undertaken thus far in the program. For the most part these developments concern circuit designs for the various power conditioning elements. These designs are being perfected to a breadboard demonstration stage. Together with the system definition activity, this technology development effort will serve to define PCE hardware requirements in a later phase of the TOPS program.

To provide some perspective, the technology developments are discussed as they relate to each functional block of the PCE. Thus, switch

developments are discussed as part of the Power Distribution Assembly since the majority of these switches will be contained in that assembly. A summary of the presently defined function and design approach for each functional block precedes the technology status discussion.

4.1 Power Distribution Assembly

Function

- Houses power control switching devices
- Number of switching circuits: 90
- Type power:

  (typical) 30 VDC
  50 VAC, 4096 Hz

- Switch ratings: up to 5 amperes
- Control signal: 5 VDC, Transistor-Transistor Logic (TTL)
  30 millisecond pulse
- Protective features: Current limit
  Current trip
- Transient suppression: Ramp-on and
  Ramp-off features

Approach

- Analyze AC and DC switching circuitry features:

  Redundancy

  Ramp turn-on

  Ramp turn-off

  Overcurrent limit

  Overcurrent trip

- Build, test and deliver:
  - A quad relay switch, applicable to AC and DC distribution, with an overcurrent trip on DC only.
  - A quad semiconductor switch, applicable to DC only, with an overcurrent trip, and an isolated light driver.
  - An AC static switch, current limited, foldback or overcurrent trip, with both saturable reactor and silicon controlled rectifier as candidates in a fifty volt RMS system.

Status

- Requirements for toggle command have been deleted.
- Quad relay and semiconductor switches with overcurrent protection for use with DC power were built and successfully tested. Results are discussed in Appendix G.
- A saturable reactor AC static switch with current limiting was breadboarded and will be tested.

4.2 Shunt Regulator Assembly

Function

- Maintains constant RTG operating conditions by regulating voltage and absorbing excess power.
- Regulation: 30 VDC $\pm$ 1%
- Excess power: 350 watts
- Losses (with no shunting): 0.5 watts
- Dynamic impedance: 0.1 ohms (0 to 1 MHz)
- Transient response: Recover to within regulation in one millisecond for a step load change of 270 watts.

Approach

- Develop and test a breadboard shunt regulator with emphasis on quad redundancy features i.e., a design that can accept either a short or open of any single part.

- The quad shunt regulator built in the previous quarter was completely tested. The results of this testing are reported in Appendix H.

4.3 TWT Converter

Function

- Provides DC to DC conversion of electrical power to satisfy traveling wave tube requirements.
- Input voltage: 30 VDC ± 1%
- Output voltage

  Helix: 3400 to 3500 VDC, settable within 0.2%; regulation ± 0.5%; ripple 1.0 volt peak to peak.

  Collector: 1425 to 1525 VDC, settable within 0.5%; regulation ±1.0%; ripple 2.0 volts peak to peak.

  Anode: 100 to 400 VDC, settable within 5.0 volts; regulation ±1.0%; ripple 1.0 volt peak to peak.

  Filament: 5.0 to 5.5 volts rms, settable within 0.1 volts; regulation ± 3.0%.

- Current

  Helix: 2 to 5 milliamperes

  Collector: 43 to 48 milliamperes

  Anode: 0.2 milliamperes

  Filament: 220 milliamperes with a 400 milliampere limit

- Operation required through atmospheric pressure decrease.

Approach

- Develop and test a breadboard unit with emphasis on transformer design and fabrication techniques and the high voltage series regulator.

Status

- Circuit designs were developed for the TWT converter as described in Appendix I.
- Seven transformer configurations have been built and tested with varying degrees of success. Latest version shows satisfactory operation though efficiency is low (70% against a goal of 90% for the overall supply).
- Two series regulator circuits have been built and tested. Improvements in converter filter characteristics are required to attenuate the input ripple to the series regulators.

4.4 Two-Phase Inverters

Function

- Provides two phase DC to AC conversion for gyros and momentum flywheels.
- Requirements

	GYROS	WHEELS
Power rating, continuous	12 watts	11 watts
Power rating, peak	20 watts	11 watts
Frequency	1600 Hz	400 Hz
Electrical configuration	3 wire	4 wire
Command logic	5 v. TTL	5 v. TTL
Phase reversal	No	Yes
Inhibit override	None	200 ms pulses
Free run	Yes	Yes
Output isolation	Yes	Not required
Output voltage	26 VAC±5%	26 VAC±5%
Free run frequency	1600 Hz+0, -2%	400 Hz ±5%
Frequency stability	±0.5%	Not required

Approach

- Develop, test and deliver breadboard inverters (1 each for gyros and momentum wheels)

Status

- A breadboard unit was built and tested to the requirements defined early in the program. No unique technology problems were identified. New designs will be developed and built to the requirements described above.

  A discussion of alternative AC motor drive circuits is presented in Appendix J.

4.5 AC Power Conditioners

Function

- Two steps are involved:
  (1) Invert power from regulated DC to AC for general distribution to the loads.
  (2) At each load, transform and rectify to multiple voltage levels.
- Inverter input voltage: 30 VDC $\pm$ 1%
- Inverter output voltage: tentatively at 50 volts rms, square wave, 8192 Hz
- Inverter to free run with loss of timing signal.

Approach

- Build and test one inverter and three transformer-rectifiers for purposes of comparing weight, efficiency and electrical performance with the DC to DC converters. Inverter and transformer-rectifiers are to furnish the loads listed in Table 3-4.

Status

- No activity to report.

TABLE 3-4

AC POWER CONDITIONING REQUIREMENTS

INVERTER	TRANSFORMER-RECTIFIER	OUTPUT VOLTAGE	PERCENT REGULATION	POWER WATTS
Input Voltage: 30 VDC ±1% Output Voltage: 50 VAC RMS ±2% square wave Output Power: 6 watts minimum 60 watts maximum Output Frequency: 8192 Hertz ±5%	No. 1 Science Data Subsystem	+5 +15 -15	±10 ±5 ±5	15.75 1.5 1.5
	No. 2 DC Magnetometer Experiment	+8 -8 +12 -12 +25 -25 +5	±1 ±1 ±1 ±1 ±.01 ±.01 ±5	.4 .4 .4 .4 .2 .2 .3
	No. 3 Tracking Receiver	+6 -6 +15 -15	±2	2.0

4.6 DC Power Conditioners

Function

- Convert from regulated 30 VDC to user voltage levels.
- Separate converters to be used at each load or functional load group.
- All switching frequencies to be synchronized by single clock signal.
- Converters to free run with loss of timing signal.

Approach

- Build and test three converters for comparison of weight, efficiency, and electrical performance with inverters and transformer-rectifiers. Loads are to be as shown for Task 4.5.

Status

- The electronic portion of the converter has been packaged using thick film microcircuitry techniques. Three such "flat pack" units have been built and functional tests were performed demonstrating feasibility. Some of the current paths must be reconfigured to reduce resistance.
- No further effort will be expended on the flat-pack technology. The three converters for comparison with inverters and transformer-rectifiers will be built using discrete piece part packaging methods.
- Design factors to be considered for DC to DC converters are discussed in Appendix K.

4.7 Power Source and Logic

Function

- Houses RTG isolation diodes, telemetry conditioning circuitry, and fault detection circuitry.

Approach

- Design and build breadboards of unique circuit elements, such as voltage monitors, current monitors, and fault detection circuits.

Status

- No activity has been initiated.

4.8 Subsystem Tests

These tests will be conducted to demonstrate the power system design concept using the breadboard assemblies of specific components. No activity has been initiated on this task.

4.9 Bench Test Equipment

This equipment will be built and used in conjunction with the subsystem tests (Task 4.8). No activity has been initiated on this task.

4.10 Advanced Circuit Development

Specific activity relating to this task is reported under Task 4.6 covering thick film microcircuitry packaging methods.

SECTION 4. PLANNED FOLLOW-ON ACTIVITIES

Scheduled tasks activities for the coming quarter are shown on Figure 4-1. The planned activities are described below:

Task	Activity
1.0 Subsystem Requirements	Sustaining effort for updating load profiles and interface requirements.
2.0 Subsystem Design	
2.1 System Description	Provide updated descriptions of AC and DC power system versions.
2.2 Operational procedures	Provide first cut description of ground, launch and flight operations including ground equipment identification.
2.3 Load Management	Update margin assessment using latest RTG output information, load profiles and conversion efficiencies based on test data, if available.
2.4 Reliability	Calculate reliability vs mission time for the preferred design.
3.0 Trade Studies	
3.1 Distribution Studies	Complete AC vs DC trade by comparing weight, power and reliability.
3.2 Energy Storage Study	Compare systems with and without batteries for the ascent and encounter phases. Consider separately the need for batteries if no RTG power is available during launch.

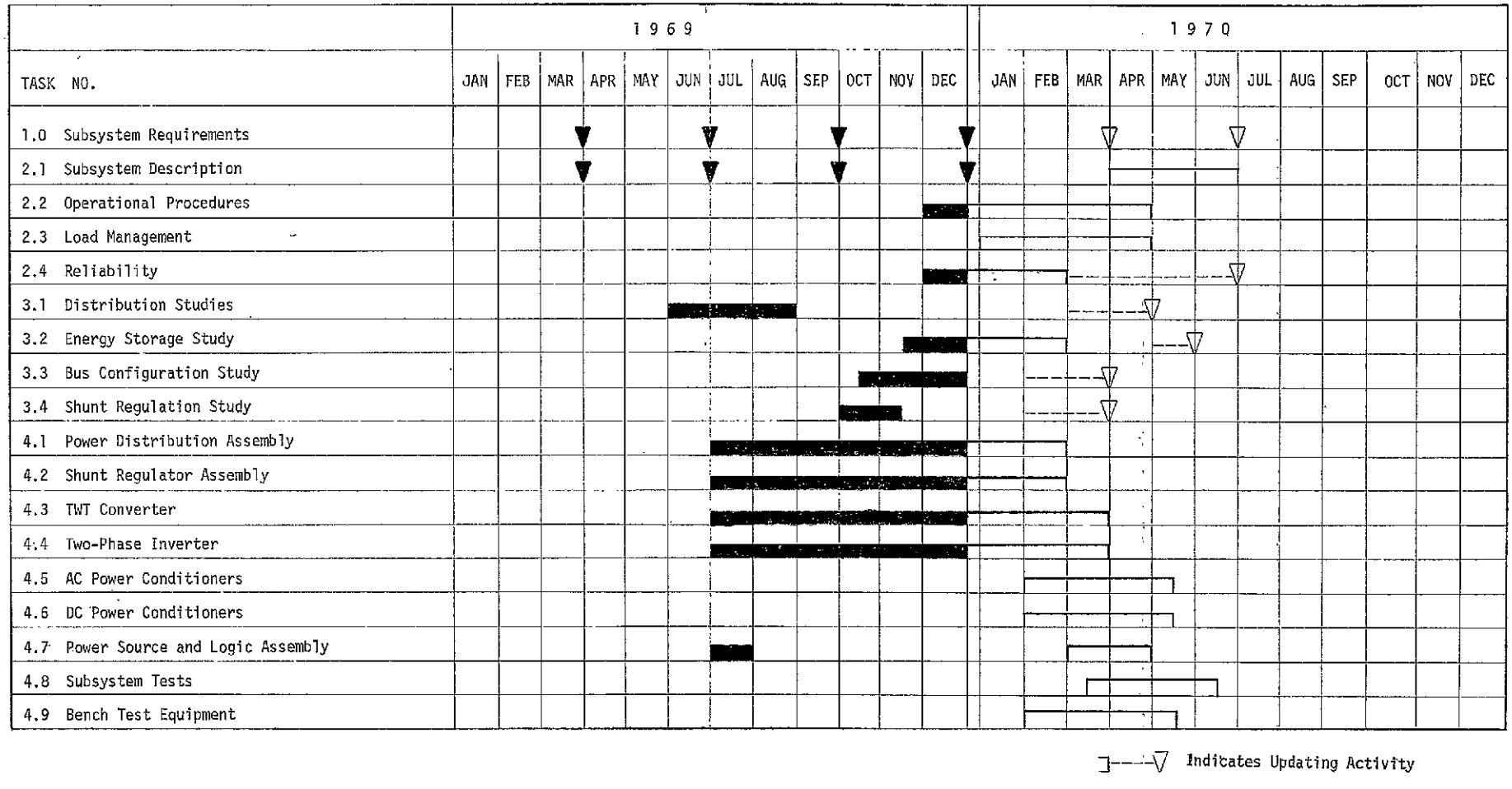

FIGURE 4-1 SCHEDULE OF KEY TASKS

FOLDOUT FRAME

FOLDOUT FRAME 2

Task	Activity
3.3 Bus Configuration	Make final selection and provide supporting trade study data.
3.4 Shunt Regulator Study	Define the logic and operational requirements for auxiliary load implementation.
4.0 Technology Development	
4.1 Power Distribution Assembly	Complete breadboard demonstration of AC static switch.
4.2 Shunt Regulator Assembly	Complete ECAP response analysis.
4.3 TWT Converter	Complete the converter breadboard.
4.4 Two-Phase Inverter	Build a second breadboard and modify the first breadboard.
4.5 AC Power Conditioners	No activity planned.
4.6 DC Power Conditioners	Fabricate and test 3 converters.
4.7 Power Source and Logic Assembly	Design and test typical telemetry circuits.
4.8 Subsystem Tests	No activity planned.
4.9 Bench Test Equipment	Generate parts list and order parts.

5.0 CONCLUSIONS

The early phases of this program have been mostly concerned with developing circuits and devices to meet the extended life requirement of the TOPS mission. Concerning this aspect of the program, the principal conclusions are:

- No severe technological problems associated with extended life capability have been encountered.
- The design of a high voltage transformer for the TWT converter has proven to be difficult. Some degree of success has been reached and further work is proceeding.
- Circuit redundancy techniques are practical and have been successfully applied to solid-state and relay switching devices, and the shunt regulator.

Greater emphasis is presently being placed on system studies for defining the power system. A number of specific studies are in process. Preliminary findings are as follows:

- As a result of recent briefings on the RTG status, it is possible that power will not be available or may be severely limited during the launch phase.
- The range of required shunt heat dissipation appears large and may necessitate that the dissipation elements be located on surfaces external to the equipment bay.

SECTION 6 NEW TECHNOLOGY

No items of new technology have been identified during the period covered by this report.

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APPENDIX A. RELIABILITY APPORTIONMENT METHOD

The method used for apportioning the PCE reliability goal is based on the two major considerations of the relative importance of each assembly in performing the PCE function, and the relative potential operational reliability of each assembly. For the first of these it is desirable that the assemblies having a more important role in accomplishing the PCE function be allocated higher reliability goals. Similarly, for the second consideration, the assemblies capable of providing higher reliability due to inherent design characteristics and operational conditions should be assigned higher reliability goals.

A functional block diagram of the PCE is shown in Figure A-1. The factors selected to represent the apportionment as discussed above and the values assigned for each assembly are shown in Table A-1.

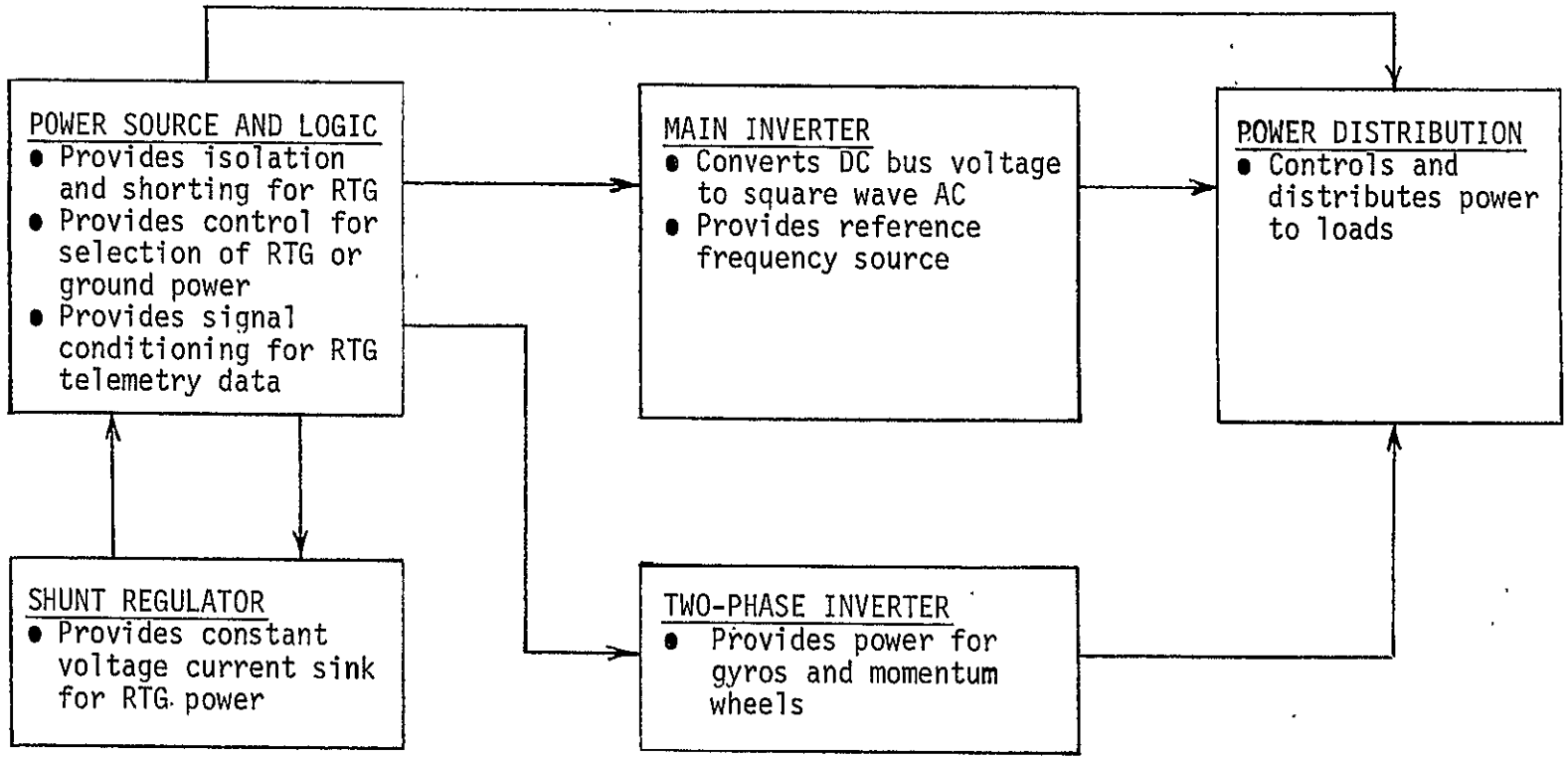


FIGURE A-1
TOPS-PCE FUNCTIONAL BLOCK DIAGRAM

TABLE A-1 TOPS-PCE APPORTIONMENT FACTORS

ASSEMBLY	IMPORTANCE FACTORS		RELIABILITY FACTORS	
	INTERACTION FACTOR	NUMBER OF FUNCTIONS	RELATIVE COMPLEXITY	DUTY CYCLE
POWER SOURCE AND LOGIC	5	3	.50	1.00
SHUNT REGULATOR	2	1	.10	1.00
MAIN INVERTER	2	2	.20	1.00
POWER DISTRIBUTION	1	1	1.00	.01
TWO-PHASE INVERTER	2	1	.40	.20

The interaction factor is a measure of the degree to which each assembly affects the performance of other assemblies and is obtained from Figure A-1. The interaction factor for each assembly is the total number of assemblies directly dependent on it for operation, including itself, and is computed as the number of arrows leaving the assembly, plus one.

The number of functions performed by each assembly is as shown on Figure A-1.

The complexity factor is a gross estimate of the relative complexity of each assembly on a scale of 1.0 for the most complex.

The duty cycle factor is the estimated fraction of time that the assembly is expected to operate during the mission, using a scale of 1.0 for full time operation.

Two basic models were considered for computing the apportionment. In one model the apportionment factors are added for computing weighting factors, and in the other model they are multiplied. The latter approach tends to provide a greater dispersion in the apportioned values. The PCE apportionment was performed using both methods with the objective of selecting the more suitable one.

The general model used for computing the apportionment is as follows:

$$Ri = Rs\left(\frac{1}{2Wi} + \frac{Xi}{2} \right)$$

where:

Ri = Reliability apportionment for the "i^{th}" assembly

Rs = TOPS-PCE System Reliability goal, 0.95.

Wi = Importance weighting factors for assembly "i".

Xi = Reliability weighting factors for assembly "i".

	ADDITIVE MODEL	MULTIPLICATIVE MODEL
Wi =	$(F_1 + F_2)\ i \quad \sum_1 \left[\frac{1}{(F_1 + F_2)}\right]\ i$	$(F_1 \times F_2)\ i \quad \sum_1 \left[\frac{1}{(F_1 \times F_2)}\right]$
Xi =	$\frac{(F_4 + F_5)\ i}{\sum_1 (F_4 + F_5)\ i}$	$\frac{(F_4 \times F_5)}{\sum_1 (F_4 \times F_5)\ i}$

And:

F_1 = Value of the interaction factor

F_2 = Value of the number of functions factor

F_3 = Value of the complexity factor

F_4 = Value of the duty cycle factor

For performing the computations, the importance factors were normalized to show the highest value as 1.0 and the remaining values were scaled proportionally. The reliability factors were already scaled in this manner. The overall effect of this scaling is to give equal weight to each of the factors when used in the additive model.

The apportionment results are shown in Table A-2 for the additive model and in Table A-3 for the multiplication model.

For analyzing the results of the two methods it is useful to compare the "probability of failure" values (1 - Reliability), as follows:

	PROBABILITY OF FAILURE			
ASSEMBLY	ADDITION METHOD	MULTIPLICATION METHOD	DIFFERENCE	% CHANGE
Power Source and Logic	.0092	.0150	+.0058	+63
Shunt Regulator	.0109	.0084	-.0025	-23
Main Inverter	.0094	.0085	-.0009	-10
Power Distribution	.0127	.0113	-.0014	-11
Two-Phase Inverter	.0086	.0078	-.0008	- 9

The major differences are a higher apportioned reliability for the Shunt Regulator, and a lower value for the Power Source and Logic, when the multiplication method is used. The maximum difference, however, (.0058) is less than 12% of the total allowable unreliability (.0058/.05 = .116) and therefore there is little value in seeking justification for preferring one method to the other.

The results using the addition model will, therefore, be used since this method offers the additional flexibility of weighting the individual factors if this becomes desirable.

TABLE A-2 ADDITION MODEL RELIABILITY APPORTIONMENT

ASSEMBLY	IMPORTANCE FACTORS				RELIABILITY FACTORS				R Apportioned Reliability
	F_1 Interaction Factor	F_2 Number of Functions	F_1+F_2 Sum of Factors	W Relative Weight	F_4 Complexity Factor	F_5 Duty Cycle	F_4+F_5 Sum of Factors	X Relative Weight	
A. Power Source and Logic	1.00	1.00	2.00	12.122	.50	1.00	1.50	.277	.9908
B. Shunt Regulator	.40	.33	.73	4.425	.10	1.00	1.10	.203	.9891
C. Main Inverter	.40	.67	1.07	6.485	.20	1.00	1.20	.222	.9906
D. Power Distribution	.20	.33	.53	3.212	1.00	.01	1.01	.187	.9873
E. Two-Phase Inverter	.40	.33	.73	4.425	.40	.20	.60	.111	.9914

$$Ri = .95^{\left[\frac{1}{2W_i} + \frac{Xi}{2}\right]}$$

$$Wi = (F_1 + F_2)i \quad \sum_i \left[\frac{1}{(F_1 + F_2)}\right]$$

$$Xi = \frac{(F_4 + F_5)i}{\sum_i (F_4 + F_5)\, i}$$

TABLE A-3 MULTIPLICATION MODEL RELIABILITY APPORTIONMENT

ASSEMBLY	IMPORTANCE FACTORS				RELIABILITY FACTORS				R
	F_1 Interaction Factor	F_2 Number of Functions	$F_1 \times F_2$ Product of Factors	W Relative Weight	F_4 Complexity Factor	F_5 Duty Cycle	$F_4 \times F_5$ Product of Factors	X Relative Weight	Apportioned Reliability
A. Power Source and Logic	1.00	1.00	1.00	35.0344	.50	1.00	.50	.5618	.9850
B. Shunt Regulator	.40	.33	.132	4.6245	.10	1.00	.10	.1124	.9916
C. Main Inverter	.40	.67	.268	9.3891	.20	1.00	.20	.2247	.9915
D. Power Distribution	.20	.33	.066	2.3122	1.00	.01	.01	.0112	.9887
E. Two-Phase Inverter	.40	.33	.132	4.6245	.40	.20	.08	.0899	.9922

$$Ri = .95 \left[\frac{1}{2Wi} + \frac{Xi}{2}\right]$$

$$Wi = (F_1 \times F_2)i \quad \sum_i \left[\frac{1}{(F_1 \times F_2)}\right]i$$

$$Xi = \frac{(F_4 \times F_5)\ i}{\sum_i (F_4 \times F_5)\ i}$$

APPENDIX B PRELIMINARY RELIABILITY ASSESSMENT FOR NICKEL CADMIUM BATTERIES

Reliability data for aerospace battery systems for a time period of 12 years is not available, but a preliminary assessment has been made based on published cell failure rates for one to six years, and extrapolated to 12 years (see Figure B-1). The resulting reliability numbers may be optimistic, but provide a basis for further study and point out the advantages of reducing the number of series cells in a battery. The "high voltage divergence" failure mode shown on Figure B-1 was not considered in the analysis since it was assumed that the low rate battery charging used in this type of application would not lead to this problem. The other three failure modes shown on Figure B-1 were summed up to produce Figure B-2. In this analysis it is assumed that the failure of any one cell by any of the failure modes is a failure of the battery.

Figures B-3, B-4 and B-5 are the calculated results using only the failure rates from Figure B-2. For a 12 year requirement, it is of interest to see the great impact of the number of cells in series. The curves indicating 2, 4 and 8 batteries were calculated on the basis that one battery is required and all additional batteries are redundant. The 9 year and 6 year reliability calculations were made primarily to derive the curves in Figure B-6 to show the decreasing reliability with life requirement. The curves of Figure B-6 for two 4-cell batteries and two 20-cell batteries are cross plots from Figures B-3, B-4 and B-5; and any other combination of series cells and redundant batteries can be plotted similarly. One of the questions raised by this analysis is, "What is an acceptable reliability for a 12 year mission?"

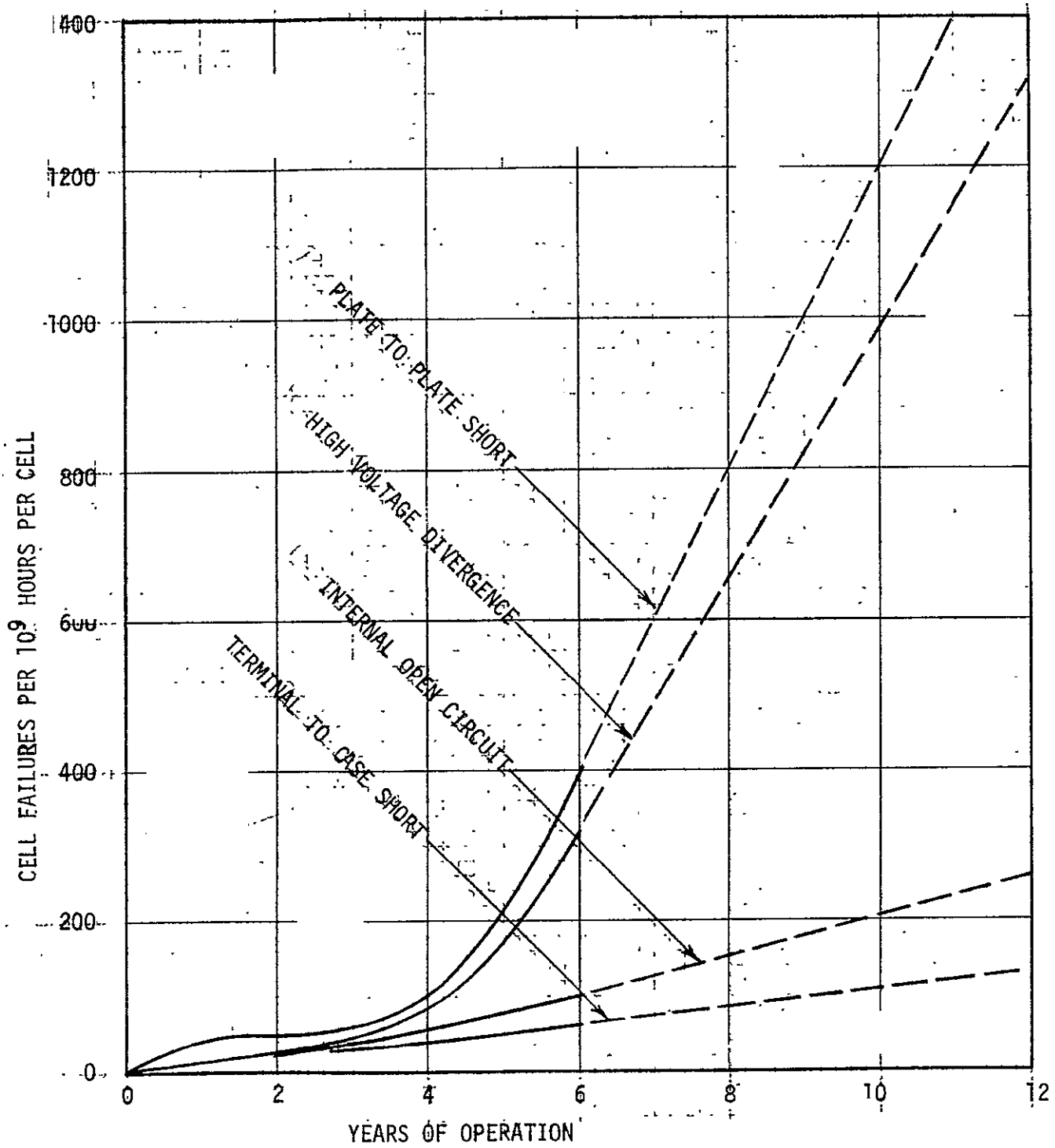


FIGURE B-1 –CELL FAILURES DUE TO SEPARATE CAUSES

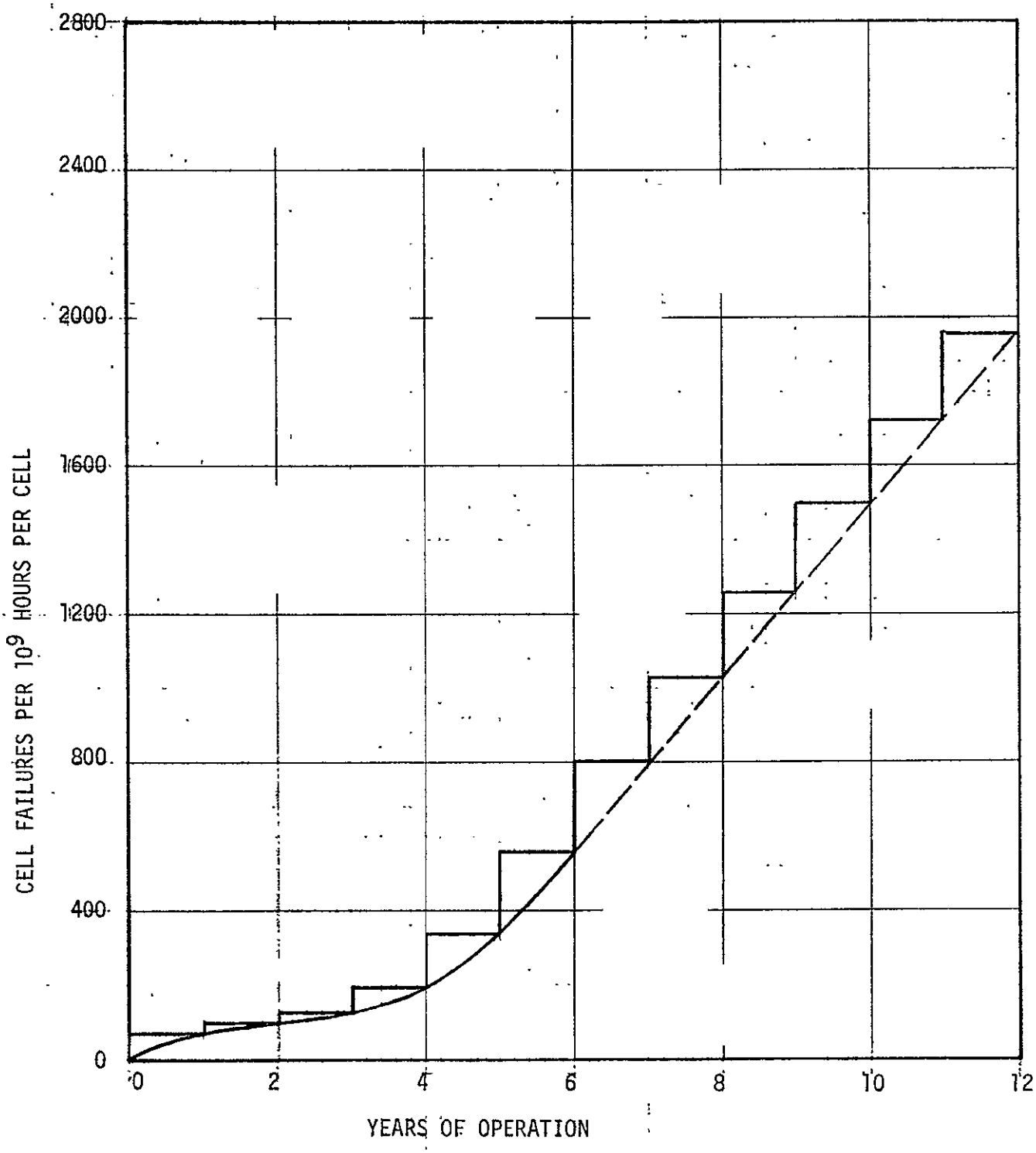


FIGURE B-2. CUMULATIVE CELL FAILURE RATES

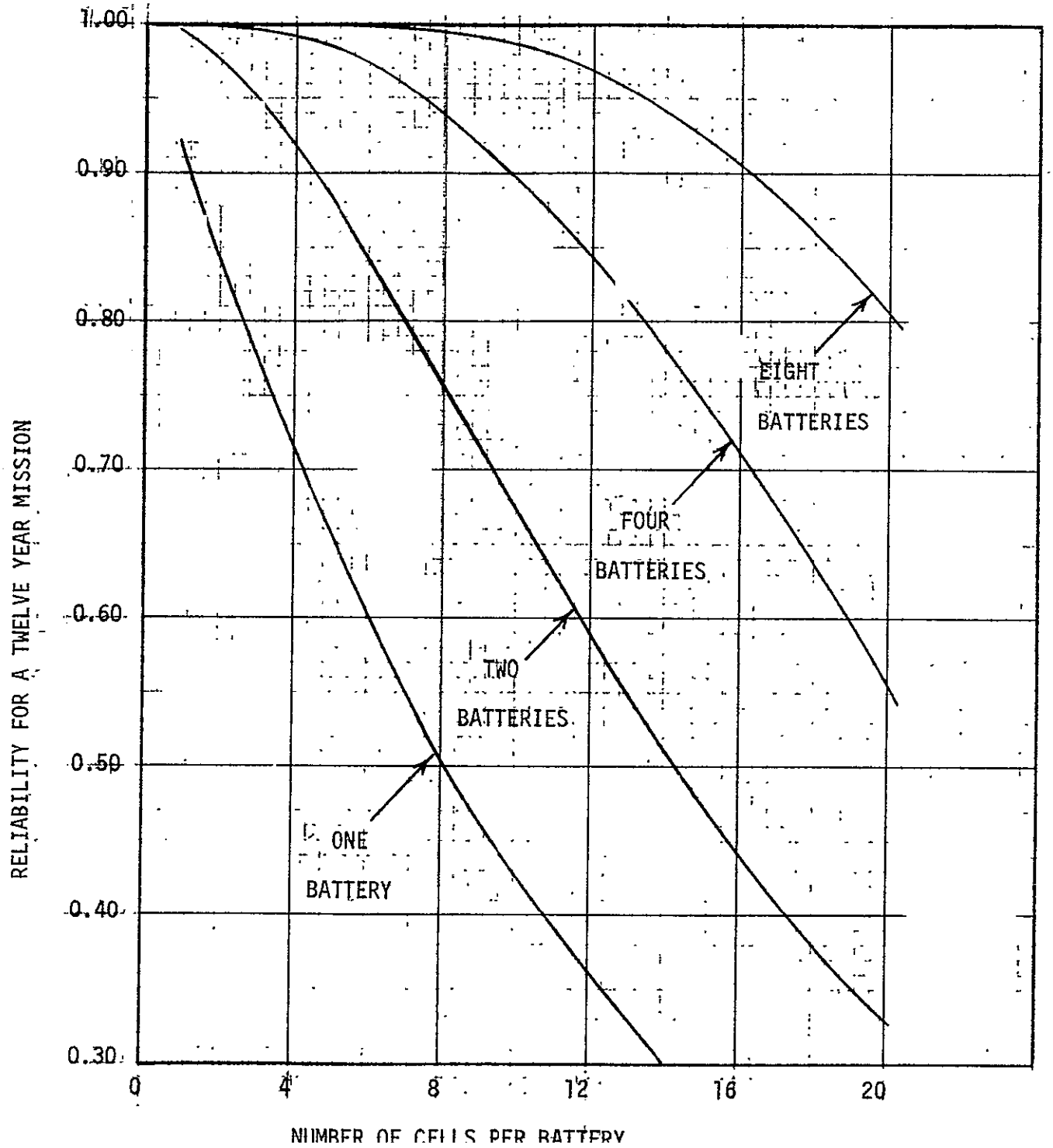


FIGURE B-3. RELIABILITY FOR A TWELVE YEAR MISSION

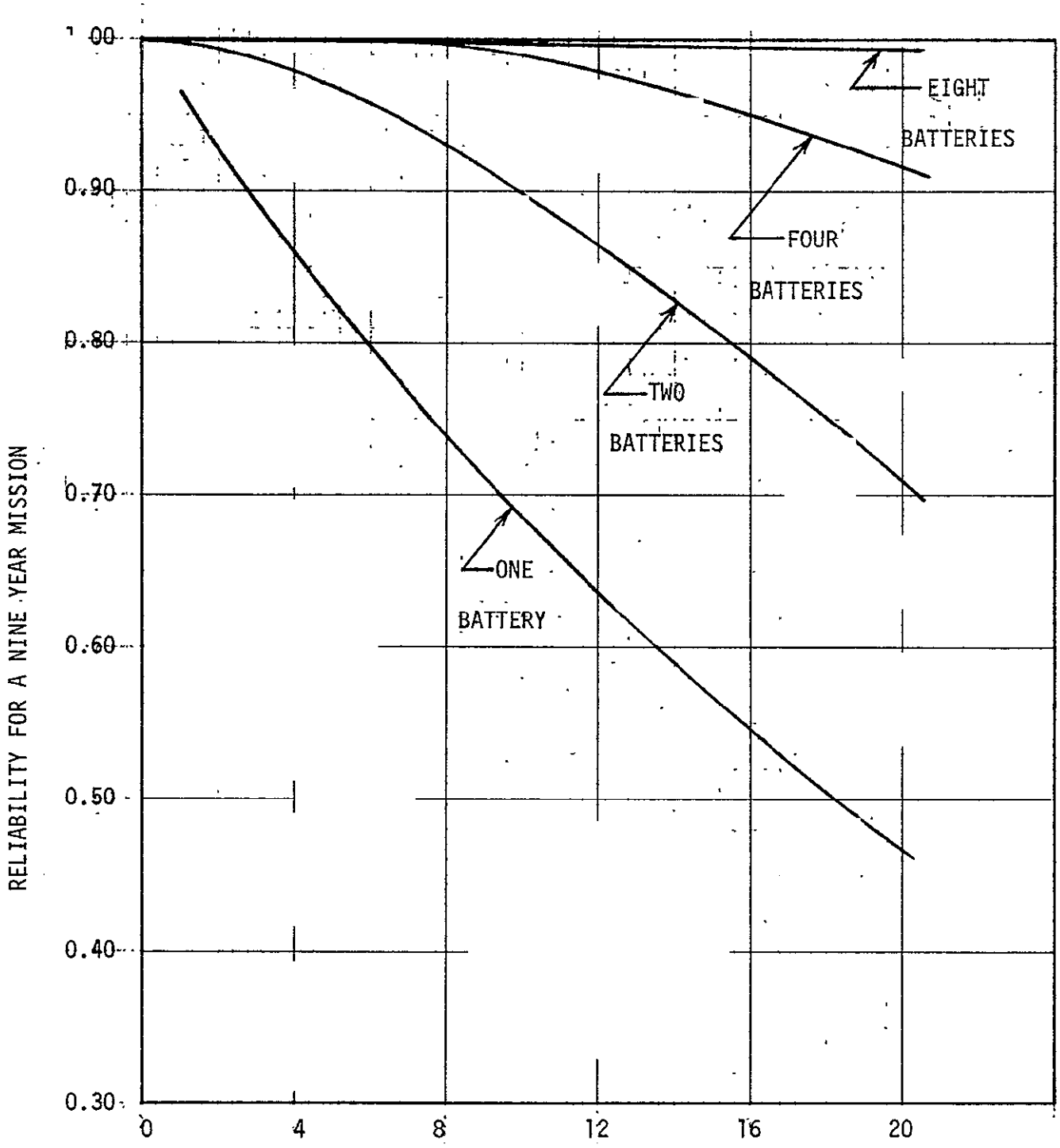


FIGURE B-4. RELIABILITY FOR A NINE YEAR MISSION

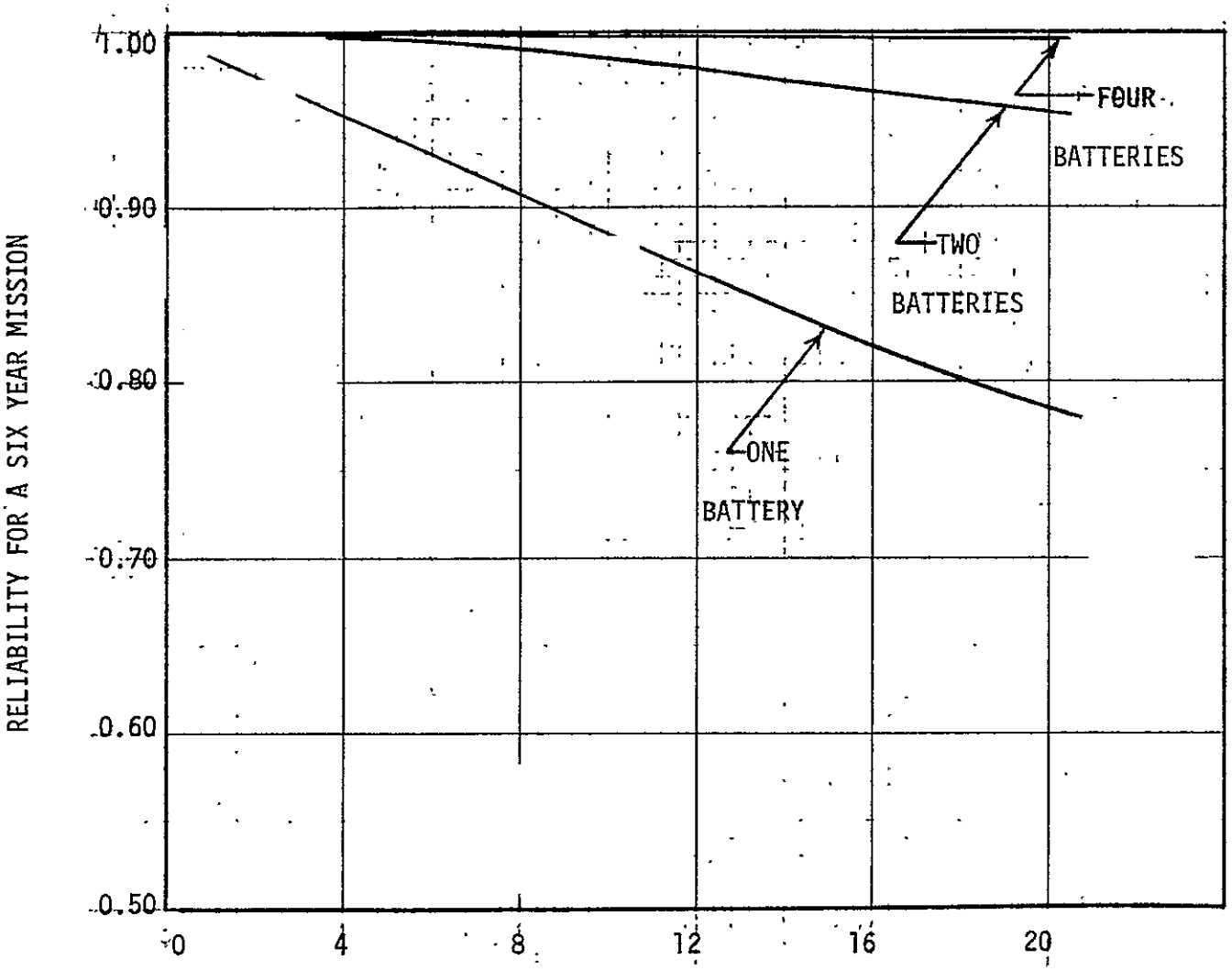


FIGURE B-5. RELIABILITY FOR A SIX YEAR MISSION

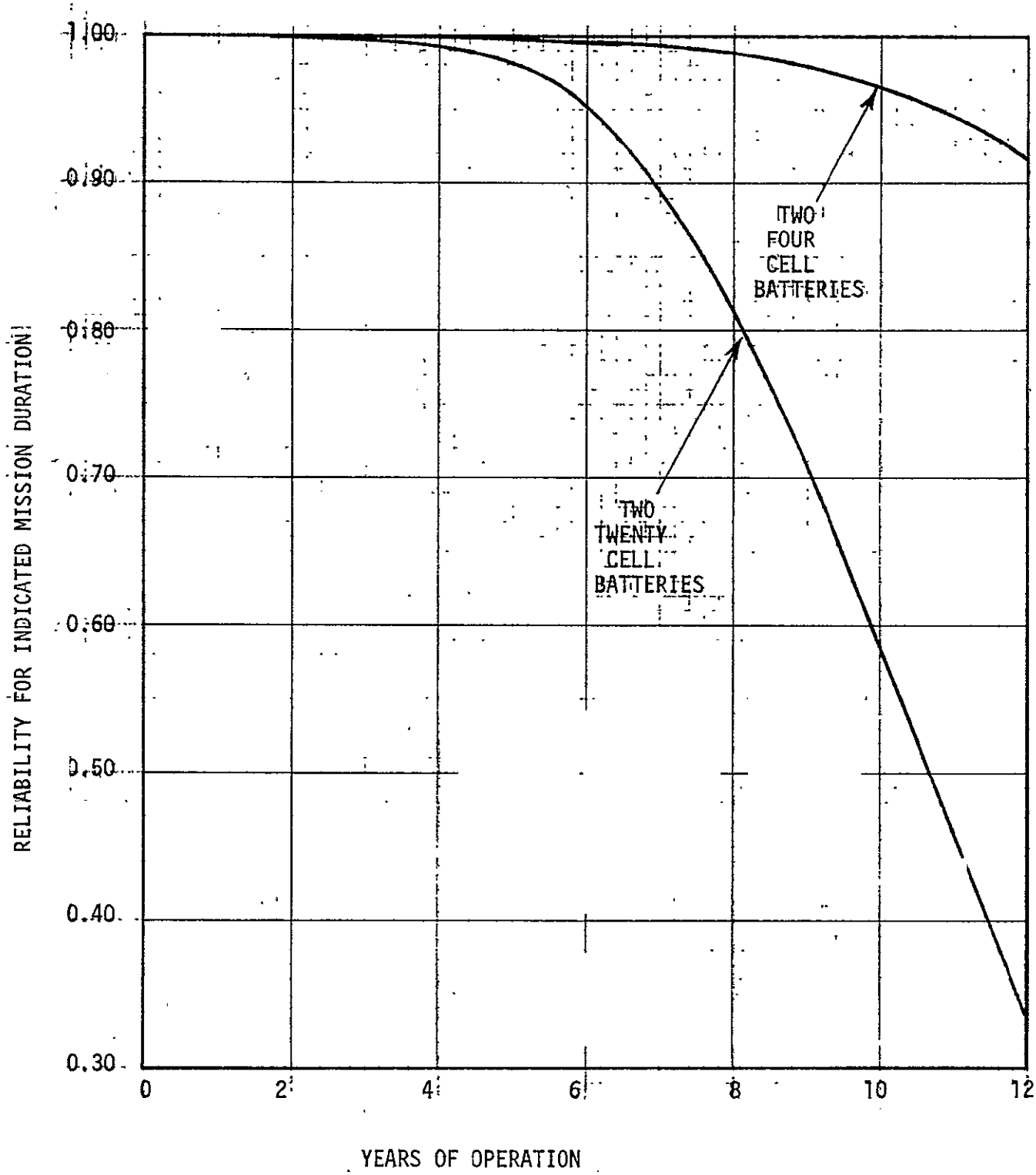


FIGURE B-6. RELIABILITY OF MULTIPLE CELL SYSTEMS

APPENDIX C COMPARISON OF BUS CONFIGURATIONS

With the use of three or more power sources, several electrical configurations are considered for supplying the load under all conditions. For describing those configurations, it is desirable to categorize all loads into three classifications; essential to spacecraft survival, critical to mission performance, and non-critical.

Figure C-1 shows a simple, isolated, multiple bus configuration with three separate power flow paths, completely redundant. This configuration assumes that the loads can be divided into three equal sets, and loss of any single set would not cause a complete loss of mission capability.

Figure C-2 shows a bus implementation in which all essential and all critical loads are supplied from a single bus powered from any one or combination of three RTG's. Failure in any non-critical load takes out, at most, one RTG and the non-critical bus involved. Failure of any RTG results in the loss of capacity of only that RTG. A failure on the critical bus effectively shorts all RTG's, however.

Figure C-3 shows how some of the non-critical loads on a bus with a faulted RTG can be powered from the non-critical bus. This presumes that command access will allow some of the non-critical loads on both buses to be turned off. A cross-over switch is provided so that some of the loads on both non-critical buses can be furnished from a single RTG in a powered-down mode.

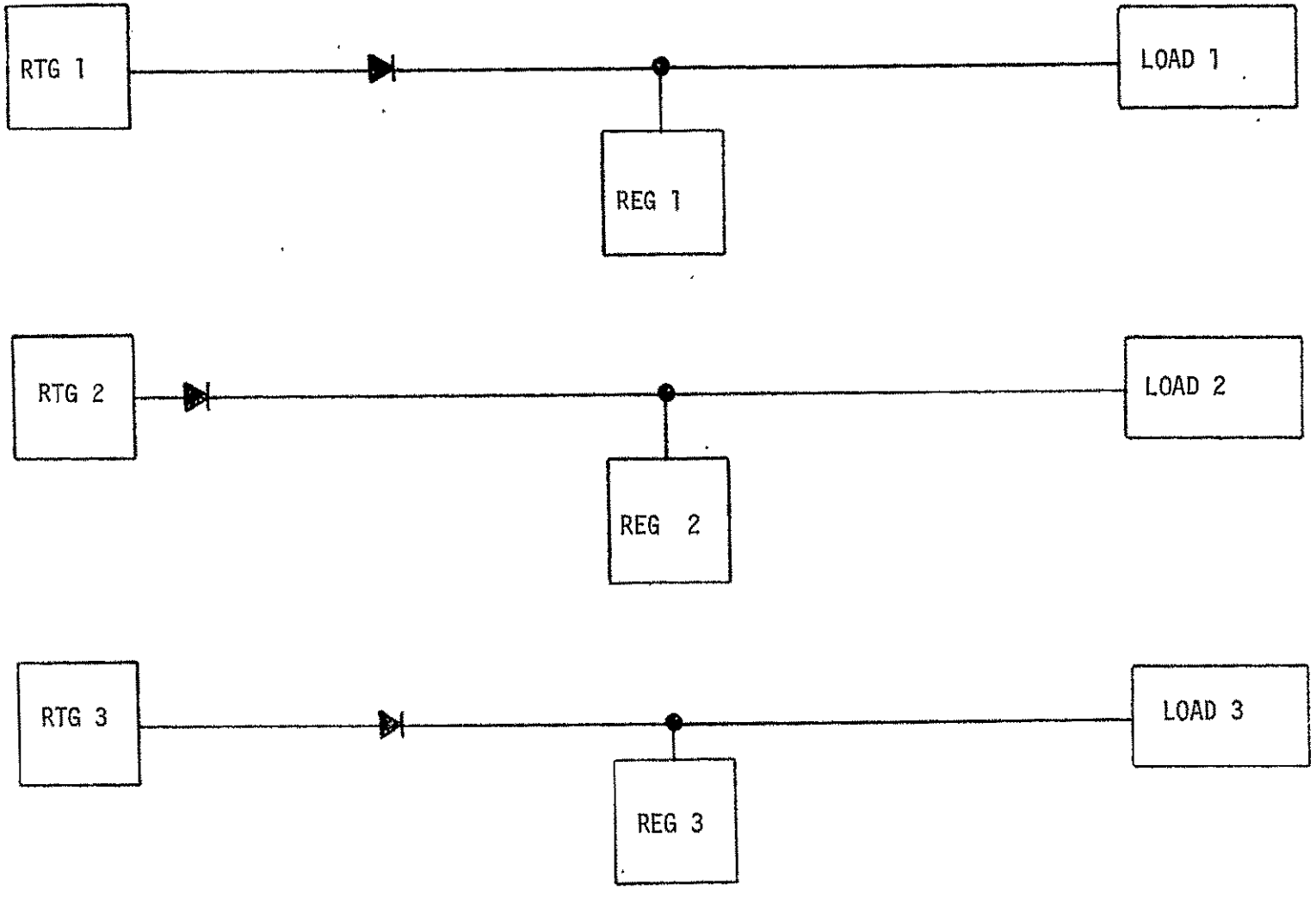


FIGURE C-1 ISOLATED MULTIPLE BUS CONFIGURATION

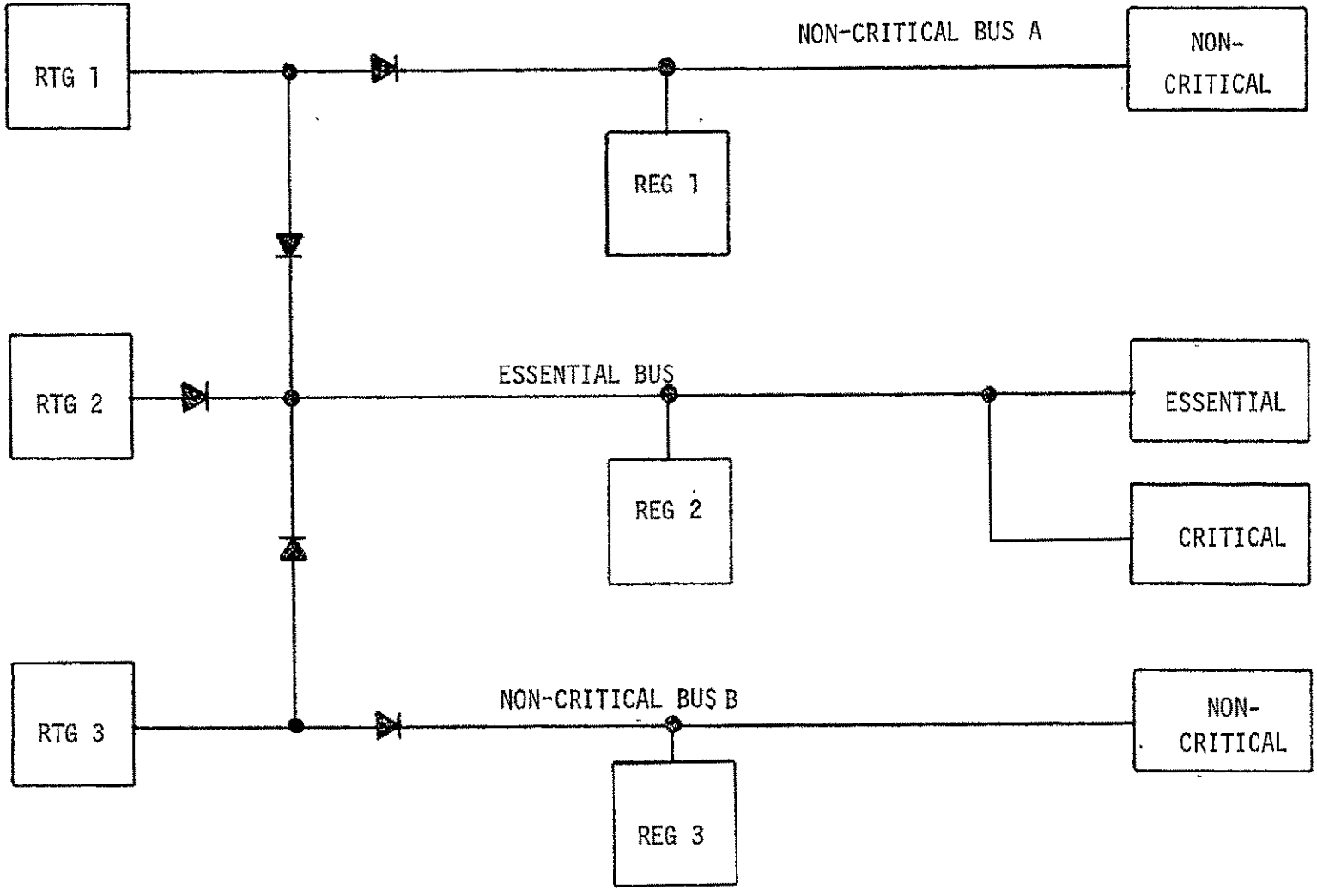


Figure C-2 Simple Multiple Bus Configuration

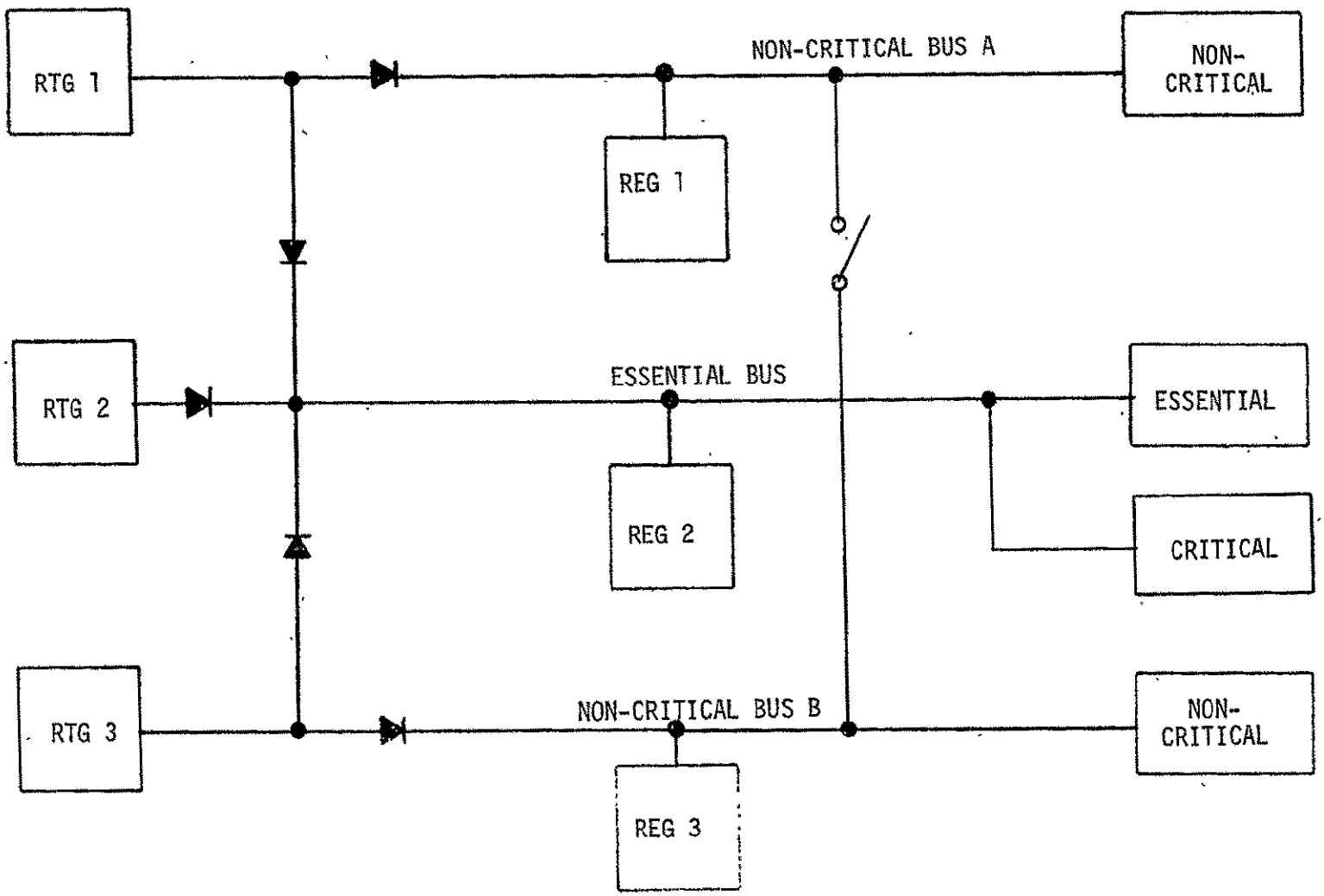


Figure C-3 Simple Multiple Bus Configuration with Power Cross-over

It may be noted that the individual bus shunt regulator can be placed on either side of the isolation diode. The downstream side placement provides the best voltage regulation, since the variation in forward voltage drop of the diode with load and temperature can be corrected by the shunt regulator on each bus. The disadvantage is that a shorted regulator can short out its bus, and that the power handling capacity of the critical bus regulator must include that power that could come from either of the other two buses in the event of regulator failure open, or mismatch in voltage setting.

The three regulators required for any split bus configuration must have a higher total power handling capacity, and thus will be larger and heavier than a single regulator. For total mission success, the multiple regulator configuration is less reliable than a single regulator. The basic quad redundant regulator was simplified to one transistor per block and one third of the basic resistors, for a modified reliability of 0.9836. For three regulators in the multiple bus configuration, the relative reliability is 0.9684.

One additional disadvantage of the arrangement is that the loads do not split up conveniently into three equal groups. In fact, the required power level for any grouping varies from mode to mode. Any such load division reduces operational flexibility and growth capability, and increases the margin required for the flight power source.

Figure C-4 is an elaboration of Figure C-2 to include a low voltage sensing circuit which can interrupt selected non-critical loads if voltage falls below specification on the essential bus. This establishes priority and automatic load scheduling for a minor decrease in available power or an increase in required load. The same considerations exist for shunt regulators, isolation

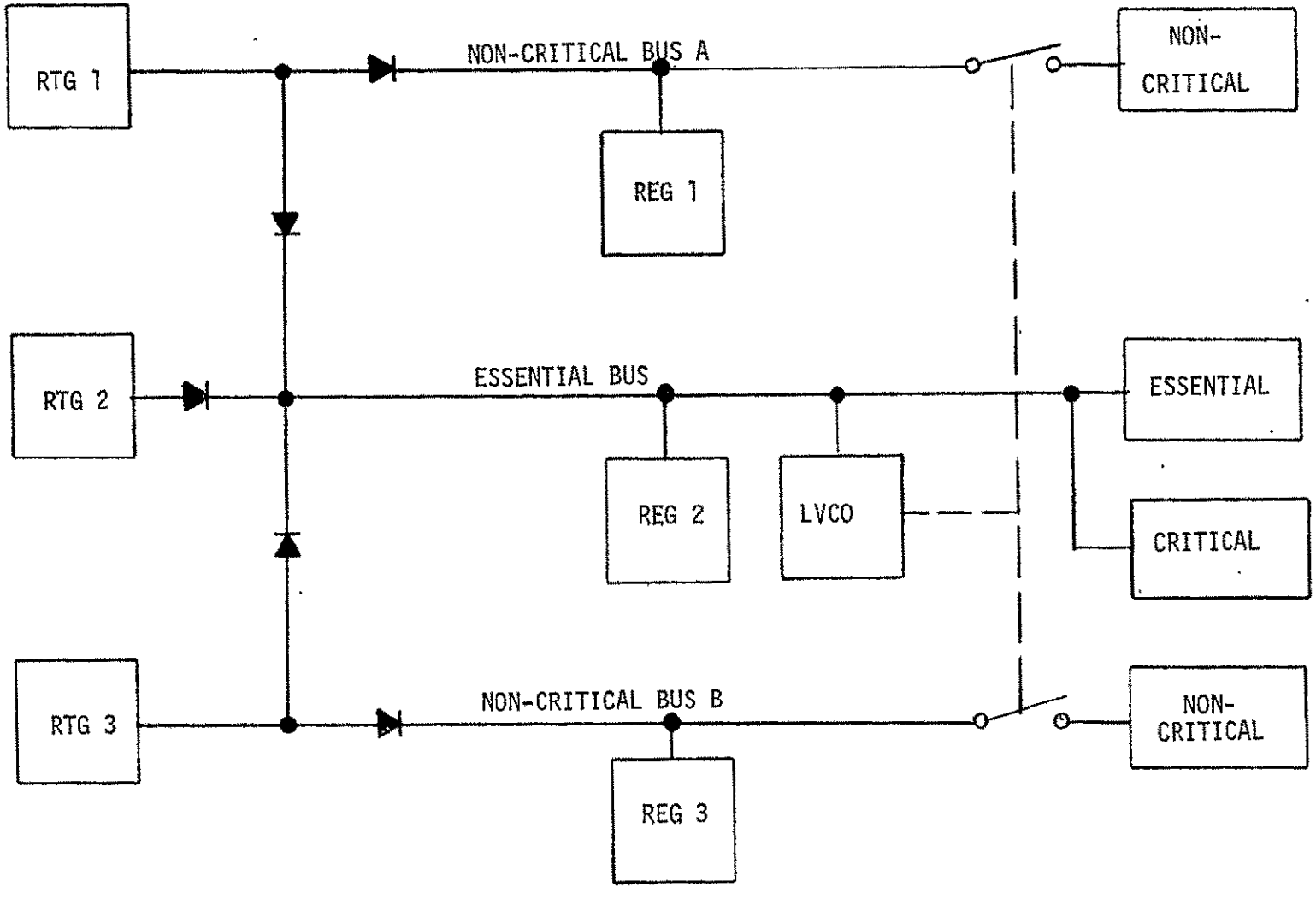


Figure C-4 Protected Multiple Bus Configuration

diodes, and RTG's. Figure C-5 shows how the same protection can be provided to the multiple bus with power cross-over. Diode logic can be used to establish power flow priority as shown in Figure C-6. Here, the essential bus can be powered from any RTG; the critical bus from its own RTG or from the non-critical bus; and the non-critical bus can be powered only from its own source. Figure C-7 provides low voltage sensing and provision to turn off non-critical loads in the event of an under voltage condition on the essential bus, (LVCO).

Figure C-8 depicts a simple single bus configuration with no protection or load priority. It can be noted that the essential power flow path is the same as for any of the previous configurations, but the loads in parallel at a lower priority can fault the total bus.

The low voltage cut off can be implemented on the single bus configuration as shown in Figure C-9. The power flow path for essential loads is the same, and protection against faulted RTG's or faulted non-critical loads has been provided. This arrangement is subject to failure if the regulator fails, but this is common to all configurations considered.

These studies indicate that no bus arrangement can protect essential loads from a shorted essential or critical load. Critical loads must be current limited to a level within the power source capability to assure continuous operation of the remaining loads. Less desirable protection can be provided by sensing load current, detecting an overcurrent condition, and switching off the faulted load.

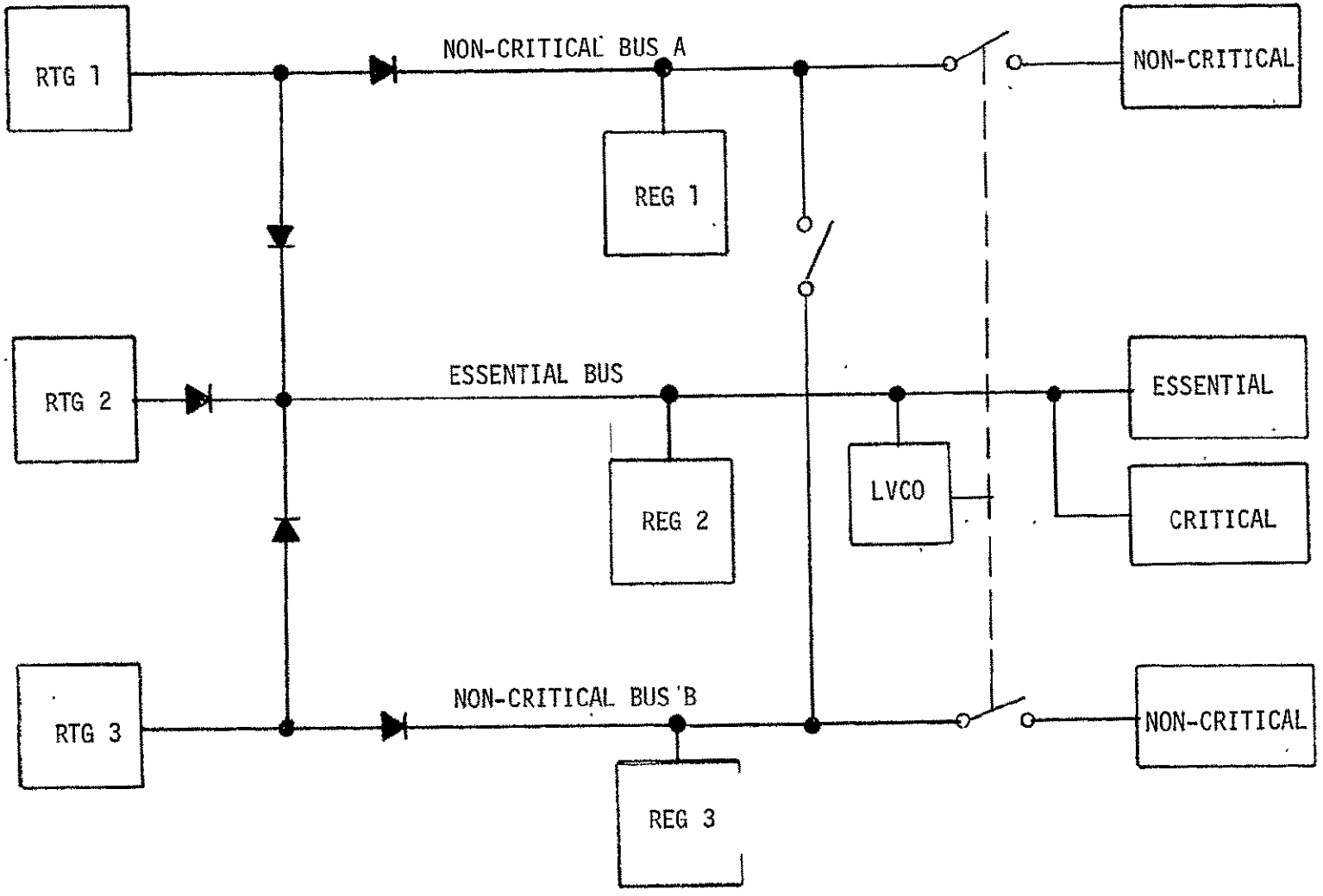


Figure C-5 Protected Multiple Bus Configuration with Power Cross-over.

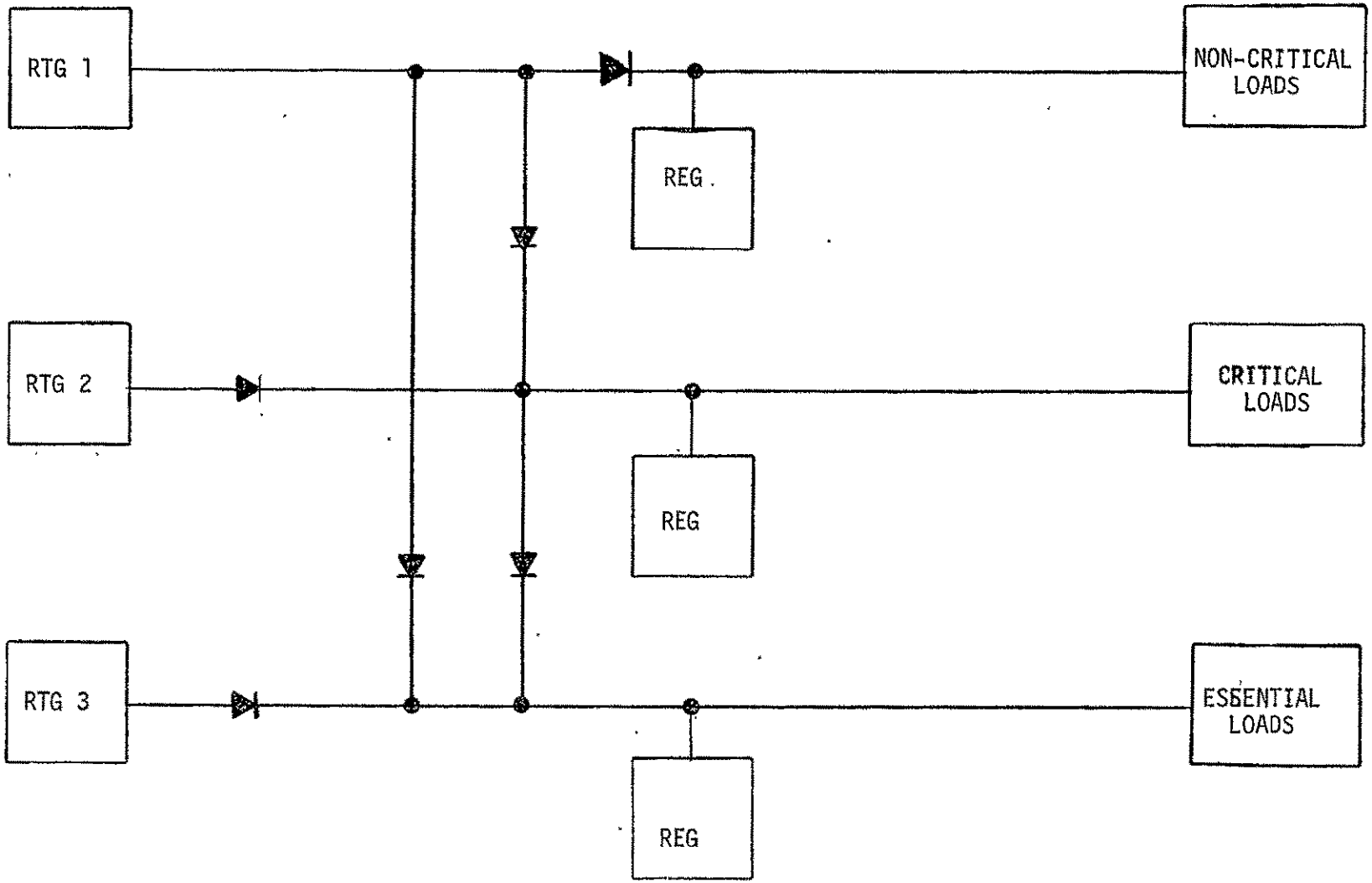


Figure C-6 Priority Multiple Bus Configuration

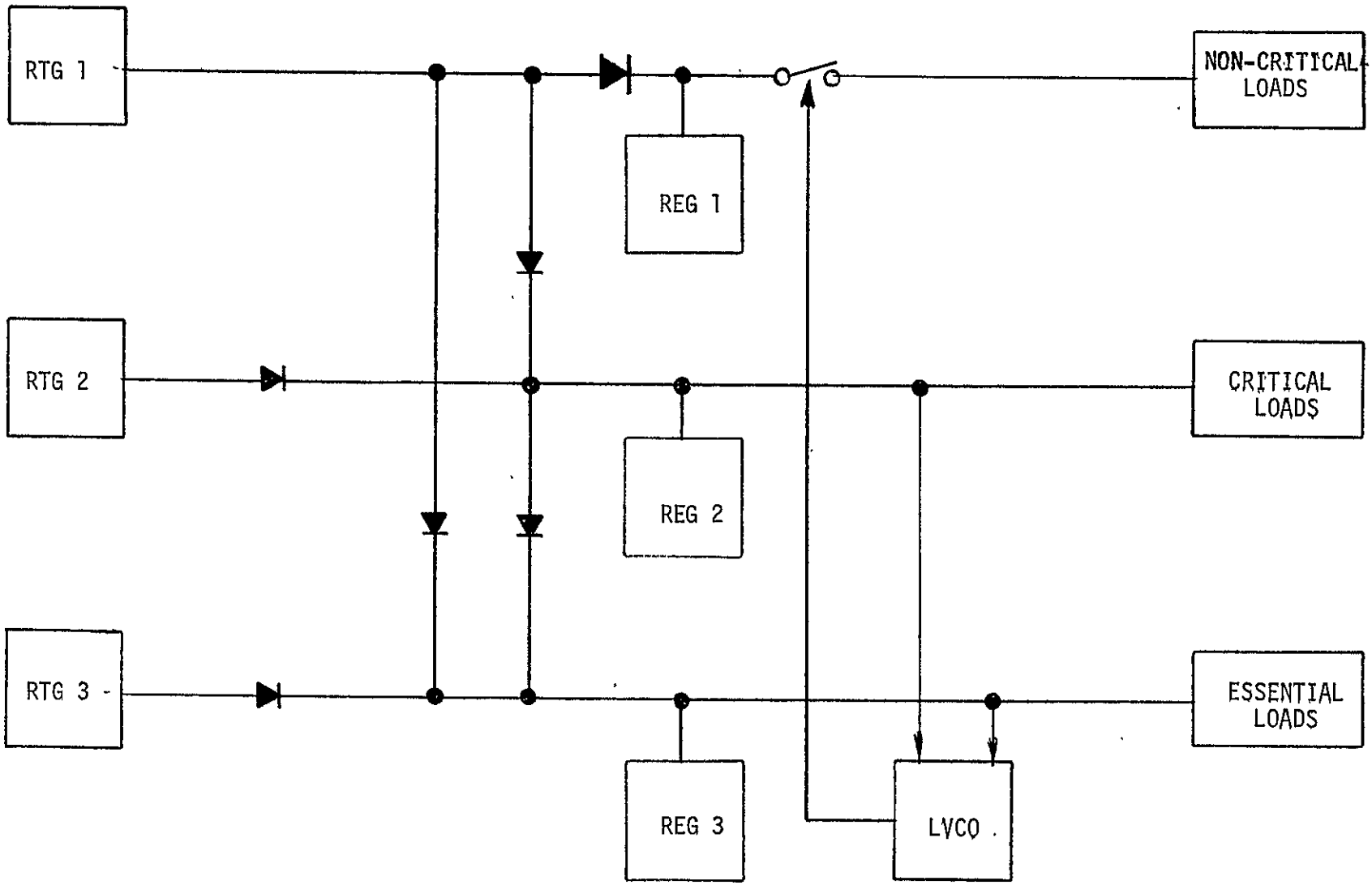


Figure C-7 Protected Priority Multiple Bus Configuration

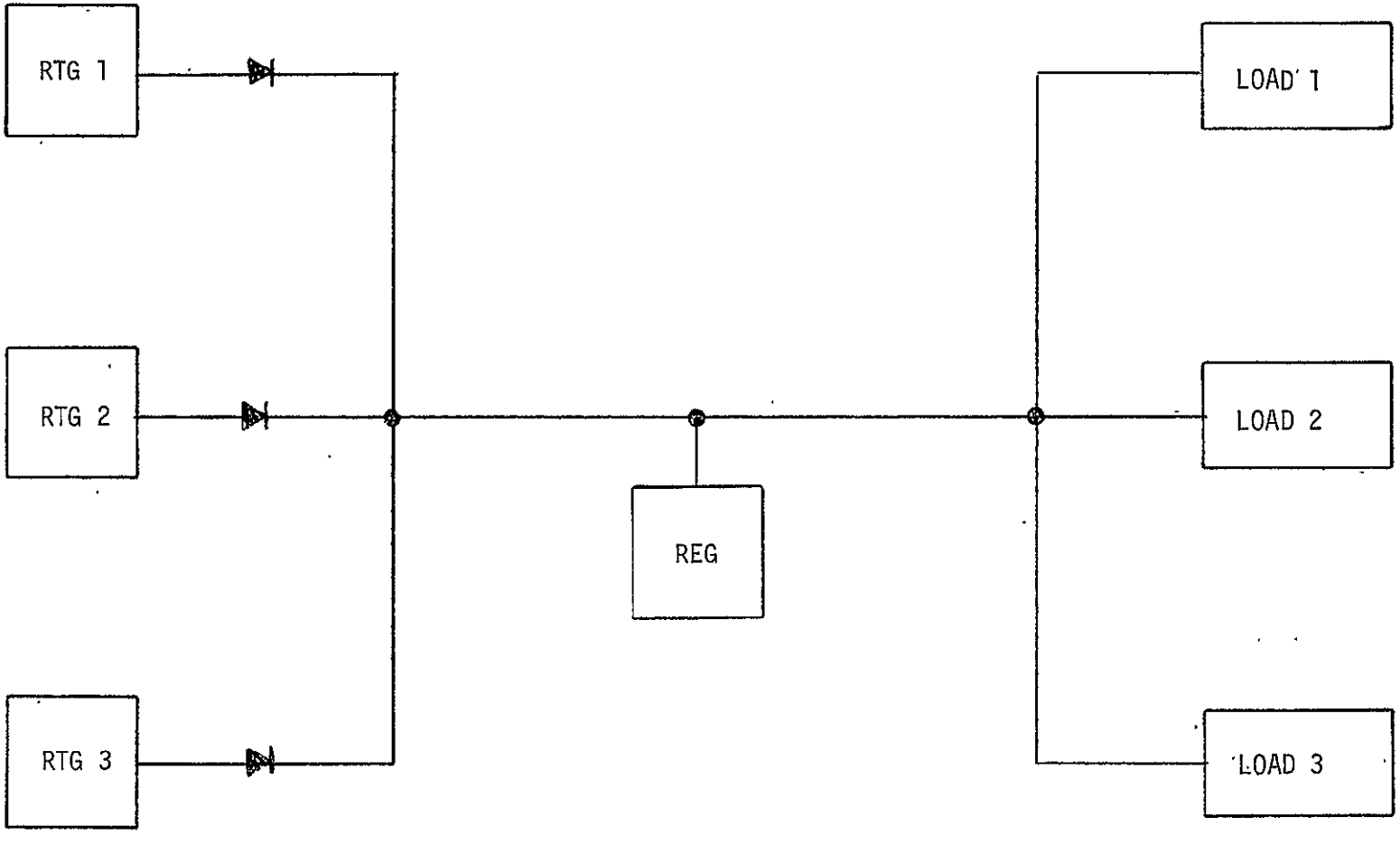


Figure C-8 Simple Single Bus Configuration

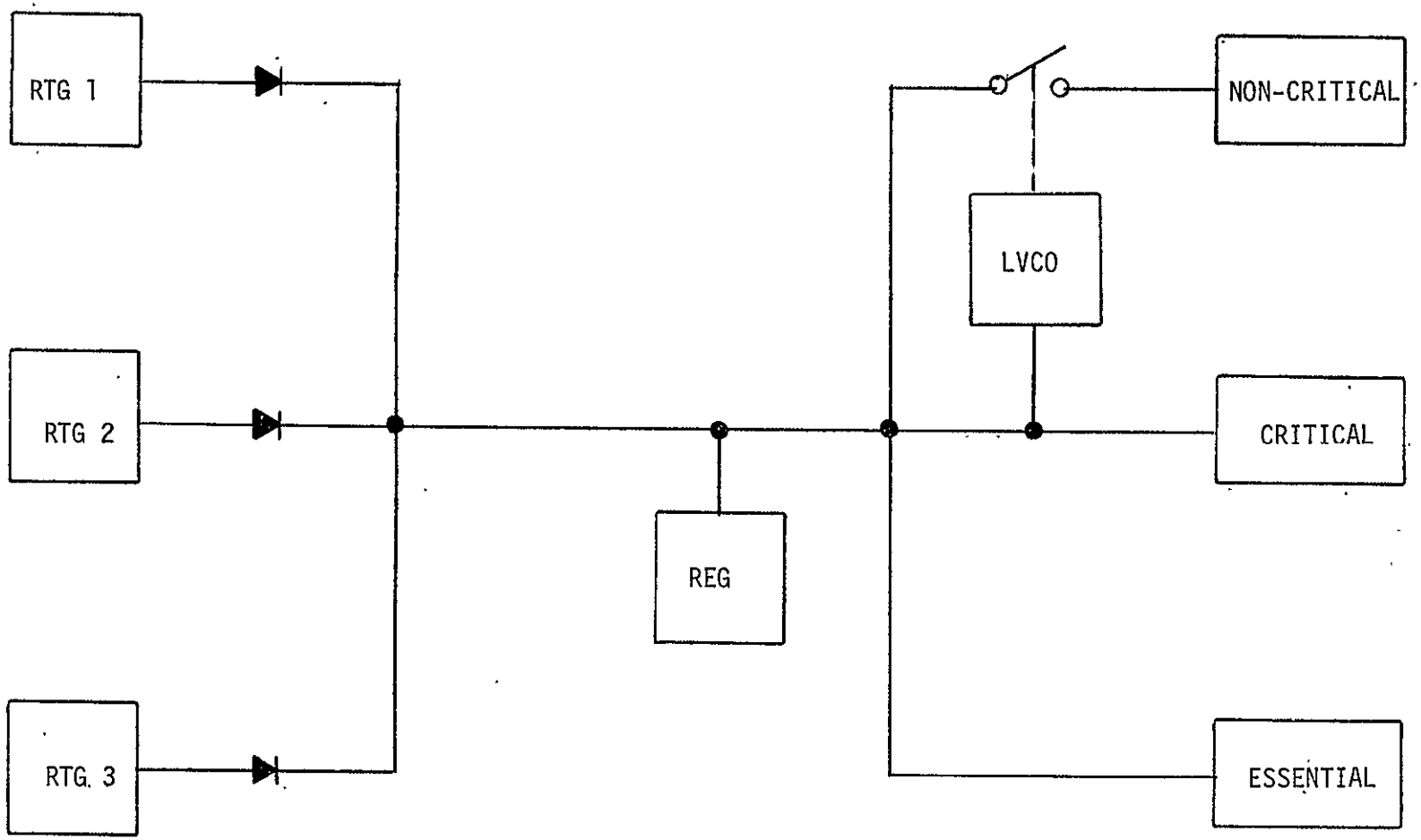


Figure C-9 Protected Single Bus Configuration

The recommended power system is the single bus configuration of Figure C-10. An automatic turn-off of non-critical loads on bus undervoltage is provided to protect essential loads in the event system power consumption exceeds RTG capability or an RTG fails.

With any busing configuration, current limiting or fault clearing by fuses, electronic circuit breaker or some other means must be used on non-critical and on critical loads. Here the single bus has an advantage in that the excess power capability of all three RTG's will be applied to any fault. Likewise, the maximum power is available if too many loads were inadvertently connected to the bus. If the loads were split, whichever RTG saw the excess load would see the excess load alone and could be loaded beyond its ability to supply significant power. The proposed single bus system has a low voltage cutoff of non-critical loads so that any load or distribution fault in those loads will not fail the spacecraft. This allows time to diagnose the problem and provide corrective action. Hence, the maximum power availability will be applied to just the required loads in the event of a malfunction.

In summary, the single bus configuration appears to have less circuitry, fewer interconnections, lower weight, and lower losses than any multiple bus configuration considered. The single bus is more flexible to load number and power changes. Based on these basic considerations, a single bus configuration is the recommended baseline.

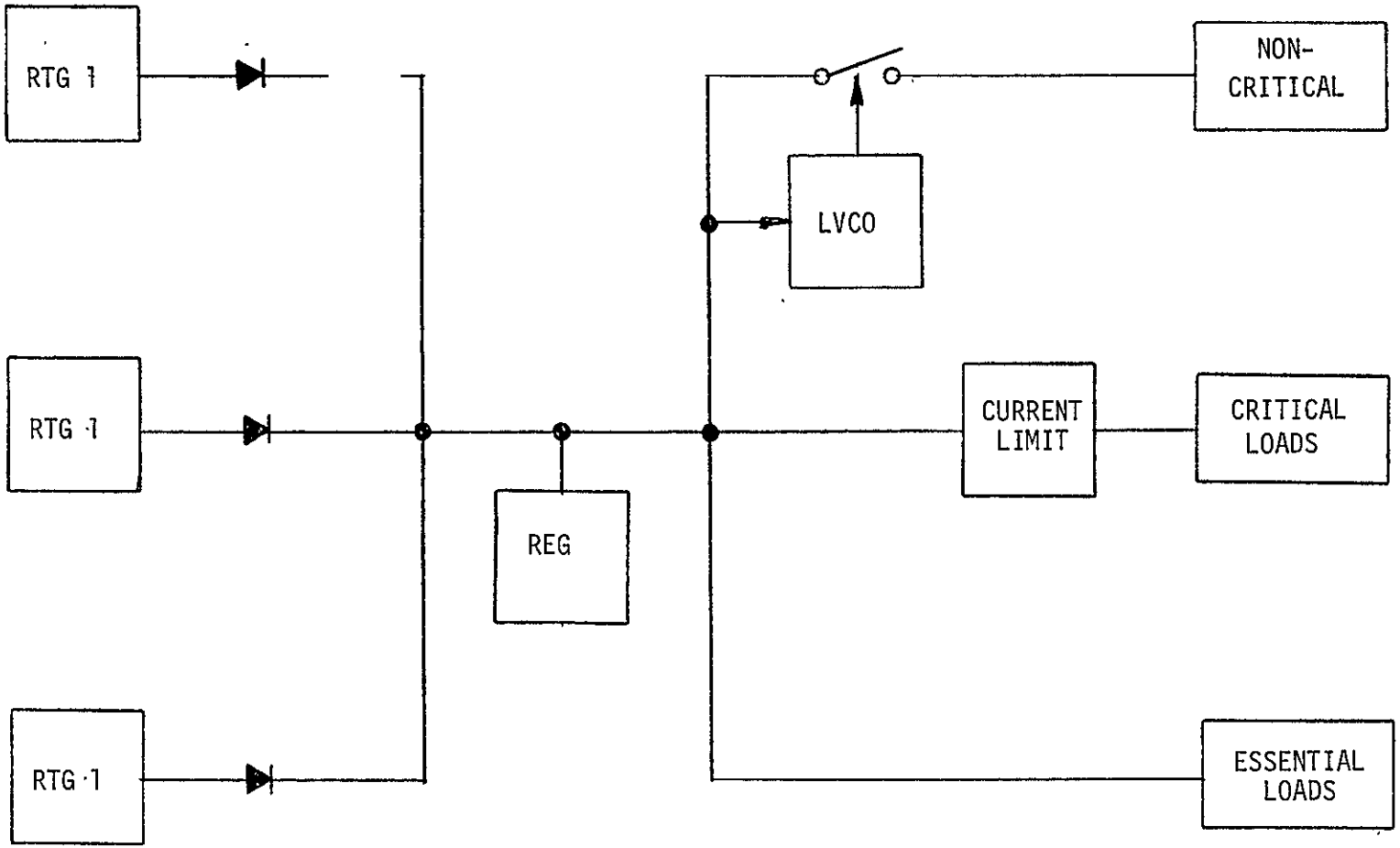


Figure C-10 Recommended Single Bus Configuration

APPENDIX D RTG RELIABILITY WITH AND WITHOUT ISOLATION DIODES

Introduction

An analysis was performed to evaluate the relative reliability of the TOPS RTG configuration with and without isolation didoes. The analysis includes configurations of three and four RTG's as shown in Figure D-1 and D-2.

The method used involves a quantitative comparison of reliability values with and without diodes. The reliability values used are based on an allocation of failure rates to the individual failure modes for the RTG's and diodes.

In order to determine the effect of a possible inaccuracy in the failure rates, the analysis includes the effect of both an increase and decrease in RTG and diode failure rates by a factor of 100.

The results of the analysis are plotted in Figures D-3 through D-9. Each figure contains a set of curves showing the variation of the ratio of a reliability figure of merit (Rj), with and without diodes, as a function of RTG and diode failure rates.

The ratio, Rj, is formulated such that values greater than 1.0 indicate a greater probability of mission success without diodes, and values less 1.0 indicate a greater probability of success with diodes.

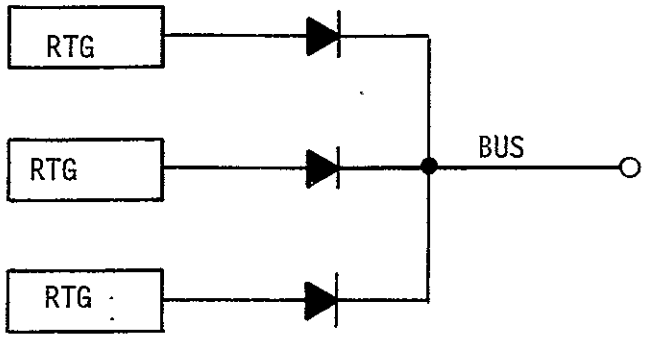


FIGURE D-1. THREE RTG/DIODE CONFIGURATION

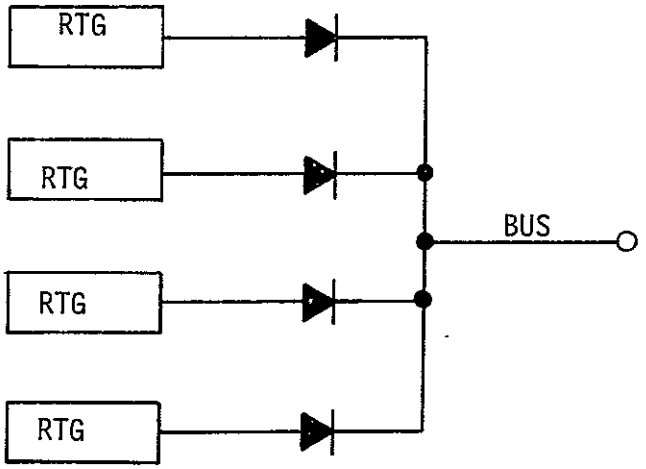


FIGURE D-2. FOUR RTG/DIODE CONFIGURATION

Figures D-4 and D-7 show the inability to meet a requirement for at least two RTG's to be up. The curves indicate that the configurations with diodes provide a higher probability of success unless the true diode failure rate is significantly higher than the nominal value.

The remaining curves are interpreted in a similar manner. In general, it is concluded that the use of isolation diodes provides higher reliability for those conditions where the loss of some (but not all) of the RTG's would still provide a significant mission value.

Conversely, if all RTG's are required to provide a significant mission return, then the diodes should be excluded.

The reliability comparison was made by evaluating the ratio

$$Rj = \frac{Pj \text{ with diodes}}{Pj \text{ without diodes}}$$

Where Pj is the probability of loss of at least j RTG's.

For the configuration with three RTG's:

P1 = Probability of loss of at least one RTG
(i.e., one, two, or all three are down)

Thus, P1 reflects the inability to meet a condition requiring all three RTG's; and R1 values greater than 1.0 indicate that there is a greater probability of all three RTG's being up if the isolation diodes are eliminated.

Similarly, P2 is the probability of loss of two or more RTG's, and reflects the inability to meet a condition requiring at least two RTG's; a value of R2 greater than 1.0 indicates that there is a greater probability of at least two RTG's being up if the isolation diodes are eliminated.

For all cases considered, values of Rj greater than 1.0 indicate a higher probability of success without diodes, and value of Rj less than 1.0 indicate a higher probability of success with diodes.

Reliability Model For A Single RTG/Diode

Three modes are defined for a single RTG/diode combination as follows:

G = Good - capable of providing full rated power in the bus configurations shown in Figure D-1.

D = Degraded - incapable of providing full rated power in the bus configurations shown in Figure D-1, but will not impair operation of the other RTG's or affect the bus voltage.

F = Failed - conditions affecting the bus voltage or other RTG's when operated in the configurations shown in Figure D-1.

The RTG modes and the symbol for the probability of each are as follows:

RTG good, $R_1 = 1 - (O_1 + S_1)$

RTG open, O_1

RTG internal short, S_1

RTG short to cold frame, $S_r = 1 - R_r$

RTG cold frame short to ground, $S_f = 1 - R_f$

The diode modes and the symbol for the probability of each are as follows:

Diode good, $R_2 = 1 - (O_2 + S_2)$

Diode open, O_2

Diode internal short S_2

Diode short to ground $S_d = 1 - R_d$

For this analysis, it is assumed that the diode heat sink is on the anode side and that a short to ground can occur only from anode to ground as follows:

This method provides protection for the bus in the event of a single diode short to ground.

It is noted that for the above modes, the RTG short to cold frame, RTG cold frame short to ground, and the diode short to ground are considered to be independent failure modes; i.e., they are not influenced by internal short or open of the RTG or diode.

The probability of experiencing each of the possible modes of operation of the RTG/diode combination can be enumerated by expansion of the expression:

$$(R_1 + O_1 + S_1) \times (R_r + S_r) \times (R_f + S_f) \times (R_2 + O_2 + S_2) \times (R_d + S_d)$$

Most of the 72 states defined by the above expression result in the degraded mode (D) for the RTG/diode combination; the computations have, therefore, been simplified by enumerating the good (G) and failed (F) states and computing the probability of being in the degraded state P (D) as:

$$P(D) = 1 - P(G) - P(F)$$

The probability expressions for each of the good states are as follows:

$R_1\ R_2\ R_r\ R_d\ R_f$ - everything up

$R_1\ R_2\ S_r\ R_d\ R_f$ - RTG short to cold frame

$R_1\ S_2\ R_r\ R_d\ R_f$ - diode shorted internally

$R_1\ S_2\ S_r\ R_d\ R_f$ - RTG short to cold frame and diode shorted internally

$R_1\ R_2\ R_r\ R_d\ R_f$ - RTG cold frame short to ground

$R_1\ S_2\ R_r\ R_d\ R_f$ - RTG cold frame short to ground and diode shorted internally

The probability expressions for each of the failed states are as follows:

$0.5 \times S_1\ S_2\ R_r\ R_d\ R_f$* - RTG shorted and diode shorted

$S_1\ S_2\ S_r\ R_d\ R_f$ - RTG shorted, diode shorted, and RTG shorted to cold frame

$R_1\ S_2\ R_r\ S_d\ R_f$ - Diode shorted internally and also shorted to ground

$O_1\ S_2\ R_r\ S_d\ R_f$ - RTG open, diode shorted internally and also shorted to ground

$S_1\ S_2\ R_r\ S_d\ R_f$ - RTG and diode shorted internally, and diode shorted to ground

$R_1\ S_2\ S_r\ S_d\ R_f$ - Diode shorted internally and to ground and RTG shorted to cold frame.

$O_1\ S_2\ S_r\ S_d\ R_f$ - RTG open internally and shorted to cold frame and diode shorted internally and to ground

$S_1\ S_2\ S_r\ S_d\ R_f$ - RTG shorted internally and to cold frame, and diode shorted internally and to ground

and

all of the above 8 modes with the addition of the RTG cold frame shorted to ground

and

$R_1\ S_2\ S_r\ R_d\ S_f$ - Diode shorted internally and RTG short to cold frame and cold frame short to ground

* In the event of an internal RTG short, i.e., shorting of some of the couples, the bus voltage will be affected only if more than half of the couples are shorted since the open circuit voltage is approximately

twice the full load voltage. It is assumed that given an RTG internal short, more than half of the couples will be shorted 50% of the time, and therefore, the probability of failure due to RTG and diode short is multiplied by 0.5. The remaining 50% of the time, only a single RTG will be lost and this is considered a degraded bus configuration.

Therefore, by collecting terms:

$$P(G) = R_1 R_2 R_d R_f + R_1 S_2 R_d R_f + R_1 R_2 R_r R_d S_f + R_1 S_2 R_r R_d S_f$$

$$P(F) = S_1 S_2 R_d + S_2 S_d + R_1 S_2 S_r R_d S_f$$

$$P(D) = 1 - P(G) - P(F)$$

Reliability Models for the Three RTG/Diode Configuration (Figure D-2)

The required probability expressions for the three RTG/diode configuration are as follows:

Let P_j = probability of loss of at least j RTG's

$$P_1 = 1 - [P(D)]^3$$

$$P_2 = 1 - 3[P(G)]^2 [P(D)] - P_1$$

$$P_3 = 1 - 3[P(G)][P(D)]^2 - P_2$$

Reliability Models for the Four RTG/Diode Configuration (Figure D-2)

The required probability expressions for the 4 RTG/diode configuration are as follows:

$$P_1 = 1 - [P(G)]^4$$

$$P_2 = 1 - 4[P(G)]^3 [P(D)] - P_1$$

$$P_3 = 1 - 6[P(G)]^2 [P(D)]^2 - P_2$$

$$P_4 = 1 - 4[P(G)][P(D)]^3 - P_3$$

Reliability Models for the Configurations Without Diodes

The computations for the three and four RTG configurations without diodes employ the same models as the "with" diode configurations by considering the diodes permanently shorted. This is accomplished by setting:

$$R_2 = 0$$
$$O_2 = 0$$
$$S_2 = 1.0$$
$$S_d = 0$$
$$R_d = 1.0$$

The JPL supplied diode failure rate (λd) of 0.05 failures per 10^6 hours was used as a baseline.

It was assumed that the ratio of shorts to opens is 9:1 and that the probability of a diode short to ground is 0.01 x probability of diode failure. The mission time is assumed to be 4193 days.

Therefore:

$$R_2 = \exp(-.05 \times 10^{-6} \times 24 \times 4193)$$
$$O_2 = 0.1\ (1-R_2)$$
$$S_2 = 0.9\ (1-R_2)$$
$$R_d = \exp(-.0005 \times 10^{-6} \times 24 \times 4193)$$
$$S_d = 1 - R_d$$

RTG's

The basic RTG failure rate is assumed to be 0.1365 failures per 10^6 hours for opens and shorts as described in Section 7 of the Quarterly Report dated October 15, 1969.

The failure rate for shorts to the cold frame is 1/20 of the basic failure rate, and the probability of a cold frame short to ground is assumed to be 0.01 x probability of RTG failure. The mission time is 4193 days.

Therefore:

$$R_1 = \exp(-.1365 \times 10^{-6} \times 24 \times 4193)$$
$$O_1 = .95\ (1-R_1)$$
$$S_1 = .05\ (1-R_1)$$
$$R_r = \exp(-0.5 \times .1365 \times 24 \times 4193)$$
$$S_r = (1-R_r)$$
$$S_f = .01\ (1-R_1)$$
$$R_f = 1 - S_f$$

Sensitivity Study Values

In order to evaluate the effect of a possible inaccuracy in failure rates, the desired parameters were obtained over the following range of failure rate values shown in Table D-1.

The models discussed were evaluated for the parameter values identified using the GE deskside computer system.

The resulting values of Rj are plotted as a function of diode and RTG failure rates in Figures D-3, D-4, and D-5 for the three RTG configuration; and in Figures D-6, D-7, D-8, and D-9 for the four RTG configuration.

Figure D-3

P_1 is the probability of loss of one or more RTG's, and therefore, indicates the inability to meet the condition where all three RTG's are required. In

TABLE D-1

VALUES FOR RELIABILITY SENSITIVITY STUDIES

DIODE FAILURE RATE ↓ / RTG FAILURE RATE →	0.01X	0.1X	NOMINAL	10X	100X
0.01X	RTG .001365 DIODE .0005	.01365 .0005	.1365 .0005	1.365 .0005	13.65 .0005
0.1X	RTG .001365 DIODE .005	.01365 .005	.1365 .005	1.365 .005	13.65 .005
NOMINAL	RTG .001365 DIODE .05	.01365 .05	.1365 .05	1.365 .05	13.65 .05
10X	RTG .001365 DIODE .5	.01365 .5	.1365 .5	1.365 .5	13.65 .5
100X	RTG .001365 DIODE 5.0	.01365 5.0	.1365 5.0	1.365 5.0	13.65 5.0

Figure D-3 all values of R_1 are greater than 1.0, and therefore, if all three RTG's are required for satisfactory performance, elimination of the diodes would provide the more reliable configuration.

This result is anticipated. The diodes are used to prevent the loss of the bus in the event of an RTG short. However, if a single RTG loss cannot be tolerated, then the diodes just contribute an additional probability of failure.

Figure D-4

P_2 reflects the inability to meet a condition requiring two RTG's. results indicate that the use of diodes results in a more reliable configuration unless the true diode failure rate is at least 3 times the nominal rate used.

The remaining figures can be evaluated in an analogous manner.

In general it is concluded that the configurations without diodes are preferable if the power distribution and load arrangement is such that all three RTG's are required to achieve a reasonable mission value. However, if a significant mission value can be realized even though one or more (but not all) RTG's cannot supply power, then the configurations with diodes provide a greater probability of success. An exception to the last statement is the condition where the true diode failure rate is several times the nominal failure rate.

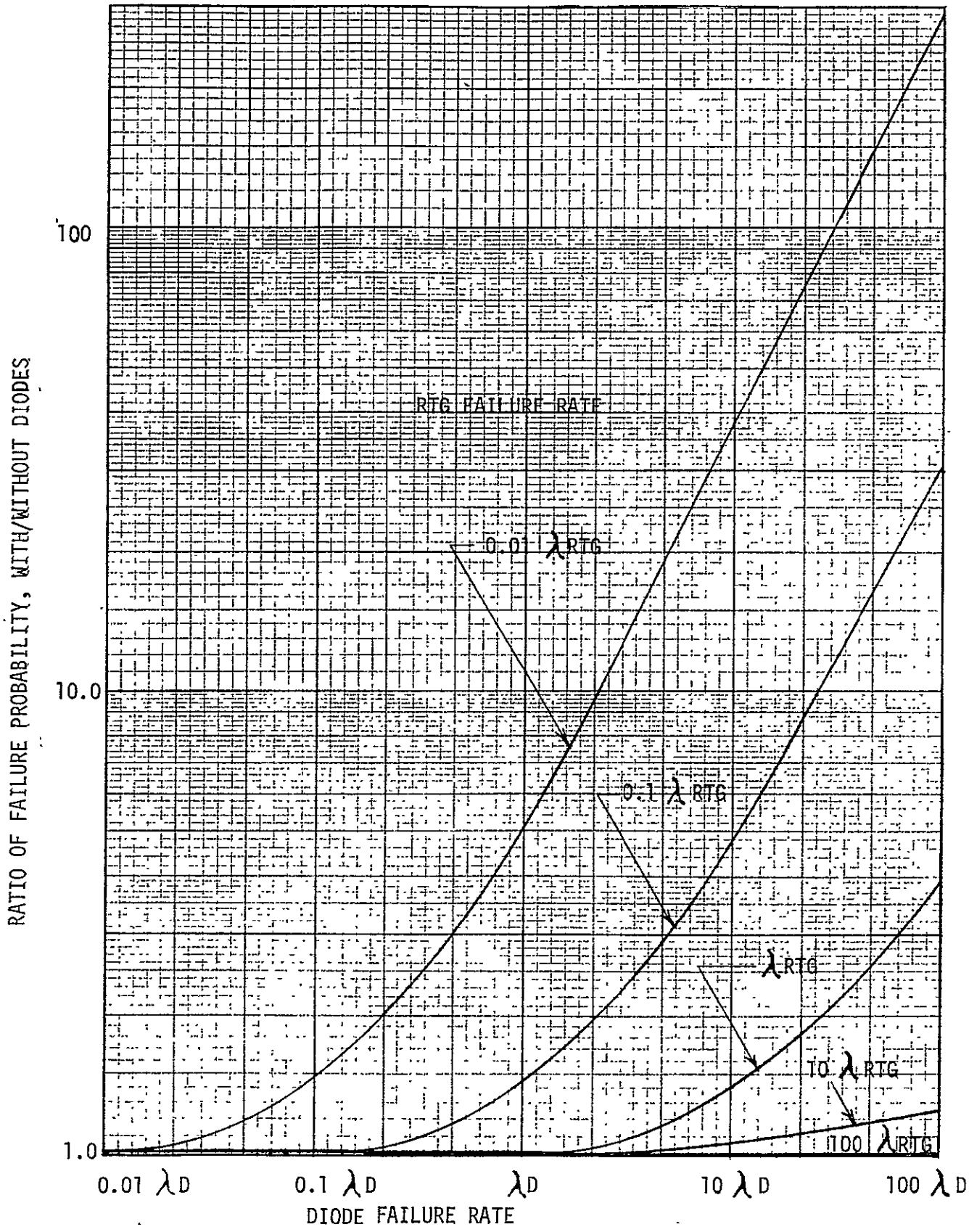


FIGURE D-3 PROBABILITY OF LOSS OF ONE OUT OF THREE RTG's

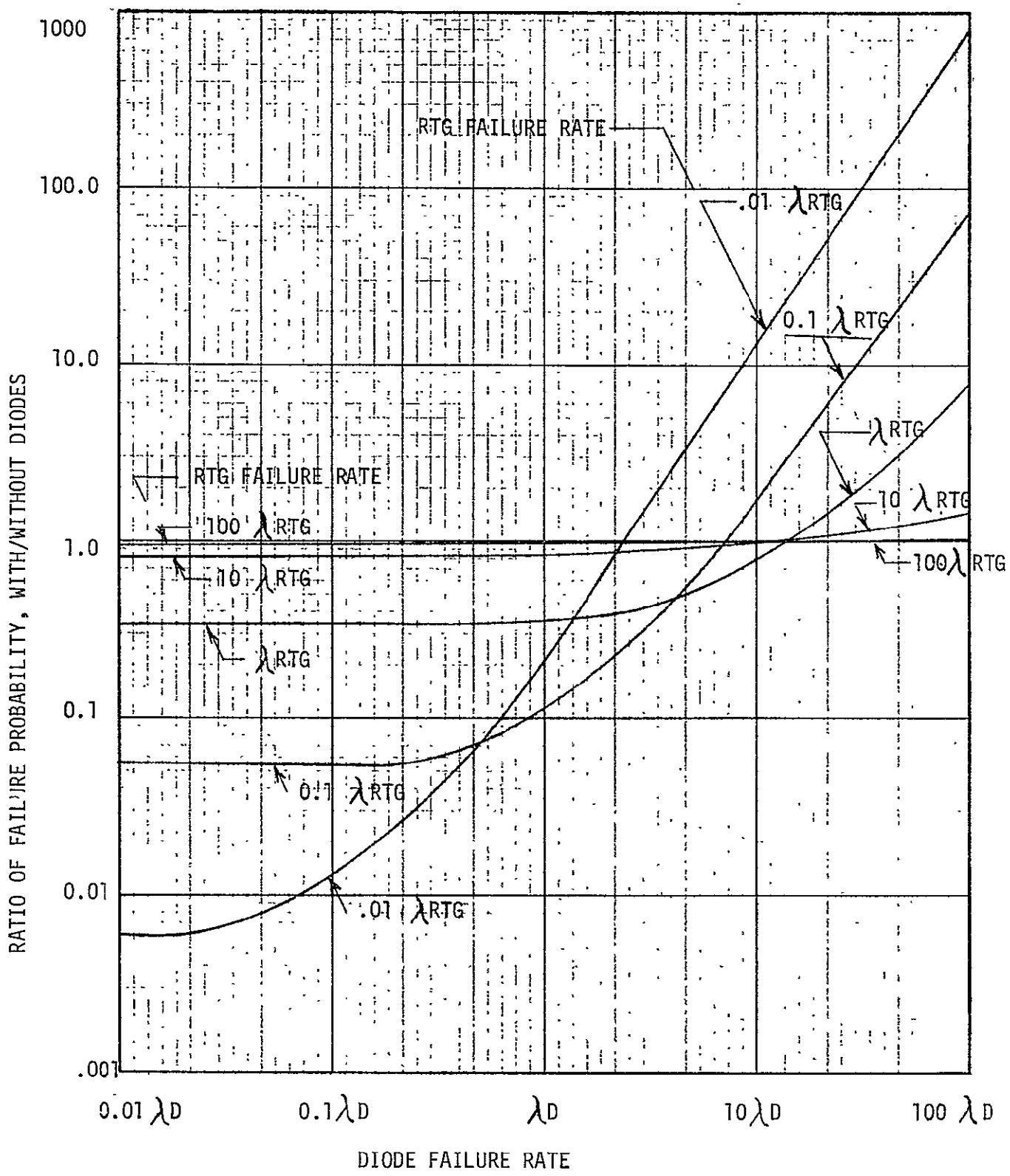


FIGURE D-4. PROBABILITY OF LOSS OF TWO OUT OF THREE RTG's

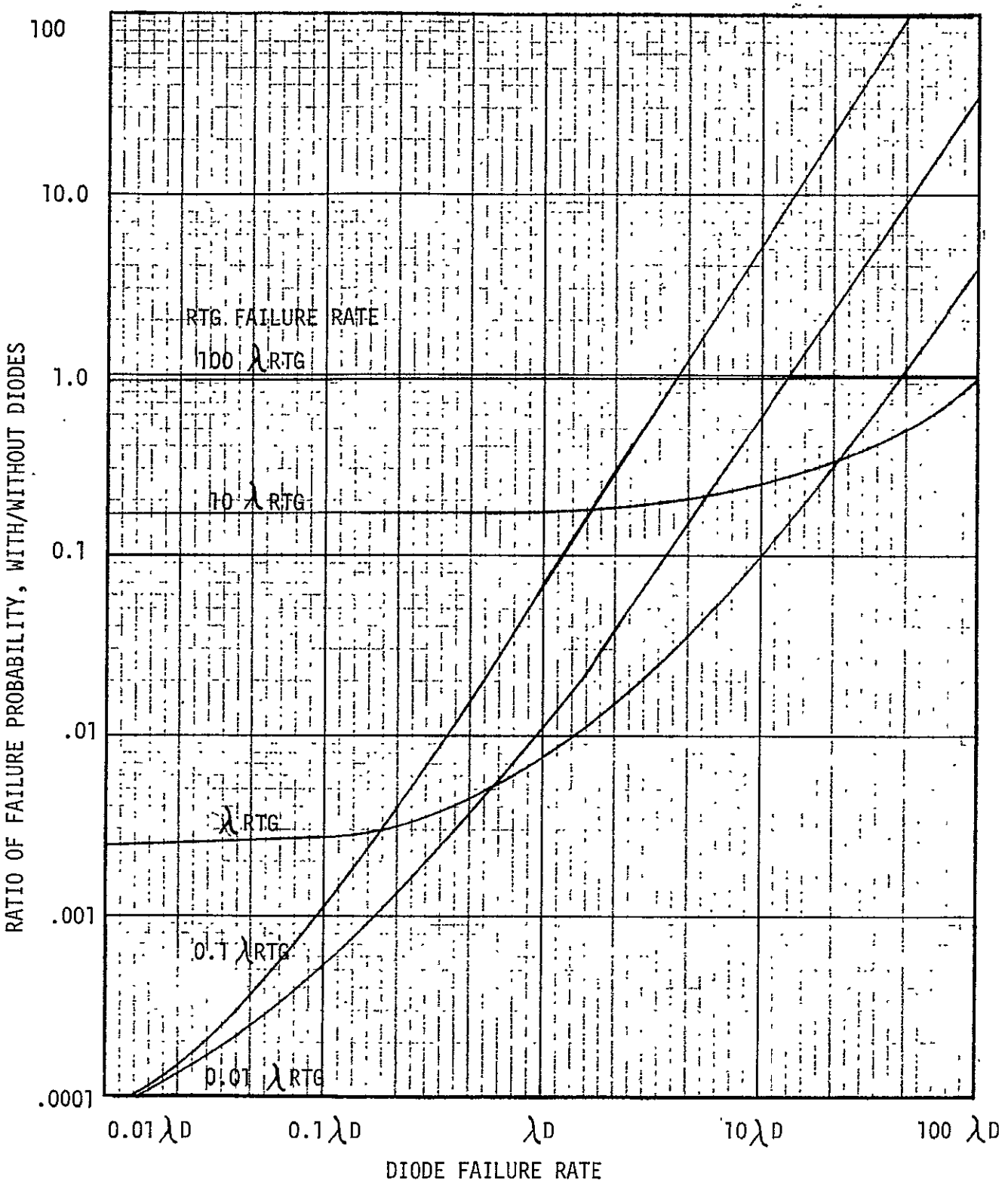


FIGURE D-5 PROBABILITY OF LOSS OF ALL THREE RTG's

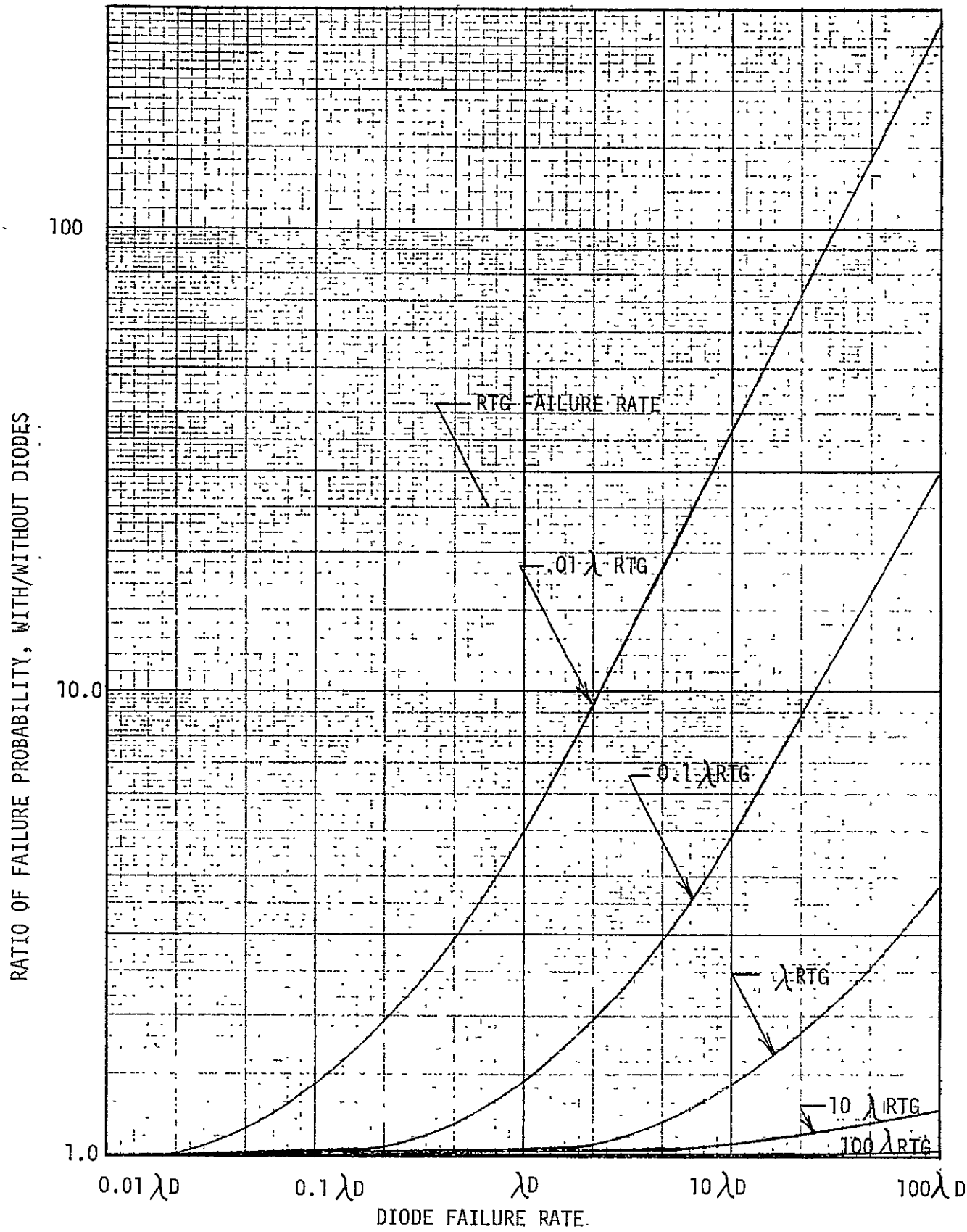


FIGURE D- 6 PROBABILITY OF LOSS OF ONE OUT OF FOUR RTG's

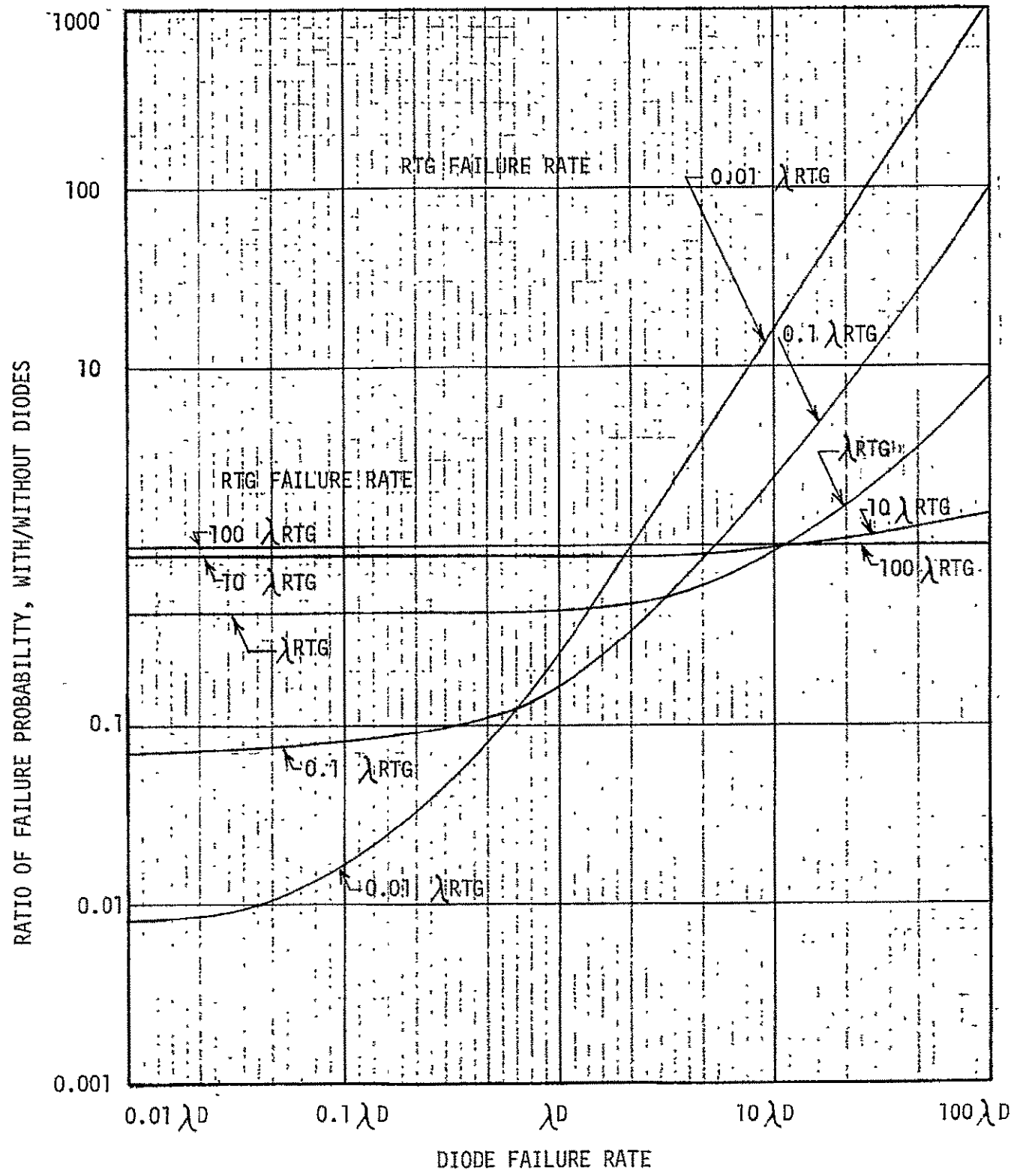


FIGURE D-7 PROBABILITY OF LOSS OF TWO OUT OF FOUR RTG's

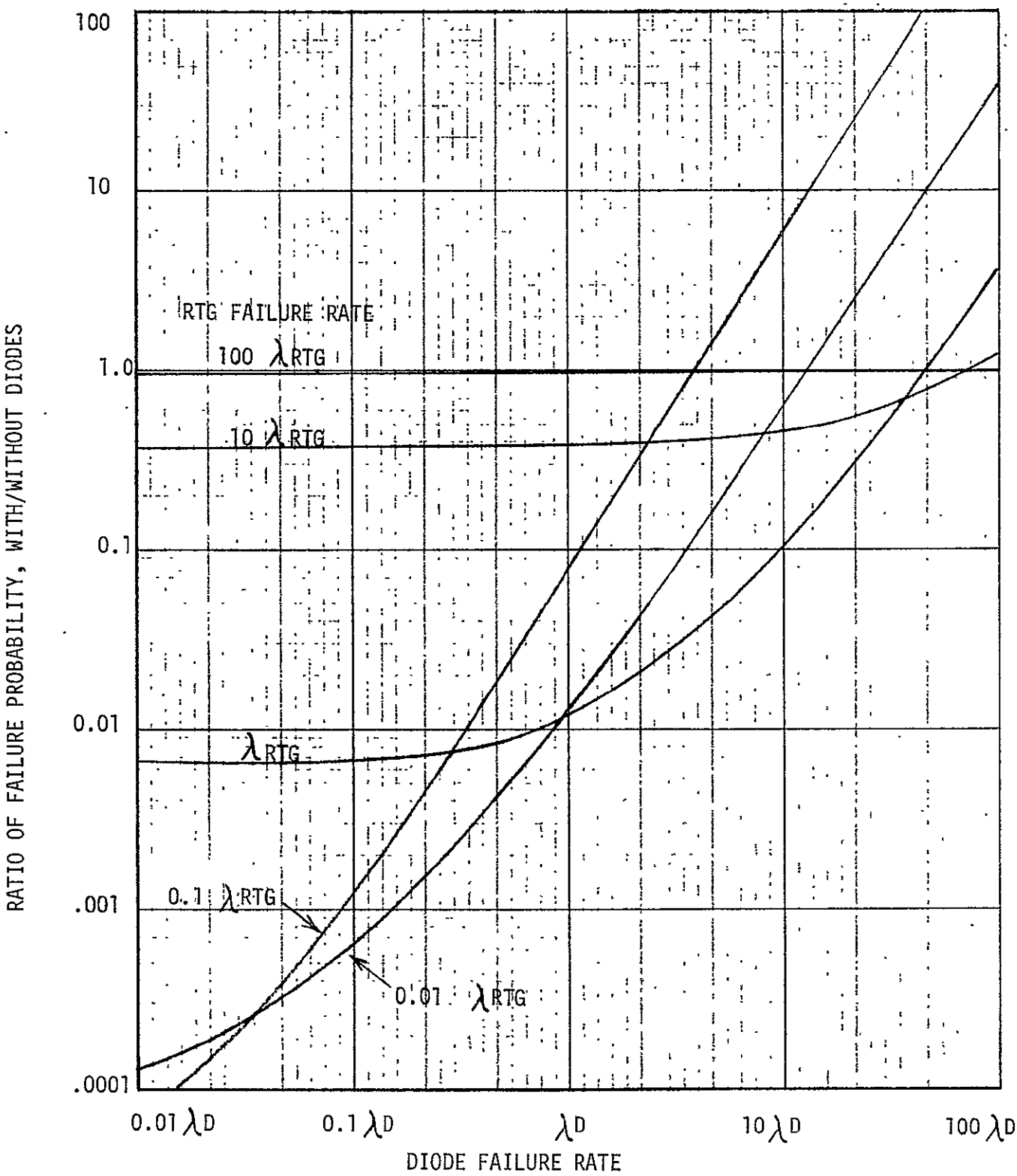


FIGURE D-8 PROBABILITY OF LOSS OF THREE OUT OF FOUR RTG's

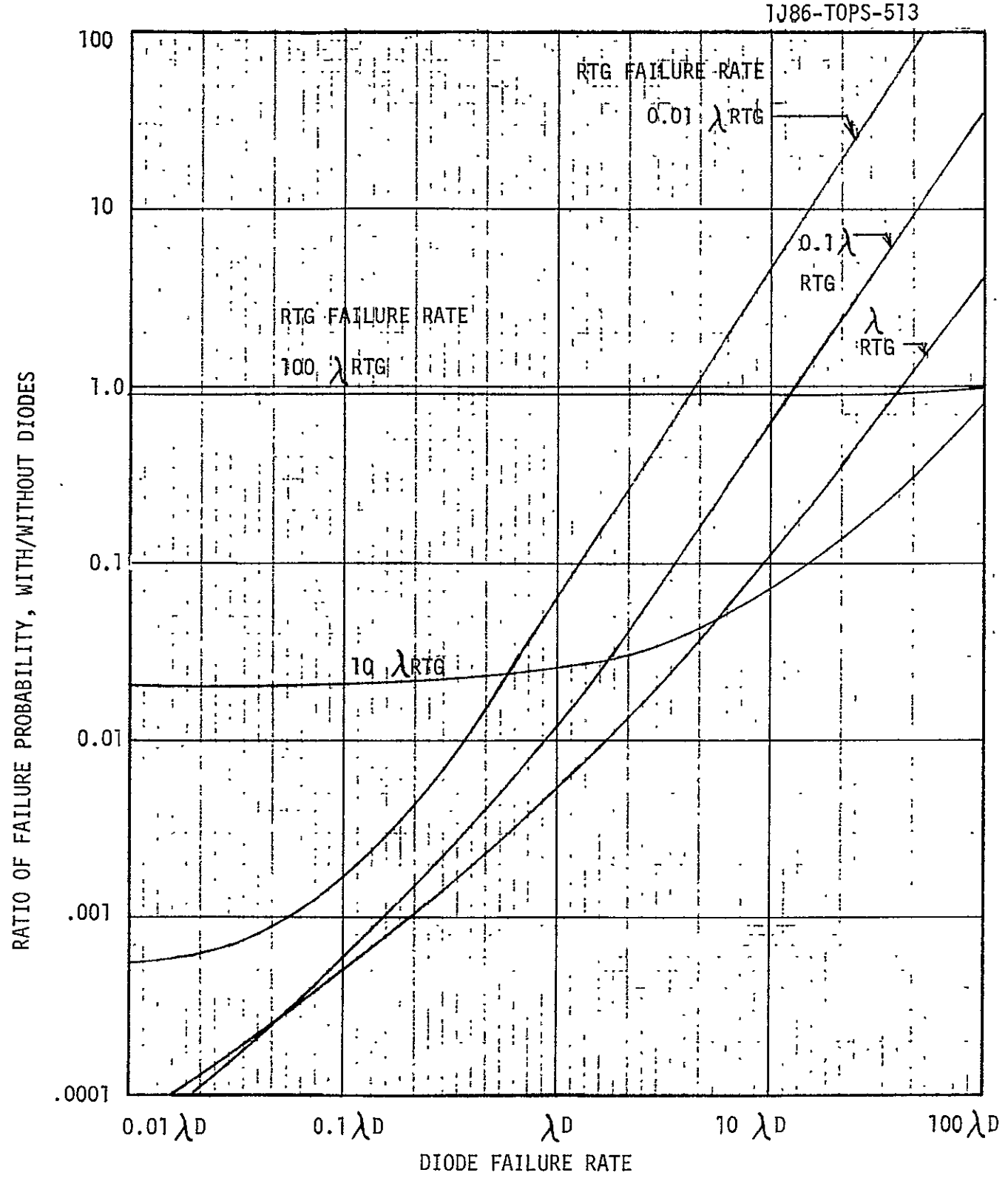


FIGURE D-9 PROBABILITY OF LOSS OF ALL FOUR RTG's

APPENDIX E EVALUATION OF ALTERNATIVE METHODS OF RTG VOLTAGE REGULATION

Four alternative methods of regulating or operating the RTG were examined. From the standpoint of efficiency, RTG transient response capability, and freedom from thermal cycling the RTG, the linear shunt regulator appears to be the better choice.

All RTG characteristics were based on data presented in Raag's memorandum. While the characteristics of the RTG design finally selected will differ from the data given, Raag's data should be sufficiently representative to allow meaningful comparisons to be made between the various regulation alternatives.

Maximum Power Point Tracking

The power output of an RTG is greater when it is new than when it is several years old. This increased power is available at a combination of voltage and current which changes as the RTG ages. A means of utilizing the extra power available when the RTG is new might be to use a voltage regulator which tracks the maximum power point of the RTG. An analysis was made to determine whether, in fact, any additional power could be obtained from the new RTG by allowing the RTG voltage to vary. A plot of the RTG power output versus voltage is shown in Figure E-1 for an RTG when new and when 12 years old. The curves indicate that, if a fixed RTG voltage is selected which is optimized for end-of-life, the loss in initial power capability will be less than 1%.

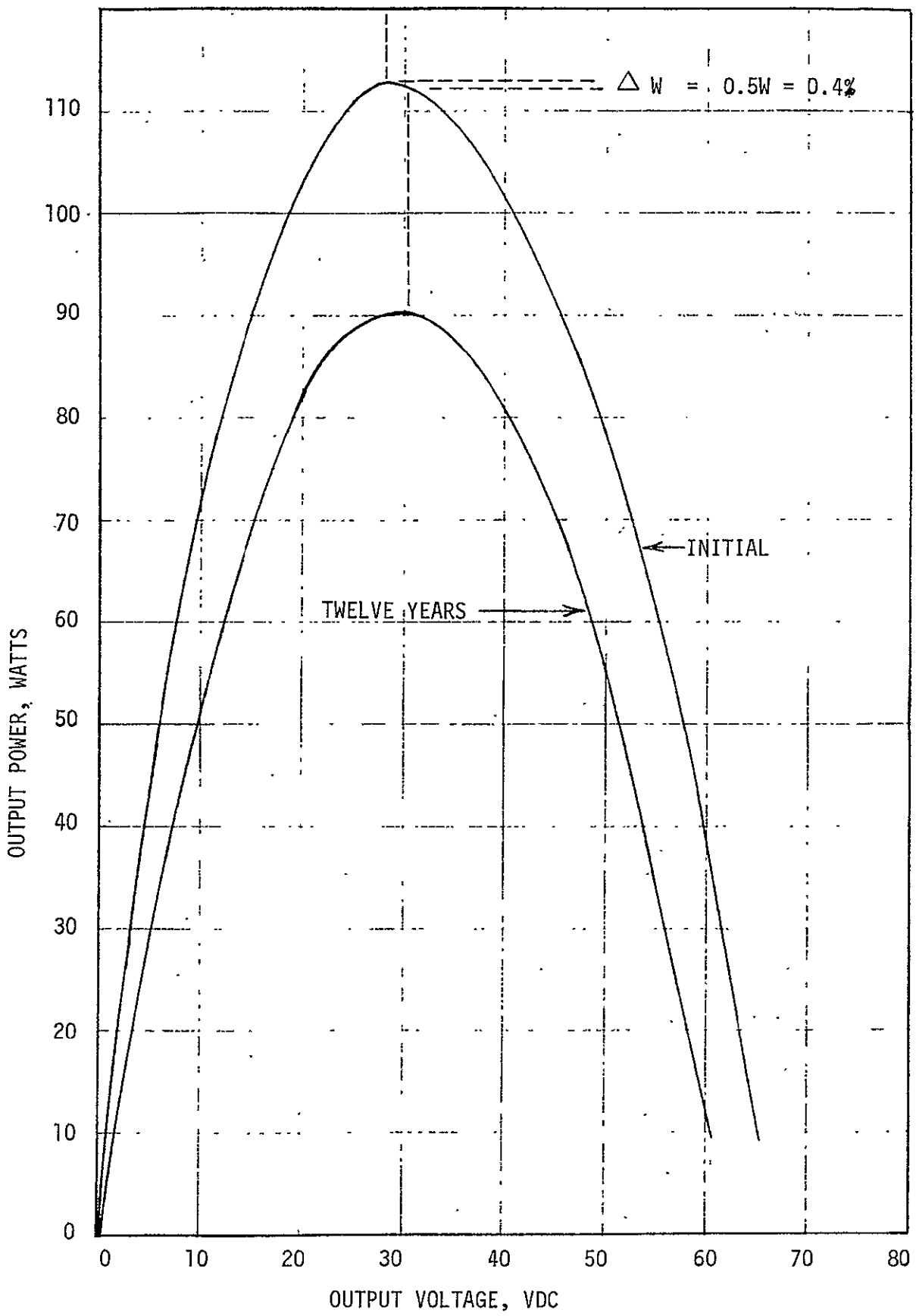


FIGURE E-1 RTG POWER-VOLTAGE CHARACTERISTIC

Thus, maximum power point tracking is not a favorable regulation approach, particularly when taking into account the additional complexity required, and the mandatory 6 to 8% in-line losses incurred to restore voltage regulation to the bus.

It is interesting to note that the initial maximum power point voltage is lower than the power point voltage at end-of-life.

Peltier Cooling

It has been suggested that the life of an RTG might be extended, or the rate of degradation of the thermoelectric elements reduced, by operating the RTG with a lower hot junction temperature. For a fixed RTG design, the hot junction temperature can be lowered under part-load conditions by withdrawing the power at lower voltages. The resultant higher currents will increase the Peltier cooling by the thermoelectric elements and lower the hot junction temperature. This method of operation requires an in-line boost regulator to produce a regulated bus.

The steady-state voltage-current (V-I) characteristics of the RTG are shown in Figure E-2, with transient V-I lines for several hot junction temperatures. As the operating point moves to lower voltages, the hot-junction temperature falls. The relationship between power and hot junction temperature is shown more clearly in Figure E-3.

Operation of the RTG in this manner is not without disadvantages. As the electrical load changes, the temperature of the RTG will change, and the resultant thermal cycling may accelerate the degradation of the RTG.

Furthermore, the reduced hot junction temperature at low load will cause a

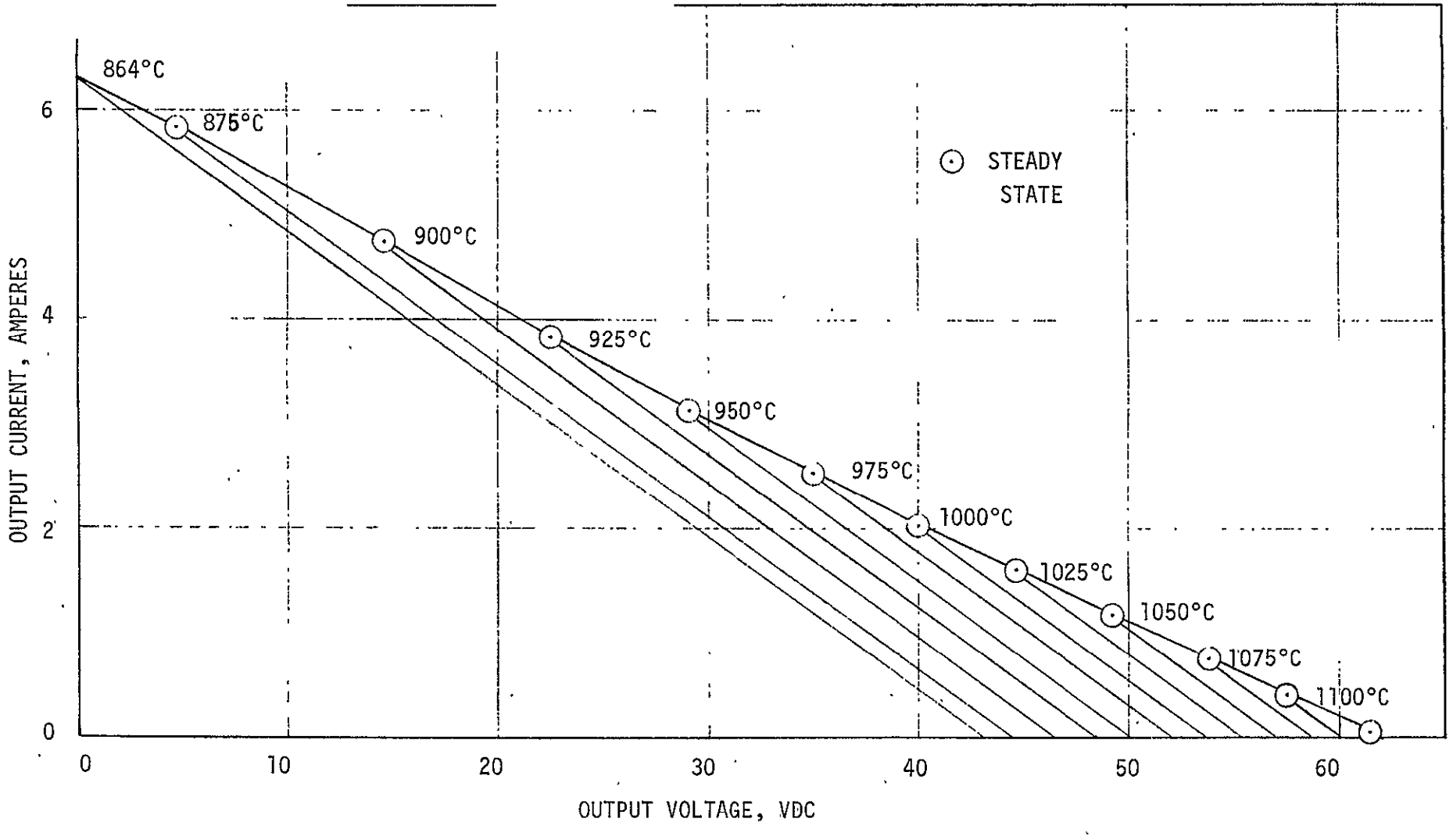


FIGURE E-2 TEMPERATURE EFFECTS ON VOLT-AMPERE CHARACTERISTICS

1J86-TOPS-513

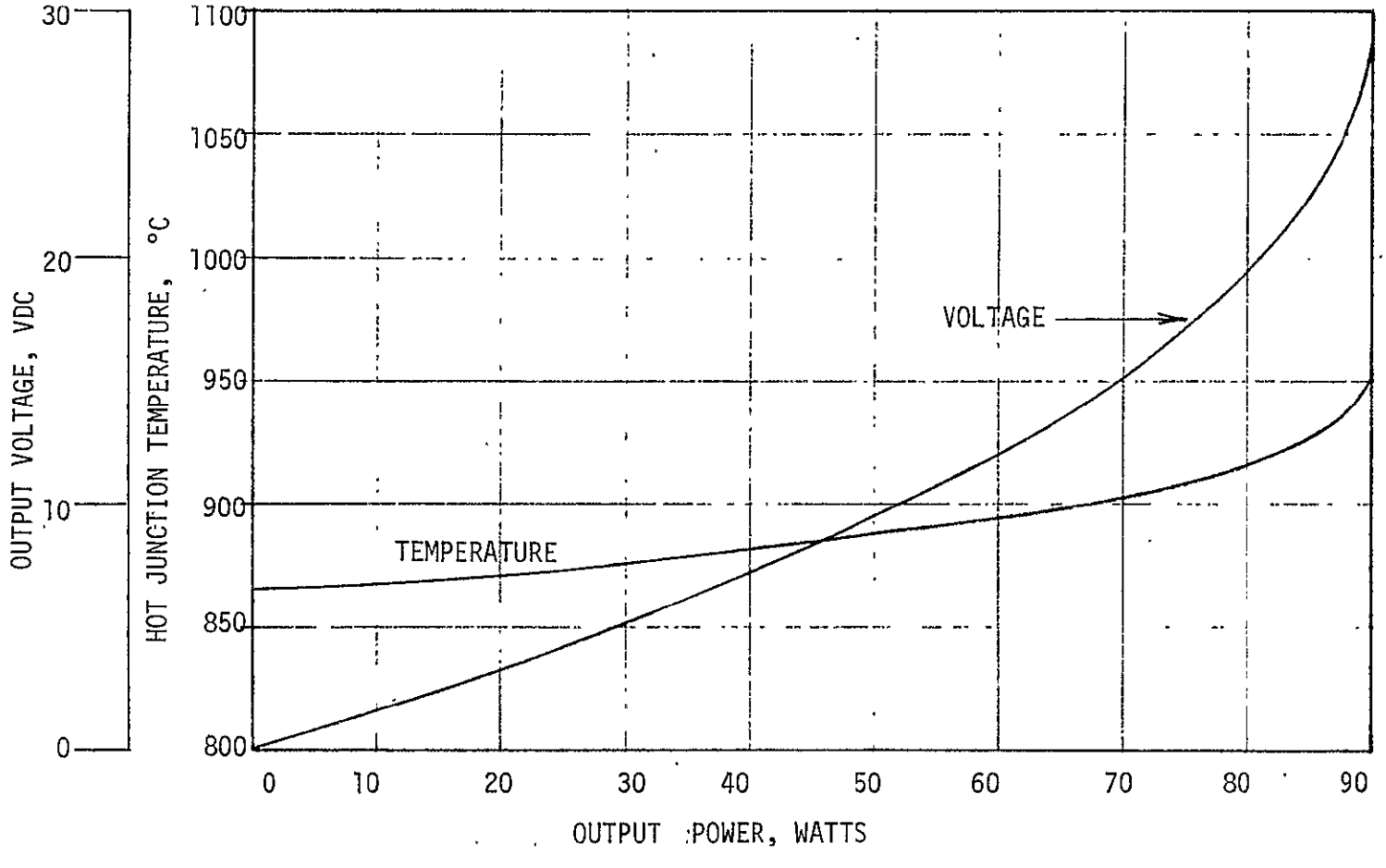


FIGURE E-3 VOLTAGE AND TEMPERATURE EFFECTS

significant reduction in the transient power capability when full load is required. When the RTG has cooled to its new lower hot junction temperature, increases in power demand will cause the operating point to rise along the transient V-I line corresponding to that temperature, which is lower than the steady-state V-I curve. This reduction in transient power capability is shown in Figure E-4. For example, assume that a 100-watt RTG is operated at 50 watts. When full load is called for, only 82 watts will be immediately available, until the RTG heats up to its normal operating temperature again.

This effect alone is sufficient reason to discontinue further consideration of this method of operation. The power loss of 6 to 10% and the complexity of the inline boost regulator are additional negative factors to consider.

Switching Shunt Regulation

The effect of a switching shunt regulator on RTG operation was studied. The switching shunt (Figure E-5) shorts the output of the RTG on a duty-cycled basis. Power is drawn from the RTG at a voltage higher than the regulated bus voltage, and the filter averages out the voltage. The operating points of the RTG alternate between Point A and Point S. By switching to the short circuit current point (S), a high current is maintained on the RTG even at no useful load, and this limits the excursion of the hot junction temperature.

An approximate analysis, the elements of which are shown in Figure E-5, indicates that, regardless of the load, the time-averaged current output of the RTG is constant, just as for the linear shunt. Thus, the Peltier component of cooling should remain constant.

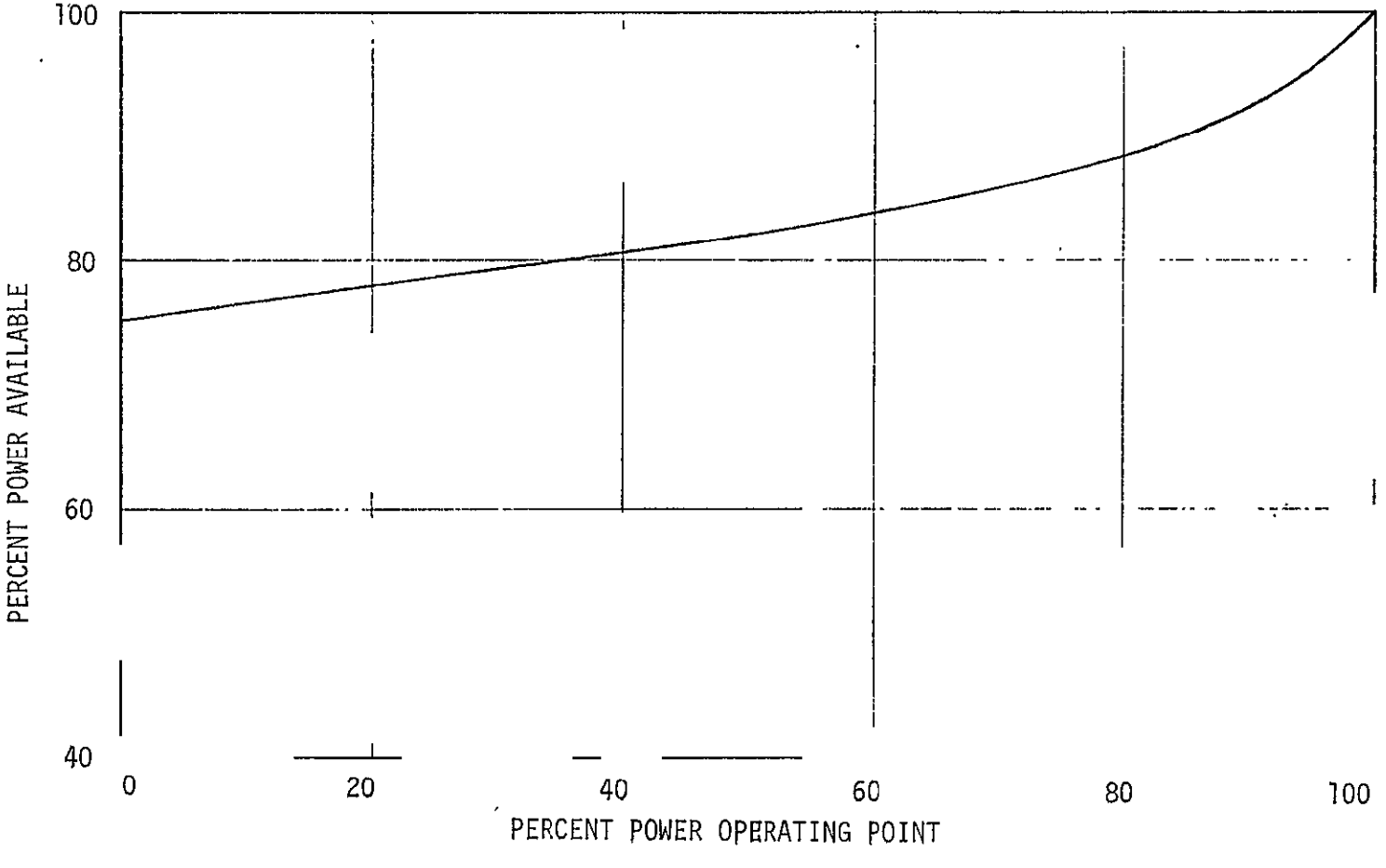


FIGURE E-4 REDUCED TRANSIENT POWER CAPABILITY

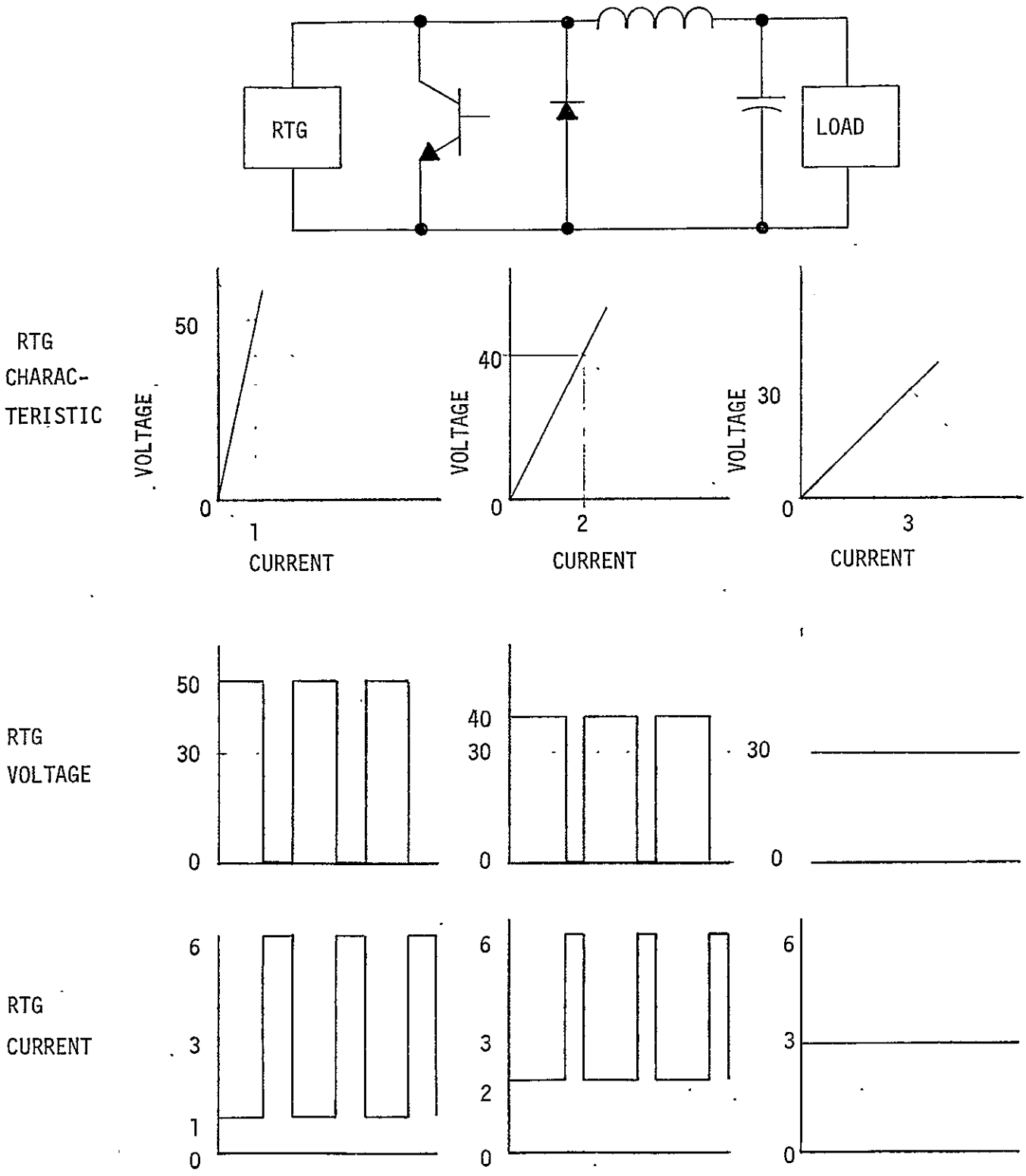


FIGURE E-5 RTG-LOAD RELATIONSHIPS

In the above analysis it was assumed for the sake of simplicity that the hot junction temperature remained constant. However, at part load the hot junction temperature will increase to some extent. Some linear approximations were made to determine this temperature variation. The two equilibrium hot junction temperatures were found which corresponded to the current of each of the two operating points (Point A and Point S), and these were averaged, weighted by the duty cycle. The results are presented in Figure E-6, indicating a rise of about 60°C in the hot junction temperature at no load. The temperature increase is expected to be slightly less when predicted by a more precise analysis taking nonlinear effects into account.

The major advantage of the switching shunt is that the heat load in the shunt regulator is relatively constant, independent of the varying spacecraft load. Whether or not this is an advantage to TOPS has not been demonstrated, as the dissipation in the linear shunt may be used constructively to stabilize the spacecraft thermal balance.

There are disadvantages to the switching shunt. The in-line filter introduces about 2 to 3% loss, and there are switching and drive losses in the switching circuit. A major problem is introduced in the area of EMI since double the RTG rated current must be switched by the switching shunt. In TOPS, this switched current is carried from the RTG's by long lines, which effectively act as large radiating antennas.

In addition, the switching shunt violates the allowable ripple current specified for the RTG, although the effect of the ripple and the need for an RTG ripple current specification has not been definitively established.

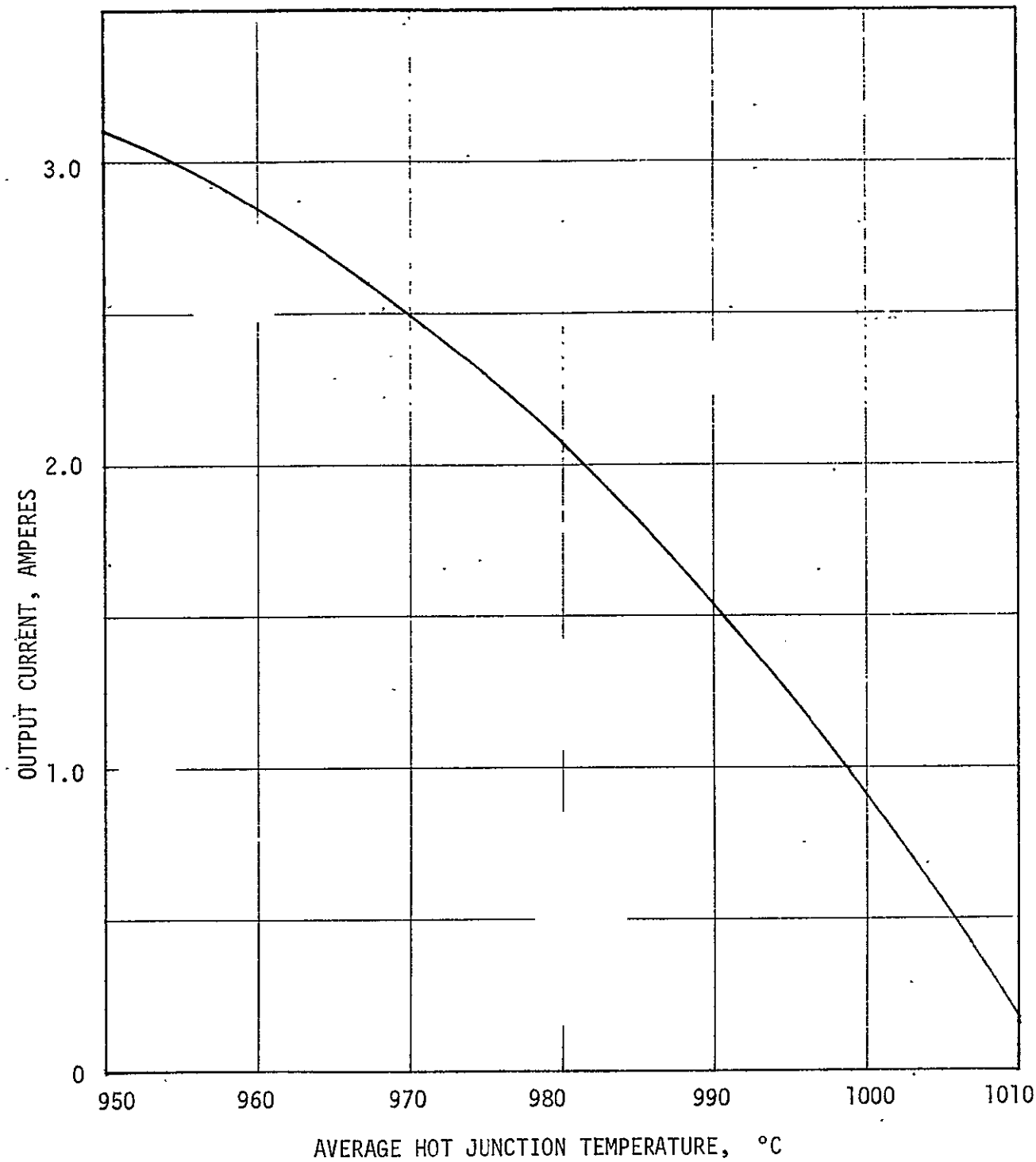


FIGURE E-6 RTG TEMPERATURE WITH SWITCHING

Because of the EMI problem, and because the losses at full load are higher for the switching shunt than for the linear dissipative shunt, it is recommended that the switching shunt regulator not be considered further.

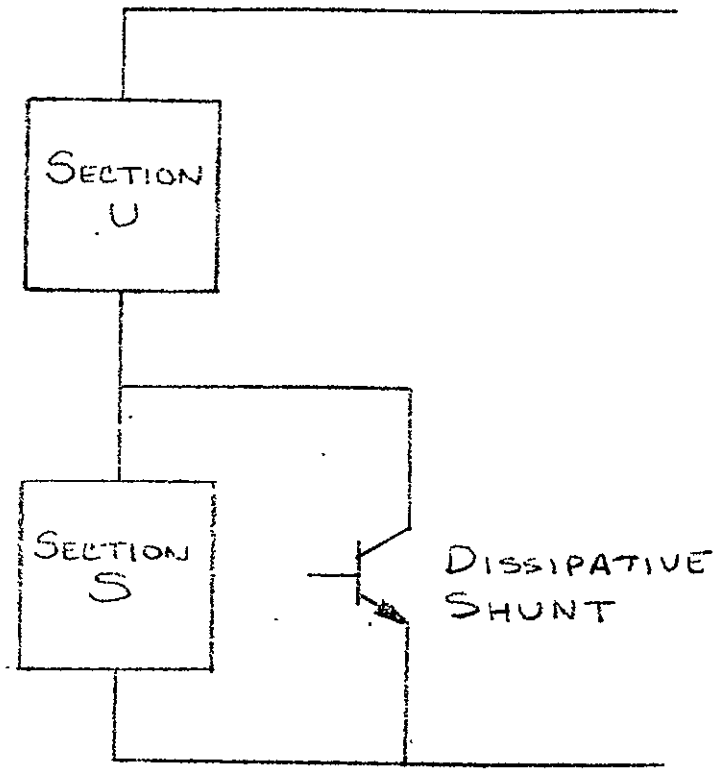
Partial Shunt Regulator

The functional arrangement of the RTG and partial shunt regulator is shown in Figure E-7. It is obvious from this sketch that alterations to the internal design of the RTG must be made to accommodate the partial shunt. The string of thermoelectric elements must be tapped at an intermediate point and extra leads brought out. Good thermal coupling should be provided between the hot junctions of the two RTG sections.

The thermal dissipation in the dissipative shunt element is shown as a function of load current in Figure E-8. Constant hot junction temperature was assumed. The maximum shunt dissipation is 33 watts, compared to 90 watts for a full shunt, so there is a reduction in the on-board power dissipation.

The shunt tap was arbitrarily set at the center of the string of elements. By adjusting the shunt tap lower in the string, the dissipation will be reduced further. The optimum tap location is a function of the minimum load and the maximum voltage characteristics of the unshunted portion of the RTG.

Problems result if good coupling is not provided between the two sections of the RTG, as shown in Figure E-9. With perfect thermal coupling between the shunted and unshunted sections the hot junction temperature will rise about 45°C from full load to no load. If there is no coupling, the hot junction temperature will rise about 180°C in the unshunted section at no load. It is



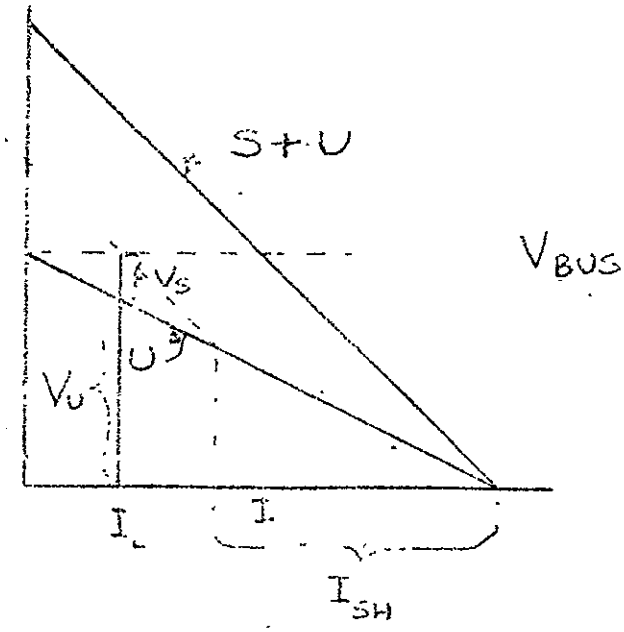


FIGURE E-7 PARTIAL SHUNT REGULATOR

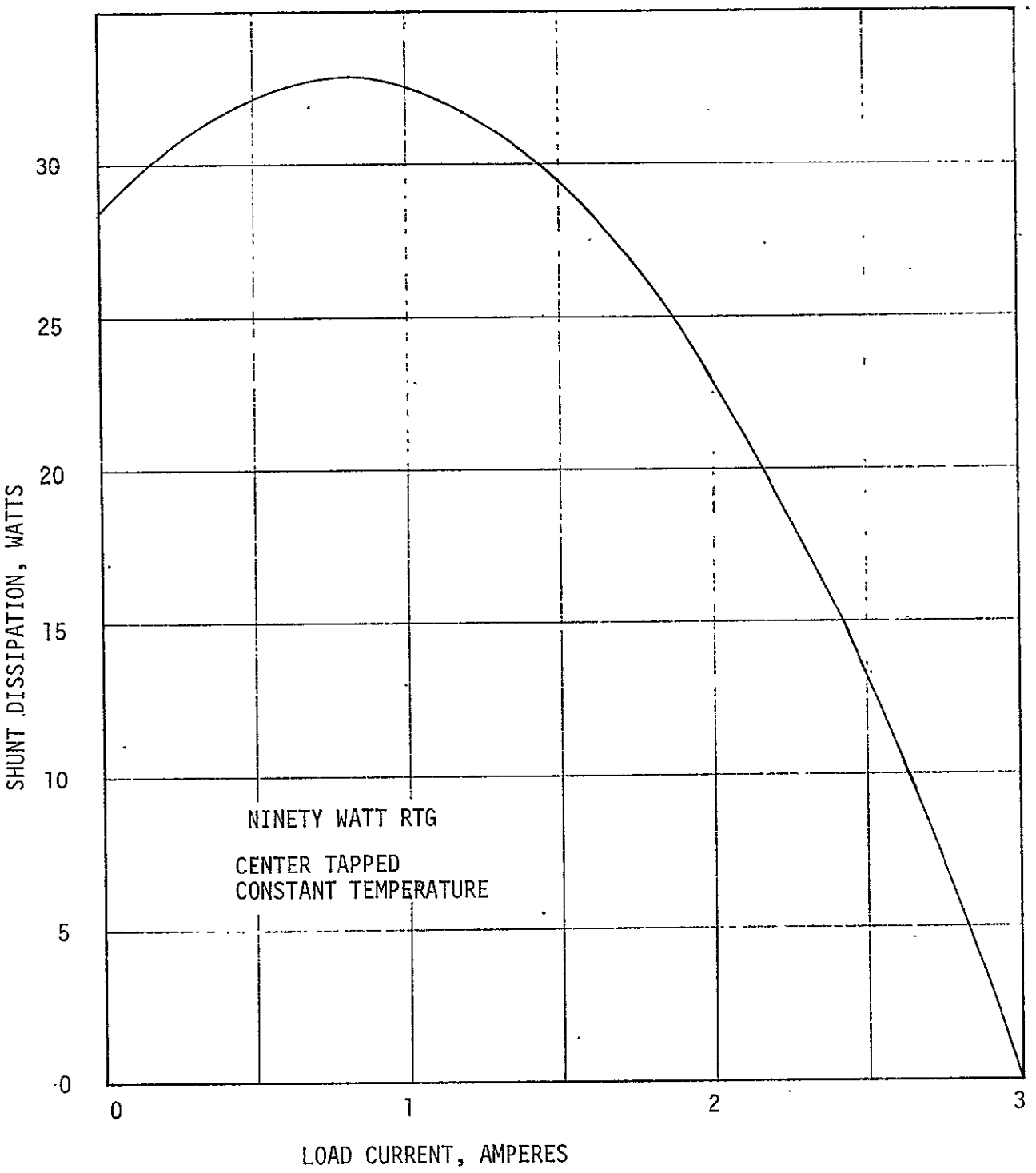


FIGURE E-8 PARTIAL SHUNT REGULATOR DISSIPATION

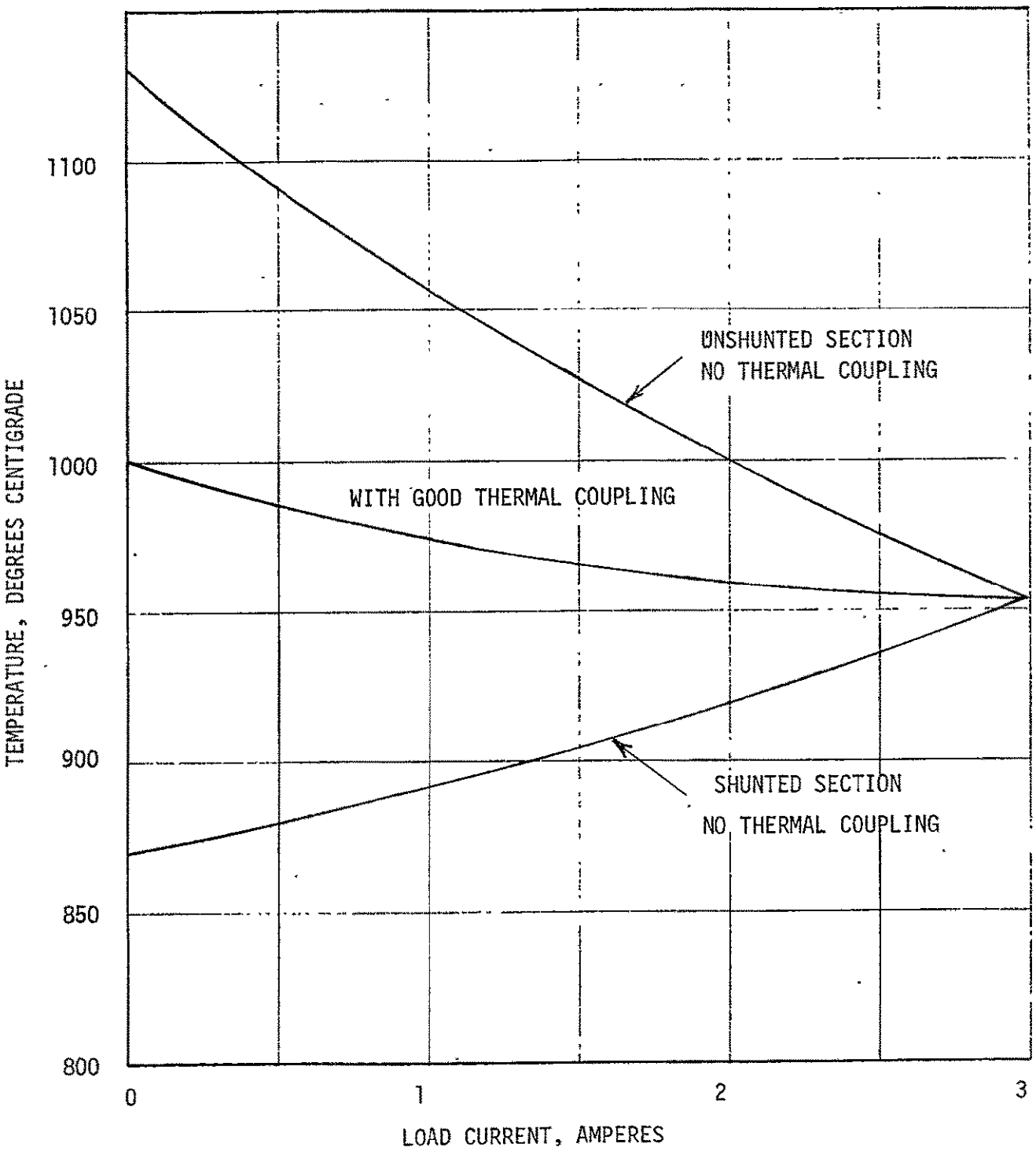


FIGURE E-9 PARTIAL SHUNT JUNCTION TEMPERATURES

believed this will increase the rate of thermoelectric element degradation, as well as induce stresses due to differential thermal expansion. In addition, elements with the RTG will undergo thermal cycling as the load varies, the one section of the RTG expanding while the other section contracts.

During the Task C RTG studies for the Voyager program a partial shunt regulator was recommended to reduce the thermal dissipation in the shunt elements. The partial shunt concept could satisfactorily be applied since the proposed RTG design used a hot frame which provided good heat transfer between the hot junctions of shunted and unshunted sections. However, the concept presently evolving in the Multi-Hundred Watt RTG study does not utilize a hot frame, and the radiative view factors between the various modules of the RTG will be severly limited by the internal geometry of the generator. It therefore appears that, for the RTG design planned to be available for TOPS, there will be relatively poor thermal coupling between the various sections of the RTG. As a consequence of this, if a partial shunt regulator were to be used, the unshunted section of the RTG would rise to high temperatures during periods of low load. Since this would most likely have an adverse affect on the RTG degradation rate, it is not recommended that a partial shunt regulator be selected for use on TOPS.

APPENDIX F. THERMAL CHARACTERISTICS OF SHUNT REGULATOR ELEMENTS

Introduction

A preliminary evaluation has been made indicating the physical requirements of fins necessary to radiate expected heat loads from transistors at peak power.

ASSUMPTIONS

Peak transistor power:	29.2 watts
Transistor type:	T063 case
Transistor Mounting area:	0.60 square inches
Resistance from junction to case:	1°C/watt

Transistors were assessed to have a beryllium oxide washer (1/16" thick) between the case and the mounting plate. The contact conductance at each interface, case to washer and washer to plate, was taken as 2.85 watt/cm^2°C. Thus, the entire resistance from junction to base was 1.17°C/watt, where base consists of the plate area directly below the transistor.

Radiation losses from fins or plates were assumed to develop from one side only, that facing space (T=0°K). A louver system, which controls the effective emittance of the plate outer surface as a function of its temperature, was assumed to be required for the system. The effective emittance used for radiation was taken as 0.67, which corresponds to the emissive capability of fully open louver blades.

Three transistors are assumed situated on a 14 x 16 x 1/16 inch available radiator plate; the transistors are positioned in such a manner as to obtain the maximum radiating efficiency, i.e., each is situated away from the plate edges and not too near each other.

Results

First, required transistor base temperatures were obtained as a function of transistor heat load and maximum allowable junction temperature. Results are presented on Figure F-1. Secondly, the allowable transistor power which can be radiated from 1/3 the plate area was determined for a given range of transistor base temperatures (See Figure F-2). The fin or plate effectiveness was calculated for each base temperature (equivalent to fin root temperature) together with other fin parameters. The capability of an isothermal plate has also been shown in Figure F-2 for comparison purposes.

Both Figures F-1 and F-2 are used together to determine the allowable heat load per transistor for a given maximum junction temperature. A given heat load is assumed in Figure F-1, and the corresponding required transistor base temperature (at some maximum junction temperature) is obtained on the ordinate. Enter Figure F-2 with this temperature, and read the corresponding allowable transistor heat load or power. Then iterate with the figures until the transistor base temperature and the heat load agree on both figures.

Results show that a power of 29.2 watts/transistor cannot be rejected if the maximum allowable transistor junction is 100°C, even in the isothermal plate condition.

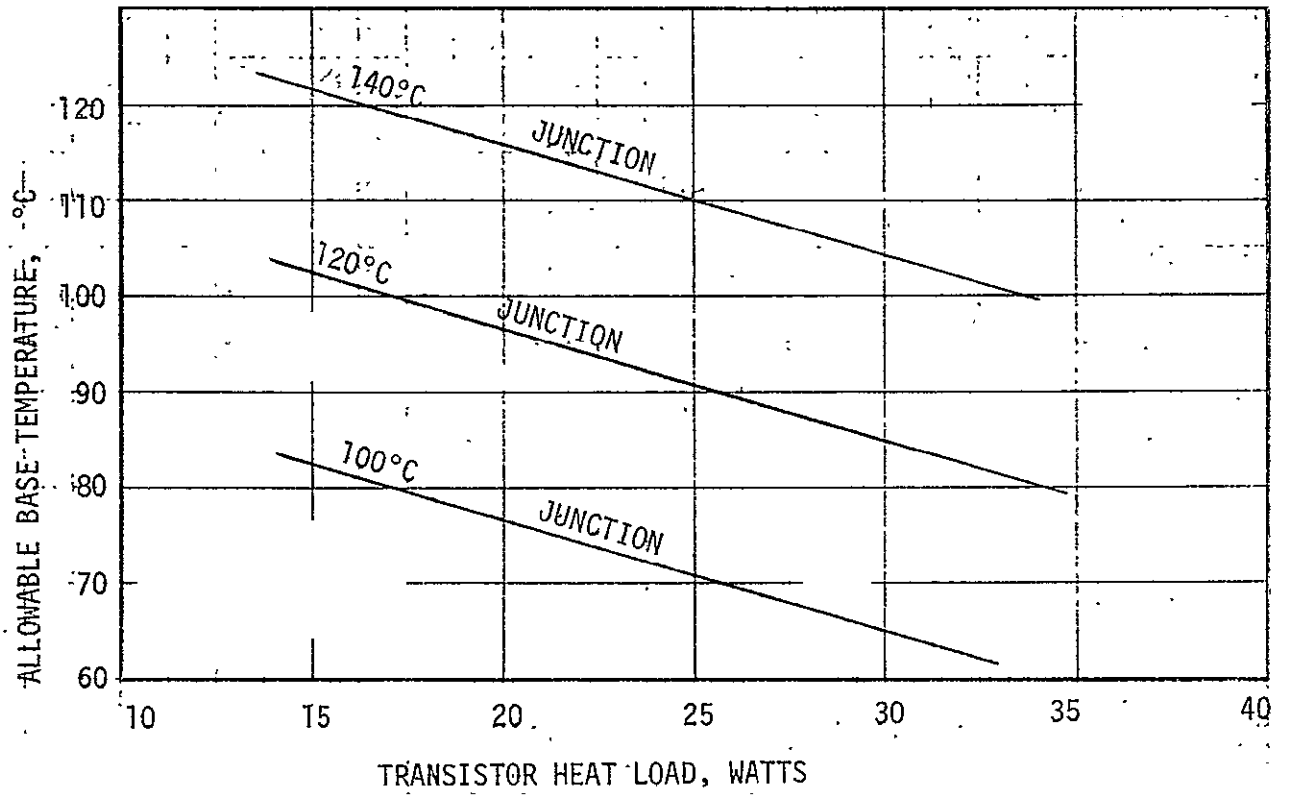


FIGURE F-1 TRANSISTOR JUNCTION TEMPERATURE

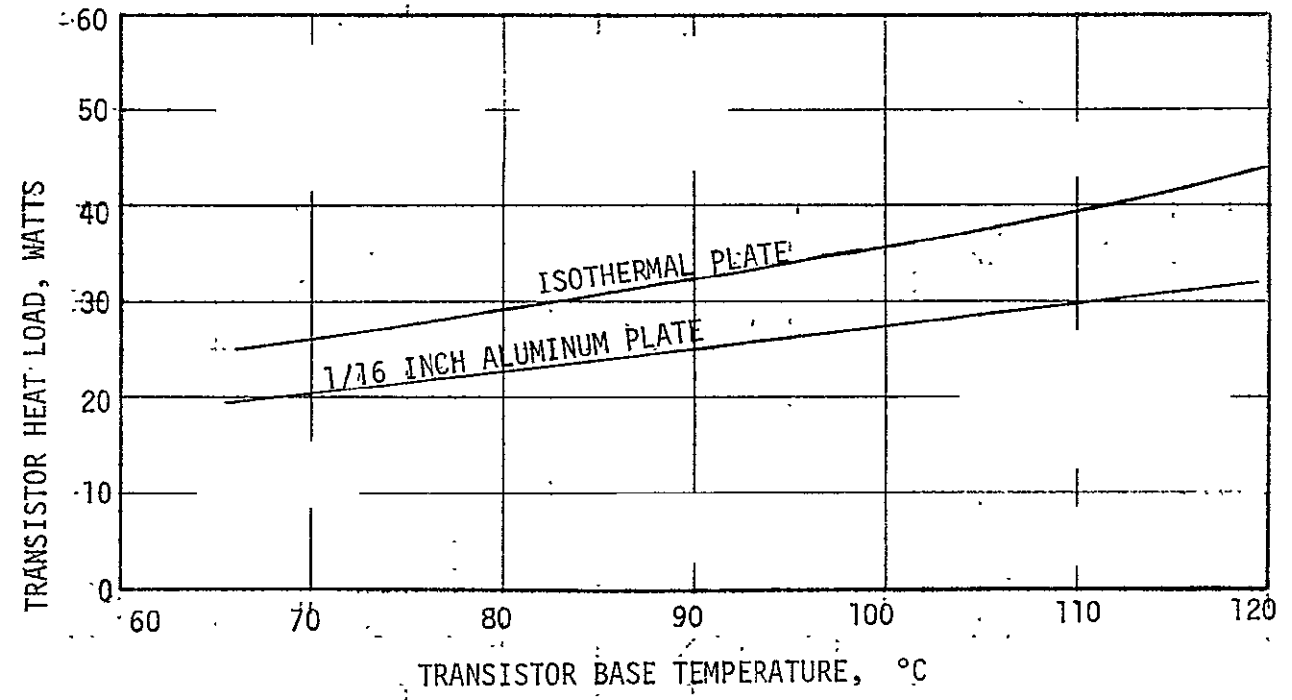


FIGURE F-2 TRANSISTOR SINK TEMPERATURE

The effectiveness of a radiating plate with a circular heat source, i.e., transistor, will be less than one. The effectiveness is the ratio of Q/Q_{max}, where Q is the actual heat loss from a real fin and Q_{max} the heat loss from an isothermal fin (the temperature at the transistor base exists throughout the entire fin).

Figure F-3 has been drawn to show that a minimum weight can be found for a fin capable of radiating the 29.2 watts dissipated by the transistor. Fin areas and thicknesses are shown as a function of fin weight.

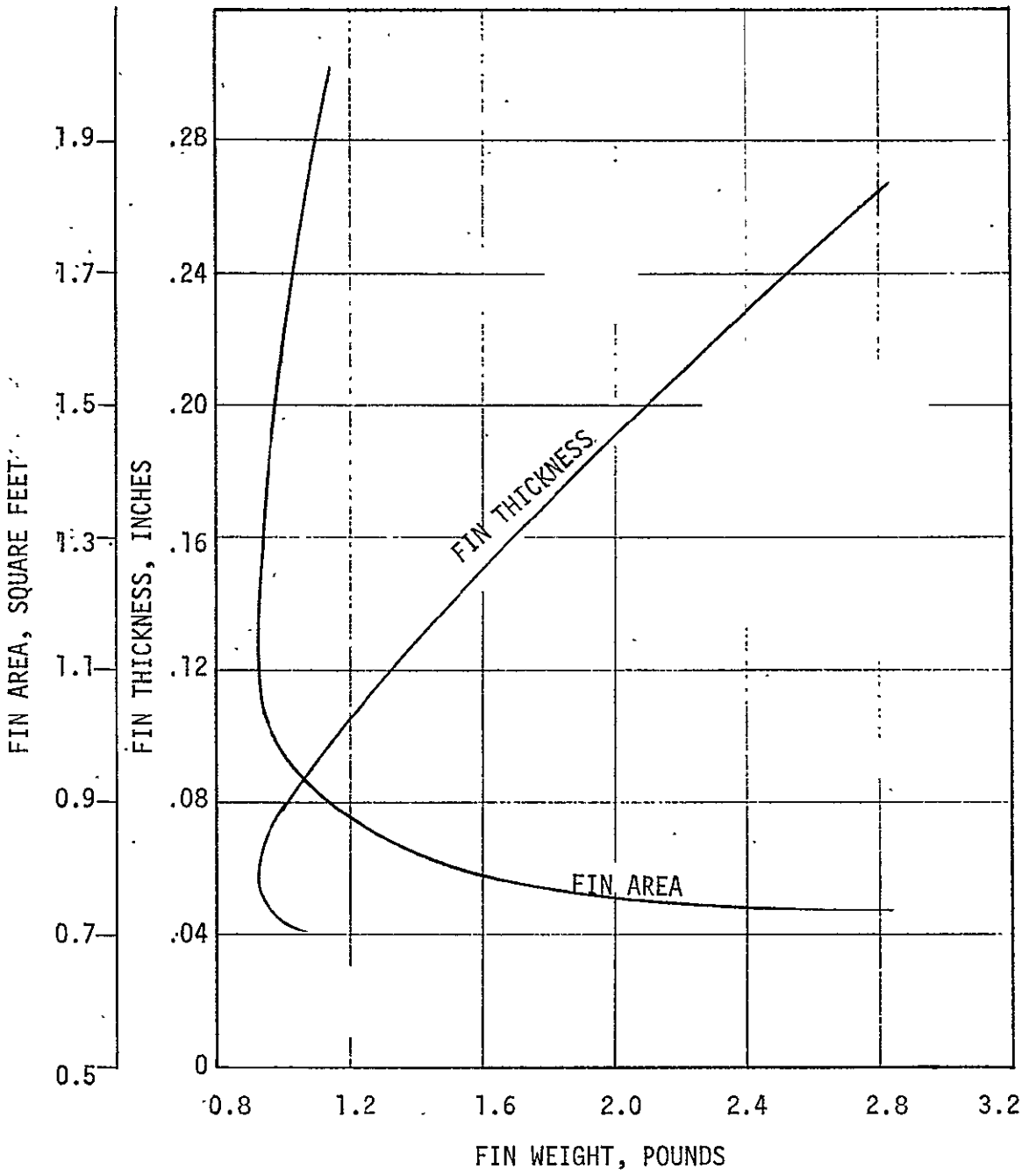


FIGURE F-3 RADIATION FIN REQUIREMENTS

APPENDIX G POWER SWITCH CONFIGURATIONS

Introduction

The primary function of the Power Control Switch is to turn on and to turn off spacecraft loads when an electrical signal is received from the flight command subsystem. Additional desirable attributes are to protect the spacecraft electrical power bus from load faults, to trip automatically on overload, to recycle automatically after trip, to be reset by command, and to control the rate of change of current to the load both at turn-on and at turn-off.

The purpose of the current limit is to isolate a faulted load from the bus and reduce the electrical power margin required within the power subsystem, and also serve as a limit on current surges at turn-on associated with charging filters. The overload trip should operate on an integrated ampere-squared-second time delay to protect semiconductors and to avoid nuisance trips. This controls the energy drawn from the spacecraft bus in the event of a sustained overload. A monostable timing circuit can be used to create a preset fixed time delay after which the load can be reapplied. If the fault persists, the overload trip will operate and reset the monostable. The tripped circuit can be reset earlier, or the timing circuit can be shut down prematurely by command. Control of current rise and fall times is desirable to reduce voltage transients on the wire feeding the load, and to prevent dynamic loss of regulation at the main bus regulator due to rapid load changes.

The following discussion provides some pertinent features of three switch circuits presently under consideration, and identifies some objectives of the immediate future, and indicates how many of the desirable features can be achieved.

Quad Solid State Switch

This circuit employs a quad transistor switch arrangement to provide redundantly both the make and break functions. The on/off control of the power switches is also quad redundant so that no single failure in the switch portion of the switch (right half of the schematic of Figure G-1) will prevent turning the load on or off.

The command portion of the circuit shown (left half of the schematic) is a toggle command receiver having a primary and a backup input. Both command inputs require a 25 to 125 millisecond command pulse duration. The primary input would be current drive to the light emitting diode of the TIXL103. The backup command is accomplished by grounding the open end of the 7.5 kilohm resistor just below the TIXL103 for the duration of the command. The backup interface is compatible with the "universal isolated switch" schematic provided by JPL.

The voltage drops at different temperatures and currents for this switch are shown in Figure G-2, "Steady State Voltage Drop versus Temperature" and Figure G-3, "Quad Transistor Switch Voltage Drop versus Temperature." Also presented are the worst voltage drops for a single pair (i.e., Q4, Q5; and Q10, Q11: or Q6, Q7; and Q12, Q13) of the transistors carrying the load, simulating the loss of half the switch due to a failure. The

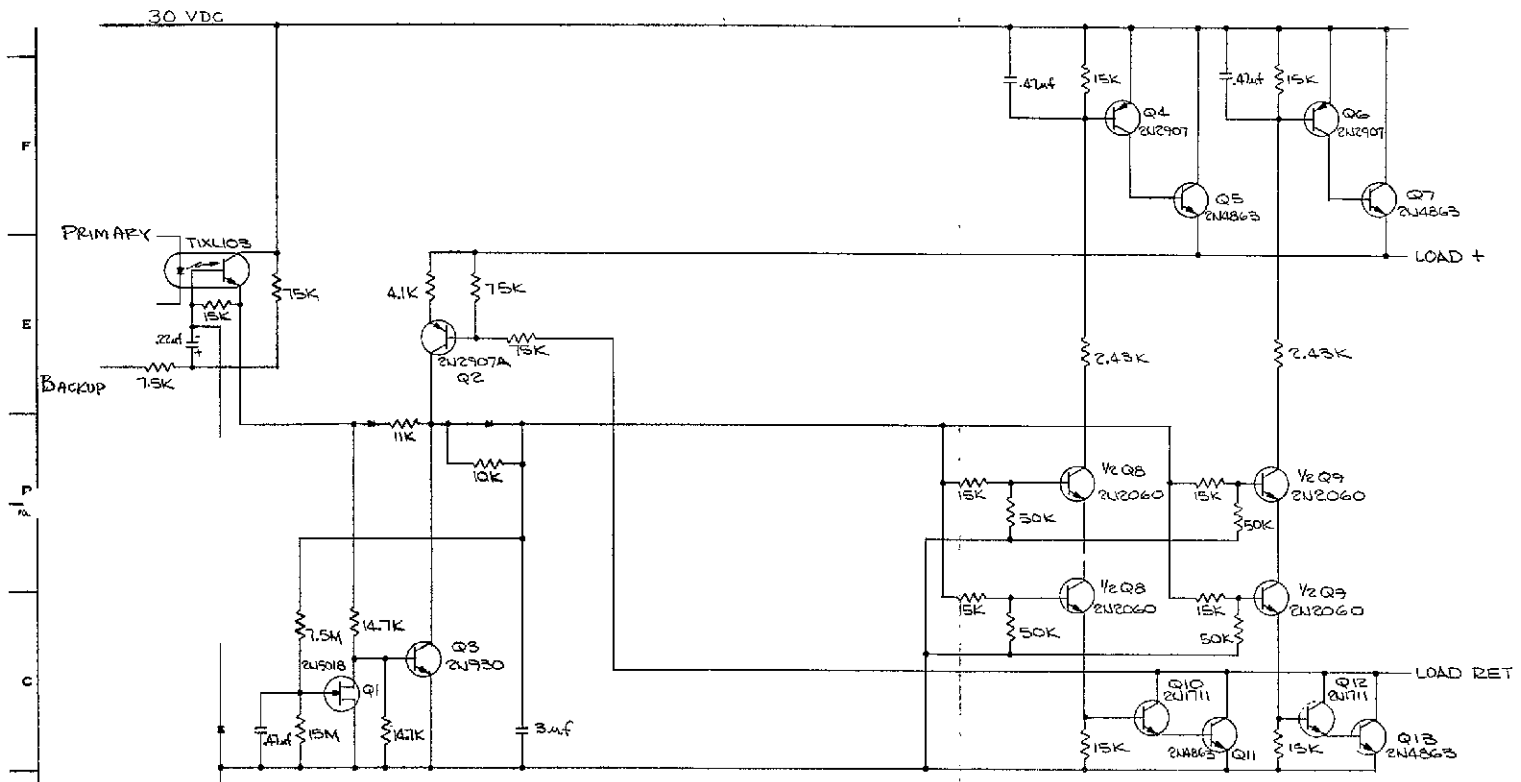


FIGURE G-1 QUAD SOLID STATE SWITCH SCHEMATIC

FOLDOUT FRAME 1

FOLDOUT FRAME 2

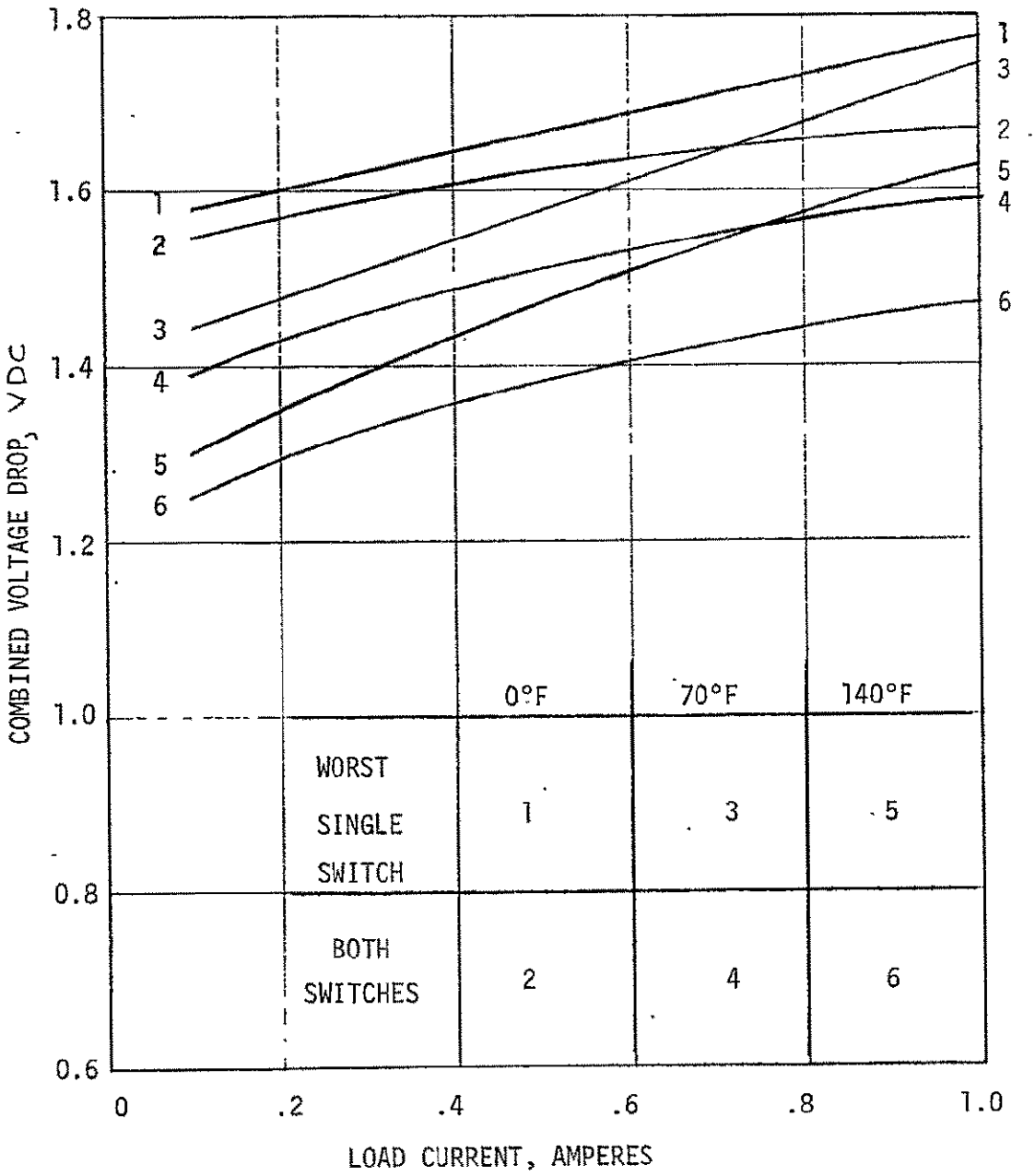


FIGURE G-2 SOLID STATE VOLTAGE DROP

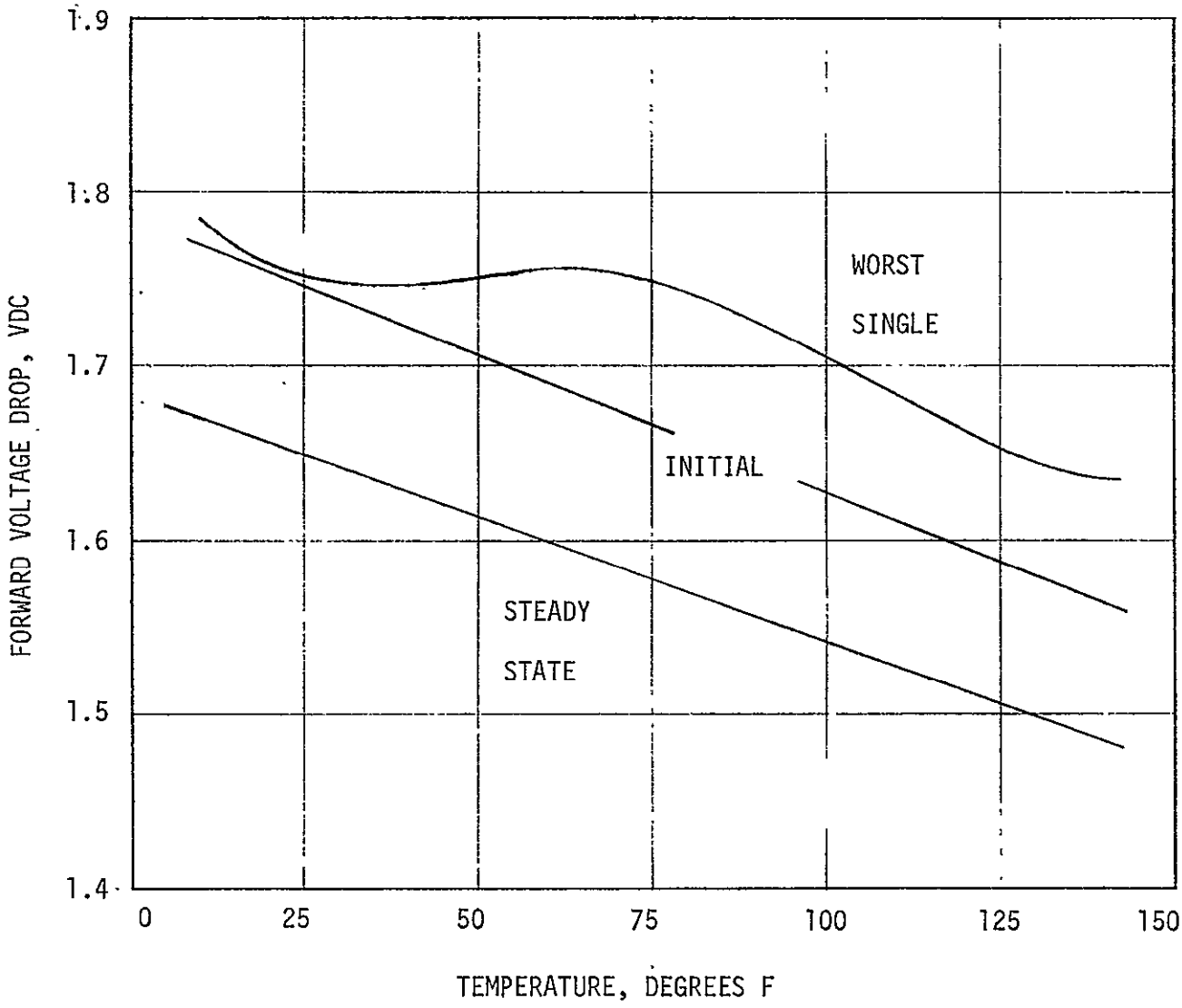


FIGURE G-3. QUAD TRANSISTOR SWITCH VOLTAGE DROP

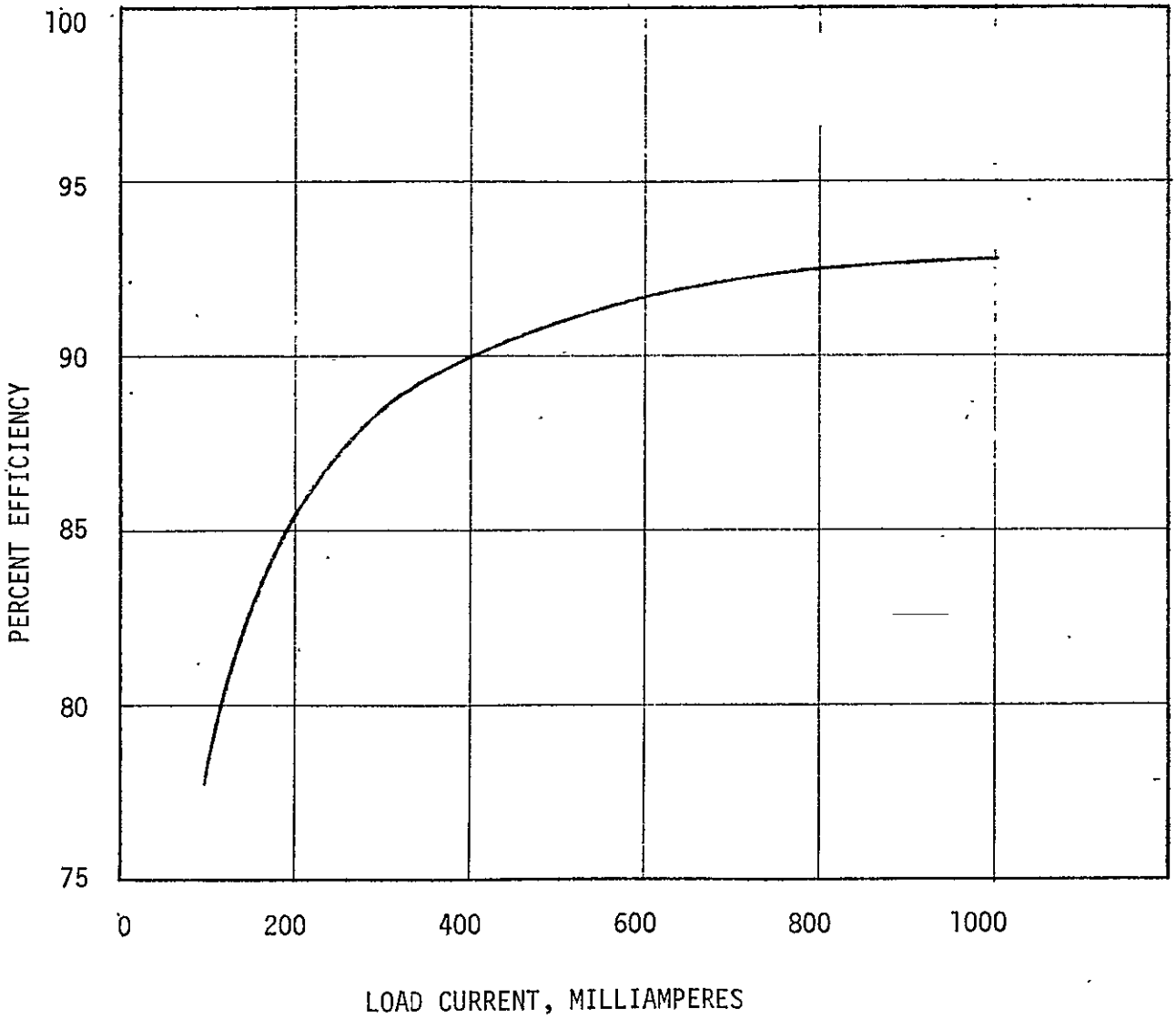


FIGURE G-4. QUAD TRANSISTOR SWITCH EFFICIENCY

"initial" curve shown in Figure G-3 is the drop when the circuit is first turned on at the indicated temperature, and the "steady state" curve is after at least five minutes of operation. The voltage drop and drive loss were used to compute power loss and the corresponding efficiencies plotted on Figure G-4, "Quad Transistor Switch Efficiency". The switch as shown would not be used for loads less than one half ampere, since the gain for an output from one hundred to five hundred milliamperes would be too low. However, the drive and output transistors could be tailored to any particular load from seven hundred milliamperes to two amperes. For a flight switch a stud mounted transistor would probably be used where the 2N4863 is shown for any load greater than seven hundred milliamperes.

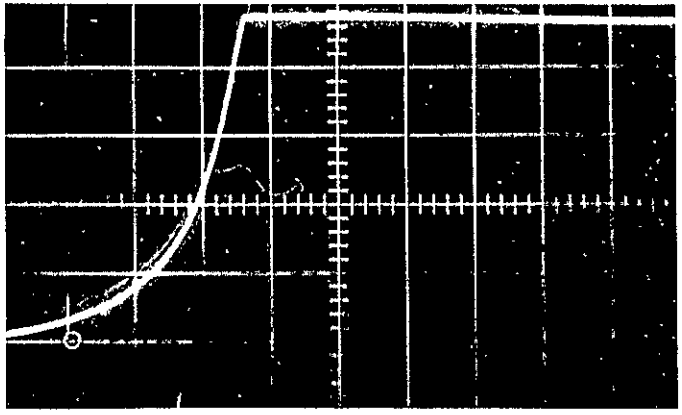
This circuit also provides controlled current rise and fall times, and photographs are shown on Figures G-5 and G-6; and a graph of $di/_{dt}$ is displayed on Figure G-7. The standby power (load off) of this circuit is negligible.

Redundant Toggle Switch

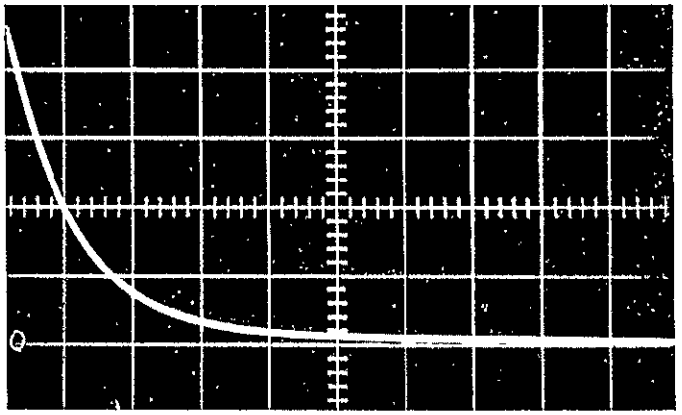
The circuit shown on Figure G-8 is a quad redundant switch. Both the prime and backup commands toggle the circuit. The expected command is a 25 to 125 millisecond pulse. Every time either the prime or backup command is received, the circuit changes state. If a prime and a backup command are received simultaneously, the output remains the same but will see a transient as both relays change state.

The command inputs are DTL, TTL levels, where the high input (+4.5 VDC) represents no command. This polarity was assumed so that the effect of harness

0.1
AMPERES

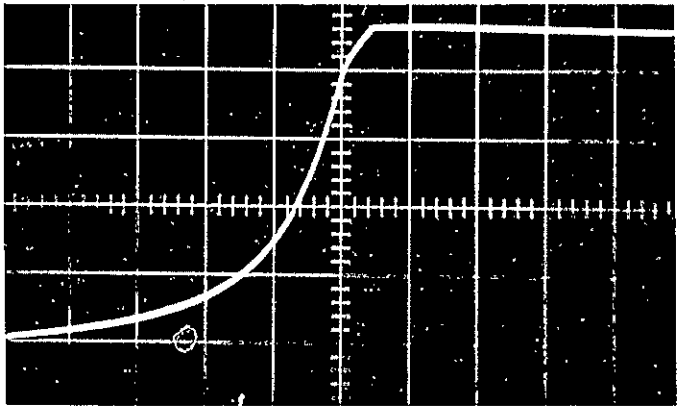


RAMP ON, 0.2 MILLISECONDS/CM

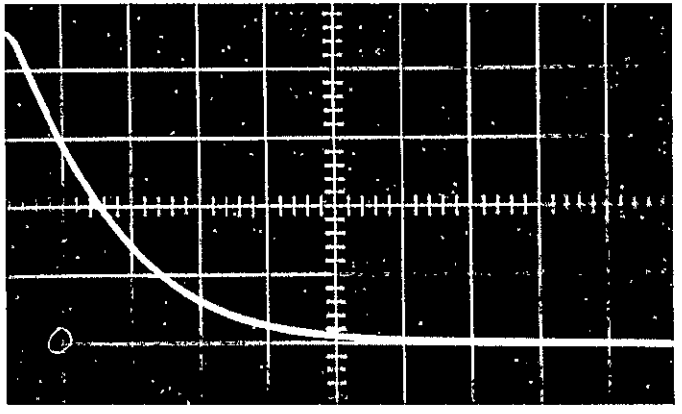


RAMP OFF, 1.0 MILLISECONDS/CM

0.5
AMPERES



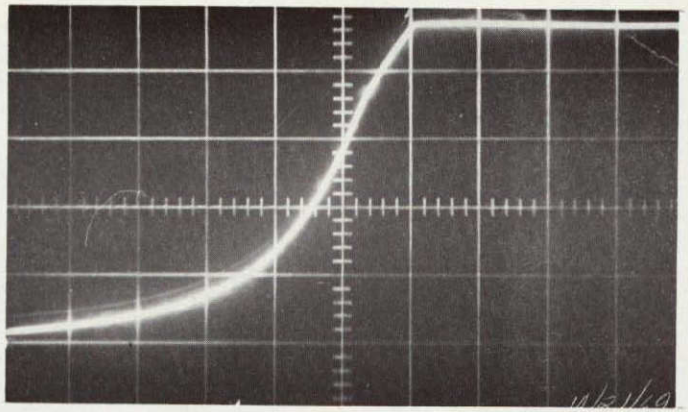
RAMP ON, 0.2 MILLISECONDS/CM



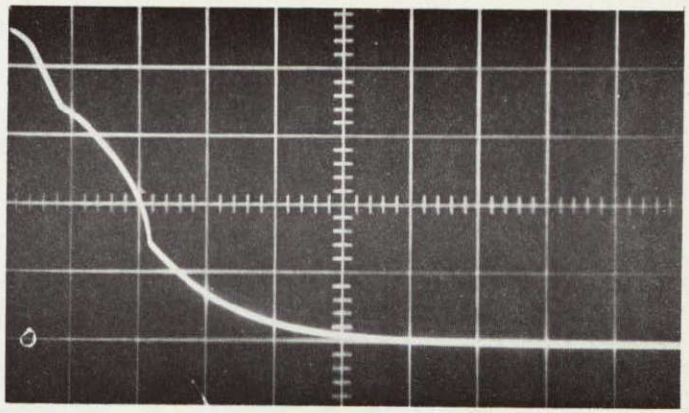
RAMP OFF, 1.0 MILLISECONDS/CM

FIGURE G-5 LOW CURRENT TRANSIENT RESPONSE

0.75
AMPERES

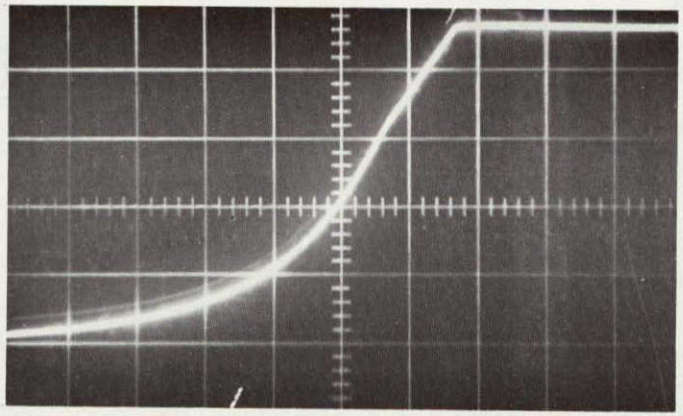


RAMP ON, 0.2 MILLISECONDS/CM

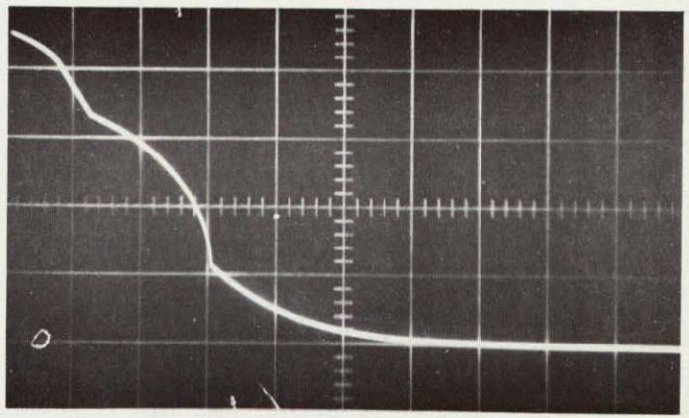


RAMP OFF, 1.0 MILLISECONDS/CM

1.0
AMPERES



RAMP ON, 0.2 MILLISECONDS/CM



RAMP OFF, 1.0 MILLISECONDS/CM

FIGURE G-6 HIGH CURRENT TRANSIENT RESPONSE

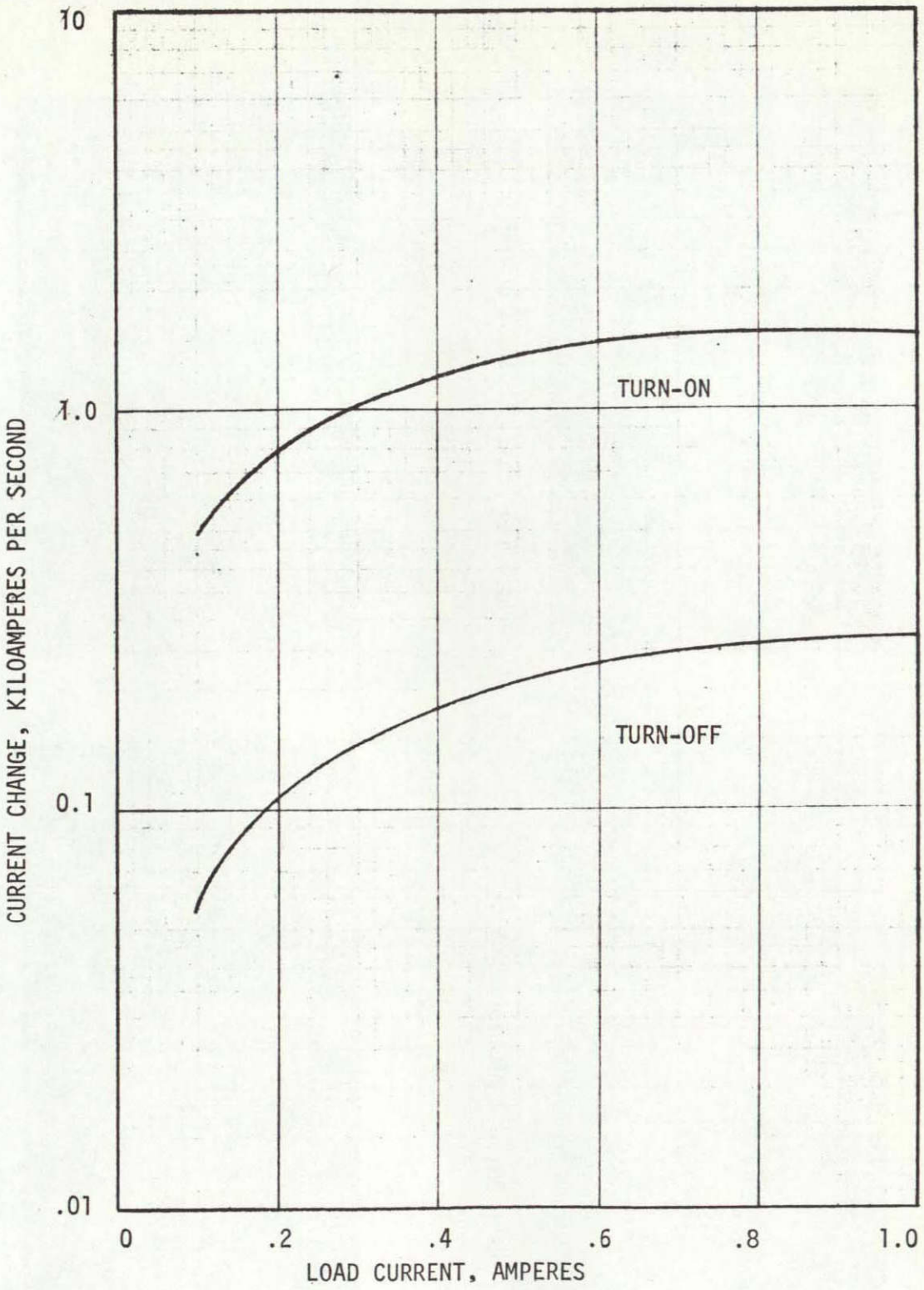
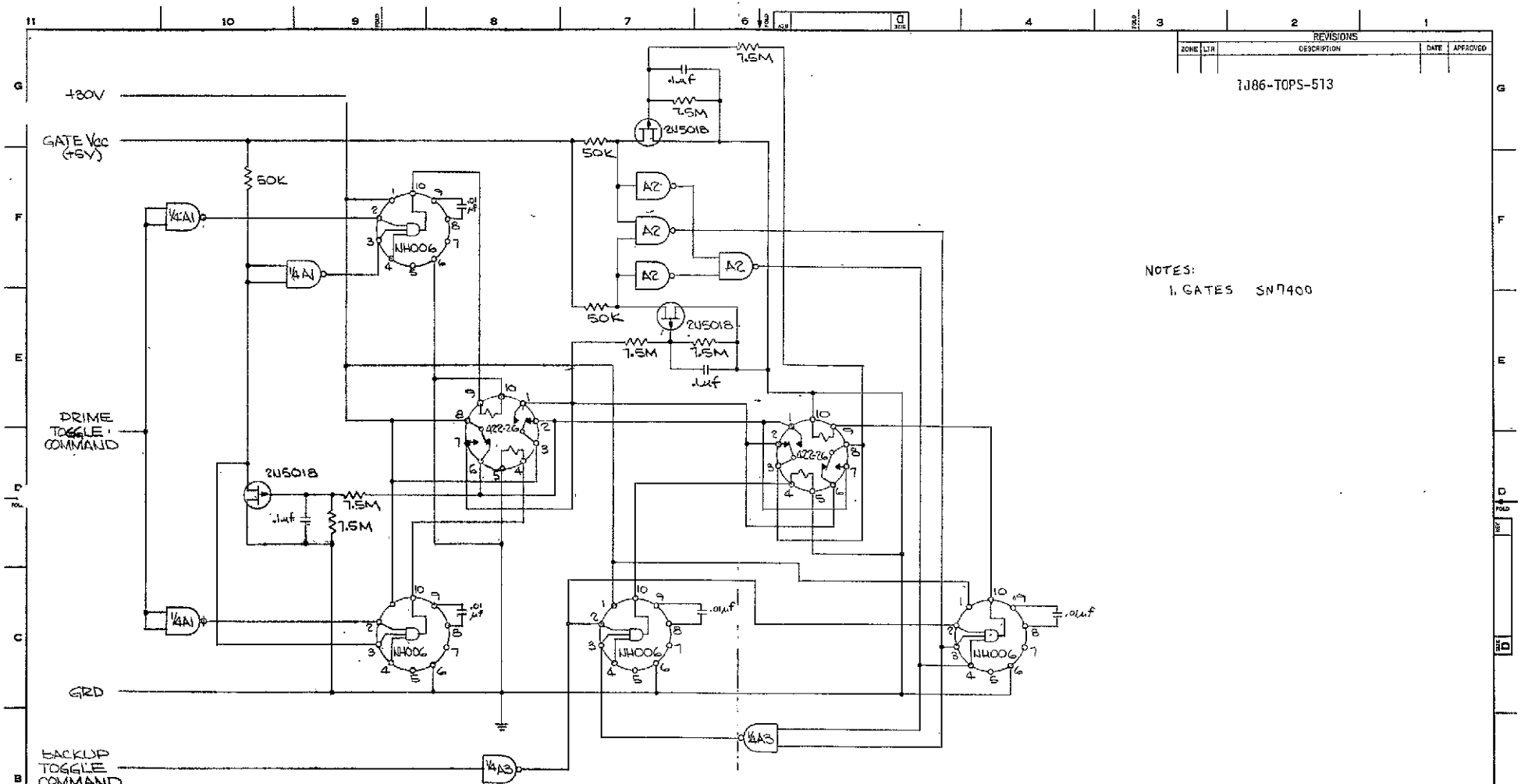


FIGURE G-7 CONTROLLED RATE OF CURRENT CHANGE



NOTES:
1. GATES SN7400

FIGURE G-8 QUAD RELAY SWITCH SCHEMATIC

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED

7J86-TOPS-513

GENERAL ELECTRIC

REDUNDANT TOGGLE SWITCH

SIZE D | CODE IDENT NO. | SCALE | SHEET 1 of 1

FOLDOUT FRAME FOLDOUT FRAME 1 FOLDOUT FRAME 2

failures (assumed predominately open) or a power failure in the command subsystem on the command line would be interpreted as no command rather than a continuous command. A continuous command to this circuit will result in oscillation.

This circuit draws twenty to forty milliamperes from a five volt bus steady state and about 1.3 milliamperes from the thirty volt line for a standby power consumption of 120 to 240 milliwatts. This could be reduced by the addition of switching to turn on the circuits only when needed, but this is additional complexity. Another disadvantage of this circuit is the need for the five volt bus.

Switch Comparison

Table G-1 is a matrix comparison of capabilities and characteristics of the solid state, redundant toggle, and toggle/backup switches.

Quad Relay Switch

The circuit of Figure G-9 provides quad redundant contacts for load power, a primary toggle command receiver, and direct control of the second relay. The command requirement is a negative pulse for 25 to 125 milliseconds at greater than -3.0 volts. The no command DC level is preferred to be +5 volts but this cirucit has capacitively coupled inputs so the DC level could be floating at any level. The significant problem with a DC level much greater or less than +5 volts is the effect of input capacitor leakage current upsetting the FET bias point. An analysis will be done to determine what levels of leakage current can be tolerated. Commands on the toggle input (input #1)

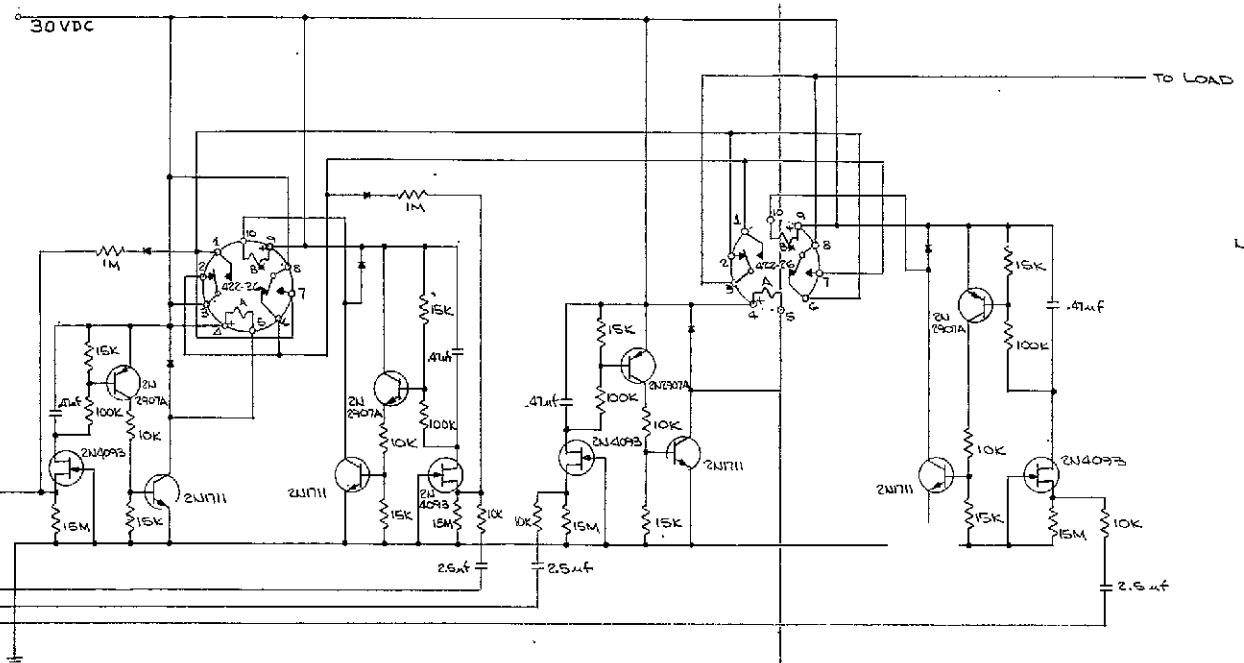
TABLE G-1

COMPARISON OF SWITCH CIRCUITS

Features / Circuit	Number of Parts	Number of Active Parts	Level of Redundancy	Reliability[1]	Controlled Rise and Fall Time	Standby Power (Load Off)	Efficiency	Failure Effects	Comments
Solid State	50	19	Load Switch Only	.980	Yes	0	90% @ 15 watts	Command Receiver could fail on or off	
Redundant toggle	28[2]	10	Full	.953	No	140-240 Milliwatts	92% @ 3 watt 99% @ 24 watts	Oscillates if command fails "ON"	Requires 5 volt bus
Toggle/ Backup	54	18	Full	.967	No	0	100% all loads	None	

Notes: 1) The solid state switch has a different level of redundancy. This comment also applies to all features of table except efficiency.

2) Four gate flat pack counted as 1 part and 1 active device since it is a single mechanical package and has a single overall failure rate.



NOTE:-
1. UNLESS OTHERWISE SPECIFIED
   A. ALL RESISTOR ARE 1/8 W.
   B. ALL DIODES ARE 1N649
2. * DENOTES COIL LAST ENERGIZED.

FIGURE G-9 TOGGLE/BACKUP RELAY SCHEMATIC

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES — TOLERANCES ON 2 PLACE DECIMALS ± 3 PLACE DECIMALS ± ANGLES ± FRACTIONS ± MATERIAL —	SIGNATURES	DRAWN	ENGR	MFG	DATES
ALL SURF. ✓	DRAWN	21	10	69	
	ENGR	A1	10	69	

GENERAL ELECTRIC — DEPT LOC

TOGGLE/BACKUP QUAD RELAY SWITCH

SIZE D — CODE IDENT NO. — SCALE — SHEET 1 OF 1

FOLDOUT FRAME 1

FOLDOUT FRAME 2

must be more than 100 seconds apart, and commands on the backup (inputs #2 and #3) must be more than 20 seconds apart. Modifications are contemplated which will reduce the time granularity restriction between toggle commands.

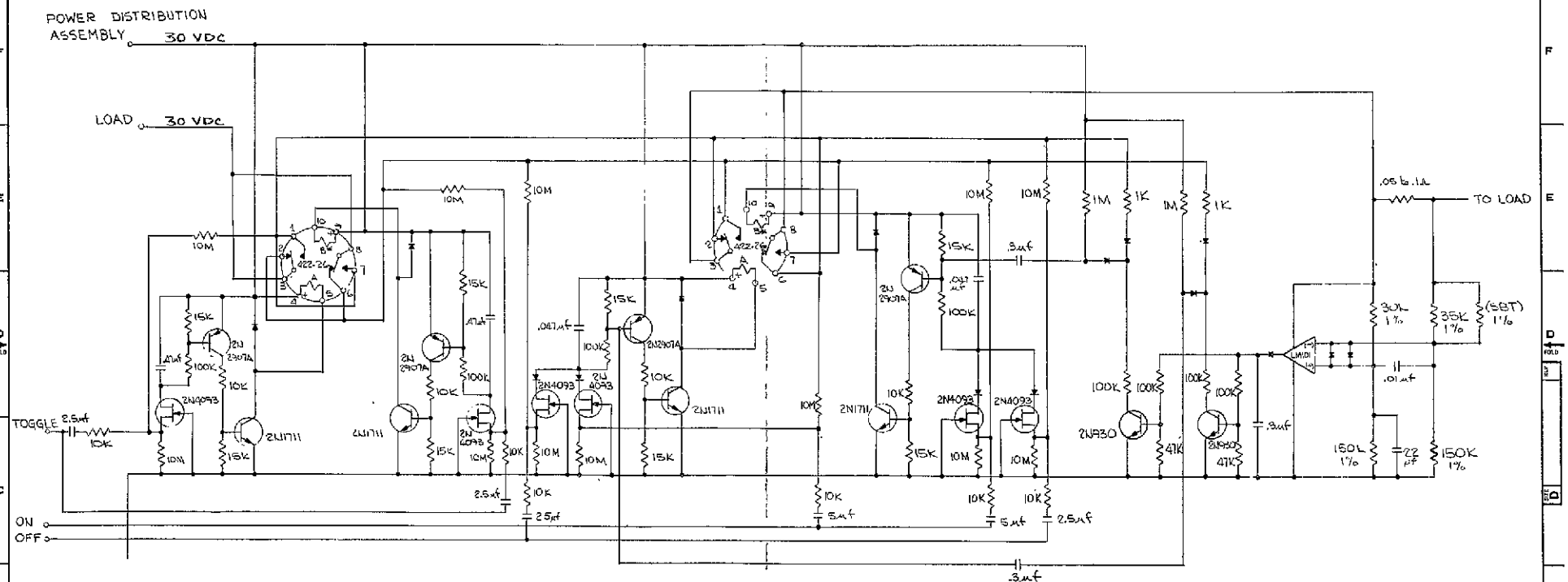
This circuit has good sensitivity. The breadboard operates with a command of only -2.5 volts, but showed no voltage change on the relay coil with a -10 volt input for 5 milliseconds. The standby power for this circuit is less than 70 micro watts in any state. Since the commands are capacitiv e coupled, a command failure will be ignored after an initial response when the failure occurred.

This circuit is relatively simple, virtually loss free, fully redundant, immune to command source failures, compatible with TTL/DTL commands, and has high noise immunity. For a relay type of switch, this circuit seems to provide the maximum of every design parameter.

The toggle/backup quad relay switch was modified to a true toggle/on-off switch as shown in Figure G-10. In the toggle/backup configuration, the state of the first relay is not known and may require two commands for proper implementation. The modified (toggle/on-off) switch need not know the relay state and can turn on or off with a single command.

This circuit requires more than seventy seconds of elapsed time between commands to ensure operation, the same as the previous toggle/backup switch.

A positive but over-ridable turn-off circuit was added to the toggle/on-off quad relay switch previously described. The turn-off occurs when "toggling" or turning "on" into an overcurrent, or an overcurrent occurs. The turn-off is accomplished by changing the second or backup relay.



NOTES
1. UNLESS OTHERWISE SPECIFIED
   A. ALL RESISTORS ARE 1/8W, ±5%
   B. ALL DIODES ARE IN 649
2. * DENOTES COIL LAST ENERGIZED.

FIGURE G-10. TOGGLE/ON-OFF RELAY SWITCH

A resitive element is placedin the 30 VDC line to the load, and an operational amplifier is used to sense the voltage across the resistor. The trip point is determined by the select-by-test resistor. Several millivolts difference could be required at the input to the operational amplifier to trigger a turn-off, which would require up to 3 millivolts across the sense resistor. A design using such a low sense voltage would probably suffer larger drifts in trip point than a design using a hundred millivolts across the resistor. This design has a nominal value of 50 millivolts across the sense resistor.

The operational amplifier output drives two transitors, one of which will cause a driving pulse (since capacitive coupling is used to the relay driver) on one of the coils of the second relay. A 1 to 100 kilohm divider output on these transistors prevents activation of the last energized coil when bus voltage is present at the one kilohm resistor.

Trip point variation with voltage and temperature is shown on Figures G-11 and G-12. The circuit was functionally tested from -20 to +80°C ambient. Trip times were 1.2 to 1.8 milliseconds for a 5 - 10% overload pulse, 2 - 3 milliseconds turning on into a 5 - 10% overload, 0.44 to 0.6 milliseconds for a 40-100% overload.

The turnoff can be overridden by a 100 millisecond "on" command to the second relay or probably by two 50 millisecond commands with several milliseconds between pulses. The override is accomplished simply by supplying an "on" command for longer than the turnoff circuit's coupling capacitor time constant.

Summary

The power control circuit characteristics are presented on Table G-1. The schematics presented are of the breadboard or what will be implemented for the the breadboard. The circuits were constructed with parts chosen for availability or their particular applicability in proving the design concept. After further experimentation and refinement to choose one or two preferred circuits, the parts will be selected from the JPL preferred list where possible or a list of parts needed but not on the preferred list provided to JPL.

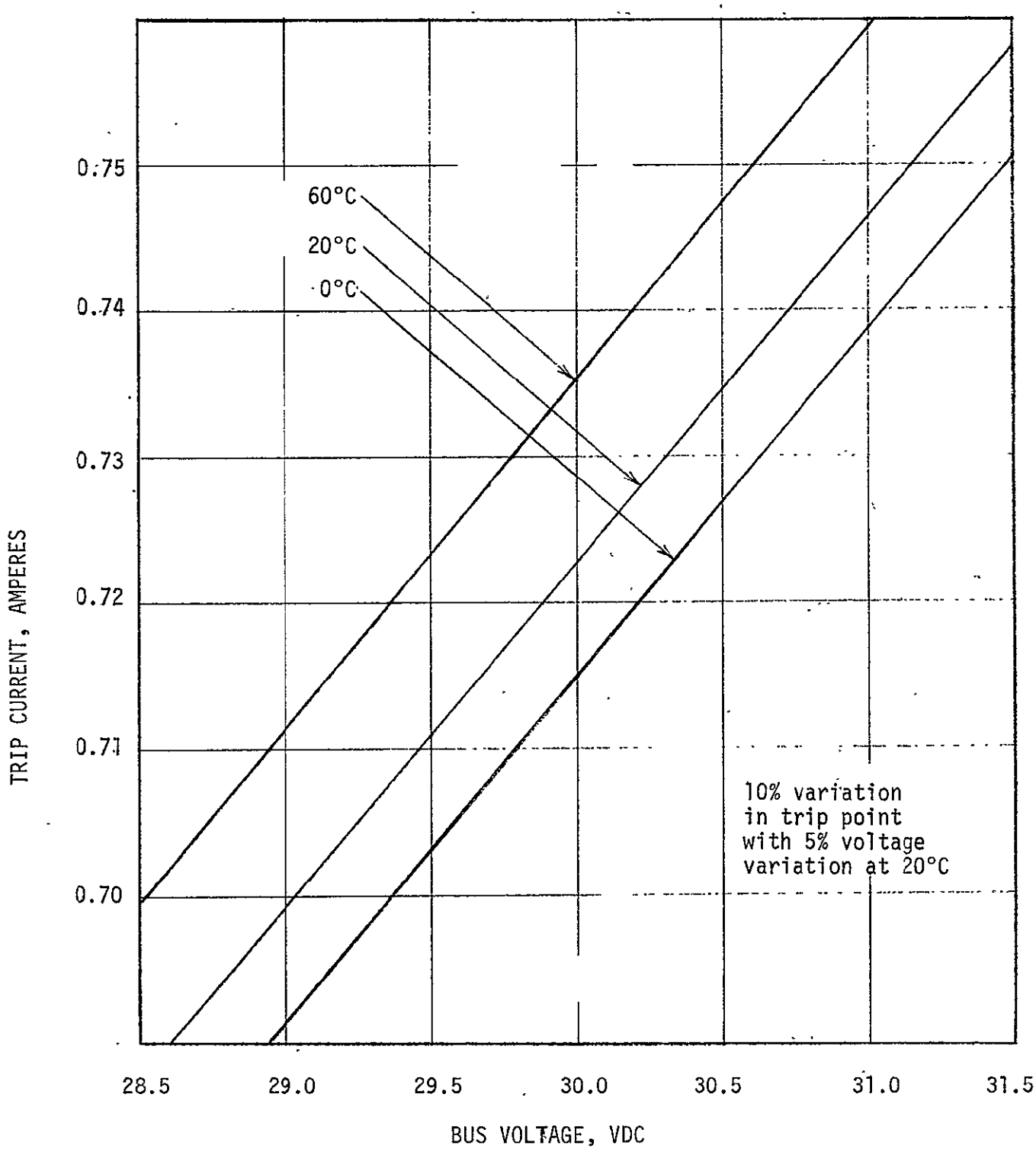


FIGURE G-11. EFFECT OF VOLTAGE ON TRIP POINT

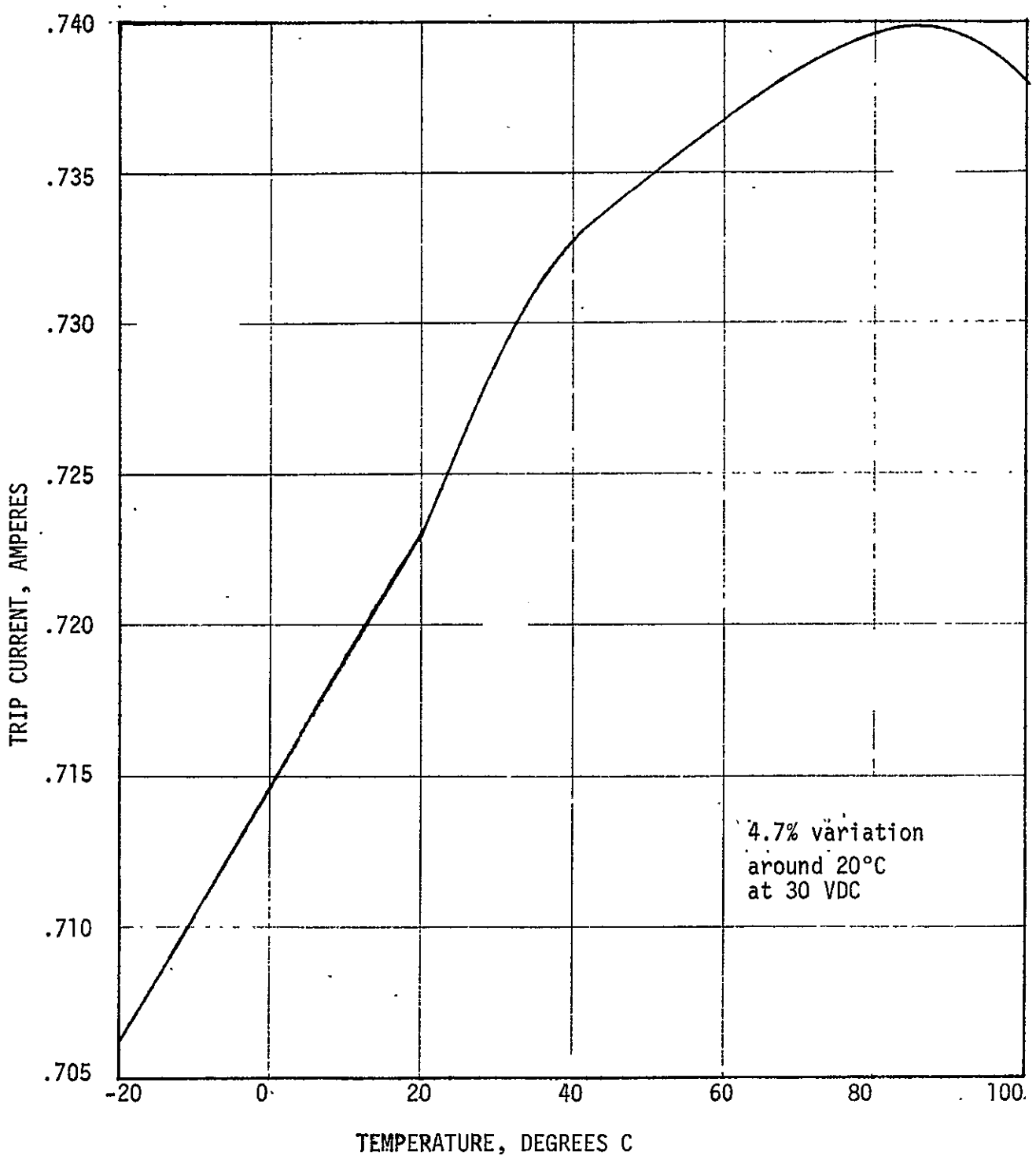


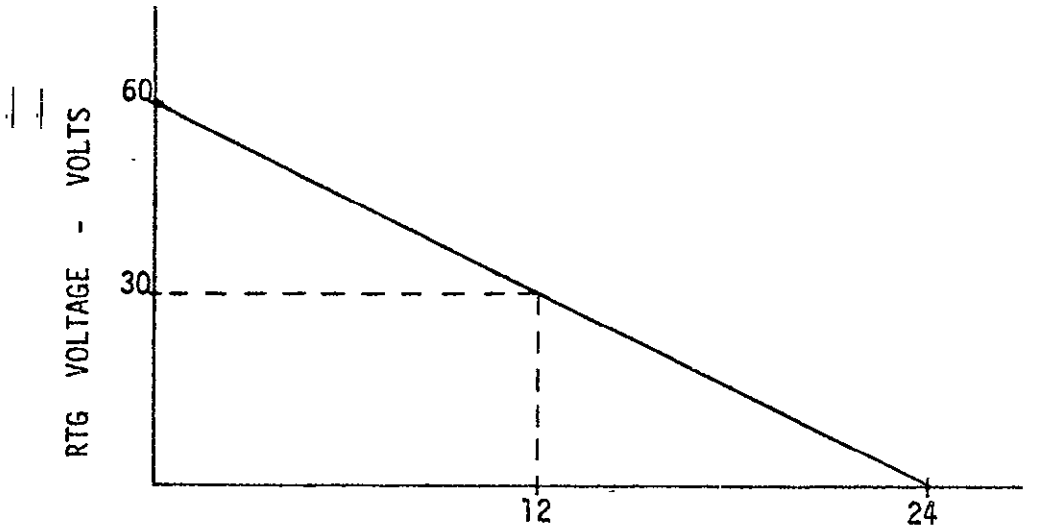
FIGURE G-12. EFFECT OF TEMPERATURE ON TRIP POINT

APPENDIX H SHUNT REGULATOR TEST RESULTS

Introduction

The TOPS "Shunt Regulator" maintains the RTG at a constant voltage, drawing essentially constant current even though the bus load changes and therefore causes the RTG to operate near its maximum power point. It maintains a DC output voltage constant against input, ambient and load changes; essentially ripple-free; providing a low dynamic impedance to transients or pulsing load currents. The shunt regulator requires constant voltage and then dissipates the current difference between the power source current capability at that voltage and the load requirement. The maximum shunt regulator power required from the RTG is maximum input voltage and maximum load current simultaneously, regardless of the actual load current.

The TOPS "Shunt Regulator" was designed to dissipate a maximum of 270 watts (that is 30 volts bus voltage times 9 amperes shunt current). The TOPS RTG characteristic to which this shunt regulator was designed is shown below.



A minimum vehicle load of 90 watts was assumed (that is a 3 ampere load current), therefore the shunt regulator has to shunt the difference between the RTG

current at 30 volts (12 amperes) and the minimum fixed load current (3 amperes). This results in a required capacity of 270 watts.

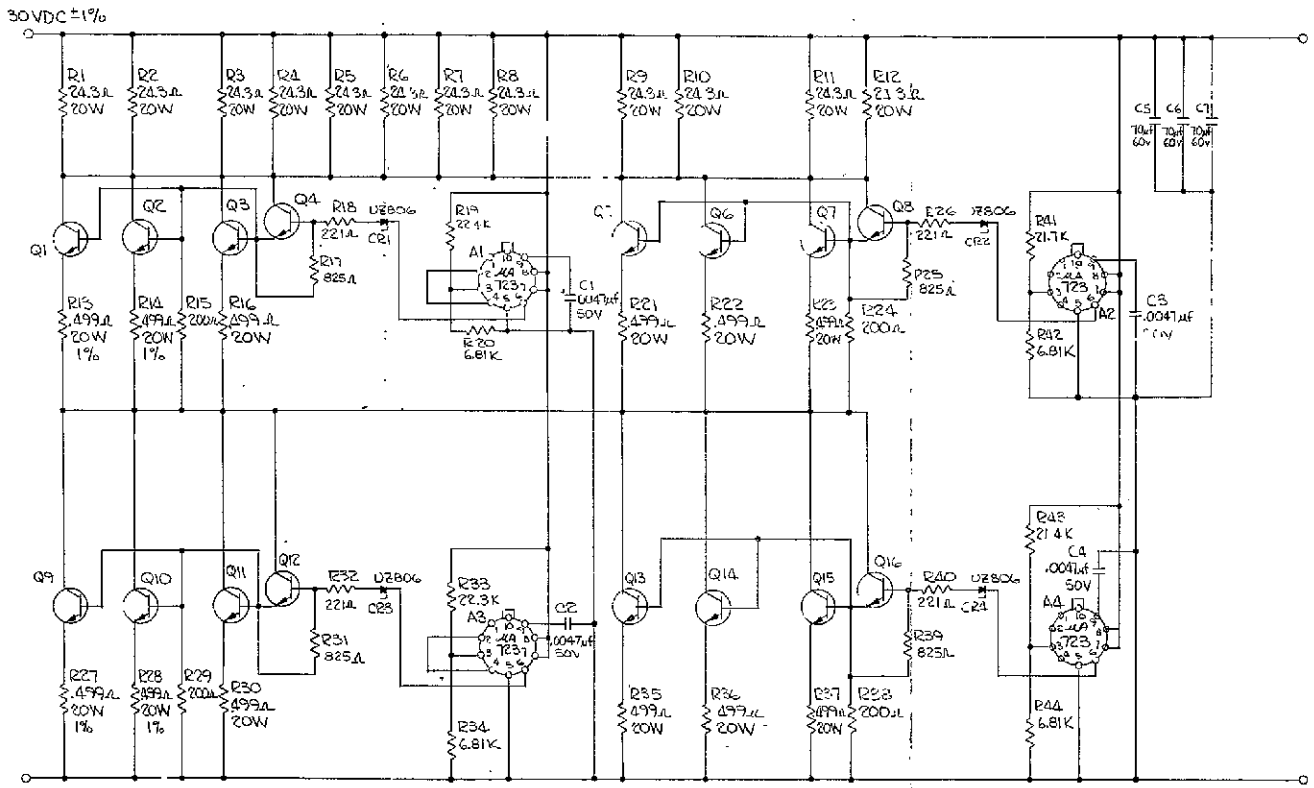
A laboratory test was conducted on the shunt regulator of Figure H-1 to test its regulation capability against a 270 watt load variation and at the specified flight temperatures of 0°C, 25°C and 40°C ambient. Also a test was conducted at type approval temperatures of -20°C and 80°C ambient. The regulation test data is presented graphically on Figure H-2 and in tabular form on Table H-1. A worst case bus voltage change of 182 millivolts was observed under the extreme type approval temperature conditions. This is within the specified regulation of 30 volts $\pm$ 1%.

The output impedance as a function of frequency and shunt regulator current variation of 3, 6 and 9 amperes was tested, using a 210 μf capacitor on the bus and also a 1000 μf capacitor for filtering. The laboratory test setup is shown in Figure H-3 and test data are presented on Table H-2 and H-3, and curves are shown in Figures H-4 through H-9. The maximum impedance is 200 milliohms with a 210 μf capacitor, 70 milliohm with a 1000 μf capacitor, and peaks at about 6 to 9KHz depending on the load current.

A transient response test was conducted at various di/dt by utilizing a ramper for the load. The test setup is shown on Figure H-10, test data are included on Tables H-4 and H-5, and response curves are shown in Figures H-11 through H-14. A typical bus voltage overshoot and undershoot for both capacitors are shown in Figure H-15. Another test was then conducted by keeping a constant

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	OUTPUT CAPACITOR ADDED	12-4-69	

1J86-TOPS-513



NOTES:-
1. UNLESS OTHERWISE SPECIFIED -
   (A) ALL TRANSISTORS ARE 2N3773.
   (B.) ALL RESISTORS ARE 1/8W.

FIGURE H-4 SHUNT REGULATOR SCHEMATIC

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES — TOLERANCES ON 2 PLACE DECIMALS ± 3 PLACE DECIMALS ± ANGLES ± FRACTIONS ± MATERIAL —	ALL BURR ✓	SIGNATURES	DAY	MO	YR
		DRAWN	19	8	69
		CHECKED			
		ISSUED			
		ENGR			
		MFG			
		NOTES			

GENERAL ELECTRIC DEPT. LOC

TOPS
SHUNT REGULATOR
(B.B. SUITCASE CONFIGURATION)

SIZE	CODE IDENT NO.	
D		
SCALE ~		SHEET 1 OF 1

FOLDOUT FRAME 1

FOLDOUT FRAME 2

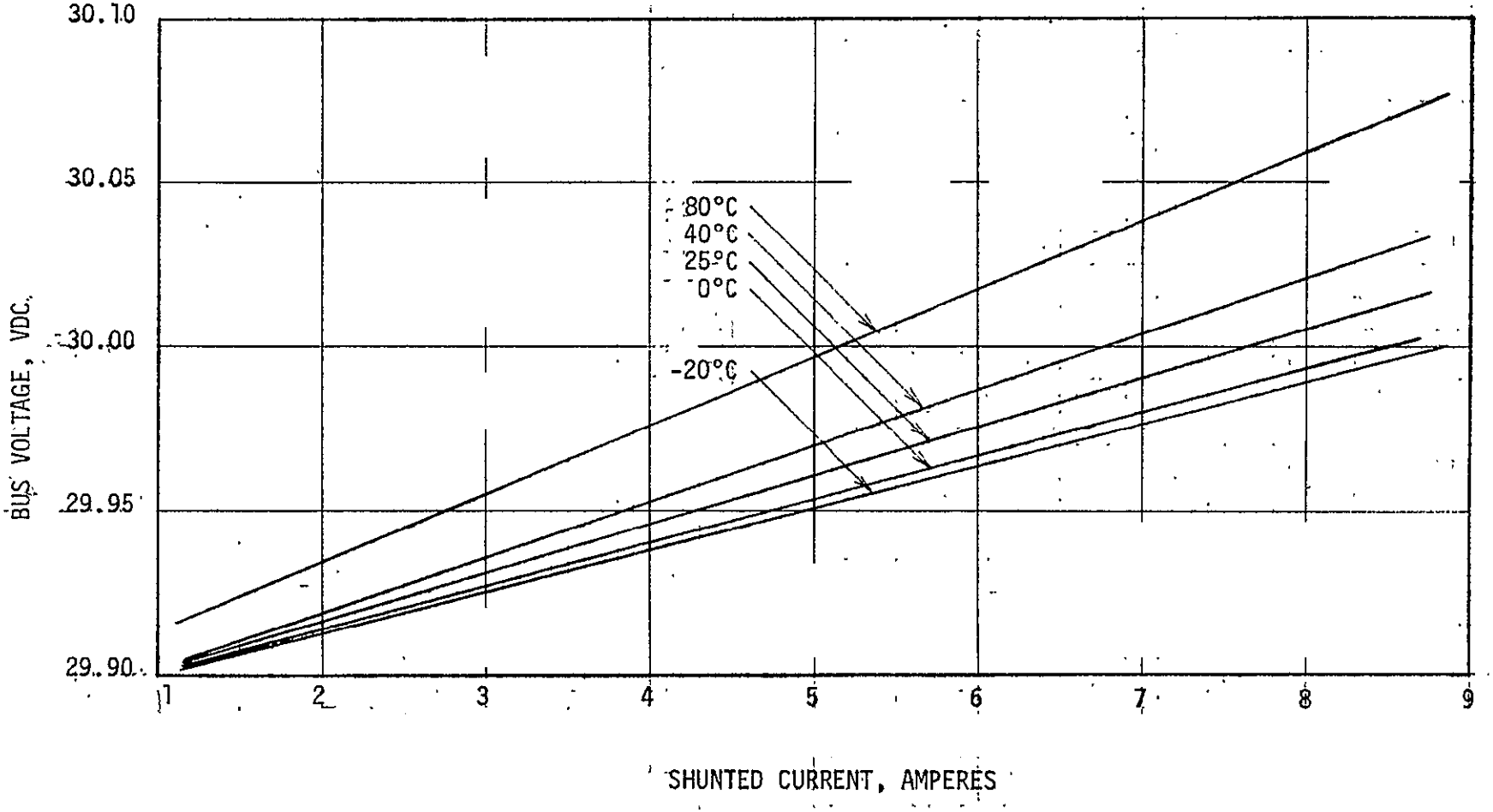


FIGURE H-2. LOAD AND TEMPERATURE REGULATION

TABLE H-1

TOPS SHUNT REGULATOR PERFORMANCE

I_{shunt} - amps \ Temp - °C	V_{BUS} - VOLTS				
	-20°	0°	25°	40°	80°
1.0	29.909	29.902	29.902	29.908	29.914
2.0	.920	.912	.916	.916	.935
3.0	.930	.926	.933	.933	.956
4.0	.942	.939	.947	.951	.976
5.0	.954	.952	.960	.969	.999
6.0	.965	.964	.975	.987	30.012
7.0	.978	.977	.991	.997	.036
8.0	.989	.990	.997	30.016	.058
9.0	.993	30.006	30.019	.036	.084

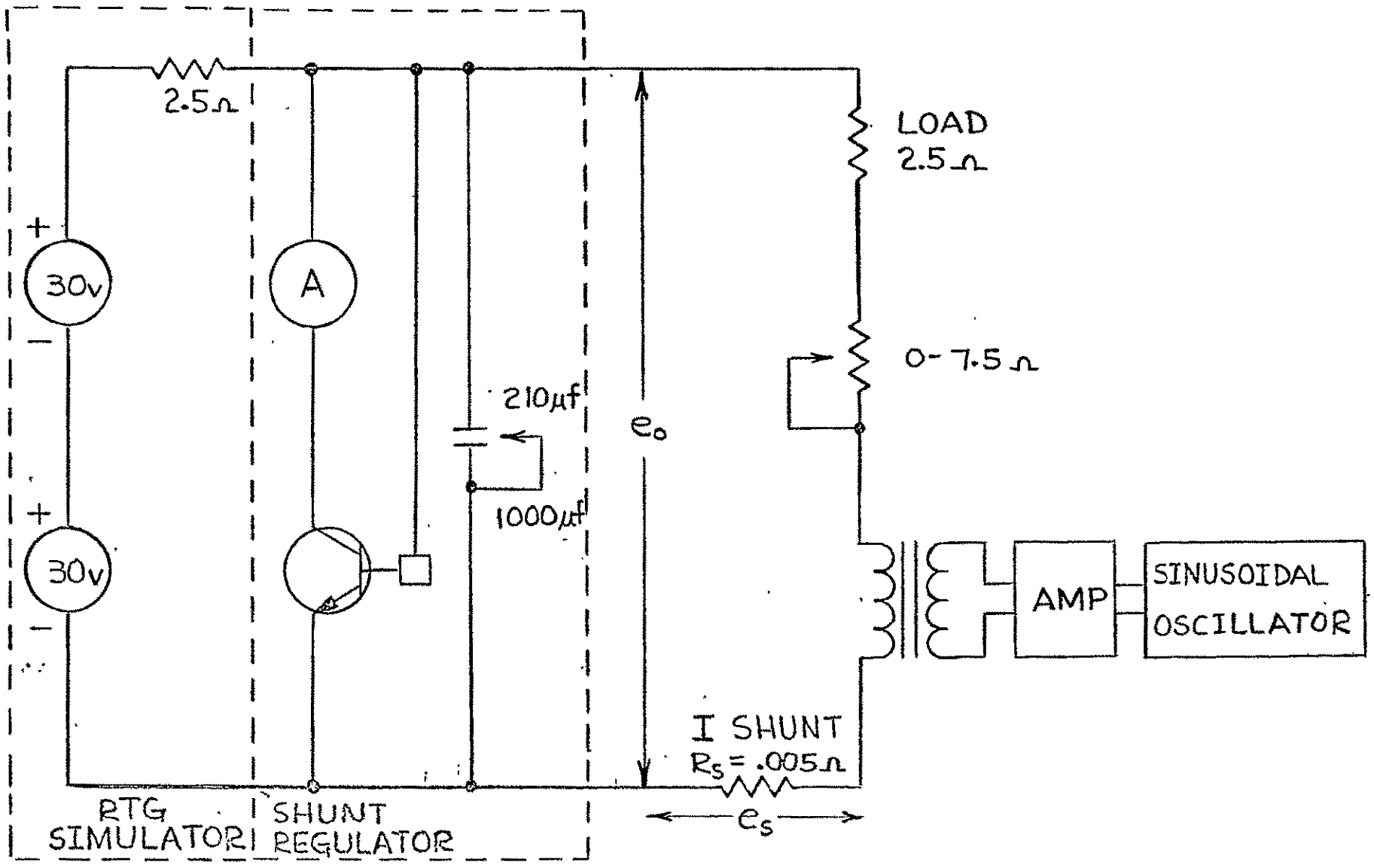


FIGURE H-3 OUTPUT IMPEDANCE TEST SCHEMATIC

TABLE H-2

OUTPUT IMPEDANCE WITH LOW CAPACITANCE

Capacitance = 210 microfarads

I-shunt - amps	3			6			9		
Freq. - Hz	e_o-mv.	e_s-mv.	Z_o-	e_o-mv.	e_s-mv.	Z_o-	e_o-mv.	e_s-mv.	Z_o-
40	2.4	13.0	.0009	1.8	1.9	.00102	1.2	5.2	.0011
100	5.0	14.0	.0018	3.6	9.5	.00189	2.0	5.2	.0019
500	25.0	14.0	.0089	17.0	9.5	.00895	10.0	5.2	.0096
1000	44.0	13.0	.0169	34.0	9.5	.01790	20.0	5.4	.0180
2000	95.0	13.0	.0360	72.0	9.5	.03790	44.0	5.4	.0400
5000	320.0	12.5	.1280	240.0	9.5	.12600	155.0	5.5	.1410
6500	430.0	12.5	.1720						
7500				340.0	9.5	.17900	220.0	5.4	.2035
10,000	340.0	12.5	.1360	280.0	9.0	.15500	190.0	5.2	.1825
20,000	160.0	8.5	.0940	140.0	8.5	.08240	90.0	4.8	.0930
50,000	50.0	9.5	.0210	44.0	9.5	.02390	42.0	7.8	.0270

TABLE H-3

OUTPUT IMPEDANCE WITH HIGH CAPACITANCE

Capacitance = 1000 microfarads

I-shunt - amps	3			6			9		
Freq.-Hz	e_o-mv.	e_s-mv.	Z_o-	e_o-mv.	e_s-mv.	Z_o-	e_o-mv.	e_s-mv.	Z_o-
40	4	32	.0006	3	24	.0006	1.5	12.0	.0006
100	8	34	.0012	6	26	.0014	3.0	13.0	.0012
500	34	31	.0055	28	25	.0056	14.0	13.0	.0054
1000	76	31	.0122	52	22	.0118	21.0	9.0	.0116
2000	160	30	.0267	112	22	.0255	42.0	8.8	.0238
5000	320	28	.0570	235	21	.0560	35.0	3.0	.0583
6000	390	32	.0610						
7000				250	20	.0625			
8300							43.0	3.0	.0716
10,000	340	30	.0567	225	19	.0592	40.0	3.0	.0668
20,000	270	32	.0422	155	18	.0430	26.0	3.0	.0434
50,000	120	26	.0231	72	16	.0250	13.0	3.0	.0216

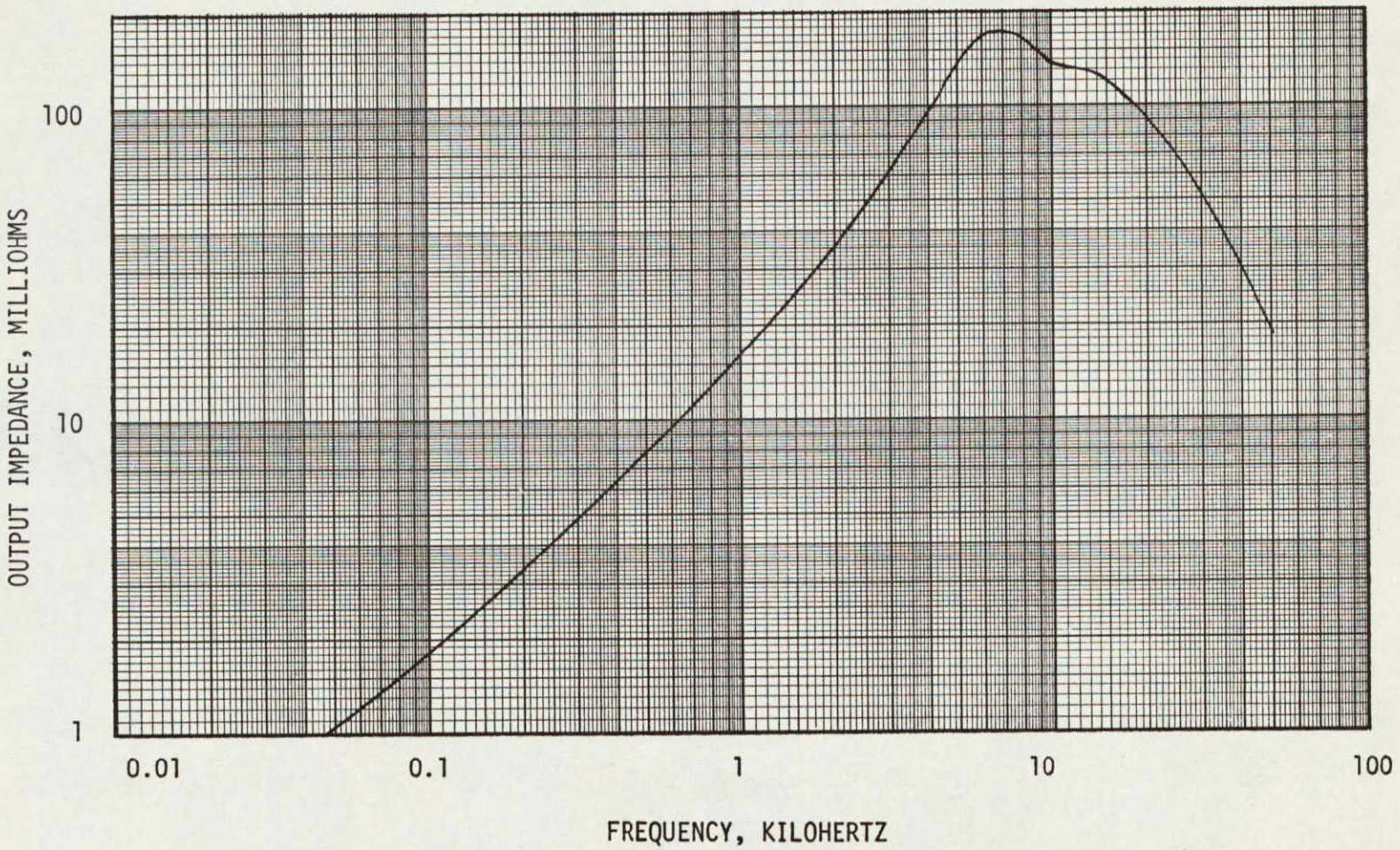


FIGURE H-4 DYNAMIC IMPEDANCE AT THREE AMPERES, 210 μF

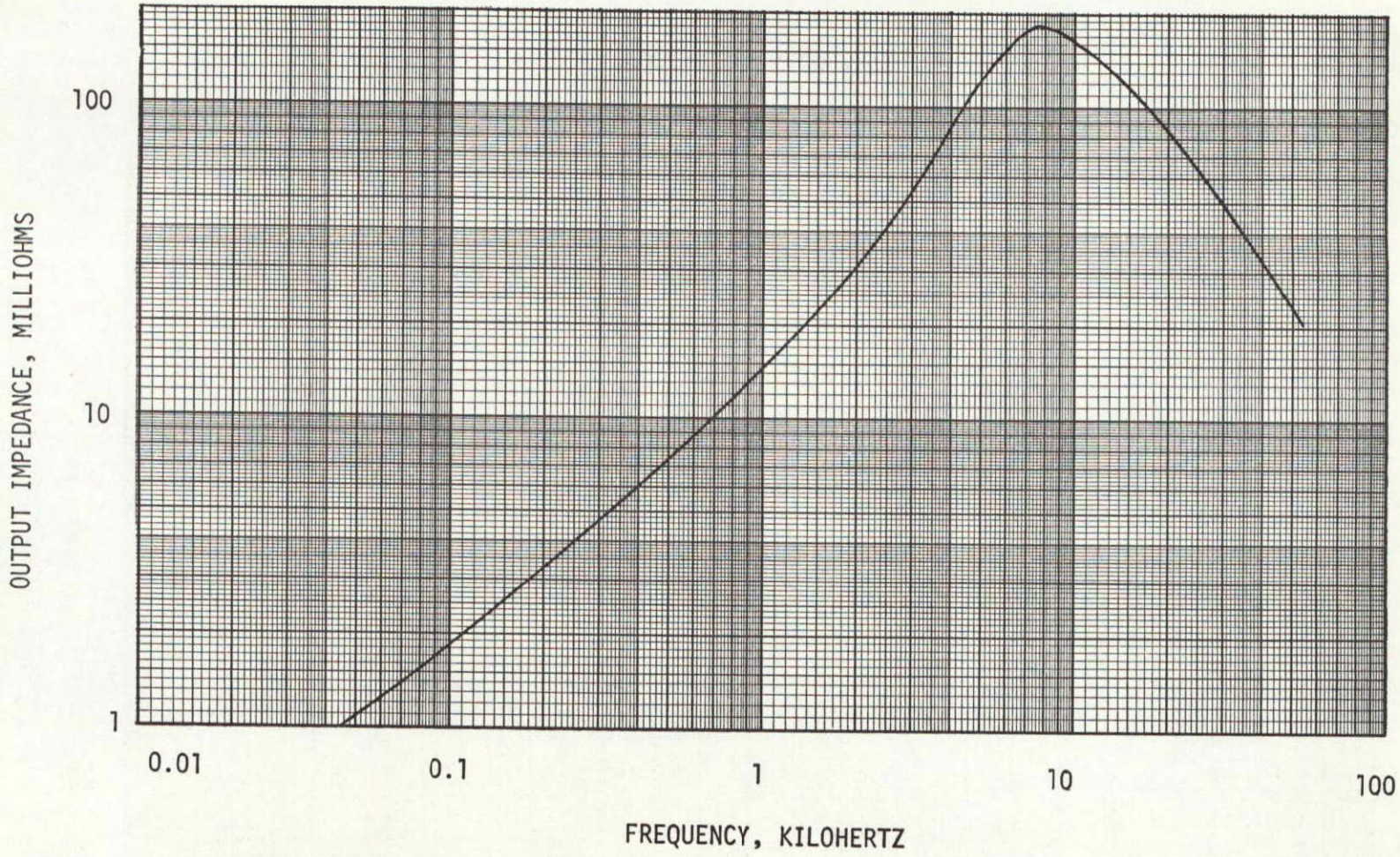


FIGURE H-5 DYNAMIC IMPEDANCE AT SIX AMPERES, 210 μF

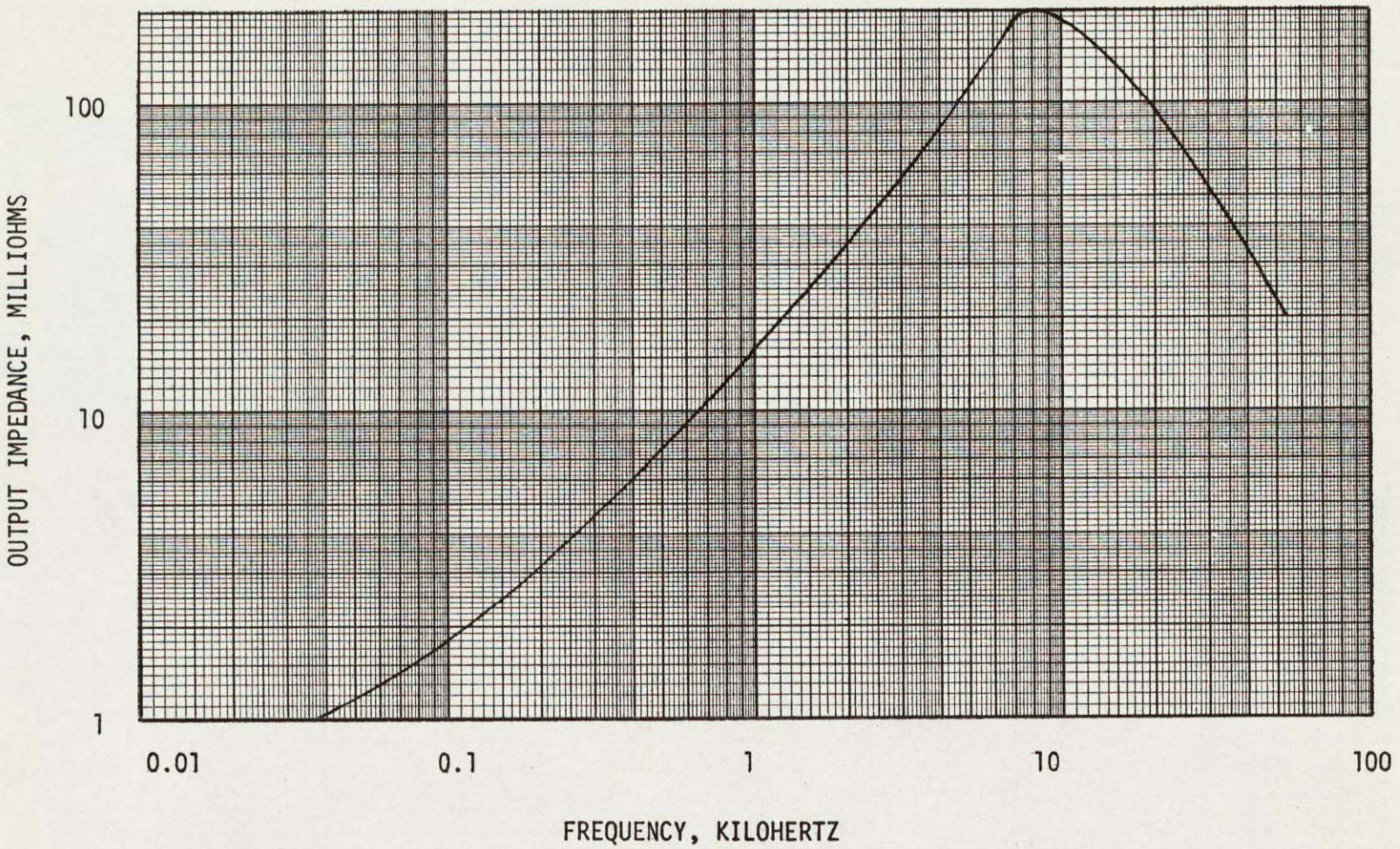


FIGURE H-6 DYNAMIC IMPEDANCE AT NINE AMPERES, 210 μF

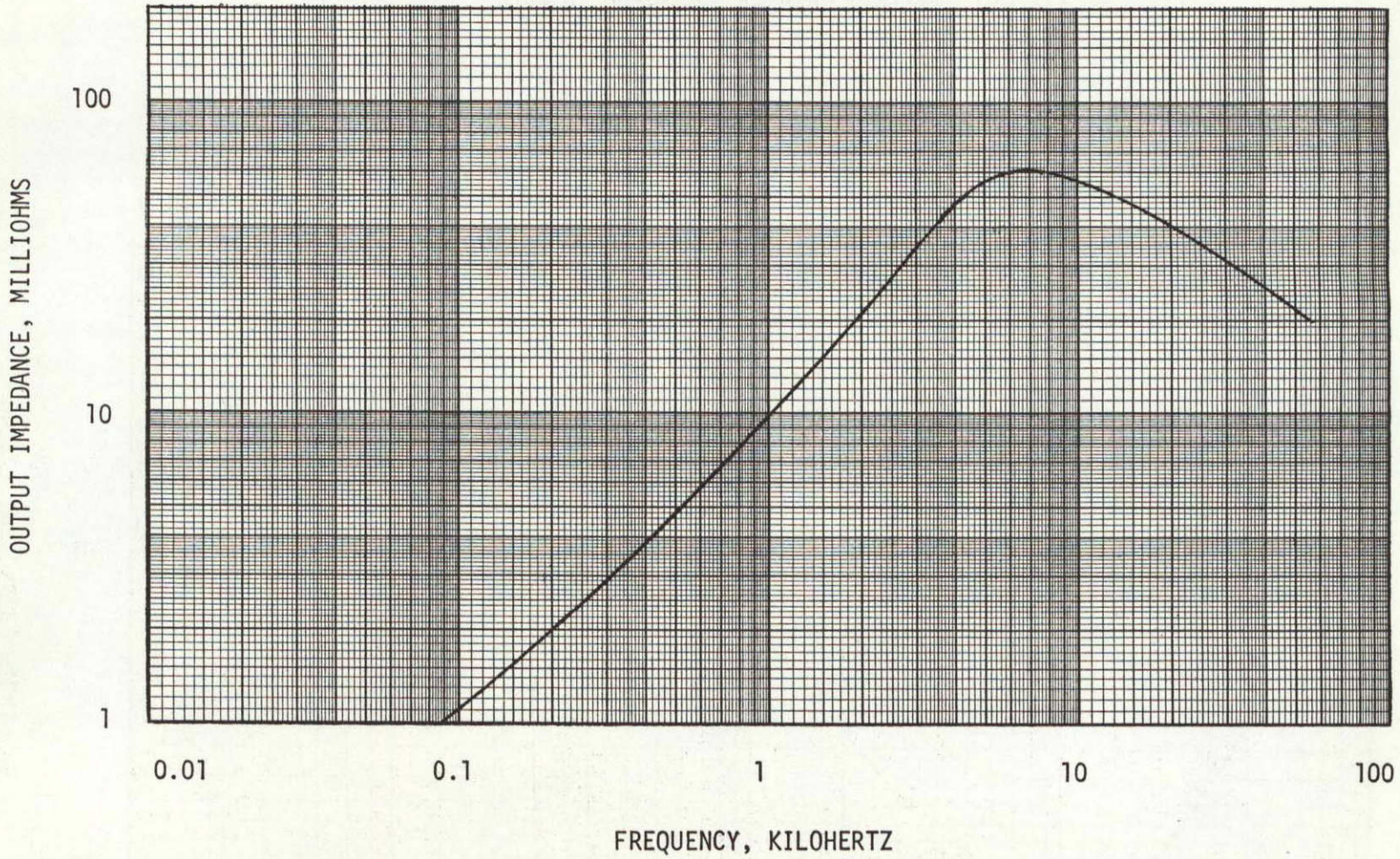


FIGURE H-7 DYNAMIC IMPEDANCE AT THREE AMPERES, 1000 μF

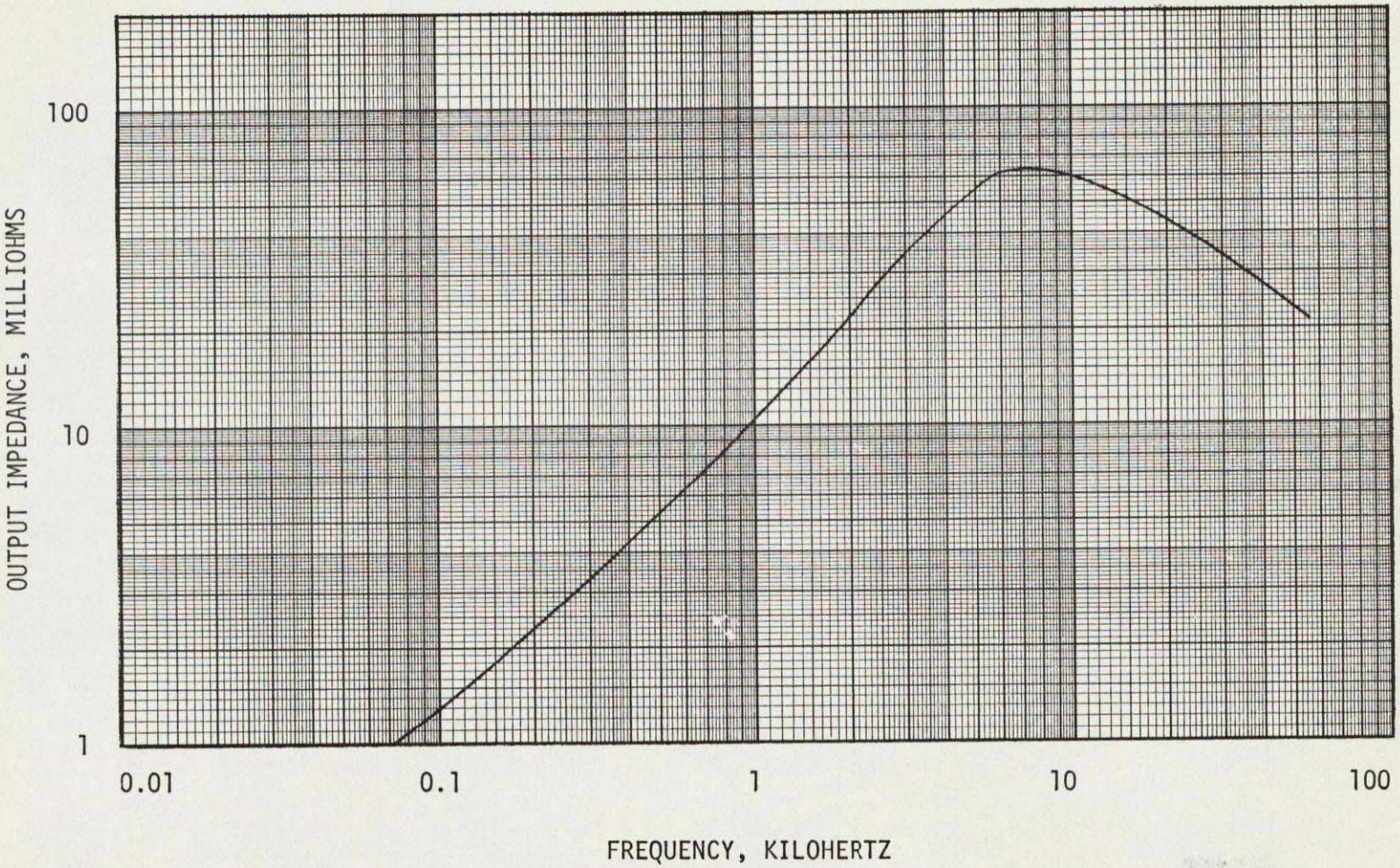


FIGURE H-8 DYNAMIC IMPEDANCE AT SIX AMPERES- 1000 μF

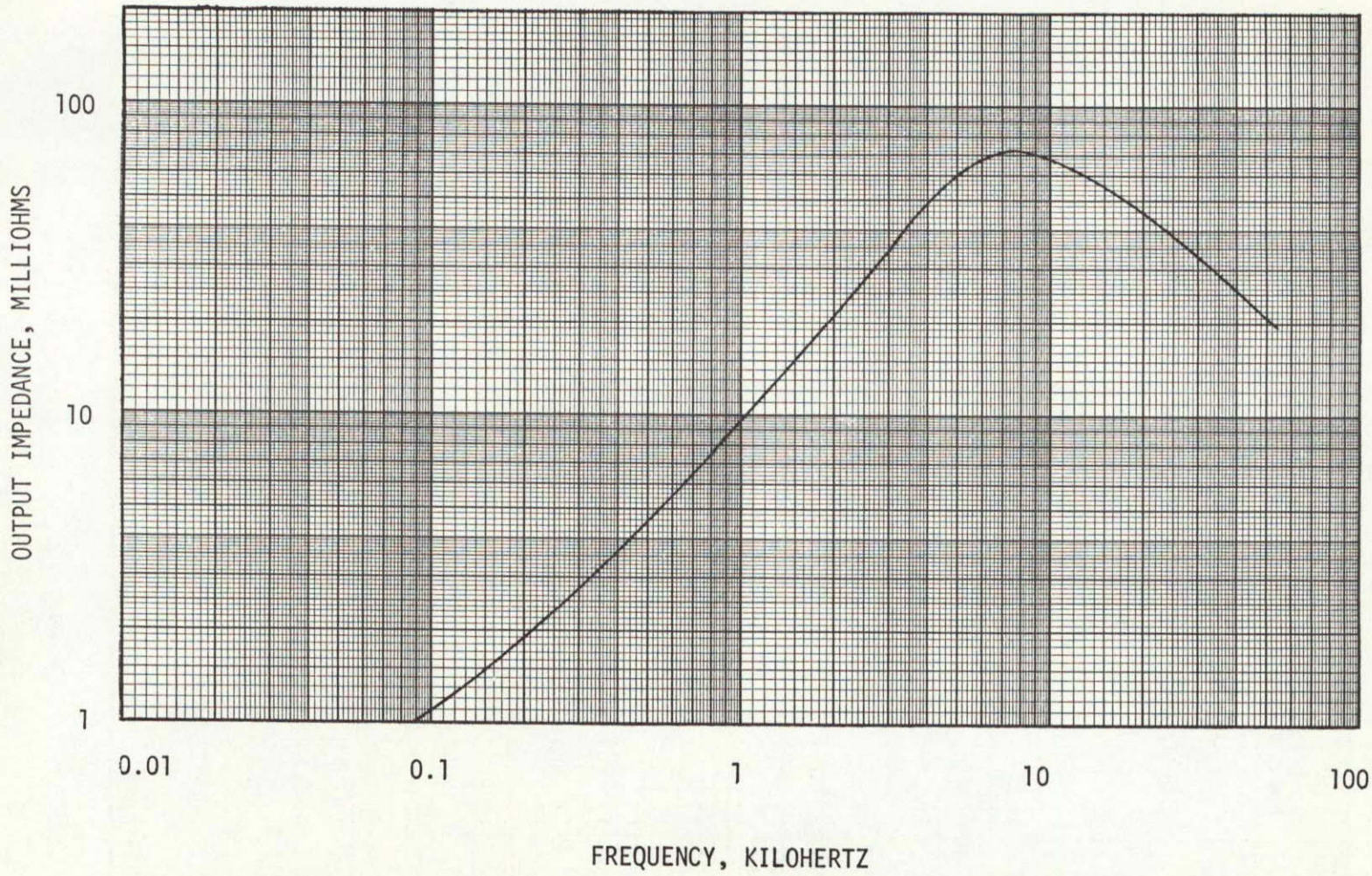


FIGURE H-9 DYNAMIC IMPEDANCE AT NINE AMPERES, 1000 μF

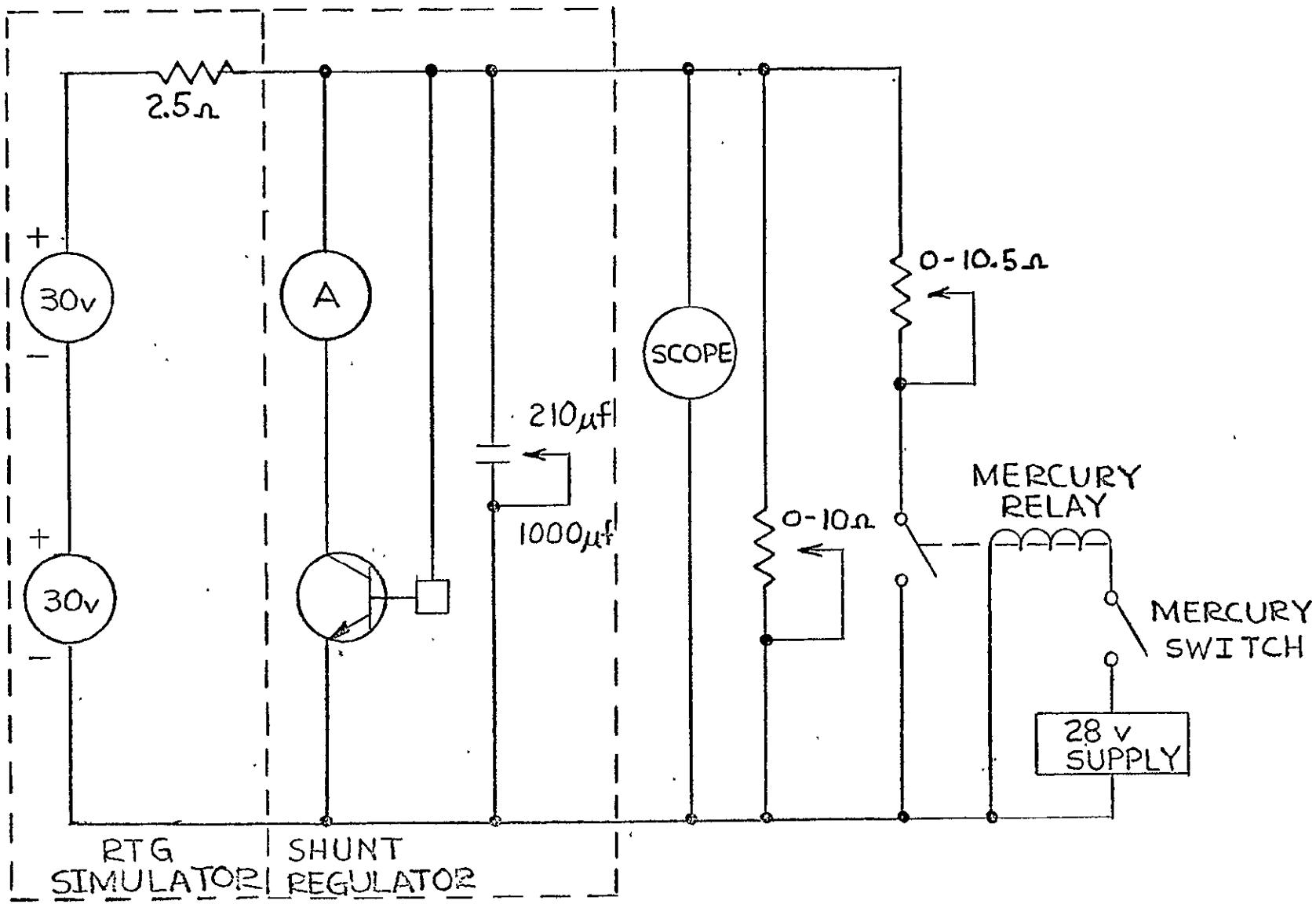


FIGURE H-10 TRANSIENT RESPONSE TEST SCHEMATIC

TABLE H-4

STEP LOAD TRANSIENT RESPONSE

LOAD RANGE AMPS	LOAD AMPLITUDE CHANGE AMPS	FINAL VOLTAGE VOLTS	LOAD POWER CHANGE WATTS	DISTURBANCE AMPLITUDE VOLTS		RECOVERY TIME MICROSECONDS	
				C=210 μf	C=1000 μf	C=210 μf	C= 1000 μf
S T E P L O A D I N G							
3 - 6	3	30.0	90	.38	.24	55	64
3 - 9	6		180	.85	.50	100	85
3 - 12	9		270	1.45	.75	500	580
6 - 9	3		90	.34	.24	70	70
6 - 12	6		180	.775	.46	260	350
S T E P U N L O A D I N G							
12 - 9	3	30.0	90	.40	.23	80	100
12 - 6	6		180	1.00	.48	110	120
12 - 3	9		270	1.90	.77	160	140
9 - 6	3		90	.38	.25	70	100
9 - 3	6		180	.975	.50	120	125

TABLE H-5

RESPONSE TO RAMPED LOADS

LOAD RANGE AMPS	LOAD AMPLITUDE CHANGE AMPS	FINAL FINAL VOLTAGE VOLTS	LOAD POWER CHANGE WATTS	DISTURBANCE AMPLITUDE VOLTS		REGULATION DI/DT AMPS/SEC.	
				C=210 μf	C=1000 μf	C=210 μf	C=1000 μf
R A M P L O A D I N G							
3 - 6	3	30.0	90	.009	.0010	60 K	171 K
3 - 9	6		180	.011	.0021	50 K	120 K
3 - 12	9		270	.014	.0032	50 K	103 K
6 - 9	3		90	.007	.001		
6 - 12	6		180	.010	.002		
R A M P U N L O A D I N G							
12 - 9	3	30.0	90				
12 - 6	6		180	.002	.0026		
12 - 3	9		270	.004	.0032	40 K	72 K
9 - 6	3		90	.0012	.0012		
9 - 3	6		180	.0020	.0022	50 K	89 K
6 - 3	3		90			67 K	200 K

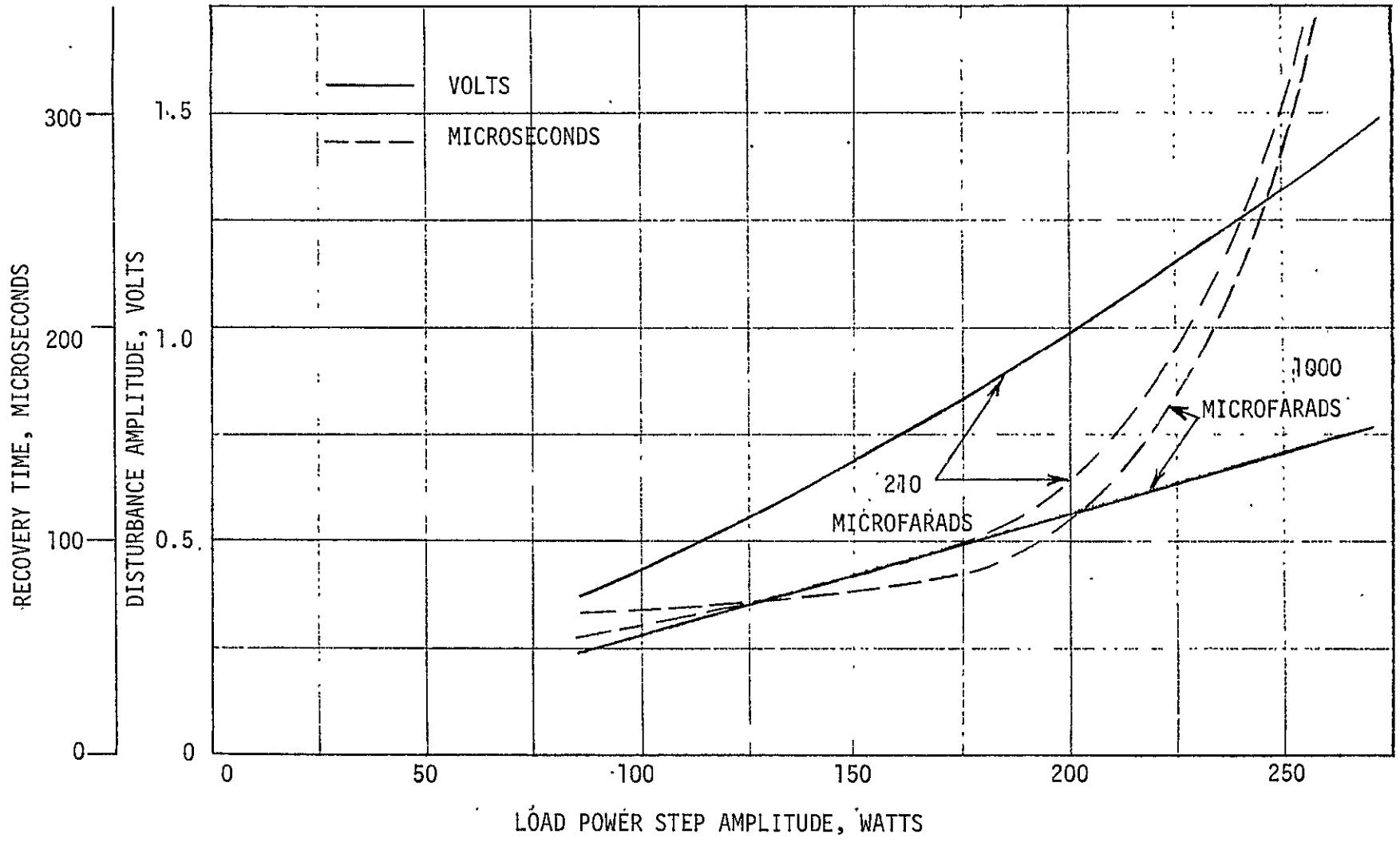


FIGURE H-11 STEP LOADING TRANSIENT RESPONSE

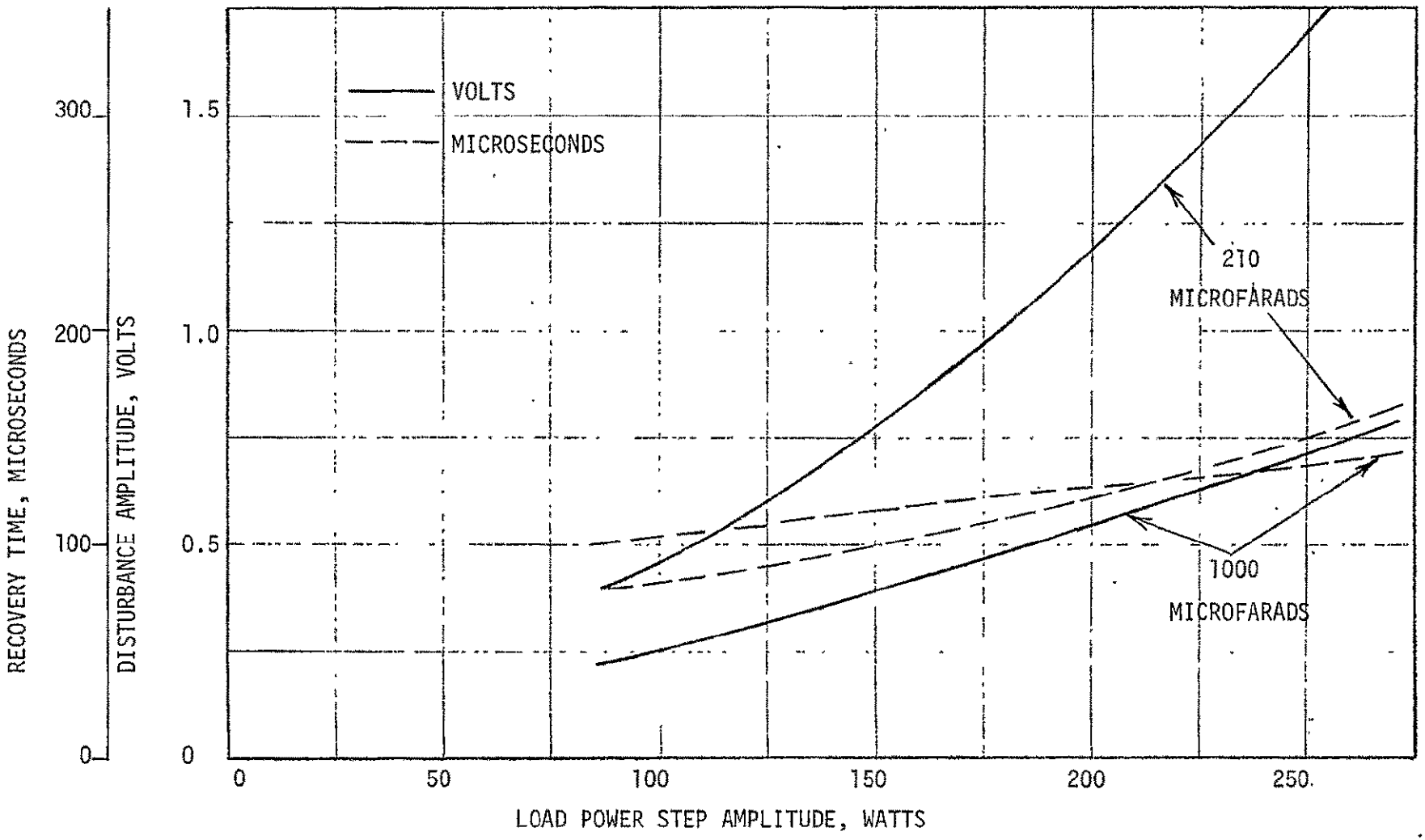


FIGURE H-12 STEP UNLOADING TRANSIENT RESPONSE

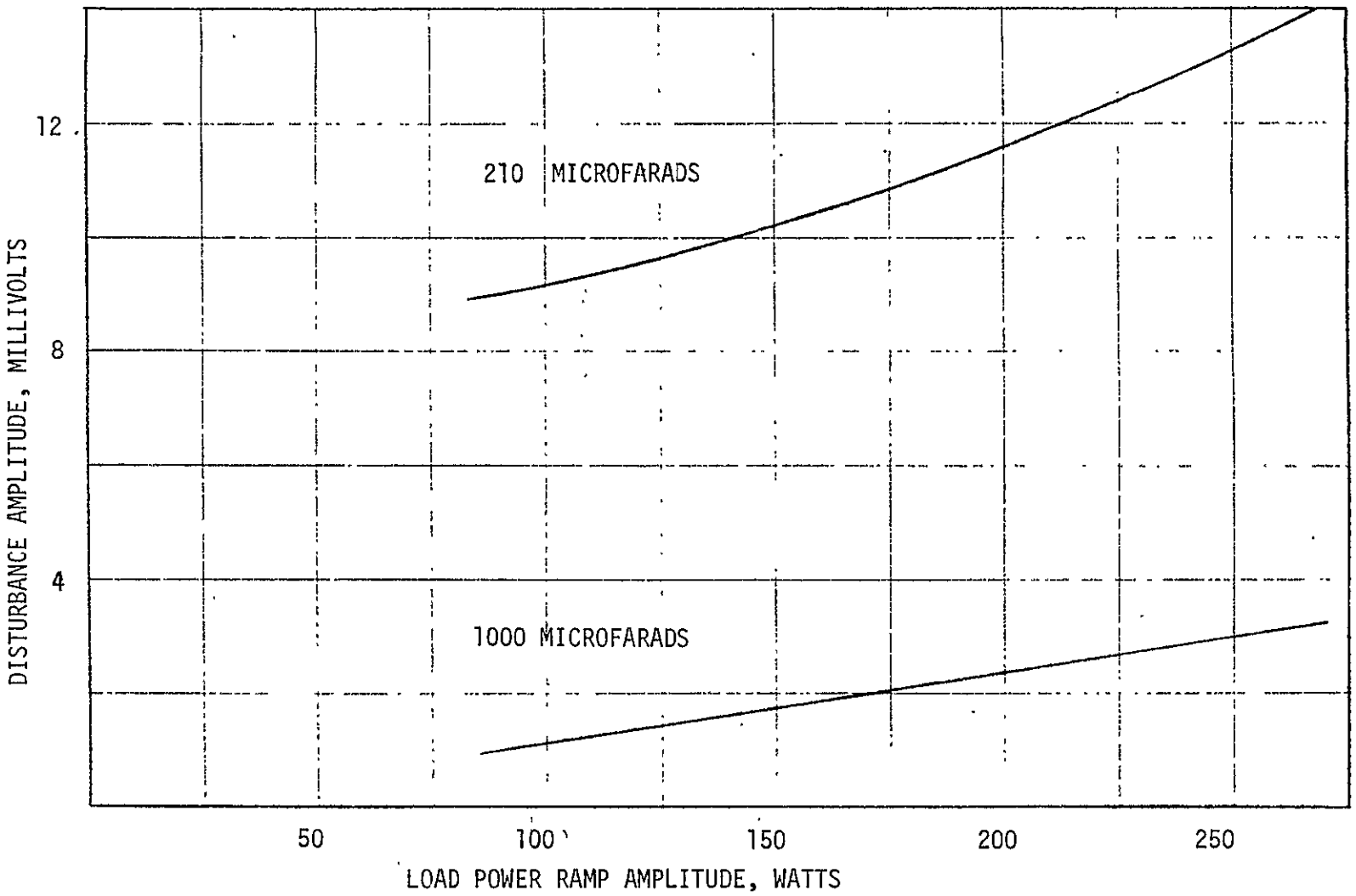


FIGURE H-13 RAMP LOADING TRANSIENT RESPONSE

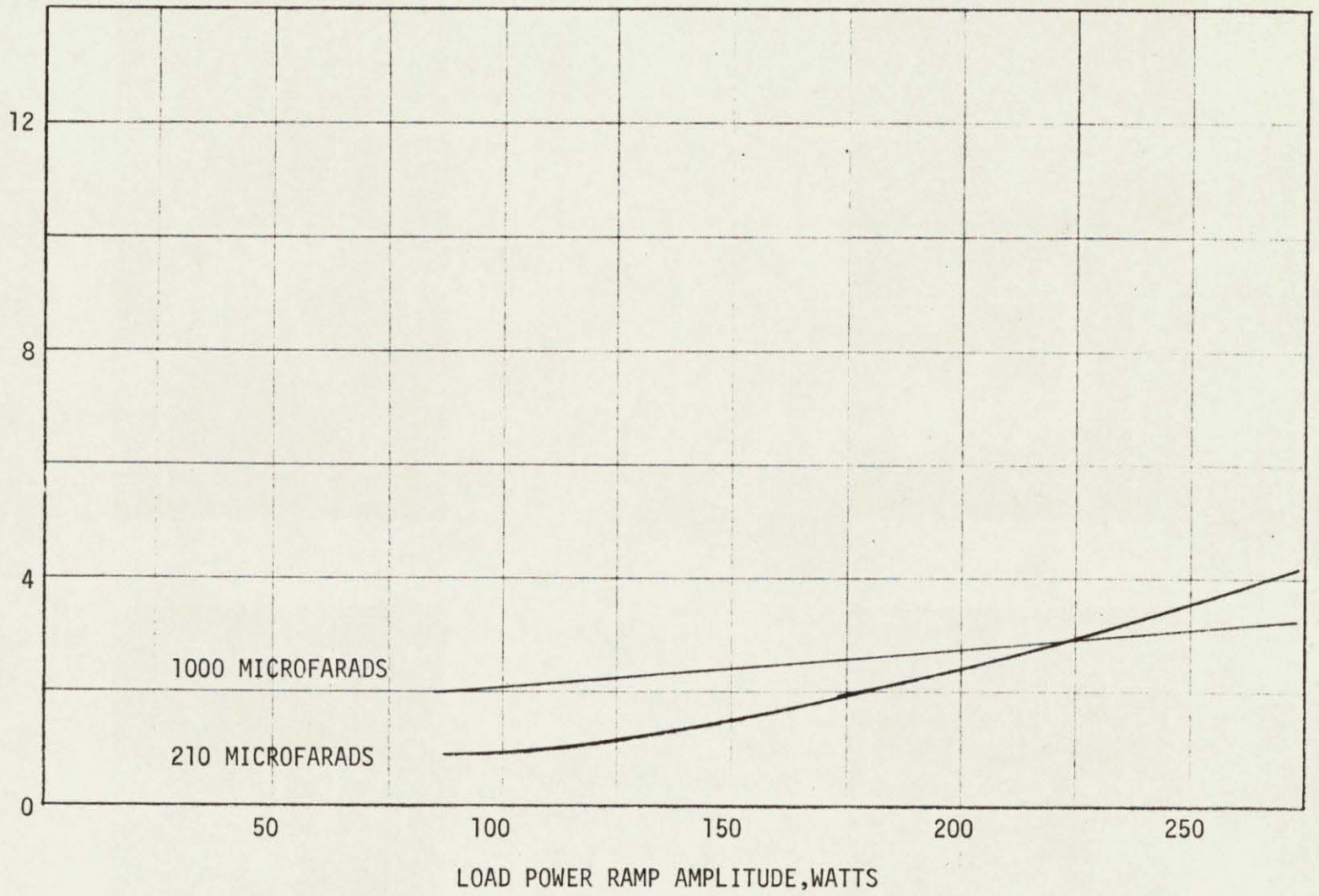
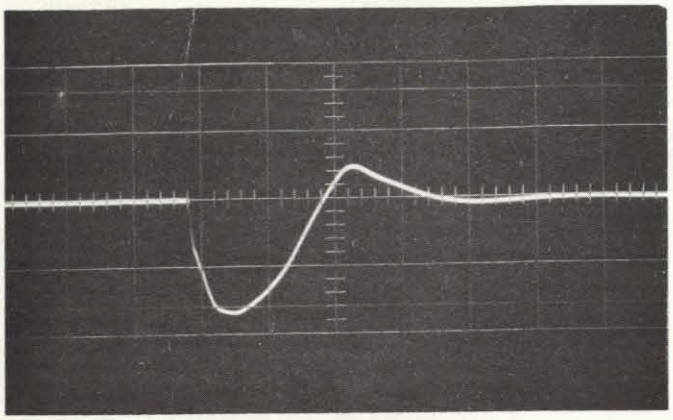


FIGURE H-14 RAMP UNLOADING TRANSIENT RESPONSE

STEP LOADING

C = 210 μf

3amps to 9amps

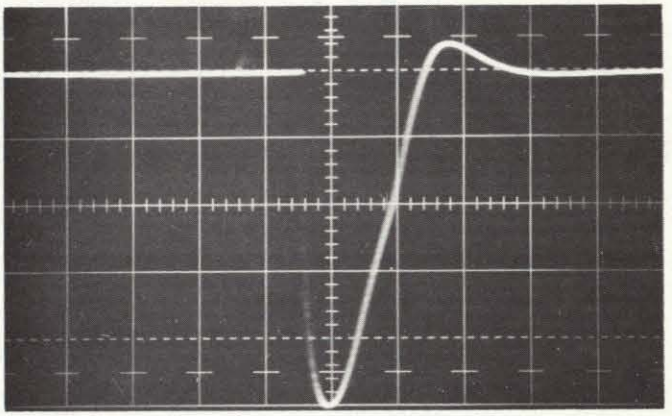


HORIZ: 50 μs/cm

VERT: .5v/cm

C = 1000 μf

3amps to 9amps



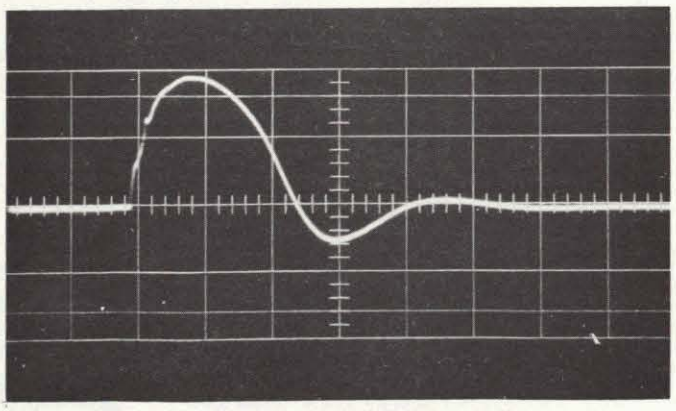
HORIZ: 50 μs/cm

VERT: .1v/cm

STEP UNLOADING

C = 210 μf

9amps to 3amps

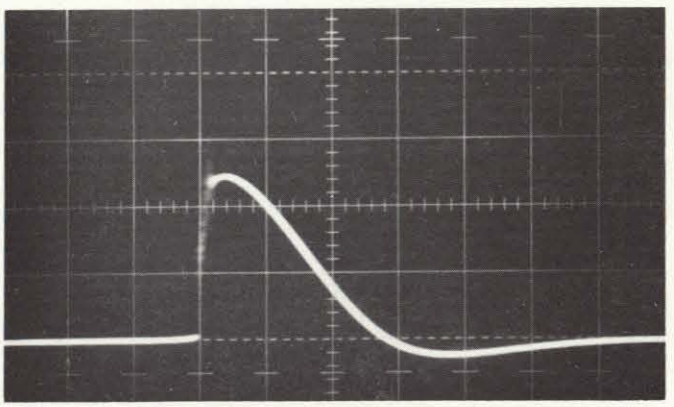


HORIZ: 50 μs/cm

VERT: .5v/cm

C = 1000 μf

9amps to 3amps



HORIZ: 50 μs/cm

VERT: .2v/cm

FIGURE H-15. TRANSIENT RESPONSE TO STEP LOADS

overshoot and undershoot of 300 millivolts and varying the load current and ramping speed. The results of this test are shown in the oscilloscope photos of Figure H-16.

Curves were plotted on Figures H-17 and H-18 showing the maximum rate of current change and the maximum total current change that could be tolerated and yet not exceed ± 300 millivolt distortion on the bus.

The standby power drain of the regulator is approximately 500 milliwatts and the shunting power transistor (2N3773) temperature rise above ambient (worst case) is 80°C, therefore at 40°C ambient environment, the maximum junction temperature is 120°C.

Shunt Regulator Response to Fault Loads

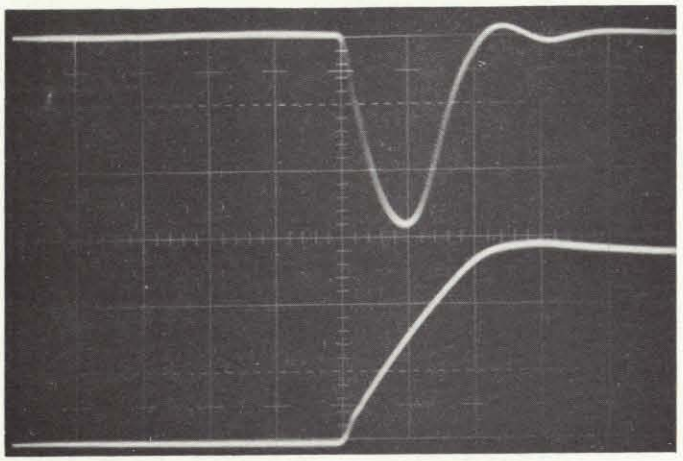
The shunt regulator was tested under fault load conditions. The source used is a simulated RTG shown in Figure H-19. The shunt regulator was operated at a minimum current (approximately .1 ampere), or at a current equal to the normal load prior to the application of the fault load. Fuses were used as the fault removal device. Load faults were applied up to four times the fuse rating.

Under these load demands the regulated bus voltage decreased to a level determined by the fault for a time period determined by the ratio of fault current to fuse rating. The regulated bus voltage dropped to levels as low as 14 volts for fault currents up to 16 amperes. After the fault was removed the bus voltage rapidly increased (within 1 - 3 milliseconds) to the required regulated voltage with an overshoot less than 1 volt. Typical traces are shown in Figure H-20.

RAMP LOADING

C = 210 μf

3amps to 9amps

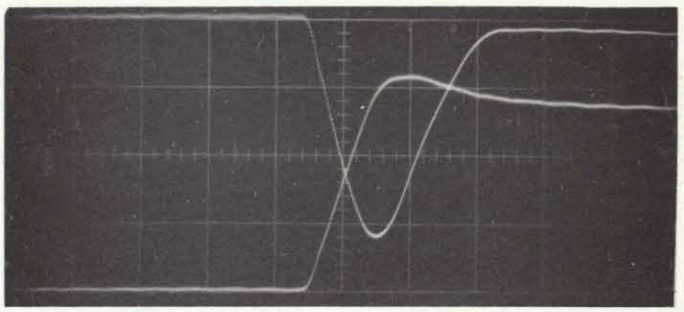


HORIZ: 50 μs/cm

	TOP	BOTTOM
VERT:	.1v/cm	2a/cm

C = 1000 μf

3amps to 9amps



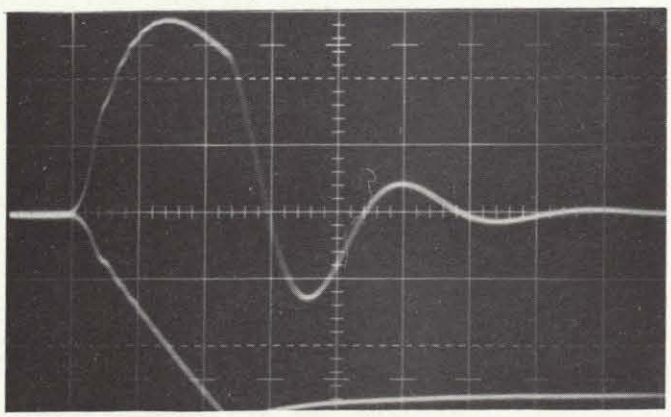
HORIZ: 50 μs/cm

	TOP	BOTTOM
VERT:	.1v/cm	2a/cm

RAMP UNLOADING

C = 210 μf

9 amps to 3 amps

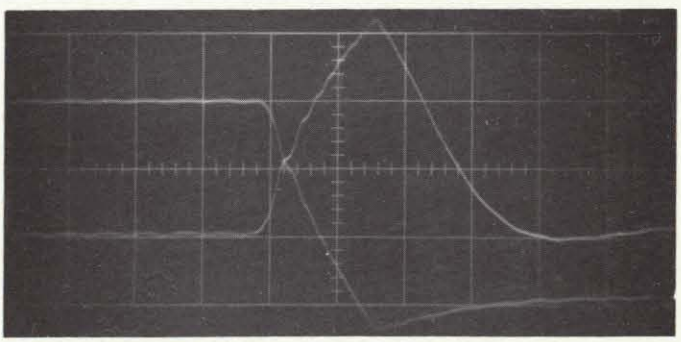


HORIZ: 50 μs/cm

	TOP	BOTTOM
VERT:	1v/cm	2A/cm

C = 1000 μf

9 amps to 3 amps



HORIZ: 50 μs/cm

	TOP	BOTTOM
VERT:	1v/cm	2A/cm

FIGURE H-16. TRANSIENT RESPONSE TO RAMP LOADS

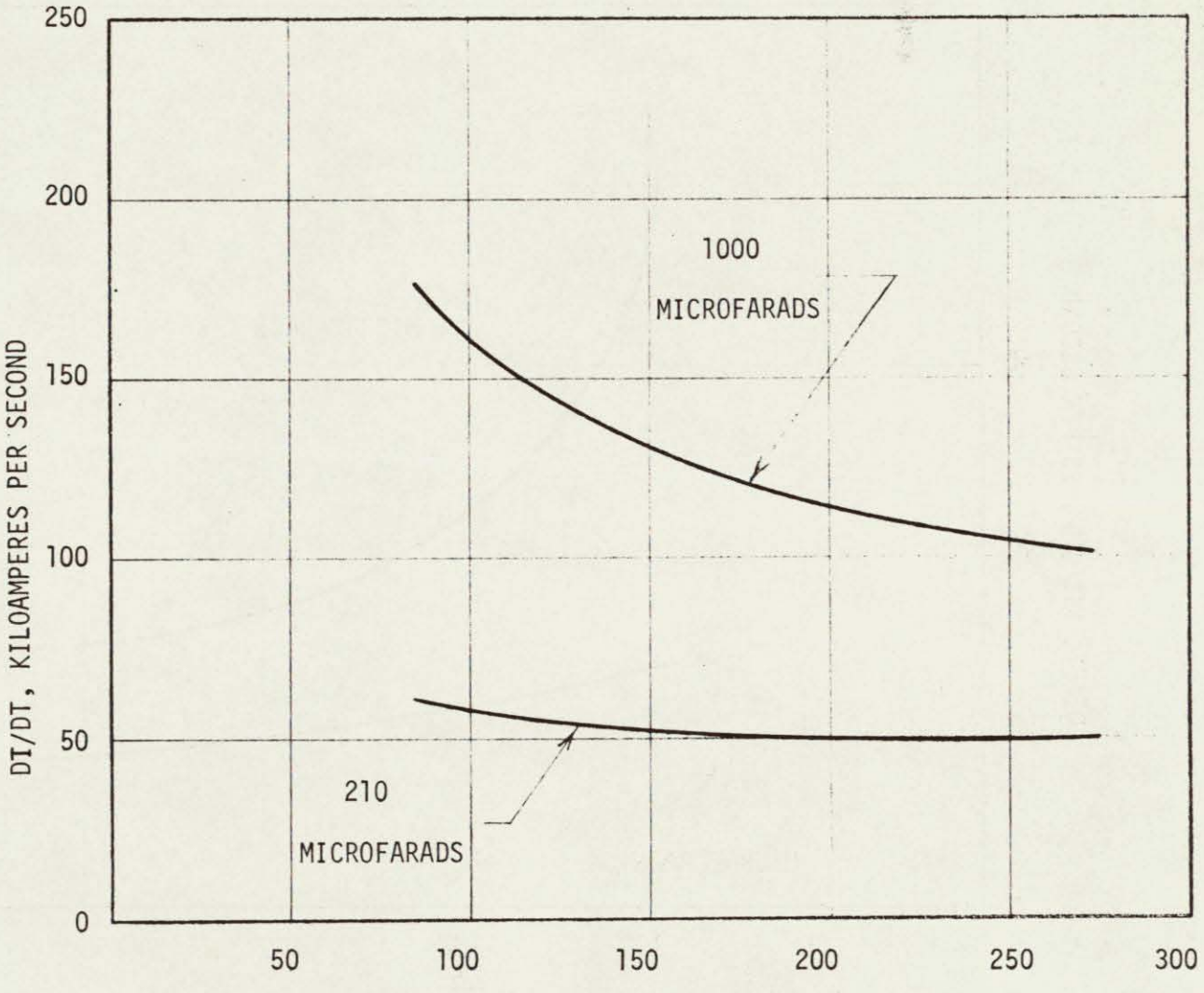


FIGURE H-17. ALLOWABLE POWER LOADING

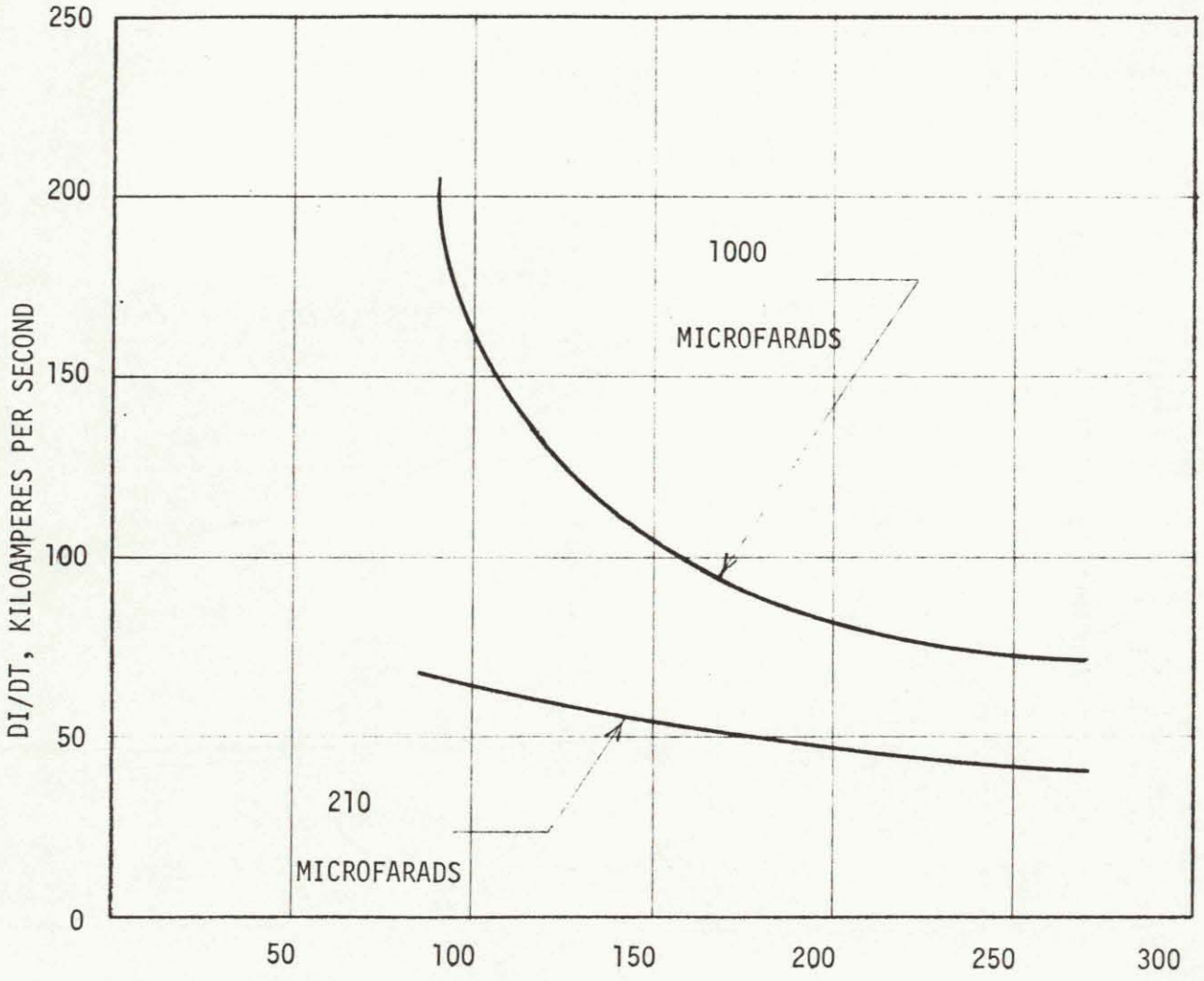


FIGURE H-18. ALLOWABLE POWER UNLOADING

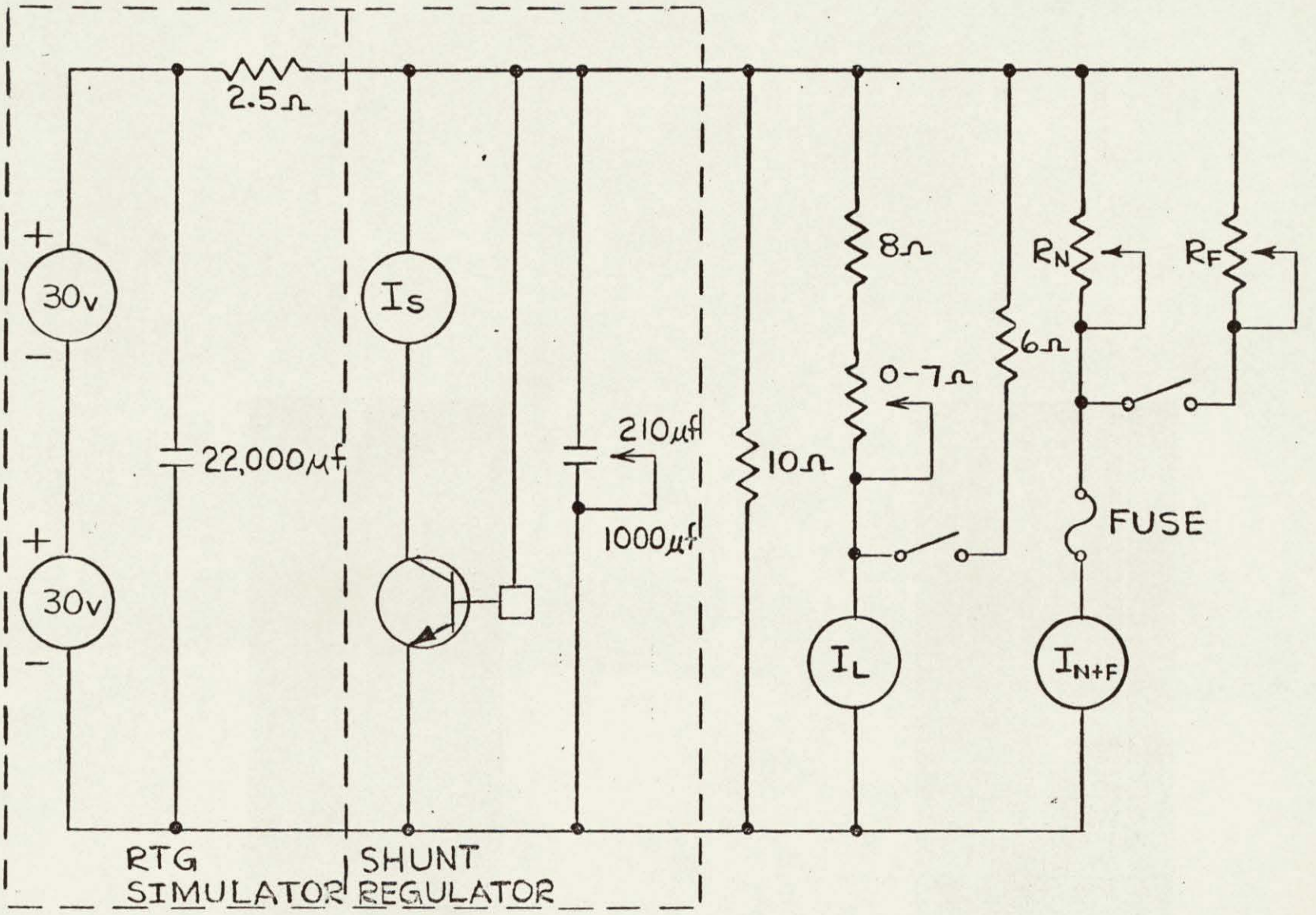
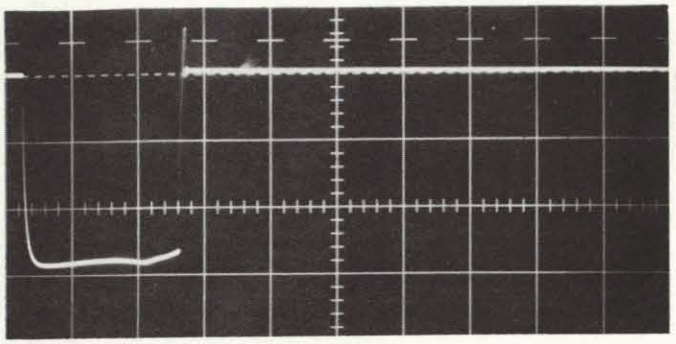


FIGURE H-19 FUSE TEST SCHEMATIC

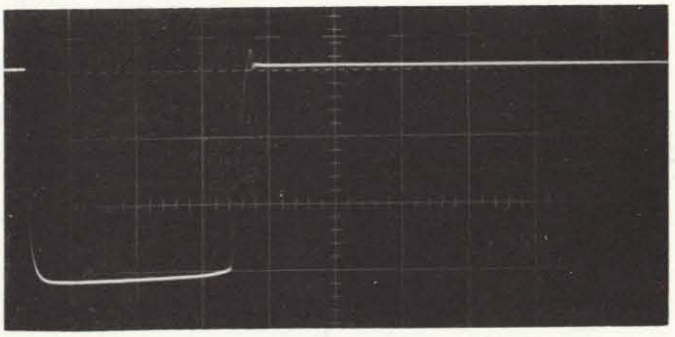
FUSE = .5 amp



HORIZ: 5ms/cm

VERT: .5v/cm

FUSE = 4.0 amp



HORIZ: 1ms/cm

VERT: 2v/cm

FIGURE H-20. TRANSIENT RESPONSE TO FUSED LOADS

For comparison, faults were generated with two different output capacitors (210 and 1000μF). The capacitor value did not greatly affect the regulator response under these operational conditions.

The majority of source faults were at a prescribed current of 2, 3 or 4 times the fuse rating. Figure H-21 is a system response for a short circuit fault. The peak current was approximately 90 amperes as a result of energy stored in the shunt regulator output capacitor. The system voltage returned to normal within 5 milliseconds.

A comparison was made between two output capacitor sizes to observe system effects with a short circuit fault. Figure H-22 is a comparison of the two responses. Note that in both cases system voltage returned in the same time period.

Finally, to demonstrate the ability of the Shunt Regulator to remain in operation under any random, single component failure, selected components underwent simulated failures both short and open. During any single component failure, the Shunt Regulator continued to operate within all specification requirements.

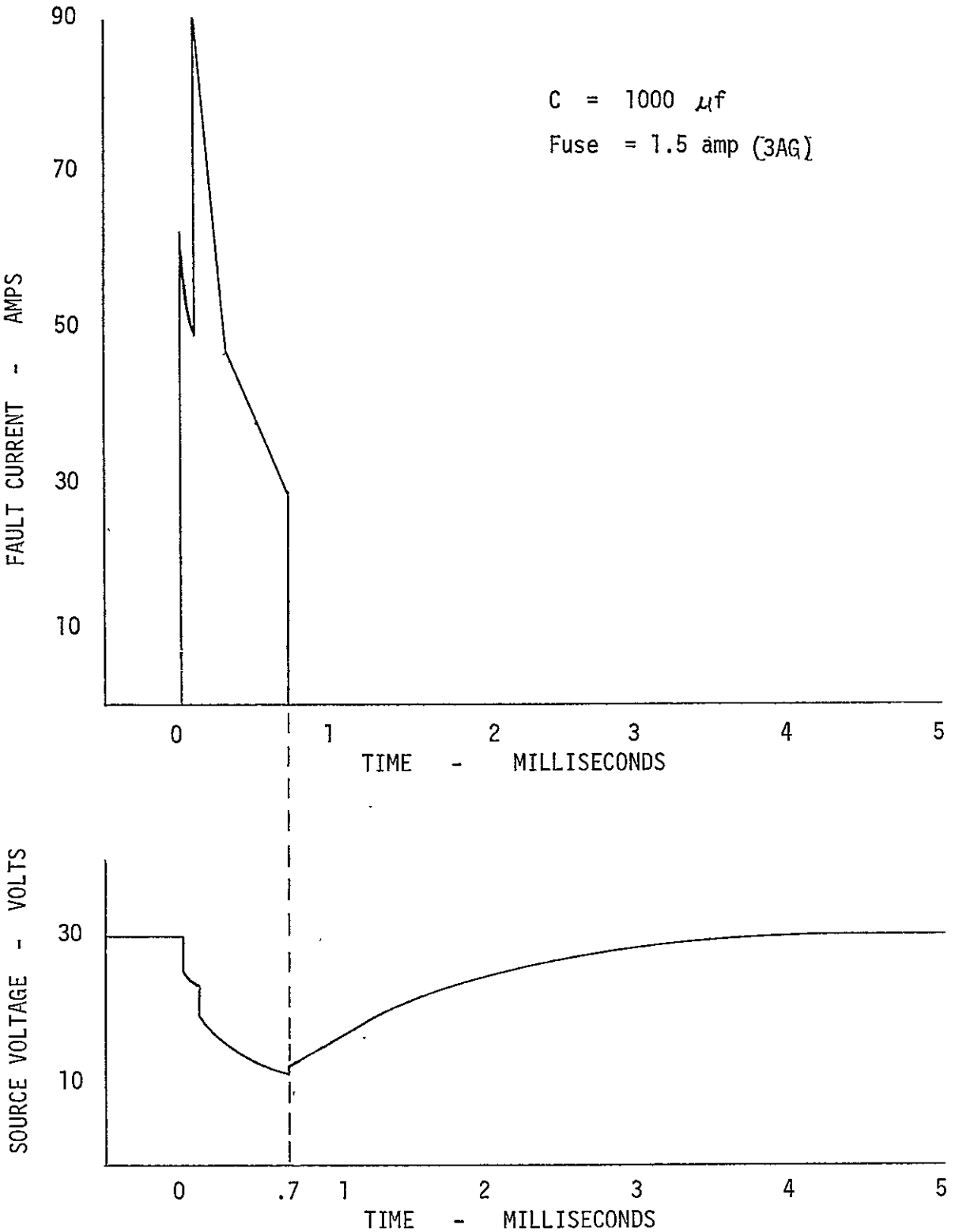
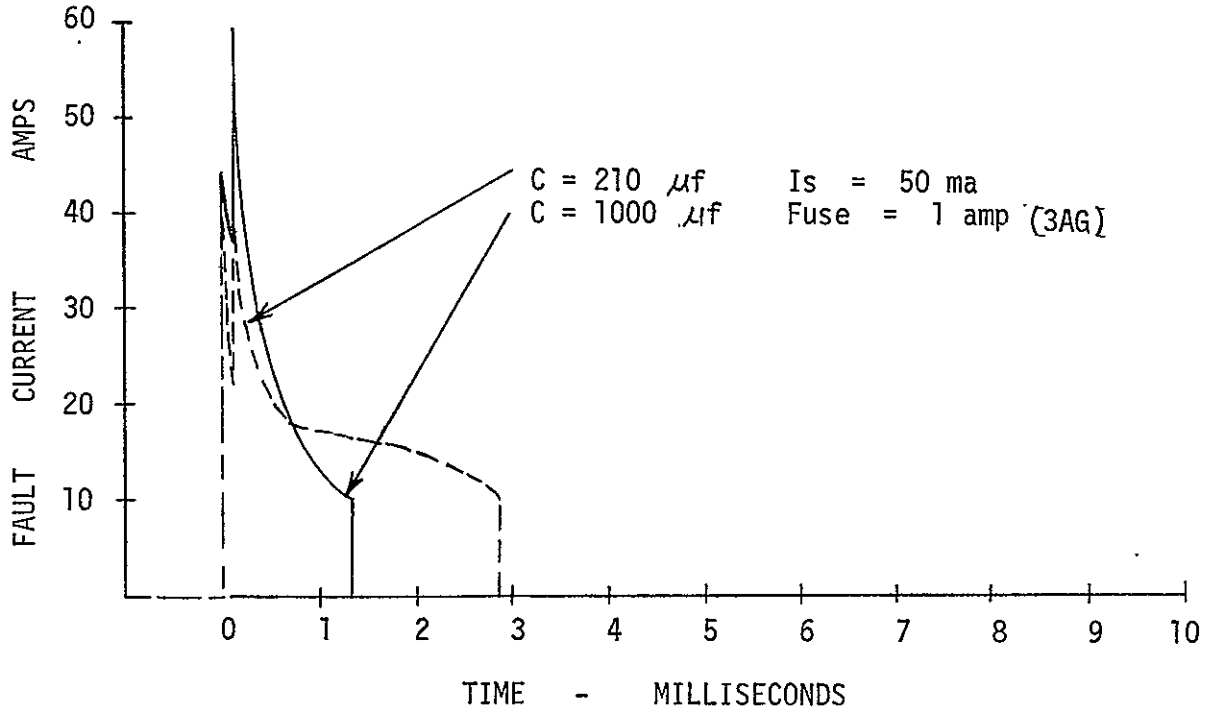


FIGURE H-21. SYSTEM RESPONSE TO A FAULT



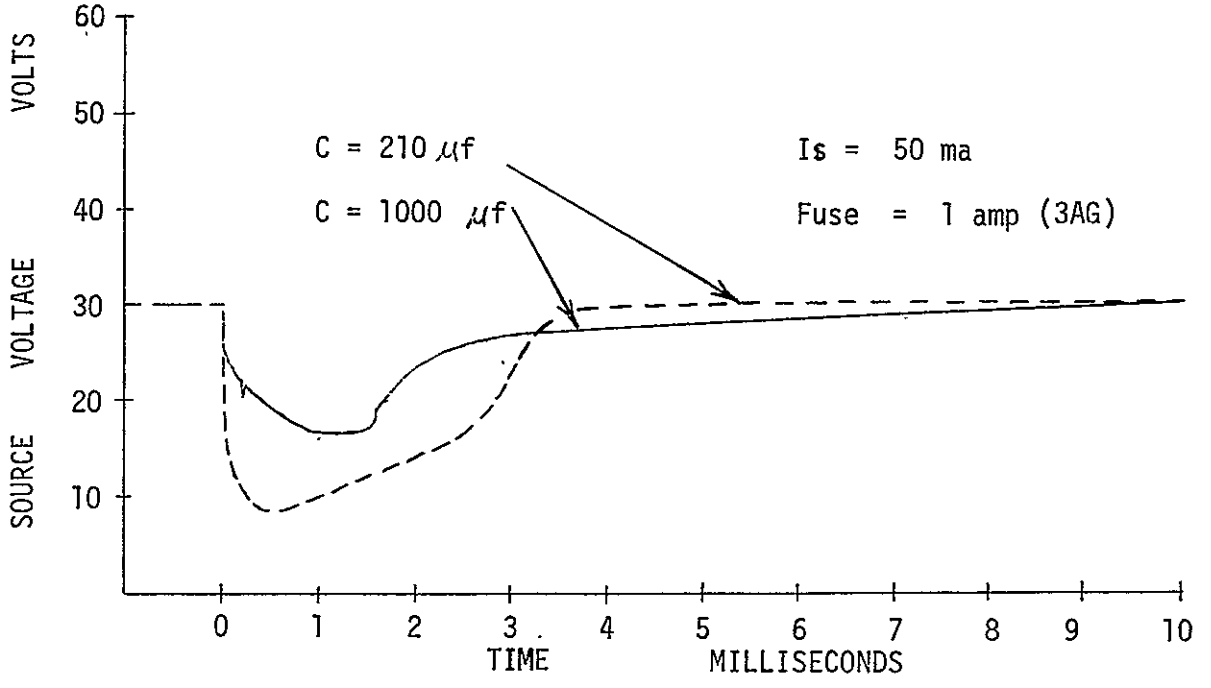


FIGURE H-22. CAPACITIVE FAULT CLEARING

APPENDIX I TWT CONVERTER DESIGN STATUS

A block diagram of the TWT Converter is shown in Figure I-1. Bus power is switched to the input filter, activating the filament supply. A driven oscillator chops the DC power to square wave AC, and a transformer reduces the voltage to the 5.2 volts required by the filament. The current limiting function is provided by the highly reactive design of the transformer.

A ninety second time delay inhibits power to a second driven oscillator until the filament has warmed up. This oscillator then chops the DC power to square wave AC which is transformed to higher than required voltages, rectified, filtered, and adjusted to the required output level by a series impedance. The helix and collector supplies are series regulated with a dissipative transistor regulator; and the anode potential, operating at constant current, is adjusted with a variable resistor.

The current limiting for the filament supply could be achieved with a saturable reactor, phase controlled rectifiers on the transformer output, dissipative regulation on the transformer DC input, or current limiting at the transformer itself. The high reactance transformer method was selected on the basis of simplicity, efficiency and reliability. It adds no parts over those required for the basic functions of chopping and transformation; it adds no in-line semiconductor voltage drops on the low voltage side of the transformer, and the reliability is equal to the basic reliability of the circuit without current limiting, since no additional failure modes are introduced.

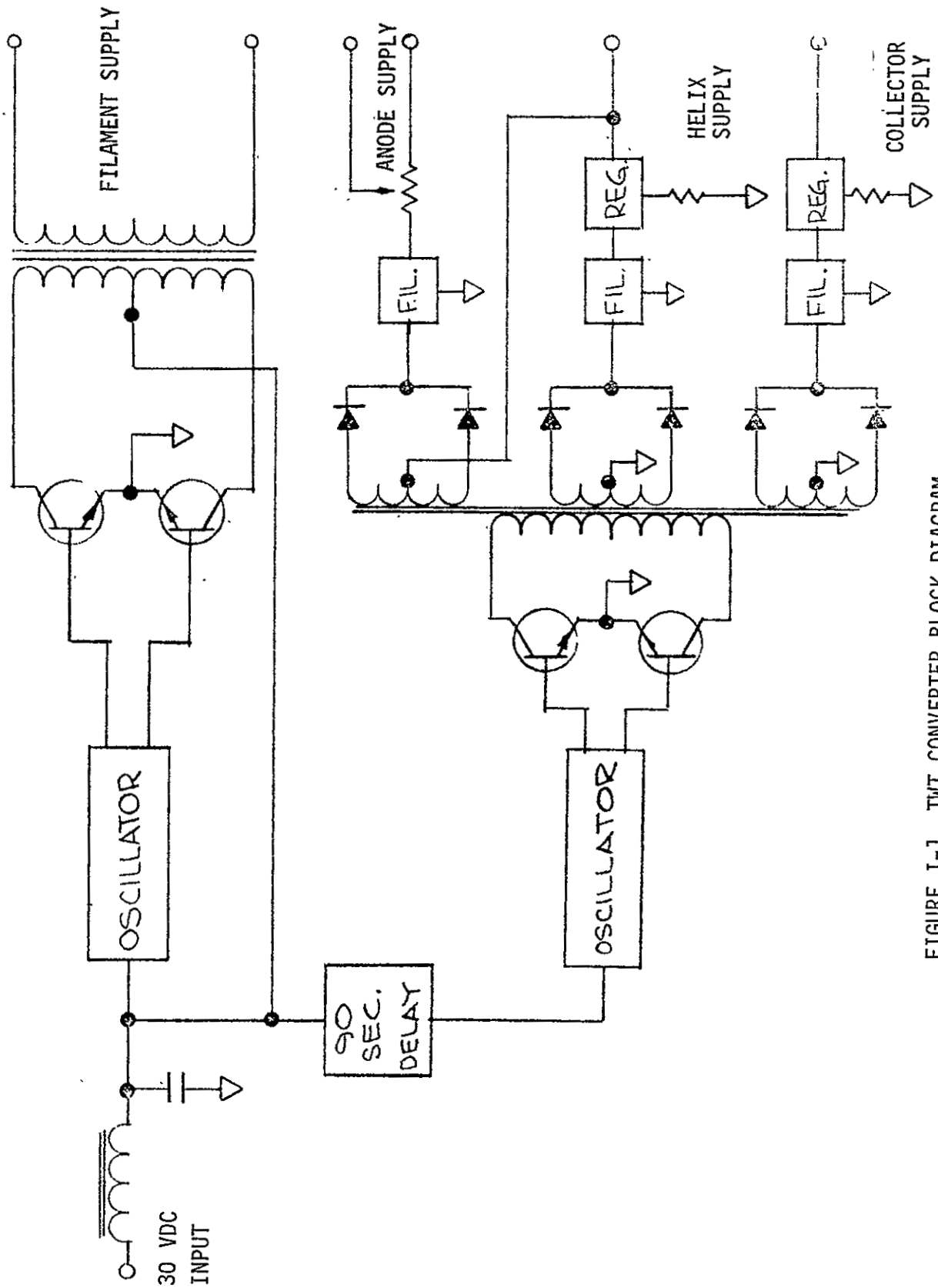


FIGURE I-1 TWT CONVERTER BLOCK DIAGRAM

The transformer is constructed on a cut "C" core, with two separate coils. One coil contains all the primary windings, and the second coil all the secondary windings. Sufficient space is left on the core window between these coils to short the magnetic path from one core leg to the other, and this is accomplished with a second cut "C" core orthogonal to the first as shown on Figure I-2. The current limiting can be adjusted by varying the air gap, and typical test data on the first transformer at room ambient is shown on Figure I-3. It can be seen that the current to be delivered at a prescribed voltage can be adjusted by varying the air gap; and that a normal operating voltage point at about sixty percent of open circuit will have a corresponding short circuit current of twice the value at the sixty percent point.

The precise output voltage for the helix and collector must be regulated against load change. This requires some form of closed loop regulator on the output voltage. Figure I-4 shows a limited range transistorized, high output voltage regulator that operates in the linear mode to achieve the required regulation and which also acts to further attenuate ripple appearing at the output of the rectified and filtered high voltage power lines from the converter. The full output voltage of the supply is sampled by the resistor string composed of R7, R8 and R4. A portion of this voltage is compared against a zener reference, CR1, which is biased into the breakdown region by current flowing through resistor R6. The design requirement for this limited range regulator is that the current flow through R4 must be held constant.

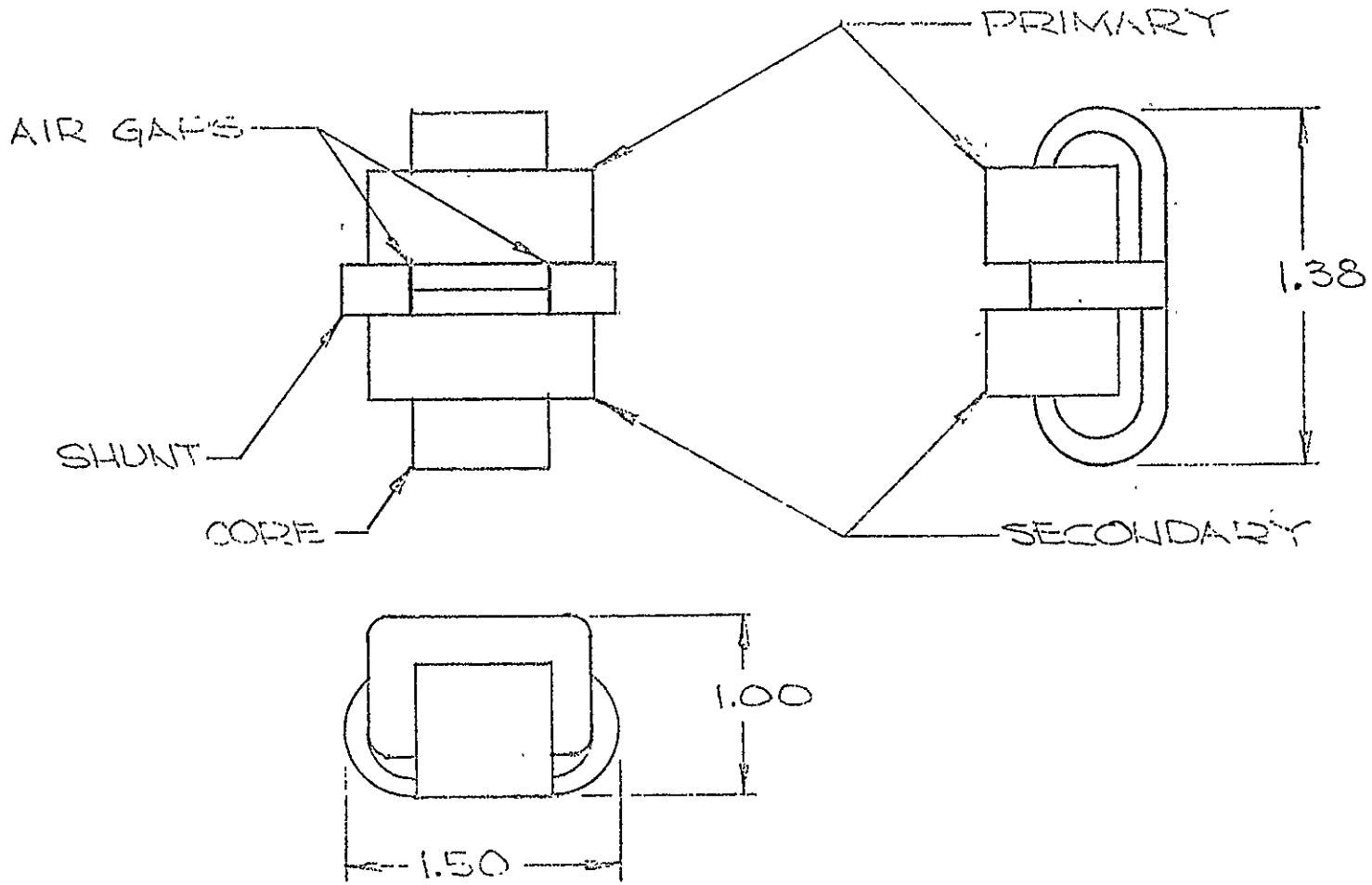
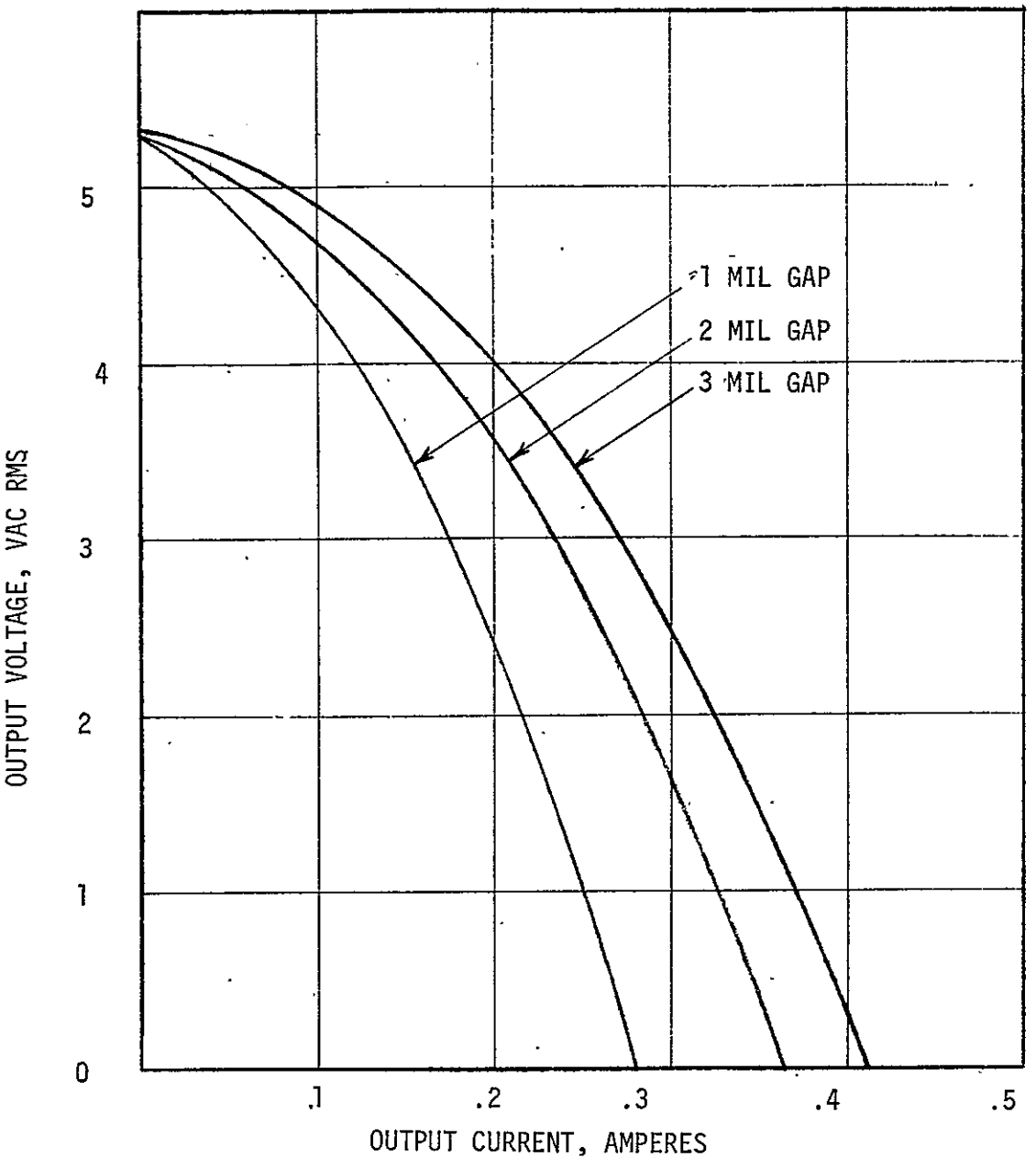
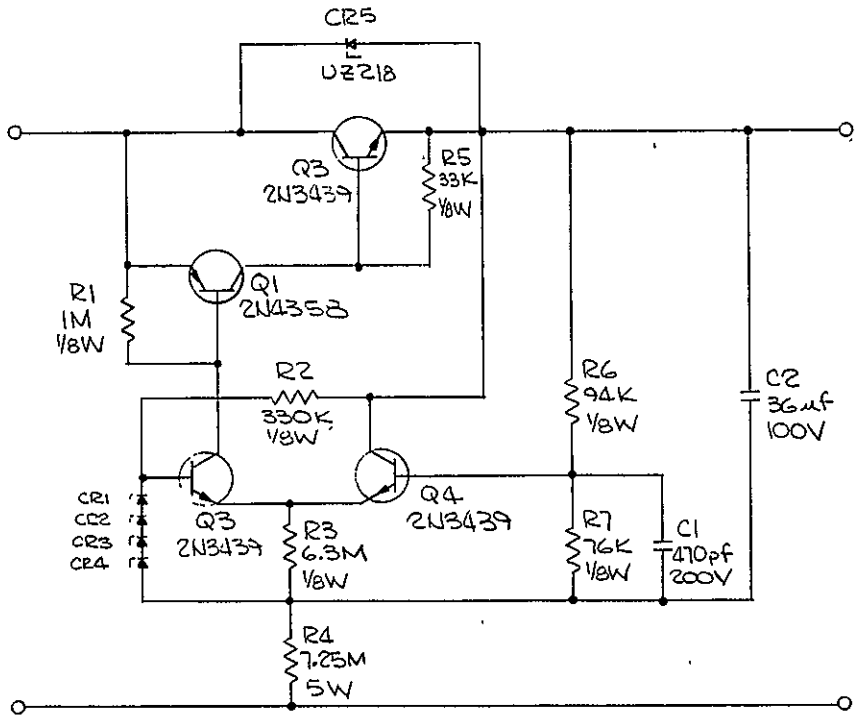


FIGURE I-2 HIGH REACTANCE TRANSFORMER



FI GURE I-3 FILAMENT SUPPLY REGULATION



CR1, CR2, CR3 & CR4 - FCT 1135

FIGURE I-4 HIGH VOLTAGE SERIES REGULATOR

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

SIGNATURES	DAY	MO	YR
DRAWN	18	8	69
CHECKED			
ISSUED			
CHARG			
MFG			
MATLS			

GENERAL ELECTRIC
DEPT LOC

TOPS
TWT 3450V ±5% (20W) REGULATOR

SIZE C | CODE IDENT NO

SCALE ~ | SHEET 1 OF 1

1J86-TOPS-513

FN903 F (5-68)
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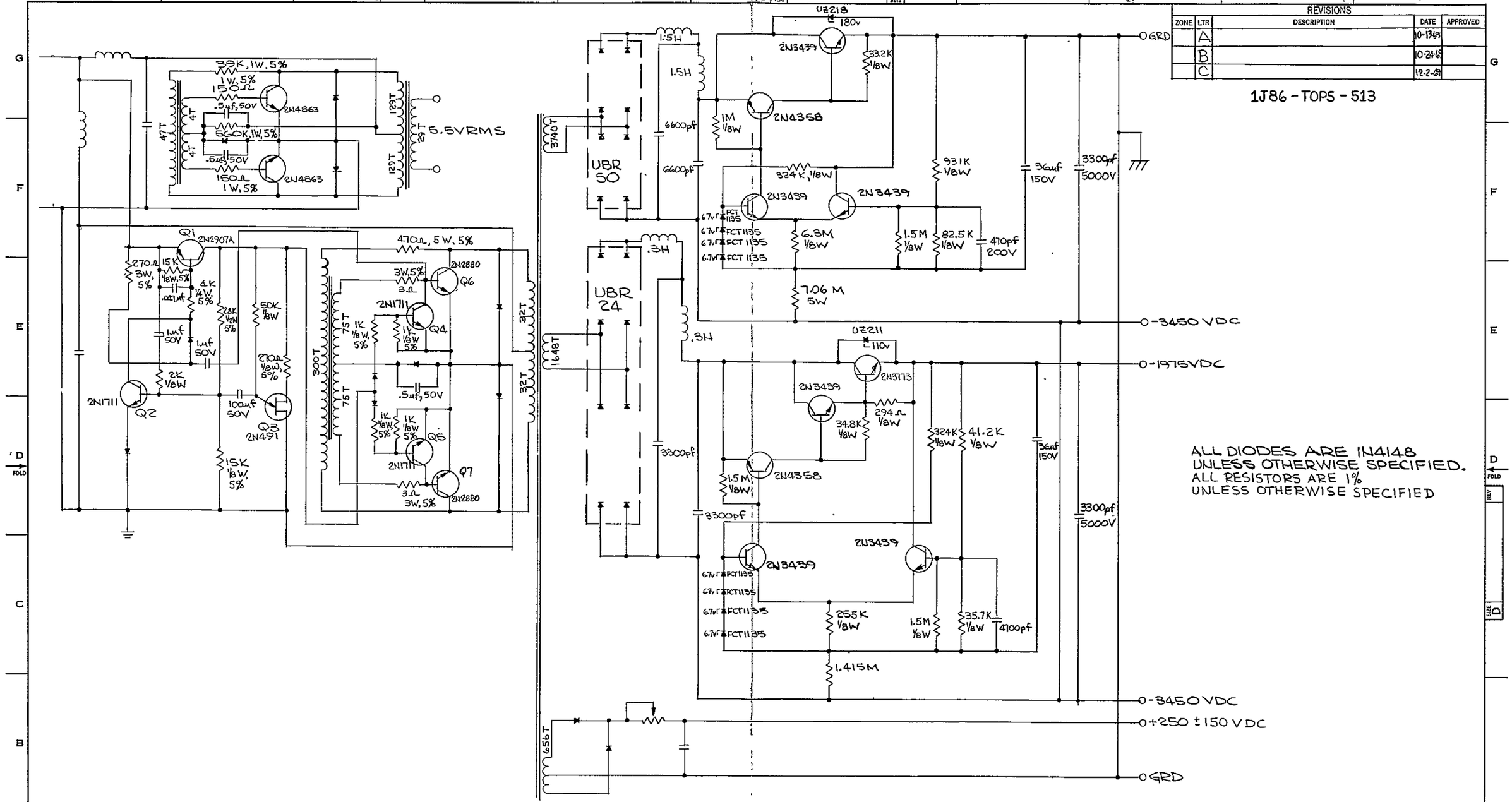
Full schematic of all circuit elements is shown on Figure I-5. The added feature here is a time delay circuit established by a unijunction transistor (Q3) which activates a series switch, transistor Q2, to provide starting base drive current to the oscillator transistors, Q4 - Q6 and Q5 - Q7.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A		10-13-67	
	B		10-24-67	
	C		12-2-67	

1J86 - TOPS - 513



ALL DIODES ARE 1N4148 UNLESS OTHERWISE SPECIFIED.
ALL RESISTORS ARE 1% UNLESS OTHERWISE SPECIFIED

I-8 FIGURE I-5 TWT CONVERTER SCHEMATIC

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES— TOLERANCES ON 2 PLACE DECIMALS ± 3 PLACE DECIMALS ± ANGLES ± FRACTIONS ± MATERIAL—	ALL SURF. ✓	SIGNATURES	DAY	MO	YR
		DRAWN J.A. Martin	30	9	69
		CHECKED			
		ISSUED			
		ENGRG			
		MFG			
		MATLS			

GENERAL ELECTRIC
DEPT LOC

TOPS
TWT CONVERTER

SIZE	CODE IDENT NO	
D		

SCALE ~ SHEET 1 of 1

FOLDOUT FRAME 1

FOLDOUT FRAME 2

APPENDIX J COMPARISON OF AC MOTOR DRIVE CIRCUITS

Three AC motor drive circuits were compared to permit a recommendation for the circuitry to power the gyro and momentum wheel requirements of the attitude control system. For evaluation purposes, the output voltage is assumed to be 26.0 VRMS for all cases. This results in a continuous power requirement of 12 watts and a peak (stall) power requirement of 20 watts, with an assumed power factor of 0.50.

The driver circuits for each configuration will accept two phase square wave signals from an on-board clock. The drive requirements would be essentially identical for both phases and for each type of power stage presented here. The driver input impedance would be greater than ten kilohms which is more than sufficient to prevent loading of the clock.

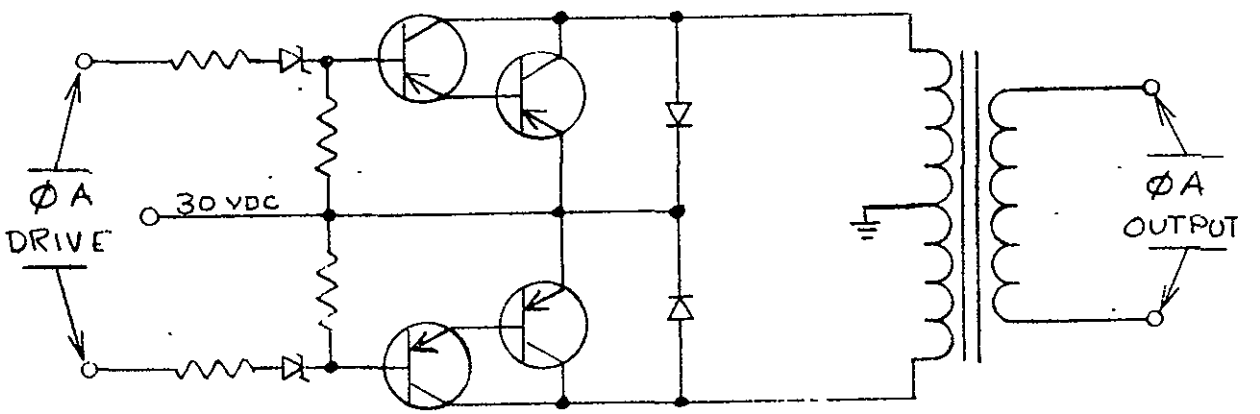


FIGURE J-1. DIRECT DRIVE, ISOLATED OUTPUT

In this approach, a power transformer with center tapped primary is required in each phase. The power transistors alternately switch power from one half of the primary winding to the other half. This results in having only one switch voltage drop in series with the load at any time. The darlington driver provides the most efficient means of driving the power switch directly from the clock.

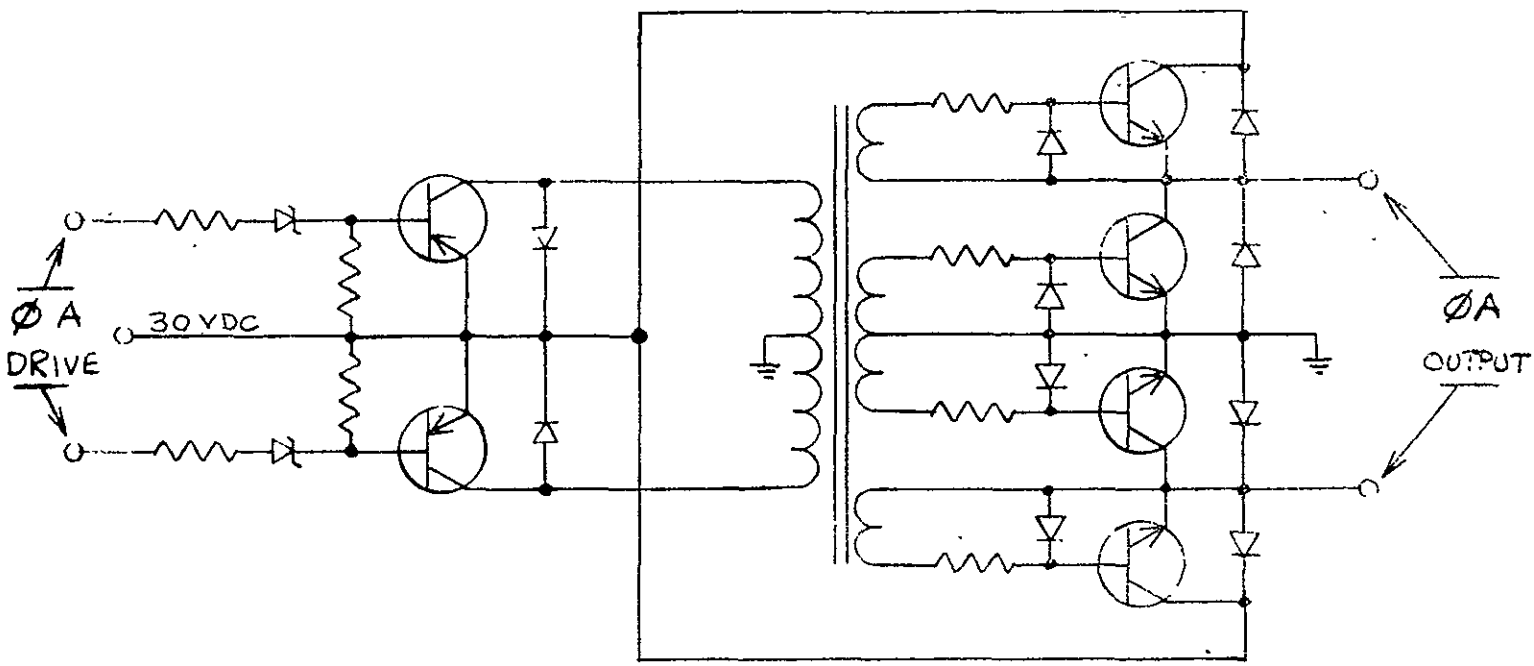


FIGURE J-2. ISOLATED DRIVE, DIRECT OUTPUT

The initial stage in this circuit operates exactly as does the circuit of Figure J-1. However, the transformer supplies base drive to a transistor bridge circuit instead of the load. The resulting reduction in required source current eliminates the need for darlington input switches.

The bridge provides the required AC by alternately switching power and returns through two transistors at each end of the load. Thus, there are two saturation voltage drops in series with the load at any time. However, the RMS voltage delivered to the motor is equal to the source minus two transistor voltage drops, or approximately 29.0 VAC RMS. A second consideration is that both ends of the motor winding must be isolated, since each is alternately connected directly to the 30 volt bus.

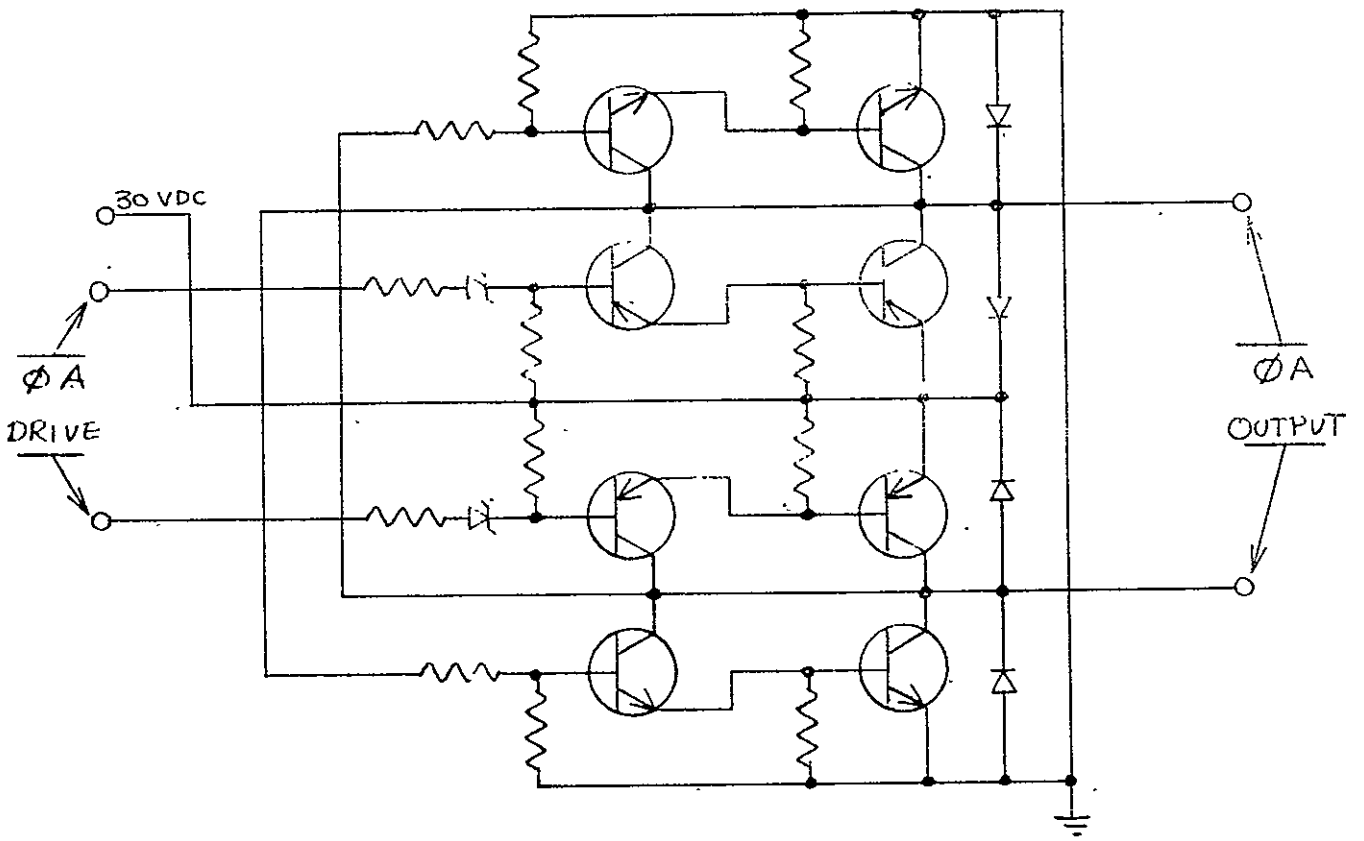


FIGURE J-3. DIRECT DRIVE, DIRECT OUTPUT

In this circuit, the signal input is applied directly to an NPN darlington pair which forms the bottom leg of the bridge. The top leg, consisting of a PNP darlington pair, receives its drive from the corresponding bottom switch.

In this manner, the need for a transformer is eliminated. However, each switch requires a darlington configuration which results in a higher saturation voltage drop than that of a single transistor (a typical drop for two transistors would be 1.5 to 2 volts). Also, as in the output bridge of circuit 2, there will be two switch voltage drops in series with the load at all times. This circuit more nearly matches the 26 VAC RMS motor requirement, but still requires isolated motor windings.

Tradeoff Characteristics

The circuit of Figure J-1 offers the following major advantages:

1. Low complexity
2. Output voltage flexibility
3. Isolation
4. High efficiency

The low complexity would indicate a high reliability, however, any increase in reliability would be offset to some extent by the very high failure rates usually applied to magnetic components. The output flexibility and isolation advantages would seem to be of importance in this particular application since the gyro requires approximately 26 VRMS and is a three wire device.

The efficiency of this circuit would approach 90%, however, it should be remembered that the magnitude of the losses in this application is very small -- approximately 60 mw per % of efficiency. Therefore, any efficiency greater than perhaps 85% would be acceptable.

The major disadvantage of this approach is the size and weight of the power transformers. The two six watt transformers required (one each phase) could weigh up to one-half pound and would account for most of the total supply weight.

In the circuit of Figure J-2, the transformer provides base drive for the transistor bridge. If a forced gain of 10 (the usual value for power switches) is used, the transformers must provide one tenth as much power. Since the primary voltage is constant, the only factor contributing to a reduction in size is less current -- therefore, smaller wire. The number of primary turns will be equal to or greater than (for a smaller core) that of the power transformer. The total number of secondary turns would be no less than half of the power transformer approach. The net result is that a driver transformer will be at least half the size of a power transformer. Since additional power transistors are required, the overall size and weight of this circuit will be approximately the same as that of Figure J-1.

The attractiveness of the circuit of Figure J-2 is further reduced by the increased complexity (approximately 3 times that of Figure J-1) required in the bridge output. This would cause a substantial decrease in the reliability figure of merit. Another factor affecting reliability is the lack of DC isolation. Any bridge circuit is highly vulnerable to failure due to inadvertent grounding of either output terminal.

The efficiency of the circuit of Figure J-2 would be slightly better than that of the first circuit even though there are two switches in series with the load. This is due to the single transistor voltage being less than one half that of a darlington. The efficiency increase, however, would be small.

The output voltage of a bridge inverter is reasonably fixed at something less than the bus voltage. In the circuit of Figure J-2, it would be about 29 VRMS. In the forced gain configuration, the saturation drop will not change significantly over a fairly wide load range (say 5 to 1). The output voltage regulation will, therefore, be better than 5% from stall to running loads.

The circuit of Figure J-3 has a complexity similar to that of Figure J-2; however, the reliability will be better due to the lack of a transformer. The output voltage will be about 28 VRMS due to the greater saturation voltage drop of the darlington stages. This drop also reduces the overall efficiency to perhaps 80%.

The greatest advantage of this circuit is size and weight. At the required power level (6 watts per phase), this circuit would not weigh more than 3/4 pound for both phases (depending upon packaging).

Summary

In the table below, a summary of the trade-off consideration given each configuration is presented. The data is for a completely packaged two phase supply, but does not include input filtering. The size and weight figures are estimates and the efficiency and regulation are calculated approximate worst case.

Circuit	Size	Weight	Efficiency	Regulation	Reliability
J-1	20 in^3	1.25#	88%	3%	0.9243
J-2	20 in^3	1.25#	89%	5%	0.8505
J-3	10 in^3	0.75#	80%	5%	0.8541

The reliability was calculated on a part count basis using TOPS failure rates and a design life of twelve years. It serves as a relative indication of reliability.

APPENDIX K DC CONVERTER DESIGN CONSIDERATIONS

Introduction

The following is a summary of the design of the DC/DC converter shown in Figure K-2. A functional block diagram of the converter is as shown in Figure K-1 below and the design of each block will be discussed.

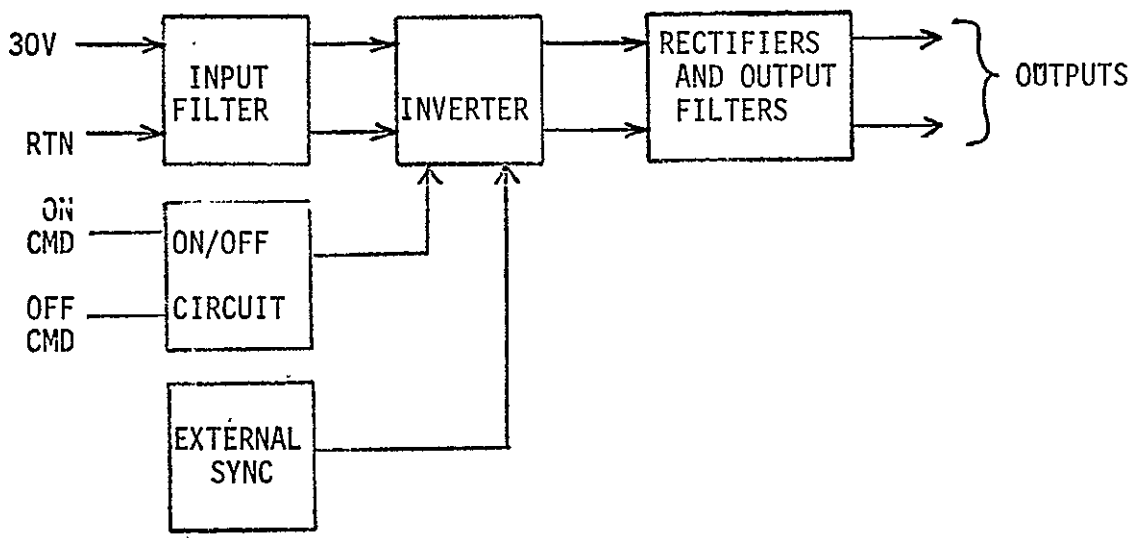


FIGURE K-1 CONVERTER BLOCK DIAGRAM

Input Filter

A filter was designed and developed in order to control radiated emission, conducted emission, audio frequency susceptibility, radio frequency susceptibility, transient susceptibility and rate of current changes (di/dt) on input power lines. The configuration features a unique application of a one millihenry transformer with its primary in series with the unregulated power line. The transformer acts as an inductor and as an impedance transformer

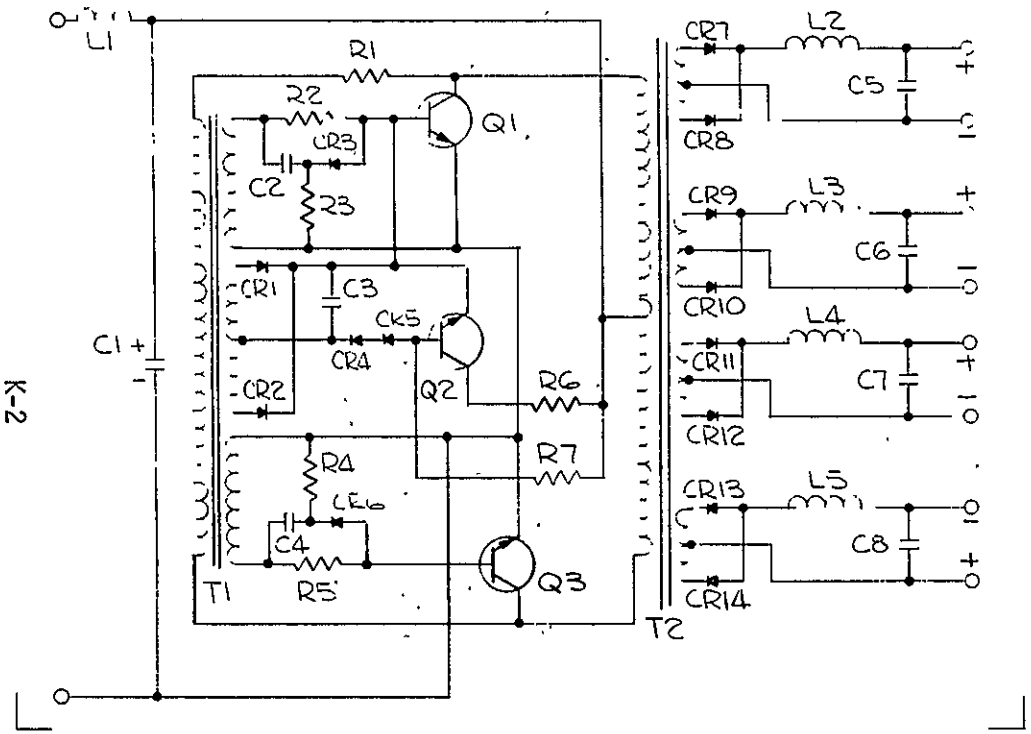


FIGURE K-2 DC TO DC CONVERTER SCHEMATIC

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES— TOLERANCES ON 2 PLACE DECIMALS ± 3 PLACE DECIMALS ± ANGLES ± FRACTIONS ± ALL SURF. ✓ MATERIAL—

SIGNATURES	DAY	MO	YR
DRAWN			
CHECKED			
ISSUED			
ENGRG			
MFG			
MATLS			

GENERAL ELECTRIC DEPT LOC

SIZE C | CODE IDENT NO | SCALE | SHEET

1J86-TOPS-513

FN903-F (5-68) PRINTED IN U.S.A.

that couples a variable impedance to the primary to provide AC noise attenuation, but dissipates no DC power. The filter also includes one fifty microhenry high frequency inductor in each input power line, followed by 150 microfarad capacitors from each line to a chassis ground. These inductors and capacitors act as a low pass filter for DC, and the chassis ground acts like a noise sink for any AC noise.

Inverter

The inverter is a basic Jensen oscillator with a transistor starting circuit. T1 is a switching transformer with a square permalloy 80 core. The design of T1 and the value of the resistor R1 determine the oscillating frequency. R1 also acts to limit the current when T1 saturates. R2 and R5 limit the current to the bases of Q1 and Q3 respectively while C2 and CR3, and C4 and CR6 increase the switching speeds of their respective transistors.

The transistor Q2 and the resistors R6 and R7 comprise the starting circuit which provides an initial current pulse to the base of Q1 insuring that the converter will begin to oscillate. After oscillation has begun, Q2 is back biased by the switching transformer, T1, and thus is turned off.

T2 is the power transformer which transforms the input voltage to the desired output levels and also provides isolation between the input and output and between outputs. A silicon iron "C" core with an inherent air gap is used for T2 because this type core does not saturate and therefore does not produce large current spikes when the switching transistors are not closely matched.

Rectifying and Filtering Output

The outputs of the inverter are rectified and then passed through a passive LC filter. The filtering smooths the commutation losses during the switching intervals and restricts the ripple within the limits of the particular load requirements. In addition to the filter network shown, there is a radio frequency interference filter attached to each output to remove the high frequency spikes caused by the switching transistors.

Power Supply On/Off Command Capability

The power supply will have the additional capability of being turned on and off upon command. The command lines will be 5V TTL. On command a 25-75 ms duration pulse will be initiated on these lines. There will be two discrete lines and commands, one to turn the power supply on and the other to turn it off. The circuit which will turn the power supply on or off is a solid state latching type which will be actuated by the commands described above. This capability has not been completely designed at this time.

Power Supply External Sync

The power supply must be capable of accepting a sync signal from the vehicle clock to prevent beat frequencies between converters which could affect magnetometer performance. This feature is to be included with the command capability change described above.

DC/DC Converter Weight Analysis

A weights analysis for a 5 watt, 4 output; and 16 watt, 4 output dc/dc converter was performed, and the results are tabulated in Table K-1.

FOLDOUT FRAME 1

TABLE K-1 DC TO DC CONVERTER WEIGHT BREAKDOWN

PART DESIGNATION	PART WEIGHTS (LBS.) 5 Watts 4 Outputs	16 Watts 4 Outputs
Q1	.007	.020
Q2	.007	.020
Q3	.007	.007
R1	.003	.005
R2	.001	.003
R3	.001	.001
R4	.001	.001
R5	.001	.003
R6	.001	.001
R7	.001	.001
CR1	.0005	.0005
CR2	.0005	.0005
CR3	.0005	.0005
CR4	.0005	.0005
CR5	.0005	.0005
CR6	.0005	.0005
CR7	.001	.003
CR8	.001	.003
CR9	.001	.001
CR10	.001	.001
CR11	.001	.001
CR12	.001	.001
CR13	.001	.001
CR14	.001	.001
C1	.020	.020
C2	.002	.002
C3	.005	.005
C4	.002	.002
C5	.010	.010
C6	.010	.010
C7	.010	.010
C8	.010	.010
T1	.045	.045
T2	.150	.470
L1	Not	Determined
L2	.02	.030
L3	.02	.020
L4	.02	.020
L5	.02	.020
Printed Circuit Board	.030	.030
Heat Sink	-	.100
Bracket	.150	.200
Hardware	.150	.160
Wire	.040	.050
Solder	.010	.010
Conformal Coating	.020	.020
Internal Connector	.020	.020
TOTAL WEIGHT (less L1)	.805	1.341

FOLDOUT FRAME 2

All the part weights are known except for the input inductor, L1, and the parts associated with the synchronous operation and the commanded ON/OFF capability.

The value, size and weight of the L1 inductor has not been completely defined, and its size depends on the results of tests yet to be run. The tests will be aimed at establishing the inductor value required to limit the turn-on transient to 125% of the average dc current. The inductor value will also be affected by increase in input current, and may become unmanageable for higher power loads.

If it is found that the inductor required to handle the dc current or to limit the turn-on transient is too large for any of the DC to DC converter loads, an alternate method for filtering or switching those particular loads may be necessary.

Since the turn-on transient is largely attributed to the current required to initially charge the filter capacitor, a method to prevent this condition and therefore reduce the size of the input inductor may be to place a switch between the input filter and the DC to DC converter. This approach will allow the filter capacitor to remain fully charged while the load is disconnected.

Due to a portion of the turn-on transient being attributed to the initial charge up of the output filter capacitors which are reflected back through the transformer, the switch approach will not eliminate all of the current overshoot.

However, the reflected capacitance is expected to be much smaller than the input capacitor, and would allow for a smaller size inductor to limit the overshoot when the switch is closed.

Therefore, all of the piece parts are included in this weights analysis shown in Table K-1 except the input inductor, L1, and parts associated with the commanded ON/OFF capability and the synchronous operation circuitry.

Thick Film Microcircuit

The piece part density of space power conditioning equipment has not kept pace with improvements in other subsystems. The non-uniform sizes and shapes of the mechanical devices and the electronic piece parts do not lend themselves to efficient packaging.

This stalemate is being broken by applying thin and thick film microcircuit techniques to power equipment. This has occurred only in the past few years, even though these techniques have been applied in other areas for 10 years. The slowness is due to the small degree of standardization and the high thermal density that occurs when high power piece parts are put into small volumes.

A task of the TOPS power conditioning equipment study was to develop a hybrid thick film microcircuit of the electronic parts of a dc to dc converter. This one basic, multipurpose circuit can be used to satisfy 35 separate requirements on the TOPS project with conditioned power levels from 1 to 25 watts. Three models have been identified for this range of power and all 3 can be built on the same conductor layout, with variations in the values of 7 piece parts only.

The inherent physical properties of the flat pack materials and construction enhances heat transfer, and balances the increased thermal density with higher conductivity and shorter thermal paths. Figure K-3 is a scale layout of the parts within the flat pack with piece part designation, and Figure K-4 is a photographic reproduction of the actual circuit.

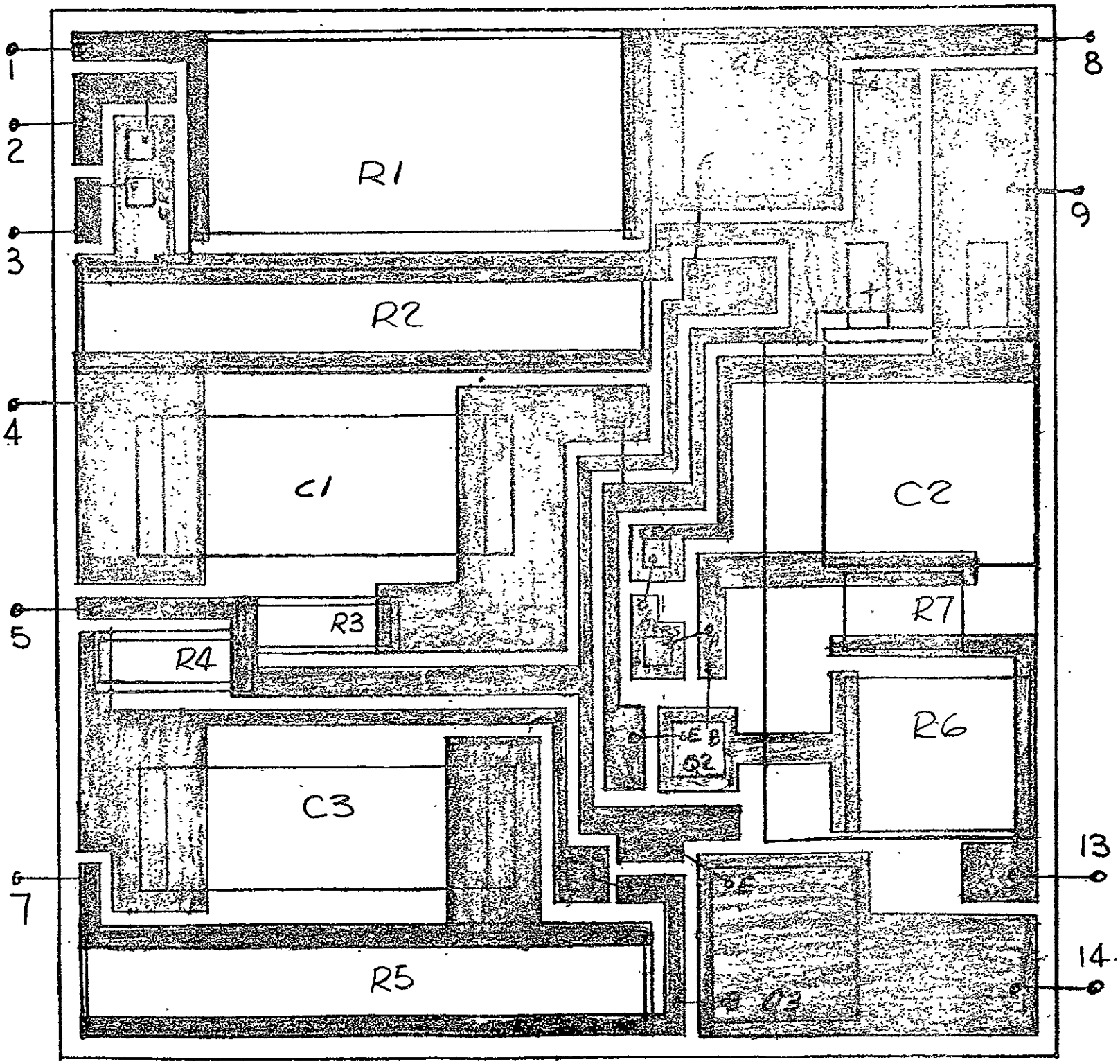


FIGURE K- 3 THICK FILM MICROCIRCUIT PHYSICAL LAYOUT

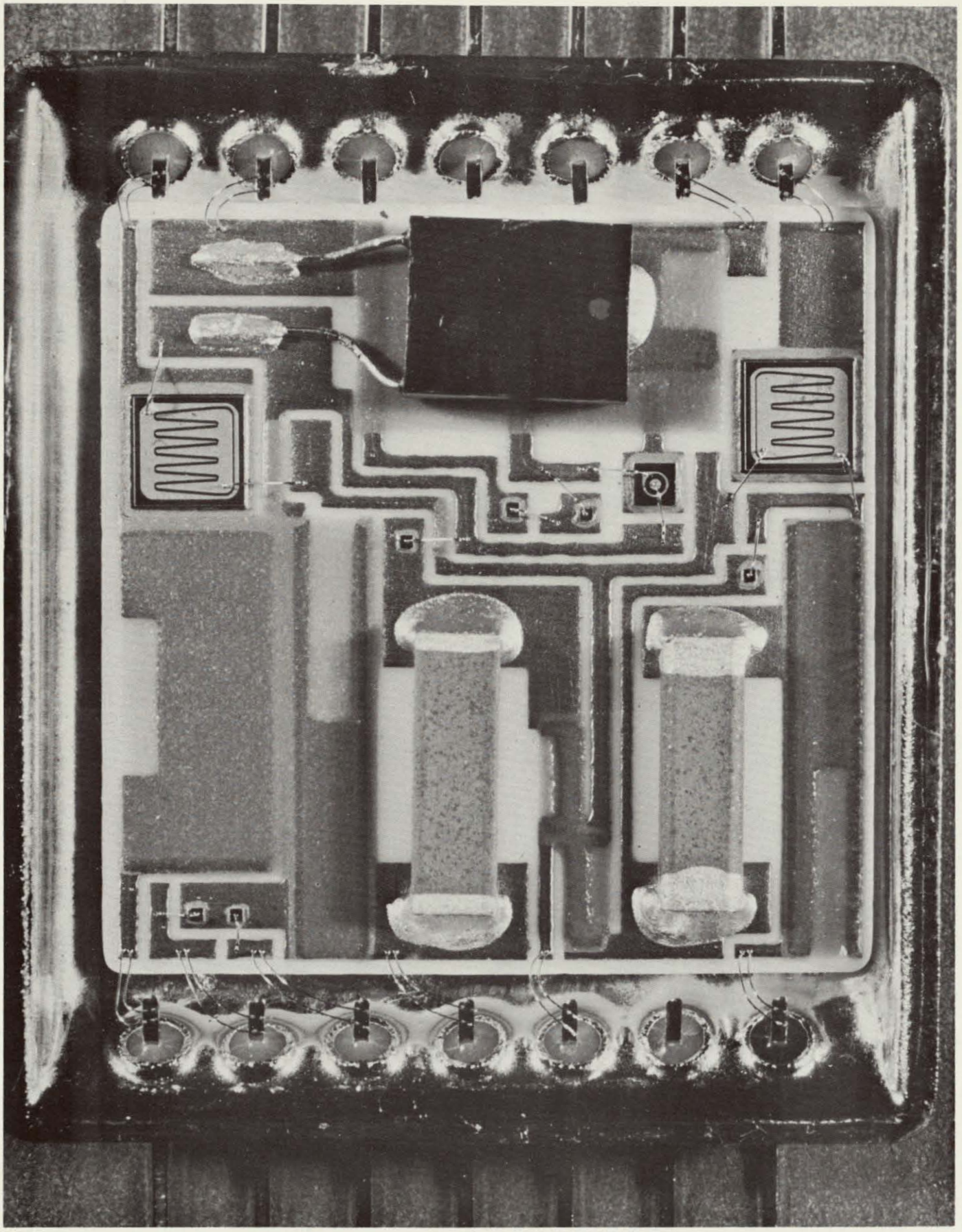


FIGURE K-4 THICK FILM MICROCIRCUIT

Thermal Considerations

The alumina oxide substrate, which is the means by which the circuit conductor and electronic piece parts are held within the flat pack, has a very high thermal conductivity and is an excellent electrical insulator. This property provides a more direct and efficient path of heat flow from the internally mounted switching power chips and the other internally mounted dissipative elements to the bottom of the metal flat pack. The flat pack in turn is then mounted or bonded to a metal heat sink with either a highly heat conductive paste, or a low temperature solder. This small number of highly efficient thermal interfaces provides excellent heat transfer. This can be compared to a semi-conductor chip that is mounted in an ordinary transistor case and insulated from the metal heatsink for electrical integrity. It uses a mechanical screw or nut for mounting, producing a higher thermal resistance to the ultimate heat sink. The flat pack itself is rated at 25 watts per square inch of mounting surface. This assumes that it is bonded to a heat sink which will adequately remove this much power.

Under normal discrete part construction of a dc to dc converter, the electrical (non-magnetic) piece parts are mounted on a printed circuit board or in a cordwood module. Either of these concepts would need additional means of heat transfer to maintain the piece parts at allowable temperatures. Further, the spacing of the discrete piece part under construction creates longer interconnections, higher power dissipation in the additional wire and increased opportunity for noise coupling into adjacent circuitry.

SUMMARY

A comparison of the flat pack to the discrete piece part circuit indicates a weight reduction of 80%, as shown in Table 2; a volume reduction of 80%; and reduces the number of interconnections with the remaining converter piece parts from 44 to 13.

TABLE K-2

WEIGHT COMPARISON OF DISCRETE PARTS VERSUS FLATPACK

WEIGHT OF DISCRETE PARTS (POUNDS)		WEIGHT OF FLATPACK (POUNDS)
R1	.003	.0125
R2	.001	
R3	.001	
R4	.001	
R5	.001	
R6	.001	
R7	.001	
CR1	.0005	
CR2	.0005	
CR3	.0005	
CR4	.0005	
CR5	.0005	
CR6	.0005	
C2	.002	
C3	.005	
C4	.002	
Q1	.007	
Q2	.007	
Q3	.007	
Printed Circuit Board	.020	
	.062	.0125

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