The Shichman-Hodges Enhancement MOSFET Model and SwitcherCAD III SPICE

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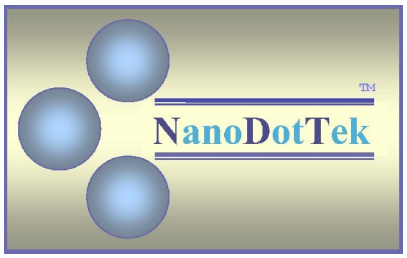

1. Introduction

Many students of electronics have learned this subject from Sedra and Smith [1]. Linear Technology Corporation has made available a freeware version of SPICE known as SwitcherCAD III (a. k. a. LTSpice™). The Shichman-Hodges [2] model for enhancement-type MOSFETs is the simplest possible model for such devices and is the Level 1 model in typical SPICE implementations for such devices. Yet the reference manual for SwitcherCAD III [3] does not explicitly state the relationship between the device model parameters as employed in the device model files and the actual Shichman-Hodges device model equations. The relationship is really spelled out in the OrCAD PSpice reference manual [4] (see p. 199 especially).

Therefore, as a convenience to those familiar with the theory of MOSFET operation according to [1] (especially Chapter 5) and those who also wish to do MOSFET circuit simulations using SwitcherCAD III this report directly spells out the relationship between the device model parameters for enhancement-type MOSFETs in SwitcherCAD III, and the device model equations in [1]. Attention here is restricted to the consideration of device DC behavior of the Level 1 (Shichman-Hodges) model. Thus, such things as device random noise (thermal and flicker), sub-threshold behavior, and high frequency effects are not considered here. However, the "basic" DC model does account for channel-length modulation effects and for the body effect. The latter can be particularly important in the design and simulation of integrated MOSFET circuits. Examples are provided of "customized" Level 1 devices using SwitcherCAD III including circuits illustrating their use.

In effect, this report is a tutorial on Level 1 MOSFET model usage in SwitcherCAD III.

2. Circuit Symbols

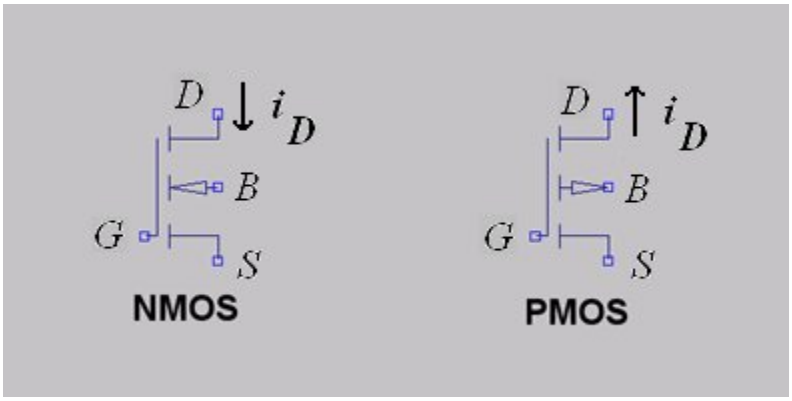

Figure 1: Schematic symbols for enhancement-type MOSFETs.

Figure 1 above shows the circuit schematic symbols for both the n-channel enhancement MOSFET (NMOS), and the p-channel enhancement MOSFET (PMOS). The symbols shown are similar to those in Figs. 5.9(a), and 5.16(a), respectively, of Sedra and Smith

[1]. And in fact these are the symbols used by Switcher CAD III (component library elements known as nmos4 and pmos4).

The symbols here reflect the fact that the body (substrate) terminal (B) is not necessarily at the same potential as the source terminal (S). For integrated circuit (IC) devices the source-substrate potential difference v_{SB} ($=v_S - v_B$) will not be zero in general. Thus, due to the *body effect,* the device threshold voltage V_t will be shifted away from the "nominal" value V_{t_0} (= zero-bias threshold voltage). In addition to accounting for the body effect the Shichman-Hodges model also accounts for *channel- length modulation* effects. This is the "slow" increase in the magnitude of the drain current due to an increase in the drain-source potential difference.

The notation respecting potentials and potential differences is the commonplace one where, for instance, node *X* is at potential v_X relative to some reference node (ground). Thus, the potential difference between nodes *X* and *Y* is $v_{XY} = v_X - v_Y$.

3. Shichman-Hodges Model Equations

Here the MOSFET model equations are taken directly from Chapter 5 of Sedra and Smith [1]. The reader is especially referred to Table 5.1, and also to Equation (5.25) in [1].

The threshold voltage for enhancement-type NMOS devices is positive. The body effect will usually increase the threshold voltage according to

$$V_t = V_{t_0} + \gamma[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}] \tag{3.1}$$

Here $V_{SB} \geq 0$ with parameters $\gamma, \phi_f, V_{t_0} > 0$. Similarly, for enhancement-type PMOS devices the threshold voltage is negative and the body effect will decrease this value (i.e., make it more negative) according to

$$V_t = V_{t_0} - \gamma[\sqrt{2\phi_f - V_{SB}} - \sqrt{2\phi_f}] \tag{3.2}$$

Here $V_{SB} \leq 0$ again with parameters $\gamma, \phi_f > 0$, but now $V_{t_0} < 0$. Equations (3.1) and (3.2) are really just (5.25) in Sedra and Smith [1].

Note that for integrated circuit (IC) MOSFET systems the substrate of NMOS devices is normally attached to the most negative power supply. For PMOS devices the substrate is normally attached to the most positive power supply. The purpose of this is to maintain a reverse-bias on the substrate-to-channel junction. In a situation such as this the potential difference V_{SB} will not necessarily be zero and so the body effect shouldn't be ignored.

It turns out that we have the following correspondences between the device model parameters in (3.1) and (3.2) and the parameters in the SPICE device model files of SwitcherCAD III:

$$Vto\ (zero-bias\ threshold\ voltage) = V_{t_0} \quad (V)$$

$$Gamma\ (bulk\ threshold\ potential) = \gamma \quad (V^{1/2})$$

$$Phi\ (surface\ potential) = 2\phi_f \quad (V)$$

Vto will be positive for NMOS devices, and negative for PMOS devices, whereas Gamma and Phi are always positive.

The threshold voltages of (3.1) and (3.2) are inputs to the following equations relating the drain current i_D to the gate-source potential difference v_{GS}, and the drain-source potential difference v_{DS}. From Table 5.1 in Sedra and Smith we find that for NMOS

$$i_D = \begin{cases} 0 & , v_{GS} \le V_t \ (cutoff) \\ K[2(v_{GS} - V_t)v_{DS} - v_{DS}^2] & , v_{GS} > V_t \ and \ v_{DS} \le v_{GS} - V_t \ (triode) \\ K(v_{GS} - V_t)^2(1 + \lambda v_{DS}) & , v_{GS} > V_t \ and \ v_{DS} \ge v_{GS} - V_t \ (saturation) \end{cases} \quad (3.3)$$

Note that $\lambda > 0$ here, and $v_{DS} \ge 0$. Similarly, for PMOS we have

$$i_D = \begin{cases} 0 & , v_{GS} \ge V_t \ (cutoff) \\ K[2(v_{GS} - V_t)v_{DS} - v_{DS}^2] & , v_{GS} < V_t \ and \ v_{DS} \ge v_{GS} - V_t \ (triode) \\ K(v_{GS} - V_t)^2(1 + \lambda v_{DS}) & , v_{GS} < V_t \ and \ v_{DS} \le v_{GS} - V_t \ (saturation) \end{cases} \quad (3.4)$$

Note that $\lambda < 0$ here, and $v_{DS} \le 0$. The senses of these currents are explicitly shown in Fig. 1 above. Note that for NMOS the normal current flow is *into* the drain while for PMOS the normal flow of current is *out of* the drain.

Equations (3.3) and (3.4) introduce two additional device modeling constants. First of all we have

$$K = \begin{cases} \frac{1}{2}\mu_n C_{ox}\frac{W}{L} & (NMOS) \\ \frac{1}{2}\mu_p C_{ox}\frac{W}{L} & (PMOS) \end{cases} \qquad (units\ of\ A/V^2) \quad (3.5)$$

where C_{ox} is the *oxide capacitance*, while μ_n is the *electron mobility*, and μ_p is the *hole mobility*. As well, *W* is the device *channel width* and *L* is the channel length with the ratio *W/L* defining the device *aspect ratio.* Parameter λ is the *channel-length*

modulation parameter (units of V^{-1}). Again, this models the "slow" increase in the size of the drain current as the drain-source potential difference increases in size. We have the following correspondences between the modeling constants of (3.3) and (3.4) and the parameters in the SwitcherCAD III MOSFET device model files:

$$Kp\ (transconduc\tan ce\ \ parameter) = \begin{cases} \mu_n C_{ox} & (NMOS) \\ \mu_p C_{ox} & (PMOS) \end{cases}$$

$$Lambda\ (channel-length\ \mathrm{mod}ulation\ \ parameter) = \begin{cases} \lambda & (NMOS) \\ -\lambda & (PMOS) \end{cases}$$

We now move on to the consideration of some examples illustrating the use of "customized" Shichman-Hodges MOSFET models in SwitcherCAD III as related to the device model equations of Sedra and Smith [1].

4. Example: PMOS Characteristic Curve

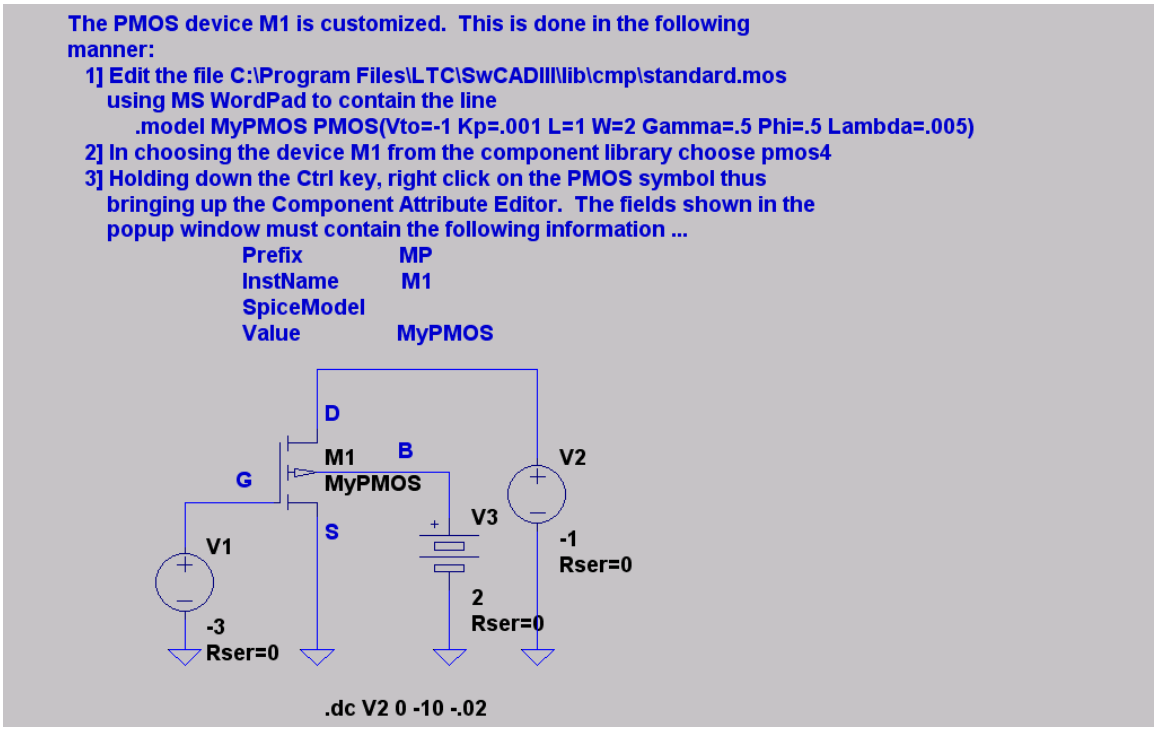

Figure 2: Example of a "customized" Level 1 PMOS device and a circuit for plotting the device $i_D - vs - v_{DS}$ characteristic curve.

Figure 2 shows a typical example of a "customized" enhancement-type p-channel MOSFET (PMOS). The comment in the figure explains how to create the desired Level 1 model. Note that the device parameters are specified in the comment. In fact,

$$K = \frac{1}{2} \cdot 0.001 \cdot \frac{2}{1} = 1 \frac{mA}{V^2}, \; V_{t_0} = -1\,V$$
$$\gamma = 0.5\,V^{1/2}, \; 2\phi_f = 0.5\,V, \; \lambda = -0.005\,V^{-1} \tag{4.1}$$

Also from Fig. 2 we observe that

$$v_{GS} = -3\,V, \; V_{SB} = -2\,V \tag{4.2}$$

Therefore, from (3.2) we find that the PMOS device has a threshold voltage of

$$V_t = -1 - 0.5[\sqrt{0.5+2} - \sqrt{0.5}] = -1 - (0.5)(0.874) = -1.437\,V \tag{4.3}$$

The transition from triode mode operation to saturation occurs (according to (3.4)) for

$$v_{DS} = v_{GS} - V_t = -3 - (-1.437) = -1.563\,V \tag{4.4}$$

For this case the drain current is (via the last equation in (3.4))

$$i_D = 0.001 \cdot (-3 - (-1.437))^2 (1 - (0.005) \cdot (-1.563)) = 2.46\,mA \tag{4.5}$$

We observe that (4.4) and (4.5) agree with the plot of $i_D - versus - v_{DS}$ in Fig. 3 (below).

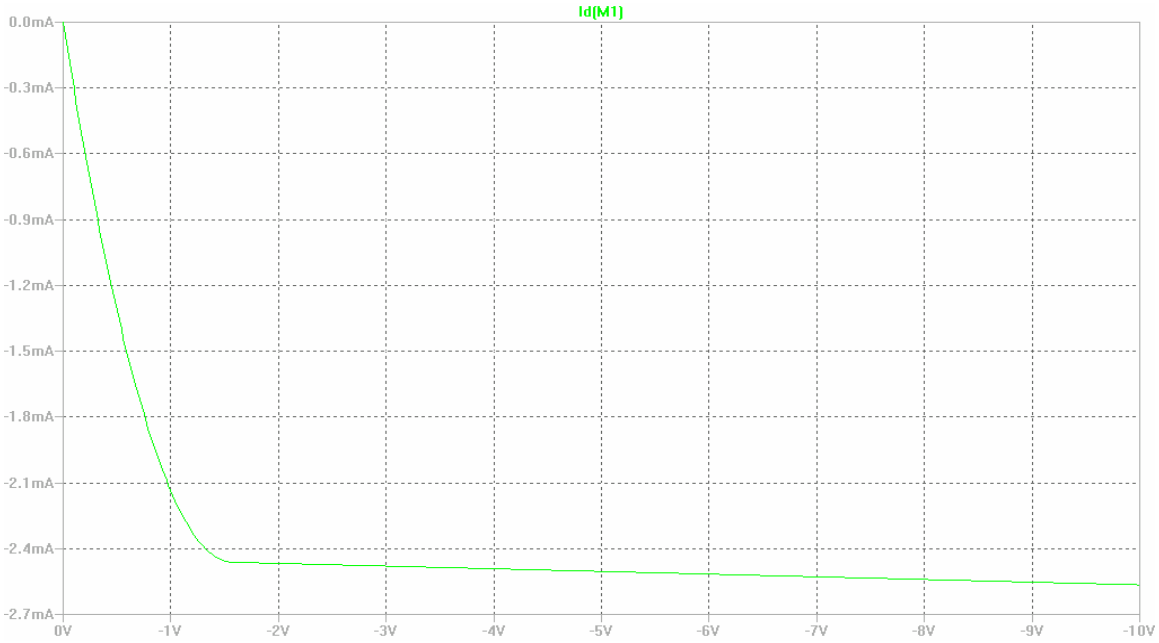

Figure 3: Plot of $i_D - vs - v_{DS}$ for the PMOS transistor in Fig. 2.

The drain current i_D in Fig. 3 is negative because SwitcherCAD III plots the current flowing *into* the drain terminal. This is opposite to the convention in Fig. 1 for PMOS.

5. Example: NMOS Characteristic Curve

The example here is very similar to that in Section 4.

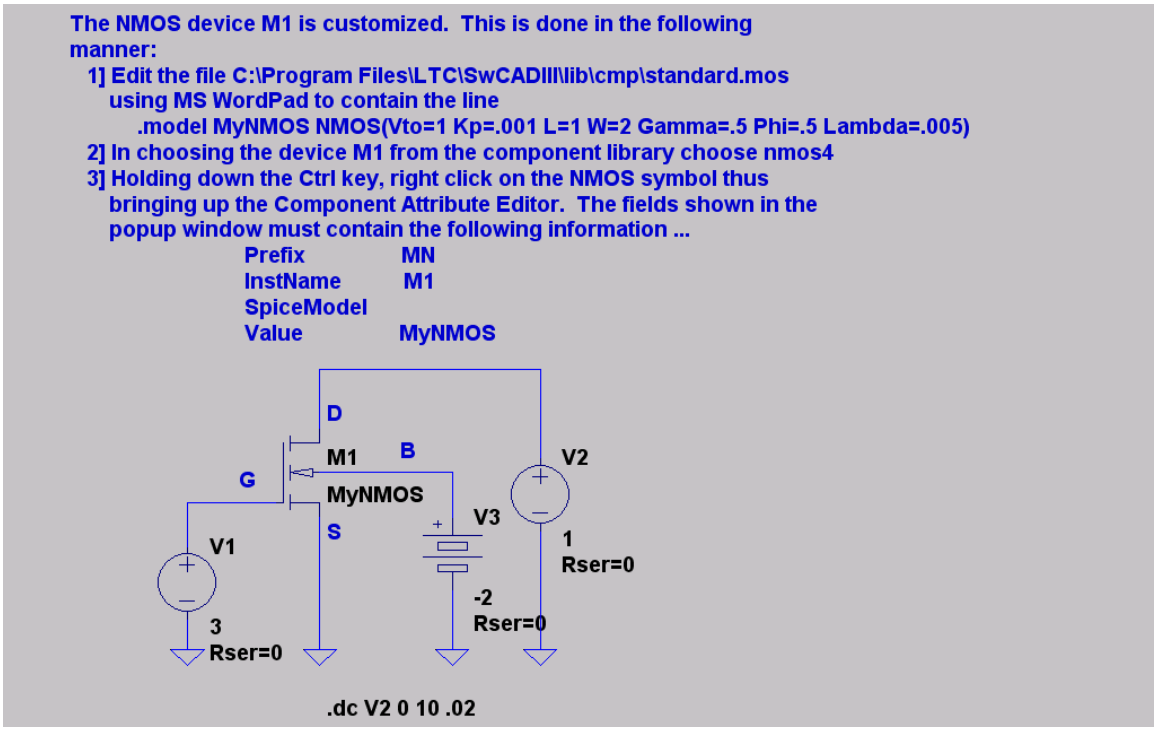

Figure 4: Example of a "customized" Level 1 NMOS device and a circuit for plotting the device $i_D - vs - v_{DS}$ characteristic curve.

Figure 4 shows a typical example of a "customized" enhancement-type n-channel MOSFET (NMOS). As for the device in Fig. 2 of Section 4 the comment in the figure here explains how to create the desired Level 1 model. Note that the device parameters are specified in the comment. In fact,

$$K = \frac{1}{2}\cdot 0.001 \cdot \frac{2}{1} = 1\,\frac{mA}{V^2},\ V_{t0} = 1\,V$$
$$\gamma = 0.5\,V^{1/2},\ 2\phi_f = 0.5\,V,\ \lambda = 0.005\,V^{-1} \qquad (5.1)$$

Also from Fig. 4 we observe that

$$v_{GS} = 3\,V,\ V_{SB} = 2\,V \qquad (5.2)$$

Therefore, from (3.1) we find that the NMOS device has a threshold voltage of

$$V_t = 1 + 0.5[\sqrt{0.5+2} - \sqrt{0.5}] = 1 + (0.5)(0.874) = 1.437\,V \tag{5.3}$$

The transition from triode mode operation to saturation occurs (according to (3.3)) for

$$v_{DS} = v_{GS} - V_t = 3 - (1.437) = 1.563\,V \tag{5.4}$$

For this case the drain current is (via the last equation in (3.3))

$$i_D = 0.001 \cdot (3 - (1.437))^2 (1 + (0.005) \cdot (1.563)) = 2.46\ mA \tag{5.5}$$

We observe that (5.4) and (5.5) agree with the plot of $i_D - versus - v_{DS}$ in Fig. 5 (below).

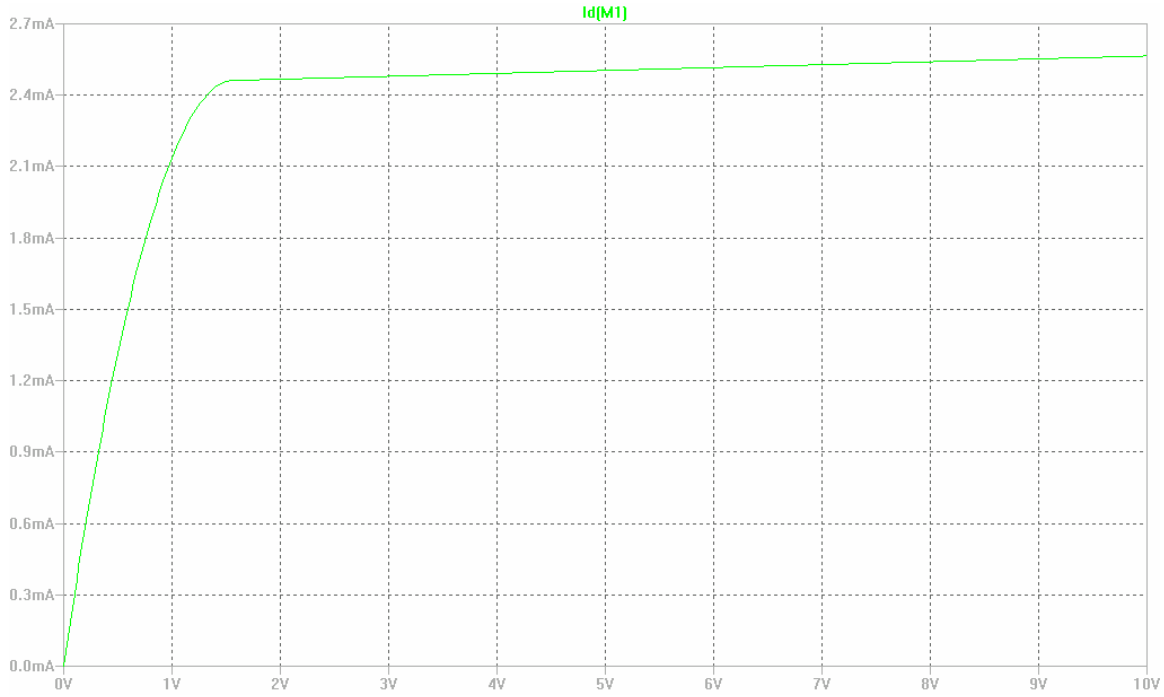

Figure 5: Plot of $i_D - vs - v_{DS}$ for the NMOS transistor in Fig. 4.

The MOSFETs specified in Figs. 2 and 4 will be used in subsequent examples.

6. Example: CMOS Transmission Gate

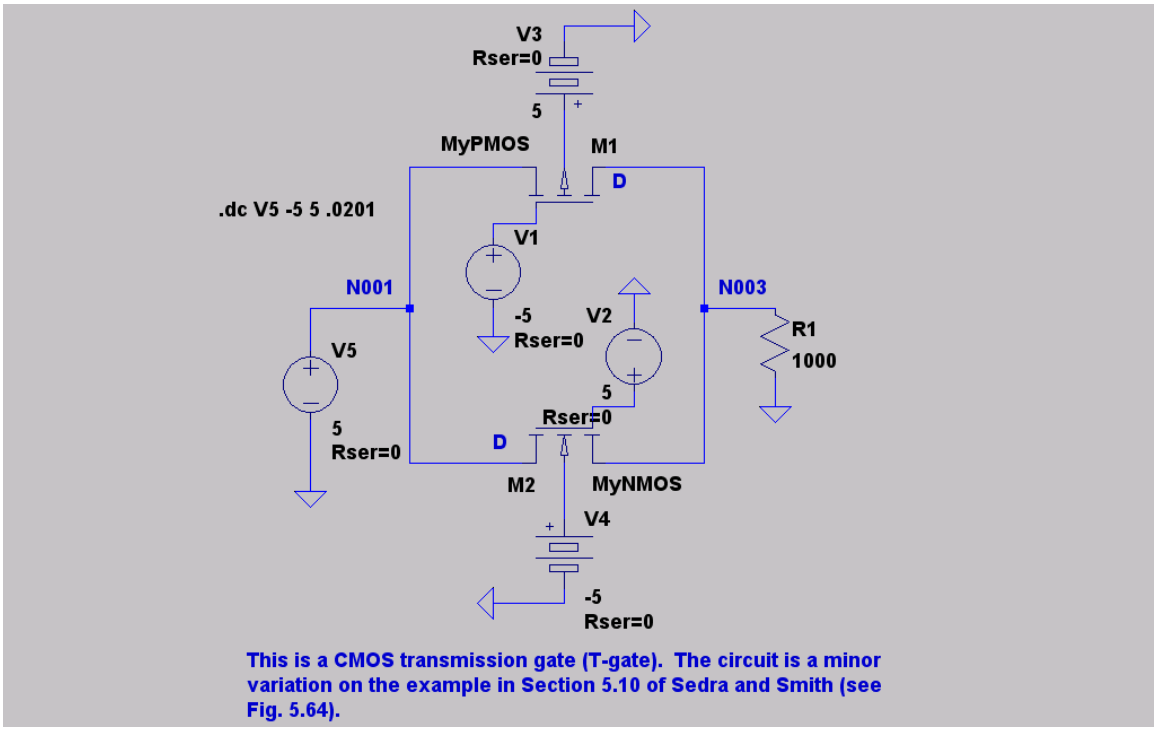

Figure 6: A CMOS transmission gate (T-gate) employing the MOSFETs described in Sections 4 and 5.

Figure 6 above illustrates a CMOS transmission gate (T-gate) and is a variation on the example in Section 5.10 of [1]. The T-gate is an electronic switch and for the situation depicted in Fig. 6 the switch is turned on (since V2 = +5 V, V1 = -5 V)[1]. The T-gate DC on-resistance may be determined from

$$R_{ON}(V5) = \frac{V(N001) - V(N003)}{I(R1)} \tag{6.1}$$

The notation emphasizes that this resistance will vary with the input voltage to the switch which is determined by the source V5. Figure 7 (below) presents a plot of (6.1) for which the body effect and channel-length modulation effects are both ignored; that is,

Gamma = 0, and Lambda = 0 for both M1 and M2 (6.2)

Of course, this is a rather idealized situation. The channel-length modulation and body effect are accounted for in the plot of Fig. 8 and so the device models in Figs. 2 and 4 are used in this case; that is, (4.1) and (5.1).

[1] To turn the switch off we set V2 = -5 V, and V1 = +5 V.

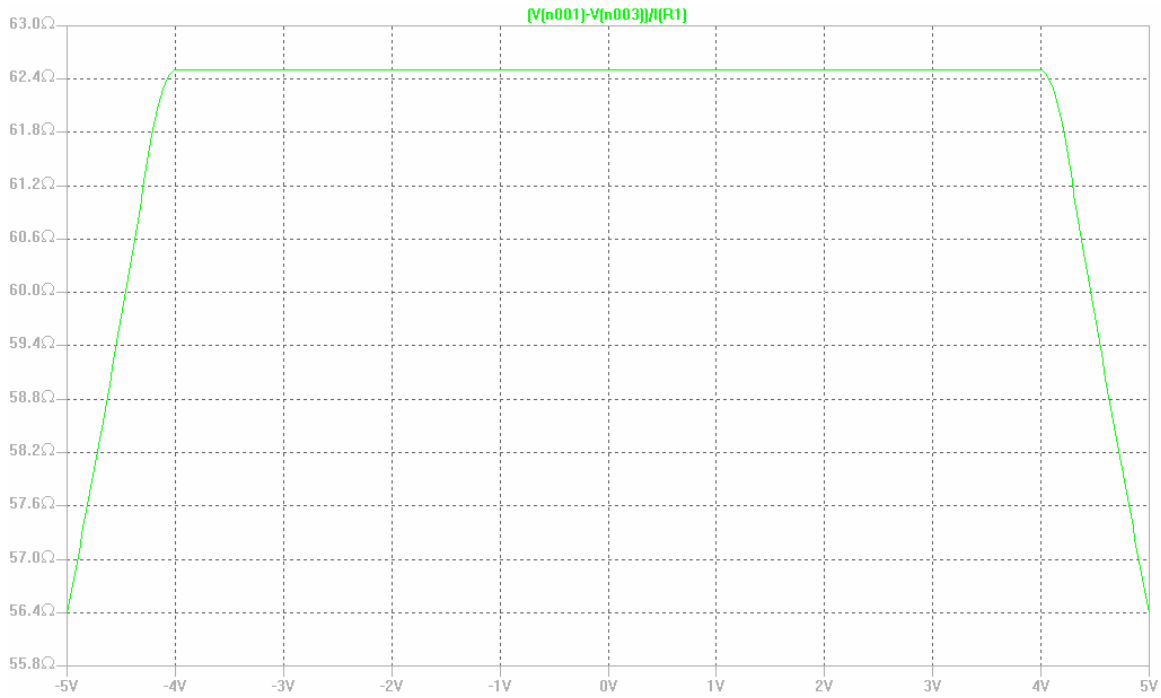

Figure 7: Plot of CMOS T-gate internal resistance (6.1) versus V5 neglecting both channel-length modulation and body effects.

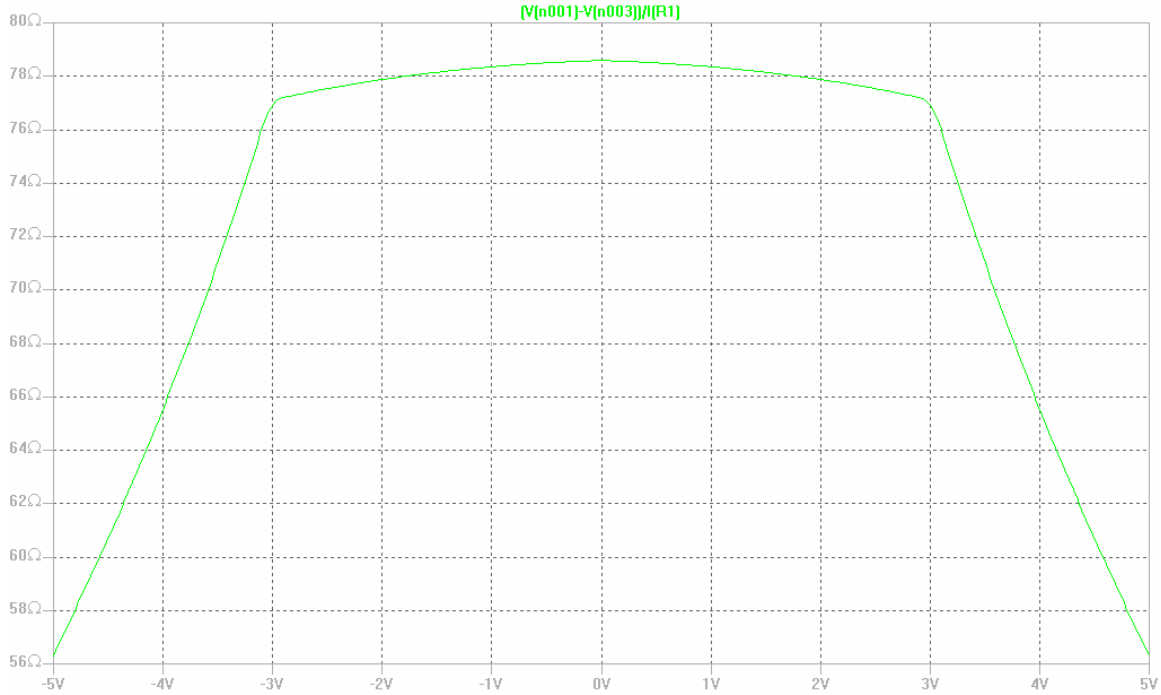

Figure 8: Plot of CMOS T-gate internal resistance (6.1) versus V5 now accounting for both channel-length modulation and body effects.

The T-gate is an electronic switch and by comparing Figs. 7 and 8 we observe that the body effect degrades switch performance by decreasing the range of V5 over which the on-resistance is relatively constant (plateau region), and also by increasing the size of the on-resistance. Also, channel-length modulation causes an increased deviation from flatness in the plateau region. (An ideal switch should have an on-resistance of zero and an off-resistance of infinity.)

A simplified calculation of the T-gate on-resistance based on the neglect of the channel-length modulation and body effects is as follows.

We need notation to distinguish between M1 and M2. M1 has threshold voltage $V_{t_1} = -V_t = -1\,V$ while M2 has threshold voltage $V_{t_2} = V_t = +1\,V$. From (3.5) M1 has parameter K given by $K_1 = 0.001\ A/V^2$, while for M2 $K_2 = 0.001\ A/V^2$. In addition to this we also have:

$$
\begin{aligned}
v_{G_k} &= \textit{gate potential of Mk} \\
v_{D_k} &= \textit{drain potential of Mk} \\
v_{S_k} &= \textit{source potential of Mk} \\
v_{B_k} &= \textit{substrate potential of Mk}
\end{aligned}
$$

where $k \in \{1,2\}$. Finally, $v_C = V2, -v_C = V1$ (with $v_C \in \{+5\,V, -5\,V\}$), $v_L = V(N003)$ is the load voltage across load resistor $R_L = R1 = 1{,}000\,\Omega$, and $v_A = V5$ is T-gate input voltage. As a rule the input voltage and load voltage are constrained to satisfy

$$-5\,V \le v_A, v_L \le +5\,V \tag{6.3}$$

Thus, on account of (6.3) we find that

$$
\begin{aligned}
v_{SB_1} &= v_{S_1} - v_{B_1} = v_A - 5 \quad \Rightarrow \quad -10\,V \le v_{SB_1} \le 0\,V \\
v_{SB_2} &= v_{S_2} - v_{B_2} = v_L + 5 \quad \Rightarrow \quad 0\,V \le v_{SB_2} \le 10\,V
\end{aligned}
\tag{6.4}
$$

Therefore, the channel-substrate junctions of both M1 and M2 are always reverse-biased. In addition, we note that for the gate potentials causing the T-gate to be turned on we have

$$
\begin{aligned}
v_{GS_1} &= -v_C - v_A = -5 - v_A \\
v_{GS_2} &= v_C - v_A = 5 - v_A
\end{aligned}
\tag{6.5}
$$

From (6.5) we see that $v_{GS_1} < V_{t_1} = -1\,V$ for all $v_A > -5 - V_{t_1} = -4\,V$. The PMOS transistor therefore conducts for $-4\,V \le v_A \le +5\,V$ if we account for (6.3). Similarly

from (6.5) we also see that $v_{GS_2} > V_{t_2} = +1\,V$ for all $v_A < 5 - V_{t_2} = +4\,V$. The NMOS transistor therefore conducts for $-5\,V \le v_A \le +4\,V$ if we account for (6.3). This implies that *both* M1 and M2 conduct for $-4\,V \le v_A \le +4\,V$. This range corresponds to the plateau in the T-gate on-resistance that is seen in Fig. 7. The body effect reduces the width of the plateau as seen in Fig. 8. Now we may estimate the T-gate on-resistance (i.e., the height of the plateau in Fig. 7).

We may assume that the input voltage v_A is small enough in magnitude so that M1 and M2 are in the triode mode of operation and such that $v_{DS_k}^2$ is small enough to be neglected. Therefore,

$$\begin{aligned} i_{D_1} &\approx 2K_1(v_{SG_1} - |V_{t_1}|)v_{SD_1} \quad \Rightarrow \quad R_{ON_1} \approx \frac{1}{2K_1(5 + v_A - |V_{t_1}|)} \\ i_{D_2} &\approx 2K_2(v_{GS_2} - V_{t_2})v_{DS_2} \quad \Rightarrow \quad R_{ON_2} \approx \frac{1}{2K_2(5 - v_A - V_{t_2})} \end{aligned} \tag{6.6}$$

The total T-gate on-resistance must be

$$R_{ON} \approx R_{ON_1} \parallel R_{ON_2} = \frac{R_{ON_1} R_{ON_2}}{R_{ON_1} + R_{ON_2}} \tag{6.7}$$

For the device parameter values of (4.1) and (5.1) we find that

$$R_{ON_1} \approx \frac{500}{4 + v_A}, \quad \textit{and} \quad R_{ON_2} \approx \frac{500}{4 - v_A} \tag{6.8}$$

For $v_A = 0\,V$ we obtain $R_{ON} \approx 62.5\,\Omega$ in very close agreement with the result in Fig. 7. This value for the on-resistance does not change much as we vary v_A over the plateau voltage range. Again, the body effect increases the size of the on-resistance as may be seen in Fig. 8.

7. Example: CMOS Logic Inverter

Another classical example of the use of complementary MOSFET transistors is in CMOS digital logic circuits of which the simplest example is the CMOS logic inverter. The circuit is illustrated in Fig. 9 below. The circuit of Fig. 9 makes use of the MOSFETs parameterized in Sections 4 and 5 (i.e., (4.1) and (5.1)).

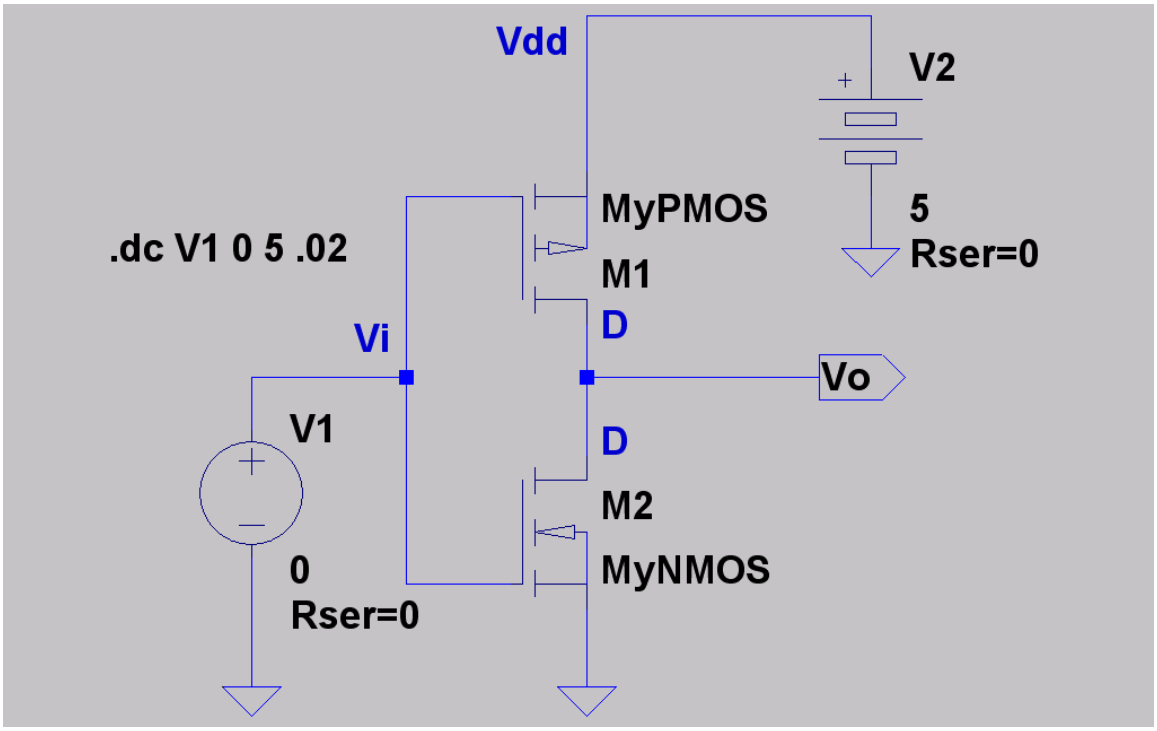

Figure 9: A CMOS logic inverter. The voltage transfer characteristic ($v_o - versus - v_i$) appears in Fig. 10.

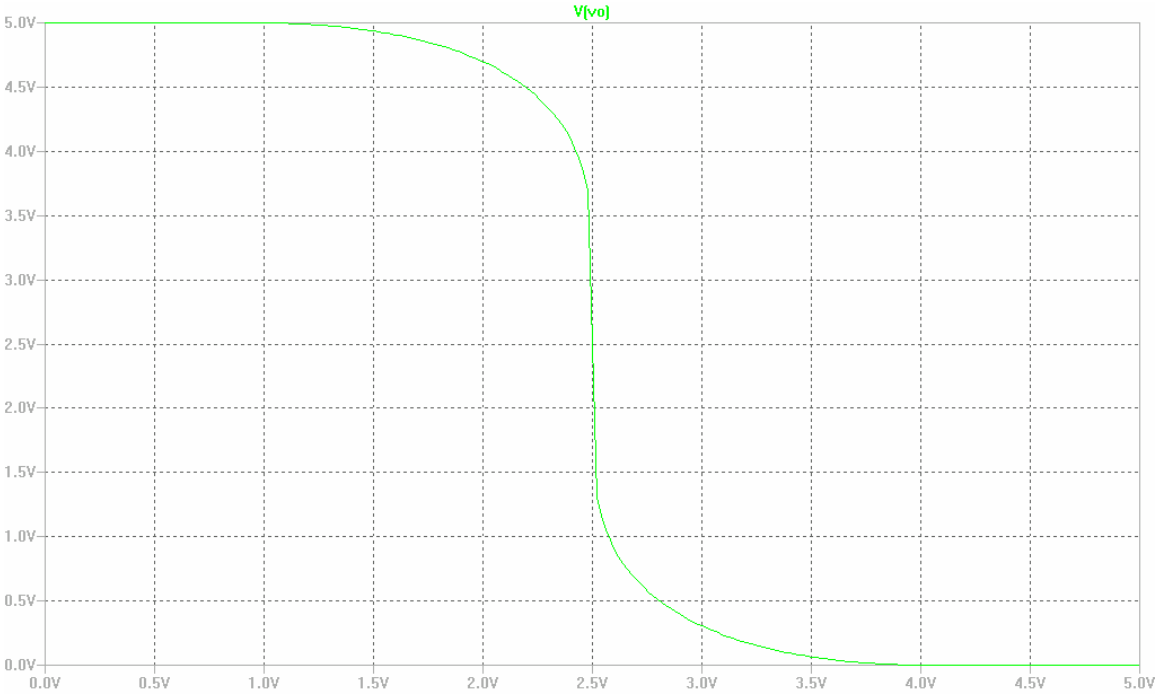

Figure 10: Plot of $v_o - versus - v_i$ for the CMOS inverter of Fig. 9.

We observe from Fig. 9 that for both of the MOSFETs M1 and M2 the source-substrate potential difference is zero and so there will be no body effect to contend with. In what follows we will neglect channel-length modulation effects. We shall obtain drain current expressions for the MOSFETs in the CMOS inverter[2].

Begin by recalling (3.4). For M1 remember that $V_{t_1} < 0$ (PMOS has a negative threshold voltage) and so we must have

$$i_{D_1} = 0 \quad if \quad v_{GS_1} = v_{G_1} - v_{S_1} = v_i - V_{dd} \geq V_{t_1}, \quad or \quad v_i \geq V_{dd} - |V_{t_1}| \tag{7.1}$$

This is the cutoff condition for M1. If on the other hand $v_i < V_{dd} - |V_{t_1}|$ then M1 will be either in the triode mode of operation or the saturation mode of operation. Triode operation occurs when $v_{DS_1} = v_{D_1} - v_{S_1} = v_o - V_{dd} \geq v_{GS_1} - V_{t_1} = v_i - V_{dd} + |V_{t_1}|$ which is the condition $v_o \geq v_i + |V_{t_1}|$. Thus, the drain current for M1 in this mode is given as

$$\begin{aligned} i_{D_1} &= K_1[2(v_i - V_{dd} - V_{t_1})(v_o - V_{dd}) - (v_o - V_{dd})^2] \\ &= K_1[2(V_{dd} + V_{t_1} - v_i)(V_{dd} - v_o) - (V_{dd} - v_o)^2] \\ &= K_1[2(V_{dd} - v_i - |V_{t_1}|)(V_{dd} - v_o) - (V_{dd} - v_o)^2] \end{aligned} \tag{7.2}$$

And thus for the saturation mode of operation we have $v_o \leq v_i + |V_{t_1}|$ with the device drain current being given as

$$i_{D_1} = K_1(V_{dd} - v_i - |V_{t_1}|)^2 \tag{7.3}$$

Now recall (3.3). For M2 $V_{t_2} > 0$ (NMOS has a positive threshold voltage) and so we must have

$$i_{D_2} = 0 \quad if \quad v_{GS_2} = v_{G_2} - v_{S_2} = v_i \leq V_{t_2} \tag{7.4}$$

This is the cutoff condition for M2. If on the other hand $v_i > V_{t_2}$ then M2 will be either in the triode mode of operation or the saturation mode of operation. The triode mode of operation occurs when $v_{DS_2} = v_{D_2} - v_{S_2} = v_o \leq v_{GS_2} - V_{t_2} = v_i - V_{t_2}$, that is, $v_o \leq v_i - V_{t_2}$. Thus, the drain current for M2 in this mode is given as

$$i_{D_2} = K_2[2(v_i - V_{t_2})v_o - v_o^2] \tag{7.5}$$

[2] The device drain current expressions also appear in Section 13.5 of Sedra and Smith [1].

Thus for the saturation mode of operation $v_o \geq v_i - V_{t_2}$ and the device drain current is now

$$i_{D_2} = K_2 (v_i - V_{t_2})^2 \tag{7.6}$$

The voltage transfer characteristic curve for the inverter as seen in Fig. 10 has five "segments" corresponding to the different operating modes of M1 and M2 which arise in the course of varying the input voltage v_i from 0 V to V_{dd} V. Using (7.1) - (7.6) it is possible to obtain formulae for the various segments of the curve in Fig. 10.

For example, the segment for which $v_o - versus - v_i$ is the most vertical occurs when both M1 and M2 are in the saturation mode of operation. Now, CMOS inverters are usually designed so that $K_2 = K_1 = K$, and also $V_{t_2} = -V_{t_1} = V_t$. If both MOSFETs are saturated then we must have $i_{D1} = i_{D_2}$ and hence via (7.3) and (7.6)

$$K(v_i - V_t)^2 = K(V_{dd} - v_i - V_t)^2 \tag{7.7}$$

This solves to yield $v_i = V_{dd}/2$. For both MOSFETs to be saturated requires that

$$v_i - V_{t_2} \leq v_o \leq v_i + |V_{t_1}| \quad \Rightarrow \quad \frac{1}{2}V_{dd} - V_t \leq v_o \leq \frac{1}{2}V_{dd} + V_t \tag{7.8}$$

Equation (7.8) gives the "length" of the vertical segment in the voltage transfer characteristic as it determines the endpoints of this segment. Here the segment is perfectly vertical as we have neglected channel-length modulation effects. However, channel-length modulation will in practice cause the segment to be steep yet not perfectly vertical. The curve in Fig. 10 actually shows this because the plot is based on the device model parameters in (4.1), and (5.1).

As another example we will work out the expression for v_o in terms of v_i for the curved portion of the characteristic curve in Fig. 10 for $v_i > V_{dd}/2 = +2.5\,V$. In fact, we must have $V_{dd}/2 \leq v_i \leq V_{dd} - V_t$. For the ranges of input and output voltages in this region of the characteristic curve we infer that M1 must be saturated, while M2 must be in the triode mode of operation. Again, $i_{D1} = i_{D_2}$ and so via (7.3) and (7.5) we have

$$K(V_{dd} - v_i - V_t)^2 = K[2(v_i - V_t)v_o - v_o^2]$$

or

$$(V_{dd} - v_i - V_t)^2 = 2(v_i - V_t)v_o - v_o^2 \qquad (7.9)$$

This is an implicit expression relating v_o to v_i. It is a quadratic in v_o, and so the formula for the solution of a quadratic equation may be employed. We may consider (7.9) for the parameter values of our example; i.e., $V_{dd} = +5\,V, V_t = +1\,V$. Thus, (7.9) solves as

$$v_o = (v_i - 1) \pm \sqrt{6v_i - 15} \quad for \quad 2.5\,V \le v_i \le 4\,V \qquad (7.10)$$

Which sign in (7.10) do we choose ? Since the output voltage decreases as the input voltage increases we must choose the minus sign.

8. Example: CMOS Pulse Width Tuner

Classically, the T-gate and the logic inverter are components in digital logic systems. However, these digital logic components are also useful in analog systems. For instance, the circuit in Fig. 11 (below) is of a CMOS pulse width tuner.

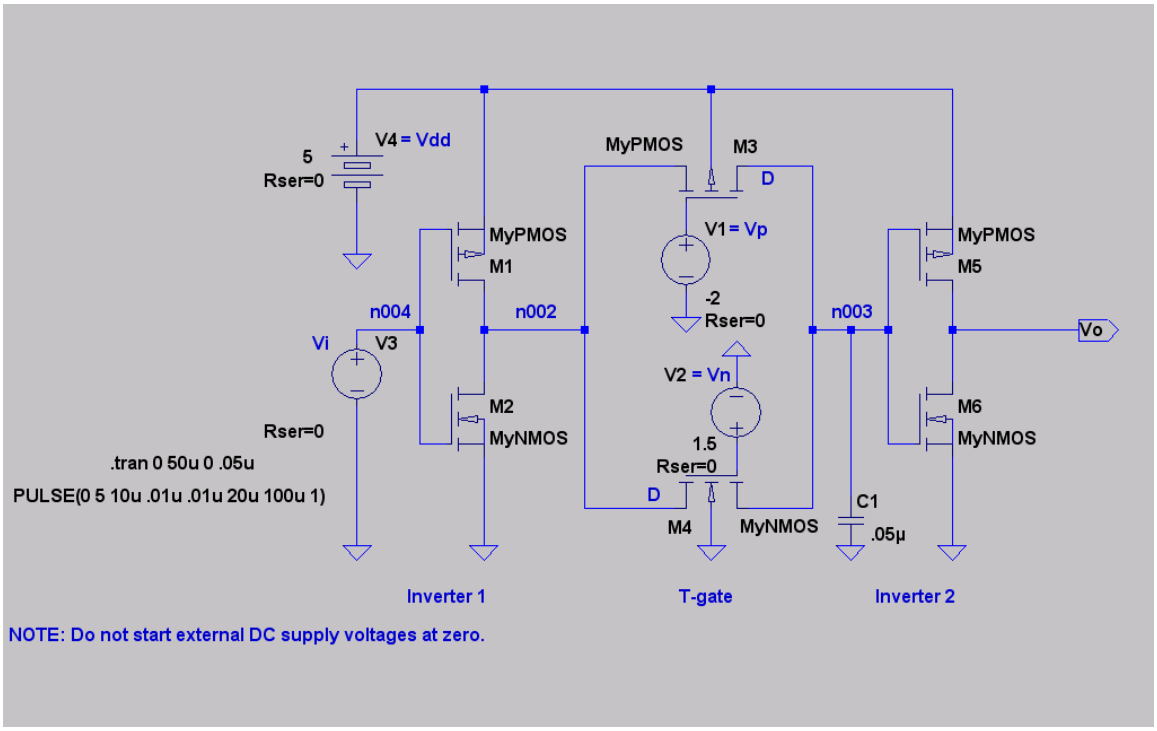

Figure 11: A CMOS pulse width tuner.

The input source V3 = V(n004) = v_i may be viewed as inputting a rectangular pulse to the circuit, and the pulse width tuner will adjust the pulse's width at the output v_o. The desired pulse width may be changed by changing the gate potentials for the MOSFETs denoted as M3 and M4 in the T-gate. This causes the T-gate's effective resistance to

change thus varying the RC time-constant involving the T-gate resistance and the capacitor C1 (includes the gate capacitance of Inverter 2).

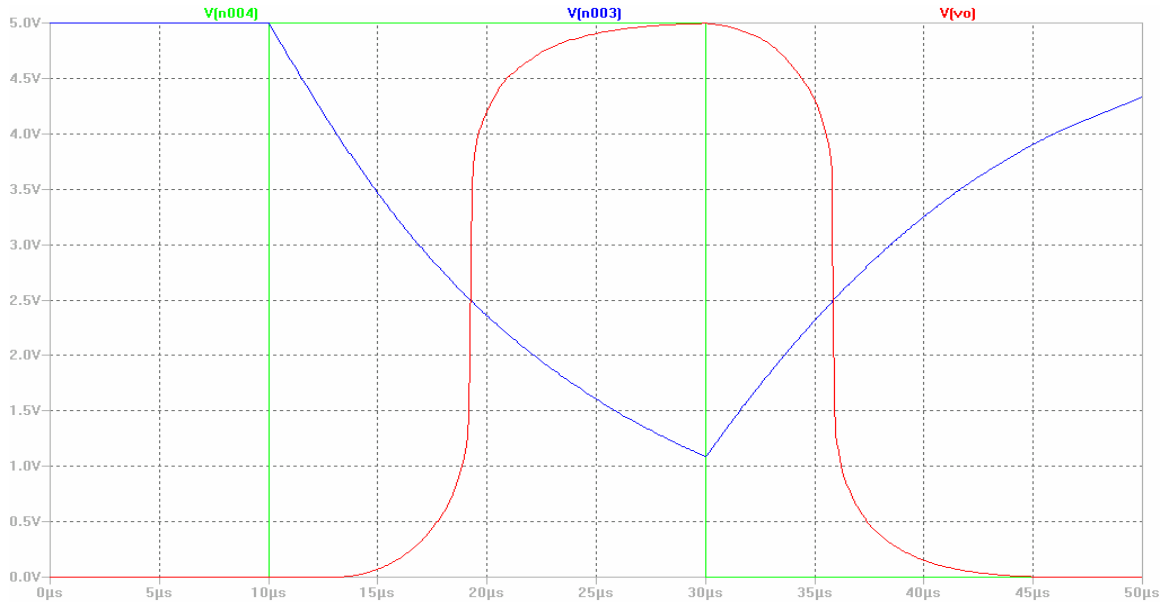

Figure 12: Plot of the rectangular input pulse V(n004), voltage drop across the capacitor plates V(n003), and the output pulse v_o for tuning voltage parameters $v_p = -4\,V, v_n = 3\,V$.

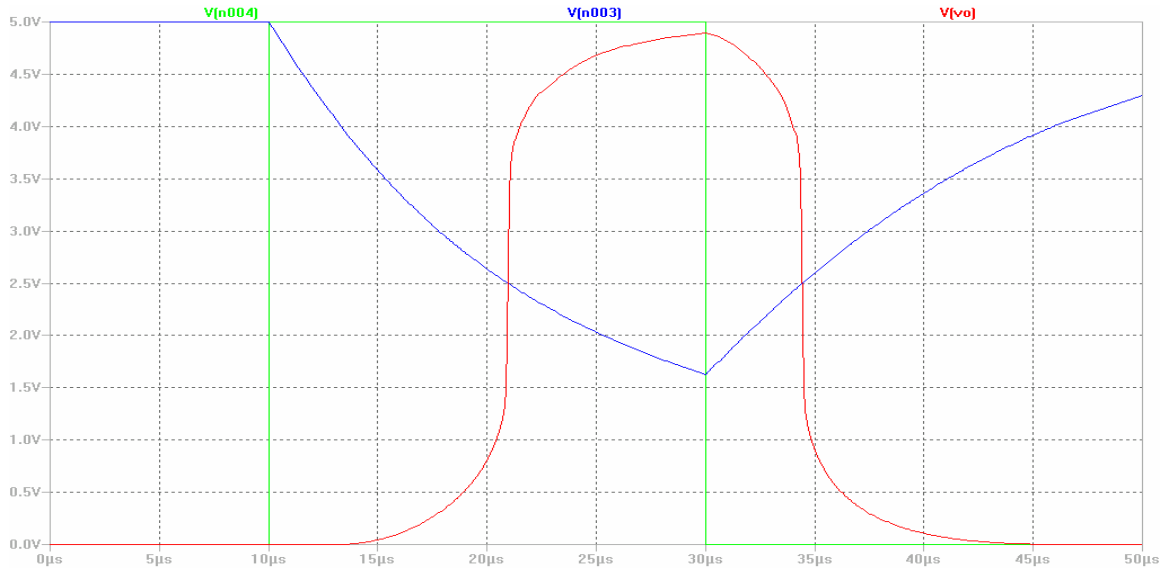

Figure 13: Plot of the rectangular input pulse V(n004), voltage drop across the capacitor plates V(n003), and the output pulse v_o for tuning voltage parameters $v_p = -2\,V, v_n = 1.5\,V$.

A typical example showing the effect of the circuit on an input pulse appears above in Fig. 12 where V1 = $v_p = -4\,V, V2 = v_n = +3\,V$. Figure 13 is another example where V1 = $v_p = -2\,V, V2 = v_n = +1.5\,V$. In both cases the pulse width is narrowed, but at the expense of a blurring of the edges.

There is growing interest in ultra wideband (UWB) wireless communications systems. In recent years CMOS-based designs for UWB system components have appeared. For example, there is Ang, Chen and Lv [5], and Marsden, Lee, Ha and Lee [6]. In fact, a version of the pulse width tuner circuit of Fig. 11 is a basic building block in the waveform generator proposed in [5] (see their Fig. 9).

Acknowledgment

SwitcherCAD III (a SPICE implementation by Linear Technology Corporation) running under MS Windows XP was used to do the SPICE simulations and for the production of illustrative figures. The latter was aided with the use of MS Paint. PDF Online™, a free online file type conversion service was used to convert the MS Word version of this report into pdf.

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