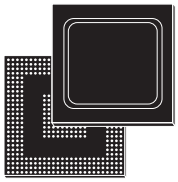
STLS2F01

Loongson 2F: High performance 64-bit superscalar MIPS® microprocessor

Data Brief

Features

- 64-bit superscalar architecture
- 900 MHz clock frequency
- Single/double precision floating-point units
- New streaming multimedia instruction set support (SIMD)
- 64 Kbyte instruction cache, 64 Kbyte data cache, on-chip 512 Kbyte unified L2 cache
- On chip DDR2-667 and PCI-X controller
- 4 W @ 900 MHz power consumption:
  - Best in class for power management
  - Voltage/frequency scaling
  - Stand-by mode support
  - L2 cache disable/enable option
- Leading edge 90 nm process technology
- 27x27 heat spreader flip-chip BGA package
- MIPS based instruction set (MIPS III compatible)



HFCBGA452 (27x27x2.9mm)

Description

The STLS2F01 is a MIPS based 64-bit superscalar microprocessor, able to issue four instructions per clock cycle among six functional units: two integer, two single/double-precision floating-point, one 64-bit SIMD and one load/store unit.

The micro architecture is organized with nine-stage of pipeline and support of dynamic branch prediction.

The memory hierarchy is composed by the first level of 64 Kbyte 4-way set associative caches for instructions and data, the second level of 512 Kbyte unified 4-way set associative cache and the memory management unit (MMU) with translation lookaside buffer (TLB).

The Loongson microprocessor family is the outcome of a successful collaboration started in 2004 between STMicroelectronics and the Institute of Computing Technology, part of the Chinese Academy of Science. Loongson microprocessors were co-developed by STMicroelectronics and the Institute of Computing Technology to address all the applications requiring high level of performance and low power dissipation.

Compared to the STLS2E02 processor, the STLS2F01 has an enhanced architecture providing higher performance, reduced power consumption, integrated DDR2 memory controller and PCI-X bus interface.

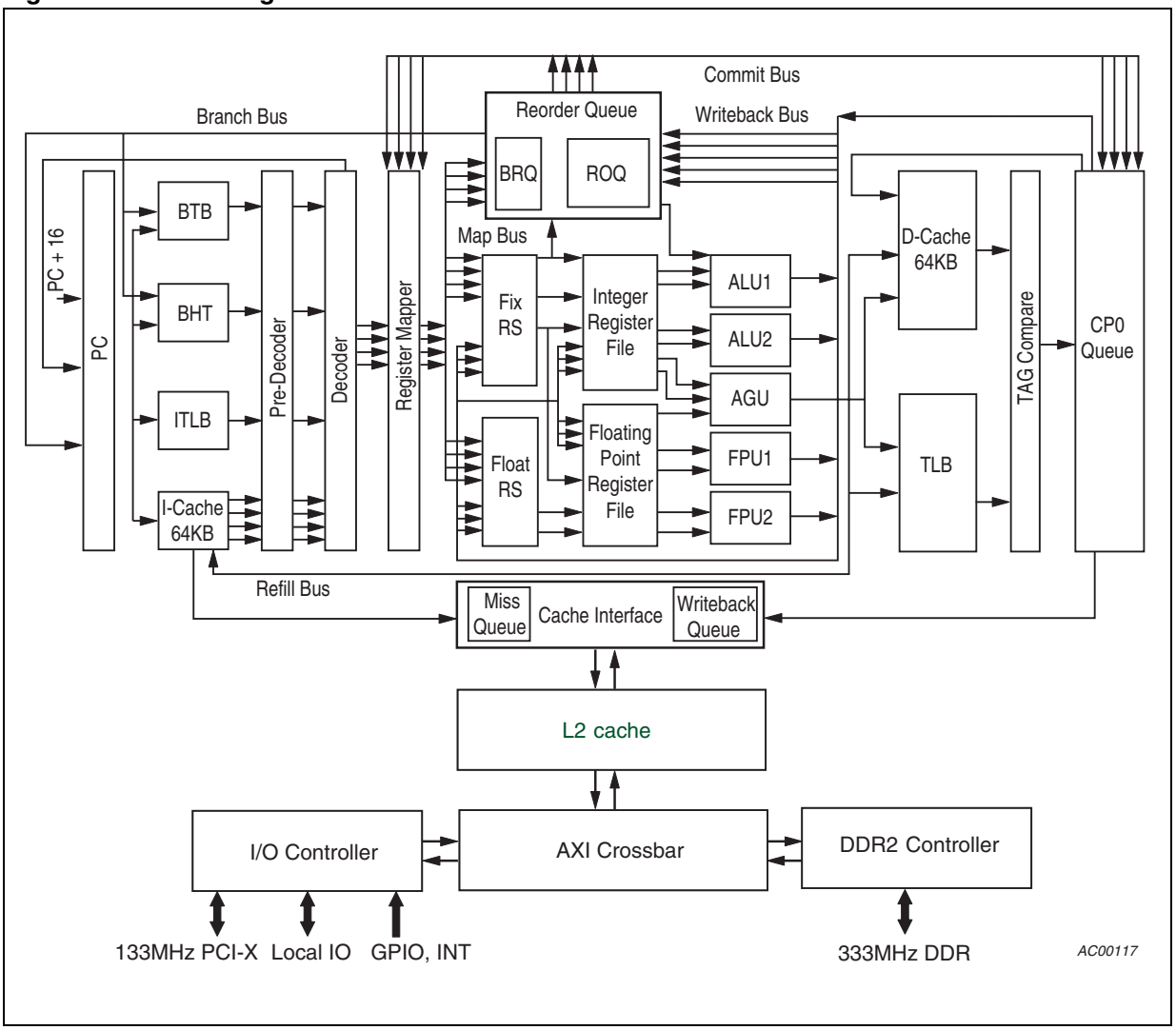
Table 1. Device summary

Part numbers	Package	Packing
STLS2F01	HFCBGA452 (27x27x2.9mm)	Tray

1 Architectural features and block diagram

- CPU
  - Out-of-order superscalar 64-bit architecture
  - MIPS based, compatible with MIPS III instruction set
  - Nine-stage pipeline organized in fetch, pre-decode, decode, reg-map, dispatch, issue, reg-read, execution and commit
  - Up to 64 instructions executed out-of-order with four issue mechanism
  - 64-bit register file (32 fix + 32 float)
  - Register renaming unit composed by 64-entry physical register files
  - Branch prediction unit
  - Six functional units: two integer, two float, one SIMD unit, one load/store unit
- Memory Hierarchy
  - 64 Kbyte + 64 Kbyte four-ways set-associative first level instruction and data cache
  - 512 Kbyte four-ways set associative unified second level cache
  - Up to 24 non-blocking accesses with on-the-fly memory disambiguation
  - Load speculation through value returned from previous pending stores
  - Miss word first access for cache miss access
  - Instruction 16-entry TLB (table lookside buffer) and unified 64-entry TLB with page size from 4 Kbyte to 4 Mbyte

Figure 1. Block diagram



2 Package information

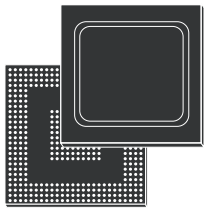
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

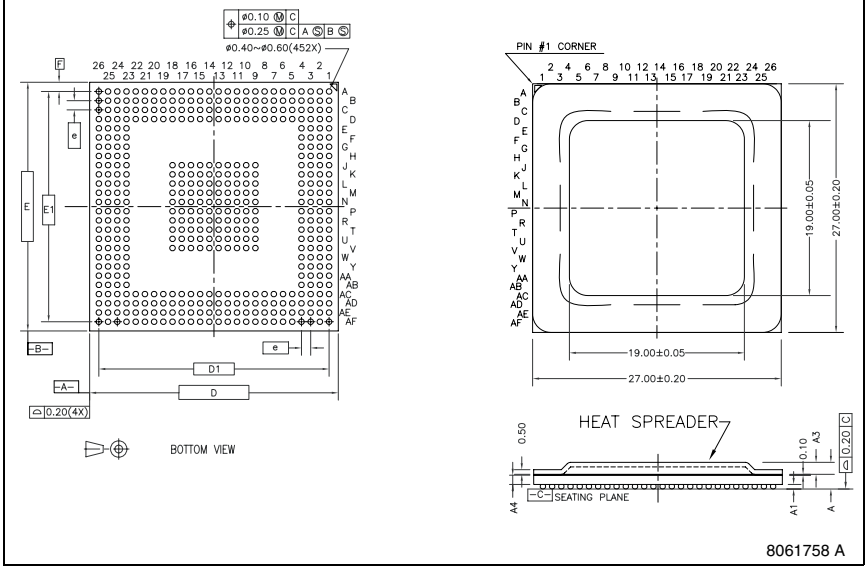
Figure 2. HFCBGA452 mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.150			0.1240
A1	0.250			0.0098		
A3		1.300			0.0512	
A4		1.000			0.0394	
b	0.450	0.500	0.550	0.0177	0.0197	0.0217
D	26.800	27.000	27.200	1.0551	1.0630	1.0709
D1		25.000			0.9843	
E	26.800	27.000	27.200	1.0551	1.0630	1.0709
E1		25.000			0.9843	
e		1.000			0.0394	
F		1.000			0.0394	
aaa			0.200			0.0079
ddd			0.200			0.0079
eee			0.250			0.0098
fff			0.100			0.0039

OUTLINE AND MECHANICAL DATA



HFCBGA452 (27x27x2.9mm)
Heat **S**preader **F**lip **C**hip **B**all **G**rid **A**rray



3 Revision history

Table 2. Document revision history

Date	Revision	Changes
31-May-2007	1	Initial release.
06-Jun-2008	2	Change in the *Features* sections: "clock frequency"

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