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DC Noise Immunity of CMOS Logic Gates

Fairchild Semiconductor
Application Note 377
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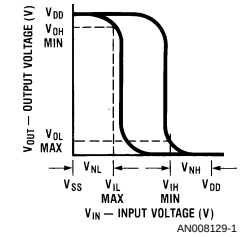
Introduction

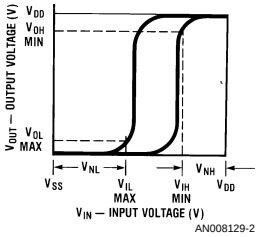
The immunity of a CMOS logic gate to noise signals is a function of many variables, such as individual chip differences, fan-in and fan-out, stray inductance and capacitance, supply voltage, location of the noise, shape of the noise signal, and temperature. Moreover, the immunity of a system of gates usually differs from that of any individual gate; thus a generalized analysis of the noise immunity of a logic circuit becomes a very complex process when one takes all the above parameters into consideration.

The complementary structure of the inverter results in a near-ideal input-output characteristic with switching point midway (45%–55%) between the "0" and "1" output logic levels. The result is a high noise immunity (defined as the maximum noise voltage which can appear on the input without switching an inverter from one state to another). Fairchild's CMOS circuits have a typical noise immunity of 0.45 V_{CC}. This means that a spurious input which is 45% of the power supply voltage typically will not propagate through the circuit. However, the standard guaranteed value through the industry is 30%.

This note describes the variation of the transfer region (or DC noise immunity) of a multiple-input gate in conjunction with the gate configuration—a consideration important in the system design.



(a)



(b)

FIGURE 1. Minimum and Maximum Transfer Characteristics for (a) Inverting Logic Function and (b) Noninverting Logic Function

Transfer Characteristics

Figure 1 illustrates minimum and maximum transfer characteristics useful for defining noise immunity for an inverter and a non-inverter. Some definitions are as follows:

$V_{IH\ min}$=the minimum input voltage high-level input for which the output logic level does not change state.

Then:

$V_{NL}=V_{ILmax}$="low level" noise immunity

$V_{NH}=V_{DD}-V_{IH}$="high level" noise immunity

V_{OHmin}=minimum high level output voltage for rated V_{NL} [for inverting function as in *Figure 1* (*a*)]

Table 1 shows the UB and B series noise immunity and noise margin ratings determined by the Joint Electron Devices Engineering Council (JEDEC). B series ratings are slightly higher than the UB series because of the buffered nature of these gates.

TABLE 1. UB and B Series DC Noise Immunity and Noise Margin (T_A=25°C)

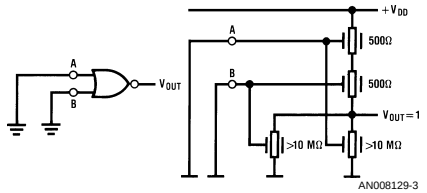
Characteristics		Test Conditions		Input Voltage (V)
		V_O (V)	V_{DD} (V)	
Input Low Voltage				
V_{IL} max				
	B types	0.5/4.5	5	1.5
		1/9	10	3
		1.5/13.5	15	4
	UB types	0.5/4.5	5	1
		1/9	10	2
		1.5/13.5	15	2.5
Input High Voltage				
V_{IH} min				
	B types	0.5/4.5	5	3.5
		1/9	10	7
		1.5/13.5	15	11
	UB types	0.5/4.5	5	4
		1/9	10	8
		1.5/13.5	15	12.5

Since the MOS transistors are voltage-controlled resistors, the transfer characteristics and consequently the DC noise immunity are determined by the parallel series combination of the transistor impedances in conjunction with the input voltages, the number of inputs, and the gate circuit configuration. This consideration becomes more important for a system designer who has harsh-noise-prone applications.

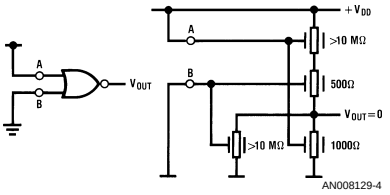
The value of the standard transistor ON resistance may vary from 10 MΩ down to almost 30Ω (depending on the dimensions of the MOS-FET and applied voltages). For different input conditions, different combinations of the impedances of the N-channel transistors connected in parallel and the P-channel transistors connected in series will come into play

for a NOR gate. This is illustrated in *Figure 2*. For a NAND gate, similar considerations hold good and give rise to varying transfer characteristics as shown in *Figure 3*.

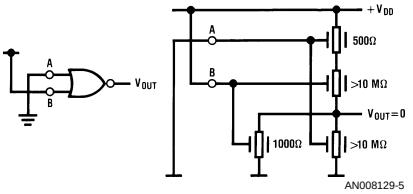
Example of CD4001



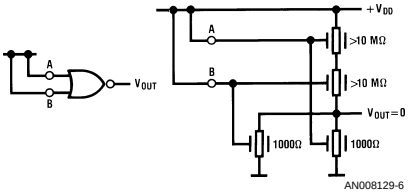
A=B=0



A=1, B=0



A=0, B=1



A=B=1

FIGURE 2. Typical Transfer ON/OFF Resistances for Various Input Combinations for CD4001

Analysis

The DC transfer characteristics of the CMOS inverter can be calculated from the simplified DC current-voltage characteristics of the N- and P-channel MOS devices.

In the transfer region, where both transistors are in saturation, the following relationships can be used for an inverter.

N-channel drain current will be:

$$I_{dsn} = \frac{K_n}{2}(V_{IN} - V_{TN})^2 \quad (1)$$

P-channel drain current will be:

$$-I_{dsp} = \frac{K_p}{2}(V_{IN} - V_{DD} - V_{TP})^2 \quad (2)$$

where:

$$K_n = \frac{\mu n\, C_{ox}\, W_n}{L_n},\ K_p = \frac{\mu p\, C_{ox}\, W_p}{L_p}$$

Taking the ratio of *Equation (2)* and *Equation (1)*:

$$\frac{|I_{dsp}|}{I_{dsn}} = \frac{K_p}{K_n} \cdot \frac{(V_{IN} - VDD - V_{TP})^2}{(V_{IN} - V_{TN})^2}$$

$$\frac{K_p}{K_n} = \frac{|Idsp|}{I_{dsn}} \cdot \frac{(V_{IN} - V_{TN})^2}{(V_{IN} - V_{DD} - V_{TP})^2} \quad (3)$$

Studies made at Fairchild show good correlations between the process monitor pattern and actual device on a wafer for drive currents. Thus the ratio K_p/K_n can be calculated for the actual device if one knows drive currents for the test pattern, widths of N- and P-channel devices and threshold voltages from a given process.

The transition voltage is calculated from basic current equations and from the fact that some current has to flow through P- and N-channel devices. Equating saturation currents and rearranging terms, one can obtain[1]:

Transition Voltage=V_{IN}*

$$= \frac{V_{TN} + \sqrt{\frac{K_p}{K_n}}(V_{DD} - |V_{TP}|)}{\sqrt{1 + K_p/K_n}} \quad (4)$$

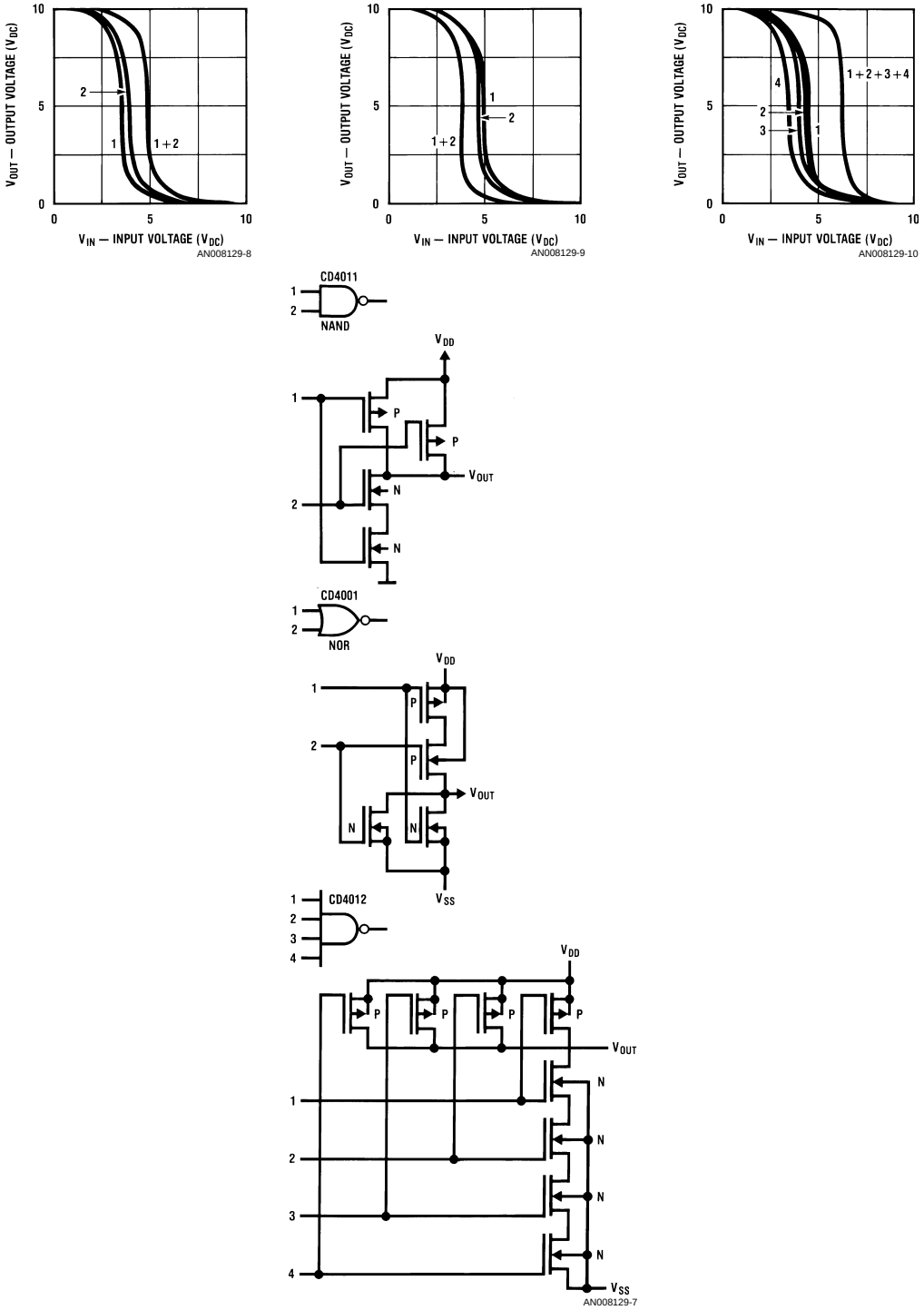


FIGURE 3. Allowed Voltage Transfer Curve Shifts which Result Due to Various Input Combinations of Multiple Input Gates

By selecting $|V_{TP}|=V_{TN}$ and $K_p=K_n$, transition voltage can be designed to fall midway between 0V and V_{DD}—an ideal situation for obtaining excellent noise immunity. However, it is not always possible to obtain equal threshold voltages because of process variations. Also, W/L ratio for a P-channel device must be made 2 or 3 times larger than W/L ratio for an N-channel device to take into account mobility variations. The designer should consider these factors when designing for the best noise immunity characteristics.

In *Equation (4)*, the value of K_p/K_n substituted is obtained from *Equation (3)*. With different gate configurations, effective W_p and W_n values change; also, K_p/K_n ratio changes and a shift in transfer characteristics results.

For the 4-input NOR gate like CD4002, an empirical relation for the low noise margin V_{NL} has been obtained, which is as follows:

$$V_{NL} \approx V_{DD}\left[\frac{1}{1.5+\frac{N_i}{N_m}}-0.1\right] \quad (5)$$

where:

N_i=number of used inputs/gate

N_m=total number of inputs/gate

The input voltage high noise margin V_{NH} can be calculated by:

$$V_{NH} \approx V_{DD}\left[0.9-\frac{1}{1.5+\frac{N_i}{N_m}}\right] \quad (6)$$

Similar equations can be derived for a NAND gate.

From *Equation (5)* and *Equation (6)*, one can see that the low noise margin V_{NL} will *decrease* as a function of the number of controlled inputs, while it will increase for a NAND gate. The input HIGH noise margin will *increase* as a function of the number of controlled inputs for the NOR gate; for the NAND gate it will decrease.

Figure 4 depicts $V_{OUT}=f(V_{IN})$ for different configurations for NOR and NAND gates. The system designer can thus use these facts effectively in his design and obtain the best possible configuration for the desired noise immunity with Fairchild's logic family.

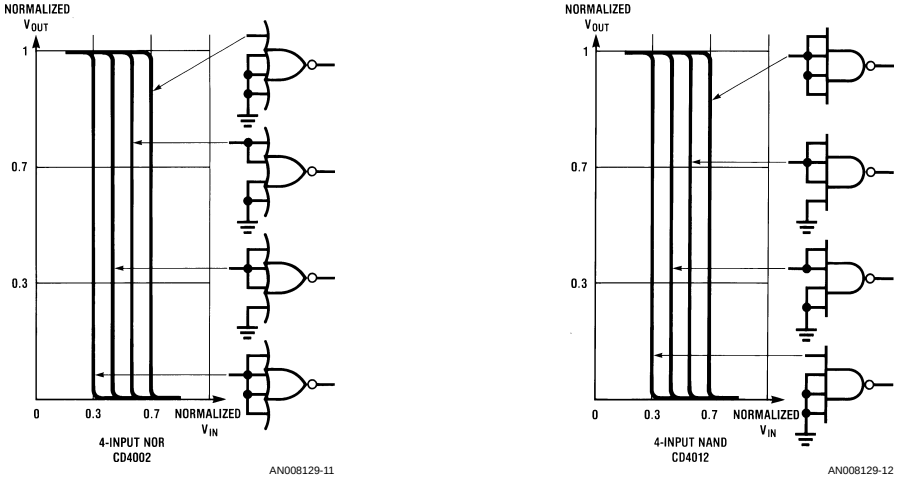
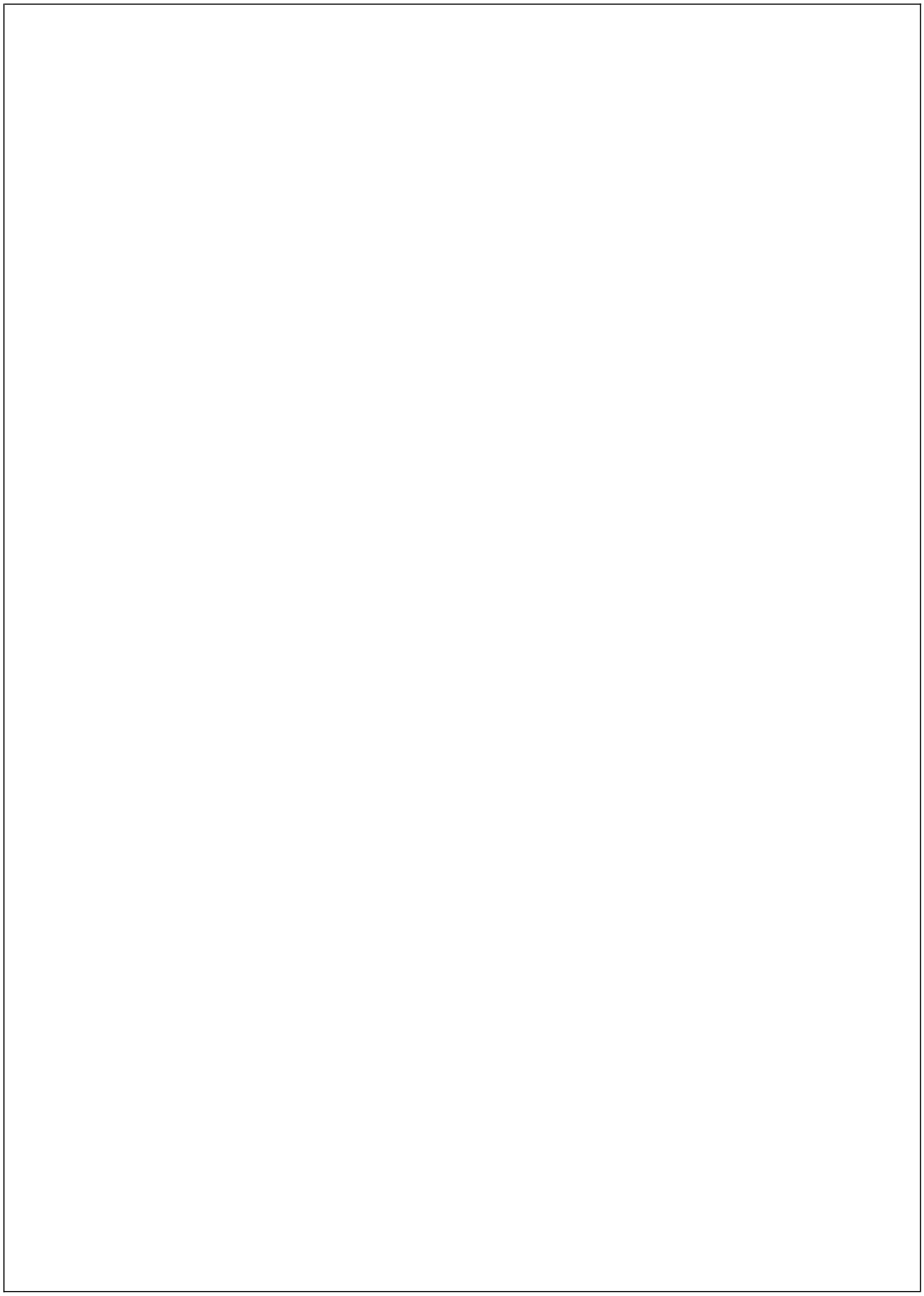


FIGURE 4. Example of Transfer Voltage Variation for NOR and NAND Gates for Various Input Combinations

1. Carr, W.N., and Mize, J.P., *MOS/LSI Design and Application*, Texas Instruments Electronic Series, 1972



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