

Single Low-Supply Current-mode CMOS Analog Multiplier Circuit

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Abstract— A simple structure of low-voltage current-mode CMOS analog multiplier circuit is presented. This multiplier circuit is based-upon quarter square algebraic identity technique by using CMOS technology. The transistors are operated in saturation region for different sub-circuits. The electronic resistor circuits are used as the input stage. The differential amplifiers are used for biased the squaring circuits. The current-mode operation can be obtained with a single supply, low-voltage, high-linearity and wide-bandwidth. This paper consists of 16 NMOSs with a 1.5 volts single supply. The achieved circuit performances have been carried out by PSpice. The input range is obtained more than $\pm 100\mu\text{A}$ with linearity error less than 1%. The frequency response can be operated larger than 150 MHz.

I. INTRODUCTION

The multiplier circuit is a very useful building block and can be applied to any analog signal processing as well as analog filter, frequency doubler, modulator etc. This paper proposes the current-mode CMOS multiplier circuit that based on a Quarter-Square Algebraic Identity technique. It consists of 2 identical structures of electronic resistors, differential pairs and squaring circuits. The single low-supply, high-linearity and wide-bandwidth can be obtained with a simple structure. The wide-input range can be also achieved and adjustable.

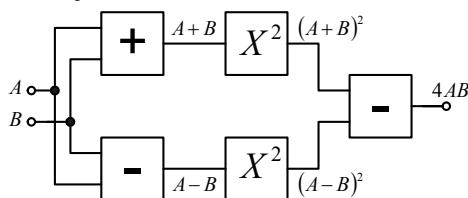


Fig.1 Quarter-Square Algebraic Identity Technique

II. QUARTER-SQUARE ALGEBRAIC IDENTITY

The Quarter-Square Algebraic Identity [2] is famous method for a multiplier implementation. There is 3 steps as shown in Fig. 1 and can be described below:

1. Sum and Subtraction both inputs.
2. Take their results of 1st step to squaring.
3. Subtraction of 2nd step with each other that output can be express as

$$V_O = [(V_1 + V_2)^2 - (V_1 - V_2)^2] = 4V_1V_2 \quad (1)$$

III. PRINCIPLES

A. Electronic Resistor Circuit [1]

This circuit employs 2 NMOS that connected as shown in Fig.2. The transistors are operated in saturation region. The voltage output (V_O) can be obtained by applying input current (I_{in}). The output voltage can be written as Eq. (2)

$$V_O = \frac{I_{in}}{k_1(V_{DD} - 2V_T)} + \frac{V_{DD}}{2} \quad (2)$$

$$\text{Where } k_1 = \mu C_{ox} \left(\frac{W}{L} \right)_1$$

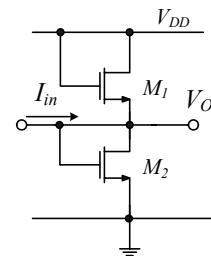


Fig. 2 Electronic Resistor Circuit

B. CMOS Differential Amplifier Circuit

Fig. 3 shows a CMOS differential amplifier circuit. The 4 MOS transistors are identical which biased by current source I . The differential outputs are according to differential input based on saturation region of MOS transistors. The voltage output can be written as follows:

$$V_O = V_{O1} - V_{O2} = -(V_A - V_B) \quad (3)$$

Actually, the input V_B is set to $\frac{V_{DD}}{2}$ in order to obtain the identical outputs swings. The output of differential

amplifier can be obtained as inverting of each other in order to applying for the particular next squaring circuit.

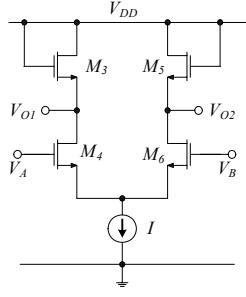


Fig. 3 CMOS Differential Amplifier Circuit

C. CMOS Differential Squaring Circuit

The operation of MOS transistor in saturation region is satisfied of square's law characteristic. The drain current of each transistor can be expressed in term of squaring function. The completed squaring function as shown in Fig.4 can be achieved by differential of summing drain current I_{O1} and I_{O2} . The current output can be expressed as

$$I_{O1} = k_2 [V_1^2 + (V_x - V_{TN})^2] \quad (4)$$

$$I_{O2} = k_2 [V_2^2 + (V_x - V_{TN})^2] \quad (5)$$

$$I_{OUT} = I_{O1} - I_{O2} = k_2 (V_1^2 - V_2^2) \quad (6)$$

Where $k_2 = \mu C_{OX} \left(\frac{W}{L} \right)_2$

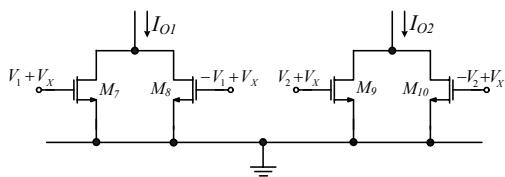


Fig. 4 Differential Squaring Circuit

III. LOW-SUPPLY CURRENT-MODE ANALOG MULTIPLIER

The complete proposed current-mode multiplier circuit can be realized by above principles. The proposed multiplier can be implemented by a symmetry structure as shown in Fig.5. The achieved output current can be found in term of a multiplication of input current, I_1 and I_2 . The +1.5V single power-supply, +0.75V bias voltage (V_B) and 80 μ A bias current (I) are used. The multiplier function output can be expressed as

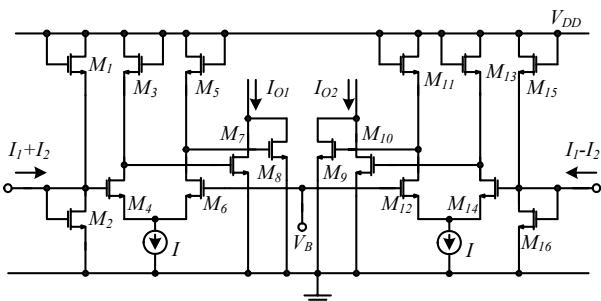


Fig. 5 The proposed current-mode multiplier

$$I_{OUT} = I_{O1} - I_{O2} = \frac{\left(\frac{W}{L} \right)_2 4 I_1 I_2}{\mu C_{OX} \left[\left(\frac{W}{L} \right)_1 (V_{DD} - 2V_T) \right]^2} \quad (6)$$

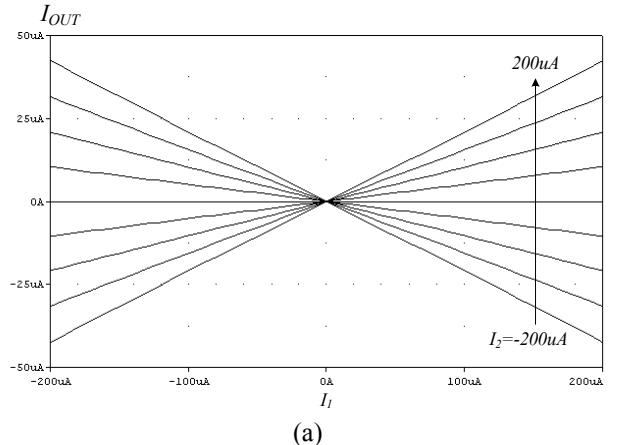
IV. THE SIMULATION RESULTS

The proposed multiplier in Fig.5 can be confirmed the performances by PSpice. The level 3 model T14Y MOSIS 0.25 μ m with the $V_{TN} = 0.42$ V, $V_{TP} = -0.55$ V, $\mu_N C_{OX} = 250.1048 \mu A/V^2$ and $\mu_P C_{OX} = 51.94153. \mu A/V^2$. The aspect ratio of transistors is shown in table 1.

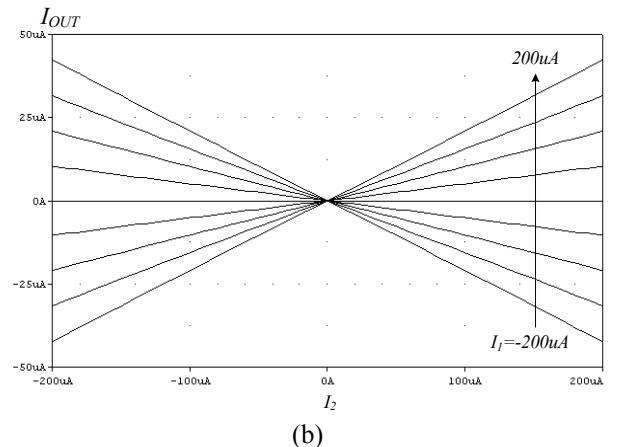
Table 1. The aspect ratio of transistors

Transistor	W/L(μ m/ μ m)
M ₁ , M ₂ , M ₁₅ , M ₁₆	60/1
M ₃ -M ₁₄	50/1

The DC-characteristic is shown in Fig. 6(a) and (b) while I_1 and I_2 input, respectively. It can be shown the linearity and $\pm 200 \mu A$ dynamic range operation. The linearity error of proposed circuit can be done by fixed maximum input I_1 while I_2 is varied and vice versa. The result of linearity error is shown in Fig. 7 that less than 2%.

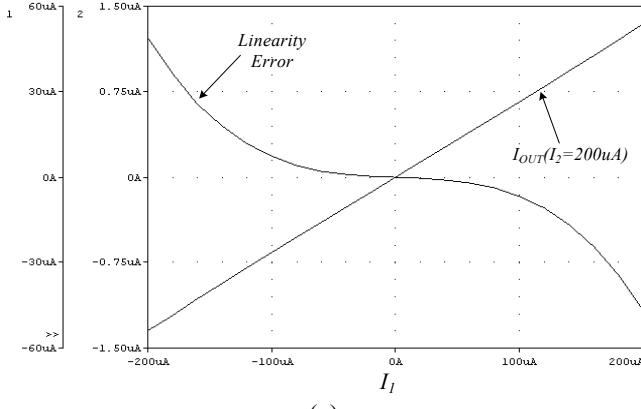


(a)

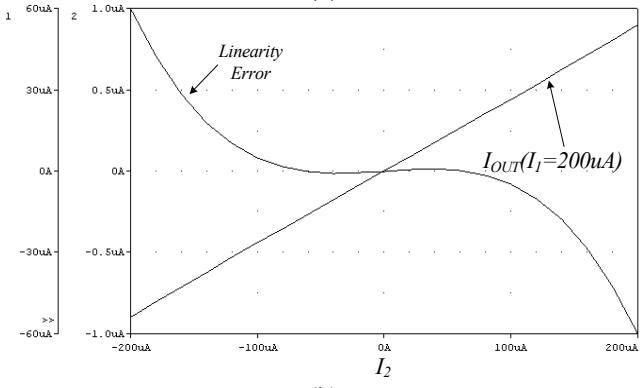


(b)

Fig. 6 The DC-characteristic of proposed multiplier



(a)



(b)

Fig. 7 Linearity error of proposed multiplier

The Fig.7 shows a linearity within the $\pm 200\mu\text{A}$ input range. The quite small linearity error is less than 0.8% while input within $\pm 100\mu\text{A}$. The actually input range can be applied more than $\pm 200\mu\text{A}$ but the linearity error will become too large. The linearity error is a main error that conforms to a THD (Total Harmonic Distortion).

The THD instances for fixed a frequency input at 1MHz and fixed input range have been illustrated in Fig.8 and 9, respectively. Consider the linear range at $\pm 100\mu\text{A}$, the THD is lowest less than 1%. The THD is highest while input range $\pm 300\mu\text{A}$ accordingly.

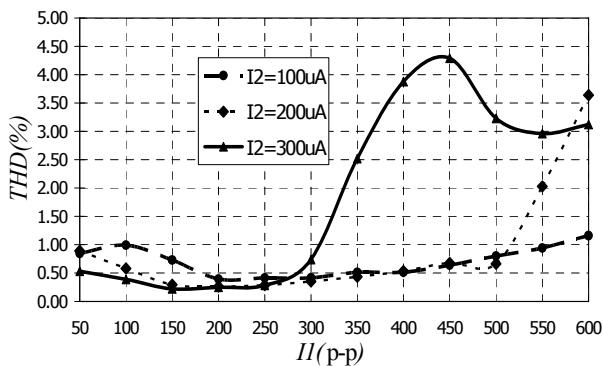


Fig. 8 THD @1MHz input of proposed circuit

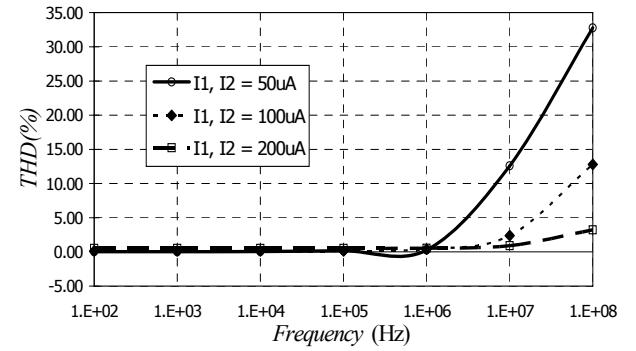


Fig. 9 THD in different frequency of proposed circuit

Fig. 10 is shown a bandwidth of proposed circuit that larger than 150 MHz while input I_2 is constant at $200\mu\text{A}$.

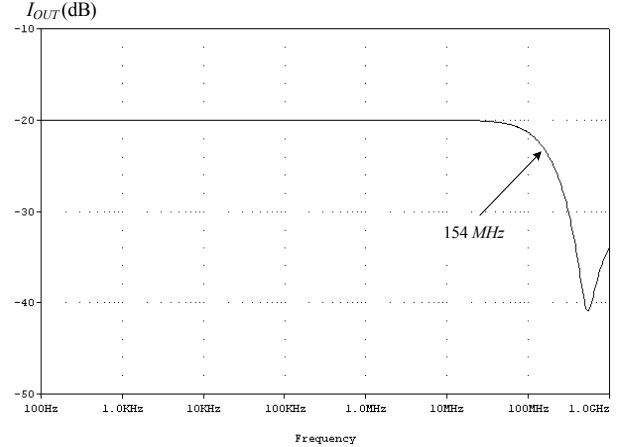


Fig. 10 Bandwidth of proposed circuit

The comparison of proposed circuit with previous works is shown in Table.2.

	[3]	[4]	[5]	[6]	Proposed
Supply	+5V	-	+3.3V	$\pm 1.5\text{V}$	$\pm 1.5\text{V}$
THD (%)	1.54 @1MHz	-	-	.014 @20kHz	0.25 @1MHz
Linearity Error	1.22%	<1%	<0.49%	2%	0.8%
Input Range	$\pm 20\mu\text{A}$	$\pm 200\mu\text{A}$	$\pm 50\mu\text{A}$	$\pm 0.8\text{V}$	$>\pm 100\mu\text{A}$
freq -3dB	22.4MHz	50MHz	66MHz	5MHz	154MHz
Tech.	2 μm	-	-	0.8 μm	0.25 μm

Table 2 The comparison of proposed circuit with previous works

V. APPLICATION

The other result for the realistic application of proposed circuit is amplitude modulation (AM). The frequency of carrier and input are 10 MHz and 500 kHz, respectively. The amplitude of both inputs is $\pm 400\mu\text{A}$ p-p. The input signal and AM output are shown in Fig. 10.

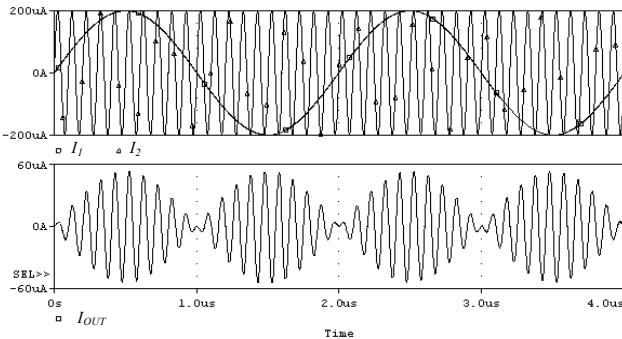


Fig. 11 AM output signal while input is 10MHz and 500kHz

VI. CONCLUSION

This paper proposes a low-voltage current-mode CMOS four-quadrant analog multiplier based on a quarter-square algebraic identity. The saturation region of MOS transistors is operated for particular sub-circuits. The THD and linearity error are less than 1%. The achieved dynamic range is more than $\pm 100\mu\text{A}$ with a single +1.5V power supply condition. The wide bandwidth 154 MHz is illustrated. The good performances are compared with the previous papers. The AM is an application for confirm the realistic applied of proposed circuit.

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