Synchronization Scheme for Low Duty Cycle UWB Impulse Radio Receiver

Heinrich Luecken, Thomas Zasowski, and Armin Wittneben Communication Technology Laboratory, ETH Zurich, 8092 Zurich, Switzerland {lueckenh, zasowski, wittneben}@nari.ee.ethz.ch

Abstract—Ultra-wide band (UWB) communication shows great potential for low-power communication for wireless sensor or body area network (BAN) applications. In particular, noncoherent receivers can be implemented with very low complexity. However, impulse radio and low duty cycle signaling involve stringent requirements on timing recovery. Standard synchronization algorithms might not be applicable due to constraints on memory capacity, clock accuracy and the sampling frequency of the receiver. Therefore, we present a scheme for burst detection and joint frame and symbol synchronization where both transmitter and receiver respect the low-duty cycle requirements. Furthermore, a subsampling analog-to-digital converter with a free running clock is assumed to meet low-power constraints. Burst detection is based on correlation with a known synchronization sequence. For symbol synchronization digital reconstruction of the symbol timing is applied, based on an FIR interpolation filter. Finally, it can be seen from performance results with real measured BAN channels that the presented synchronization algorithm is very well suited for the use in such applications.

I. INTRODUCTION

One of the most promising technologies for the use in wireless body area networks is ultra wideband (UWB) communications. Due to the relatively small delay spread and the moderate path loss in a body area network (BAN), very high peak data rates can be achieved with this technology. Such high peak data rates in combination with a very low duty cycle operation allow for realization of medium data rate systems with ultra low power consumption. Recently, an energy detector based UWB transceiver structure for wireless sensor networks and BAN was presented [1]. The power consumption of this transceiver is estimated to be less than 1 mW. The average data rate of 500 kbps is achieved by transmission with 1% duty cycle and a peak data rate of 50 Mbps. To allow for burst-wise processing and reduced clock frequency in the digital part of the transceiver, analog and digital part are decoupled by a random access memory (RAM). The limited memory size and processing resources prohibit the use of standard synchronization schemes [2]. Therefore, in this paper a synchronization scheme is presented which also considers the limitations given by the low duty cycle operation and energy detector frontend.

The low-complexity demands and the specific transceiver design in [1] also impose special requirements on the synchronization. Although there exist approaches with reduced sampling rates as suggested in [3] the necessary sampling rates are still in the order of the inverse of the pulse duration. This would result in a sampling rate that is about two to three times higher than the one specified in [1]. Synchronization for a subsampling receiver with low sampling rates is evaluated in [4] but does not consider an energy detection receiver. In [5], a synchronization scheme has been presented for an energy detection receiver. This scheme shows a good performance, but requires eight integrators, which increases complexity and power consumption of the transceiver as presented in [6].

In this paper, we present a synchronization scheme for low complexity energy detection receivers with low-duty cycle operation. The synchronization is divided into three phases. Burst synchronization is based on transmission and correlation of a training sequence, while symbol synchronization is achieved by interpolation of the receive signal and adaptation of the sampling instance in digital domain. For performance evaluation, we assume the system requirements from [1]. However, the presented synchronization scheme can be applied for different burst lengths and duty cycles.

The remainder of the paper is organized as follows. In Section II, a short overview on the considered system model of the energy detector is given. Burst and symbol synchronization algorithms for energy detection based low-duty cycle systems are presented in Section III and Section IV, respectively. The performance which can be achieved using these both synchronization schemes is presented in Section V and compared to the optimum synchronization. Finally, conclusions are presented in Section VI.

II. SYSTEM MODEL

A block diagram of the considered energy detection receiver chain is shown in Fig. 1. A burst wise transmission using pulse-position modulation (PPM) with a duty cycle of $\eta = 1\%$ and a peak data rate of 50 Mbps is assumed yielding an average data rate of 500 kbps. Using such a low duty cycle a very low power consumption can be achieved and requirements on the digital functionalities, as e.g. clock frequency or random access memory (RAM) size, can be relaxed. The frequency band between $f_1 = 3.5$ GHz and $f_u = 4$ GHz is chosen to achieve a small path loss as well as small interference from communication systems around 2 and 5 GHz. The receive signal is amplified by a low noise amplifier (LNA) and then filtered by a band-pass. With such an ordering reduced power consumption is achieved on cost of interference robustness. However, we assume that interference can be handled by appropriate interference avoidance schemes such as presented in [7]. After the bandpass filter, the signal is amplified by

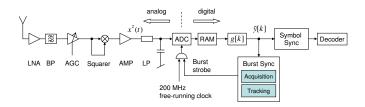


Fig. 1. System model of the considered energy detector

a variable gain amplifier (VGA) controlled by an automatic gain control (AGC), squared and amplified again by a third amplifier (AMP). The estimated over-all noise figure (NF) of the analog part of the receiver is 5.4 dB as shown in [1].

The amplified and squared receive signal including noise is denoted as $x^2(t)$, which is fed to a first order low-pass (LP). The impulse response of the low-pass is given by

$$h_{\rm LP}(t) = 1/T_0 \cdot e^{-t/T_0}$$
 for $t > 0$, otherwise 0, (1)

with $T_0 = (2\pi f_c)^{-1}$ and f_c denoting the low-pass cut-off frequency. The cut-off frequency is chosen to $f_c = 5$ MHz. The filtered signal $x_{LP}^2(t)$ is given by the convolution

$$x_{\rm LP}^2(t) = \int_0^\infty x^2(t-\tau) \cdot e^{-\tau/T_0} d\tau.$$
 (2)

The low-pass signal is sampled by an analog-to-digital converter with frequency $f_s = 1/T$ at time instances kT. The ADC together with a RAM builds the interface to the digital receiver part. The ADC is driven by a clock at two times the pulse rate, i.e., at $f_s = 200$ MHz, implying an over-sampling factor $N_{\text{ovsa}} = 2$. To achieve a finite integration window, which approximates an ideal integrator for energy detection a subsequent digital filter is used [8]. We propose to use an FIR filter g[k], which consists only of two filter taps chosen as g[0] = 1 and $g[1] = -\exp(-T/T_0)$. This leads to an integrator output of

$$\tilde{y}[k] = \int_0^T x^2 (kT - \tau) \cdot e^{-\tau/T_0} d\tau.$$
 (3)

For $T_0 \gg T$ the approximation $e^{-\tau/T_0} \approx 1$ can be used, simplifying (3) to

$$\tilde{y}[k] \approx \int_{(k-1)T}^{kT} x^2(\tau) d\tau, \qquad (4)$$

resulting in the desired integration over the time window of length T. Based on this signal, burst and symbol synchronization as well as the decoding are performed. This structure is an efficient way to limit the integration window length and shows good interpolation properties due to a low cut-off frequency of the low-pass.

III. BURST SYNCHRONIZATION

Due to constraints given by the limited RAM size, processing resources and clock frequency, the receiver cannot sense the channel continuously. Hence, burst and symbol synchronization schemes are proposed that are able to cope with the requirements of a low duty cycle transmission system. We consider primarily pairwise synchronization for point-topoint communication, e.g. to establish data transfer between two devices such as hearing aids. However, the presented scheme may be used as a building block for more complex schemes with suitable MAC.

Using low duty cycle operation, a node must switch on its receiver only during the time when the transmitter sends data, i.e. the periodic burst time window. In the time between consecutive bursts, the node can switch off the analog part of the receiver to save power. Hence, during burst synchronization the receiver has to estimate the burst time window and account for clock offsets.

The burst synchronization is split up into an acquisition, confirm and tracking phase as shown in Fig. 2. In acquisition phase, a coarse synchronization is obtained such that receiver and transmitter are using the same wakeup and sleep window. After detecting the burst, in a confirmation state the result of the acquisition is verified. If that is successful, the transceiver changes to tracking state and the data transfer can be established. In tracking state the fine alignment of the duty cycle is done as well as a joint frame and symbol synchronization. Clock mismatches are accounted for by tracking the burst window with a standard delay locked loop (DLL) architecture. For instance, this can be done with a low-complexity first order closed loop control.

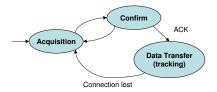


Fig. 2. State diagram of the synchronization scheme

For acquisition of the burst timing window the low duty cycle signaling must be taken into account. Due to the limited RAM size and the slower clock in the digital part of the receiver it is not possible to search for the signal continuously over time. Assuming a duty cycle of $\eta = 1\%$, it would be desirable also for the acquisition to switch on the analog part of the receiver only in the order of 1% of the time. Fig. 3 shows the timing diagram of the proposed synchronization scheme for the burst acquisition and confirm state. Two nodes synchonize mutually their receive time window. The nodes transmit beacon bursts periodically every 1 ms with a duration

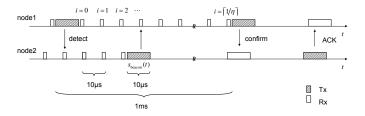


Fig. 3. Timing diagram of burst synchronization

of 10 μ s according to the low duty cycle operation. The beacon bursts consists of a repetition of a known sequence with good autocorrelation properties of length N_{seq} . Between sending the bursts, the receiver senses the channel every 10 μ s, but only for the few samples of the sequence length N_{seq} . This signal is repeatedly stored in memory for one burst period, whereas in the meantime the analog receiver can be still switched off. In that way, the memory requirements are relaxed and it is still assured that the burst window is covered and the stored signal contains the correlation sequence. The search window is denoted by *i*, with correspondingly $i = 0, 1, \ldots, \lceil 1/\eta \rceil$, where η denotes the duty cycle. It is necessary to sense the channel $\lceil 1/\eta \rceil + 1$ -times to cover the burst window. Every of these listen time slots comprises $N_{\text{seq}} \cdot N_{\text{ovsa}}$ -samples, since at least one full sequence should be contained in a window.

As correlation sequences Barker and M-sequences are considered. The synchronization sequence is modulated by onoff-keying (OOK), to provide better correlation properties compared to PPM. The pulse rate is correspondingly 100 MHz. Hence, the transmission signal of the beacon can be written as

$$s_{\text{beacon}}(t) = \sum_{n=1}^{N_{\text{beacon}}} \sum_{k=1}^{N_{\text{seq}}} c[k] \cdot p\left(t - (k + nN_{\text{seq}})\frac{T_{\text{symb}}}{2}\right)$$
(5)

where $p(\cdot)$ denotes the transmit pulse shape, $c[k] \in \{0, 1\}$ the synchronization sequence, $T_{\text{symb}}/2$ the pulse repetition time and N_{beacon} the number of sequence repetitions per burst. Accordingly the signal $s_{\text{beacon}}(t)$ is transmitted every 1 ms.

Detection is performed by the maximum of the periodic correlation, which is given by

$$\tilde{\varphi}_{i} = \max_{m} \sum_{k=1}^{N_{\text{seq}}} \tilde{c}[k] \tilde{y}_{i} \left[(kN_{\text{ovsa}} + m) \mod N_{\text{seq}} N_{\text{ovsa}} \right]$$
(6)

where $\tilde{c}[k] = 2c[k] - 1$ is the synchronization sequence in $\{-1, 1\}$. In that way the DC offset can be removed from the signal. The periodic correlation is computed over the received data samples of the different time slots *i*. The algorithm assumes that the maximum of the correlation corresponds to the burst window. Therefore, the estimated burst time window index is given by

$$\hat{i} = \arg\max\tilde{\varphi}_i.$$
 (7)

Accordingly the burst strobe will be set to time window \hat{i} and the receiver switches to confirm state. In confirm state, the channel is sensed over a full burst time, centered around the estimated time window. The correlation with the known sequence can now be computed over multiple repetitions achieving a higher processing gain. The length of the uncertainty window is now in the order of the processing resources of the considered system. Therefore standard estimation methods can be used as shown in [9]. If the peak of the correlation is above a threshold, it is assumed that the acquisition was successful and it can be switched to data transfer and tracking state. Otherwise, the receiver goes back

to acquisition state and searches for the burst time window again. The transmitter keeps on sending the beacon burst. If the acquisition could not be confirmed after several cycles, the transmitter induces a random back-off, accounting for the unlikely situation of colocated beacons or the case that no other node is in communication range.

IV. SYMBOL SYNCHRONIZATION

Knowing the coarse position of the bursts after burst synchronization, symbol synchronization is performed for data detection. The symbol synchronization is split up into timing estimation and timing recovery. The timing estimation algorithm determines the starting point of the burst and the fractional delay of the sampling point. Using this information, timing recovery applies an interpolation filter to reconstruct the sampling point for symbol decision by the decoder [10]. The concept is depicted as a block diagram in Fig. 4. The interpolation filter is denoted as $h_{\hat{\varepsilon}}[k]$ and implemented as an FIR filter.

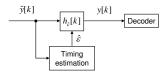


Fig. 4. Block diagram of symbol synchronization by interpolation

Timing estimation is based on a preamble. The data burst packet structure consists of a preamble followed by the data symbols. It is chosen that every burst contains $N_{\text{symb}} = 500$ data symbols, whereas the preamble is based on an M-sequence of length N_{sync} . Similar to burst synchronization the preamble is modulated with OOK. In that way, the crosscorrelation between data and training sequence is small, since the data is modulated by PPM.

After detection of the burst position the receiver searches over the receive signal, which is stored in memory. The correlation of the receive signal $\tilde{y}[k]$ and the known Msequence $\tilde{c}[k]$ is given by

$$\varphi[m] = \sum_{k=1}^{N_{\text{sync}}} \tilde{c}[k] \cdot \tilde{y}[kN_{\text{ovsa}} + m].$$
(8)

The ideal correlation function is assumed to be triangular, as depicted in Figure 5.

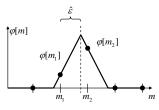


Fig. 5. Correlation function and timing estimation

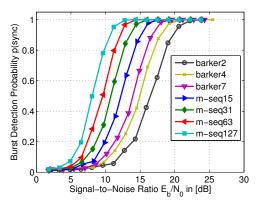


Fig. 6. Burst detection probability in AWGN channel

Therefore, the optimal sampling point (corresponding to the widest eye opening) can be estimated based on the maximum of the computed correlation and the bigger of the two neighbors, denoted as $\varphi[m_1]$ and $\varphi[m_2]$, respectively. By superimposing the assumed triangular correlation function the correlation peak is given by geometric relation as

$$\hat{\varepsilon} = \frac{\varphi[m_2]}{\varphi[m_1] + \varphi[m_2]},\tag{9}$$

where $\hat{\varepsilon}$ denotes the estimated sampling offset. This estimated offset is handed over to the interpolation filter. For frame synchronization m_1 is used by the decoder to determine the start of the data symbols.

The interpolation filter $h_{\hat{\varepsilon}}[k]$ computes intermediate values $y(kT - \hat{\varepsilon})$ between the signal samples $\tilde{y}[m]$. If aliasing effects are neglected due to non-ideal low-pass filtering, the time-shifted signal denoted as $y(kT - \hat{\varepsilon})$ could be perfectly reconstructed. An optimal MMSE interpolator can be designed by using a Wiener filter as shown in [11]. However, due to complexity constraints, we use a 4-tap approximation of the fractional delay by the general least squares method as shown in [12]. For practical implementation the interpolation filter can be combined with the filter g[k], which was described in Section II.

V. PERFORMANCE RESULTS

The performance of the proposed receiver and synchronization algorithm is evaluated by simulation. For burst synchronization the detection probability is chosen as figure of merit, whereas for symbol synchronization the bit error rate (BER) is simulated. The performance is plotted versus the signal-tonoise ratio (SNR) E_b/N_0 , where E_b denotes the energy per bit and N_0 the noise power spectral density. The transmit pulse is shaped by a 3rd order butterworth bandpass. As specified in [1], for the analog part of the receiver a noise figure of 5.4 dB is assumed. The clock inaccuracy and jitter are assumed to be negligible during one burst.

Fig. 6 shows the performance of the burst detection scheme. The acquisition of the time window is simulated for synchronization sequences of different length. Barker sequences of length 2, 4 and 7 bits are chosen as well as M-sequences of

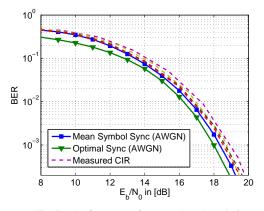


Fig. 7. Performance of proposed modem design

length 15, 31, 63 and 127 bits. The burst detection probability is estimated by Monte Carlo simulation, where a frequencyflat channel and additive white Gaussian noise (AWGN) is assumed. The receiver assumes a randomly chosen sampling offset ε , which is uniformly distributed in [0, T] and constant for one burst. A correct burst synchronization is assumed if the maximum over the correlation as given by (7) corresponds to the right time window. In all the other cases false synchronization is assumed and accordingly the burst detection probability p(sync) is derived.

The simulation results show the dependency of burst detection probability on the sequence length. The lower the SNR, the longer the sequence need to be to still provide a sufficient detection probability. However, with increasing sequence length not only the memory and computational complexity grows but also the duty cycle of the receiver during the burst synchronization phase.

Requiring a detection probability of p(sync) = 0.98 at an SNR of $E_b/N_0 = 17$ dB the necessary sequence length can be read off from Fig. 6. It can be seen that a sequence length of 15 bits is sufficient. A sequence length of 15 Bit and a duty cycle of 1% implies for the proposed algorithm a necessary memory size of 3000 samples. The proposed algorithm is robust against misclassification due to the confirm state and acknowledgment, before data transmission can be established. Therefore a detection probability of p(sync) = 0.98 is sufficient for reliable operation of the burst synchronization scheme.

Symbol synchronization and frame synchronization are evaluated by simulation of the data transfer. We assume an uncertainty window of 100 samples for the burst strobe, which corresponds to a clock inaccuracy of 500 ppm. A packet structure with a M-sequence as preamble of length $N_{\text{sync}} = 31$ bits is chosen, followed by 500 data bits in BPPM. Fig. 7 shows the bit error rate versus the SNR. The curve marked with squares shows the performance of the proposed receiver and symbol synchronization algorithm. The performance is averaged over the sampling offset ε , which is assumed to be uniformly distributed in [0, T]. The curve marked with triangles shows the performance of the modem for optimal synchronization. It can be seen that on average the symbol synchronization induces a performance loss of

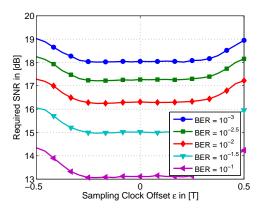


Fig. 8. Required SNR for different sampling offset and BER

about 0.4 dB in high SNR region compared to the perfect synchronization. At low SNR a larger gap can be observed due to the limited length of the synchronization sequence. The estimate of the sampling offset $\hat{\varepsilon}$ becomes noisy and errors due to false frame synchronization can occur. However, subtracting the noise figure of the analog part of the receiver of 5.4 dB, the performance is only about 2 dB worse compared to the AWGN bound for noncoherent PPM detection [13]. This performance degradation is due to non-ideal filters and pulse shape. The dashed lines show the performance of the modem using impulse responses of four measured BAN channels [14]. The channels were measured on a human head from ear to ear. The performance loss due to the frequency selective channels is in the order of 0.5 dB.

To analyze the influence of the timing recovery and interpolation, the bit error rate for arbitrary fixed sampling offsets ε is shown in Fig. 8. It can be seen that in a certain range the reconstruction by interpolation shows marginal performance loss. However, if the sampling points have been picked at the worst time instances, a performance loss of about 1.1 dB can be observed. This is due to aliasing effects and the suboptimal interpolation filter. The signal can not be reconstructed exactly because the low pass filter is not ideal.

To specify the length of the preamble for data packets, the timing estimation has been investigated. An M-sequence of length $N_{\rm sync} = 31$ Bits turns out to be sufficient. Based on this sequence, Fig. 9 shows the root mean squared (RMS) of the estimation error for the sampling offset $\hat{\varepsilon}$ obtained by (9). The RMS is plotted for different values of ε . It can be seen, that above an SNR of 15.5 dB the estimation error is below 0.1 samples. In high SNR, the estimator (9) performs better for ε around 0.5*T*, because the signal energy is split to $\varphi[m_1]$ and $\varphi[m_2]$. For ε around 0, one of correlation results is dominated by noise, leading to the performance characteristic as shown in Fig. 9.

VI. CONCLUSIONS

A digital synchronization scheme for burst and joint symbol and frame synchronization for an impulse radio UWB receiver was investigated. Performance results show that for burst synchronization a 15 bit M-sequence is sufficient. Symbol

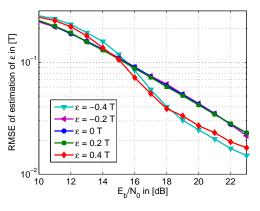


Fig. 9. Estimation error of estimated sampling offset

synchronization by using an FIR interpolation filter shows on average a performance loss of about 0.4 dB. This relaxes requirements on the sampling frequency of the ADC, memory size and the computational complexity.

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