Message from the Editors

The chapters of this edited volume present original research first publicly revealed at the 2007 International Workshop on Innovative Architecture for Future Generation High Performance Processors and Systems (IWIA'05). The meeting took place at Maui Research & Technology Center, Maui, Hawaii in January 2007. These meetings promote interaction between computer architects, compiler writers and application developers. The 2007 special focus was on multi-core systems and hierarchical systems and ways to explore single-program parallelism on such systems. Today's processors are increasingly multi-core and significant performance gains as well as cost and power savings can be achieved if applications are parallelized.

A total of 19 researchers from the US, Europe, and Japan representing both academia and industry presented their current work and discussed future directions at the meeting. Participants were invited based on submission and review of their extended abstracts. The attendees were given an option to submit a full paper after the meeting for review and possible publication in this volume. The twelve chapters of this volume are the result of these submissions, which were reviewed and selected by the program committee.

We would like to thank all the authors who submitted a paper for publication in this special volume. The editors also thank the program committee members and the external reviewers without whose hard work this volume would have been impossible. Finally, the help and support of Tak Sagimura of Maui Research and Technolgy Center are gratefully acknowledged.

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