Low-dropout voltage reference: an approach to low-temperature-sensitivity architectures with high drive capability

H. Aminzadeh, R. Lotfi and K. Mafinezhad

A modified circuit topology for voltage references capable of providing very high load current with low-temperature-sensitivity output voltage is presented. Employing a proportional-to-absolute-temperature current source and a complementary-to-absolute-temperature voltage source in a novel closed-loop configuration, the output voltage can be tuned over a wide range of voltages lower or higher than the silicon bandgap voltage. These features make the configuration a promising competitor for low-dropout regulators. A possible implementation of the proposed topology in 0.18 μm technology shows that the simulated 0.9 and 1.3 V voltage references have fast and stable operation for load currents up to 100 mA. The temperature coefficient for both design cases is smaller than 37 ppm/°C.

Introduction: To provide large AC and DC load currents, voltage references with low output-impedance are essential for many applications [1]. With no output buffer placed in series, a first-order sub-bandgap reference able to sink and source load currents up to 5 mA is proposed in [1]. The circuit is based on a BiCMOS error amplifier with proportional-to-absolute-temperature (PTAT) input-referred offset. However, full-CMOS circuit realisations with higher order of temperature compensation are of more interest.

Many techniques have been proposed to implement bandgap references with high-order temperature-compensation [2]. However, most of them cannot provide any current [3], some generate a fixed reference value [3], many cannot be designed for sub-bandgap voltages [2], and some have implementation issues such as a pre-regulated output requirement and/or precisely-matched current mirrors [2]. In this Letter, we present a modified architecture which combines many essential features such as small dropout voltage, high output current, and low temperature sensitivity.

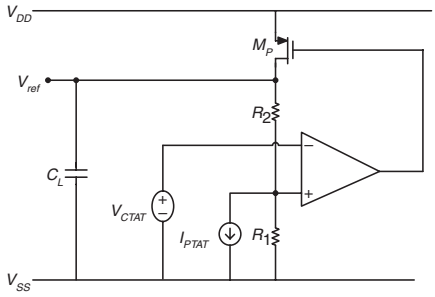

Fig. 1 *Proposed architecture for buffered voltage reference*

Proposed architecture: operation principle: Fig. 1 shows the proposed architecture which can be a substitute for low-dropout regulators (LDOs). The negative input terminal of the error amplifier is biased via a simple complementary-to-absolute-temperature (CTAT) voltage source. To directly compensate for the temperature dependence of the output voltage, a PTAT current source is also added. Assuming a high DC gain for the amplifier, the reference voltage (V_{ref}) can be calculated from

$$V_{ref} = (1 + \frac{R_2}{R_1})V_{CTAT} + R_2 I_{PTAT} \tag{1}$$

Hence, if carefully designed, a buffered yet tunable voltage reference with minor sensitivity against temperature variations is realised. In order to have a zero-temperature coefficient (ZTC), the derivative of (1) against temperature must become equal to zero; i.e.

$$\begin{aligned} &\left(1 + \frac{R_2}{R_1}\right)\frac{\partial}{\partial T}V_{CTAT} + R_2\frac{\partial}{\partial T}I_{PTAT} = 0 \\ &\Rightarrow \frac{\partial}{\partial T}V_{CTAT} = -(R_1||R_2)\frac{\partial}{\partial T}I_{PTAT} \end{aligned} \tag{2}$$

If (2) holds at a temperature, the output will not be a function of the temperature. Therefore, while the value of $R_1 \| R_2$ determines the temperature dependence of the output voltage, the ratio of R_2/R_1 can be used to set its absolute value. Another advantage of the proposed architecture is the small dropout voltage; i.e. similar to an LDO, the difference between supply voltage (V_{DD}) and V_{ref} can be kept as low as a couple of hundred millivolts even if the load current (I_{Load}) is increased to several milliamps.

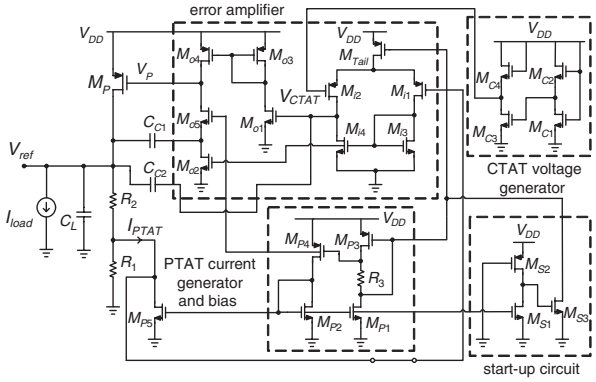

Fig. 2 *Complete schematics of proposed architecture*

Proposed architecture: implementation: A possible implementation of the proposed circuit of Fig. 1 is shown in Fig. 2. With good approximation, the threshold voltage of MOS transistors decreases linearly with temperature, according to $V_{TH}(T) = V_{TH}(T_0) - \alpha(T\text{-}T_0)$ (T is the absolute temperature and T_0 is the temperature where α has been evaluated [3]). Based on this observation, the CTAT voltage reference of Fig. 1 has been implemented using a simple architecture generating a threshold-referenced output (see Fig. 2) [4]. For imperfect line regulation, the output voltage mathematical representation of this circuit consists of two terms with different weights. One of these terms is related to V_{DD} and the other to V_{TH}. Under certain circumstances for device sizes, the term related to V_{DD} becomes zero, leading to

$$V_{CTAT} = \sqrt{\gamma}V_{TH} \tag{3}$$

where $\gamma = (W/L)_{C3}/(W/L)_{C4}$. A start-up stimulation mechanism is not required for this unit since an operating point with no current flowing is not stable.

To make the structure fully compatible with CMOS technology, the PTAT current source is implemented based on an approach utilising MOS devices in weak inversion (Fig. 2) [5]. As a particular case of general equations, setting $(W/L)_{P1} = (W/L)_{P2} = (W/L)_{P5}$ and $(W/L)_{P4}/(W/L)_{P3} = e$ will make all currents PTAT and I_{PTAT} will be

$$I_{PTAT} = \frac{nV_T}{R_3} = \frac{nkT}{qR_3} \tag{4}$$

where n is the subthreshold slope parameter, k is the Boltzmann constant and q is the electron charge. In addition to generating the required PTAT current, this circuit is also used to bias the amplifier core of the reference.

The proposed implementation for the error amplifier is also depicted in Fig. 2. The amplifier is a part of a regulation loop which controls the current of the pass transistor, M_P. This transistor serves to isolate V_{DD} from V_{ref} and, at the same time, to provide the required load current. In addition to the input differential stage (M_{i1}-M_{i4} and M_{Tail}), a push-pull stage (M_{o1}-M_{o5}) along with two compensation capacitors (C_{C1} and C_{C2}) have also been added to the topology of this amplifier.

If the combination of the opamp offset voltage and that of the CTAT generator (i.e. V_{OS}) is included into the analysis, combining (1), (3) and (4) results in the following expression for V_{ref}:

$$V_{ref} = \left(1 + \frac{R_2}{R_1}\right)\sqrt{\gamma}V_{TH} + \frac{R_2}{R_3}nV_T + \left(1 + \frac{R_2}{R_1}\right)V_{OS} \tag{5}$$

Based on condition (2), to gain a ZTC reference-voltage (V_{ZTC}) one should have

$$\frac{R_3}{R_1||R_2} = \frac{nk}{q}\frac{1}{\alpha\sqrt{\gamma}} \tag{6}$$

which will simplify (5) into

$$V_{ref} = V_{ZTC} = \left(1 + \frac{R_2}{R_1}\right)\sqrt{\gamma}(V_{TH}(T_0) + \alpha T_0 + V_{OS}) \tag{7}$$

If V_{OS} is assumed to be independent of temperature, then V_{ref} will be completely temperature-insensitive. In addition, while R_3 and γ can help to satisfy condition (6) for any reference value, the ratio R_2/R_1 adjusts the absolute value of buffered V_{ZTC} to be smaller, equal or larger than the silicon bandgap voltage. The threshold-referenced circuit of Fig. 2 can be optimised to meet an acceptable performance in terms of temperature linearity and process variation. As the line regulation might not be perfect in this case, the power supply of the threshold-referenced circuit can be made constant by supplying it from the regulated V_{ref}. As zero-current state is not a stable point for this unit, this does not cause any problem during the start-up. As a result, this technique has also been applied to improve performance.

To show that the proposed bandgap reference can be flexibly designed for a wide range of specifications, two reference-voltage circuits are designed and simulated in a 0.18 μm CMOS process. With a 10 pF and a 50 pF load capacitor and a 100 pF and a 130 pF total compensation capacitor, the 100 mA-1.3 V and 100 mA-0.9 V designs are able to operate at 1.5 and 1.1 V minimum line voltages, respectively. Fig. 3 shows the temperature variation of the 1.3 V reference voltage for minimum and maximum load currents. Both designs consume less than 50 μA of quiescent current. For $T = [-25°C, 85°C]$, the average temperature coefficients are about 25 ppm/°C and 36 ppm/°C for the 1.3 and 0.9 V references, respectively. The 0.1% settling errors for positive and negative 100 mA load current steps are, respectively, 1.67 and 1 μs for the 1.3 V design and 1.74 and 4.48 μs for the 0.9 V design.

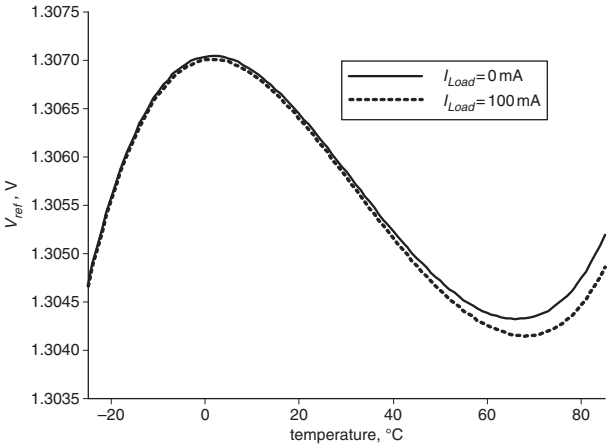

Fig. 3 *Simulated variation of reference voltage against temperature for 1.3 V design*

Conclusions: A new circuit architecture for buffered bandgap references with high current drive capability and low sensitivity against temperature variations is proposed. Simulations in all process/temperature corners as well as Monte-Carlo simulations in a 0.18 μm CMOS process show that the voltage reference circuit can provide up to 100 mA of load current while the temperature coefficient remains less than 37 ppm/°C in a wide range of temperatures.

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