

Guest Editors' Introduction: Opportunities and Challenges of 3D Integration

David S. Kung
IBM

Yuan Xie
Pennsylvania State University

■ **INTEREST IN 3D INTEGRATION** is being renewed as researchers are facing challenges from the complexities, and cost, of scaling to 22 nm and beyond. Innovative device structures such as finFET, and extremely thin fully depleted silicon-on-insulator (ETSOI), must be deployed to continue scaling. Even with those novel device structures, however, we can no longer achieve the performance gain we have been accustomed to without also incurring an unacceptable increase in power.

The cost of technology development in the nanoscale domain can run into the billions because massive lithographic retooling is required to cross the 22-nm barrier. The chip industry, therefore, is actively pursuing 3D integration as a viable alternative to provide density scaling. In addition, 3D IC technology allows more transistors to fit onto chips with a fixed-area form factor, and so makes possible an increasing set of diverse functions for portable devices such as smart phones and other PDAs.

3D IC technology offers chip architects unprecedented flexibility and options. Heterogeneous technologies such as RF, analog, and MEMS can be used for each layer, and designers can mix older and newer technologies to reduce cost. A more optimized chip-level architecture can be achieved by having more cores and special-purpose acceleration engines integrated into the chip. Reuse of existing hard-IP blocks and the known-good die strategy will allow a 3D stacked chip to be assembled at a lower cost and a reduced time to market than will a 2D chip implementation.

The possibility for integrating a memory stack with a computational layer significantly extends the memory capacity and bandwidth per computational core, and increases the proximity of the memory to the

computational cores. Such benefits from capacity, bandwidth, and proximity are fundamental for increasing the performance and reducing the power consumption of a manycore system. Intercore communication within a manycore chip is a major challenge because adding more narrow interconnects simply exacerbates the nonscaling behavior of wires. 3D IC technology offers relief by giving designers a way to provide an on-chip optical interconnect layer to connect the cores with one another.

All these advantages for 3D design will not be free: numerous challenges must be overcome before 3D integration will become mainstream. At the top of the list are thermal issues: innovative cooling techniques must be developed to ensure that the chip can operate at temperatures required for reliability and performance targets. With a small footprint and limited through-silicon via (TSV) densities, delivering adequate power to the transistors in every layer is difficult, especially if the vertical dimension begins to increase. Fluctuations in the temperature profile will aggravate power noise and lead to systematic variations. Researchers must develop thermal and power management schemes based on accurate analysis to mitigate these issues. New test strategies will also be required to handle the limited test access mechanisms and their fine probe pitch.

This special issue of *IEEE Design & Test* includes four articles on diverse topics that address some of these challenges. In the first article, "Opportunities and Challenges for 3D Systems and Their Design," Emma and Kursun describe the system design opportunities offered by 3D integration, and then discuss the design and test challenges for 3D ICs, with various new design-for-manufacture and DFT issues. The second article, "Optimizing Decoupling Capacitors in 3D

Circuits for Power Grid Integrity" by Sapatnekar et al. presents a design automation solution for power grid optimization using MIM and CMOS decoupling capacitors. The authors propose a congestion-aware 3D power supply network optimization algorithm to apply a sequence-of-linear-programs-based method to find the optimal trade-off between the two schemes.

The third article by Lee et al., "Test Challenges for 3D Integrated Circuits," focuses on testing issues. One of the potential obstacles to 3D technology adoption is the insufficient understanding of 3D testing issues and the lack of DFT solutions. This article describes testing challenges that include problems unique to 3D integration, and summarizes early research results in this area.

One of the potential early applications for 3D integration is memory stacking for multicore/manycore architecture, such that the massive parallel TSVs from memory to logic cores can provide a much higher memory bandwidth and therefore mitigate the "memory wall" challenges faced by future manycore design. In the fourth article, "3D DRAM Design and Application to 3D Multicore Systems," Sun et al. present a 3D DRAM architecture design and the potential for using 3D DRAM stacking for both L2 cache and main memory in a 3D multicore architecture. The experimental results from a full-system simulator demonstrate the performance advantage of such a heterogeneous 3D DRAM architecture over a wide spectrum of workloads.

WITH INTENSE RESEARCH ACTIVITIES from academia and industry ongoing, it is expected that most of these issues will eventually be resolved. However, the fate of 3D integration will ultimately depend on whether or not there are profitable and

widespread applications that can reap the benefits of 3D integration and whether or not the return on investment justifies its deployment. The next several years will be critical for the validation of 3D integration technology. It will be one of the highlights of this century if such a field of dreams becomes a reality. ■

David S. Kung is the senior manager of the Design Automation Department at the IBM T.J. Watson Research Center and is responsible for charting the future direction of design tools research for IBM. His research interests include logic and physical synthesis, and design methodology for high-performance microprocessors. He has a PhD in physics from Stanford University and is a Senior Member of the IEEE.

Yuan Xie is an associate professor in the Computer Science Engineering Department at Pennsylvania State University. His research interests include EDA, computer architecture, and VLSI design, with a focus on 3D integrated circuits. He has a PhD in electrical engineering from Princeton University. He was a recipient of the NSF CAREER award in 2006, IBM Faculty Award in 2008, and Best Paper Award in ASP-DAC 2008.

■ Direct questions and comments about this article to Yuan Xie, 354E IST Building, Pennsylvania State University, University Park, PA 16802; yuanxie@cse.psu.edu or to David S. Kung, Design Automation, 33-109A, IBM T.J. Watson Research Center, Yorktown Heights, NY 10598; kung@us.ibm.com.

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