

Tutorial T2B

Cost / Application / Time to Market Driven SoC Design and Manufacturing Strategy

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Abstract

Choosing the right strategy for SoC design is critical to have maximum business benefit out of the SoC. This tutorial looks at different factors, like cost, application of use, time to market, time in market etc, which can impact the SoC design life-cycle. These factors can affect several parameters like partitioning of SoC functionalities into hardware/software, selection of right hardware platform like FPGA/ structured ASIC/ ASIC/ASIP, selection of process node/ number of metal layers/ package etc. The business factors can even influence design parameters like power gating, multi Vt design, voltage island etc. It can also influence the design methodology like selection of IP, selection of the verification process and usage of high-level design exploration flow etc.

Speaker Biographies

Barun Kumar De is currently working as Senior Business Development Manager in SmartPlay Technologies. SmartPlay is second largest VLSI design Services Company in India with 450+ team of VLSI engineer. Barun is involved in IP business and turnkey SoC design services business in SmartPlay. Before that Barun has worked in companies like Wipro, SoftJin, Open-Silicon, Texas Instruments and Atrenta. He has done B.E. in electronics and telecommunication from Jadavpur University and MBA from IIM Calcutta.

Anupam Chattopadhyay received his B.E. degree from Jadavpur University, India in 2000. He received his MSc. from ALaRI, Switzerland and PhD from RWTH Aachen in 2002 and 2008 respectively. During his PhD, he worked on automatic RTL generation from the architecture description language LISA, which was commercialized later by CoWare (now part of Synopsys). He further developed several high-level optimizations and verification flow for embedded processors. In his doctoral thesis, he proposed a language-based modeling, exploration and implementation framework for partially re-configurable processors. He has published more than 40 technical papers, authored one book and several book-chapters in the above research areas.

Prof. Dr.-Ing. Chattopadhyay spent over 3 years in various engineering and research positions at industry. In his most recent industrial position he was serving as a Member of Consulting Staff at CoWare, India, where he was responsible for enhancing the quality and capability of a high-level processor synthesis toolsuite. Since 2010, Prof.

Dr.-Ing. Chattopadhyay is with RWTH Aachen University as an assistant professor in the UMIC research cluster. He is heading the research group of MPSoC Architectures.

Ansuman Banerjee is currently working as an Assistant Professor at the Advanced Computing and Microelectronics Unit, Indian Statistical Institute Kolkata. His research interests include design automation for embedded systems, hardware/software verification, CAD, and automata theory. Ansuman received his B.E. from Jadavpur University, and M.S. and Ph.D. degrees from the Indian Institute of Technology Kharagpur-- all in Computer Science. He spent about 6 months at the National University of Singapore as a research fellow working in software verification and about 4 years at Interra Systems India Pvt. Ltd. in various roles. Ansuman has published about 30 research articles in the area of formal verification over the past ten years of research as a student and as an industry practitioner.