A Low SIR Impulse-UWB Transceiver Utilizing Chirp FSK in 0.18 μm CMOS

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***Abstract*—An ultrawideband transceiver employing chirp pulse modulation is proposed for LDR communication. In contrast to the Gaussian pulse, a transmitted pulse modulated with different chirps can maximize the transmitted energy under low supply voltage and is thus amenable to the voltage scalability of the advanced CMOS technologies. The binary data is encoded with different chirp frequencies and two identical pulses are sent per data bit to enable non-coherent demodulation which simplifies the receiver architecture. A demodulation calibration loop is also incorporated to optimize the SIR performance. In-band/out-of-band SIR as low as -21 dB/-59 dB can be tolerated in order to achieve BER better than 10^{-3}. Implemented in 0.18 μm CMOS, the transceiver can sustain data rates up to 20 Mbps, and achieve energy efficiency of 0.77 nJ/bit for transmitting and 2.7 nJ/bit for receiving under 1.8 V supply.**

***Index Terms*—Chirp spread spectrum (CSS), CMOS, frequency-shift keying (FSK), non-coherent, signal to interference ratio (SIR), transceiver, ultrawideband (UWB).**

I. Introduction

In 2002, the Federal Communications Committee (FCC) opened up the frequency band from 3.1–10.6 GHz for ultra-wideband (UWB) communication, which has signal spectrum occupying more than 500 MHz bandwidth with an average power spectral density (PSD) limit of -41.3 dBm/MHz [1]. The large bandwidth coupled with low PSD can enable high data rate communication while allowing co-existence with other existing narrowband systems. Current UWB systems are mainly based on two schemes, i.e., orthogonal frequency-division multiplexing (OFDM) or impulse radio (IR). The former can achieve better spectral efficiency but increases the hardware complexity due to the extensive digital signal processing required. In addition, it forgoes the attractive features of accurate timing and radar since the large bandwidth is effectively sub-divided down to many small sub-bands [2]. On the other hand, IR-UWB offers simple transceiver architectures and its nanosecond pulse can provide accurate timing required for ranging or localization. However, the simplicity is often gained at the expense of flexibility in obtaining FCC mask compliant spectrum. For example, pulse repetition frequency (PRF), pulse width and pulse peak amplitude can be traded off to obtain the desired spectrum [3]. For low data rate (LDR) communication, this usually constrains UWB systems to the use of pulses with large peak amplitude and narrow width, which cannot be easily generated using advanced CMOS technologies under low supply voltage. Besides the two mentioned schemes, UWB systems employing continuous wave (CW) chirp modulation have also gained attention recently [2], [4].

Another major impediment to the proliferation of UWB systems is the performance degradation in the presence of strong interferers. For out-of-band interference, such as the 2.4–2.5 GHz and 5–6 GHz WLAN signals, circuit level approaches such as pre-filtering and frequency selective front-ends have been used to attenuate these interferers but at the cost of increased circuit complexity and higher power requirements [5], [6]. For in-band interference, such as other UWB or WIMAX signals, sub-banded IR-UWB [7], [8] with band-hopping has been proposed. Basically, multiple UWB sub-bands are allocated for transmission and the RX chain selects only the optimal sub-band with minimal in-band interference while disregarding the others. This approach suffers from poor spectral efficiency and proves sub-optimal in interference-free communication channels. Besides band-hopping, receiver processing gain can also be used to mitigate the in-band interference [9]. However, this requires the spreading of the desired signal energy evenly throughout the allocated spectrum.

In this work, we propose a transceiver that employs UWB pulses with chirp modulation. The use of chirp modulation within the transmitted pulse eliminates the pulse width and amplitude constraints faced by conventional IR-UWB. FCC mask compliant spectrum can be easily generated with wider pulse width and smaller peak amplitude, which makes the transceiver more amenable to advanced CMOS technologies. In addition, chirp modulation also allows a more even spread of the transmitted spectrum as compared to the conventional IR-UWB and improves the receiver processing gain. A demodulator calibration loop has also been proposed in this work to trade off the sensitivity with interference robustness. The interference robustness is achieved by excluding the portion of

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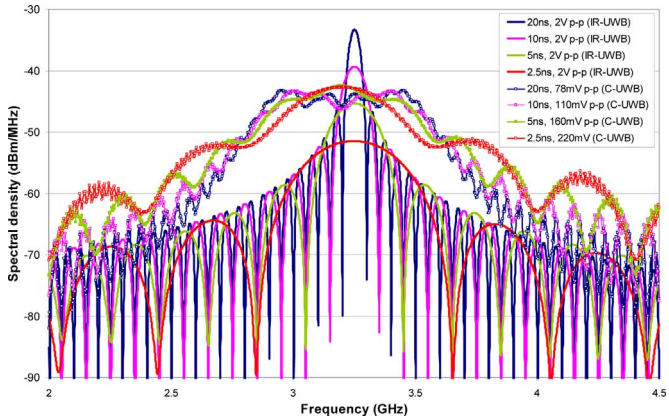

Fig. 1. PSD of chirped UWB (C-UWB) pulses and comparison with conventional IR-UWB (OOK modulation) using Gaussian pulses for varying pulse widths at a data rate of 4 MHz under 1 V supply.

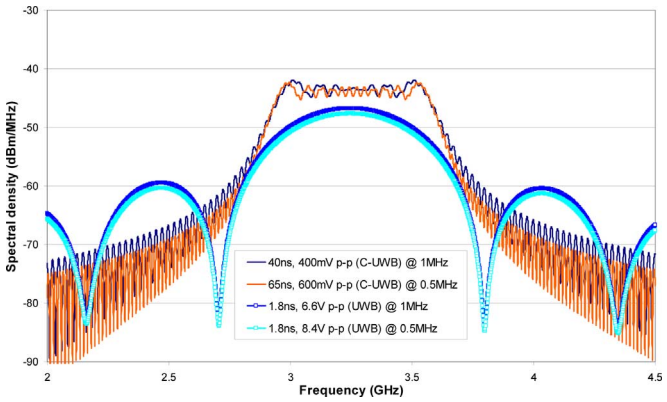

Fig. 2. Comparison of the PSD of the C-UWB and conventional IR-UWB pulse swings required to achieve comparable spectral coverage for LDR (1 MHz, 0.5 MHz).

the received spectrum corrupted by in-band interference during demodulation and thus lowering the sensitivity of the receiver.

This paper is organized as follows. Section II introduces the IR-UWB pulse with chirp modulation and explains the working principles of the proposed transceiver topology. Based on this topology, the required design specifications for the various blocks within the transceiver are defined in Section III. Sections IV and V provide the circuit level implementations as well as the measurement results for both the transmitter and receiver blocks respectively. Section VI describes the overall system measurement setup and results. Finally, the concluding remarks are given in Section VII.

II. System Overview

A. Chirped UWB Pulse

IR-UWB radios typically use high order Gaussian pulses that are scaled to fit the desired bandwidth by varying the pulse width and amplitude [3]. For LDR communication, this inevitably results in pulses with extremely narrow width (< 1 ns) and high peak swing (> 5 V). This is not scalable with more advanced CMOS technologies which are not amenable to large voltage swings due to lower supply. A chirp is a linear frequency modulated pulse and can be written in the time domain as

$$c(t) = A_c \sin[(\omega_0 + \beta \cdot t)t], \quad 0 \le t \le t_p \tag{1}$$

where ω_0 is the initial frequency of the chirp, β is the chirp rate and t_p is the duration of the chirp pulse. Unlike the conventional Gaussian pulse, chirp modulation allows the flexible trade off between the pulse amplitude and pulse width to achieve evenly spread spectrum across the 500 MHz bandwidth. Therefore, similar PSD can be realized with longer pulse width and lower peak amplitude. The proposed system can therefore be voltage scalable with the advanced CMOS technologies. Fig. 1 compares the PSD of a 500 MHz chirp with that of a typical Gaussian pulse for various t_p under a conservative 1 V supply voltage, i.e., the differential p-p swing is constrained to 2 V. We can clearly observe that in order to transmit near the FCC mask level without overshoot at 4 MHz data rate, the Gaussian pulse would require $t_p \sim 5$ ns but its bandwidth would drop to about 150 MHz. On the other hand, in order to meet the 500 MHz bandwidth constrains, $t_p \sim 2$ ns is required which results in a very drastic drop in the transmission power. In comparison, the C-UWB pulse optimally utilizes the available spectrum for all t_p and as a result is able to transmit significantly more power per symbol and hence is capable of much larger transmission range. In addition, the evenly spread spectrum with sharp roll-off at the band edges also improves the receiver processing gain which can help mitigate in-band interference [9].

The superiority of our scheme in LDR cases is further highlighted in Fig. 2. At data rates of 1 MHz and 500 kHz, the C-UWB pulses can be lengthened (40 ns, 65 ns) while restricting the swing requirement to 600 mV p-p at most. However, to achieve a comparable PSD, a Gaussian pulse would require much larger voltage swings in excess of 6.6 V p-p. This limitation makes Gaussian pulses not scalable to advanced technologies for LDR applications.

B. Proposed Transceiver

The proposed transceiver is shown in Fig. 3. Binary data "1" and "0" are encoded with different chirp frequencies which occupy frequency band B1 (3.15–3.55 GHz) and B2 (3.45–3.9 GHz) respectively. The overlapped spectral region (3.45–3.55 GHz) contains less than 2.5% of the overall band energies due to sharp spectral roll-off and hence loss of sensitivity due to inter symbol interference (ISI) is insignificant. Burst mode operation is employed in the transmitter through a low duty cycle clock (TX_clk) which activates the TX blocks only during the pulse generation period to achieve power savings. The on period of TX_clk, t_{on}, which directly controls the transmitted pulse width, t_p, is made programmable. To simplify the receiver architecture with non-coherent demodulation, two identical pulses are sent consecutively per data bit. Therefore TX_clk is operated at twice the data rate (DR). The chirp control generator (CCG) and chirp pulse generator (CPG) blocks are calibrated manually from baseband so as to maintain a relatively linear chirp range

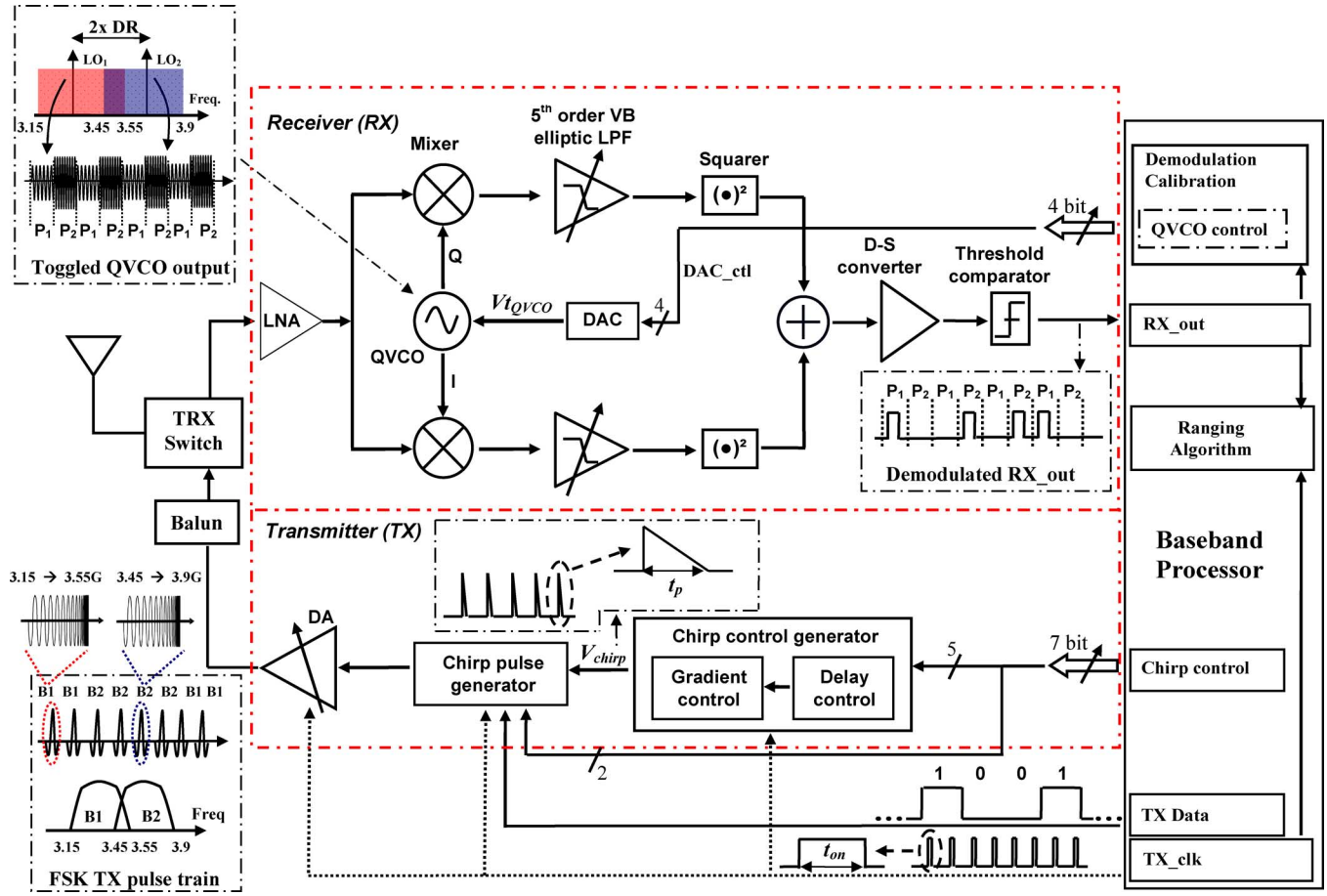

Fig. 3. System architecture.

and maximize spectrum utilization regardless of the pulse width.

In the receiver chain, the received pulse is first amplified by a wideband low noise amplifier (LNA) and then down-converted using a toggled quadrature voltage controlled oscillator (QVCO). The QVCO toggles between two tones (LO_1 and LO_2) alternatively with each tone occupying half of the data period (P1 and P2). The large signal bandwidth (~ 400 MHz) relaxes the synthesizer precision requirement and obviates the need for a phase locked loop (PLL). The toggling of the QVCO is achieved with a 4-bit DAC. As the binary data are encoded as different frequency bands, only the right LO tones will down-shift the signal to the baseband for correct demodulation. As an example, when "1" is transmitted, only LO_1 will down-shift the desired signal correctly which will result in energy detection during P1 and no energy detection during P2. By comparing the output energy in intervals P1 and P2, the transmitted data can then be recovered [8]. A programmable low-pass filter (LPF) followed by squarer is employed after the mixer to perform energy detection.

As the LO frequency determines the down-shifted band, it can be adjusted to either optimize the receiver sensitivity or improve interference robustness. A demodulation calibration loop (DCL) is therefore incorporated to fine tune the LO frequency depending on the objective. Its structure and implementation will be discussed in Section V.

III. Transceiver Specifications

A. Transmitter

As mentioned, the proposed scheme is attractive because it enables the use of wider and low-swing pulses. However, the duration of the pulses, together with the temporal spreading due to filtering creates an upper bound for the possible data rate in order to avoid ISI. In order to achieve flat PSD and concurrently exploit the power savings from the duty-cycling in the TX, minimum and maximum pulse widths of 2 ns and 15 ns were deemed appropriate from simulation for a maximum target data rate of 20 Mbps. This results in peak swing amplitude ranging from 0.22 V to 0.08 V in order to meet the FCC mask requirement. By optimally utilizing the frequency allocation under the mask we can maximize the total transmission power and can consequently target larger transmission distance (> 10 m) as compared to traditional IR-UWB.

It is essential to ensure that the chirp frequency varies linearly with time over the pulse duration in order to ensure the flatness of the transmitted PSD. Using the frequency chirp pulse described in (1) and assuming that LC VCO is employed, the following capacitance relation can be determined:

$$\omega_{TX\_chirp} = \omega_0 + \beta t = \frac{1}{\sqrt{L(C_o + C_{delta})}} \quad , 0 \le t \le t_p \tag{2}$$

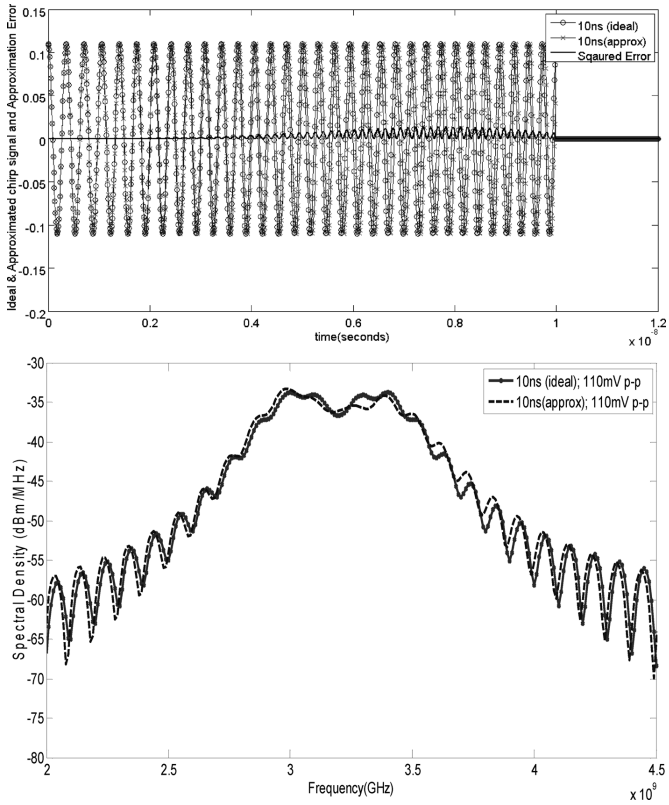

Fig. 4. Time and frequency domain representations of the ideal and approximated chirp for $t_p = 10$ ns and $\mathrm{PRF} = 8$ MHz.

where ω_0 is the initial frequency of the chirp, C_0 is the fixed capacitance that generates ω_0, and C_{delta} is the variable capacitance that gives rise to the chirp over the desired range. It should be noted that a linear up-chirp is assumed in (2). As the chirp frequency (~ 400 MHz) is much smaller than the ω_0 (~ 3 GHz), (2) can be further simplified to

$$\Rightarrow \quad C_0 + C_{delta} = \frac{1}{L(\omega_0 + \beta t)^2} = \frac{C_0}{\left(1 + \frac{\beta t}{\omega_0}\right)^2} \approx C_0\left(1 - \frac{2\beta' t}{\omega_0}\right) \quad , 0 \le t \le t_p. \quad (3)$$

Equation (3) shows that the total tank capacitance should be linearly decreasing with time in order to obtain the linear up-chirp. It should be noted that in order to compensate for the inherent underestimation in (3) due to approximation, β' is chosen to be smaller than the ideal β and varies from 195 MHz/ns to 20.25 MHz/ns for $2 \text{ ns} < t_p < 15$ ns. It can be seen from Fig. 4 that with this adjustment, the mean squared error of the approximated PSD is less than 2.9% which is negligible in our application.

B. Receiver

Interference mitigation is key to successful co-existence of UWB with existing wireless technologies like 802.11 WLAN, Bluetooth, GSM etc. Pre-select filter is commonly employed prior to the LNA to eliminate the out-of-band interference. However, on-chip filters tend to worsen the system noise figure while the off-chip solution increases the cost [10]. In this implementation, an LNA with dual gain mode is utilized whereby the low gain mode is selected when there is a strong out-of-band interferer in close proximity.

1) Sensitivity and Linearity: The sensitivity equations for IR-UWB receiver is given as follows:

$$Sensitivity = P_{RS}|_{\mathrm{dBm/Hz}} + NF|_{\mathrm{dB}} + SNR_{\min}|_{\mathrm{dB}} + 10\log(B) + 10\log(F_{duty}) \quad (4)$$

where P_{RS} is the noise power that source resistance (R_{S}) delivers to the receiver, *NF* is the noise figure of the receiver, *SNR* is the desired signal-to-noise ratio to achieve the target bit error rate (BER), B is the total signal bandwidth, and F_{duty} is the ratio of pulse width to the total bit period. It should be pointed out that last term is added to (4) to accurately reflect the true noise floor as the recovered signal is only compared with the noise during the pulse width. Assuming a 5 dB SNR for acceptable BER, 7 dB system noise figure in high gain mode, pulse width of 10 ns at data rate of 4 Mbps and a 500 MHz signal bandwidth, the achievable sensitivity of the system is -86 dBm.

Although the in-band interferer can be mitigated to a certain extent by employing the DCL, the overall interference robustness which includes both in-band and out-of-band interferers still very much depends on the linearity of the receiver front-end. Assuming strong out-of-band interference from both an ISM band device (2.4 GHz) and a WCDMA device (1.7 GHz) with transmission power $+20$ dBm at proximity of 1 meter, the resulting interference power level at the receiver would be -17 dBm assuming normal free space path loss. Due to the nonlinearity of the LNA, both front-end desensitization and/or intermodulation products that fall within the desired signal band can reduce the SNR. To avoid desensitization, the LNA needs to have 1 dB compression point that is larger than -17 dBm. The band-pass filtering provided by both antenna and LNA will further relax the 1 dB compression point requirement. To mitigate inter-modulation products, the desired *IIP3* of the LNA can be derived as follows [11]:

$$SDR = 20\log\left(\frac{A_{sig,out}}{A_{IM3,out}}\right) = P_{sig,in}|_{\mathrm{dBm}} + 2 \times IIP3|_{\mathrm{dBm}} - 3 \times P_{Interferer,in}|_{\mathrm{dBm}} \quad (5)$$

where *SDR* is the signal to distortion ratio, $A_{sig,out}$ and $A_{IM3,out}$ are the amplitude of desired output signal and inter-modulation product respectively, $P_{sig,in}$ and $P_{Interferer,in}$ are the input signal power and interferer power in dBm respectively. Since the baseband typically can have large processing gain through coding (> 10 dB), desired *SDR* of 5 dB [16] is assumed. With $P_{sig,in}$ at the sensitivity level and out-of-band suppression of 20 dB provided by the band-pass characteristics of antenna as well as LNA, this will result in *IIP3* requirement of -10 dBm.

Since LNA and antenna gain roll-off will not suppress in-band interference and may not sufficiently suppress strong out-of-band interferers, the LNA gain must be lowered in order to avoid compression in these cases. Assuming a 10 dB drop in

gain, the NF of the LNA is expected to deteriorate by about 3.5 dB and hence a system NF of -10.5 dB is targeted. Assuming the case of a 3.5 GHz WiMax interferer, aggressive baseband filtering will be required which will reduce the effective received signal power by about 4 dB. Hence, the target sensitivity of the system is moderated to -78.5 dBm in the presence of strong interferers. Targeting a SIR of -40 dB at 3.5 GHz, the tolerable interference power would be -38.5 dBm and we can recalculate the *IIP3* requirement from (5) as -16 dBm.

2) LO Generation: The quadrature direct down-conversion architecture significantly relaxes the phase noise and frequency drift specifications for the local oscillator. Simulations show that due to the wide 500 MHz signal bandwidth, the allowable $LO_{1,2}$ deviation from the center frequency without significant loss ($>$ 3 dB) in sensitivity is up to ± 50 MHZ. A free-running tunable LC tank QVCO is employed to generate the desired LO tones, where a DAC is used to vary the voltage controlling the frequency. The feasibility of using an open loop QVCO has been previously shown in [23] which also targets a comparable frequency variation tolerance of roughly 100 MHz. In addition, [23] employs ring oscillator and should suffer more severe PVT issues compared to our LC oscillator. This approach eliminates the need for a PLL thereby saving power and complexity, and also avoids synthesizer spurs. This prevents the folding of undesired adjacent signals into baseband through mixing with the synthesizer spurs and hence avoids the resulting reduction in sensitivity [10], [12].

3) Baseband Filtering: As mentioned earlier, LO frequency determines the down-shift of the signal band and can be adjusted to place the in-band interference out of the passband of the baseband LPF. Therefore bandwidth and roll-off of the LPF define the amount of interference suppression as well as the receiver sensitivity. As an example, we consider the scenario of an in-band WiMax (3.5 GHz) interferer. By adjusting LO_1 to the sub-optimal frequency of 3.3 GHz (50 MHz from the center), the interferer is down-converted to 200 MHz. With the input signal power at the sensitivity level of -78.5 dBm (under strong interference) and again assuming an interference level of -38.5 dBm, if we employ a filter with 3 dB cutoff at 75 MHz, stop-band attenuation of 45 dB is required. On the other hand, if there is no interferer present, LO_1 should be adjusted to the desired center frequency of 3.35 GHz and the LPF cutoff should be extended to the full signal bandwidth to maximize the received signal energy for better demodulation. Therefore the bandwidth of the LPF is made programmable from 75 MHz to 245 MHz. This allows the trade-off between sensitivity and interference mitigation. It should be pointed out that the filter bandwidth should be adjusted according to the $LO_{1,2}$ tone frequencies.

IV. Transmitter Implementation

The transmitter circuits and the corresponding timing diagram for chirp generation are shown in Figs. 5 and 6 respectively. The pulse generator (PG) is a differential LC VCO. Chirp modulation for different binary data (B1:3.15~3.55 GHz, B2:3.45~3.9 GHz) is obtained by varying the total PG tank capacitance, C_{tank}. C_{tank} consists of a bank of fixed capacitors (C_{bank}) switched directly by the TX data and 2 accumulation mode varactors, $C_{var1,2}$ controlled by the chirp control generator (CCG) output, V_{chirp}. The switching of C_{bank} encodes the TX data as bit "1" or "0" by toggling between two different UWB sub-bands, B1 and B2.

Since the PG requires a finite start-up time (t_{su}) during each duty-cycle excitation, V_{chirp} must be delayed correspondingly. The rising edge of TX_clk is delayed through a current starved inverter with adjustable pull-down current (I_{PDN}) to generate clk_del. The finest delay accuracy available is 0.24 ns which is sufficient for $t_p > 2$ ns. This accuracy can be increased as desired by increasing the number of control bits for I_{PDN}. The clk_del then triggers the discharge of C_{load} to generate the delayed V_{chirp}. It should be noted that C_{load} is initially charged to Vdd when TX_clk is low and the discharging current (I_{dis}) is made programmable through binary weighted current sources ($\mathrm{N_{PD1-3}}$). As the varactor's capacitance varies approximately linearly with the control voltage (V_{chirp}), for linear sweeping of the oscillator frequency during pulse generation, V_{chirp} has to observe a linear relationship with time. The discharging transient that is responsible for generating V_{chirp} can be described as (6), shown at the bottom of the page, where V_{TH} is the threshold voltage of the transistors ($\mathrm{N_{PD1-3}}$), R_{NPD} is the equivalent resistance of the transistors ($\mathrm{N_{PD1-3}}$) in linear region, and $T_0 = V_{TH}C_{load}/I_{ds}$ is the time instant when the transistors switch operating region. The discharging transient goes through two different phases as described by (6) due to the different operating regions of the transistors ($\mathrm{N_{PD1-3}}$). When the transistors are in saturation region, they behave like a constant current source (I_{dis}), and C_{load} discharges linearly with time. Once V_{chirp} falls below a certain value, the transistors go into linear region and behave like a switch resistance (R_{NPD}). C_{load} will now discharge exponentially with time. If the pulse duration is smaller than the RC time constant, the exponential relationship can be approximated as a linear relationship as shown in (6). The nominal I_{dis} that correctly models a 10 ns pulse with $C_{load} = 10$ pF is simulated to be 1.73 mA. Across expected temperature corners the variation in I_{dis} was simulated to be $+5\%$ to -9%. As (3) and (6) both observe linear relationships with time, transistors ($N_{\mathrm{PD1-3}}$) can be switched on/off to modify I_{dis} and R_{NPD} or C_{load} can be changed so that (6)

$$V_{chirp} = \begin{cases} Vdd - \frac{I_{dis}t}{C_{load}} & V_{chirp} > Vdd - V_{TH} \\ (Vdd - V_{TH})\, e^{-(t-T_0)/R_{NPD}C_{load}} \approx (Vdd - V_{TH})\left(1 - \frac{t-T_0}{R_{NPD}C_{load}}\right) & V_{chirp} < Vdd - V_{TH} \end{cases} \quad (6)$$

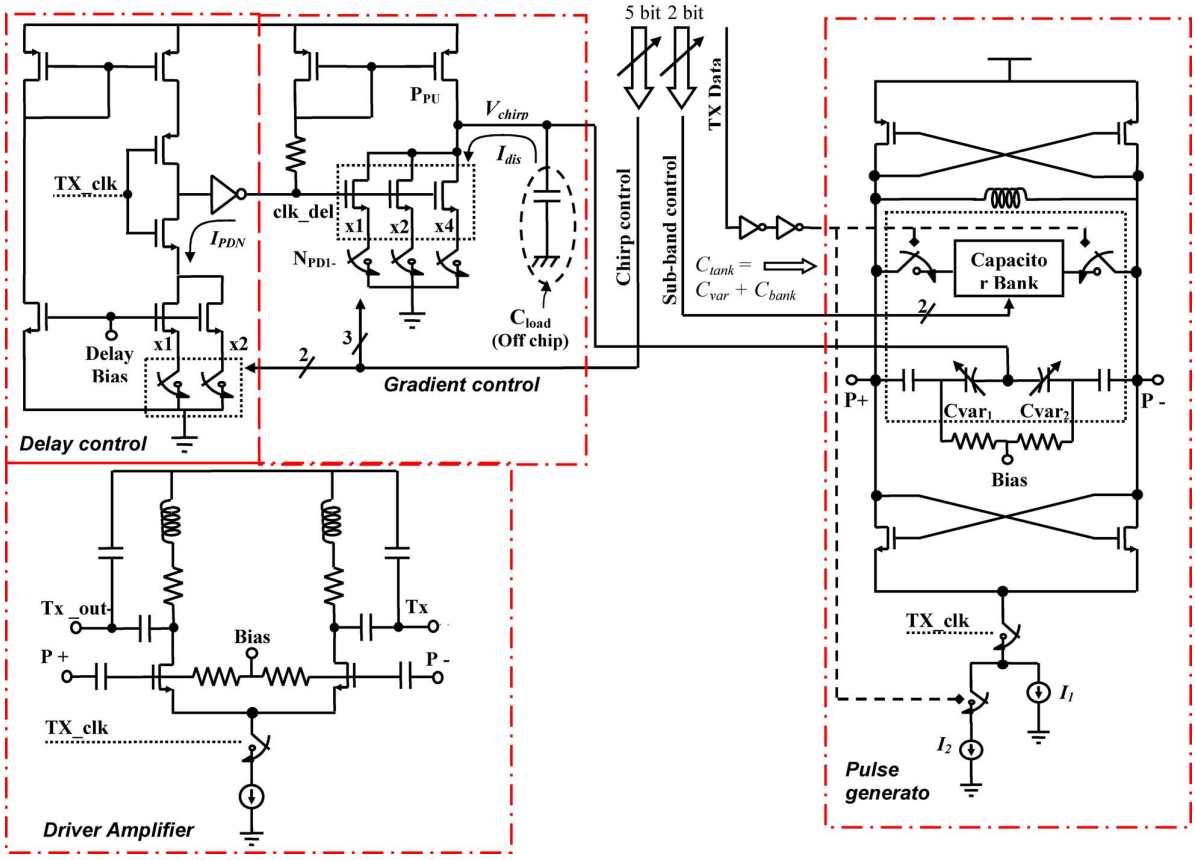

Fig. 5. Transmitter circuits.

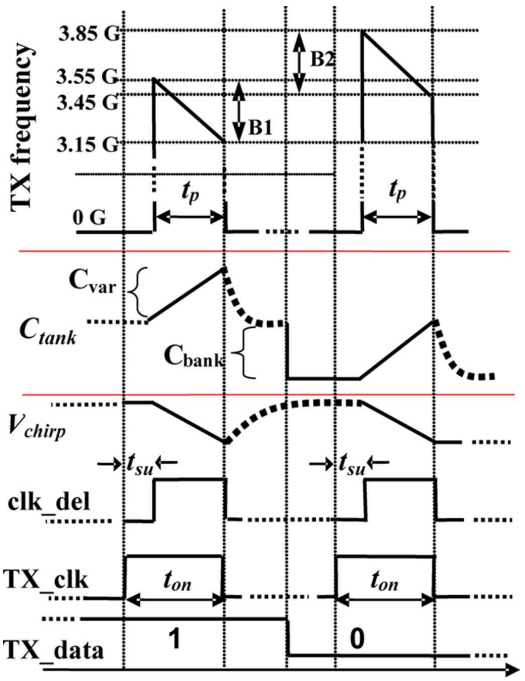

Fig. 6. Transmitter timing diagram for chirp pulse generation.

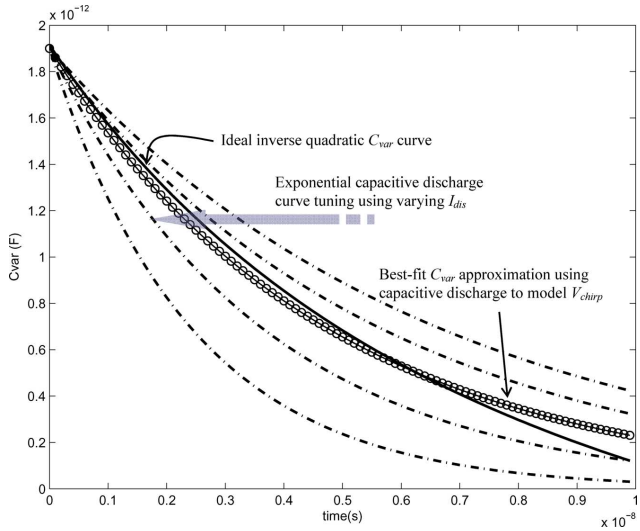

Fig. 7. Approximation of ideal inverse quadratic decay for C_{var} using exponential capacitive discharge to obtain a linear-in-time 10 ns chirp.

exhibits similar gradient as (3) for all t_p. In order to dynamically tune the discharge rate across PVT, V_{chirp} can be compared with a comparator threshold (for instance 0.2 Vdd) at the end of the discharge time. I_{dis} would need to be increased/ decreased if V_{chirp} is higher/ lower than the threshold in order to maintain a constant chirp range. Simple bang-bang control can be employed to adjust I_{dis} by switching NPD_{1-3} based on the comparator output. The simulated capacitance and theoretical estimated capacitance using (3) are compared in Fig. 7, which shows the feasibility of adjusting $\mathrm{N}_{\mathrm{PD1-3}}$ to achieve close resemblance between the simulated capacitance and the theoretical calculation. It should be noted that Fig. 7 shows that both the

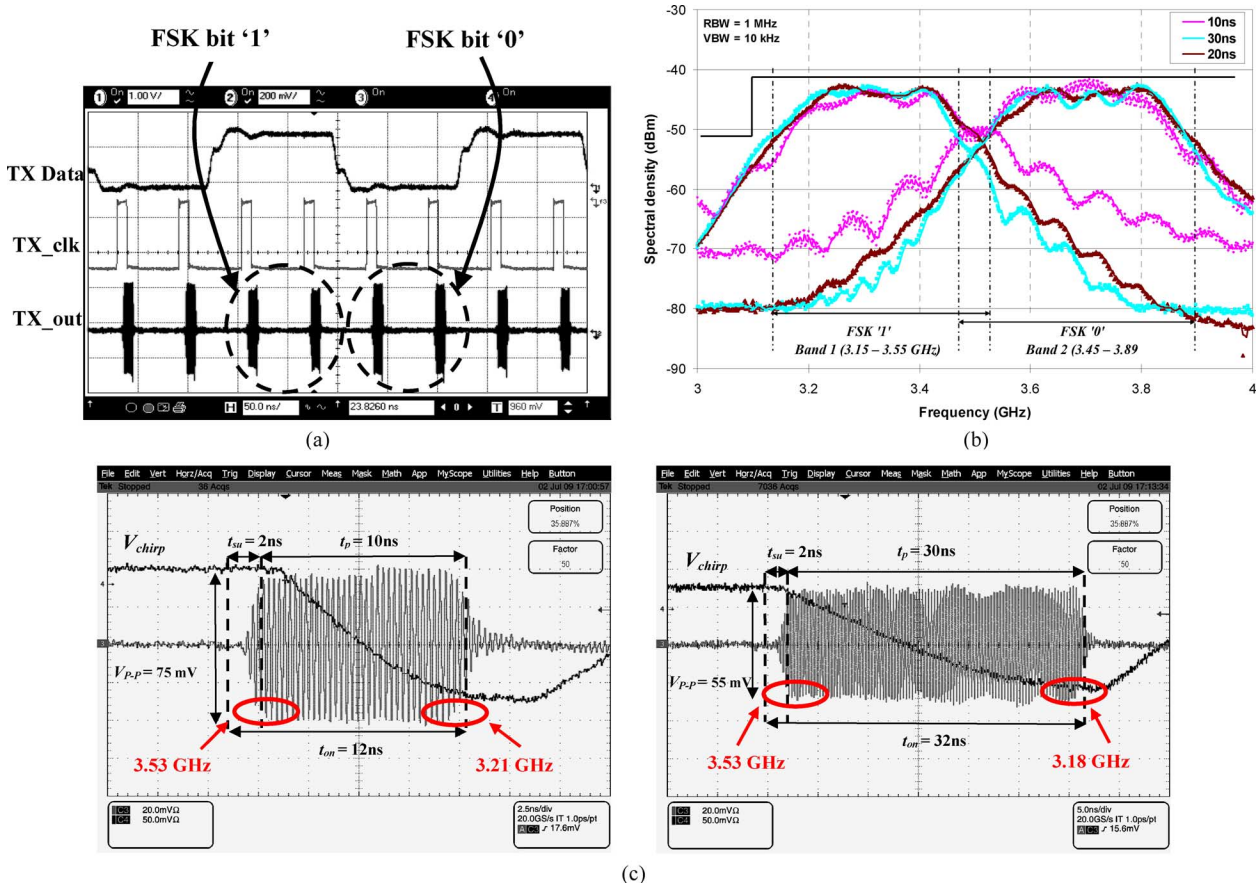

Fig. 8. (a) Measured FSK modulated TX pulse train (b) FSK sub-band spectra for varying pulse width, $t_p = 10$ ns to 30 ns @ 8 MHz data rate and (c) Corresponding band 1 pulses and V_{chirp} shaping for $t_p = 10$ ns and 30 ns.

curves are inherently non-linear and hence the estimates of (3) and (6) are not strictly accurate. However, since the curves are both convex, albeit varying in the degree of convexity, (3) and (6) have similar estimation errors and can still be used as an effective means of comparison. In actual implementation, V_{chirp} is applied to the source/drain nodes of the varactors to eliminate the effect of voltage dependent junction capacitance presented by the substrate(p)-nwell(n) diode. Although this will result in down-chirp rather than up-chirp, the preceding discussion on UWB pulse with chirp modulation remains valid.

In order to maintain an equal chirping range ($\sim$ 400 MHz) and power level for both sub-bands (B1 and B2), the oscillator start-up time (t_{su}) has to be kept constant regardless of whether bit "1" or "0" has been transmitted. However, as the center frequency is different, the quality factor of the LC tank would differ slightly. This will result in the parallel tank resistance and consequently t_{su} to be slightly different. To compensate for this, an additional current ($I_2 \approx 8.3$ mA) is switched on and off in tandem with the transmitted bit. This modifies the trans-conductance of the cross-coupled pair to compensate for the slight change in the tank resistance resulting in similar oscillation amplitude and t_{su} for both data bits. With the introduction of I_2, the startup times for B1 and B2 vary in tandem from 0.72 – 2.81 ns and 0.7 – 2.5 ns respectively across PVT. A key benefit of C-UWB is that since the chirp range is independent of pulse width, as long as the relative delay between the B1 and B2 pulses is minimal (< 0.31 ns in our implementation), no dynamic calibration is required for I_2 to compensate for PVT variations.

A simple differential tuned amplifier is adopted as the driver amplifier (DA) for the 50 Ω antenna load. The passive RLC network also serves as a wideband matching network to impedance-match the differential antenna. It provides a tunable voltage gain of -25 to $+8$ dB and is linear up to an output power level of $+2$ dBm for both B1 and B2 sub-bands in simulation. As pointed out in [3], FCC mask compliance necessitates that peak amplitude and data rate follow an inverse relationship. The 33 dB gain range of the DA enables it to accommodate data rate spanning more than 2 decades. The DA gain is set so as to meet the UWB spectral mask and is manually calibrated off-line by monitoring the output PSD of pulses. The instantaneous current drawn by the DA at the typical gain of $+2$ dB is 22.3 mA. In such low-gain application, even though the current drawn varies by about $\pm 6\%$, the DA gain changes by less than 1 dB. Due to the relative gain stability, no dynamic gain regulation mechanism was required.

The measured chirp modulated IR-UWB pulse train ($t_p = 10$ ns and $PRF = 8$ Mbps) and its PSD with varying pulse width are shown in Fig. 8(a) and (b) respectively. The corresponding V_{chirp} control voltage and chirp modulated pulse for B1 sub-band with various pulse widths is also illustrated in Fig. 8(c). As shown, the transmitter can achieve evenly spread PSD regardless of the pulse width in contrast to the conven-

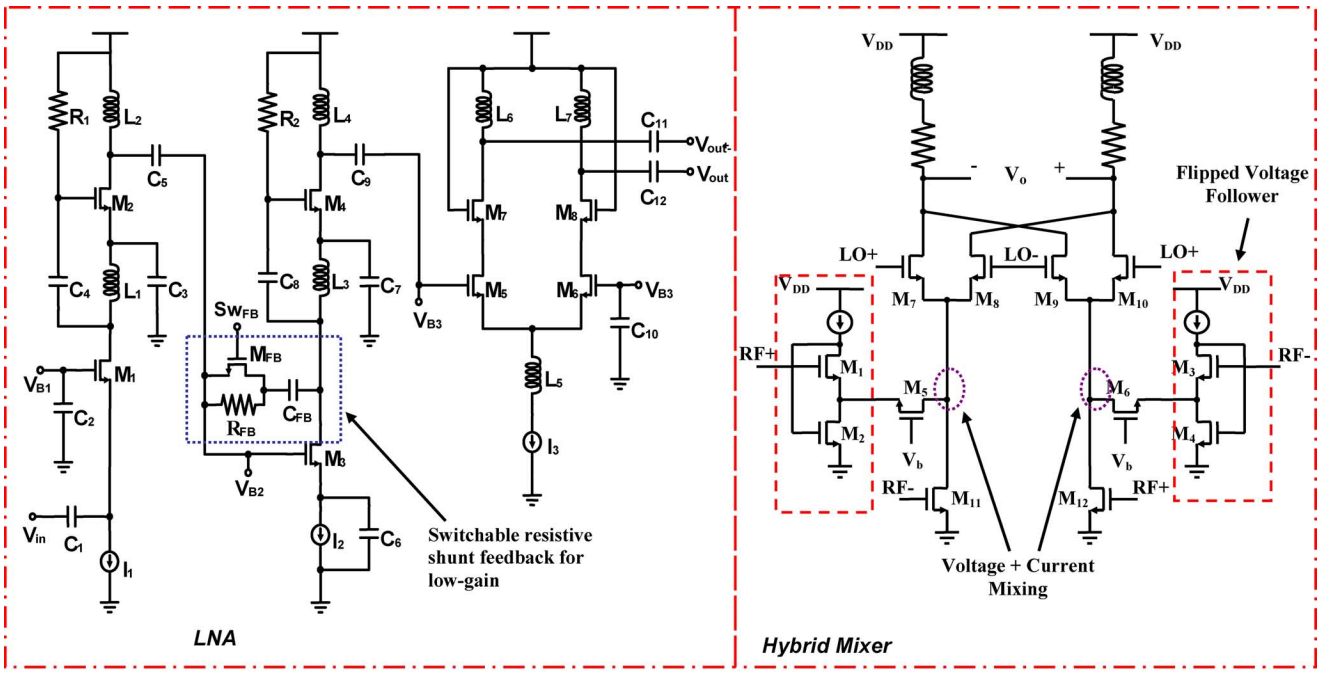

Fig. 9. Receiver front-end circuits: (a) LNA and (b) Mixer.

tional IR-UWB pulse. In addition, the required output amplitude is much smaller compared to [3] and [13] for similar data rates. The transmitter consumes 14 mW at *PRF* of 20 Mbps. The power hungry pulse generator (CPG) and DA blocks of the transmitter consume average instantaneous currents of 17 mA and 22.3 mA respectively and even after duty-cycling dominate the Tx power consumption because the Delay and Gradient control blocks consume less than 100 μA in total. Hence the transmitter energy efficiency is dependent mainly on the pulse length and data rate. In order to deliver maximum power in the LDR case, longer pulses need to be generated which means that even though the overall power consumption will be proportionately lower, the $\mathrm{E/b}$ will eventually deteriorate for very low data rates since the CPG and DA blocks will have to be switched on for longer per pulse. However as discussed in Section II.A, unlike conventional IR-UWB, the lower swing requirements would enable this architecture to be scaled to operate with lower supplies at advanced technology nodes, which would lower $\mathrm{E/b}$ without compromising transmission range. This represents a significant and unique advantage especially in the LDR domain.

V. Receiver Implementation

A. RF Front-End

The LNA needs to provide sufficiently high front end gain to counteract the subsequent attenuation incurred in the later filtering and squaring stages [8]. As shown in Fig. 9(a), the LNA circuit consists of 5 gain stages in total to achieve broadband gain and matching characteristics. Current reuse technique is employed for the first 4 single-ended gain stages. For wideband matching and noise figure considerations, single-ended common gate amplifier is used as the input stage. A differential amplifier stage is used to provide both the gain and the

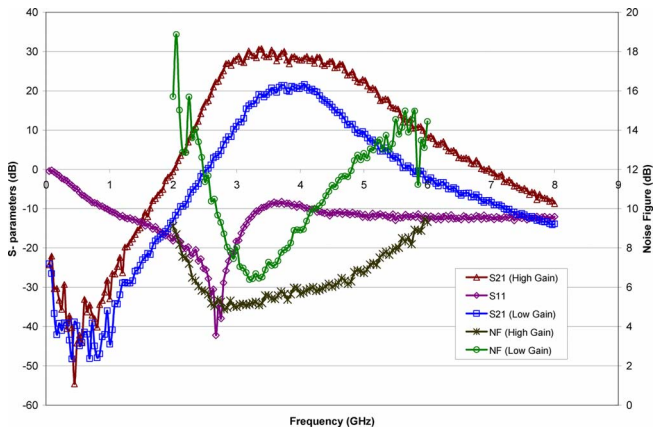

Fig. 10. Measured LNA S-parameters and noise figure.

single-to-differential conversion, which helps to improve the system IP2. To mitigate interference, two gain settings have been implemented in the LNA to trade off the receiver linearity with gain. The low gain mode can be achieved by turning on the transistor $\mathrm{M_{FB}}$, thus bypassing the feedback resistance $\mathrm{R_{FB}}$ employed in the 3rd stage shunt feedback amplifier. This will lower the overall impedance at the output of 2nd stage and reduce the gain. The measured on-wafer LNA S-parameters and the associated NF in both gain modes are shown in Fig. 10. In-band power gain of 27 dB and 18 dB is achieved in high gain and low gain mode respectively. The noise of the 3rd/4th stage and balun gets referred to the input. Since the first two stages of LNA do not supply too much gain, the referred noise causes the NF to deteriorate in the low-gain state. The impedance matching is not very good in the 3.3 – 4 GHz range which can be improved further by fine tuning the $\mathrm{g_m}$ of the input stages. Changing the

gain by tuning the 3rd stage modifies the tuning load at the output of the 2nd stage LNA and results in narrower band-pass characteristic in low gain mode.

Other gain switching techniques such as varying transistor transconductance (gate voltage bias or transistor sizing) [17], [18] , current steering [19] and resistive shunt feedback [20], were also explored. The first technique offers the advantage of simplicity but requires a finely controlled voltage bias to be able to achieve desired gain. Moreover, transistor size switching (with fixed gate bias) requires a compromise between gain and power consumption. Similar to the resistive shunt feedback approach, the current steering technique provides the advantage of fixed power consumption in different gain modes. However, the shunt feedback approach improves the wideband response of the amplifier and more importantly the stability in a high-gain amplifier [20]. We thus found that the proposed current re-use, multistage LNA with resistive shunt feedback gain tuning offered the best compromise between high gain, wide bandwidth, low power consumption and ease of gain switching implementation.

Fig. 9(b) shows a double balanced mixer combining the Gilbert cell and gate-source injection architectures that is used in I/Q path. This hybrid structure of employing both voltage and current mixing helps to improve the conversion gain and bandwidth [12]. The trans-conductor M11-M12 provides the current mixing whereas the flipped voltage followers (FVF) formed by M1-M4 achieves voltage mixing. The voltage gain of the FVF is the major source of gain variability and is relatively constant at around 0.83 as long as we ensure that the transistors M1-M4 are in saturation. This means that the gate bias voltages of M1 and M3 need to be in the range of roughly 0.6 V – 0.95 V. The size of transistors M7-M10 is chosen as a compromise between abrupt switching and maintaining output bandwidth larger than 250 MHz. Noise and linearity improvements are also achieved by lowering the tail current with appropriate gate bias to M11-M12. Linearity considerations demand a low overall conversion gain because of the very high gain of the preceding LNA stage. In order to ensure that M11, M12 remain in saturation and that the tail current to the Gilbert cell remains small, a gate bias voltage in the range of 0.7 V – 0.95 V is required so as to ensure that the mixer is linear up to an input level of 15 mV $\pm$ 5%. By employing replica bias, we easily achieve a bias voltage accuracy of better than 2% across PVT and hence ensure that the gain and linearity of the mixer remain effectively constant.

LC QVCO shown in Fig. 11(b) is used to generate the I and Q path LO tones. The symmetric coupling between the two oscillators through cascode connection as well as complementary cross-coupled pairs helps improve the phase noise performance [14]. A 4 bit R-2R DAC, shown in Fig. 11(a), is used to tune the varactor and thus the LO frequency (f_{osc}). Hence, 16 distinct $LO_{1,2}$ tones spanning the UWB band (3.3 – 4.2 GHz) can be generated with $\mathrm{K_{VCO}}$ of around 600 MHz/ V as shown in the tuning curves in Fig. 12. It can also be seen that the maximum frequency variation across the entire tuning range is within the 50 MHz tolerance over all PVT corners. The DAC resistors and switch resistances need to be minimized to reduce the charging time for fast frequency hopping. The DAC output

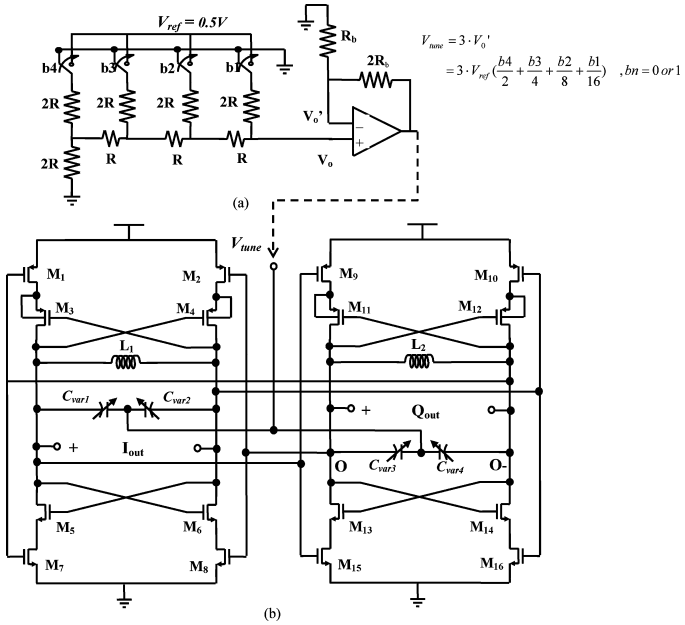

Fig. 11. (a) R-2R DAC and (b) QVCO circuit.

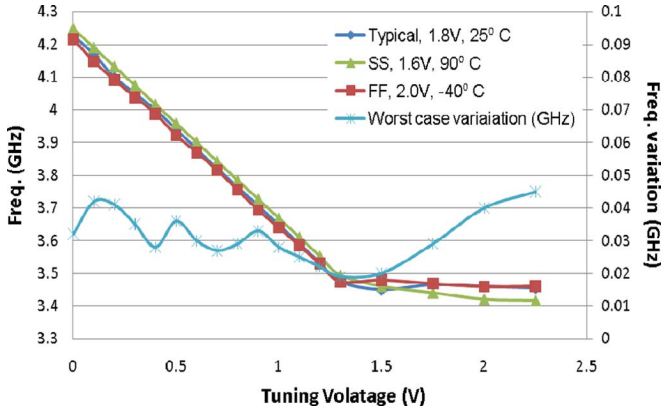

Fig. 12. Simulated QVCO tuning curve at circuit corners.

goes through a non-inverting op-amp buffer before driving the varactor. As the demodulation of the transmitted data relies on the switching between LO_1 and LO_2, the DAC settling behavior ultimately determines the maximum achievable data rate. The worst settling scenario occurs when the frequency is switched between maximum LO_2 (DAC = 4b′0000) to minimum LO_1 (DAC = 4b′1111) as shown in Fig. 13. The larger capacitance to achieve lower LO_1 slows down the settling to 17.5 ns while the reverse switching (LO_1 to LO_2) only takes about 4.5 ns. Taking the total settling time of 22 ns into consideration, maximum data rate of 18.2 Mbps can be achieved for pulse width of 10 ns. It should be noted that the frequency difference between LO_1 and LO_2 would be smaller in actual implementation ($<$ 600 MHz), resulting in faster settling and higher maximum achievable data rate. To ensure correct demodulation, the down-mixing of the incoming pulse by $LO_{1,2}$ should only occur after $LO_{1,2}$ has settled. This is ensured by skewing the RX and TX system clocks manually during the measurement. If automatic calibration is required, the down-shifted signal energy can be monitored to skew the RX clock with respect to the TX clock

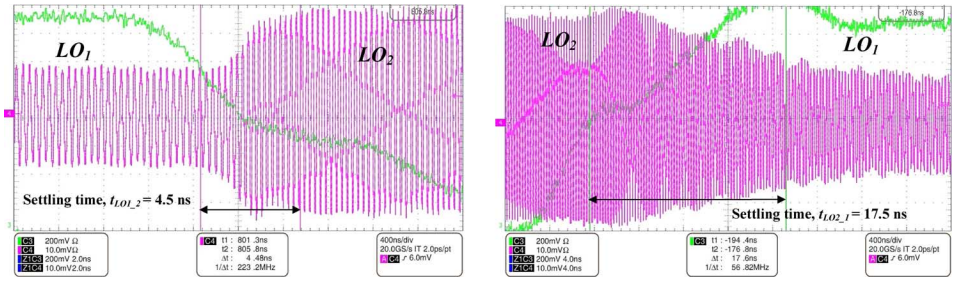

Fig. 13. Single-ended QVCO output (Active probe attenuation $= 10\times$) switching between $LO_1 = 3.42$ GHz and $LO_2 = 4.2$ GHz.

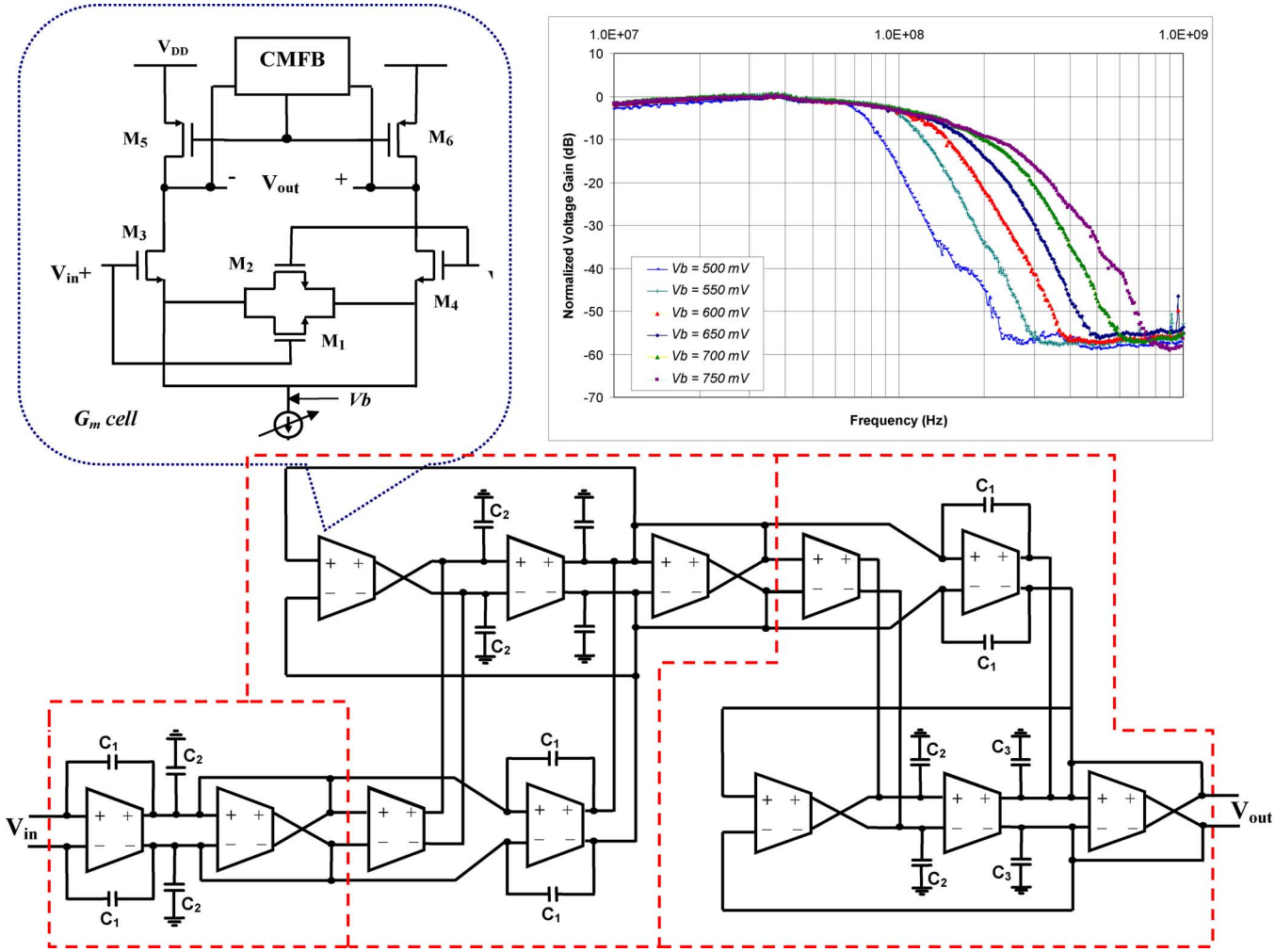

Fig. 14. 5th order elliptic variable bandwidth LPF circuit and measured transfer characteristics at different g_m settings using current bias voltage, Vb.

dynamically. The implemented QVCO exhibits phase noise profile of -106 dBc/Hz at 1 MHz and -130 dBc/Hz at 10 MHz offset and phase mismatch less than 3.5°. In order to judge the effect of phase noise, we have simulated the system with an ideal QVCO operating at the band center frequencies and compared it to the case when the QVCO phase noise is introduced. Our simulation shows that the RX sensitivity only degrades by 0.6 /1.1 dB with the measured phase noise profile and the LNA is in high /low gain setting respectively.

Due to the wideband nature of the proposed chirp modulated UWB pulse, AC coupling can be employed to remove DC offsets due to LO leakage and flicker noise without significant signal energy loss for demodulation. The combined RX front-end achieves a voltage gain of 31/ 40 dB, NF of 10/ 7.5 dB and IIP3 of -15 /-29 dBm in the low/ high gain modes respectively while the mixer achieves LO-IF and RF-IF isolation better than 25 dB. As expected, linearity is significantly poorer in the high gain state which implies that the antenna and LNA gain roll-off needs to provide larger than the 20 dB out-of-band attenuation assumed in the linearity calculations.

B. Analog Baseband

The analog baseband consists of a LPF with variable bandwidth, a baseband squarer and a comparator. To achieve in-band

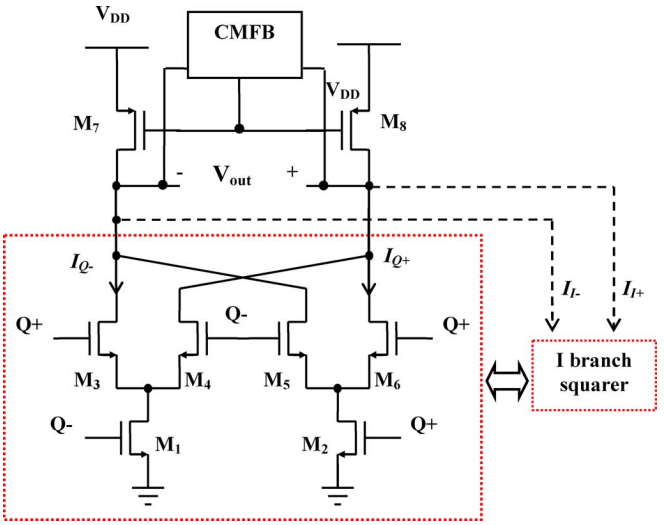

Fig. 15. Four quadrant baseband squarer.

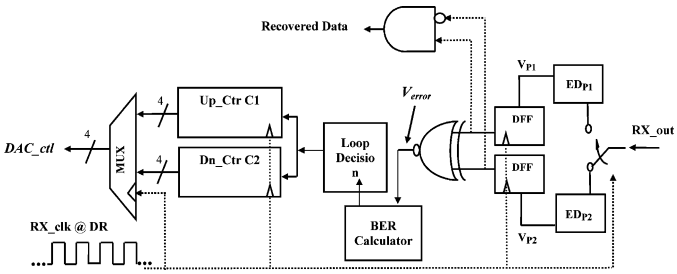

Fig. 16. Functional representation of the demodulation calibration loop.

interference mitigation as discussed in Section III-C, the LPF needs to exhibit fast roll off with large stop-band attenuation of 50 dB. Therefore, a 5th order elliptic filter with 0.1 dB pass-band ripple is chosen. The filter is implemented as a cascade of one 1st order and two bi-quad $\mathrm{G_m}$-C stages as shown in Fig. 14. Identical trans-conductance cells are used and the variable bandwidth is achieved by tuning the trans-conductance through bias current. The $\mathrm{G_m}$ cell consists of a differential pair degenerated with triode transistors M1/M2 for improved linearity performance. All cells within the filter are DC coupled and the output common mode is set at 0.9 V through a common mode feedback (CMFB) circuit. From simulation, $\mathrm{G_m}$ needs to change from 0.12 to 0.71 mS in order to vary the filter cutoff from 75 to 250 MHz. The tuning is achieved by controlling the tail bias current through an external voltage Vb and the resulting tunable low-pass characteristics is shown in Fig. 14. The LPF suffers from 4.5 dB loss and two additional differential amplifier stages (not shown) are used to boost the signal by 28 dB before sending to the squarer.

A four-quadrant self multiplier-shown in Fig. 15 implements the squaring operation. Squaring is performed at baseband to relax the input bandwidth requirement and achieve a larger squarer gain (A_{sq}). The simulated A_{sq} of the squarer is 75 and is linear up to input level of $\sim 150\ \mathrm{mV}$. The I and Q path signals are combined in current domain through common active loads (M7/M8). The differential to single-ended converter further amplifies this combined signal by 9.5 dB before sending to a dual threshold Schmitt trigger comparator which further improves noise immunity.

The bottleneck for the system linearity and NF is predominantly in the front-end and the analog baseband does not degrade either metric significantly. System simulations of the total receiver chain performance confirm that the $\mathrm{NF} = 10.33\ \mathrm{dB}/7.57\ \mathrm{dB}$ and $\mathrm{IIP3} = -16.4/-29.5\ \mathrm{dBm}$ for gain of 31/40 dB. Capable of up to 20 Mbps operation, the RX consumes between 30 mA (31 dB RF gain/ 75 MHz passband) to 55 mA (40 dB RF gain/ 245 MHz passband) under a 1.8 V supply.

C. Demodulation Calibration Loop

As discussed earlier, the choice of $LO_{1,2}$ ultimately determines the optimal trade-off between sensitivity and in-band interference rejection. For optimized sensitivity, the LO frequency must be positioned near the band center frequency and the LPF cutoff must be increased so as to maximize the captured signal energy. On the other hand, interference mitigation requires a smaller LPF cutoff and careful shifting of LO frequency so as to move the in-band interference out of the LPF passband. The demodulation calibration loop continuously monitors the demodulated data and dynamically shifts the LO tones by varying the 4 bit DAC input for LO_1 and LO_2. The functionality of the DCL is illustrated in Fig. 16 and is realized on field programmable gate array (FPGA).

First, the demodulated data (*RX_out*) from comparator output is sent to two energy detectors ($\mathrm{ED_{P1,P2}}$) which detect the presence of a viable signal in time windows (P1, P2) corresponding to $LO_{1,2}$. The energy detector outputs ($\mathrm{V_{P1}}$, $\mathrm{V_{P2}}$) are then stored in two D-flip-flops triggered by the RX_clk. Assuming correct demodulation scenario, $\mathrm{V_{P1}}$ and $\mathrm{V_{P2}}$ will only be high if "1" and "0" are transmitted respectively. Moreover, only one of them should be high during each bit period according to our modulation scheme discussed earlier. Therefore, correct data can be recovered by a logical "AND" of the two D-flip-flop outputs as illustrated. Conversely, a demodulation error is detected if the energy detector outputs are either both high or low together (through XNOR) and is recorded by the BER block. During calibration, two 4 bit counters are used to cycle through all the possible $LO_{1,2}$ settings. The up-counter shifts the LO_1 frequency upward, whereas the down-counter shifts the LO_2 frequency downward. The output of these counters is multiplexed to the DAC control of the QVCO. For each $LO_{1,2}$ combination, the BER is collected and stored. After cycling through all the possible combinations, the $LO_{1,2}$ combination that provides the smallest BER is utilized for the subsequent demodulation for optimal trade off between sensitivity and interference mitigation. If no suitable LO setting is found in the high gain mode, then the LNA, which operates in high-gain mode by default is switched to low gain and we search for the optimal $LO_{1/2}$ tone settings again.

The DCL calibration is performed every time the BER performance of the TxRx becomes larger than the target BER of 10^{-3} as a result of entering a new interference environment. Due to its off-line nature, the DCL calibration time specifications are dependent solely on the expected frequency of calibration. Since there are 8 possible LO settings for each band, the

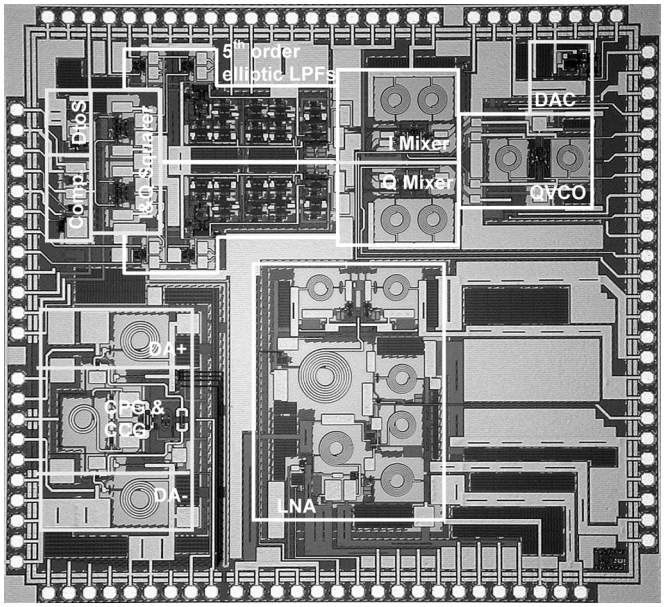

Fig. 17. Die photo.

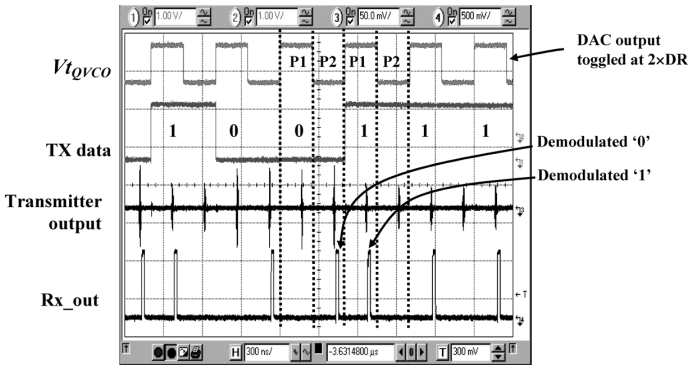

Fig. 18. Time domain demodulation and receiver output showing frequency to position translation. (2 Mbps DR, 4 MHz PRF, $LO_{1/2} = 3.3/3.7$ GHz).

average number of cycles needed is $7 \times 7 \times 1.5 = 73.5$ (assuming a 50% chance of finding the optimal setting in high and low gain modes). Then assuming a data rate of 4 MHz, the target DCL target time is $(73.5 \times 10^5)/4 \times 10^6 \approx 1.8$ s.

VI. System Measurements

The transceiver IC is integrated in Chartered's 0.18-μm CMOS technology and housed in a QFN48 package. The die shown in Fig. 17 occupies about 2.5 mm $\times$ 2.7 mm. The packaged IC is mounted on a Rogers high frequency PCB test bed while the demodulation calibration block and all the signal processing of the digital baseband (as shown in Fig. 3) are implemented in FPGA. The digital settings for the chirp control and LPF variable bandwidth control are varied manually through on-board switches. The pseudo-random (PR) transmitted data pattern (TX data) and the transmitter clock (TX_clk) are generated by the FPGA. The recovered baseband data from RX is fed back to the FPGA where it is sampled and digitized for further baseband processing. A high frequency oscilloscope was used to monitor the time domain operation of the system and a snapshot of a typical data transmission and corresponding pre-sampling demodulator output are shown in Fig. 18. The demodulation of transmitted data from chirp modulated UWB pulse can be clearly observed.

The measurement setup for the BER and SIR measurement is illustrated in Fig. 19. For BER measurements, a 10^{10} bit PR data packet is transmitted to the receiver through a variable attenuator. The TX-RX communication delay is then determined by viewing the transmitted data pattern and the digitized demodulation output in a logic analyzer. By compensating for this fixed delay, the two bit streams are then aligned and compared using a BER computation algorithm implemented in the FPGA. The attenuation of the transmission link is then increased step-wise and the resulting BER degradation is measured and shown in Fig. 20. It can be seen that the receiver sensitivity of -84 dBm is achieved at 10^{-3} BER for *DR* of 4 Mbps with transmitted pulse width of 10 ns. It should be noted that this minimum system sensitivity is observed under high gain mode in the absence of any interference signal. For optimal demodulation, the $LO_{1,2}$ tones are fixed at the sub-band center frequencies of 3.35 GHz and 3.70 GHz and the LPF is operated at 160 MHz pass-bandwidth.

In SIR characterization, a single tone interferer is introduced across the band of interest while measuring the BER. For this test, the receiver input power level is maintained at 4 dB above the minimum achievable sensitivity (-80 dBm) while the interferer power level is gradually increased to the limit where the receiver BER reaches 10^{-3}. This maximum tolerable interference power level is plotted against the interference frequency in Fig. 21. The receiver is switched between high gain and low gain mode during measurement to ensure that the achievable SIR is not limited by the RF front-end. From the measurement, the receiver can achieve out-of-band SIR of -59 dB, which is limited by the linearity achieved at low gain mode. The attenuation of the power combiner was not considered in the measurement as it does not affect the SIR. However, it must be noted that the actual input interference and signal powers at the receiver are in fact ~ 1.5 dB lower than reported in Fig. 21. Also, the interference levels below 3.1 GHz can be higher than the front-end P-1 dB because of the narrowing of the passband in low-gain mode as shown in Fig. 10. With the proposed DCL and by adjusting LPF cutoff correspondingly, in-band SIR of better than -21 dB is achieved even when the interference frequency coincides with the center of the transmitted signal sub-band B1 and B2 (3.4 GHz and 3.7 GHz). The systems ability to optimally trade off the system sensitivity (from -84 dBm to -80 dBm) for better in-band/out-of-band interference immunity (SNR $= -21$ dB at 3.4 GHz/-59 at 4.1 GHz) is clearly demonstrated in Fig. 21.

For the DCL, 10^5 bit data packet is sent repeatedly under different $\mathrm{LO}_{1/2}$ settings as described in Section V.A and the best setting is chosen. The worst-case calibration time would be when all $7 \times 7 = 49$ $\mathrm{LO}_{1/2}$ settings have to be cycled twice – once for each gain setting. Hence the measured calibration time is $(2 \times 49 \times 10^5)/\mathrm{Data\ rate}$. At very low data rates (< 1 MHz), the calibration time can become quite large and hence the BER accuracy has to be sacrificed by using a smaller test data packet size in order to maintain acceptable calibration time.

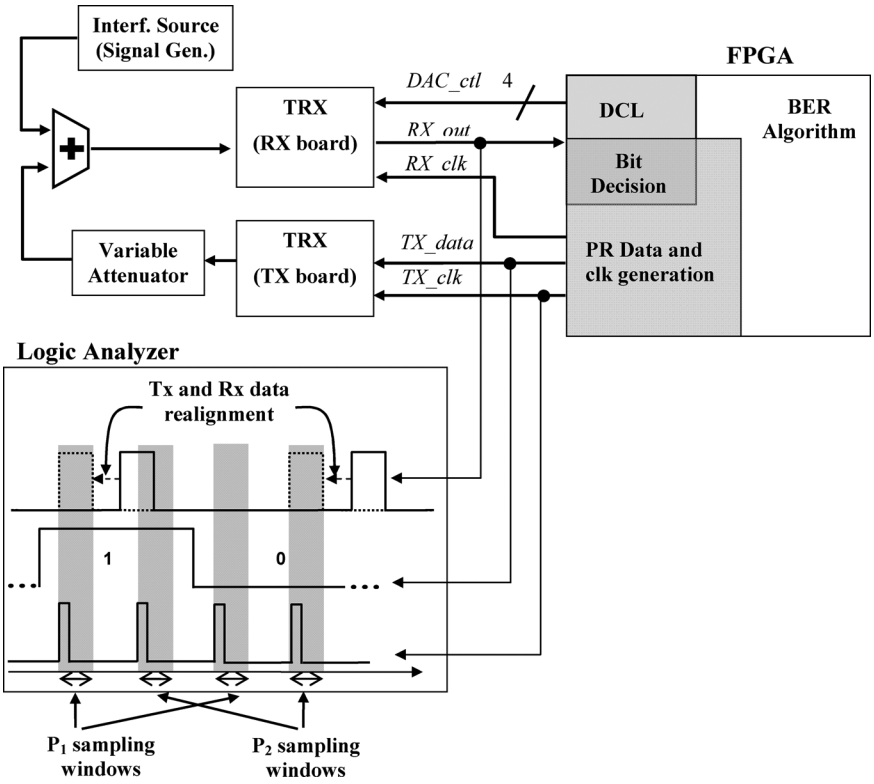

Fig. 19. BER/ SIR measurement setup.

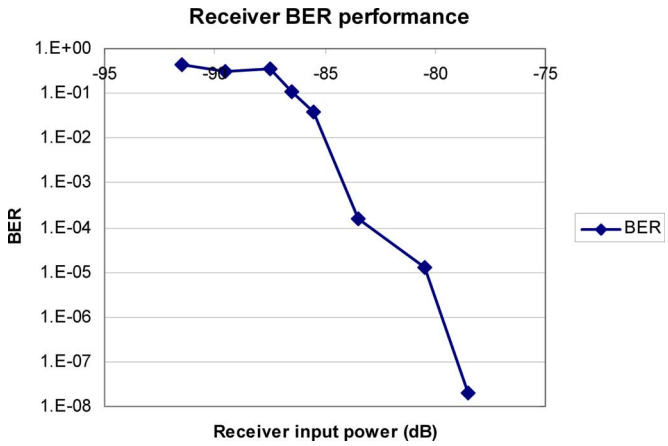

Fig. 20. Measured receiver BER versus input power @ 4 MHz data rate.

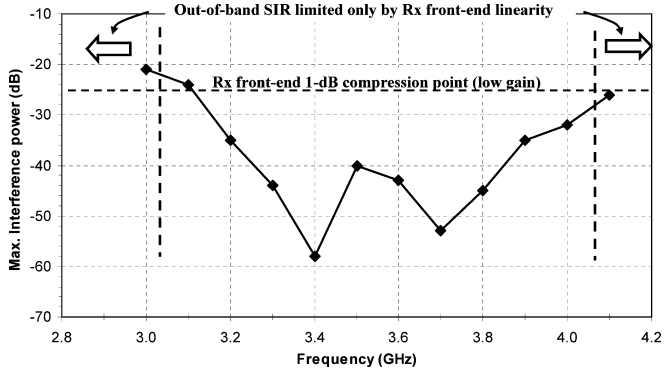

Fig. 21. Measured maximum tolerable in-band interference power, $\mathrm{P_{int}}$ to maintain 10^{-3} BER @ 4 MHz data rate when received power, $\mathrm{P}_{in} = -80$ dBm.

The transceiver requires 0.77 nJ/bit for transmitting and 2.7–4.95 nJ/bit for receiving. The transceiver performance has also been tabulated and compared with the state-of-the-art IR-UWB transceivers in Table I. As shown, our work has extremely competitive interference mitigation capabilities and provides the added benefit of low system complexity and scalability. At first glance, the bit energy efficiency of our transceiver might appear low. However, for the transmitter it would be unfair to compare only the $\mathrm{E/b}$ without accounting for the significantly larger achievable range afforded by the C-UWB approach, especially for LDR applications. For instance, [7] achieves much lower transmit $\mathrm{E/b}$ (108 pJ/b) than our work in $0.18\ \mu\mathrm{m}$ technology. However, it must be noted this power efficiency is obtained by using extremely narrow, low-swing pulses and relying on very high data rates (1 Gb/s) to achieve spectrum utilization. Consequently, the transmission range of this scheme is severely limited by the lack of adequate energy in each individual pulse. Moreover, at low data rates, the bandwidth (500 MHz) and inherent swing limitations (approx. 2 Vp-p) would mean that the Gaussian pulse, unlike the C-UWB pulse can neither be made longer nor of larger amplitude. This lack of flexibility of IR-UWB drastically reduces spectral efficiency and hence would render this transceiver highly unsuitable for LDR communication when compared to the C-UWB approach. If long transmission range is not required, the power hungry blocks of our transmitter can be duty-cycled further and $\mathrm{E/b}$

TABLE I
SUMMARYOF MEASURED RECEIVER PERFORMANCE AND BENCHMARKING AGAINST STATE OF THE ART IN PUBLICATION.

Author / Institution	This work	Lee et al. / MIT [8]	Ryckaert et al. IMEC[15]	Medi et al. UCLA[7]	Lachartre et al. CEA-LETI-Minatec [21]	Sanghoon et al. ETRI [22]
Product / Publication	-	ISSCC 2007	JSSC 2007	JSSC 2008	ISSCC2009	ISSCC2010
Approach	Chirp modulated UWB TX, Quad. energy detection RX	Sub-banded PPM RX	Quad. Analog Corr. PPM RX	Channelized BPSK TXRX	OOK/PPM/BPSK	BPPM-BPSK Coherent
Technology / Supply	0.18µm CMOS 1.8 V	90nm CMOS 0.65 V	0.18µm CMOS 1.8 V	0.18µm CMOS 1.8 V	0.13µm CMOS 1.2 V	0.13µm CMOS 1.2 V
Sensitivity (BER)	-84 dBm (10^{-3}) @4Mbps	-99 dBm (10^{-3}) @100kbps	-	-	Maximum -78dBm @1Mbps	-79dBm Maximum
Out-of-band SIR (10^{-3} BER)	-59 dB@4Mbps	-46 dB@100kbps	-54 dB *	0 dBm (interferer power level)	-	-
In-band SIR (10^{-3} BER)	-21 dB@4Mbps	-15 dB@100kbps	-44 dB †*	-20 dBm (interferer power level)	-	-
Data rate	<20 Mbps	0 - 16.7 Mbps	< 1 Mbps	1 Gbps	<31Mbps	<27.24Mbps
Power	0.77nJ/b (TX) 2.7 - 4.95nJ/b (RX)	2.5nJ/b (RX)	1.44nJ/pulses (RX)	108pJ/b (TX) 98pJ/b (RX)	0.022nJ/b (TX) 2.26nJ/b(RX)**	3.3nJ/b (TX/RX)
Area	2.5×2.7mm^2	1×2.2mm^2	5×1.6mm^2	4.3×3.5mm^2	8 mm^2	-

† Only measured for in-band interference signals > 250MHz away from the transmitted signal center frequency
* BER is achieved with certain coding gain or receiver processing gain (32 pulses for 1 bit)
** Only analog part of the receiver considered

can be reduced drastically by reducing t_p. By using t_p in the same range as that typically used in IR-UWB (< 2 ns) the proposed transceiver can easily achieve comparable $\mathrm{E/b}$.

For the receiver, [7] reported the bit energy efficiency considering only 1 ns pulse width without considering the time needed to turn on the receiver and synthesizer, and thus could be misleading. In [15], 32 pulses are used to encode 1 bit to obtain coding or processing gain for enhanced sensitivity. This relaxes the RF front-end design and might result in lower receiver power consumption. However, the actual data bit energy efficiency could be much worse ($32\times$) than the reported figure. In [8], the lower energy efficiency is due to the lower supply voltage employed, which is feasible in 90 nm technology. The total current consumption is actually about 55 mA and is comparable to our design. In addition, the proposed pulse system can be modified slightly to mimic similar pulse position modulation technique employed in [8]. This could then reduce the required turn on time of the receiver and result in better energy efficiency. We also observe that the receiver $\mathrm{E/b}$ is quite comparable to even the mostly digital application of [21] even though the digital current has been omitted from the $\mathrm{E/b}$ calculations.

VII. CONCLUSION

A scalable, low complexity IR-UWB transceiver utilizing chirp modulated UWB pulses has been demonstrated. The proposed pulses have been shown to be a much more flexible and power-efficient alternative to Gaussian monocycle pulse generation in order to fully utilize the FCC spectral mask. A time interleaved toggled LO demodulation scheme has been implemented in the receiver. Through a demodulation calibration loop which optimizes the LO frequency placement and LPF with variable bandwidth, optimal trade off between energy detection (sensitivity) and interference mitigation can be achieved. In-band and out-of-band SIR of -21 dB and -59 dB has been achieved.

REFERENCES

[1] "FCC Notice of Proposed Rule Making, Revision of Part 15 of the Commission's Rules Regarding Ultra-Wideband Transmission Systems," FCC, Washington, DC, ET-docket 98-153.
[2] H. Liu, "Multicode ultra-wideband scheme using chirp waveforms," *IEEE J. Sel. Areas Commun.*, vol. 24, no. 4, pp. 885–891, Apr. 2006.
[3] S. Diao, Y. Zheng, and C. H. Heng, "A CMOS ultra low-power and highly efficient UWB-IR transmitter for WPAN applications," *IEEE Trans. Circuits Syst. II*, vol. 56, no. 3, pp. 200–204, Mar. 2009.
[4] *IEEE Standard for Information Technology – Telecommunications and Information Exchange Between Systems – LANs and MANs*, IEEE Std 802.15.4a-2007.
[5] Y. Gao, Y. Zheng, and B. L. Ooi, "0.18 μm CMOS dual-band UWB LNA with interference rejection," *Electron. Lett.*, vol. 43, no. 20, pp. 1096–1098, Sep. 2007.
[6] G. Cusmai, M. Brandolini, P. Rossi, and F. Svelto, "A 0.18-μm CMOS selective receiver front-end for UWB applications," *IEEE J. Solid-State Circuits*, vol. 41, pp. 1746–1771, Aug. 2006.
[7] A. Medi and N. Won, "A high data-rate energy-efficient interference-tolerant fully integrated CMOS frequency channelized UWB transceiver for impulse radio," *IEEE J. Solid State Circuits*, vol. 42, no. 11, pp. 2515–2525, Nov. 2007.
[8] F. S. Lee and A. P. Chandrakasan, "A 2.5 nJ/b 0.65 V 3-to 5 GHz subbanded UWB receiver in 90 nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 116–117.
[9] J. F. Gerrits, J. R. Farserotu, and J. R. Long, "Low-complexity ultra-wide-band communications," *IEEE Trans. Circuits Syst. II*, vol. 55, no. 4, pp. 329–333, Apr. 2008.
[10] R. Roovers, D. M. W. Leenaerts, J. Bergervoet, K. S. Harish, R. C. H. van de Beek, G. van der Weide, H. Waite, Y. Zhang, S. Aggarwal, and C. Razzell, "An interference-robust receiver for ultra-wideband radio in SiGe BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 40, pp. 2563–2572, Dec. 2005.
[11] B. Razavi, *RF Microelectron.*. Upper Saddle River, NJ: Prentice Hall, 1998, pp. 20–22.
[12] G. Yuan, K. Cai, Y. Zheng, and B. L. Ooi, "A wideband CMOS multiplier for UWB application," in *Proc. IEEE Int. Conf. Ultra-Wideband*, Sep. 2007, pp. 184–187.

[13] T. Terada, S. Yoshizumi, M. Muqsith, Y. Sanada, and T. Kuroda, "A CMOS ultra-wideband impulse radio transceiver for 1-Mb/s data communications and ± 2.5-cm range finding," *IEEE J. Solid-State Circuits*, vol. 41, pp. 891–898, Apr. 2006.
[14] J. H. Chang and C. K. Kim, "A symmetrical 6-GHz fully integrated cascode coupling CMOS LC quadrature VCO," *Microwave Wireless Comp. Lett.*, vol. 15, no. 10, pp. 670–672, Oct. 2005.
[15] J. Ryckaert, M. Verhelst, M. Badaroglu, S. D'Amico, V. Deheyn, C. Desset, P. Nuzzo, B. Van Poucke, P. Wambacq, A. Baschirotto, W. Dehaene, and G. Van der Plas, "A CMOS ultra-wideband receiver for low data-rate communication," *IEEE J. Solid-State Circuits*, vol. 42, pp. 2515–2527, Nov. 2007.
[16] J. G. Proakis, *Digital Communications*, 4th ed. New York: McGraw-Hill, 2001, p. 511.
[17] C.-T. Fu, C.-L. Ko, and C.-N. Kuo, "A 2.4 to 5.4 GHz low power CMOS reconfigurable LNA for multistandard wireless receiver," in *Proc. IEEE Radio Frequency Integrated Circuits Symp.*, 2007, pp. 65–68.
[18] C. Chen, M. A. Do, K. S. Yeo, and C. C. Boon, "A low power UWB direct conversion receiver with pulse detectors," in *Proc. Int. SoC Design Conf.*, 2009, pp. 17–20.
[19] H. Zheng, S. Lou, D. Lu, C. Shen, T. Chan, and H. C. Luong, "A 3.1 GHz-8.0 GHz single-chip transceiver for MB-OFDM UWB in 0.18-μm CMOS process," *IEEE J. Solid-State Circuits*, vol. 44, pp. 414–426, Feb. 2009.
[20] Y.-C. Chen, W.-K. Yeh, R.-L. Wang, and H.-D. Yen, "2–10 GHz UWB low noise amplifier using a cascode structure with resistive shunt feedback," in *Proc. Asia-Pacific Microwave Conf.*, 2007, pp. 1–3.
[21] D. Lachartre, "A 1.1 nJ/b 802.15.4a-compaliant fully integrated UWB transceiver in 0.13 μm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 312–313.
[22] S. Joo, "A fully integrated 802.15.4a IR-UWB transceiver in 0.13 μm CMOS with digital RRC synthesis," in *ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 228–229.
[23] N. Pletcher, J. Rabaey, and S. Gambini, "A 52 μW wake-up receiver with -72 dBm sensitivity using an uncertain-IF architecture," *IEEE J. Solid State Circuits*, vol. 44, no. 1, pp. 269–280, Jan. 2009.

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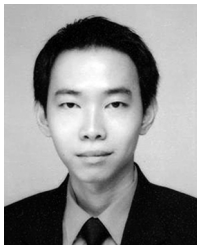

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