High-mobility carbon-nanotube thin-film transistors on a polymeric substrate

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We report the development of high-mobility carbon-nanotube thin-film transistors fabricated on a polymeric substrate. The active semiconducting channel in the devices is composed of a random two-dimensional network of single-walled carbon nanotubes (SWNTs). The devices exhibit a field-effect mobility of 150 cm^2/Vs and a normalized transconductance of 0.5 mS/mm. The ratio of on-current (I_{on}) to off-current (I_{off}) is ~100 and is limited by metallic SWNTs in the network. With electronic purification of the SWNTs and improved gate capacitance we project that the transconductance can be increased to ~10–100 mS/mm with a significantly higher value of I_{on}/I_{off}, thus approaching crystalline semiconductor-like performance on polymeric substrates. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1854721]

Researchers are currently developing thin-film transistors (TFTs) using various organic semiconductors in order to construct electronics on polymeric materials for such "macroelectronic" applications as lightweight flexible displays, smart materials, inexpensive radio frequency identification, etc., whereby the performance metric is not driven by Moore's law scaling as in conventional microelectronics but is instead determined by the low-cost per unit area and the compatibility with large-area, noncrystalline substrates.[1] The goal is to eventually use fabrication techniques analogous to printing technology to produce inexpensive electronics on flexible sheets. However, the available semiconducting materials for these applications such as amorphous or organic semiconductors have relatively low electron mobilities and are unsuitable for higher speed applications.[1,2]

We recently proposed an alternative semiconducting material for such applications that consists of a two-dimensional random network of single-walled carbon nanotubes (SWNTs).[3] Individual SWNTs are known to possess an extremely high electron mobility, $\mu > 10\,000$ cm^2/Vs,[4] operate at high frequencies >1 GHz,[5,6] and can be deposited from solution onto polymeric substrates.[7,8] A major roadblock for using SWNTs in nano- or microelectronic applications is the lack of a manufacturable process to precisely assemble SWNTs into small devices. The use of random networks of SWNTs circumvents this issue for relatively large-area macroelectronic devices [device area $\gg 1/$(nanotube density)] since the devices then exhibit the averaged properties of a large number of random individual SWNTs. We have found that such SWNT networks are electrically continuous over arbitrarily large areas and that we can fabricate the networks into devices with high yield using conventional processing techniques.[3] Our initial devices, which were fabricated on an amorphous SiO_2 substrate, exhibited a tenfold higher field-effect mobility ($\mu \sim 10$ cm^2/Vs) than amorphous Si (*a*-Si) TFTs[2] indicating the potential of this new material for use as the active semiconducting material for macroelectronic devices. Similar results have been achieved with such random network SWNT transistors fabricated on flexible polymeric substrates.[9,10]

In a somewhat similar approach, recent work has succeeded in fabricating thin-film transistors using an array of parallel semiconductor nanowires as the active electronic material.[11] These semiconductor nanowire TFTs achieved a $\mu = 119$ cm^2/Vs and a normalized transconductance of 0.09 mS/mm. These values compare favorably to those observed in *a*-Si TFTs where $\mu = 1$ cm^2/Vs and $g_m = 0.01$ mS/mm are typical.[2] This result, along with those described above, indicate that networks and/or arrays of high-mobility SWNTs or semiconducting nanowires are promising nanomaterials for macroelectronic applications.

In this letter we report a significant improvement in the performance of SWNT TFTs fabricated on a polymeric substrate. We have achieved a normalized transconductance of 0.5 mS/mm for a 7-μm-channel length SWNT TFT operated at $V_{SD} = -1.5$ V. The field-effect mobility of the device is 150 cm^2/Vs which approaches the mobility of a p-type crystalline Si MOSFET. We also discuss the device design and material improvements required for further performance gains. As techniques are developed to electronically purify SWNTs we predict that it will be possible to produce SWNT TFTs with a normalized transconductance in the range of 10–100 mS/mm, thus approaching single-crystal semiconductor performance on polymeric substrates.

We fabricated the SWNT TFTs using the following process. A 10-μm-thick layer of polyimide was spin coated onto a silicon wafer and cured in a nitrogen ambient in stages of 100 °C steps for 1 h each to a maximum temperature of 300 °C. Gate metal fingers and contact pads were formed on the polyimide surface by electron beam deposition and liftoff of 25 nm of Ti. These gate metal fingers were covered with 100-nm-thick gate dielectric pads of silcon oxide by electron-beam evaporation and liftoff of fused silica. The wafer was soaked for 1 h in a 3%–5% solution by volume of 3-aminopropyl trimethoxysilane. The wafer was blown dry and then soaked in a solution SWNTs prepared in the following manner: (a) 1% by weight of sodium dodecyl sulfate (SDS) was mixed in water and ultrasonicated until dissolved; (b) one mg/ml of SWNT powder (Carbolex as-grown SWNTs) was added and ultrasonicated at 10 W for 45 min;

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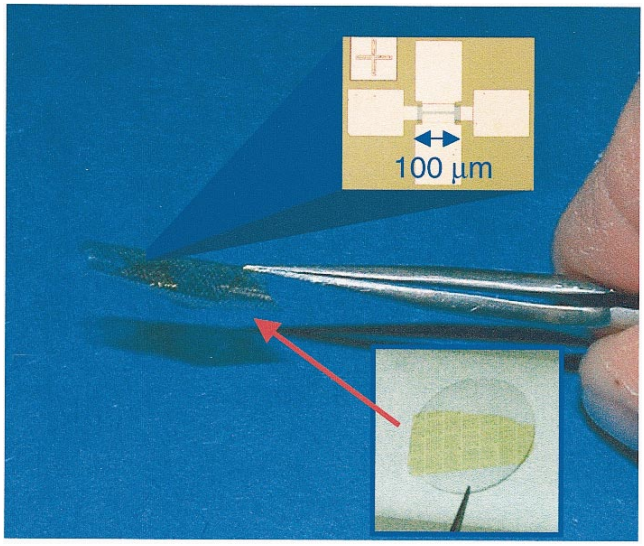

FIG. 1. (Color) Optical image of a flexible, curled film of SWNT TFTs constructed on a 10-μm-thick film of polyimide. The lower inset shows the same film supported by a glass substrate. The upper inset is a magnified image of an individual TFT.

(c) the solution was centrifuged for 1 h at 12 000 g, and the liquid was decanted, leaving behind sediment formed by centrifugation; (d) the centrifugation and decanting process was repeated until no sediment formed. The wafer was removed from the CNT solution and blown dry when a continuous nanotube network has formed (~50–100 h in the CNT solution) as determined by test pieces treated exactly as the device wafer and periodically removed to check sheet resistance. This leaves the entire wafer coated with the SWNT network. The wafer was then soaked in DI water for at least 1 h to remove any residual SDS. Source-drain contact pads were formed by electron-beam evaporation and liftoff of 100 nm of titanium. A photoresist layer was patterned to cover the active area of the devices, and a commercial CO_2 snowjet from Applied Surface Technologies was used to remove all SWNTs not protected by the photoresist. Figure 1 shows an optical micrograph of an array of devices on a freestanding film of the polyimide after it was peeled from the Si substrate.

Figure 2(a) and 2(b) show the device characteristics for a typical SWNT TFT fabricated with a channel length, $L_{SD}=7$ μm, and a channel width, $W=130$ μm. The normalized device transconductance ($\equiv g_m/\mathrm{W}$) is 0.5 mS/mm at $V_D=-1.5$ V and the current on-to-off ratio is 70 at $V_D=0.01$ V. Note that the transconductance is scaled by the full width of source-drain channel, W. Commonly in such SWNT or nanowire devices the transconductance is normalized by the width of the SWNTs/nanowires which results in a much larger value because the percentage surface coverage of SWNTs/nanowires is typically very low (<1%). The value we report is more useful for comparison to competing TFT technologies while the latter method reveals the high performance capabilities of the individual SWNTs/nanowires in such devices. Although the exact number of current paths in our network devices is difficult to count, we note that AFM images determine that the fill factor in our devices is ~1%, indicating that the current drive per conducting path in the SWNT network is quite high.

From Fig. 2(b) and using the formula, $\mu=L_{SD}^2 g_m / C_G V_D$, we calculate a field-effect mobility of

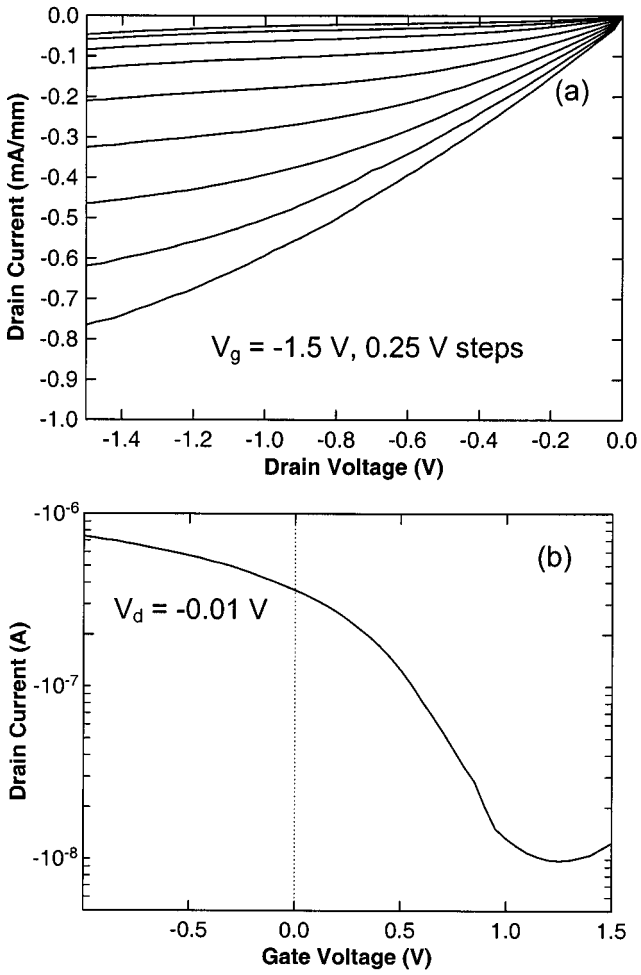

FIG. 2. (a) Drain current of a SWNT TFT vs the drain voltage measured at gate voltages ranging from −1.5 to 0.5 V in 0.25 V steps; (b) drain current vs gate voltage measured at a drain voltage of −0.01 V.

150 $\mathrm{cm}^2/\mathrm{Vs}$ at $V_D=0.01$ V. In this analysis we used the full parallel-plate gate capacitance, $C_G=\varepsilon W L_{SD}/L_{OX}$, in estimating μ. This value of C_G slightly overestimates the gate capacitance and correspondingly underestimates the mobility of the current paths in the SWNT network due to its low fill factor (see the discussion of the gate capacitance below). This mobility value approaches the field-effect mobility observed in p-type crystalline Si MOSFETs and demonstrates that SWNTs are a viable nanomaterial for high-performance electronics on polymeric substrates.

The device transfer characteristics shown in Fig. 2(b) indicate an I_{on}/I_{off} value of 70. This value is typical with values ranging from 400 to 50 observed in an array of ten devices. While a low off-state current is not required for amplifier applications, a high value of I_{on}/I_{off} is required for switching or logic applications. The off-state leakage is caused by metallic and small-band-gap semiconducting nanotubes in the network that are not fully depleted by the gate bias. Attempts to increase the transconductance either by increasing the SWNT density or by decreasing the channel length lead to a reduced value of I_{on}/I_{off} as the percentage of metallic conduction paths increases. Consequently, the electronic purity of the SWNT source material is a major factor that currently limits additional improvement of our device performance. It should be noted that researchers are making significant progress towards eliminating metallic

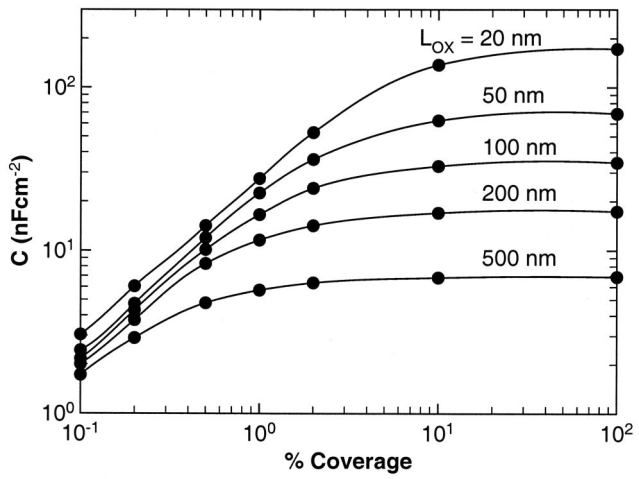

FIG. 3. Calculated values of the gate capacitance (circles) vs the % coverage of SWNTs for various gate oxide (SiO_2) thicknesses ranging from 20 to 500 nm. The solid lines are guides for the eye.

nanotubes by a variety of techniques that include selectively removing metallic SWNTs from the source material[11–19] or by chemically converting the metallic SWNTs into semiconducting ones.[20] As these primarily semiconducting SWNT source materials become available, the SWNT density can be increased significantly while also achieving a high value of I_{on}/I_{off} that is necessary for switching applications.

An increased SWNT density coupled with a thinner gate dielectric would significantly increase the transconductance of SWNT TFTs. Figure 3 shows the results of a calculation[21] of the gate capacitance versus nanotube density for various SiO_2 gate oxide thicknesses that range from 500 to 20 nm. For low nanotube densities the gate capacitance increases in proportion to the density of nanotubes. However, as the spacing between nanotubes becomes comparable to the thickness of the gate oxide, the value of the gate capacitance saturates, approaching the value of a parallel-plate capacitor. This saturation of the gate capacitance occurs when the field lines from neighboring SWNTs begin to overlap. According to this calculation, increasing the nanotube density will produce a corresponding increase in the transconductance up until the mean distance between nanotubes approaches the oxide thickness, after which there is limited additional gain. For our 100-nm-thick gate oxide, the maximum transconductance will be achieved for nanotube surface coverages $\sim$1% which is close to our observed coverage.

In addition to increases in nanotube density, the gate capacitance can be increased by using high-κ gate dielectrics such as HfO_2[22–26] or by using solid-state electrolytic gates.[27] It has been demonstrated that by using these materials the gate capacitance per nanotube can approach the quantum capacitance limit of 4 pF/cm.[22,28] Our model calculations indicate that our current gate capacitance/nanotube is $\sim$0.2 pF/cm indicating that there is room for an order of magnitude increase in gate capacitance per SWNT by using such materials. Coupling this capacitance increase with a density increase to $\sim$10% surface coverage,[29] we can reasonably expect to achieve SWNT TFTs with a transconductance in the range of 10–100 mS/mm.

In conclusion, we have fabricated high-mobility TFTs on a polyimide substrate using a random network of SWNTs as the active semiconducting material. The transistors exhibit a transconductance and field-effect mobility that is approximately two orders of magnitude larger than *a*-Si-based TFTs. With the anticipated development of electronically pure SWNT source materials and the use of advanced gate materials the TFT performance can be improved even further. Thus, the use of high-mobility nanomaterials is a promising approach to realizing high-performance macroelectronic devices and circuits on large-area polymeric substrates.

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