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Microprocessors Thermal Challenges for Portable and Embedded Systems Using Thermal Throttling Technique

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Abstract

High performance systems bring high temperatures, which result in decreased lifetime reliability, increase total power consumption, rapidly deplete battery energy, thereby bring transient errors.
The management of how a computer system will dispose of heat is an integral part of microprocessor design.
Thermal throttling technique regulates the thermal environment by alternating between running the processor at full speed and placing the processor in a sleep state whenever the upper limits of the thermal envelope are reached. This technique can be applicable for high performance portable and embedded systems thermal management by deliver higher performance at the same die temperature or the same performance at a lower die temperature, which allow the possible elimination of passive/active cooling solutions, reduces system weight and time-to-market as there is no need for explicit microprocessors thermal management.

In this paper a thermal throttling technique is presented, that coordinates between processors thermal states and running states. Simulation results verifies that, by using the presented method, more than 7% of further reduction in generated temperature is obtained. When temperature is high, the presented method is considered to be the most effective technique.

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Key Words: -Dynamic Thermal Management-DTM, Thermal Throttling Technique

1. Introduction

The microprocessors industry has been growing rapidly for the past decade leads to high system energy consumption. As energy density has increased exponentially with Moore's Law, energy consumption reduction and thermal cooling challenges have become a prominent and vexing aspect of computer systems design, and emerged as a major constraint in the design of microprocessors [1].

Most of the energy consumed by a microprocessor is dissipated as heat due to the resistive behavior of the processor circuits. The temperature of a chip, which is a measure of the amount of heat energy stored in it, is directly related to the power density that consumed per unit area of the processor chip [2].

Microprocessors thermal management gets demanding because of [3, 4]:

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- Increasing power need requires the need of increased heat handling capacity in thermal solutions.
- Increasing power density need to spread or smooth heat out.
- Increasing box or case temperature reduced margins safety of temperature.

A processor is typically designed to meet a specific thermal design power. The thermal throttling solution is required to dissipate the maximum power consumption and temperature of a processor. The main aim of this technique is to lowering the processor clock speed and is generally to reduce processor temperature.

Thermal management has become a research focus in recent years. J. Donald and M. Martonosi, presents a framework and methodology for evaluating a variety of thermal control options in [5], their performing thermal control combination includes both control-theoretic distributed DVFS and a sensor-based migration policy. Amit Kumar et al. in [6] proposed HybDTM, a system-level framework for doing fine-grained coordinated thermal management using a hybrid of hardware and software techniques. Finally, a novel technique for determining the placement of temperature sensors on complex Multi-Processor Systems-on-Chips (MPSoCs) floorplans are proposed by F. Zanini et. al. in [7].

This paper presented a new thermal throttling technique for dynamic thermal management approach that is applicable for portable and embedded systems. Results show that, this technique is more effective thermal management concepts to enable faster clock rates and increased heat dissipation at chip levels.

2. Heat Generation in Microprocessors

The basic construction unit of high performance portable/embedded processor integrated circuits is a CMOS layout, and the basic construction unit of CMOS layout is a MOS transistor. Each transistor can be turned on or off like a switch depending on the voltage difference between the gate terminal and the source terminal. Higher numbers of transistors are connected together in a particular topology to form a logic gate. Each gate has its own input signals and output signals. Figure 1-a shows the basic CMOS inverter circuit, If the input voltage has a transition from HIGH to LOW (or logic 1 to 0), and output node is LOW initially, for the inverter to perform the correct computation, the output voltage level has to transit from LOW to HIGH (or logic 0 to 1) after amount delay of time. During the low-to-high transition at output node, the load capacitance C_L has to be charged from 0 to V_{dd}. The charging path is from the power supply (V_{dd}) through the turned-on PMOS transistor to the output node, whereas the NMOS transistor is turned off. The PMOS can be modeled as a resistor when it is turned on. Thus the inverter can be simplified as a first-order RC circuit as shown in figure 1-b, where R_P is the equivalent resistance of the turned-on PMOS [3,6].

The total energy drawn from the power supply for this voltage transition is $C_L V_{dd}^2$. But the energy actually stored in the capacitor is 0.5 $C_L V_{dd}^2$ half of the total energy. Where the other half of the total energy is dissipated in the form of Joule heat in the resistor R_P. The output node may be discharged to ground if the input signal makes a low-to-high transition, thus the remaining half of the total energy is dissipated as heat in the resistor R_N as shown in figure 1-c. Therefore, every switching event as a result of computation draws some amount of energy from the power supply, and this energy is eventually transformed into heat dissipation.

During the switching period of time for input transition, for a short time both the PMOS and the NMOS are partially turned on, causing short-circuit current flowing from the supply to ground, which causes some heat generation in the CMOS circuits.

Another source of heat generation in CMOS processors systems is due to the leakage energy. CMOS transistors are not ideal switches. They still conduct some small amount of current even if they are supposed to be off; this current is called leakage current. Thus it draws energy from the power supply and dissipated as heat through the resistance in their flow path [6,7].

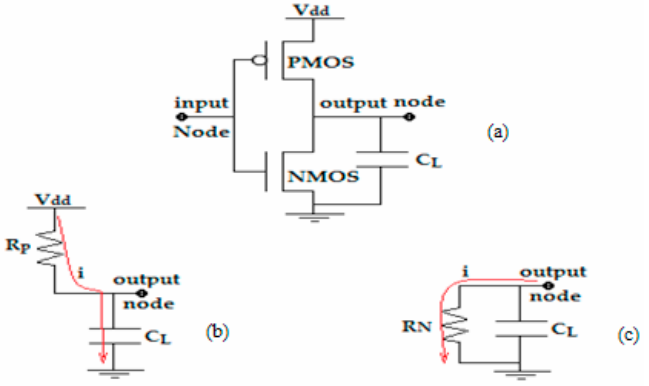


Fig. 1. (a) Basic CMOS inverter Circuit, (b) The low-to-high transition, (c) The high-to-low transition

In addition to the generated heat in CMOS transistors, Joule heating is occur in term I^2R when electrical current flows through on-chip metal interconnects that connect the transistors because the interconnects are not ideal electrical conductors and have finite amount of resistance R and hence Joule heating.

The energy consumed by the CMOS transistors is dissipated in the form of heat in the transistors and interconnects, and are eventually removed to the environment by heat transfer. The amount of heat generated or dissipated in unit amount of time is known as heat generation rate Q.

3. Dynamic Thermal Management

To avoid the costs of over designing of the thermal solution, some high performance processors use a dynamic thermal management technique that reduces the processor power consumption when the die temperature reaches its operating limit. This technique uses an on die thermal throttling clock control logic to maintain a safe operating temperature. Figure 2 shows the non-uniformity of die temperature distribution, the temperature detection method based to the hottest spot on the die to detect the maximum temperature [8].

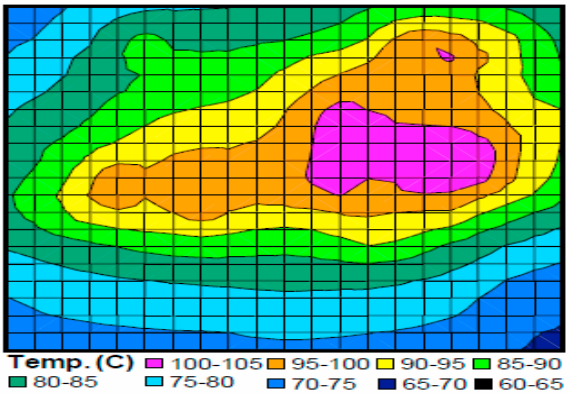


Fig. 2. Processor simulated Thermal image (example)

The CMOS inverter is the basic building block for processors design, the thermal design power of a CMOS inverter can be written as,

$$P_{total} = C_L V_{dd}^{\ 2} f + P_{channel} + P_{gate} \quad (1)$$

Where P_{total} is the total power, C_L is the switching load capacitance, V_{dd} is supply voltage, $P_{channel}$ is the channel leakage power which is proportional to V^3, and P_{gate} is the gate leakage power which is proportional to V^5. The $P_{channel}$ and P_{gate} are significantly increase for the high performance generations of process technology depends on the microprocessor architecture, and the efficiency of the power reduction techniques implemented on the chip.

The main single factor impacting power consumption is the operating voltage, to maximize power reduction; the processor operating voltage and operating frequency are reduced while servicing a thermal event. Once the frequency is reduced, the voltage transition can start performed to the execution of the application. The combination of frequency and voltage reduction results in a significantly better power/performance efficiency when servicing a thermal event [2].

Thermal management mechanism when the thermal event occurs, initiates a frequency transition event. At this time a hysteresis timer is also started to limit the frequency of transitions into and out of the thermal management state. Prior to stopping the processor clock, there is stopping of application execution, in order to lock to a new operating frequency. When the new frequency is locked, the DTM wake up the processor and returns the execution flow to the user application. If the processor still operates at maximum temperature, the processor continues executing in the low power state. When the temperature has dropped below the maximum temperature, DTM ramps the voltage and frequency back to the nominal operation point and return the processor to the nominal performance level. Figure 3 shows thermal management efficiency vs. minimum processor voltage, the most power efficient operating point is the lowest possible operating voltage and frequency while servicing a thermal event constraint [2,8].

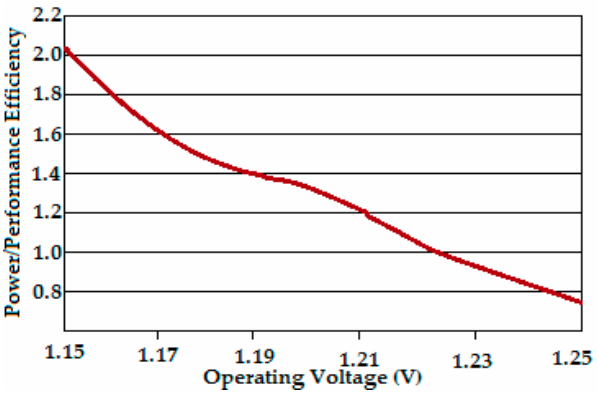


Fig. 3. Thermal management efficiency and operating voltage relationship (example)

4. The Processor Temperature Estimation

The processor temperature can be estimated based on the processor's energy input known depending on the thermal characteristics of the heat sink. The heat sink's energy input can be expressed by [9],

$$m\,\Delta T = \Delta Q = \int_{t1}^{t1+\Delta t} P_{total}(t)\,dt \tag{2}$$

Where, m is mass of heat sink, Δt is elapsed time, ΔT is heat sink's temperature increase, ΔQ is difference in input energy, and P_{total} is the total dissipated power.
The variation in processor's temperature can be given by,

$$dT = \frac{P_{total}}{m}\,dt \tag{3}$$

The energy output of the heat sink ΔQ is given by,

$$\Delta Q = \frac{T - T_o}{R}\,t = m\ \Delta T \tag{4}$$

Where, R is thermal resistance, and T_o is ambient temperature. Transforming equation 4 into Newton's law of cooling,

$$dT = -(T - T_o)\,dt \tag{5}$$

P_{total} can be determined from equations 3 & 5,

$$p_{total} = -\int_{t1}^{t1+\Delta t} m(T - T_o)\,dt \tag{6}$$

To build a simple thermal model for CMOS circuits, based on the power model above, assuming that there is no thermal interaction between processor and any other system units, and the processor inlet ambient temperature does not change [10].

For typical portable and embedded systems with heat source and heat sink, the stable temperature is the balance point where the heat generating speed should be equals to the heat dissipation speed. The higher the temperature requires the faster the heat dissipation speed. The heat generated by processor is dissipated along two paths: one to the heat sink spreader and then to ambient, and another down to the raw motherboard. The processor has different stable temperatures and affected by several factors.

- The heat generation of the processor is determined by the CPU utilization or throughput.
- The higher the velocity of dynamic thermal cooling flow, the quicker the heat dissipation from the processor to the ambient.
- The technique of thermal reduction control or thermal throttling.
- Finally, the ambient temperature affects the stable temperatures: The higher the ambient temperature, the higher the stable temperatures.

The following equation can be well used to calculate the stable temperatures,

$$T = T_o + P_{total} + \psi_{processor} \tag{7}$$

Where, $\Psi_{processor}$ is the thermal resistance from the processor to the ambient; thermal resistance is the ratio of the change of stable temperature over the change of power consumption [9,10].
The dynamic temperature changes with varying processor throughput or workload in program execution. It is given by,

$$T(t + \Delta t) = T(t) + (T_{stable} - T(t)) + (1 - e^{\frac{\Delta t}{\tau}}) \tag{8}$$

Where, τ is the time for the temperature difference to be reduced by 1/e, and can be determined by the processor temperature changes using actual physical testing or simulation overhead.

5. Thermal Throttling

The management of how a device will dispose of heat is an integral part of microprocessor design. Operating temperature rises as heat collects in a device, potentially causing damage and affecting performance.

High performance portable and embedded processors have high CPU utilization, and are typically designed to meet a specific thermal design power. The thermal throttling solution is required to dissipate the maximum power consumption of the processor, to maintain the processor below its maximum operating temperature within a safe temperature range [11].

To prevent the increasing heat from damage of processor or accidental shutdown while at high workload, the processor thermal throttling technique regulates the thermal environment by alternating between running the processor at full speed and placing the processor in a sleep state whenever the upper limits of the thermal envelope are reached. This technique will force processor to enter partially idle mode according to preset processor operating temperature. When the system senses the processor operating temperature reaching the preset value, the processor operating bandwidth will be decreased to the preset idle percentage to cool down the processor, and a sound or LED indicator can be placed to indicate that the throttling mode is working.

Obtaining real temperature readings directly from the processor, temperature sensors would be ideal. These sensors are based on analog CMOS circuit designs, and placed in one of the hot spots of the processor chip (register File). The thermal sensor TC1047A is the preferred sensor in this study. It develop an output voltage proportional to temperature with a nominal temperature coefficient of 6.25mV/°C and 10mV/°C respectively. Both temperature-to-voltage converters can sense a -40°C to +125°C temperature range while operating from a single 2.5V supply. The devices feature an offset without the need for a negative supply voltage. The extremely low operating current minimizes self-heating and maximizes battery life.

High accuracy, low operating current and small packages make this sensor ideal for a variety of applications such as high speed processors, cellular phones, consumer electronics, printers, industrial control appliances, and office equipments. Simplified schematic of the TC1047A temperature sensor is shown in figure 4. (More details about the operation of TC1047A can be found in [12].

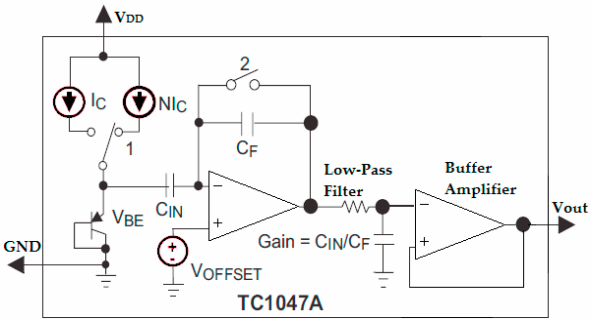


Fig. 4. Simplified schematic of the TC1047A Temperature sensor

The circuit diagram of figure 5 below can be used to measure the processors temperature and multiple locations of the system. The operational amplifier functions as an averaging circuit to provide a composite voltage output that can be used to adjust the contrast.

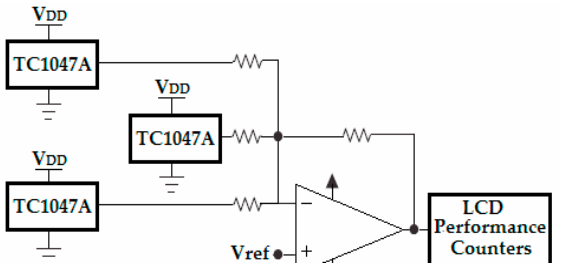


Fig. 5. The temperature measure schematic including TC1047A temperature sensor

Figure 5 has been designed, and then simulated using temperature counters monitoring tool. The sense resistors with a value of 0.01Ω are used with each TC1047A. The voltage drop measured across the sense resistor and then amplified by the current sense amplifier and sent to the labeled output of the performance counters tool. To measure the total dissipated power, the A. Thomas measurement platform is used in combined with temperature measure circuit diagram.

6. Simulation Results

Using temperature counters as a temperature monitoring tool on a PC (3.8V, 3.2GHz CPU, 2GB DDRAM Pentium IV Processor), the operating system is Windows-XP SP2. The processor supports 10 frequency-voltage pairs, from 2.2GHz 3.2 GHz. The most conservative voltage settings, range from 2.0V to 3.8V. These ranges of voltages are preferable to operate with unique corresponding frequency. Different SPEC CPU2000 benchmarks for separate instances are run. These benchmarks are able to distinguish the way a hardware device temperature is increasing with workload and the way its temperature decrease when the workload is finished. Therefore, a thermal benchmark is composed by three components as shown in Figure 6 [13].

- The range from [0-t_1) is the temperature idle mode. In this mode only the power saving mechanisms are prevented to occur.
- The range from [t_1-t_2) is a warming mode when a certain workload is executed.
- The range from [t_2-t_3) is the cooling mode for the component to reach again the idle state temperature.

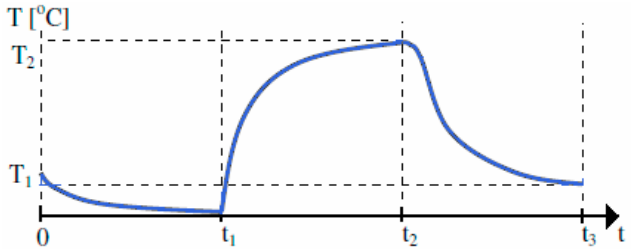


Fig. 6. The thermal benchmark behavior

SPEC CPU2000 includes two benchmark suites, CINT2000 and CFP2000, only CINT2000 are run (gzip, vpr, gcc, mcf, crafy, parser, eon, perlbmk, gap, vortex, bzip2, twolf) . Figure 7 shows temperatures of the gcc benchmarks. The normalized temperature and power for CINT2000 benchmarks are shown in figures 8 and 9 respectively.

The CINT2000 benchmarks actually achieve significant temperature reduction and power savings due to their relatively higher variability accompanied by unaffected observable of performance degradations. Thus, overall

improvement of the system remains significant and effective. The temperature and power counters of the control system observed that achieves improvements of the processor temperature reduction is high as 7.474%, and power savings is high as 7.244 for the CINT2000 benchmarks. Although these improvements for portable and embedded system applications for variable workloads are considered as a quickly-varying thermal reduction behavior.

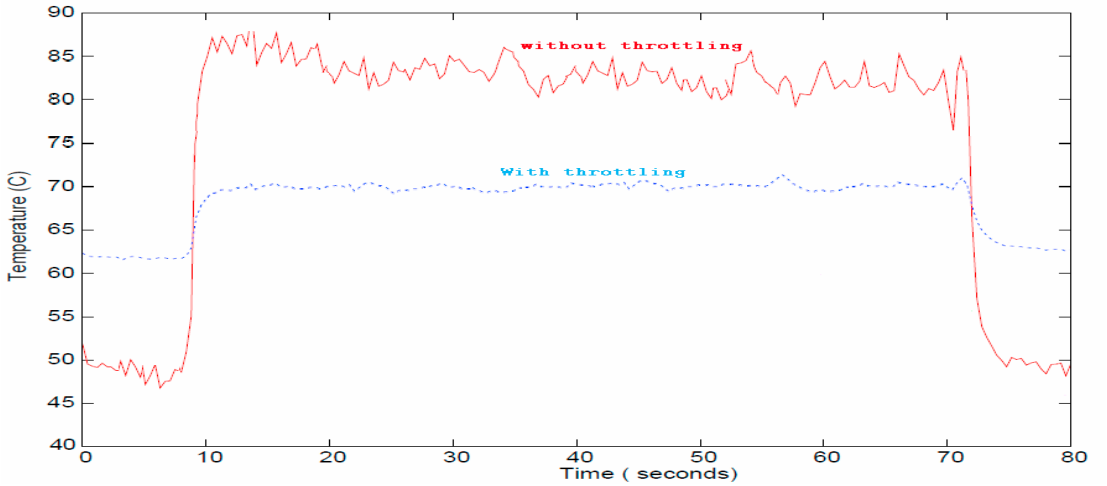
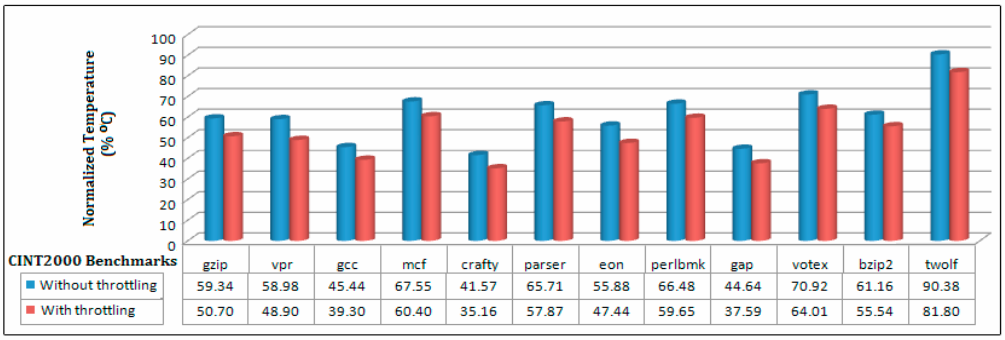
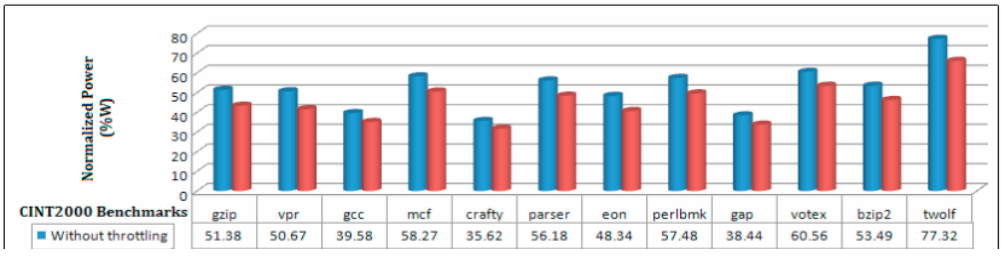


Fig. 7. Temperatures for gcc benchmark



CINT2000 Benchmarks	gzip	vpr	gcc	mcf	crafty	parser	eon	perlbmk	gap	votex	bzip2	twolf
Without throttling	59.34	58.98	45.44	67.55	41.57	65.71	55.88	66.48	44.64	70.92	61.16	90.38
With throttling	50.70	48.90	39.30	60.40	35.16	57.87	47.44	59.65	37.59	64.01	55.54	81.80

Fig. 8. The normalized temperatures for CINT2000 benchmarks



CINT2000 Benchmarks	gzip	vpr	gcc	mcf	crafty	parser	eon	perlbmk	gap	votex	bzip2	twolf
Without throttling	51.38	50.67	39.58	58.27	35.62	56.18	48.34	57.48	38.44	60.56	53.49	77.32

Fig. 9. The normalized Power for CINT2000 benchmarks

7. Conclusion

Thermal management is one of the biggest bottlenecks for high performance processor chip designers. Current processors design challenges in portable and embedded systems becoming more complex and high transistor count, both thermal management and power consumption reduction is becoming significant bottlenecks in the design process.

This paper presents the processors thermal throttling techniques to predict and characterize dynamically thermal reduction based on the power dissipation and workload variation behavior using temperature counters as a temperature monitoring tool. It develops workload-adaptive dynamic power management methods that proactively respond to the changes in application demands.

The thermal throttling technique, which is presented throughout this paper, control loop has a high progress, and can significantly improve processor temperature and power efficiency especially for portable and embedded microprocessors. Results shows that the processor temperature reduction is high as 7.474%, and power savings is high as 7.244 for the CINT2000 benchmarks.

Therefore, it is possible to integrate and use the thoughts of this technique with existing processor to study system level power and thermal issues for various high performance processors accurately.

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