On the Low-power Design, Stability Improvement and Frequency Estimation of the CMOS Ring Oscillator

Vratislav MICHAL

ST-Ericsson, 12 rue Jules Horowitz, 38019 Grenoble, France.

vratislav.michal@stericsson.com

Abstract. *In this paper, a simple method allowing optimization of the CMOS ring oscillator frequency dispersion and power consumption is presented. It is shown, that for range of tens of MHz and less, the power consumption and variation of the frequency can be considerably reduced by using 3-stage, resistively coupled ring oscillator, with minimum channel width W and large channel length L MOS transistors. In addition, a simple analysis allowing to estimate the oscillator frequency from the process and transistor parameter values is provided.*

Keywords

Ring oscillator, CMOS inverter delay, CMOS inverter chain, Frequency stability of ring oscillator.

1. Introduction

The single-ended ring oscillator is the digital oscillator, produced by cascade connecting of an odd number n of inverters in a loop. The equal delay T_i of each inverter results in the generated clock frequency [1]:

$$F_{CLK} = \frac{1}{n \cdot T} \tag{1}$$

The inverter count should be preferably either small or a prime number, in order to minimize the probability of higher harmonic signal generation [2]. The power consumption of the ring oscillator is determined by *i*) the crossconduction losses, when the inverter input voltage close to $V_{DD}/2$ make simultaneously conducting both N and PMOS, and *ii*) the capacitive losses, caused by the periodical charging/discharging of the inverters capacitances [3]:

$$P = n\frac{C\,V_{DD}^2}{T_{CLK}} \tag{2}$$

In this formula, C is the capacitance sum present in the inverter output node, V_{DD} the power supply voltage and $T_{CLK} = 1/F_{CLK}$. The power consumption P can reach high values (hundreds of μW), depending on the oscillator design.

The method allowing to decrease the power consumption P, and frequency sensitivity to V_{DD} is presented in this paper. In the 2nd section, formula allowing a rough estimation of the ring oscillator clock frequency F_{CLK} is delivered, by using linearization of the CMOS inverter. The inverter delay T is determined as the function of the transistor parameters (W/L, K_P, V_{TH}), V_{DD} and load capacitance C_{IN}. In 3rd section, we shows that contrarily to the usual design based on fast - minimum channel length (L) inverters (see *e.g.* [4]), the power consumption can be considerably lowered (namely for low clock frequencies), by using minimum channel width (W) of the MOS transistors, whereas the clock frequency setting is done by increasing the channel length L. Finally, simple method of oscillator frequency accuracy improvement is shown in section 4, based on resistively-coupled CMOS inverters.

2. Ring Oscillator Linear Analysis

The recent sub-μm CMOS process exhibits typically inverter delay in range of several picoseconds. However, the use of ring oscillator as the asynchronous clock generator usually requires the frequencies of several MHz. Generally, setting of the oscillator frequency is done in two ways:

1) Cascading of *n* inverters: results in the long inverter chain topology (Fig. 1). For instance, a 100MHz generator requires some 80 inverters in 0.5μm CMOS process, whereas 40nm CMOS process needs around 1100 gates in series. The series cascading of the inverters leads to a high quiescent current (I_Q in order of hundreds of μAs), independent on n, and potential odd harmonic generation [2]. Beside these drawbacks, the cascading technique allows to generate very sharp square wave signal, because it exploits the faster inverters available in the technology.

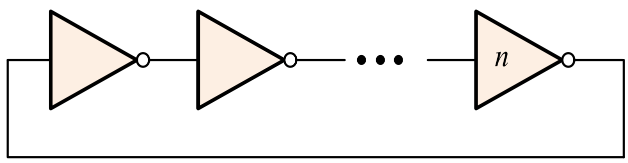

Fig. 1. Setting of the oscillator frequency by the long inverter chain.

2) **Slowing inverters by extra capacitors or RC filters** [5]: allows to decrease the count of the inverters by slowing their transient response (increasing inverter delay T). For identical clock frequency and identical inverters W and L, the power consumption is comparable with previous solution (see Tab. 1), whereas the output signal contains less high harmonics compounds (is more sinusoidal – like, see Fig. 3), and is therefore less advantageous.

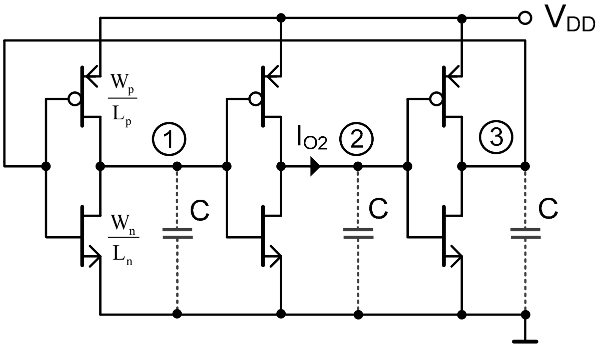

Fig. 2. Decreasing of the oscillator clock frequency by extra capacitors slowing the inverter transient responses.

An example of comparison between both methods in 0.5µm and 40nm CMOS process is shown in following table:

TYPE	0.5µm CMOS (3.6V) W_N/L_N=0.6/0.5, W_P/L_P=1.2/0.5 (µm)			40nm CMOS (1.8V) W/L_N=0.17/0.04, W/L_P=0.22/0.04 (µm)		
	n	C	P	*n*	C	P
(1)	830	-	650 µW	11k	-	275 µW
(2)	3	1.6 pF	648 µW	3	2.3 pF	225 µW

Tab. 1. Comparison of the ring oscillators designed by previously mentioned methods for F_{CLK} = 10MHz.

From this table, we can notice high power consumption, which is comparable *e.g.* with more accurate PLL generators.

2.1 Estimation of CMOS Inverter Delay

The usual expression (1) of the ring oscillator frequency, or inverter delay T available in literature [1, 3], [6-8] does not clearly highlight the relationship between the MOS transistor parameters and frequency F_{CLK}. We therefore determine here an approximate formula of the oscillator frequency, based on the inverter delay T estimation. The estimation will be done upon evaluation of the example of simulated waveforms of a 3-stages ring oscillator (Fig. 2 with C = 0) shown in Fig. 3. In this figure, we can notice three waveforms shifted by 120°, corresponding to the node voltages from schematic Fig. 2, as well as the output current I_{O2} of second inverter.

By focusing to the points where the peaks of current I_{O2} occur, we notice that the voltage rise or fall of waveform (2) is nearly linear between the intersections with the previous inverter output voltage. We also notice that these intersections are approximately at V_{THN} and $V_{DD}-|V_{THP}|$.

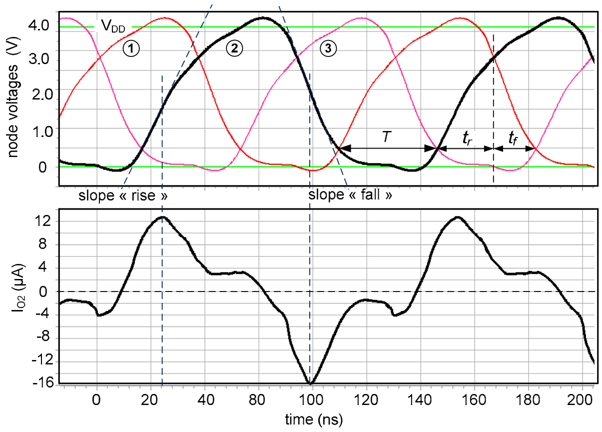

Fig. 3. Simulation example of three stage ring oscillator (0.5µm CMOS, W/L = 0.6/0.5 (µm), n = 3, k = 2 and V_{DD} = 3.6).

The rising and falling slopes (slew rates) of the node voltages can be determined from the peak currents of the P- and N-MOS and input capacitances of following inverter:

$$\frac{dV_{rise}}{dt}=\frac{I_{DP\max}}{C_{IN}}, \quad and \quad \frac{dV_{fall}}{dt}=\frac{I_{DN\max}}{C_{IN}} \tag{3}$$

where I_{DPmax} and I_{DNmax} are the peak currents. These currents can be determined from the saturated-MOS drain current formula (V_{GS} voltage at the peak current instants is close to V_{DD}):

$$\begin{aligned} I_{DN_{\max}} &= \frac{K_{PN}}{2}\frac{W}{L}\left(V_{DD}-V_{THN}\right)^2 \\ I_{DP_{\max}} &= k\frac{K_{PP}}{2}\frac{W}{L}\left(V_{DD}-|V_{THP}|\right)^2 \end{aligned} \tag{4}$$

In this equation, constant k is the scaling ratio between P- and N-MOS channel width ($W_P = k{\cdot}W_N$, L_P=L_N). The C_{IN} capacitance in (3) is the sum of the passive capacitor C and input inverter capacitance. At $V_{DD}/2$, this capacitance can be expressed as:

$$C_{IN}=C+C_{ox}\left(W_P\cdot L_P+W_N\cdot L_N\right) \tag{5}$$

which, for C = 0, can be rewritten as:

$$C_{IN}=C_{ox}W\cdot L\left(k+1\right) \tag{6}$$

The rise and fall times between V_{THN} and $V_{DD}-|V_{THP}|$ (see Fig. 3) can be then expressed as:

$$\begin{aligned} t_r &= \frac{\Delta V}{I_{DP_{\max}}/C_{IN}}=\frac{2C_{ox}L^2\left(k+1\right)\left[V_{DD}-\left(V_{THN}+|V_{THP}|\right)\right]}{kK_{PP}\left(V_{DD}-|V_{THP}|\right)^2} \\ t_f &= \frac{\Delta V}{I_{DN_{\max}}/C_{IN}}=\frac{2C_{ox}L^2\left(k+1\right)\left[V_{DD}-\left(V_{THN}+|V_{THP}|\right)\right]}{K_{PN}\left(V_{DD}-V_{THN}\right)^2} \end{aligned} \tag{7}$$

The expected high variation of the ring oscillator frequency allows us to suppose V_{THN} = $|V_{THP}|$ = V_T with negligible error. This assumption results in summing of t_r and t_f into a simplified form:

$$T = \frac{2C_{ox}L^2(k+1)(V_{DD}-2V_T)}{(V_{DD}-V_T)^2}\left(\frac{1}{k\cdot K_{PP}}+\frac{1}{K_{PN}}\right) \quad (8)$$

Here, $T = t_r + t_f$ approximate delay of one inverter, loaded by the inverter with identical W and L sizes. The clock frequency of the oscillator using n-inverters chain can therefore be determined from the above mentioned *Eq*.(1):

$$F_{CLK} = \frac{1}{n\cdot T} \quad (9)$$

From equation (8), we can notice that the ring oscillator frequency F_{CLK} does not depend on the transistor W, but is strongly dependent on the L, V_{DD} and process parameters.

3. Power Consumption Optimization

The power consumption of the ring oscillator can be found from (2) (crossconduction looses not included):

$$P = \frac{nC_{ox}W\cdot L(k+1)V_{DD}^2}{n\dfrac{2C_{ox}L^2(k+1)(V_{DD}-2V_T)}{(V_{DD}-V_T)^2}\left(\dfrac{1}{kK_{PP}}+\dfrac{1}{K_{PN}}\right)} = \frac{W}{L}\cdot\frac{V_{DD}^2(V_{DD}-V_T)^2}{2\cdot(V_{DD}-2V_T)\left(\dfrac{1}{kK_{PP}}+\dfrac{1}{K_{PN}}\right)} \quad (10)$$

This equation might indicate that the power consumption does not depend on n. This could be right if L can be chosen arbitrarily. In reality, channel length L given by clock frequency (9) depends also on the parameters n and k. The (10) can be therefore rewritten into more comprehensive form:

$$P = \alpha\frac{W}{L(n,k...)} \quad (11)$$

where α corresponds to the constant remaining terms in (11). From this equation, we notice that the lower power consumption can be obtained by minimizing the W/L ratio. As already mentioned, the transistor W does not influence the oscillator frequency (9) and should be therefore set to the technological minimum.

On the contrary, the transistor channel length L is conditioned by the oscillator frequency (8), (9), and should be maximized. However, it follows from (8) and (9), that maximal value of L can be obtained for minimal $n = 3$ and $k = 1$.

Except to an increase of the inverter input capacitance C_{IN}, the increased channel length considerably lowers the inverter output and crossconductance currents (*i.e.* state when both N- and P-MOS transistors conduct simultaneously). This actually increases the inverter delay (thanks to the slow charging of the following input capacitance C_{IN}), without an excessive increase of the quiescent current I_Q. It is to be noted, that the power consumption gain is more important for longer channels length (*i.e.* for lower frequencies F_{CLK}). For higher frequencies, where resulting L is low, additional current limitation needs to be applied in the inverter. Moreover, in order to maintain low overall consumption of the oscillator, a current limitation in the output buffer is also important, in order to limits the cross-conduction losses during slow transitions phases of oscillator output voltage (see circuit shown in Fig. 6 or inverters mentioned in ref. [1]).

3.1 Simulation Example

The demonstration of presented low-power design methodology is shown here by a simulation of an oscillator example designed in 0.5µm and 40nm CMOS process for F_{CLK} = 10MHz. For 0.5µm CMOS, the transistor dimensions were found by several hand-made iterations as W/L = 0.5/10.8 (µm). As mentioned above, optimal parameters $n = 3$ and $k = 1$ were chosen (*i.e.* schematics from Fig. 2 with $C = 0$). The simulated quiescent current corresponding to this configuration is 4.1µA (14.8µW, Tab. 2.), which can be compared to 180µA obtained with solution 1) or 2) (Tab. 1). By considering K_{PP} = 18µA/V^2, K_{PN} = 75µA/V^2, V_T = 0.6V and C_{OX} = 3.5·10^{-2}F/m^2, and by using Eq.(8), we obtain the inverter delay T = 30ns corresponding to the clock frequency F_{CLK} = 11.1MHz (9).

As we can see on the simulated example of 0.5µm version (Fig. 5), a slight asymmetry (DC) of the generated output voltage occurs, due to identical N- and P-MOS W/L (compare Fig. 3 (k = 2) with Fig. 5 (k = 1)).

0.5µm CMOS (3.6V) $n = 3, k = 1$			40nm CMOS (1.8V) $n = 3, k = 1$		
W/L	I_Q	P	W/L	I_Q	P
10.8/0.5	4.1 µA	14.8 µW	0.17/9.2	1.7 µA	3 µW

Tab. 2. Power consumption of the optimized ring oscillators designed for F_{CLK} = 10MHz (compare with Tab. 1).

4. Frequency Stability Optimization

The accuracy of the ring oscillator frequency is naturally affected by V_{DD}, temperature and process parameters variations. For instance, the *min*/*max* frequency of the oscillator designed in previous section 3.1 is 5.6/17.5 MHz over −25 to 125ºC temperature and 2.5 to 4.8V V_{DD} voltage range, and 8.9/11 MHz over process slow/fast corners (for V_{DD} = 3.6V, Temp = 27ºC). The main factor related to the frequency variation is the quadratic term in (4) resulting in the quadratic relationship between the inverter input voltage slopes dV_{rise}/dt and dV_{fall}/dt (3) and V_{DD} voltage. However, as the voltage difference between V_{TH} and V_{DD}/2 increase linearly with V_{DD}, the slopes dV_{rise}/dt and dV_{fall}/dt should also increase linearly. This effect causes the standard inverter to have negative V_{DD} voltage vs. propagation delay relationship.

Ref. [1] suggests interesting solution, which rely on the oscillator composed of the classical inverters (*i.e.* those having negative propagation delay vs. V_{DD} voltage tendency), and the constant-current biased inverters, having positive propagation delay vs. V_{DD} voltage tendency. By this way, the overall propagation delay of the oscillator can be partially V_{DD} insensitive.

An alternative solution presented here relies on the structure, having the slopes dV_{IN}/dt of the inverter input voltages linearly dependent on V_{DD}. This means that all inverters have identical - low V_{DD} propagation delay sensitivity. This feature can be achieved by the oscillator scheme shown in following Fig. 4. Here, the linear V_{DD} vs. input voltage slope dependence is mediated by the large-value coupling resistances, placed between the inverters. As we can deduce from Fig. 4, the input voltage slopes dV_{IN}/dt are determined by the input capacitance given by (6), coupling resistances, but also by the non-negligible substrate capacitance of the integrated resistances. Unfortunately, the effect of distributed substrate capacitance makes the hand-made calculation complicated, in spite the good models accuracy.

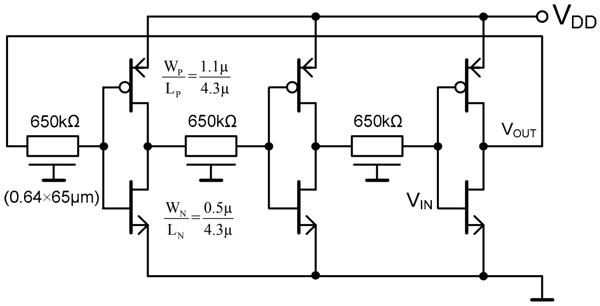

Fig. 4. Ring oscillator with low frequency dispersion (low V_{DD} sensitivity, F_{CLK} = 10MHz, I_Q = 6.7μA).

The F_{CLK} sensitivity improvements provided by Fig. 4 schematic is demonstrated here by transient simulation. We notice significantly lower *min/max* frequency variation: 8.4/11.6 MHz (over V_{DD} and temperature range), and slightly higher variation of slow/fast process corners: 8.5/11.8 MHz (caused mainly by the used unsalicided N+ poly resistor process variation). When focusing on the V_{DD} variation only, the ratio of *min/max* frequency was simulated as 0.84 in 2.5 to 4.8V range.

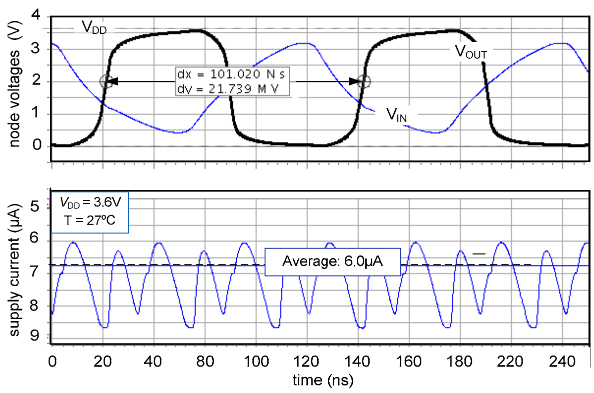

Fig. 5. Simulation example of Fig. 4 three-stage resistively coupled ring oscillator with low V_{DD} sensitivity.

On the simulated waveforms shown in Fig. 5, we can observe one fast output-node waveform (compare to Fig. 3), able to drive low input capacity buffer, and "slow" inverter input voltage V_{IN}. We also notice small increase of quiescence current to 6.7μA, caused by higher crossconductance looses. The possible crossconductance looses of the oscillator output buffer can also be limited, *e.g.* by an inverter with current limitation (Fig. 6. or inverters in [1]), advantageous namely for oscillator with slow transition rates output voltage (*i.e.* oscillator Fig. 2).

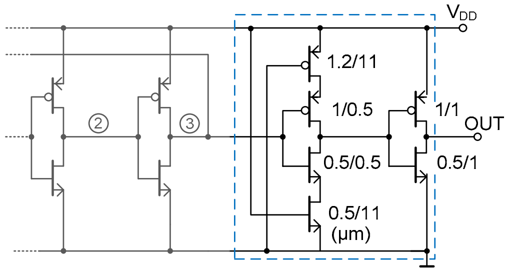

Fig. 5. Low C_{IN} output buffer with crossconduction current limitation. The crossconductance current is limited by the large *L* transistor at the V_{DD}/GND power rails.

5. Conclusion and Comments

The analysis shown in this paper allows to obtain an informative relation between the ring oscillator clock frequency and the basic design parameters. However, due to the large dispersion of the generated frequency, the value spreading should be verified by the corner analysis simulation. The presented power consumption and accuracy optimization brings benefits mainly in the application where the oscillator is used as the asynchronous clock generator in *e.g.* low quiescent current sleep mode. A simulation example of the 10MHz ring oscillator shown here yields the power consumption reduction by 40 times, and more than half of the frequency spreading, compared to the standard design techniques.

References

[1] G. JOVANOVIC, M. STOJCEV. A method for improvement stability of a CMOS voltage controlled ring oscillators. ICEST 2007, vol. 2, pp. 715-718, 2007.

[2] SASAKI, N. Higher harmonic generation in CMOS/SOS ring oscillators. *IEEE Transactions on Electronic Devices*, Vol. 29, 1982.

[3] SEGURA, J., HAWKINS, C.F. CMOS electronics, how it works, how it fails (ch. 4). *Book IEEE edition*, ISBN 0-471-47669-2, 2004.

[4] MATSUDA, T. et al. A combined test structure with ring oscillator and inverter chain for evaluating optimum high-speed/low-power operation. *In proceeding of International Conference on Microelectronic Test Structures,* 2003.

[5] Generating Switched-Capacitor Filter Clock, *Application note 724* of MAXIM (www.maxim-ic.com, 2001).

[6] ADLER, V., FRIEDMAN, E. G. Delay and power expressions for a CMOS Inverter Driving a resistive-capacitive load. *IEEE International Symposium on Circuits and Systems ISCAS '96*, 1996.

[7] JEPPSON, K.O. Modeling the influence of the transistor gain ratio and the input-to-output coupling capacitance on the CMOS inverter delay. *IEEE Journal of Solid-State Circuits*, Vol. 29, 1994.

[8] SAKURAI, T. CMOS inverter delay and other formulas using α-power law MOS model. *In proceeding of IEEE conference on Computer-Aided Design ICCAD-88*, 1988.