TI SimpleLink™ CC3000 Module – Wi-Fi 802.11b/g Network Processor

FEATURES

- **Wireless network processor**
  - **IEEE 802.11 b/g**
  - **Embedded IPv4 TCP/IP stack**
- **Best-in-class radio performance**
  - **TX power: +18.0 dBm at 11 Mbps, CCK**
  - **RX sensitivity: –88 dBm, 8% PER, 11 Mbps**
- **Works with low MIPS and low-cost MCUs with compact memory footprint**
- **FCC, IC, and CE certified with a chip antenna**
- **HW design files and design guide available from TI**
- **Integrated crystal and power management**
- **Small form factor: 16.3 mm × 13.5 mm × 2 mm**
- **Operating temperature: –20°C to 70°C**
- **Based on TI's seventh generation of proven Wi-Fi solutions**
- **Complete platform solution including user and porting guides, API guide, sample applications, and support community**

APPLICATIONS

- **Home automation**
- **Home security**
- **Connected appliances**
- **Smart energy**
- **M2M communication**

DESCRIPTION

The TI CC3000 module is a self-contained wireless network processor that simplifies the implementation of Internet connectivity (see Figure 1). TI's SimpleLink™ Wi-Fi solution minimizes the software requirements of the host microcontroller (MCU) and is thus the ideal solution for embedded applications using any low-cost and low-power MCU.

The TI CC3000 module reduces development time, lowers manufacturing costs, saves board space, eases certification, and minimizes the RF expertise required. This complete platform solution includes software drivers, sample applications, API guide, user documentation, and a world-class support community.

For more information on TI's wireless platform solutions for Wi-Fi, go to TI's Wireless Connectivity wiki (www.ti.com/connectivitywiki).

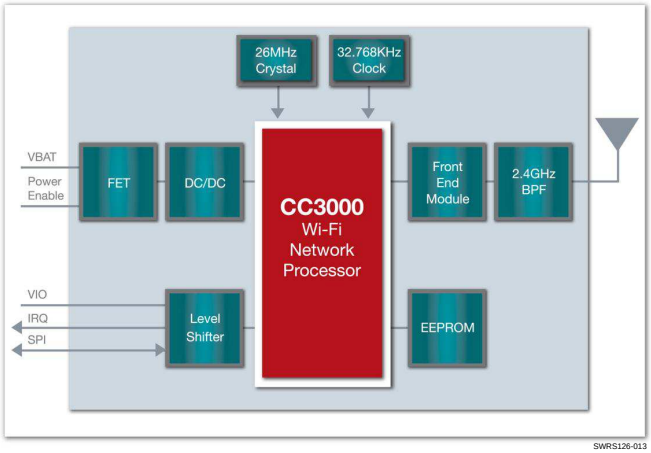

Figure 1. Wi-Fi Solution for TI SimpleLink CC3000 Module

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FEATURES

WLAN

- 802.11b/g integrated radio, modem, and MAC supporting WLAN communication as a BSS station with CCK and OFDM rates from 1 to 54 Mbps in the 2.4-GHz ISM band
- Auto-calibrated radio with a single-ended 50-Ω interface enables easy connection to the antenna without requiring expertise in radio circuit design.
- Advanced connection manager with seven user-configurable profiles stored in an NVMEM allows automatic fast connection to an access point without user or host intervention.
- Supports all Wi-Fi security modes for personal networks: WEP, WPA, and WPA2 with on-chip security accelerators
- Smart Config™ WLAN provisioning tools allow customers to connect a headless device to a WLAN network using a smart phone, tablet, or PC.

Network Stack

- Integrated IPv4 TCP/IP stack with BSD socket APIs enables simple internet connectivity with any microcontroller, microprocessor, or ASIC.
- Supports four simultaneous TCP or UDP sockets
- Built-in network protocols: ARP, ICMP, DHCP client, and DNS client enable easy connection to the local network and to the Internet.

Host Interface and Driver

- Interfaces over 4-wire serial peripheral interface (SPI) with any microcontroller, or processor at clock speed up to16 MHz
- Low footprint driver provided for TI MCUs and easily ported to any processor or ASIC
- Simple APIs enable easy integration with any single-threaded or multi-threaded application.

System

- Works from a single, preregulated power supply or connects directly to a battery
- Separated I/O voltage rail allows flexible integration with host processors
- Ultra-low leakage shut-down mode with current <5 µA
- Integrated clock sources

EEPROM

- Integrated EEPROM stores firmware patch, network configuration, and MAC address.
- Programmable through an I2C interface or over APIs from the host, allowing over-the-air firmware upgrades
- Can store 5 KB of user data accessible to the host application, enhancing the MCU NVM

PACKAGE INFORMATION

Module Outline

For the PCB layout of your applications, TI recommends the footprint shown in Figure 2.

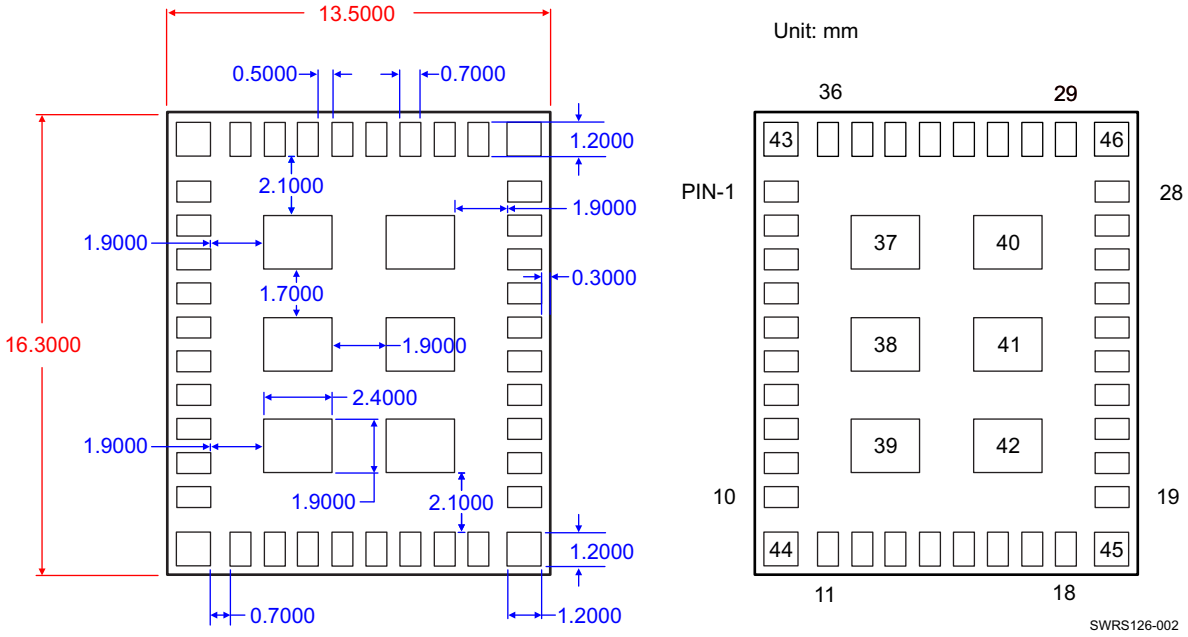

Figure 2. CC3000 Module Footprint and Pinouts

Pin Description

Table 1 describes the CC3000 module pins.

Table 1. CC3000 Module Pins Description

Pin	Signal Name	Type	State at Reset	State After Reset	Voltage Level	Description
1	GND	GND	—	—	—	Ground
2	Reserved_1	—	—	—	1.8 V	Reserved. Connect to test point.
3	NC	—	—	—	—	Not connected
4	Reserved_2	—	—	—	1.8 V	Reserved. Connect to test point.
5	WL_EN2(1)	I	Hi-Z	—	—	Mode setting
6	WL_RS232_TX(2)	O	Hi-Z	Force 1	1.8 V	RS232 test-mode signal (1.8-V logic). Connect to test point. Serial connection for CC3000 radio tool.
7	WL_EN1	I	Hi-Z	—	—	Mode setting
8	WL_RS232_RX(2)	I	Hi-Z	PU	1.8 V	RS232 test-mode signal (1.8-V logic). Connect to test point. Serial connection for CC3000 radio tool.
9	GND	GND	—	—	—	Ground
10	GND	GND	—	—	—	Ground
11	GND	GND	—	—	—	Ground
12	SPI_CS	I	Hi-Z	PU	VIO_HOST	Host interface SPI chip-select (CS)
13	SPI_DOUT	O	Hi-Z	PU	VIO_HOST	Host interface SPI data out
14	SPI_IRQ	O	Hi-Z	Force 1	VIO_HOST	Host interface SPI interrupt

(1) Connect WL_EN1 to WL_EL2 for proper operation of the module.
(2) Leave unconnected in function module.

Table 1. CC3000 Module Pins Description (continued)

Pin	Signal Name	Type	State at Reset	State After Reset	Voltage Level	Description
15	SPI_DIN	I	Hi-Z	PU	VIO_HOST	Host interface SPI data in
16	GND	GND	—	—	—	Ground
17	SPI_CLK	I	Hi-Z	PD	VIO_HOST	Host interface SPI clock
18	GND	GND	—	—	—	Ground
19	VBAT_IN	Power	—	—	V_{BAT}	Power supply input, 2.7 to 4.8 V
20	GND	GND	—	—	—	Ground
21	EXT_32K	—	—	—	—	Not used. Connect to ground.
22	GND	GND	—	—	—	Ground
23	VIO_HOST	Power	—	—	VIO_HOST	VIO host supply voltage
24	Reserved 3	—	—	—	—	Reserved. Connect to test point.
25	GND	GND	—	—	—	Ground
26	VBAT_SW_EN	I	—	—	VIO_HOST	Module enable. Connect to host GPIO.
27	SDA_EEPROM(3)	I/O			1.8 V	I2C data line from EEPROM
28	SDA_CC3000(3)	I/O			1.8 V	I2C data line from the CC3000 module
29	SCL_EEPROM(4)	I/O			1.8 V	I2C clock line from EEPROM
30	SCL_CC3000(4)	I/O			1.8 V	I2C clock line from the CC3000 module
31	GND	GND	—	—	—	Ground
32	GND	GND	—	—	—	Ground
33	GND	GND	—	—	—	Ground
34	GND	GND	—	—	—	Ground
35	RF_ANT	RF	—	—	—	WLAN antenna port, 50-Ω single
36	GND	GND	—	—	—	Ground
37	GND	GND	—	—	—	Ground
38	GND	GND	—	—	—	Ground
39	GND	GND	—	—	—	Ground
40	GND	GND	—	—	—	Ground
41	GND	GND	—	—	—	Ground
42	GND	GND	—	—	—	Ground
43	GND	GND	—	—	—	Ground
44	GND	GND	—	—	—	Ground
45	GND	GND	—	—	—	Ground
46	GND	GND	—	—	—	Ground

(3) Connect SDA_EEPROM and SDA_CC3000 through a 0-Ω resistor.
(4) Connect SLC_EEPROM and SLC_CC3000 through a 0-Ω resistor.

ESD PERFORMANCE

Because electrostatic discharge (ESD) can damage this integrated circuit, TI recommends handling all integrated circuits (ICs) with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision ICs can be more susceptible to damage because very small parametric changes can cause devices not to meet their published specifications.

Table 2 describes the ESD performance.

Table 2. ESD Performance

HDM(1)	CDM(2)
1000 V	500 V

(1) JEDEC ESD HBM spec JS-001-2012
(2) JEDEC ESD CDM spec 22C101E

MODULE SPECIFICATIONS

Absolute Maximum Ratings

Parameters	Pin	Min	Max	Unit
VBAT_IN	19	–0.5	+6.0	V
VIO_HOST	23	–0.5	+4.6	V
I2C and WL_RS232	27, 28, 29, 30, 6, 8	–0.5	+2.1	V
SPI interface	12, 13, 14, 15, 17	–0.5	+4.6	V
VBAT_SW_EN	26	–0.3	+6.0	V
Storage temperature range	–	–40	+85	°C

Recommended Operating Conditions

Rating	Condition		Sym	Min	Max	Unit
Operating ambient temperature				–20	+70	°C
VBAT_IN				2.7	4.8	V
VIO_HOST supply voltage				1.8	3.6	V
SPI interface						
High-level input voltage	VIO_HOST =	1.8 to 1.95 V	VIH	VIO_HOST x 0.65		V
		1.95 to 2.7 V		1.6		
		2.7 to 3.6 V		2		
Low-level input voltage	VIO_HOST =	1.8 to 1.95 V	VIL		VIO_HOST × 0.35	V
		1.95 to 2.7 V			0.7	
		2.7 to 3.6 V			0.8	
Input voltage			VI	0	3.6	V
Output voltage	Active state		VO	0	VIO_HOST	V
Input transition rise or fall rate			$\Delta t/\Delta v$		5	ns/V
VBAT SW EN						
High-level input voltage			VIH	1.1	5.5	V
Low-level input voltage			VIL	0	0.4	V

Power Consumption

Parameters	Test Conditions	Typ	Max	Unit
802.11b TX current	VBAT = 3.6 V Tamb = +25°C Po = 18 dBm, 11 Mbps L = 2048 bytes tdelay (idle) = 40 µs	260	275	mA
802.11g TX current	VBAT = 3.6 V Tamb = +25°C Po = 14 dBm, 54 Mbps L = 2048 tdelay (idle) = 40 µs	190	207	mA
802.11bg RX current	VBAT = 3.6 V	92	103	mA
Shut-down mode	VBAT = 3.6 V VBAT_SW_EN = 0 V		5	µA

WLAN Transmitter RF Characteristics

(TA = +25°C, VBAT = 3.6 V)

Characteristics	Condition (Mbps)	Min	Typ	Max	Unit
Maximum RMS output power	1		18.3		dBm
	2		18.2		
	11		18.1		
	6		17.0		
	9		17.0		
	18		17.0		
	36		15.5		
	54		14.0		
In-band power variation				±1	
Transmit center frequency accuracy				±20	ppm

Receiver RF Characteristics

(TA = +25°C, VBAT = 3.6 V)

Characteristics	Condition (Mbps)	Min	Typ	Max	Unit
Sensitivity	1 DSSS		–97.5		dBm
	2 DSSS		–95.0		
	11 CCK		–89.0		
	6 OFDM		–91.0		
	9 OFDM		–91.0		
	18 OFDM		–87.0		
	36 OFDM		–81.0		
	54 OFDM		–75.0		
Maximum input level	802.11b			–10	dBm
	802.11g			–20	

SPI HOST CONTROLLER INTERFACE

The SPI is the primary host interface to the CC3000 module.

The SPI interface contains the five-line, master and slave communication model shown in Figure 3.

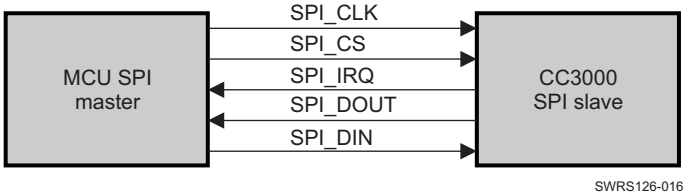

Figure 3. SPI Host Connectivity

Table 3 highlights the CC3000 SPI pin names and functions.

Table 3. SPI Line Description

Pin Name	Description
SPI_CLK	Clock (0 to 16 MHz) from host to slave
SPI_CS(1)	CS (active low) signal from host to slave
SPI_DIN	Data from host to slave
SPI_IRQ(2)	Interrupt from slave to host
SPI_DOUT	Data from slave to host

(1) SPI_CS selects a CC3000 module, indicating that a master wants to communicate to the device.
(2) SPI_IRQ is a dual-purpose slave to the master direction line: in SPI IDLE state while no data transfer is active, driving SPI_IRQ low indicates to the master that the CC3000 module has data to pass to it; driving SPI_IRQ low following SPI_CS deassertion indicates that the CC3000 module is ready to receive data.

SPI Timing

Figure 4 shows the SPI timing sequence.

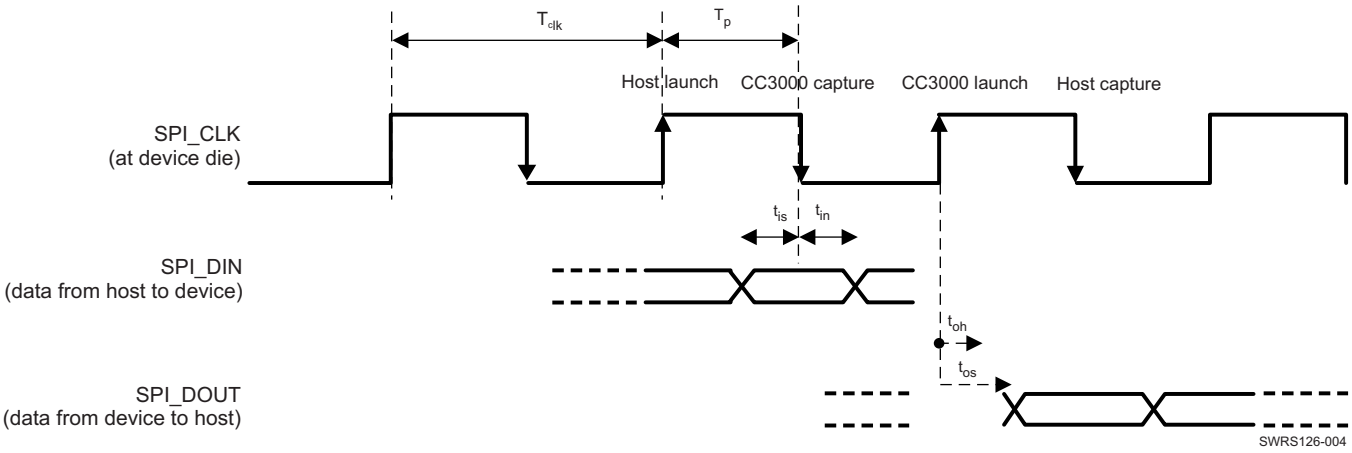

Figure 4. SPI Timing Sequence

Table 4 lists the SPI timing parameters.

Table 4. SPI Timing Parameters

Symbol	Parameter[1][2]	Min	Max	Unit
T_{clk}	Clock period	62.5		ns
T_p	High pulse width (including jitter and duty cycle)	25[3]	37.5[3]	ns
t_{is}	RX setup time; minimum time in which data is stable before capture edge	5		ns
t_{ih}	RX hold time; minimum time in which data is stable after capture edge	5		
t_{os}	TX setup propagation time; maximum time from launch edge until data is stable		10.2	
t_{oh}	TX hold propagation time; minimum time of data stable after launch edge	3		
C_L	Capacitive load on interface		20	pF

(1) The SPI_CS signal is considered to be asynchronous.
(2) In this example, launch is on the rising edge, and capture is on the falling edge. The opposite scheme can be configured.
(3) 40% to 60% DC (valid for the minimum clock period)

POWER-UP SEQUENCE

Figure 5 demonstrates the wake-up sequence of the CC3000 module.

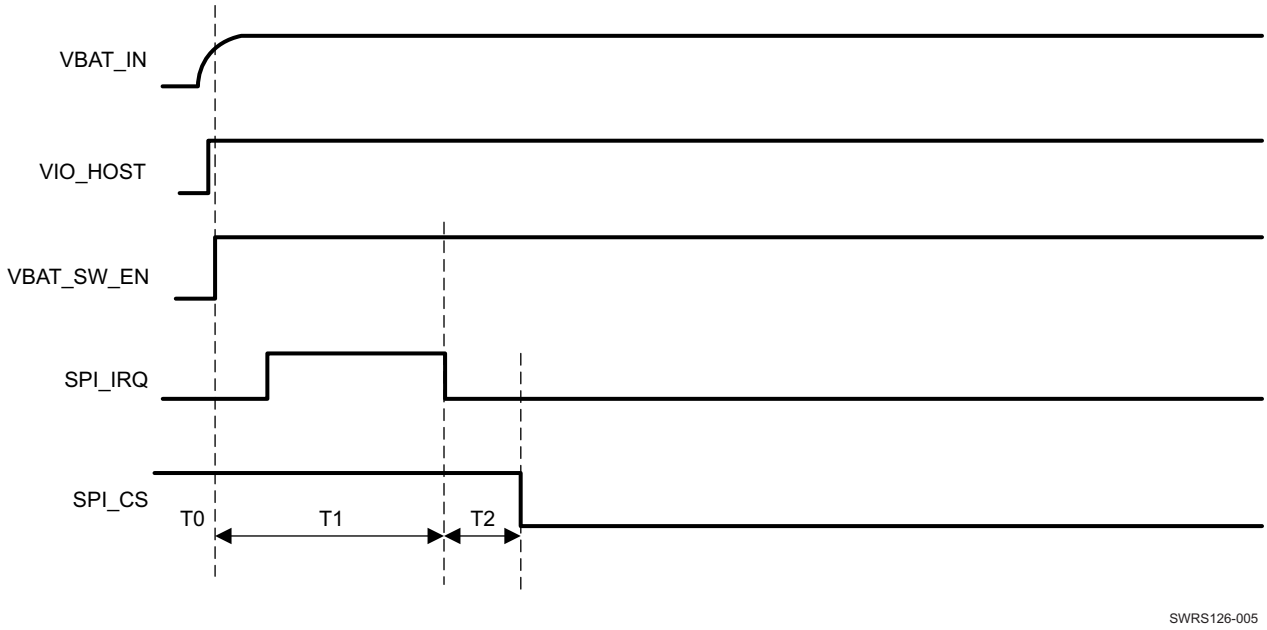

Figure 5. CC3000 Module Power-On Sequences

NOTE

- VBAT_IN and VIO_HOST must be available before VBAT_SW_EN is asserted.
- At wake-up time (T1): The CC3000 module powers up after SPI_IRQ changes state to LOW. T1 is approximately 53 ms.
- At T2: The normal master SPI write sequence is SPI_CS low, followed by SPI_IRQ low (CC3000 host), indicating that the CC3000 core module is ready to accept data. T2 duration is approximately 7 ms.

CC3000 Enable Pins Configuration

Table 5 describes the CC3000 mode of operation based on the enable (EN) pins setting.

Table 5. CC3000 EN Pins Configuration

Mode	State
Test mode(1)	WL_EN1: Leave disconnected. WL_EN2: Connect to ground.
Functional mode(2)	WL_EN1 and WL_EN2 are shorted together.

(1) For CC3000 radio tool operation
(2) For normal operation

Test Mode Serial Interface

The CC3000 module contains a dedicated WLAN serial interface to connect to the CC3000 radio tests tool, an external PC-based software test utility, during development and evaluation phase (see Figure 6 and Table 6). The CC3000 radio test tool utility can be obtained from the CC3000 TI wiki (www.ti.com/connectivitywiki).

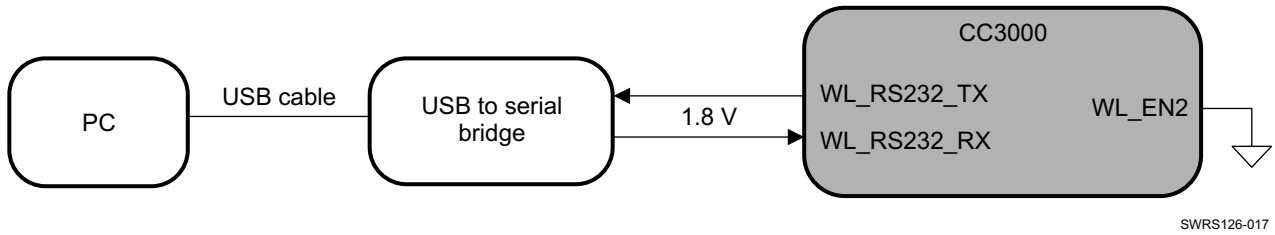

Figure 6. CC3000 Test Mode Serial Interface Connection

Table 6. CC3000 Test Mode Debug Interface Description

Signal Name	Function
WL_RS232_TX	Connection with CC3000 radio PC-based software(1)
WL_RS232_RX	

(1) WL_EN2 pins must be grounded while bringing up the CC3000 radio tool.

SURFACE MOUNT INFORMATION

The CC3000 module uses a flat shield cover designed for a fully automated assembly process. For baking and reflow recommendations, follow MSL level 4 found in the JEDEC/IPC Standard J-STD-20b. The classification temperature (T_C) for the module is 250°C.

MECHANICAL INFORMATION

Module Mechanical Outline

Figure 7 shows the mechanical outline for the CC3000 module.

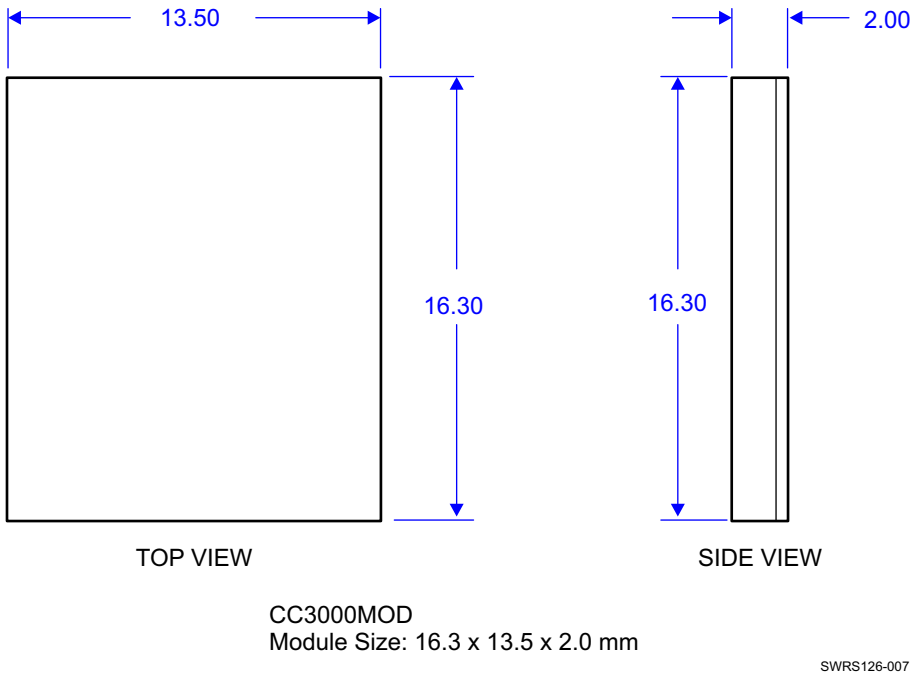

Figure 7. CC3000 Module Mechanical Outline

Package Marking

Figure 8 shows the CC3000 module package marking.

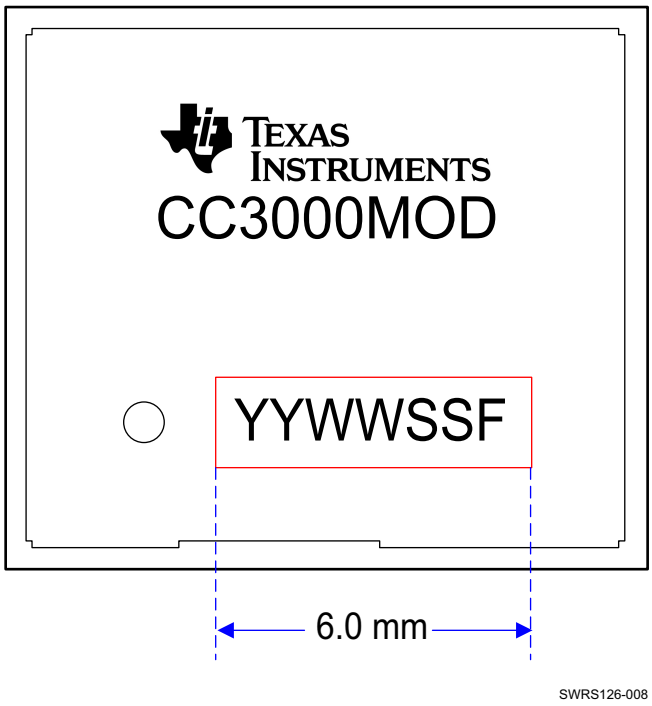

Figure 8. CC3000 Module Package Marking

Table 7 defines the marking code.

Table 7. Package Marking Definitions

Code	Definition
YYWWSSF	Date
YY	Year (for example, 2012 = 12)
WW	Week (01 through 53)
SS	Serial number from 01 to 99 to match manufacturer lot number
F	Reserved for internal use

Ordering Information

Table 8 lists the CC3000 module part numbers.

Table 8. CC3000 Module Part Numbers

Order Number	Description
CC3000MOD	CC3000 module, 44 modules per tray
CC3000MODR	CC3000 module reel, 1200 modules per reel

REFERENCE SCHEMATICS AND BILL OF MATERIALS

Figure 9 shows the schematics for the CC3000 to host reference design.

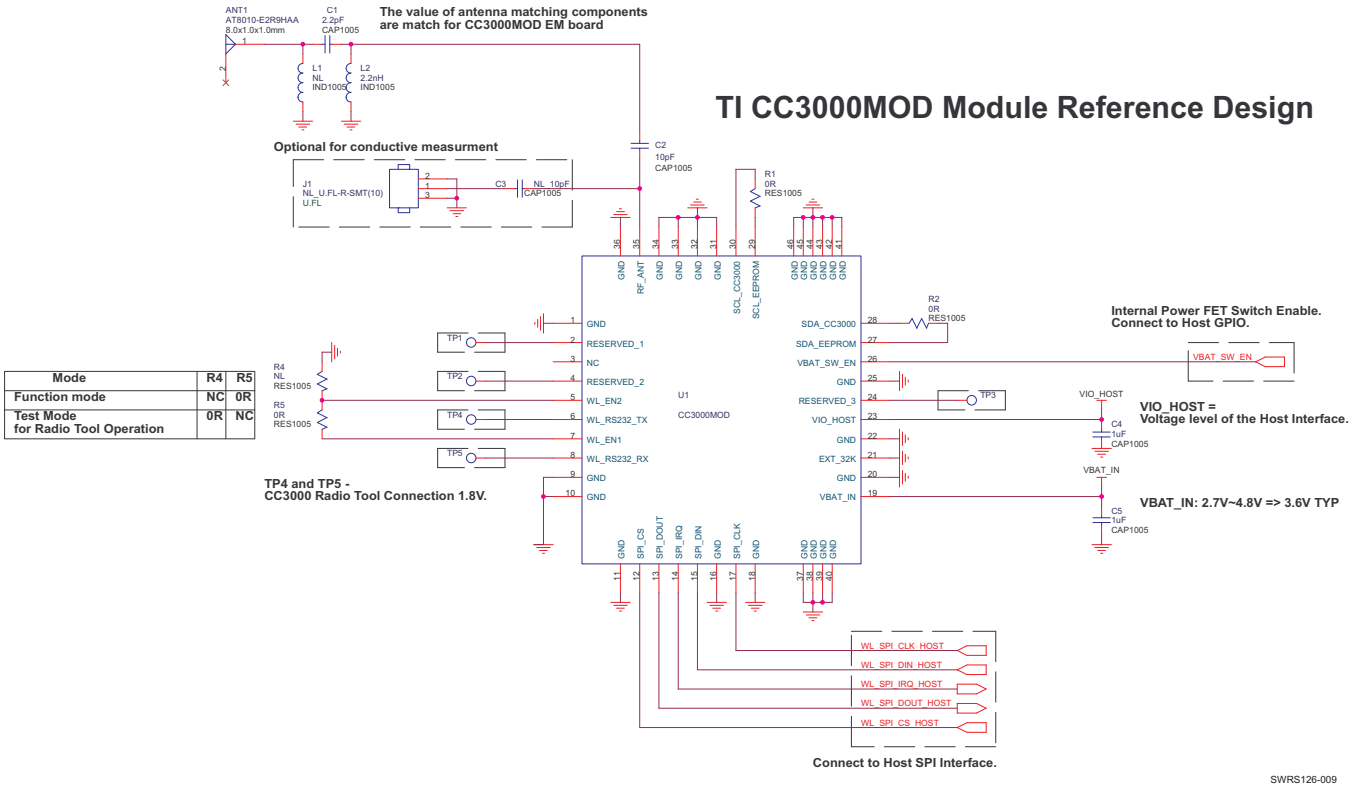

Figure 9. CC3000 Module to Host Reference Design

NOTE

For flexibility, VIO_HOST supports both cases in which the VBAT and VIO voltages of the MCU can be the same or different.

Table 9 lists the bill of materials.

Table 9. Bill of Materials

Part Reference	Description	Manufacturer	Manufacturer PN
ANT1	2.4-GHz chip antenna, 8.0 × 1.0 mm	ACX	AT8010-E2R9HAA
C1	C0402, 2.2 pF	Walsin	0402N2R2C500LT
L2	L0402, 2.2 nH	ACX	HI1005-1C2N2SMT
C2(1)	C0402, 10 pF	Walsin	0402N100J500LT
C4, C5(1)	C0402, 1 µF	Murata	GRM155R60J105KE19D
R1, R2, R5(1)	R0402, 0R	Walsin	WR04X000PTL
J1	RF coaxial U.FL, SMD	Hirose	U.FL-R-SMT-1(10)

(1) Any component with similar values can be used.

DESIGN RECOMMENDATIONS

This section describes the layout recommendations for the CC3000 module, RF trace, and antenna.

Antenna

The ACX ceramic antenna is mounted on the CC3000 EVM board with a specific layout and matching circuit for the radiation test conducted in FCC, CE and IC certifications. Figure 10 shows the location of the antenna on the EVM board as well as the RF trace routing from the CC3000 module.

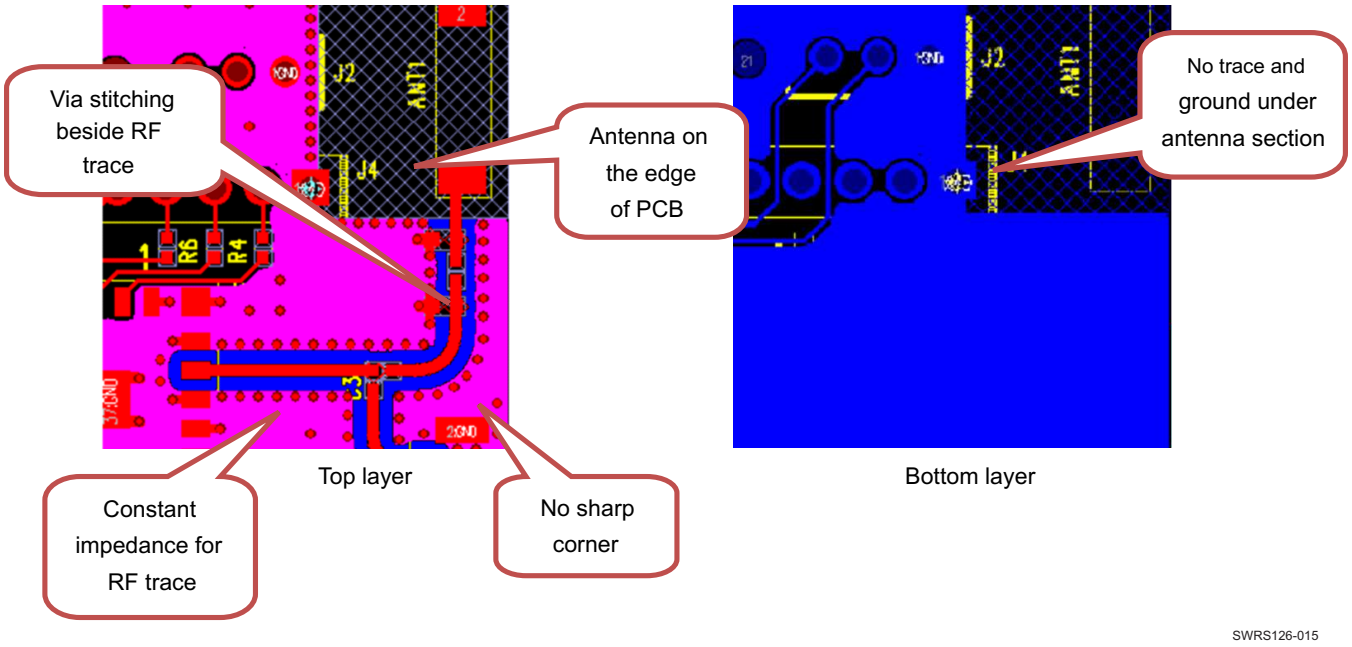

Figure 10. RF Trace and Antenna Design for PCB Layout

Module Layout Recommendations

Observe the following module layout recommendations (see also Figure 11):

- Have a solid ground plane and ground vias under the module for stable system and thermal dissipation.
- Do not run signal traces underneath the module on a layer where the module is mounted.
- Signal traces can be run on a third layer under the solid ground layer and beneath the module mounting layer.

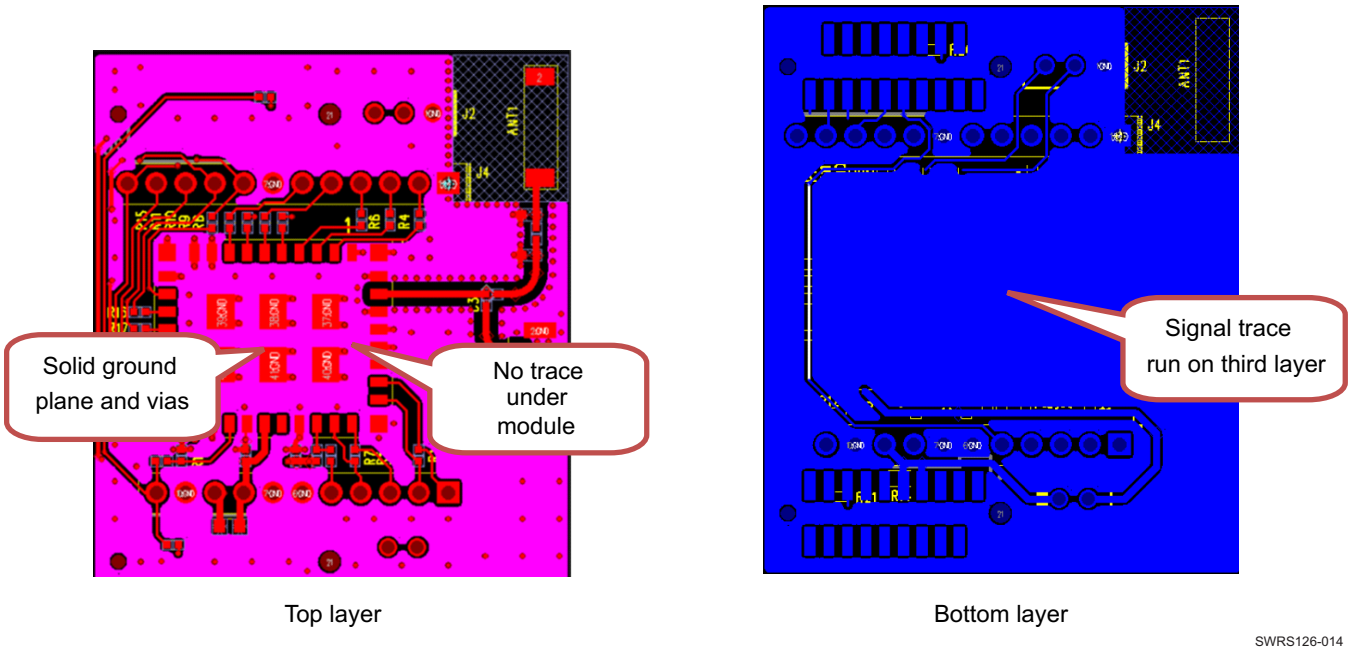

Figure 11. Module Layout

RF Trace and Antenna Layout Recommendations

Observe the following recommendations for RF trace and antenna layout (see also Figure 10):

- RF traces must have 50-Ω impedance (microstrip transmission line).
- RF trace bends must be gradual with a maximum bend of approximately 45 degrees and with trace mitered. RF traces must not have sharp corners.
- There must be no traces or ground under the antenna section.
- RF traces must have via stitching on the ground plane beside the RF trace on both sides.
- RF traces must be as short as possible. The antenna, RF traces, and the module must be on the edge of the PCB product in consideration of the product enclosure material and proximity.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC3000MOD	NRND			46	84	TBD	Call TI	Call TI	-20 to 70		
CC3000MODR	NRND			46		TBD	Call TI	Call TI	-20 to 70		
CC3000MODT	NRND			46		TBD	Call TI	Call TI			
CC3000YFVR	NRND	DSBGA	YFV	126	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		CC3000	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265