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19 August 1981

USSR Report

CYBERNETICS, COMPUTERS AND AUTOMATION TECHNOLOGY

(FOUO 19/81)

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USSR REPORT

CYBERNETICS, COMPUTERS AND AUTOMATION TECHNOLOGY

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INTEGRATED CIRCUITS

SM-3 AND SM-4

INTEGRATED CIRCUITS

UDC 621.396

ANALOG AND DIGITAL INTEGRATED CIRCUITS

Moscow ANALOGOVYYE I TSIFROVYYE INTEGRAL'NYYE SKHEMY in Russian 1979 (signed to press 5 Apr 79) pp 2-5, 331-335.

[Annotation, foreword, conclusion and table of contents from book "Analog and Digital Integrated Circuits", by Sergey Viktorovich Yakubovskiy, Nikolay Arsen'yevich Barkanov, Boris Petrovich Kudryashov, Lev Ionovich Nissel'son, Mikhail Nikiforovich Topeshkin and Lyubov' Petrovna Chebotareva, Izdatel'stvo "Sovetskoye radio", 68,000 copies, 336 pages]

[Text] Annotation

Analog and digital integrated circuits. S. V. Yakubovskiy, N. A. Barkanov, B. P. Kudryashov. Edited by S. V. Yakubovskiy. Moscow. Sovetskoye Radio, 1979, 336 pages, illustrations (Design of radio-electronic apparatus with integrated circuits).

This is a survey of the basic series of analog and digital integrated circuits produced by the electronics industry. Cited are:methods for their manufacture parameters and characteristics, and the operating principles of the basic components. Trends are shown in the development of logic circuits. Data is given on microprocessors and the special features of their application. Factors that affect the integrated circuit reliability are covered; special features in using integrated circuits in designing radio-electronic apparatus are described; and recommendations are given on preventing integrated circuit failures for various external effects and technological operations.

This book should be useful to engineers working in the design of radio-electronic apparatus and interested in problems of selecting integrated circuit components and in the special features of their application, as well as to students of respective specialties.

The book contains 73 tables, 186 illustrations and 64 items in the bibliography.

Foreword

The basic directions for the development of the national economy for 1976-1980, determined by the 25th party congress, stated that among the main ways to increase the efficiency of production was the problem of "improving decisively the quality

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of all types of manufactured products; expanding the assortment of goods; and increasing the production of new types of products that meet modern requirements"[1]. Its solution is impossible without further development of electronics that provides not only for the creation of complex automated systems for the control of production processes, but also for the development of new in principle products for mass consumption. The expansion of the area of application of electronic devices is one of the special features of scientific technical progress at the modern stage.

Starting with the sixties, the development of electronics began with the appearance and rapid development of integrated circuits (IC). Integrated circuits make it possible to create modern complex electronic devices of acceptable sizes and weights, and guarantee their high reliability. The widest application of IC was in the design of digital devices.

To a constantly greater degree, the properties and characteristics of IC determine the technical characteristics of computers. Modern digital integrated circuits are complex products that realize the functions of entire blocks and units of computers. It is this that was responsible for the appearance of an entirely new direction in electronics -- the creation of microprocessors. While simple digital IC were the basis for designing third generation computers, the assimilation in production of microprocessors that have IC with a higher functional complexity and universality made it possible to organize the processing of digital signals in a new way and, therefore, to hope for a wide introduction of digital methods of processing data into various areas of technology (even those where previously the use of electronics produced no essential effect). Fourth generation computers are being created on the basis of microprocessor sets (4 to 5 individual housings).

Three stages may be conditionally singled out in the development of technology and circuitry. The first stage was the development of basic integrated circuits that perform simple logic functions (AND-NOT, OR-NOT, AND-OR-NOT etc., with each series, as a rule, containing triggers). At this stage, IC with 10 to 50 elements were created.

The second state was the development of more complicated functionally completed units (counters, registers. decoders, half-adders etc.) with from 50 to 500 elements. Because of such new circuits, the functional composition of the previously developed series was constantly expanded.

The third stage was the development of complex functional devices with an integration level of from 500 to 10,000 elements on one chip. This stage arrived at the beginning of the 10th Five-Year Plan period. The third stage circuits were used to create pocket engineering calculators with wide calculation possibilities on the basis of preliminary programing of the problem being solved.

In the process of developing digital integrated circuit electronics, along with bipolar circuits, there were developed and widely applied unipolar MOS [metal oxide semiconductors]: of the p and n types, complementary MOS [KMOP], MOS with nitride insulation (MNOP) and several others. It is the digital circuits with MOS transistors that made it possible to increase the number of elements in a chip to 10,000 and design such complex circuits as main memories (OZU) with a large data volume, memories with random access and permanent memories.

The experience of using the entire variety of methods to manufacture the IC obtained during the past 10 years confirmed the convenience of applying the high technical characteristics of bipolar type TTL [Transistor Transistor logic] and ESL [Emitter connected logic] circuits, as well as MOS type circuit elements. The Single System of Electronic Computers (YeS EVM) were created by the combined efforts of CMEA member countries, as well as was a broad family of small computers and calculators (from the simplest school calculators with four arithmetic operations to universal calculators -- with programing which may be used in scientific research.

The past 10-year period also gave apparatus developers a new basis for an analog component: a large assortment of universal operational amplifiers, comparators, analog-digital and digital-analog converters, voltage stabilizers, switches, as well as a set of low, intermediate and high frequency amplifiers. The use of analog IC made it possible to simplify the adjustment of devices, increase their reliability and accuracy and, in many cases, eliminate necessary servicing.

In recent years, the creation of apparatus on the basis of IC without housings with the common sealing-in of units became an independent direction. This method made it possible to obtain high wiring density and reduce the size and weight of special apparatus.

The domestic electronics industry manufactures a great number of modern digital and analog microcircuits that become the component basis of modern radio-electronic apparatus (REA) for industrial purposes.

The pledge of high reliability of (REA) is the correct application of the microcircuits and the observance of their operating modes; violation of these conditions, however, because of insufficient knowledge of their technical properties, electrical parameters and operating modes, results in failures most frequently.

The purpose of this book is to provide the basic technical characteristics of digital and analog microcircuits, describe methods for their manufacture and the functional composition of the series, as well as to draw attention to the special features of using IC in developing radio electronic apparatus and to recommend the reliable manufacture of microcircuits and the reliable installation of the apparatus.

The material cited in the book is based on the results of correlating the experience in developing and using integrated microcircuits.

The authors express their deep gratitude to professor B. F. Vysotskiy, doctor of technical sciences, B. N. Fayzulayev, candidate of physical-mathematical sciences, Ye. I. Gal'perin, G. A. Podol'skiy, V. I. Kotikov and V. L. Shilo, candidates of technical sciences, who participated actively in discussing the content and structure of the book, and who made valuable comments on the material content and its arrangement. The authors are also grateful to V. N. Bulanova and V. A. Ushibyshev for their help in the preparation and makeup of the manuscript.

The authors request that remarks and suggestions on improving the book be directed to: Moscow, 101000, Main Postoffice, box 693, Izdatel'stvo "Sovetskoye Radio".

<div align="right">The Authors</div>

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Conclusion

Microelectronics is developing very rapidly. In 1977-1978, new technological directions were assimilated, new microcircuit memories and microprocessors using MOS transistors of the p and n types, bipolar injection circuits (I^2L) and transistor-transistor logic circuits using Schottky diodes were developed.

A number of permanent memories using MOS transistors and a number of microprocessor sets were developed during the preparation and publication of this book.

Of interest is a new memory -- the IC 556RT4. This is a 1024 bit permanent memory with the possibility of single-stage programing by the user. Made with TTL components with Schottky diodes it makes it possible to obtain an address access time of 90 nanoseconds using 0.5 milliwatt/bit.

IC K535RYe1 and K505 RYe3 4096 bit memories were developed using p type MOS transistors. These memories can be programed by order cards. The IC K535RYe1 has a 1.7 microsecond access time and uses 0.12 milliwatts/bit. The IC K505RYe3 has an access time of 1.5 microseconds and uses 0.25 milliwatts/bit. The circuit input interfaces with a TTL circuit through a 133LA15 circuit, while the output interfaces directly with a TTL circuit.

The IC K568RYe1, with full address decoding output amplifiers and an "IC access" control circuit was created using MOS transistors. The IC program is also implemented by order cards. The circuit has a large capacity (as compared to previously mass-produced permanent memory units). It has 16,384 bits (2048x8), uses 0.021 milliwatts/bit, its data readout time is 0.8 microseconds and the circuit output interfaces with TTL circuits.

Of great interest are IC memories K573RR11-K573RR14 with data erasing by means of ultraviolet rays that provides for long data storage when the power source is disconnected. The microcircuit has a data capacity of 4096 bits with various memory organizations: two K573RR11 and K573RR12 circuits have a memory organization of 512x8 bits and differ in functional purposes of leadouts, K573RR13 and K573RR14 have a memory organization of 1024x4 and differ in functional purposes. It has 10 reprograming cycles and the data storing time is 10,000 hours.

Microprocessor sets series K581, K536, K584, K582 and K588 were also developed and introduced in recent years.

The K536 series of the microprocessor set is made with p type MOS and consists of 13 microcircuits that provide the following functions: arithmetic-logic devices (K536Ik1 and K536Ik9); microprogram devices (K536IK2 and K536IK8); input-output control devices (K536IK3, K536IK4 and K536IK5): voltage to code converter (K536IK6); channel selector control device (K536IK7). Moreover, the sets include two power amplifier circuits (K536UI1 and K536UI2) and a cycle pulse oscillator circuit (K536GP1).

The series K581 microprocessor set is made of n type MOS and consists of five microcircuits implementing the following functions: arithmetic-logic devices (K581IK1, K581IK1A)*;

*Circuit K581IK1 with index A has a cycle time $\geqslant$ 600 nanoseconds -- without the index $\geqslant$ 400 nanoseconds.

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operation control (K581IK2, K581IK2A); microprogram memory units (K581RU1, K581RU1A); instruction storage units (K581RU2, K581RU2A), as well as a program memory unit to implement operations of expanded arithmetic and operations with a "floating" decimal point (K581RU3 and K581RU3A).

Series K582 and K584 microcircuits are used to build four-stage parallel microprocessors with injection logic (I^2L). The 588IK1 microprocessor program control device was developed with complementary MOS.

Recently, new analog microcircuits were also developed. They include: the K157UD1A,B medium power operational amplifiers with a maximum output current of up to 300 milliamperes; the quick-acting K574UD1 operational amplifier with a speed of voltage rise of up to 50 volts/microsecond; and the K551U1D1A,B precision operational amplifiers.

The number of comparators increased by the following microcircuits: 5975A1 operating on ESL logic and 597SA2 compatible with TTL logic. The type 140UD13 preamplifier was developed with an input impedance of not less than 50 megohms.

The microcircuit series intended for TV and radio reception was supplemented by the K174UN8 power amplifier with a two-watt output power, and the K174UN9 power amplifier with a power output of up to seven watts. The following TV devices were developed and assimilated in series production: the K174UP1 -- brightness signal amplifier; the K174UR3 -- amplifier-limiter; the K174KhA3 -- noise suppressor in sound data channels; the K174KhA1 -- detector of the red-blue color signal discriminator.

The set of semiconductor analog-digital converters [ATsP] expanded further. Thus, the following devices have been developed: a ten-stage ATsP with MOS transistors type 572PA1 with a multiplier, compatible with TTL circuits, and a 12-stage ATsP with MOS transistors type 594PA1 compatible with TTL circuits. A switching series was supplemented by 16-channel MOS switches with types 590KN1 and 591KN1 decoders, compatible with TTL logic and, finally, power sources for integrated circuits are being developed further. Integrated voltage stabilizers, types 142YeN3 and 142YeN4, were developed with an external voltage divider and an output current of up to one ampere.

The development rates of domestic microelectronics are such that in several years, the integrated circuits considered in this book, logic, as well as analog, will change considerably and a part of the reference material will lose its value. However, the basic conclusions of the authors that the high potential reliability of integrated circuits, built-in in their development and production, must be preserved in the development, production and operation of radio-electronic apparatus, and will remain unchanged. If the authors are able to impress this conception on the reader, they will consider their problem solved.

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Foreword

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TERMINOLOGY IN MICROELECTRONICS AND CLASSIFICATION OF INTEGRATED CIRCUITS

Moscow ANALOGOVYYE I TSIFROVYYE INTEGRAL'NYYE SKHEMY in Russian 1979 (signed to press 5 Apr 79) pp 6-17

[Chapter 1 from book "Analog and Digital Integrated Circuits", by Sergey Viktorovich Yakubovskiv, Nikolay Arsen'yevich Barkanov, Boris Petrovich Kudryashov, Lev Ionovich Nissel'son, Mikhail Nikiforovich Topeshkin and Lyubov' Petrovna Chebotareva, Izdatel'stvo "Sovetskoye radio", 68,000 copies, 336 pages]

[Text] Chapter 1

Terminology in microelectronics and classification of integrated circuits

1.1. Introduction

Microelectronics is a developing field of electronics Basically, it is the creation of an integrated element base used to develop apparatus. The term integrated electronics combines the "element," as well as the "apparatus" microelectronics. Many concepts in the field have still not established themselves firmly; therefore, questions of terminology in Russian, as well as in many foreign languages are fairly complex. In 1969, the International Electrotechnical Commission (MEK) issued the second supplement to publication 147-0 (1966) [2] in which, for the first time, terminology was presented in the field of integrated circuits. The supplement included the definition of several of the most common terms such as microelectronics, microcircuit, integrated microcircuit etc.

In our country, the first attempts to regularize terms and definitions were attempted in 1967 when a norm "Integrated microcircuits. Terminology" was issued. The lack of status of this document made it impossible to recommend it as compulsory. In connection with the considerable expansion of the use of integrated circuits, the necessity arose of a government standard on terminological questions in the field of microelectronics which was developed on the basis of the above-mentioned norm and the MEK publication and, in 1971, it was approved by the USSR Gosstandart [3]. GOST 17021-71 included 16 terms and along with general terms such as integrated microcircuit, semiconductorintergrated microcircuit, there were also given single-valued definitions for parts of integrated circuits (for example, substrate, housing).

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Terms whose definitions were given in the above-mentioned GOST were widely used in technical documents. However, the development of microelectronic means, the increase in the wiring density and in the number of elements on one chip had already led, in 1973, to the necessity of reworking this GOST for the purpose of correcting it and introducing new terms. In 1975, this work was completed by the approval of GOST 17021-75 [4].

Below are given the terms as per GOST 17021-75, their definitions and the synonyms of these terms which are widely used in production and in technical literature.

1.2.1. Integrated Microcircuits, Elements, Components

An integrated circuit (IC) is a microelectronic article that fulfills a certain function of converting and processing signals and has a high packing density of the electrically connected elements (or elements and components) and chips. This article is considered a single whole from the standpoint of the requirements of tests, acceptance, delivery and operation.

In abbreviated form, integrated microcircuits are called IMS. The synonym of an integrated microcircuit is the term integrated circuit or, still simpler, microcircuit. Of all the indicated terms, integrated circuit (IC) is the most frequently used. It has two subordinate terms, whose description is given by the above-mentioned GOST. These are concepts of an element of an integrated circuit (or simply element) and component of an integrated circuit (or simply component).

An element of an integrated circuit means the part of the IC that realizes the function of some simple electroradio element (for example, transistor, diode, resistor, capacitor). This part is inseparable from the IC chip (or its substrate). The element cannot be separated from the IC as an independent article; therefore, it cannot be tested, packed and operated. Examples of integrated elements are: a film resistor in a hybrid IC and an integrated transistor in an IC semiconductor.

An integrated circuit component also means a part of an IC that realizes the function of some electroradio element. However, before assembly this part was an independent article in special packing (complementing article). In principle, a component may be separated from a manufactured IC. Examples of integrated components are: a transistor without a housing or a ceramic capacitor in a hybrid IC.

1.2.2. Design Elements

In developing technical documentation for IC or in preparing descriptions of IC designs, writers of the indicated documents must frequently use such terms as housing, substrate, board, wafer, chip, as well as some special terms that determine special features of the internal structure of the IC.

The IC housing is the part of the IC structure intended to protect it from external effects and to connect it to external electrical circuits by leadouts (IC are packed in the housing). The types and sizes of the housings are also subject to government standardization (see GOST 17467-79 [4]).

The IC substrate is an intermediate product intended for elements of hybrid and film IC, interelement and (or) intercomponent connections, as well as contact pads to be applied to it.

The IC board is part of the substrate (or the entire substrate) of the hybrid (or frequently film) integrated circuit, to whose surface the film elements of the IC, the interelement and intercomponent connections and contact pads are applied.

The semiconductor wafer is an intermediate product of semiconductor material (usually it is a round thin disk) used to make IC semiconductors. It should be noted that in IC production this term is used not only for the initial intermediate product, but also for a plate with elements of semiconductor microcircuits formed on it (therefore, this term is used during the entire technological process from its beginning to the cutting of the group article into individual chips).

IC chips are the parts of the wafer obtained after it is cut (usually they form a network in the shape of equal rectangles), in the volume and on the surface of which are formed elements of the semiconductor microcircuit, interelement connections and contact pads.

A contact pad, present in any IC, no matter what its technological or functional features are, is a metallized pad on the plate or on the chip intended to connect contact leadouts and integrated circuits, as well as to monitor its electrical parameters and modes.

An integrated circuit without a housing is a term which recently acquired great importance because such circuits are used widely in microassemblies and microcircuits. While in the usual IC the housing serves to protect against external effects, the IC without a housing has no such protection of its own (at least, from mechanical effects). For connection to external electrical circuits, an IC without a housing must have its own leadouts and its full protection is provided by the housing of the device in which this IC is installed.

The leadout of an IC without a housing is a conductor connected electrically to the contact pad of the chip and mechanically to its surface. The main purpose of the leadout is to provide an electrical contact to one of the circuits of the IC without a housing when it is connected to external electrical circuits. Leadouts of the IC without a housing carry a considerable part of the heat. Leadouts of IC without a housing may be hard (round, columnar or beam-shaped). Hard leadouts may be used for mechanical fastening of an IC without a housing, without pasting it.

1.2.3. Simple and Complex IC

Until recently there was no decisive concept of the complexity of integrated circuits in literature, either abroad or domestically. When defining the term "large-scale integrated circuits" (BIS), an attempt was made to use, as the basis, the quantitative factor as well as the factor of the functional complexity of the microcircuit. In the first case, suggestions were made to define the BIS as a circuit containing 50, 100 or 10,000 circuit elements. For example, to define

a "large digital circuit" an attempt was made to use an elementary digital switch as a counting unit. In this case, it was considered that a "large" circuit must have no less than 100 digital switches. Concepts of "small," "medium" and "large" scale integration began to penetrate domestic leterature from abroad. However, deprived of numerical definitions, these concepts in each individual case, expressed only the subjective concepts of the author. In the seventies, following this tradition, in scientific literature, the terms "very large integrated circuit," "superlarge integrated circuit" and even "colossal integrated circuit" appear.

Supporters of defining BIS,depending upon its functional complexity, proposed dividing the circuits into four integration levels: elementary, circuit, subsystem level and finally, system level.

The study of all the proposals led to the idea that a quantitative factor must be used as a basis for a definition that defines precisely the quantity of the elements in the microcircuit chip or housing. GOST 17021-75 defined the term, "degree of integration of the integrated circuit," as an indicator of the degree of complexity of the IC, characterized by the number of elements and components. The degree of integration is defined here by formula $K = lgN$, where K is the coefficient defining the degree of automation, rounded to the nearest largest integer, while N is the number of elements and components in the IC. In accordance with this formula, an integrated circuit of the first degree of integration is called an IC containing up to 10 elements and components inclusive. An IC of the second degree of integration contains from 11 to 100 elements and components inclusive correspondingly, IC with 101 to 1000 elements and components inclusive should be called IC of the third degree of integration. Similarly IC with elements from 1001 to 10,000 or from 10,001 to 100,000 are IC of the fourth and fifth degrees of integration.

When designing electronic apparatus and selecting the elements, the so-called packing density of the elements in the integrated circuit is of great importance. By packing density is meant the ratio of the number of elements and components of the integrated circuit to its volume (without taking into account the volume of the leadouts).

1.2.4. Microassemblies and Microunits

GOST 17021-75, besides using terms with a direct relation to integrated circuits gives, in the form of reference material, a whole series of terms related to the field of application of IC. Such terms belong to the concept of microelectronics. Here it is defined as the field of electronics that spans the problems of research, design, manufacturing and the use of microelectronic products with a microelectronic product meaning an electronic device with a high degree of integration.

The term "microassembly" has several synonyms used in technical literature and documentation, but the definition of this term was not always given clearly. Thus, for example, before 1975 "microassembly" meant a microcircuit consisting of various elements and integrated circuits. The synonymsfor microassembly may be the terms used in literature such as: hybrid, integrated functional unit (GIFU), large integrated functional unit (BIFU), a large hybrid integrated circuit (BGIS) and a hybrid large integrated circuit (GBIS).

GOST 17021-75 defined the microassembly term as a microelectronic article that fulfills a certain function and consists of elements, components and integrated circuits (with and without housings), as well as other electroradio elements, in various combinations, developed and manufactured by developers of concrete radio-electronic apparatus for improving its miniaturization indicators. The GOST does not define a microassembly as an article with or without a housing, i.e., a micro-assembly may or may not have its own housing. Thus, a microassembly is not classified by the GOST by its complexity.

A microunit is a   microelectronic article which, besides micro-assemblies, may contain integrated circuits and components. Finally, the miniaturization level term of a microelectronic article characterizes the quantitative measure of the effect of using the totality of technical solutions, directed to the full utilization of the advantages obtained from the reduction in volume, weight and power used by the apparatus.

Indicators of the REA [Radio-electronic apparatus] miniaturization level are: REA meeting the modern technical standard of microelectronic articles; other articles used in REA meeting the modern level of miniaturization; efficiency of comprehensive miniaturization of apparatus; technical compatibility of "noninte-grated" articles of electronic equipment, and electric equipment with integrated circuits.

1.3. IC Classification

Depending upon the manufacturing technology, integrated circuits may be semi-conductor, film or hybrid. GOST 17021-75 gives the following definitions for these three varieties of IC.

A semiconductor integrated circuit is called an IC all of whose elements and inter-element connections are made in the volume and on the surface of the semiconductor. The semiconductor integrated circuit may also be called a semiconductor micro-circuit.

Sometimes the semiconductor integrated circuit is called a "solid" (or solid-body) circuit. This term found its way into domestic literature due to unqualified translations from the English*. GOST 17021-75 defines this term as inadmissible.

A film integrated circuit (or film circuit) whose elements and interelement con-nections are made in the form of films is called an IC. This film and thick film IC are variations of technical designs.

The difference between thin film and thick film IC may be quantitative and quali-tative. Integrated circuits with a film thickness of up to 1 micron belong to thin film IC conditionally while integrated circuits with film thickness greater than 1 micrometer belong to thick film IC. Qualitative differences are determined

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*Solid state electronics (English) -- semiconductor electronics.

by the manufacturing technology of the films. Elements of thin film IC are applied to the substrate, as a rule, by thermal-vacuum precipitation and cathode spraying, while elements of thick film IC are made primarily by silk screening with subsequent burning in.

Finally, hybrid integrated circuits (equivalent term -- hybrid microcircuits) are IC containing, besides elements, simple and complex components (for example, chips of semiconductor IC). A particular case of hybrid IC is a multichip IC (a totality of several IC without housings on one substrate).

Depending upon their functional purpose, integrated circuits are divided into two basic categories -- analog and digital.

Analog integrated circuits (analog microcircuits) are IC intended to convert and process signals that change in accordance with the continuous function law. A particular case of analog IC is an IC with a linear characteristic (linear microcircuit).

Digital integrated circuits(digital microcircuits) are IC used to convert and process signals expressed in a binary or other digital code. A variation of the digital microcircuit definition is the term logic microcircuit (operations with a binary code are described by logic algebra).

As a rule, analog and digital IC are developed and manufactured by manufacturing enterprises in the form of a series. Each series is characterized by the degree of completeness. A series contains several IC of distinctive types which, in their turn, may be divided into rated types.

According to GOST 17021-75, a series of integrated circuits contains a totality of IC which can implement various functions, but have a single design-technological form and are intended to be used in combination. As a rule, the composition of a promising series is being expanded with time.

IC that have concrete functional purposes and their conditional designations are called rated types of integrated circuits. By a type of integrated circuit is meant a totality of rated types of IC that have concrete functional purposes and their conditional designations.

1.4. System of Conditional IC Designations

The entire diversity of manufactured integrated circuits according to the adopted conditional designation system is divided into three groups: semiconductor, hybrid and others. Film IC, which are presently manufactured in a limited quantity, as well as vacuum IC and ceramic IC, are frequently referred to as the last group. The groups indicated above are assigned the following digits: 1, 5, 7 -- semiconductor IC (designation 7 is assigned to semiconductor IC without housings); 2, 4, 6, 8 -- hybrid IC; 3 -- other IC.

According to the nature of the functions implemented in radioelectronic apparatus, IC are subdivided into subgroups (for example, oscillators, modulators, triggers,

amplifiers) and types (for example, frequency, phase, duration, voltage converters). The classification of integrated circuits in accordance with their functional purpoise is shown in Table 1.1.

According to the adopted system of designations, an IC must consist of 4 elements.

The first element -- a digit corresponding to the design-technological group.

The second element -- two-three digits assigned to a given IC series as the ordinal number of the development. Thus, in the first two elements are three-four digits that determine the total number of the IC series.

The third element -- two letters, corresponding to the subgroup and the IC type (see Table 1.1).

The fourth element -- the ordinal number of the IC development in a given series in which there may be several equal in the functional criterion of the IC. It may consist of one digit, as well as several digits. GOST 18682-73 does not limit this number.

Below is shown an example of a conditional designation of an integrated semiconductor operational amplifier with an ordinal of the series development -- 40, the ordinal number of the development of the given circuit in the series according to the functional criterion -- 11.

1. Series
2. UD
3. Ordinal number of a microcircuit development according to functional criterion in the given series
4. Type (according to functional purpose)
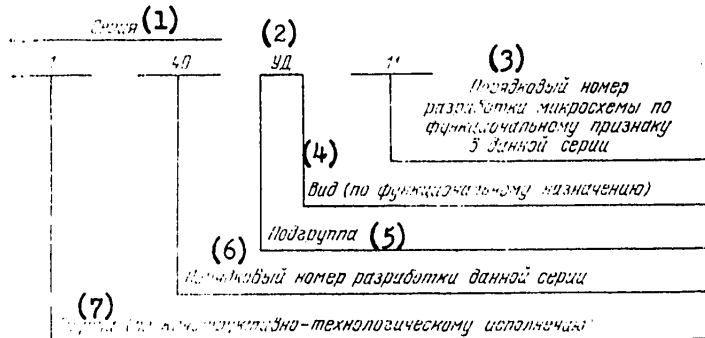
5. Subgroup
6. Ordinal number of given series
7. Group (according to the design-techological makeup).

Table 1.1

Functional classification of IC

Subgroup		Type		Letter Designation of the rated type
Name	Letter Designation	Name	Letter Designation	
Oscillators	G	Harmonic signals	S	GS
		Rectangular signals (including self-excited multivibrators, blocking oscillators etc.)	G	GG
		Linearly changing signals	L	GL
		Special shape signals	F	GF
		Noise	M	GM
		Others	P	GP
Detectors	D	Amplitude	A	DA
		Pulse	I	DI
		Frequency	S	DS
		Phase	F	DF
		Others		
Switches and keys	K	Current	T	KT
		Voltage	N	KN
		Others	P	KP
Logic elements	L	Element AND-NOT	A	LA
		Element OR-NOT	Ye	LYe
		Element AND	I	LI
		Element OR	L	LL
		Element NOT	N	LN
		Element AND-OR	S	LS
		Element AND-NOT/OR-NOT	B	LB
		Element AND-OR-NOT	R	LR
		Element AND-OR-NOT/AND-OR	K	LK
		Element OR-NOT/OR	M	LM
		Expanders	D	LD
		Others	P	LP
Multifunctional circuits	Kh	Analog	A	KhA
	Digital		L	KhL
	Combined		K	KhK
	Other		P	KhP
Modulators	M	Amplitude	A	MA
		Frequency	S	MS

Table 1.1 continued

Functional Classification of IC

Subgroup		Type		Letter Designation of the rated type
Name	Letter Designation	Name	Letter Designation	
Modulators	M	Amplitude	A	MA
		Frequency	S	MS
		Phase	F	MF
		Pulse	I	MI
		Others	P	MP
Sets of elements	N	Diodes	D	ND
		Transistors	T	ND
		Resistors	R	NR
		Capacitors	Ye	NYe
		Combined	K	NK
		Others	P	NP
Converters	P	Frequency	S	PS
		Phase	F	PF
		Duration	D	PD
		Voltage	N	PN
		Power	M	PM
		Level	U	PU
		Code-analog	A	PA
		Analog-code	B	PA
		Code-code	R	PR
		Others	P	PP
Circuits for secondary power sources	Ye	Rectifiers	V	YeV
		Converters	M	YeM
		Voltage stabilizers	N	YeN
		Current stabilizers	T	YeT
		Others	P	YeP
Delay circuits	B	Passive	M	BM
		Active	R	BR
		Others	P	BP
Selecting and comparing circuits	S	Amplitude (signal level)	A	SA
		Time	V	SV
		Frequency	S	SS
		Phase	F	SF
		Others	P	SP

Table 1.1 continued

Functional Classification of IC

Subgroup		Type		Letter Designation of the rated type
Name	Letter Designation	Name	Letter Designation	
Triggers	T	Type JK	V	TV
		Type RS	R	TR
		Type D	M	TM
		Type T	T	TT
		Dynamic	D	TD
		Schmidt	L	TL
		Combined (types DT,RST etc)	K	TK
		Others	P	TP
Amplifiers	U	High frequency*	V	UV
		Intermediate frequency*	R	UR
		Low frequency*	N	UN
		Pulse signals*	I	UI
		Repeaters	Ye	UYe
		Read-out and retrieval	L	UL
		Indication	M	UM
		DC*	T	UT
		Operational and differential*	D	UD
		Others	P	UP
		*Voltage and power amplifiers (including low-noise		
Filters	F	Upper frequencies	V	FV
		Lower frequencies	N	FN
		Band	Ye	FYe
		Rejector	R	FR
		Others	P	FP
Shapers	A	Rectangular pulses (biased multivibrators, blocking oscillators, etc.	G	AG
		Special shape pulses	F	AF
		Address currents (shapers of voltages or currents)	A	AA
		Discharge currents (shapers of voltages or currents)	R	AR
		Others	P	AP

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Table 1.1 continued

Functional Classification of IC

Subgroup		Type		Letter Designation of the rated type
Name	Letter Designation	Name	Letter Designation	
Memory matrices: elements	R	Storage		
		Main memories (OZU)	M	RM
		Permanent memories (PZU)	V	RV
		OZU with control circuits	U	RU
		PZU with control circuits	Ye	RYe
		PZU with control circuits and one-time programing	T	RT
		PZU with control circuits and multiple programing	R	RR
		Analog memory (AZU) with control circuits	A	RA
		Others	P	RP
Elements of arithmetic and discrete devices	I	Registers	R	IR
		Adders	M	IM
		Half-adders	L	IL
		Counters	Ye	IYe
		Coders	V	IV
		Combined	K	IK
		Others	P	IP

A letter is sometimes added to the end of the conditional designation that defines the technological spread of the electrical parameters of the given rated type. The concrete value of the electrical parameters and the difference between the rated types is given in the tachnical documentation (for example, IC133LA1A differs from IC133LA1B).

In some series (this is also stipulated in the technical documentation), the letter at the end of the conditional designation of the IC defines the type of the housing used for the given rated type. For example, the letter P designates a plastic housing, while the letter M -- a ceramic housing. For microcircuits utilized in widely used devices, the letter K is at the beginning of the conditional designation. The designation then appears as K140UD11. If, after the letter K, there is also shown the letter M ahead of the series number, this indicates that all the given series is manufactured with a ceramic housing (for example, KM155LA1).

A series made for export(with a pitch of housing leadouts of 2.54 mm) is especially stipulated with the letter E before the letter K in the conditional designation, (for example, EK561LS2), while the series in the variation without housing, without leadouts being connected to the chip of the microcircuit -- is stipulated by the letter B ahead of the series designation (for example, KB524RP1A-4).

For IC without housings, in the shortened designation, a digit is introduced after a hyphen to characterize a corresponding design modification (for example, 703LB1-2): with flexible leadouts-1*; with ribbon leadouts, including those made with polyamide film-2; with hard leadouts-3; on a common plate (undivided)-4; separated without loss of orientation (for example, pasted on the film)-5; with contact pads without leadouts (chip)-6.

It should be noted that before the introduction of GOST 18682-73 [6] (i.e., before 1973), the assignment of conditional designations was made in accordance with the existing technical-norm documentation. After 1973, most IC received new conditional designations. However, for a certain number of IC for which no new technical documentation was issued, old conditional designations were continued.

The old and new conditional designations differ by the letter designations of subgroups and types (the latter is due to an increase in the number of types in GOST 18682-73 as compared to the previously existing documentation.

An example of the old designation of an IC type 1LB331 is shown on the next page.

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*Modification "1" is applied to microcircuits with a number of leadouts no greater than 16.

Серия **(1)**

(2) Порядковый номер разработки (по функциональному признаку в данной серии)

1   ЛБ   33   1

(3) Порядковый номер разработки данной серии

(4) Подгруппа и вид (по функциональному назначению)

(5) Группа (по конструктивно-технологическому исполнению)

1. Series

2. Ordinal number of development (according to functional criterion in the given series)

3. Ordinal number of development of the given series

4. Subgroup and type (according to functional purpose)

5. Group (according to design-technological makeup)

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4. GOST 17021-75. Integrated microcircuits: Terms and definitions
5. GOST 17467-79. Integrated microcircuits: Basic sizes.
6. GOST 18682-73. Integrated microcircuits: Classifications and systems of conditional designations.

2291
CSO: 1863/209

UDC 621.396

EMITTER-CONNECTED TRANSISTOR LOGIC CIRCUITS

[Text] Chapter 3

3.5 Emitter-connected Transistor Logic Circuits

Digital IC emitter-connected transistor logic circuits (ESTL) are transistor switching circuits with connected emitters and, compared to other digital keys, have the highest speed of operation and a high power consumption. High speed of operation (or to put it another way, a small average time of propagation delay) of ESTL is due to the fact that transistors in these keys operate in an unsaturated (linear) mode. Emitter repeaters that accelerate the process of charging the capacitance of the load are used at the circuit output. A reduction in the propagation delay time is also achieved due to the limitation of the output voltage gradient which, however, leads to a reduction in the interference rejection of the ESTL circuits. Of the digital IC ESTL developed in recent years, the most widely used are series 100 and K500 that are similar to a widely known MS10,000 series abroad (original developer -- the Motorola Co.).

We will consider the principle of designing the ESTL switch on an example of a basic series 100 logic element that implements simultaneously functions OR-NOT and OR (Fig. 3.21). The circuit consists of a differential amplifier assembled with VT1 and VT4 and VT5 transistors. When the signal gradient is applied to the input of this amplifier, current I_9 may flow either through transistor VT5 to whose base is constantly applied reference voltage U_{on} =-2.9 volts (during this time a negative blocking voltage is present at inputs X_1-X_4), or through transistors VT1-VT4, when a voltage greater than U_{on} is applied to their bases.

Output emitter repeaters (transistors VT7 and VT8 are connected to the bias level source $U_{cm\,y}$ =-2 volts ± 5% through external load resistors R_{H1} and R_{H2} with rated resistances of 51 ohms. The low output impedance of the circuits provides for the matching of the output and input levels of the logic elements when they are operating together and the possibility of feeding signals into a cable with 50 ohm wave impedance. The ESTL circuit is connected to a negative voltage power source U_{Hn}=5.2 volts ± 5%. The collector circuits are grounded. Such a connection provides a lower dependence of the output voltage on inductions from the feed circuit and a better interference rejection. The value of the logic gradient for the ESTL is 0.69 millivolts, while the interference rejection reserve is -125 millivolts. Negative and logic levels of the ESTL circuits (U'_{Bbix} =0.96 volts, U^0_{Bbix} =-1.65 volts) low in value, make it impossible to interface them directly with the TTL [Transistor-transistor logic] series circuits. The joint operation of TTL and ESTL circuits is implemented by special circuits of mutual level converters, entering the composition of all the above-indicated ESTL series.
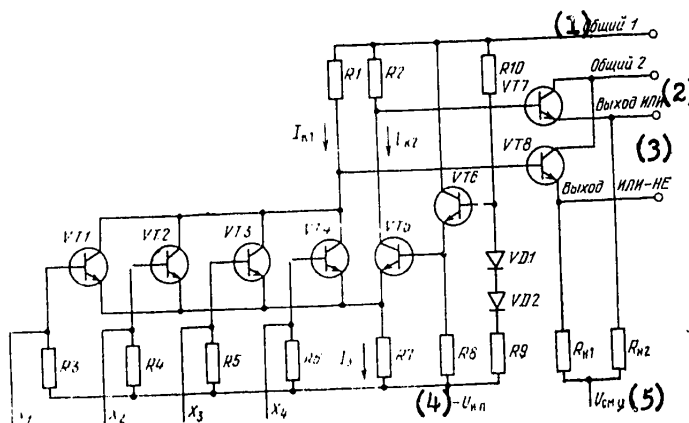
Fig. 3.21. Basic logic element OR-NOT/OR of the ESTL series

1. Common 1
2. OR output
3. OR-NOT output

4. U_{Hn}

5. $U_{cm\,y}$

All inputs to the base logic element through leakage resistors R3...R6, with a resistance of about 50 kohms, are connected to power source U_{Hn} =-5.2 volts ± 5%. This connection makes it possible to leave the unused inputs in the apparatus unconnected. To eliminate the effect on the logic part of the circuit of pulse interferences originating in the collector circuits of the emitter repeater at

the moment of switching the circuit when operating with a low impedance load, two "ground" buses are used: one for output emitter repeaters and the other -- for the internal logic part of the circuit.

Reference voltage U_{on} =-2.09 volts is produced by a special temperature-compensated circuit (transistor VT6, diodes VD1, VD2, as well as resistors R8, R9, R10) and is selected so that it would be lower than minimum voltage 1. We will consider the principle of operation of the basic logic element (Fig. 3.21). If a low voltage level, corresponding to 0 (U_{BX}^{0} =-1.85 volts), is applied to all inputs $X_1 \ldots X_4$, transistors VT1-VT4 are cut-off (only leakage currents are flowing) because their emitters have the following voltage applied:

$$U_{\ni} = U_{on} + U_{6,VT5} = -1.29 + (-0.80) = -2.09 \text{ volts}$$

The level of current $I_{\ni}$ is determined by voltage $U_{\ni}$ and the rating of resistor R7. Current $I_{\ni}$ flows through open transistor VT5 to whose base is applied reference voltage U_{on}, as well as resistors R7 and R2. A voltage drop U_{R2}=-0.98 volts is produced across resistor R2. The voltage at the OR output at this moment corresponds to level 0(U_{Bblx}^{0} =-1.65 volts), while at the output of OR-NOT, the voltage corresponds to 1 ($U_{Bblx}^{'}$ =-0.96 volts) (voltage $U_{\sigma_{\ni}}$ of transistor VT7 should be added to the voltage drop across resistor R2).

When a high voltage level, i.e., 1 ($U_{BX}^{'}$ =-0.81 volts), is supplied to one of the inputs (or to all inputs $X_1 \ldots X_4$), the input transistor opens because the reference voltage selected was more negative than the minimal voltage 1. Transistor VT5 closes by the formed voltage gradient and all of current $I_{\ni}$ will flow through the opened input transistor (one of the VT1-VT4 row) and resistors R1 and R7. The negative voltage on the joined collectors of the input transistors will increase to level -.97 volts and a level, corresponding to 0, will be established at the output of the emitter repeater VT8, while 1 will be established at the output of emitter repeater VT7. Thus, the circuit produces logic function OR at the output of transistor VT7 and logic function OR-NOT at the output of transistor VT8. Thus, jumps in the input signal cause switching of current $I_{\ni}$ which, depending upon the value of the input signal, flows either through transistor VT5 or through transistors VT1-VT4. Because of this, the circuit with joined emitters is frequently called a current key. The paraphase outputs of the basic ESTL switch shorten the propagation path of the signals in digital devices. The presence of emitter repeaters that have low output impedance at the circuit outputs, provides a considerable load capacity of the ESTL circuits ($K_{pa3} > 15$). To provide a still higher load capacity the ESTL digital series include special circuits with a high branching coefficient (K_{pa3} = 50...100 at $C_H > 100$ picofarads).

An increase in the joining coefficient with respect to inputs may be achieved by connecting a logic expander to the basic circuit; however, this causes a considerable reduction in the speed of operation of the circuit due to parasitic capacitances; therefore, expander circuits are not included in the ESTL series [3]. We will now consider ESTL circuits in greater detail.

3.5.1. Functional Composition of the ESTL Series

In recent years technological successes made it possible to increase the functional possibilities of the ESTL series considerably. Along with logic elements and D triggers, decoding and multiplex circuits, memories and arithmetic device units were introduced into these series. This provides for their wide use in high speed computers. The functional composition of the ESTL digital series, developed in recent years, and their analogs are shown in Table 3.13.

We will consider in greater detail the purpose and special features of operation of several IC of series 100. IC types 100LM101, 100LM102, 100LM105, 100LM109 and 100LYe106 (and corresponding IC of series K500) implement functions OR-NOT and are designed with the basic logic element.

IC types 100LP115, 100LP116 are receivers from the line and may be used in two modes: as receivers of a paraphase signal from a two-wire communications line (in this case, the built-in leads in the housing of reference voltage source are not used) and as logic elements with constant voltages 0 or 1 at the output (with an external connection of the leadout from the reference voltage source with certain input leadouts. The use of both modes simultaneously for elements contained in the same IC housing is permitted.

IC type NR400 is a matrix of load resistors (four resistors rated at 500 ohms and four resistors rated at 800 ohms) which, with proper switching, are used as a load on the nonmatching inputs of the logic circuits of the series.

IC type 100TM130 (Fig. 3.22a) are two D triggers -- "latches," equipped with setting (S), resetting (R), synchronizing (C_E) inputs and a general synchronization input (C). Data is received from input D during the time when $C=0$; $\overline{C}_E=0$. In this case, any change in the data at input D is transmitted to the trigger output. The data is stored at the moment that the signal at input C changes from state 0 to state 1. For $\overline{C}_E=1$, the trigger is suppressed at input C. A forced setting of the trigger into state 1 (input S) and resetting (input R) is done when $C=\overline{C}_E=1$; in this case, the signal at input D does not affect the trigger. When the trigger is controlled by the R and S inputs, the setting and resetting pulses should not overlap in time.

IC type 100TM134 [Fig. 3.22b), unlike IC type 100 TM130, has two data inputs, D_1 and D_2 and an additional selector input S. When 1 is applied to input S, the data is recorded only by input D_1; when 0 is applied to input S, the data is recorded only by input D_2.
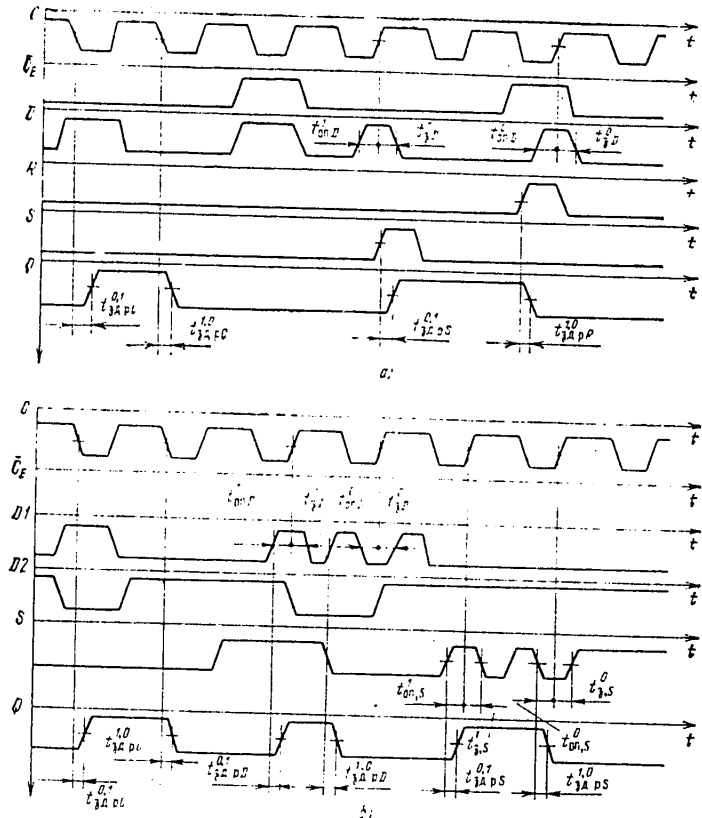
Fig. 3.22. Time diagrams of D trigger operation for IC type 100TM130 (a) and type 100TM134 (b).
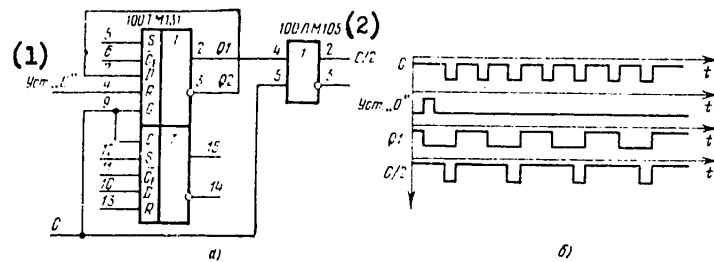
Fig. 3.23. Frequency divider for IC type 100TM131 (a) and its time diagram (b).

1. Zero setting   2. 100LM105

Table 3.13

Compositions of ESTL series and their functional analogs in the MS10000 series

| Functional purpose | ESTL series | | Analog MS10000 | Variation without housing 700 | No. of Figure in supplement 3.2 |
	100	K500			
Four logic elements 2OR-NOT/2OR	100LM101	K500LM101 K500LM101T	MS10101	700LM101-2	3.2.1
Three logic elements 2 OR-NOT and logic element 2 OR-NOT/2 OR	100LM102	K500LM102 K500LM102T	MS10102	700LM102-2	3.2.2
Two logic elements 2 OR-NOT/2 OR and logic element 3 OR-NOT/3 OR	100LM105	K500LM105M K500LM105T	MS10105	700LM105-2	3.2.3
Two logic elements 3OR-NOT and logic element 4 OR-NOT	100LE106	K500LYe106T K500LYe106M	MS10106	700LYe106-2	3.2.4
Three logic elements "exclusion OR-NOT/OR"	100LP107	K500LP107 K500LP107M	MS10107	700LP107-2	3.2.5
Two logic elements 5 OR-NOT/5OR, 4 OR-NOT/4 OR	100LM109	K500LM109 K500LM109M	MS10109	700LM109-2	3.2.6
Two logic elements 3OR with high power input	100LL110	K500LL110T K500LL110M	MS 10110	700LL110-2	3.2.7

Table 3.13 continued

Variation without housing

Functional purpose	ESTL series		Analog MS10000	200	No. of Figure in supplement 3.2
	100	K500			
Two logic elements 3 OR-NOT with high power input	100LE111	K500LYe111T K500LYe111M	MS10111	700LYe111-2	3.2.8
Four line receivers	100LP115	K500LP115 K500LP115T	MS10115	700LP115-2	3.2.9
Three line receivers	100LK116	K500LP116 K500LP116T	MS10116	700LP116-2	3.2.10
Two logic elements 2-3 OR-2 AND-NOT/3 OR-2 AND	100LK117	K500LK117 K500LK117M	MS10117	700Lk117-2	3.2.11
Logic element 3-3-3-4 OR-4 AND	100LS119	K500LS119M	MS10119	700LS119-2	3.2.13
Two logic elements 3-3 OR-2 AND	100LS118	K500LS118M	MS10118	700LS118-2	3.2.12
Resistor matrix	—	—	—	700NR1-2	—
Two D triggers	100TM231	K500TM231M K500TM231T	MS10231	700TM231-2	3.2.47
Logic element 3-3-3-3 OR-4 AND-NOT/3-3-3-3 OR-4 AND	100LK121	K500LK121 K500LK121M	MS10121	700LK121-2	3.2.15
Level converter	100PU124	K500PU124 K500PU124T	MS10124	700PU124-2	3.2.16
Level converter	100PU125	K500PU125 K500PU125T	MS10125	700PU125-2	3.2.17

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Table 3.13. continued

Functional purpose	ESTL series		Analog MS10000	Variation without housing 700	No. of Figure in supplement 3.2
	100	K500			
Two D triggers	100TM130	K500TM130 K500TM130M	MS10130	700TM130-2	3.2.18
Two D triggers	100TM131	K500TM131T K500TM131M	MS10131	700TM131-2	3.2.19
Four triggers with latch	100TM133	K500TM133T K500TM133M	MS10133	700TM133-2	3.2.20
Two D triggers	100TM134	K500TM134 K500TM134M	MS10134	700TM134-2	3.2.21
Universal binary counter	-	K500IYe136	MS10136	-	3.2.22
Universal decimal counter	-	K500IYe137	MS10137	-	3.2.23
Universal shift register	100IR141	K500IR141	MS10141	-	3.2.24
SOZU 64 word memory - 1 bit	100IR141	K500RU148 K500RU148M	MS10148	-	3.2.25
12-input parity check circuit	100IYe160	K500IYe160 K500IYe160T	MS10160	700IYe160-2	3.2.26
3-stage low level decoder	100ID161	K500ID161M	MS10161	700ID161-2	3.2.27
3-stage high level decoder	100ID162	K500ID162M	MS10162	700ID162-2	3.2.28
8-channel multiplexer	100ID164	K500ID164M	MS10164	700ID164-2	3.2.29
Rapid transfer circuit	100IP179	K500IP179 K500IP179T	MS10179	700IP179-2	3.2.30
Duplexed high speed adder-subtractor	100IM180	K500IM180 K500IM180T	MS10180	700IM180-2	3.2.31
Resistor matrix	100NR400	K500NR400T	MS10400	700NR400-2	3.2.32

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Table 3.13 continued

Functional purpose	ESTL series		Analog	Variation without housing	No. of Fig-ure in sup-plement 3.2
	100	K500	MS10000	700	
SCZU 16-bit memory with control circuits	100RU401	K500RU401 K500RU401M	MS10401	700RU401-2	3.2.33
Associative memory with readout (2 words with 2 bits each)	100RU402	—	—	700RU402-2	3.2.34
Memory with 256 bits (256 words with 1 bit each) with circuit controls	—	K500RU410	MS10410	—	3.2.35
Memory with 128 bits (128 words with 1 bit each) with circuit controls	—	K500PU411	MS10411	—	3.2.36
Memory with 128 bits (128 words with 1 bit each) with circuit controls	—	K500RU412	MS10412	—	3.2.37
Permanent PZU memory with 1024 bits	—	K500RU149	MS10149	—	3.2.38
Arithmetic-logic device for 16 operations with 2 4-bit words	100IP181	K500IP181T K500IP181	MS10181	700IP181-2	3.2.39
Two OR logic elements with high power output	100LL210				
Two OR-NOT logic elements with high power output	100LYe211				
Two reproduction amplifiers	100UL480				
Coding element with priority	100IV165				

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Table 3.13 continued

Functional purpose	BSTL series		Analog Variation without housing	No. of Fig-ure in supplement 3.2
	100	K500		
Four D triggers with input multiplexers	100TM173			
Two control circuits with voltage key	100KN490			
Three line receivers	100LP216	K500LP216M K500LP216T		
Line exciter	100LP128	K500LP128		
Two control circuits with universal current key	100KT491	—		
Line receiver	100LP129	K500LP129		

Notes 1.: IC series 100 and K500 have the same temperature range (-10...+70°C) and are made in the following housings: series 100 -- in housings 402.16-1, series K500 -- in housing 201.16-1, 201.16-5, 201.16-6, 238.16-2, 239.24-2. 2. Index M means that the microcircuit has ceramic housing type 201.16-5, 201.16-6; index 10 - in ceramic housing 201.16-1.

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IC type 100TM1 (Fig. 3.23) is two double D triggers of the ms type with separate inputs for setting S, resetting R, synchronizing $\overline{C}_E$ and with common synchronization input C. The data is received on the master trigger from input D at C=0 and $\overline{C}_E$=0. During this time, the slave trigger stores the data received by the trigger in the previous cycle. The data storing occurs when the signal changes at input C from state 0 to state 1. In this case, trigger m changes to the storage mode, while trigger s changes to the receiving mode. Previously recorded data in the m trigger is transferred to the output of the circuit. At $\overline{C}_E$=1, the trigger is blocked at input C.

To achieve the calculating mode it is necessary to connect output Q to input D and feed counting pulses to input C or C_E (Fig. 3.23b). Compulsory setting (S) and resetting (R) are achieved at any moment of time, independently of the state of other trigger inputs (Fig. 3.24).
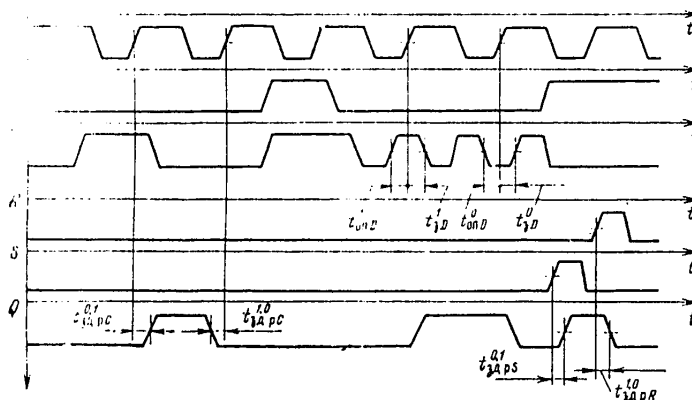
Fig. 3.24. Time diagram of a D trigger type 100TM131 operation in the calculation mode.

IC type 100TM133 is four D triggers with strobing elements at the trigger inputs. Strobing elements are divided with respect to trigger pairs by strobing outputs (G1, G2), synchronization input $\overline{C}_E$ and common synchronization input C. The data is received from input D at C= 1 and $\overline{C}_E$ =1, in this case direct data transmission from the input to the output of the system may be blocked by signal 1 at the input of the strobing element. Data storing occurs when the signals change at inputs G1 and G2 from state 1 to state 0. When all triggers are synchronized with respect to the common input C, 0 must be set at the inputs of separate synchronization or they must remain switched off. With separate synchronization of trigger pairs with respect to $\overline{C}_E$ inputs, the common synchronization input C must remain switched off , or signal 0 must be fed to it (Fig. 3.25).

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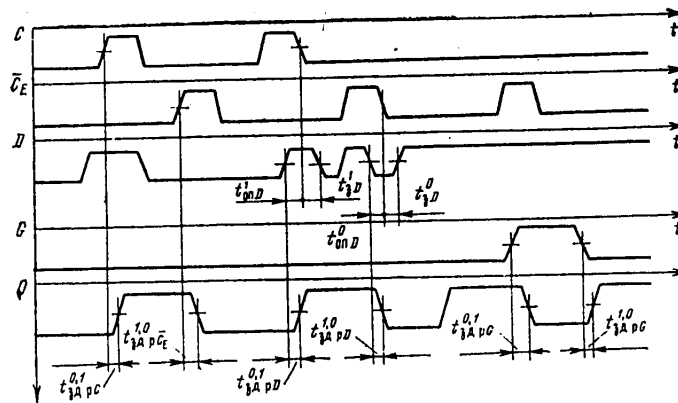
Fig. 3.25. Time diagram of D trigger type 100TM133.

To provide proper operation of the trigger circuits, it is necessary to take into account a number of additional parameters shown in the above-cited time diagrams:

$t_{3D}^{1,0}$, $t_{3S}^{1,0}$ -- minimum allowable delay time of the signal front or cut-off at inputs D or S with respect to the positive synchronization pulse front; $t_{oh D}^{1,0}$, $t_{oh S}^{1,0}$

-- minimal allowable time for advance of the front and cut-off of signals at inputs D or S with respect to the positive front of the synchronization pulse. The values of these parameters must be as follows: $t_{on D}^1$ with respect to the D input -- not less than 2.5 nanoseconds; $t_{on S}^1$ with respect to the S input -- not less than 3.5 nanoseconds, t_{3D} with respect to the D input -- not less than 1.5 nanoseconds and t_{3S} with respect to the S input -- not less than 1.5 nanoseconds.

IC type 100ID164 is an 8-channel multiplexer with an inhibition input W made of basic logic elements. The presence of the inhibition input makes it possible to organize high level decoding circuits and implement an "OR wiring" operation of circuits for multiplexing (combining) over eight channels. IC type 100IYe160 (12-input parity check circuit) is a combination of nine logic elements that implement the "OR locking" to function. The circuit is designed to determine a parity of words up to 12 bits long. The output voltage corresponds to level 1 if an odd number of digit "units" is present at the circuit inputs.

IC type 100IP179 is a high-speed carry unit and is designed for combined use with IC types 100IP180 or 100IP181 in high-speed acting arithmetic and logic devices, operating with long words. The circuit consists of ten OR-NOT-OR logic elements in which the collectors of the input transistors are combined in an "OR wiring" circuit. IC type 100IP181 are high-speed universal arithmetic-logic devices (ALU), designed to implement 16 logic functions and 16 arithmetic operations with two four-bit numbers.

$A_0 \ldots A_3$ and $B_0 \ldots B_3$ are data inputs. Input variables A and B in the positive logic circuits are fed in the complementary code and output function Y, in this case, is also formed in the complementary code. The direct code of variables A, B and of output funcetion Y is used in the operation of the ALU in the negative logic function (0 corresponds to the upper level and 1 -- to the lower level). Inputs $S_0 \ldots S$ are used to assign the code of the function being implemented. Depending upon the signal at output M, the device implements logic or arithmetic operations. Full internal carry circuits are built-in in the ALU circuit. Input C is the carry input from the previous stages. The carry signal into the following stage is formed at output X_2.

The combined utilization of IC types 100IP 181 and 100IP179 makes it possible to almost halve the arithmetic operation time for 32-bit words. Two complementary group carry signals (outputs X_1 and X_3) produced in the ALU are used in the accelerated carry operating mode. The implementation of logic transformations of input variables A and B is done when signal 1 is fed to input M which blocks the internal carry circuits.

The value of the typical parameters of the ALU in inplementing arithmetic operations with words from 4 to 64 bits long, using accelerated carry circuits in 100IP179, are shown in Table 3.14. For the combined operation of series 100 and IC series 133 and 155 circuits, IC type 100PU124 is used. It consists of four 2-input level converters for transferring from TTL to IC of the ESTL type, as well as type 100PU125, which consists of four 2-input level converters for transferring from ESTL to IC type TTL.

We will consider the operation of level converters in greater detail. Fig. 3.26a shows one of four level converters included in IC type 100PU124. It consists of input diodes VD1-VD4, an input emitter repeater (transistor VT1), a differential amplifier (transistors VT5 and VT7), operating in a current switching mode, emitter repeaters(transistors VT4 and VT8), as well as a source of reference voltages (transistors VT9 and VT10).

TTL feed voltage (5.0 volts +5%) is fed to leadout 9 and the ESTL feed voltage (-5.2 volts ± 5%) is applied to leadout 8. Leadout 16 (common) is grounded and the load is connected to paraphase outputs 4 and 2. For strobing all four elementary converters located in this IC, second inputs of each converter are combined at leadout 6.

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Table 3.14

Typical parametersof the ALU type 100IP181 when operating with accelerated carry circuit type 100IP179

Word length, bits	Adding time nanoseconds		Number of IC	
	With series carry	With accelerated carry	type 100IP181 in ALU	type 100IP179 in ALU circuit with accelerated carry
4	7	–	1	–
8	11	–	2	–
12	14	13	3	1
16	17	16	4	1
32	30	18	8	2
48	43	20	12	3
64	56	22	16	4

The reference voltage source forms the bias voltage for the current oscillator (transistor VT6). This voltage is taken off the emitter of transistor VT10. Two reference voltages are also created, U_{on_1} =- 1.8 volts and U_{on_2} =-0.7 volts. Voltage U_{on_1} from emitter of transistor VT9 is fed to one input of the differential amplifier (base of transistor VT7), the voltage from resistor R12 enters the base of still another current oscillator (transistor VT2). When a 2.4 volt signal is applied to the input, a voltage of about 0.05 volts originates at the base of transistor VT3 and the voltage on the base of transistor VT5 will,in this case, be approximately equal to 0.8 volts which corresponds to level 1 in the ESTL circuits. Transistor VT5 is found to be open, level 0 is established at output 4 and level 1 -- at output2. To suppress interference pulses originating at the moment of switching in the feed circuits of the TTL circuits, diodes VD1 and VD2 are installed at the level converter input.

Fig. 3.26b shows a circuit of one of the four level converters in IC type 100PU125. The circuit consists of a current key (transistors VT3, VT5 and VT10), equipped with a stable current oscillator in the emitter circuit (transistor VT6 and resistor R9) and an output stage (similar to the inverter in the TTL circuits), operating in the saturation mode (transistors VT4, VT7,...VT9.). Feed foltage 5.0 volts ± 5% is applied to leadout 9 and feed voltage -5.2 volts ± 5% is applied to leadout 8. Leadout 16 (common) is grounded.

A bias is applied to the stable current oscillator from the internal source of reference voltages (elements VT1, VT2, VD1...VD4, R1...R4) and two reference voltages are also used: U_{on_1} =-2.8 volts, taken off the collector of transistor VT2 and U_{on_2} =1.29 volts, entering from the emitter of transistor VT1. Reference voltage U is used to fix the output voltage of 0 when the circuit inputs are connected to the -5.2 volt voltage source or are free.

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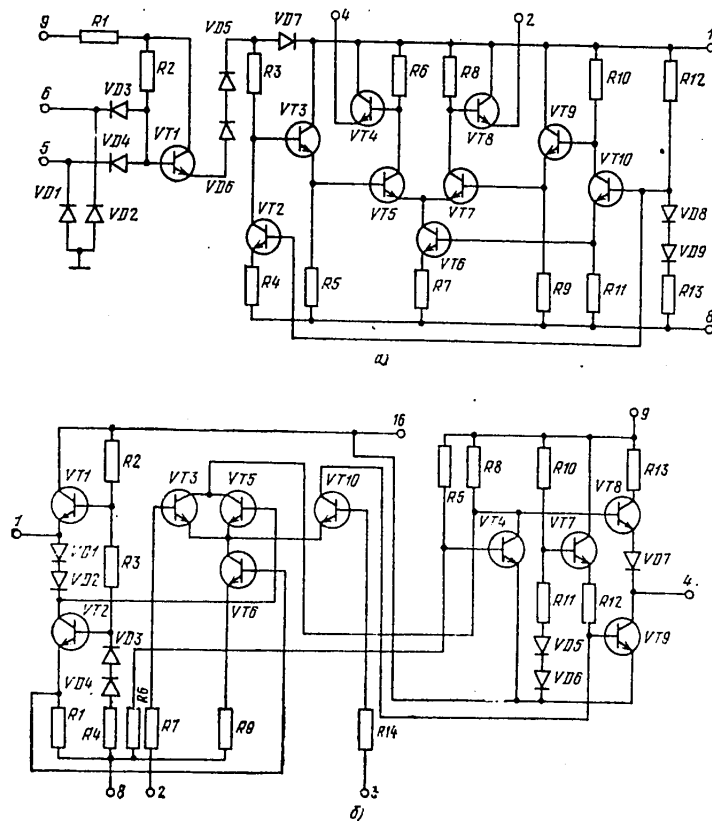
Fig. 3.26. Level converter for transferring from the TTL to the ESTL (IC type 100PU124 (a) and for transferring from the ESTL (IC type 100PU125) (b).

When using the circuit as a one-input level converter, the reference voltage U (leadout 1) is fed to leadouts 2 or 3 depending on whether the circuit must produce an inverted or noninverted conversion. Thus, in case U_{on2} is connected to input 3 and 1 is present at input 2, transistor VT3 is open, while transistor VT10 is closed. The voltage of the VT3 transistor collector is about 1 volt which is enough to block transistor VT8 reliably. The current through open transistorVT7 enters the base of transistor VT9, insuring its saturation,as a result of which

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voltage $U^O_{вых} \leqslant 0.5$ volts is established at output 4, corresponding to level 0 of the TTL circuits. When logic 0 is fed to input 2, transistorVT10 opens and VT3 closes. The voltage on the base of transistor VT9 reduced to the level of 1 volt which leads to the closing of transistor VT9. The voltage on the collector of transistor VT3 increases, which leads to the opening of transistor VT8. As a result a voltage is established at output 4 which corresponds to level 1 of TTL circuits ($U^1 = 2.4$ volts).

When all four elements of circuit 100PU125 are used, reference voltage U_{on2} from leadout 1 is fed to corresponding inputs of all four elements. In designing functional units using level converter circuits, it should be taken into account that the zero level $U^O_{вых} \leqslant 0.5$ volts is somewhat higher than the zero level of TTL circuits ($U^O_{вых} \leqslant 0.4$ volts) which reduces the noise resistance of the latter by 100 millivolts.

The branching coefficient of level conterters when operating at inputs of IC series 123, 155 is no greater than 8, and at inputs of IC series 130 -- no greater than 6.

IC type 100RU401 is a superoperative memory with nondestructive readout and consists of a matrix of trigger memory elements organized as 16 one-bit words. The matrix is equipped with a circuit for address and bit control. The electrical functional circuit of such a memory (Fig. 3.27a) consists of 16 triggers (elements for storing data) organized into a two-dimensional (along X and Y) 4x4 matrix (VT1-1...VT4-4), 8 address formers (F), read-in amplifiers(3п 0,3п 1) and two read-out amplifiers (Сч 0, Сч 1). The circuit operates in three modes: data storing, read-out and read-in. Addressing (selection when reading out and reading in) is done by simultaneously feeding level 1 into selected address buses (X,Y). Zero level must be maintained at all address buses not selected. When there are no signals at read-in amplifier inputs ($U_{вх \, зпо} = 0$, $U_{вх \, зп1} = 0$) the signal from the selected cell of data storage is fed over the read-out buses to the input of the read-out amplifier 0 or 1. Depending upon whether 0 ar 1 were read-in in the selected cell, level 1 is formed at the output of the corresponding amplifier. The interrogated cell stores its data. Switching the trigger to the new state will occur only when new data is received. To read-in 0 or 1,it is necessary to supply level 1 simultaneously to the selected buses x, y and to one of the read-in buses (3п 0 or 3п 1 respectively).

The data storage element (Fig. 3.27b) is an unsaturated trigger with direct coupling made with two three-emitter transistors VT1 and VT2, and three resistors. In the storage mode, the trigger has emitters E2...E5 operating while the circuits of emitters E1, E6 are disconnected. In the read-out and read-in modes, the trigger has emitters E1, E6 operating, while circuits of emitters E2...E5 are disconnected. Read-out and read-in is done over the P_1 and P_2 buses.

IC type 100RU402 is an associative memory device. The associative memory device (AZU) is designed for operation with 2-bit words. Besides storage functions, the
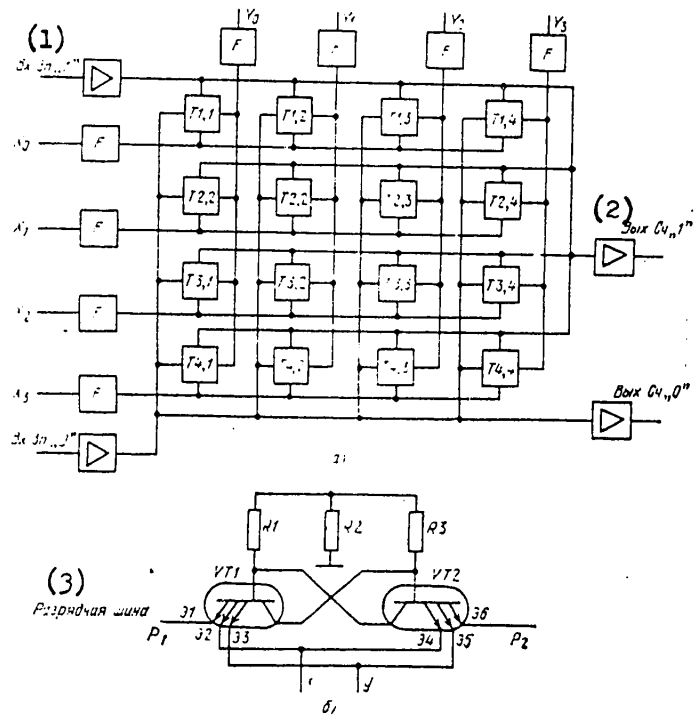
Fig. 3.27. Electrical functional circuit of a superoperative memory (a) and a
data storage element (b).
1. *Вх Зп 1*   -- input read-in 1   3. bit bus
2. *Вых Зп 1*   -- output read-out 1.

AZU does arithmetic operations on the stored numbers. At the basis of the AZU
design is a system of access by a tag -- the access to the needed word and its
selection is made by a tag contained in the desired word itself. Associative
selection (search mode) in microcircuit 100RU402 may be made under conditions of
"masking" the interrogated data. The retrieval is over two buses for each address.

Combinations 1-0 and 0-1 are used respectively for the retrieval of the 1 and the
0 states. Combinations 1-1 correspond to the "mask," i.e., in this case, the re-
action at the "word comparison" output corresponds to noncoincidence of the inter-
rogated data and any data stored under any address.

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3.5.2. Basic Electrical Parameters and Typical Characteristics of IC type ESTL

Digital type ESTL IC, besides the usual list of electrical parameters typical for other digital IC also have special static parameters: input and output threshold voltages.
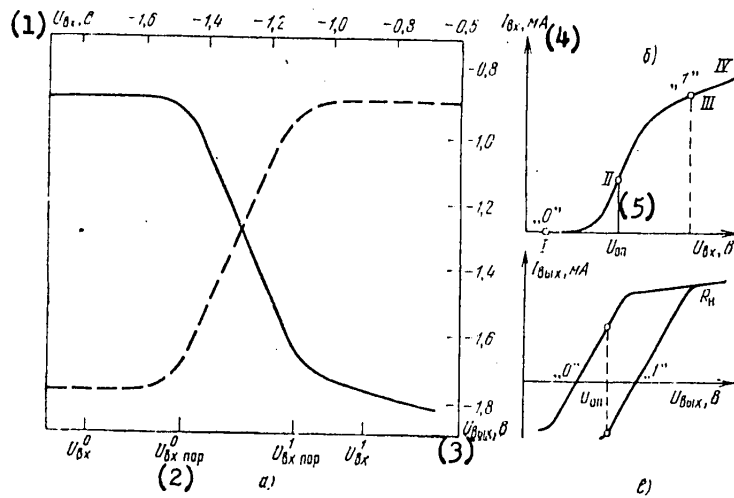
Fig. 3.28. Characteristics of basic logic element of the ESTL series;
a -- transfer (OR-NOT output, solid line; OR output, broken line)
b -- input, c -- output, with respect to current.

1. $U_{\text{вх}}$, volts -- input voltage
2. $U_{\text{вх пор}}$ -- threshold input voltage

3. $U_{\text{вых}}$ volts -- output voltage
4. $I_{\text{вх}}$, milliamps -- input current
5. $U_{\text{оп}}$ -- reference voltage.

Fig. 3.28a shows the typical transfer characteristics of a basic logic element of series 100, K500 with direct and inverse outputs. By means of these curves, it is possible to give the following parameter definitions for ESTL circuits: $U^1_{\text{вх пор}}$, $U^0_{\text{вх пор}}$ -- input threshold voltages; $U^1_{\text{вых пор}}$, $U^0_{\text{вых пор}}$ -- output threshold voltages; $U^1_{\text{вх}}$, $U^0_{\text{вх}}$ -- input voltages; $U^1_{\text{вых}}$ $U^0_{\text{вых}}$ -- output voltages of unity and zero. These parameters may be used to calculate the following: voltages of static noise resistance $U^1_{\text{пом}} = U^1_{\text{вых пор}} - U^1_{\text{вх пор}}$ and $U^0_{\text{пом}} = U^0_{\text{вх пор}} - U^0_{\text{вых пор}}$, logic gradient $U_\text{л} = U^1_{\text{вых}} - U^0_{\text{вых}}$, as well as the zone of switching $\Delta U = U^1_{\text{вх пор}} - U^0_{\text{вх пор}}$.

Taking into account the low values of output logic and the unavoidable technological spread of rated elements (therefore, also of the electrical parameters of the keys), maximum and minimum parameter values were established for the ESTL circuits that determine the transfer characteristic (Table 3.15). These parameters correspond to the allowable values of static interferences (for $-10 < t < 75^\circ C$) $U^1_{\text{пом}} \geq 125$ millivolts, $U^0_{\text{пом}} \geq 155$ millivolts; to deviation of output levels of 1 and 0 (for $t = 25^\circ C$), $\Delta U^0_{\text{вых}} \geq 690$ millivolts; switching zone (for $t = 25^\circ C$) $\Delta U_\text{л} \leq 370$ millimeters.

We will now consider the input characteristic of the basic logic element OR-NOT/OR of the ESTL series (Fig. 3.21). The input characteristic of this circuit (Fig. 3.28b) has four zones.

In zone 1 the input transistors are blocked and the input current is low (equal to the leakage current between the collector and the base). Entire current $I_\text{э}$ flows through the emitter circuit of transistor VT5. In zone II, as the voltage increases on one of the input transistor VT1-VT4, it gradually becomes conducting. The input current increases which increases collector current $I_{\text{к}1}$ due to the corresponding reduction in collector current $I_{\text{к}2}$ of transistor VT5. At a certain value of voltage $U_\text{вх}$, collector current $I_{\text{к}2}$ is reduced to a value considerably lower than $I_\text{э}$. In this case, the current through resistor R7 remains practically constant.

In zone III, as voltage $U_\text{вх}$ increases further, current $I_\text{э}$ and voltage U_{R7} will increase as a result of which the differential input impedance of the circuit will rise sharply. In zone IV, the transistor becomes fully conducting and picks up all of current $I_{\text{к}1} \approx I_\text{э} = \text{const}$.

In the cut-off state of the circuit, at voltage 1 on output 2, its working point is located on zone I of the input characteristic, while in the conducting state -- in zone III. Zone II is a transition zone. In this state the input impedance is minimal, while in zones I and III for $U_\text{вх}$ equal to voltages 0 or 1 the input impedance is high.

Table 3.15

Electrical parameters of IC series ESTL that determine the transfer characteristic

Parameter	Parameter values at t, °C						Values of electrical mode at inputs, volts, at $U_{ип} = -5.2$ volts			
	-10		25		75		$U^1_{вх\,пор}$	$U^0_{вх\,пор}$	$U^1_{вх}$	$U^0_{вх}$
	min.	max.	min.	max.	min.	max.				
Output threshold voltage 1, $U^1_{вых\,пор}$, volts	-1.040		-0.980				-1.165	-1.495	—	—
							-1.105	-1.475	—	—
							-1.105	-1.450	—	—
Output voltage 1, $U^1_{вых}$, volts	-1.020	-0.860	-0.960	-0.810	-0.900	-0.720			-0.860	-1.880
		-1.650							-0.810	-1.850
									-0.720	-1.830
Output threshold voltage 0, $U^0_{вых\,пор}$, volts				-1.630		-1.605	-1.165	-1.495	—	—
							-1.105	-1.475	—	—
							-1.045	-1.450	—	—
Output voltage 0, $U^0_{вых}$, volts	-1.880	-1.670	-1.850	-1.650	-1.830	-1.625			-0.860	-1.880
									-0.810	-1.850
									-0.720	-1.830

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Table 3.16

Electrical parameters of IC series of ESTL

Parameter	Values		Ambient temperature, t^o, C
	minimal	maximal	
Input current 0, $I_{\partial x}^0$, microamp .	0.5	–	25
Input current 1, $I_{\theta x}^1$, microamp.	–	265	25
Output threshold voltage	-.92	–	75
1, $U1_{\textit{Bbixnop}}$, volts	- 1.04	–	-10
Output threshold voltage	–	-1.605	75
0, $U_{\textit{Bbixnop}}^0$, volts	–	-1.650	-10
Output voltage 1, U_{Bbix}^1 ,	-0.9	-0.72	75
volts	-1.02	-0.86	-10
Output voltage 0, U_{Bbix}^0 , volts	-1.88	-1.67	-10
Current used I_{nor}, ma	–	25	75
Time of propagation delay when connected, $t_{3\mathcal{A}p}^{1,0}$, nanoseconds	–	2.9	25
Time of propagation delay when disconnected $t_{3\mathcal{A}p}^{0,1}$, nanoseconds	–	2.9	25
Output branching coefficient		15	75 -10
Power consumed P_{nor} , milliwatts (per logic element OR-NOT/OR)	–	35	25

The output characteristics of the key at the transistor VT8 output (see Fig. 3.21) are shown in Fig. 3.28c. Depending upon the value of the given voltage at the output, current I_{Bbix} will flow into or out of the circuit. At each circuit state, the reduction in U_{Bbix} at the VT8 transistor output leads to this transistor being more conductive, and an increase in outflowing output current I_{Bbix}. An increase in U_{Bbix} makes this transistor less conducting and increases the inflowing output current I_{Bbix} . A further increase in U_{Bbix} may make the emitter repeater fully nonconducting, after which the current will be determined by the load impedance which will determine the slope of characteristic $I_{Bbix} (U_{Bbix})$.

The low output impedance of the emitter provides a high loading capacity of the ESTL circuits on DC. However, the actual loading capacity in the dynamic mode, due to the input capacitance of the circuit and the capacitance of the wiring is reduced to K_{pa3} = 15.

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We will now consider the dynamic parameters of the ESTL circuits. The basic parameter that determines the dynamic properties of the circuit is the propagation delay time when connecting and disconnecting ($t^{1,0}_{3\text{Д} P}$, $t^{0,1}_{3\text{Д}P}$). ESTL circuits are the quickest digital IC. At normal conditions and load impedance R_H= 51 ohms, their typical propagation delay time is 7 nanoseconds. The delay time is measured at the level of 50% from the full gradient of the logic level when the circuit is switched.

It may be seen from the characteristics shown in Fig. 3.29 that the greatest effect on the propagation delay is produced by a change in the feed voltage, the voltage bias level and by an increase in the capacitive loading.

ESTL series 100, K500 are considered to have identical electrical parameters and differ only in functional composition, the type of housing and the operating conditions. Table 3.16 shows the values of the operating electrical parameters of the basic logic element of series 100 and K500 in a temperature range. The limiting allowable modes of operation for the ESTL series is shown below:

Maximum feed voltage, $U_{\text{ип}}$, volts	-7 for 5 millisec; -6 constantly
Maximum input voltage $U_{\text{вх } max}$, volts	0
Minimum input voltage $U_{\text{в1 } min}$, volts	-5.5
Maximum output current $I_{\text{вых } max}$, milliamp	40

3.5.3. Certain Special Features in the Use of IC type ESTL

We will consider the special features of using IC type ESTL on an example of the series 100. As already mentioned above, ESTL circuits have a negative feed voltage source of -5.2 volts $\pm$ 5% and, because of this, negative voltages of logic levels. Moreover, ESTL circuits logic levels are low in absolute value($U^1_{\text{вых}} \approx$ - 1 volt and $U^0_{\text{вых}}$ =-1.65 volts). All this does not allow direct connection to inputs and outputs of IC type ESTL to IC type TTL or the use of MOS structures. For the mutual interfacing of logics, special circuits of converter 100ПУ124 and 100ПУ125 must be used. In wiring apparatus of IC series 100 (besides IC types 100ЛП115, 100ЛП116 and 100ЛП124) all unused inputs and outputs are left free.

Unused inputs of IC types 100ЛП115 and 100ЛП116 must be connected to a reference voltage source (leadout 9 of IC type 100ЛП115 and leadout 11 of IC type 100ЛП116) or to feed voltage source $U_{\text{ип}}$ = -5.2 volts $\pm$ 5%. Unused inputs of IC type 100ПУ124 are connected to feed source $U_{\text{ип}}$ = 5.0 volts $\pm$ 5% through a resistor rated at 1 kohm. No more than 20 unused inputs may be connected to one resistor. If it is necessary to feed a constant signal 0 to inputs of several IC, it may be obtained from any logic IC series 100 that forms signal 0 with the connected inputs. The number of loads which may be connected to the output of such an element should not exceed 24.
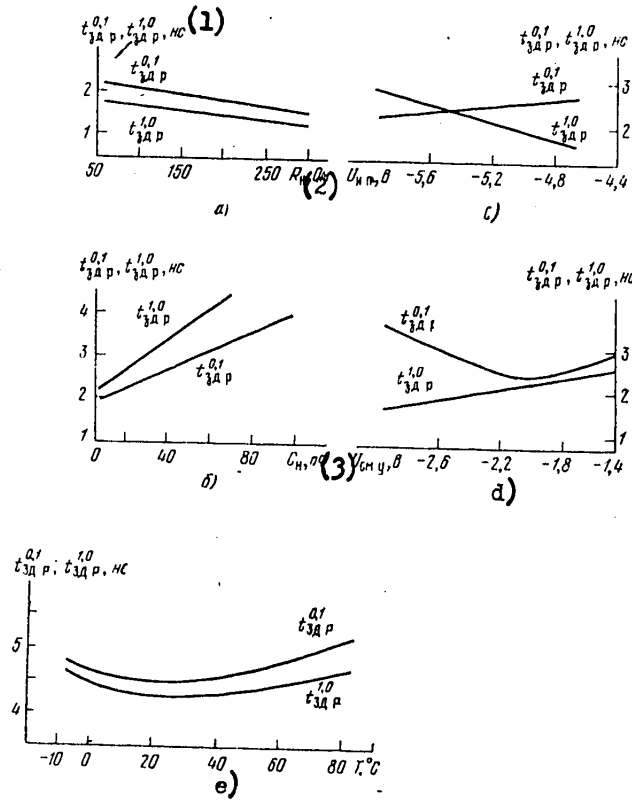
Fig. 3.29. Relationships between dynamic parameters and: resistive load (a),
load capacitance (b); voltage feed source (c); bias voltage (d);
and temperature (e).

1. nanoseconds   3. picofarads
2. ohms

The ESTL microcircuits considered above allow a combination of direct and inverse
outputs into a "wired OR" and a "wired AND" with a combination coefficient $K_{o\sigma} \leqslant$

$\leqslant 4$, as well as a combination of a direct output with an inverse one (Fig. 3.30).
The latter combination method makes it possible to receive and transmit signals
from several elements over one common communications line (Fig. 3.31a).
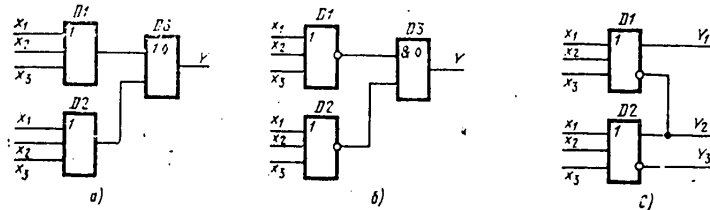
Fig. 3.30. Combination of IC type ESTL outputs into a "wired OR" (a) into a "wired AND' (b), a combination of direct and inverse outputs (c).

It should be remembered that as the number of combined outputs is increased, the levels of output voltage change, which leads to a reduction in the noise resistance of the IC. Moreover, in the "wired OR" operating mode when even one IC is switched from state 1 to state 0, a negative interference appears at the output of the combined circuits (Fig. 3.31b) which may cause a false operation of the load element. The amplitude and duration of the interference depends on the length of the communications line that connects the elements in the "wired OR." Taking the above into account, it is recommended to combine outputs within one board and, if possible, outputs of IC which are beside each other. Taking the output from the board of an IC that does not have an output combination is recommended.
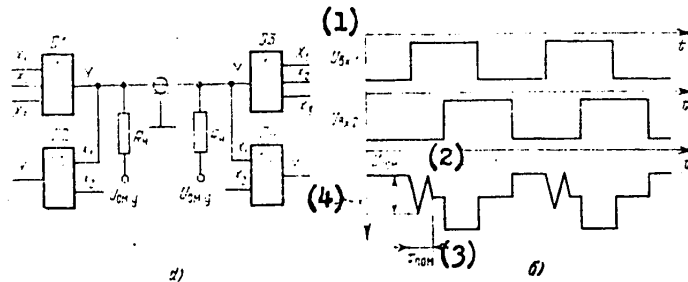
Fig. 3.31. Circuit for signal transmission from several IC type ESTL over one common communications line (a) and a time diagram (b)

1. $U_{\text{в}X}$ -- input voltage

2. $U_{\text{пом}}$ -- interference voltage

3. $U_{\text{вых}}$ -- output voltage

4. $\tau_{\text{пом}}$ -- interference time

As already mentioned above, ESTL circuits have a fairly high load capacity ($K_{pag} \geq 10$) which is due to the low input impedance of the emitter repeaters with which the keys are equipped and the low values of the input current (less than 265 microamperes). Within one board, the load capacity increases to $K_{pag} = 20$ and for microcircuits 100LL110 and 100LYel11, designed to operate simultaneously on three transmission lines, the load capacity is still higher ($K_{pag} = 30$).
It is recommended that the output of trigger circuits be loaded no more than with 6 inputs of IC loads. It is recommended to connect inputs of no more than 16 keyloads to the output of circuits, combined in a "wired OR." In this case, the reduced level of the output voltage and an increase in the propagation delay time should be taken into account.

When the logic element operates with a load resistor rated at 51 ohms (at $U_{cM y} = -2$ volts) the delay increase when connecting one input of the IC load is 0.1 nanoseconds, while the change in the duration of the output signal front for an increase in the load from 1 to 10 inputs does not exceed 0.5 nanoseconds. In all cases, when determining the allowable number of inputs that may be connected to the IC output, it is necessary to take into account the combination of several inputs within these IC. With the direct operation of elements with one another (over short lines of communications), resistors of various ratings connected to voltage sources $U_{un} = -5.2$ volts or to $U_{cH y} = -2.0$ volts may be used in the emitter circuits of the output repeaters.

The presence in the above-considered ESTL series triggers and logic elements of various types makes it easy to design typical functional computer units and discrete automatic system devices. Fig. 3.32 shows a 4-stage shift register circuit. The output part of the circuit is made up of 100TM131 triggers, the parallel data input circuit -- is made up of IC type 100LS119, while the output part is a decoder with two inputs and four outputs made of IC type 100LM105. To increase the number of register stages, data is fed to input D_{n-1} from the output of the previous stage and to input D_{n-4} from the output of the following stage. Depending on the type of signal, operations, enumerated in Table 3.17, are implemented at inputs S_1 and S_2 by the circuit.

Synchronous binary pulse counter (Fig. 3.33) is made of IC types 100TM131 (D5, D6, D8.1), 100LS118 (D1...D4) and 100LM105 (D7). Input Q_{n-1} implements the carry from the previous stage and output Q_{n-4} -- the carry to the following stage. The counter operation is controlled at input S of IC100LM105. With 1 at the S input, the circuit implements the function of a counter. With 0 at the S input, the circuit operates as four triggers and receives data in inputs $D_0 \ldots D_3$.

The combined utilization of ESTL and TTL circuits (Fig. 3.34) makes it possible to design special purpose units. Fig. 3.34a shows an indication circuit, designed with IC type 100PU125 (D1) (series ESTL) and IC type 133LA7 (D2) (series TTL) using the NSM 6,3-20 incandescent lamp as an indicator.
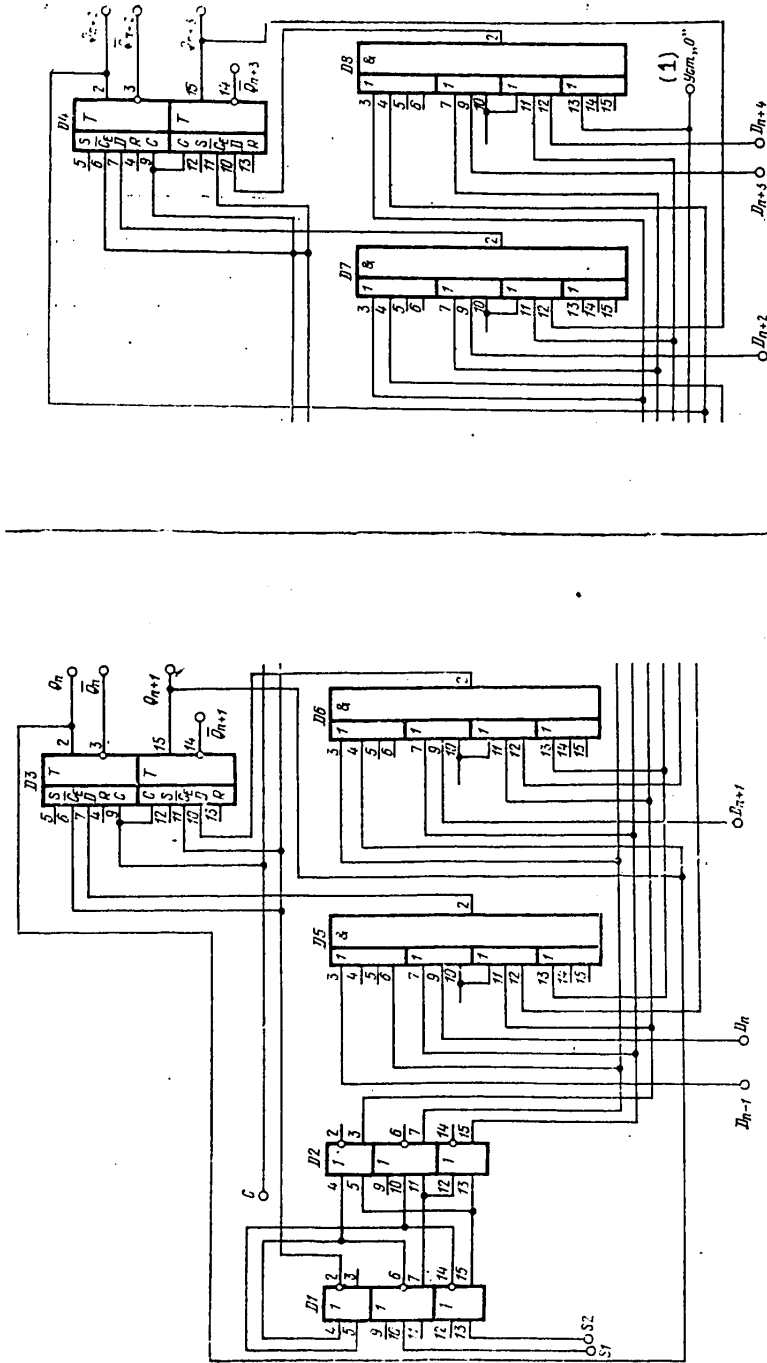
Fig. 3.32.   Circuit of a 4-stage shift register, made of triggers 100TM131 (D3, D4), IС100LM105
(D1, D2) IС100LS119 (D5...D8).

1.   Set 0

Table 3. 17

Operations implemented by the four-stage shift register, depending on signals S_1 and S_2

Inputs		Implemented operation
S_1	S_2	
0	0	Blocking
1	0	Shift right
0	1	Shift left
1	1	Data received in inputs D (the circuit operates as four triggers with separate inputs and outputs)

Table 3.18

Rated resistance resistors R1 and R2 with parallel matching

P, ohms	R_1, ohms	R_2, ohms
50	81	130
75	121	195
100	162	260
150	243	390

Taking into account the high-speed action of the ESTL circuits, special attention should be given to the arrangment of the communications lines between individual IC, as well as to boards and units. Circuits types 100LP115 and 100LP116 which are paraphase signal receivers from a two-wire communications line, were considered previously. However, data transfer between individual circuit boards may be implemented by single-phase signals (Fig. 3.34b).

When a single-phase signal is fed from the output of IC series 100 (D1...D3) to one of the inputs of the IC types 1ooLP115 (D5...D7) or 100LP116, a reference voltage must be fed to the second input, produced in IC type 100LP115 (leadout 9) or 100 LP116 (leadout 11) located in the board from which the signal is transmitted Fig. 3.34b). One reference voltage source on the transmitting board (D4) may be loaded in the receiving board with no more than 10 inputs. Each IC type 100LP115 or 100LP116 may be used as a reference voltage source (D4) when transmitting beyond the limits of the board and as a signal receiver from the communications line (D5...D7). The reference voltage transmission line must be decoupled at the transmitting and receiving ends by no less than 1000 picofarad capacitors.

Three basic communications methods are recommended within the limits of one board. The series method is used for a communications line not over 200 millimeters
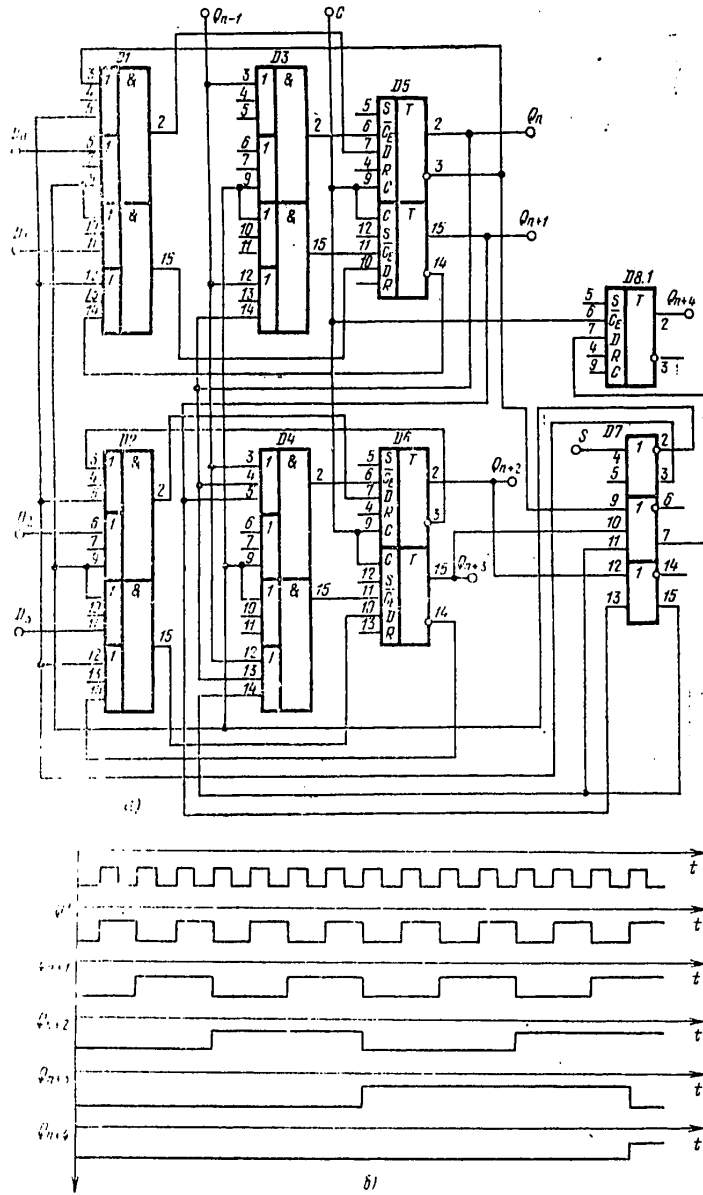
Fig. 3.33. Synchronous binary pulse counter from 0 to 15 (a) and time diagram of counter operation (b).

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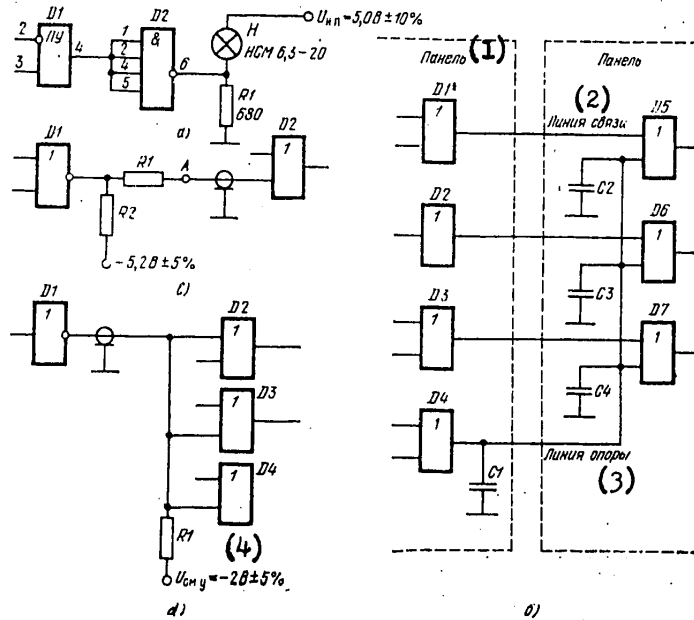
Fig. 3.34. Some ESTL connection circuits:
a -- indication circuit; b -- data transfer circuit between two boards of the device; c and d -- series and parallel matching of communications lines.

1. Panel
2. Communications line

3. Reference line
4. -2 volts

between the IC signal source and the load resistor. IC loads are connected along this communications line. The recommended length of the communications line should not be greater than 30 mm. In the beam method, beam lines no longer than 70 mm branch out at the end of which are connected IC loads. The load resistor is connected to one of the IC loads. Finally, in the concentration method, from the point of connection of the load resistor, at the end of communications line 200 mm long, communications lines also 200 mm long branch out to IC loads.

To eliminate "ringing" at the signal receiver input, it is recommended that the data be transmitted over a matched communications line. Fig. 3.34c, d shows circuits for implementing the series and parallel methods for matching communications lines. For communications lines with wave impedance P = 50 ohms, rated resistors R_1= 43 ohms and R_2 = 240 ohms (with series matching) and R_1 = 51 ohms (with parallel matching) are used. Another method for parallel matching (by means of two resistors, R1 and R2, connected at the end of the line) is allowed, using the voltage of the bias level source U_{cmy} = -5.2 volts $\pm$ 5% to which resistor R2 is connected. The recommended values of resistors R1 and R2, depending on the wave impedance of the line, are shown in Table 3.18.

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PROVIDING RELIABILITY OF INTEGRATED CIRCUITS IN THEIR PRODUCTION AND IN ASSEMBLY OF APPARATUSES

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[Text] Chapter 5

Providing Reliability of IC [Integrated circuits] in the Production and Assembly of Apparatus

5.1. Design-Technological Principles of High Reliability

High reliability of semiconductor IC is one of main reasons they became the basis of modern radioelectronic apparatus. The high reliability of IC is insured by the group method of producing IC elements, by a smaller number of interelement connections and the lower level of power consumed.

In the group production method, all IC elements are manufactured in one technological cycle under rigidly controlled conditions, and with a minimum use of manual labor. The physio-chemical compatibility of materials and processes provide equal reliability of all IC elements. The reliability of the functional device, assembled with discrete parts, depends on the quality of the complementing electric-radio elements (ERE) which are manufactured at many enterprises at different times on dissimilar equipment. The connections between the contact pads on the semiconductor IC chip are made by thermocompression (or ultrasonic) welding. Vacuum spraying of metal and thermocompression welding provide a reliable connection of the elements. If we compare a usual unit and an integrated circuit containing a thousand equivalent ERE, then in integrated circuits, the number of interconnections by the "usual" method is reduced to 1-100th-1/150th. As a result, the reliability of the apparatus is increased because the number of the most probable sources of failures -- interelement connections -- is reduced considerably, moreover, they are made by the most perfect methods.

A number of IC types are characterized by low power consumption. With low dissipation power, the operating temperature of a chip increases little compared to the ambient temperature and, therefore, conditions are favorable for retardation of the physio-chemical processes leading to failures.

The actual reliability of IC as the property to implement given functions and to preserve its parameters within given limits with time, determined by the operating conditions, depends on many factors: the perfection of the circuit, the quality of the initial materials and the complementing components, and the quality and stability of the technological process of IC manufacture.

In IC production, monitoring operations are carried out not only at the end of the final stage of manufacture, but are converted to a quality control operation over the entire technological process. However, the technological process control is clearly insufficient because in the IC manufacturing process, not only are operator errors possible but also random deviations, related to the quality of the materials and working equipment. Therefore, a single system of checks and rejections of the finished products is introduced in each technological process of semiconductor manufacture to detect IC with apparent as well as hidden defects if possible. For this purpose single norms and methods of boundary tests were established that make it possible to determine reserves of electrical and mechanical properties when developing new articles, and check the efficiency of these or other measures introduced in the technological process in series production of IC.

The true reliability of IC is determined only in operating the apparatus. First of all, it must be concluded that the reliability of IC in operating various series (made at various semiconductor plants) is practically the same in devices developed in one and the same apparatus enterprise. At the same time, the reliability of IC of one and the same series in apparatus, manufactured at various plants, is found to be very different. This is the result of differences in the technological standard of manufacture of the apparatus which can also be made in nonspecialized enterprises.

The use of highly reliable IC does not always automatically provide such reliable apparatus. The preservation of the reliability of IC in the apparatus is determined, to a considerable degree, by their proper use at all stages of development, production and operation. The proper use of IC here means the implementation of recommendations on electrical modes and assembling methods, a debugged technological process of manufacture of the apparatus and the use of measures to protect IC from static electricity, thermal and other effects. Achieving and maintain maximum operational reliability of IC (and consequently, the quality of the apparatus) depends greatly on the level of the processes of the design of the apparatus, its preparation for production and the tune-up of the equipment and the skill of the personnel.

The purpose of this chapter is to acquaint the reader with several measures taken to insure the reliability of integrated circuits, as well as to make the necessary recommendations on using IC when manufacturing the apparatus.

5.2 Operational Quality Control

To achieve a given level of IC quality in all production lots along with a thorough finishing off of the product design and the improvement of the technological process, a rigid operation by operation quality control is used in production. Due to this, an unsuitable product is rejected at certain stages of the production cycle. Moreover, constant quality control over the parameters of the technological process (for example, temperature, time intervals, gas consumption), technical condition of equipment, and a check   of the skill of the operators is carried out.

Table 5.1 lists the basic stages of the technological processes, the monitored characteristics, and gives the criteria for evaluating the proper progress of the process. The number of monitoring stages, the volume and type of monitoring (continuous or selective) are determined in each concrete case depending upon the required level of reliability of the IC (standard or especially reliable), the type and importance of the stage of technological process.

The second stage of production quality control is establishing relationships between types of IC failures, the parameters of the technological process and developing recommendations to correct them. An analysis of causes for IC failures is objective information that makes it possible to improve the technological processes. Table 5.2 shows an example of the plan-schedule of measures directed toward the elimination of causes of failures of semiconductor IC. The data in Table 5.2 must be analyzed along with the figures, references to which are given in the table. These diagrams show the relative change in the share of IC failures of a certain type, depending upon the period of implementation of the measures. The measures in Table 5.2 are numbered for convenience of analysis. The effectiveness of the internal measures is illustrated in Table 5.3 where the dynamics of the reduction in IC failures for the three above-mentioned causes is shown.

5.3 Rejection Tests

IC manufacturers are interested in the best technological processes and strive to have   thorough production quality control for the purpose of increasing the percentage of finished product yield, and reducing the rate of IC failures.

However, demands for reliable IC from the users cannot be satisfied only by improving the production process and the system of operation by operation quality control. A system of rejection tests of the finished product as a means of increasing the reliability of the product as compared to the level considered standard at the given moment plays a great role in solving such problems.

Rejection tests of IC are intended mainly for early detection of (preworking) failures, caused by operator error as well as by random deviations related to the quality of the initial materials and the operation of the equipment in the process of IC manufacture. The introduction of rejection tests for the entire product is based on the fact that the rate of IC failures, in the general case, decreases with time. Fig. 5.2 shows the characteristic distribution of IC failures in production and the tests of one of the samples of the apparatus. The greatest number of

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failures (up to 80%) occurs at the stage of production and tests of small assembly units of the apparatus and decreases noticeably when these units are consolidated (curves 1, 2 and 3) as well as for the entire product (curve 4). With the rejection tests, it is possible to remove microcircuits from the production lot that have hidden defects and thus increase the reliability of the apparatus, "shifting" the failures of breaking in to the stage of rejection testing.

Table 5.4 shows an example of the composition and conditions of rejection tests to which 100% of the IC produced are subjected. As may be seen from Table 5.4, rejection tests are made in a logical sequence and are interdependent. Methods and modes are used for rejection tests that take into account the special features of the manufacturing technology and IC design. Here hidden IC defects are detected, but not failures that are not inherent in the given technology and design. The selection of methods and conditions of tests are based on the knowledge of the physical nature of the IC failures which originate at various kinds of climatic, mechanical and electrical effects. The levels of external effects are selected by the results of IC tests so that there remain certain stability reserves.

In setting up the sequence of carrying out the rejection tests, it proceeds on the basis that they must begin with such types of effects which will make it possible to eliminate immediately IC with hidden defects that cause the greatest percentage of failures in operation. At the final test stages, methods are used that will make it possible to eliminate poor IC whose defects were not detected in the previous tests from the production lots. Rejection tests include methods that facilitate the stabilization of electrical parameters and reduce the spread of their values.

The first rejection test is visual inspection after the operation of dividing the wafers into chips and before the sealing operation. Experience shows that this type of inspection is one of the most important methods that makes it possible to detect many production defects which cannot always be detected electrically or in other types of tests.

Visual inspection makes it possible to reject IC in which the following violations were detected: defects of chip metal-coating (scratches and voids in metal-coated tracks and contact pads, signs of corrosion and flaking, unetched sections of metal coatings, shifting in the metal-coated layout), scribing defects (cracks in the active area of the circuit, under contact pads and metal coating, splits and damage to the chip) or diffusion defects (nonuniform and parasitic diffusion). In some places there may be no passivated protective oxide on a part of the p-n junction, shifts of layers in photolithography, and defects in the protective dielectric film may be seen (remnants of the dielectric film on contact pads, scratches and holes).

Insulation defects can be found in IC chips (absence of separating insulation, contamination of the surface of the chip), fixed or loose particles of foreign material on the chip's surface, defects of welded joints on the chip and housing leadouts, as well as defects of wire leadouts (the sag is greater or smaller than the norm; uneven flexibility of the wire, grooves, reduction in diameter; distance between wire leadouts that are less than the norm).

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Table 5.1

Stages of the technological process and the approximate volume of operation by operation quality control,characteristic for IC production

Monitored characteristics	Evaluation criterion
Manufacturing of semiconductor wafers	
Thickness, plane-parallel, roughness	Percent of set value
Structure defects: linear, displacements, inclusions	Number per unit area
Surface orientation	Percent of average value
Specific resistance	Percent of set value
Equipment	Meeting technical condition requirements
Passivation (oxidation) of surface	
Equipment operation mode: change of temperature with time	Allowable deviation range
Velocity of gas flow up to the start and in the process of oxidation	Allowable deviation of gas flow velocity
Thickness of the raised (or precipitated) layer	Allowable deviation from norm
Density of microholes and cracks	Allowable number of defects per unit area
Size of microholes	Maximum allowable size of holes
Equipment	Meeting technical condition requirements
Photolithography	
Sizes, combination, quality of etching, microholes, presence of foreign particles	Meeting requirements of visual inspection
Properties of solvents; specific weight, viscosity, solid particle sediment, storage temperature	Correspondence to certificate
Modes of drying and exposing: temperature time	Allowable deviation from the norm
Exposition modes: intensity of light, time	
Adhesion quality	Force for peeling film
Modes of etching processes: density (frequency of etching sections), temperature, time (velocity of etching each level of passivation or metal coating).	Allowable deviations from the norm
Conditions for making each type of mask: relative humidity, temperature, dust in the environment; quality of surface (density and diameter of microholes, roughness of edges	Same Meeting requirements of visual inspection

Table 5.1 continued

Monitored characteristics	Evaluation criteria

Epitaxial build-up

Conditions and storage time	Allowable deviation
Thickness of epitaxial layer	Percent of set value
Specific resistance	Same
Defects of packing, dislocation, holes, bulges, pits, depressions, scratches, irregular edges	Meets of requirements of visual inspection
Equipment mode: temperature of the epitaxial tube, composition and parameters of the gas flow	Allowable deviation

Diffusion

Depth of diffusion junctions of emitter and base	Same
Specific resistance	Percent of set value
Equipment mode: temperature of diffusion tube, composition and parameters of the gas flow	Allowable deviation

Metal coating

Purity of wafer, temperature of wafer and metal, film thickness (including along the edges of the contact windows) -- effect of shading	Meeting requirements of visual inspection and force for peeling the films

Scribing

When scribing with a diamond cutter: slope angle, pressure, velocity and direction of cutter movement. When scribing by quantum optical oscillator beam: power and resolution capacity of beam; depth and width of scribing; mechanical damage; cracks, metal scaling, chips, scratches	Meeting requirements of visual inspection

Chip assembly

Temperature, time, ultrasonic power, chip orientation, ambient parameters	Allowable deviations

Connection of internal leadouts

Temperature, pressure, time for making connection, metal composition, rupture force, ambient parameters	Same

Table 5.2

Approximate plan-schedule of measures directed to the elimination of IC failures

Type of IC failure	Correcting measures	Period of introducing measures
1. Rupture of wire leadout due to failures of the thermocompression connection (see Fig. 5.1a)	1.1. Rejection of potentially unreliable IC by centrifuging	IV quarter of 1927
	1.2. Monitoring the rupture force of the gold wire	I quarter of 1973
	1.3. Monitoring the detachment force of the thermocompression connection	I quarter of 1973
	1.4. Change in the design of the welding tool (needle) to increase the detachment force of the thermocompression connection	
	1.5. Introduction of the technological operation of "dropping" an IC on an oaken board from a height of 1 meter	IV quarter of 1973
	1.6. Introduction of a process of continuous degreasing and annealing the gold wire	II quarter of 1975
2. Rupture of plating due to poor adhesion (Fig. 5.1b)	2.1 Introduction of a process for spraying on aluminum by an electron beam	IV quarter of 1972
	2.2. Introduction of group spraying on by electron beam from a water-cooled crucible	I quarter of 1974
3. Rupture of connection due to formation of intermetallic phases at the interface of dissimilar metals (see Fig. 5.1c)	3.1. Reduction in annealing temperature	IV quarter 1973
	3.2. Reduction of burn-in temperature of aluminum and replacing oxygen medium by nitrogen	IV quarter 1974
	3.3. Stabilization and monitoring the temperature of the tool and changing the heating mode in the process of setting the chip on the base	IV quarter 1974

Table 5.3

Dynamics of reducing IC failures

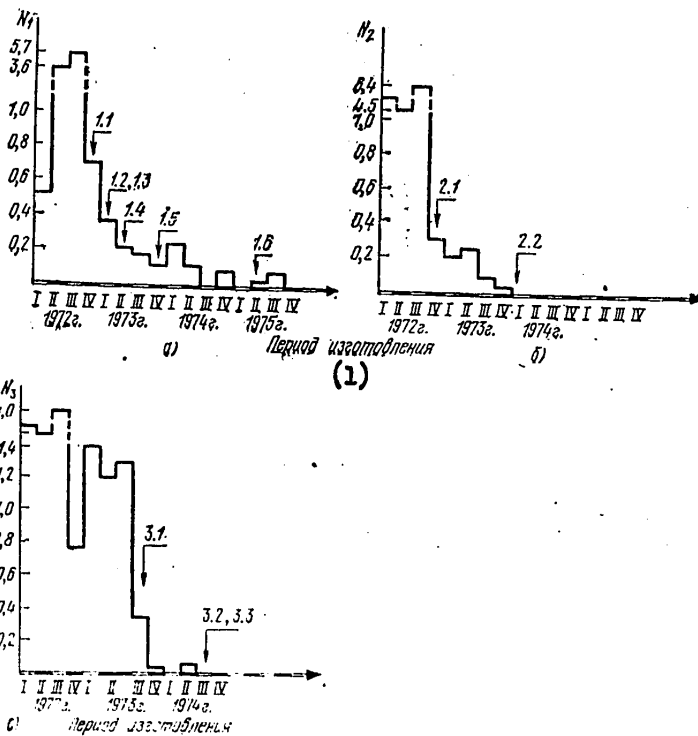| Type of failure	Share of IC failures of a certain type (% of all failures) by years			
	1972	1973	1974	1975
Rupture of wire leadout due to thermocompression connection defects	13.7	4.1	4.7	2.8
Rupture of plating due to poor adhesion	18.8	2.7	0	0
Rupture of connections due to the formation of intermediate phases at the interface of dissimilar materials	10.1	19.6	1.2	0

Fig. 5.1. Reduction in the number of IC failures (N) occurring for various reasons depending upon the use of correction measures: a -- break in thermopressure welding; b -- break in connections due to poor adhesion; c -- break in connections due to the presence of intermetallic phases. 1. Period of manufacturing.

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Table 5.4

Rejection tests

Type	Conditions
Visual IC inspection before sealing	Inspection of chips under a microscope (not less than 80 magnification) to meet requirements on limiting the number of defects of each type and their total number, shown in specification
Annealing for parameter stabilization: before sealing	Hold IC at a temperature exceeding upper value in specification for 48 hours
After sealing	Hold IC at upper value of temperature for 24 hours
Cyclic temperature effect	Alternate effect of upper and lower values of ambient temperature (transfer from one chamber to another for not more than 3 minutes). Number of continuously following cycles - 5
Line loads	Effect of line loads with accelerations of 10,000... 20,000 g in the direction of the vertical IC axis for 1 minute
Seal check: small leaks	Check seal within $1 \times 10^{-3} ... 1 \times 10^{-7}$ liters. μ m/second by the mass-spectrometer method
Average leaks	Check IC seal, pressure-molded in Freon, in an indication liquid. Determine seal at 1×10^{-2} liters. μ m/second
Large leaks	Check seal in an indicator liquid
Measurement of electrical parameter	Monitor IC parameters according to specifications at normal temperature
Electrical thermal aging tests for higher reliability IC	IC test at constant electrical load and maximum allowable temperature
Measurement of electrical parameters	Check of meeting electrical parameters of IC in accordance with specification
Static parameters	Check at the lower and upper values of ambient temperature in specification
Dynamic parameters	Check at normal ambient temperature
Exterior visual inspection	Check of structural elements (welded and soldered seams and joints between glass and metal) under a microscope with magnification not less than 16. Visual inspection of coatings and labeling

Defects in chip connection (chip orientation not according to design drawing, leadout crosses, the eutectic covers less than the allowable part of the chip perimeters, too much paste and glass, defects of the housing base (deformation of the housing, peeling of the gold coating, shifts of the coating and eutectic), defects of the housing (absence of leadouts, corrosions, presence of drops of glue, tin on the flangeoof the housing on the side of the cover), as well as defects in assembly (chip on board glued too high, board bent) that originate in inaccurate assembling of IC.

After annealing to stabilize, parameters and sealing, IC are subjected, in turn, to the effects of their high and low values of ambient temperatures to detect a mismatch between thermal expansion coefficients of individual IC parts. After these tests, the IC must preserve their external appearance and the electrical parameters.

The mechanical integrity of the design is checked by testing on a centrifuge. The microcircuits are attached to the housing in a special device and are subjected to the effect of linear loads which produce forces along the vertical IC axis corresponding to accelerations of 10,000 g for hybrid, and 20,000 g for semiconductor microcircircuits. These forces are usually sufficient to detect defects of welded connections of internal leadouts and poorly attached chips.

In testing IC, devices with improper seals are rejected. The widest failure mechanism in such IC is due to the moist air penetrating the housing and water vapor condensing causing corrosion of the metal coating. Further electrical tests are made in which IC not corresponding to technical norm documentation (INTD) are rejected.

After that, IC which are to meet higher reliability requirements are subjected to special electrical thermal tests which are tested until they fail. This type of testing shows defects not detected in visual inspection very effectively. Typical defects which may be overlooked in visual inspection (but may be detected in thermal current tests) are scratches on the metal coating, thinner metal coating on the oxidation treads and microholes in the oxide under the metal-coated tracks. These defects may also include poor electrical contacts and surface contaminations that cause instability of IC parameters

The final type of test is an all-around investigation of basic IC electricl parameters under normal climatic conditions, as well as at the upper and lower values of the temperature in the specification. Electrical tests are also made at a combination of electrical modes (input signals, loads, feed voltages) which are the worst for the given type of test within the limits of specifications. Rejection tests are completed by checking commercial type IC, with special attention being given to inspecting the quality of welded and soldered joints, glass in the metal joints, the labeling and integrity of the coatings of the leadouts and the housings.

By analyzing typical experimetal data that characterize the effectiveness of rejection tests in the process of production (Table 5.5), it is possible to conclude that the complex of rejection tests makes it possible to detect a considerable number (including 43.2% of the number tested) of potentially unreliable IC and thus raise considerably the quality of IC lots supplied for use in the REA.

Table 5.5

Effectiveness of rejection tests

Type of test	Share of defective IC	Basic types of defects and their share, %
Visual inspection of quality of connecting leadouts	5	Absence (unwelded) connection -- 26.4 Repeated thermocompression -- 17.0 Shift of leadout beyond area of contact pad -- 13.6 Pinched leadout -- 10.6 Shift of welded joints on the crosspieces -- 8.0 Others -- 24.4
Visual inspection of chips	3.7	Splits -- 10.7 Photolithography defects -- 10.7 Others -- 29
Annealing for stabilizing parameters:		
before sealing	0.0	-
after sealing	0.0	-
Cyclic effect of temperature	0.0	-
Linear loads	0.0	-
Leak tests:		
small leaks	7.0	Not in accordance with norm
medium and large leaks	1.9	same
Monitoring electrical parameters at normal conditions	7.4	-
Electrical thermal aging	0.7	-
Electrical tests:		
check of static parameters at higher temperature	0.6	-
Check of static parameters at lower temperatures	4.7	-
Check of dynamic parameters	1.6	-
Inspection of exterior of IC	10.6	Splits and cracks in housing -- 54.4 Twisted leadouts -- 16.0 Labeling defects -- 9.4 Damaged coatings -- 20.2
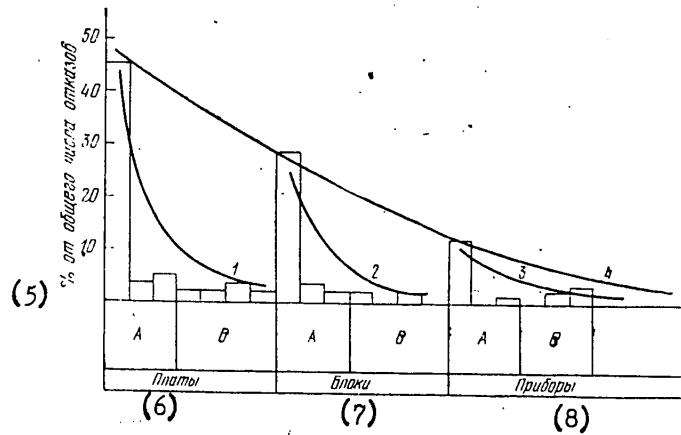
Fig. 5.2. Distribution of IC failures in production and testing of apparatus:

1. failures of printed boards

2. failures in units
3. failures in devices
4. total number of failures
A. shop test stage

B. stage when product is released
    to quality control department

5. % of total number of failures

6. circuit boards
7. units
8. devices

Inasmuch as rejection tests using   above-cited methods are compulsory for all
manufccturing plants, the IC quality of various suppliers is equalized to a consid-
erable extent. Now IC that have passed through one and the same "rejection bar-
rier" at various plants have a similar quality level.

5.4 Effect of External Factors on Apparatus Production

A typical technological process of apparatus manufacture using small-scale mecha-
nization tools is shown in Fig. 5.3.
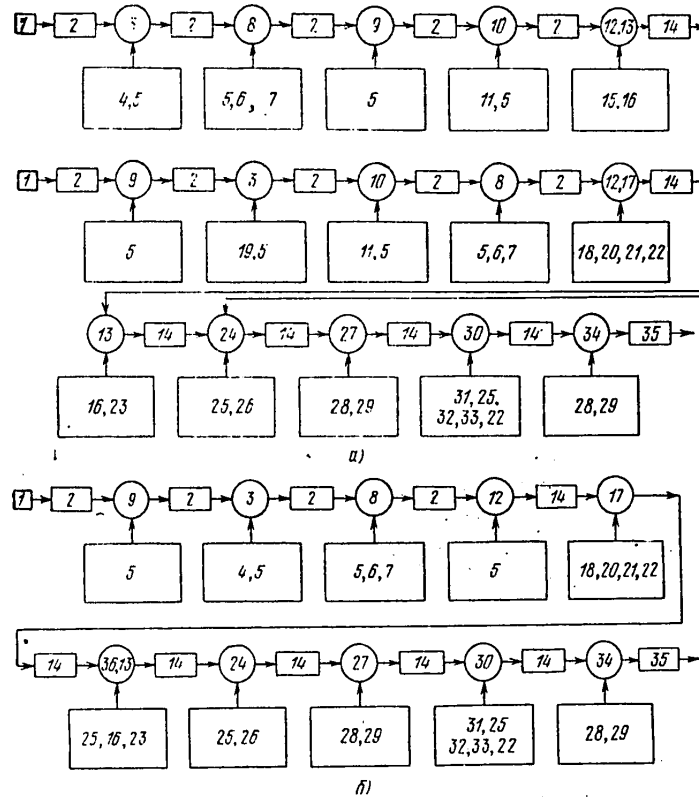
Fig. 5.3. Technological route of passage of IC circuit in manufacturing apparatus in housings types 1 and 3 (a) and housings type 4 (b):

1. IC
2. technological packing
3. forming and trimming leadouts
4. die for forming and trimming the size
5. magnetic vacuum or optic tweezers
6. crucible with thermal regulator
7. device for tinning
8. tinning leadouts

9. making up sets
10. trimming inactive leadouts
11. die with keying device
12. installation
13. soldering
14. board

19. die forming and trimming to size
20. spatula
21. device for gluing
22. thermostat

23. semiautomatic soldering device
24. cleaning flux from boards
25. brush
26. vat
27. regulation
28. control panels, devices
29. hot-cold chamber
30. protection against moisture
31. paint and varnish
32. centrifuge
33. pulverizer

Key to Fig. 5.3. continued

15. device for soldering IC without
     gluing
16. electric soldering device single-core
17. gluing
18. injector

34. functioning and control check

35. assembly unit
36. fluxing

The sequence of operations and transfers indicated in the technological routes of circuits may change depending on the special design features of the assembly units and the specifics of production. In passing over these routes, the IC are subjected to the effects of various external factors: mechanical, temperature, chemical and electrical (Table 5.6).

Mechanical forces are applied to IC in assembly operations, forming and trimming leadouts, and mounting and gluing the IC to the printed circuit board. Forces acting on leadouts and their insulation may damage the sealing of the housing. Temperature effects are related to the operations of tinning, soldering and dismantling. In these operations, heat passes through the leadouts to the chip or substrate and produces heating of the structural elements of the IC. Chemicals affect the plating material of the housings and the IC labeling when fluxing, cleaning the flux off the printed circuit boards, applying moisture protection and dismantling. And, finally, electrical effects are related to discharges of static electricity through the IC. This effect also takes place at all technological operations if no special measures are taken to reduce and remove static electricity charges from production areas.

As may be seen from Table 5.6, IC are subjected many times, although to a different degree, to effects of external factors in the environment. The most dangerous of them are the actions of the operator because they depend to the greatest degree on the individual preparation of the operator and they are the most difficult to control.

In the process of apparatus production, if the modes and equipment quality do not correspond to the problem of producing highly reliable apparatus, various kinds of IC defects and failutes may originate (Table 5.7).

5.5 Forming and Trimming Leadouts

One basic requirement that the IC housing must satisfy is the preservation within it of comparatively dry air during its entire service life. The presence within the housing of moisture, chemically active and electrically incompatible with semi-conductor substances facilitate the origination of sudden, as well as gradual, failures. They happen due to the corrosion of metals and their alloys and inter-contact connections, and the deterioration of electrical characteristics caused by changes in the surface and volumetric conductivities and ionic contamination.

Under normal conditions, any surface of a substance is covered by a thin moisture of from 0.01 to 0.001 micrometers. Due to the small values of a molecule of

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Table 5.6

External factors acting on IC in the process of apparatus assembly

Source of action	Assembly	Forming and trimming leadouts	Fluxing and tinning wires	Mounting and gluing IC on circuit board	Fluxing and Soldering
Operator	E, M	E	E	E,M	E
Material covers of working positions and rooms	E	-	-	E	E
Packing	E,M	E,M	E,M	E.M	-
Assembly tools	E,M	E,M	E,M,T	E,M	E,M,T
Technological Equipment	-	M,E	E	M	-
Flux	-	-	Kh	-	Kh
Solder	-	-	T	-	T
Washing liquid	-	-	-	-	-
Varnish solvent	-	-	-	-	-
Equipment and materials for moisture protection	-	-	-	-	-

	Cleaning off flux	Regulation	Moisture protection	Functioning test	Disassembly
Operator	E	E	E	E	E,M
Material covers of working positions and rooms	-	-	-	-	E
Packing	-	-	-	-	E,M
Assembly tools	-	-	-	-	E,M,T
Technological equipment	M,E	E	E	E	-
Flux	-	-	-	-	Kh
Solder	-	-	-	-	T

Table 5.6 continued

External factors acting on IC in the process of apparatus assembly

Source of action	Cleaning off flux	Regula-tion	Moisture Protection	Function-ing test	Disassembly
Washing liquid	Kh	-	-	-	-
Varnish solvent	-	-	-	-	Kh
Equipment and materials for moisture protection	--	-	E,M	-	-

Note: designations of actions: E -- electrical; Kh -- chemical; T -- temperature; M -- mechanical.

2.7×10^{-10} meters and the low viscosity of water, moisture is able to penetrate even the intermolecular spaces of complex inorganic compounds. In this case, mechanical destruction of materials occurs, along with a change in the electrical properties of the surfaces, corrosion of metals and their alloys. To avoid this, the sealing of microcircuit housings is usually done in an atmosphere of dry nitrogen in which the water content does not exceed 10 parts per million.

Metals, glass and ceramics used in manufacturing IC housings are practically impenetrable to gas and moisture. Most plastics are hygroscopic to some degree. To preserve a dry inert atmosphere within the housing, the seams between unlike metals should be maximally sealed. According to the adopted norms, a good soldered seal passes not over 1 cm^3 of gaseous helium at a pressure difference of 1 atmosphere in 30 years (practically, this means absolute air impenetrability).

Metals are joined to metals by soldering with soft or brazing solders, hot or cold welding or their combination. Soldering of glass to glass or ceramics is done by melting them at high temperatures, or gluing with low-melting glass. Sealing a metal-glass seam which insulates the leadouts electrically from the IC housing is a complex technical problem. This is because most of the common glass has low coefficients of linear expansion and heat conductivity, while most metals conduct heat well and have high linear expansion coefficient. The difference in the speeds of the heating and cooling of glass and metal parts og soldered joints, and the difference in the linear expansion coefficients leads to mechanical stresses and damage to the joints. As far as IC operatng conditions are concerned, glass and metal are considered compatible if the difference in their linear expansion coefficients do not exceed 4×10^{-7} per centigrade degrees [4].

Usually, in sealing IC leadouts where they come out from the housing, crystallizable glass solders (for example, of the "Piroceram" type) are used. The technology of obtaining such a sealed joint by soldering is based on the formation of a glass-ceramic joint with the crystallization of boron lead-zinc glass. In this method,

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the glass is melted by the heat and spreads thoroughly, wetting the joined surfaces of the ceramics, glass and metals like the metallic solder wets and joins metal parts in common soldering).

When the soldered glass is heated further "devitrification" occurs and centers and crystallization of the seam material are produced. The sizes of the crystals formed are proportional to the time and temperature of the process. The strength of such a sealing seam is determined by its crystalline structure and is twice that of a seam from amorphous glass. Moreover, at mechanical loads, microscopic cracks are formed in joints with noncrystallized glass which create paths for moisture penetration into the housing through the glass. In crystallizable glass, however, the microscopic cracks end at the crystals and do not pass through the joint. By regulating the content of the crystalline phase of the seam material, it is possible to change its temperature linear expansion coefficient (TKR) from 40×10^{-7} to 120×10^{-7} per degree centigrade which agrees well with the TKR values for a great number of glass, ceramics and metals used to make housing parts.

The Kovar alloy (iron, nickel, and cobalt) or the Silmet alloy (iron, nickel and chromium) are most frequently used for IC leadouts. These alloys have low TKR values that agree well in the working and technological temperature range with the expansion coefficients of most glass (the TKR for Kovar is 47×10^{-7} per degree centigrade and for glass - - 46×10^{-7} per degree centigrade).

An essential special feature of most types of IC housings is that part of the leadout length is under the cover of glass (or ceramics). This cover should not be damaged in forming the leadouts.

Contradictory demands are made on the IC housing. Thus, the housing must be sufficiently strong mechanically to withstand loads originating in the apparatus production and operation and, at the same time, it must be as small as possible with a shape permitting the greatest density of REA assembly. This contradiction must be taken into account, providing a complex of technical measures for preserving the reliability of the microcircuits in designing and producing the apparatus.

In implementing the technological operations on preparing the IC for assembling on the printed circuit board (straightening, forming and trimming leadouts), the leadouts are subjected to stretching, bending and compression. In this case, the stretching force P_1 is applied to the most sensitive mechanical forces zone of the housing -- the seal inlet (Fig. 5.4). If the stretching force is excessive, cracks may originate in the glass or ceramics of the housing where the leadouts pass the housing leading to an immediate, or what is worse, a subsequent loss of housing seal.

The die design for forming and trimming leadouts (Fig. 5.5) must insure the production of independent and sequential forces for clamping P_2, forming P_3 and trimming P_4. The values of these forces are selected so that they insure the integrity of leadout plating, apply the minimal stretching force along the leadout axis and obtain a given configuration. In forming and trimming the IC leadouts, it is

Table 5.7

Possible types of IC failures under various effects

Oject of effect	Technological operation	Effect factor parameter	Type of possible violation and failures
		Mechanical	
IC leadouts	Straighten, forming and trimming	Pulling force Clamping force	Insulator cracking, causing loss of housing seal; leadout deformation (pinching, twisting, breakage)
Insulator, housing base, flexible connections, chip or substrate	Mounting and gluing IC to the board, dismantling	Static force of clamping housing to board	Insulator cracking, causing loss of housing seal. Deformation of housing bottom causing cracking and separation of chip, substrate and breakage of flexible conductors. Destruction of housing
		Temperature	
Leadout coating	Input control straightening, forming and trimming	Force of clamping leadout	Dents and scratches on leadouts leading to corrosion
Leadout insulator, chip, suggstrate, active elements and flexible leadouts	Tinning, soldering, dismantling, drying	Overheating the leadout or solder	Insulation cracking, causing loss of housing seal. Peeling of substrate or chip (in case they are glued) from the mounting surface of the housing, causing breakage of leadouts
		Increased operating temperature	Thermal deformation of protective coatings of chips, causing breakage of flexible leadouts
		Chemical	
Coating and labeling	Fluxing, cleaning, moisture-proofing, dismantling	Chemical activity	Corrosion of coating or basic material of leadouts and housing, and destruction of labeling designations and paint-varnish coatings

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Table 5.7 continued

Possible types of IC failures under various effects

Object of effect	Technological operation	Effect factor parameter	Type of possible violation and failures
		Electrical	
Passive and active IC elements, metal coating, p-n junctions, protective oxide	All technological operations	Electrical charge (number of effects, capacitance and resistance in the discharge circuit, voltage difference)	Puncture of oxide, degradation of IC parameters due to puncture in the semiconductor structure

permitted to leave tool traces (prints) on the IC leadouts, that do not damage the plating on the leadouts. Table 5.8 shows allowable values of clamping and forming forces at which damage of plating does not lead to corrosion. Depending upon the cross section of the IC leadouts, the value of stretching force P_1 should not exceed the values shown in Table 5.9.

Table 5.8

Allowable forces of forming and clamping

Sequence of force actions	Cross section of housing leadouts, mm	Clamping N	microPa	Forming N	MicroPa
Weak traces of working parts of the die on the surface of leadouts in the form of compacting the coating	0.1x0.3 0.15x0.45	13.7 19.6	30.4 30.4	18.6 27.4	29.4 29.4
Maximum allowable traces of die parts on leadout coating	0.1x0.3 0.15x0.45	17.6 27.4	39.2 39.2	24.5 37.2	39.2 39.2
Impermissible damage of leadout coating in the form of dents	0.1 x 0.3 0.15x0.45	21.6 32.3	48.0 48.0	31.3 46.0	49.0 49.0

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The die design should profice rigid fastening of each IC leadout outside the glass or cermaics buildup. A leadout section of 1 mm from the body of the housing should not be subjected to bending or twisting deformations. Allowable bending radii should be maintained in forming. Forming IC leadouts of a rectangular cross section should be done with a bend radius of not less than two leadout thicknesses, while leadouts with a round cross section -- with a radius not less than two diameters.

Table 5.9

Maximum values of stretching forces

Leadout cross section, mm	Stretching force per one leadout, Newton
Up to 01	0.245
Above 0.1 to 0.2	0.49
Above 0.2 to 0.5	9.8
Above 05 to 2.0	19.6

The IC leadouts inside the housing or leadouts not used in the circuit of its application and not affecting the working capacity of the IC, may be trimmed 1.0 mm from the housing body; however, it should be taken into account that a considerable part of the heat is removed over IC leadouts (especially of small sizes).

In a typically improper design of a technological device, the formation of leadouts of type 4 housings (Fig. 5.6b), a gap (not less than 0.5 mm from the body of the housing), necessary to preserve the integrity of the ceramics was not left. A die of such design may damage the housing seal of the IC.

Fig. 5.7 shows another typical assembly error. We will assume that the forming of IC leadouts, intended for installation on a multilayer printed circuit board with open contact pads, was done at the depth of the second-third layer (Fig. 5.7a). Actually, however, it was necessary to solder them to other layers. In assembly, the leadouts were bent manually at the inlet of the seal (the bend angle in the vertical plane may reach $\pm$ 60%). Straightening the leadouts made without rigid fastening of the leadout zone on a section 1 mm from the body of the housing (i.e., without using the technological device) may lead to damage of the leadout at the housing. With such a method of assembly, the IC may lose its seal during the consequent mechanical forces when operating the apparatus because the deformed leadouts are in a stressed condition (Fig. 5.7b).

5.6 Tinning and Soldering

In the production of radio electronic apparatus, group methods are widely used to implement individual technological operations, for example, tinning IC leadouts by "dipping into melted solder" or soldering by means of a "wave of solder." These modes of operations (temperature of the melted solder, contact time between the solder and the housing leadouts, area of the contact zone of the leadout with the solder), selected without taking into account the heat transfer characteristics of concrete types of IC housings may lead to a destructive effect of heat shocks on IC.

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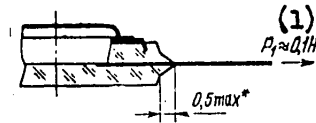
Fig. 5.4. Direction of stretching force in forming and trimming leadouts
1. $P_1 \approx$ 0.1 Newton
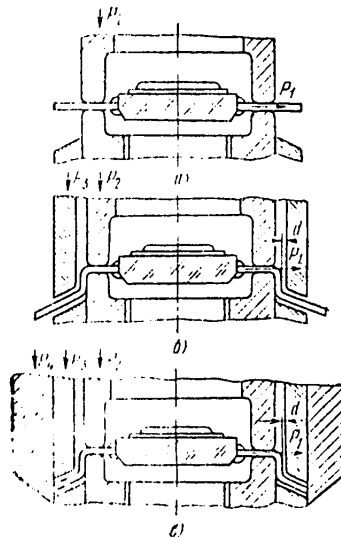

Fig. 5.5. Forming and trimming IC leadouts:
a -- clamping the leadouts; b -- forming the leadouts; c -- trimming
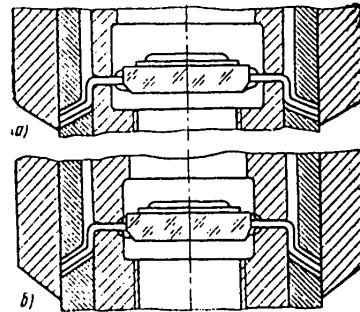the leadouts.

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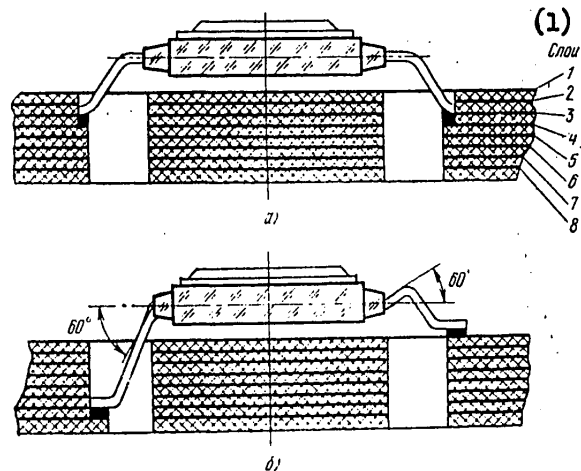Fig. 5.6. Correct (a) and incorrect (b) forming leadouts of a planar housing

Fig. 5.7. Correct (a) and incorrect (b) assembly of planar housings on a multi-layer printed circuit board with open contact pads.

1. Layers

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Fig. 5.8 shows schematically individual elements of IC design which are subjected to thermal effects and participate in heat transfer. A temperature gradient is produced along the IC leadout in contact with the melted solder causing the transfer of heat. The heat exchange is implemented from the soldering zone (zone A) through the leadout metal to the ceramic base of the housing body (2) and further to the IC chip (4). The heat flow is also transmitted to the chip from the inner part of the leadout (zone B) through the internal connecting conductor (3).

The speed of heat transmission depends on the temperature difference, on the heat conductivity of the material and the configuration of the IC structure elements. The heat conductivity coefficient is calculated by formula

$$\lambda \ [w/(m \cdot {}^\circ C)] = Q/\Delta t \cdot S \cdot \Delta T/\Delta l, \tag{5.1}$$

where Q is the amount of heat, joules; ΔT -- temperature gradient, $^\circ C$; l -- distance from heat source; $S = \Delta Q/T$ -- system entropy, joules/degree. Formula (5.1) contains the specific heat of the system $c = Q/\Delta t$ and the temperature gradient grad $T = \Delta T/\Delta l$. Values of heat conductance coefficients of several materials used in the IC structure are shown below.

Material	λ, watts/(meters. $^\circ C$
Silver	460
Copper	390
Beryllium oxide	208
Aluminum	203
Silicon	83.5
Aluminum	19.6
Kovar	19.7
Glass (borosilicate)	1.1
Laminated epoxy plastic	0.28

To evaluate the degree of the heat effect in tinning and soldering, it is necessary to know the material heat transfer coefficient of IC structure elements

$$a = \lambda/c\rho, \tag{5.2}$$

where λ -- coefficient of heat conductivity, c -- specific heat, joules (kg. $^\circ C$); ρ -- density, kg/m^3. This coefficient is determined experimentally for each type of IC housing and a given maximum temperature of elements in individual structures.

Fig. 5.9 shows diagrams of heat distribution for five housing designs. Isotherms are shown on these figures that characterize the degree of heating of IC elements when tinning leadouts. This data was obtained by thermal melting indicators whose action is based on the irreversible and sharp change in color when a certain
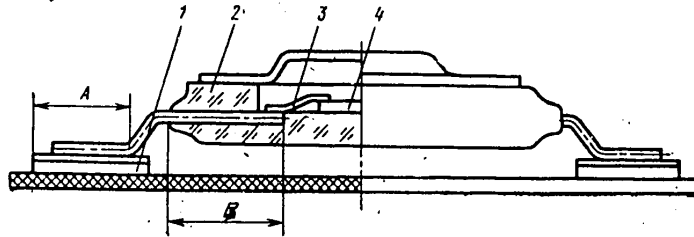
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Fig. 5.8. Heat exchange circuit in tinning and soldering external IC leadouts:

1. contact pad	3. internal connecting conductor
2. housing	4. IC chip

critical temperature is reached. In the experiment, thermal melting indicators with various critical temperatures were coated on the substrate or bottom of the IC. Then the IC was enclosed by covers, and fastened in a special holder made of textolite, and the tinning operation was done by dipping the leadouts in melted solder (temperature of the melted solder was $260° \pm 5°C$), distance from housing to solder surface was 1 mm, the contact time between the leadouts and solder was 3 seconds.

The devices used in the experiment provided a minimal removal of heat from the IC housing; in this case, the linear shifts perpendicular to the surface of the solder were held to an accuracy of $\pm$ 0.2 mm.

To determine the precise temperature values (the thermal melting indicators gave only limits of temperature changes), and to evaluate the changes of this temperature with time, temperature measurements were made on the most typical IC elements (leadouts, substrate, chip) by a thermal electric method for different modes of tinning and soldering. The temperature was measured by a low-inertia copper-constantan thermocouple with an 0.06 mm electrode diameter which made it possible to reduce the measurement error and the thermocouple effect on the true value of the temperature. In the experiment, the thermocouple was attached to the measurement point, then the housing cover was closed and sealed by "cyacrin" glue. The thermocouple indications were recorded by a high-speed self-recording device.

The relationships between the temperatures of the IC elements of various types in the process of tinning and the tinning time and the distance to the solder surface are shown in Fig. 5.10.

Fig. 5.9. Temperature distribution of IC housing heating when tinning leadouts:
a -- type "Tropa" housing; b --planar housing 401.14-1; c -- housing
151.15-1; d -- type "Po ol" housing; 3 -- round housing 301.12-1.

In this figure temperature zones obtained by thermal indicators of melting, are
shown for comparison. The test results show that temperature values obtained by
the thermoelectrical method are in the temperature zone determined by the thermal
indicators of melting. An analysis of the experimental data indicates that the
temperature difference of heating IC elements when tinning and soldering reaches
10...20°C and for all housing types 301.12-1, the tinning mode is more "rigid."
Tinning parameters are shown below.

Parameters of tinning mode	Norm
Max. soldering temperature, °C	250
Max. time the leadouts are in the melted solder, seconds	2.0
Min. distance from housing "body" to boundary of solder along the leadout length, mm	1.3
Max. allowable number of dippings of the same leadouts into the solder	2
Minimum interval of time between two dippings of the same leadouts into the solder, minutes	5.0

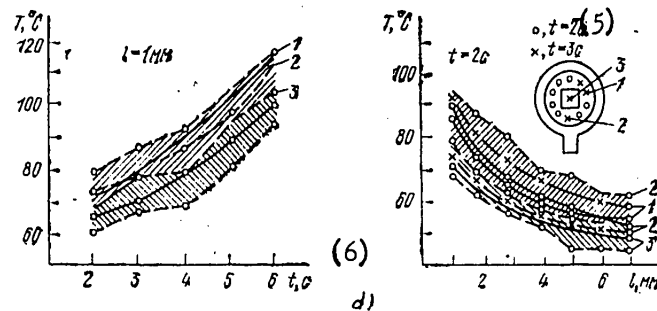Fig. 5.10. also continued on the next sheet

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Fig. 5.10. (continued from previous sheet) Relationship between temperature of
IC elements in the process of tinning and tinning time (t) and the
distance (1) between the level of solder for housings series 217 (a),
106 (b), 218 (c) and 122 (d). The numbers on the curves correspond
to the points of the IC elements at which the measurement is made;
solder temperature is 260 ± 5ºC.

5. t = 2 seconds   6. t, seconds

In tinning, the solder should not touch the seal inlets of the housing. The sol-
der should not fall on glass or ceramic parts of the IC housing. The boundary of
solder flowing on leadouts should be no closer than 1 mm to the body of the hous-
ing (Fig. 5.11a); however, some nonuniformity of tinning along the length of the
leadout is allowed. The minimum length of the tinning section along the leadout
length from its end must be no less than 0.6 mm (Fig. 5.11b), but "icicles" on
the ends of IC leadouts are permitted (Fig. 5.11c).

It is necessary to make sure that connections are not formed between the leadouts
and the soldering surface should be continuous without cracks, pores and untinned
sections (Fig. 5.11d).

Equipment used for tinning must insure the setting and measuring of the tempera-
ture with an error no greater than ± 5ºC.

The quality of soldered connections should be determined by the following criteria:
the soldered surface should have a light or mat finish without dark spots and
foreign inclusions. The shape of the soldered connections must have concave fil-
lets of solder along the seam (without an excess of solder). The contours of the
leadouts should come through the solder. In soldering IC housings with planar
leadouts the following is permitted: a flooding form of soldering in which con-
tours of individual IC leadouts are fully hidden under the solder on the soldered
side of a connection (Fig. 5.11e, f), partially covering the surface of the con-
tact pad with solder along the soldering perimeter, but in no more than two places,

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not exceeding 15% of the total area (Fig. 5.11g), solder bits of conical shape (Fig. 5.11h) and rounded shape (Fig. 5.11i) where the soldering tool is removed, a small shift of the leadout within the contact pad (Fig. 5.11j) and the spread of solder (only within the boundaries of the leadout length, suitable for wiring).
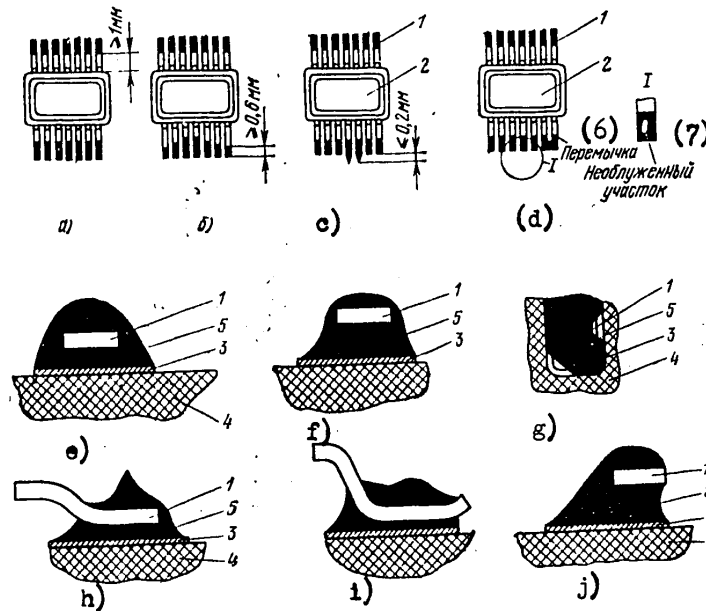
Fig. 5.11. Examples of tinning and soldering leadouts of a planar housing:
a -- zone of solder flow; b -- allowable nonuniformity of tinning;
c -- presence of "icicles"; d -- nonuniform tinning and false connec-
tions; e, f -- flooding form of soldering; g -- partial tinning of con-
tact pad; h, i -- conical shape solder beads; j -- small shift of
leadouts; 1 -- leadout; 2 -- housing; 3 -- contact pad; 4 --printed
circuit board; 5 -- solder; 6 -- connection; 7 -- untinned section

When soldering IC leadouts into metal-coated holes, the soldered connections must be according to the sketches shown in Fig. 5.12a-d. The solder on the side of the housings should not spread beyond the boundaries of the contact pads. The leadout end may be untinned. The metal-coated wiring holes must be filled with solder to a height of not less than 2/3 of the thickness of the board. The correction of defective connections from the side of the IC mounting on the board is not per-mitted.

Fig. 5.12. Examples of soldering housings with plug-coupler leadouts:
a, b, c, d -- soldering in metal-coated holes; e, f, g -- soldering
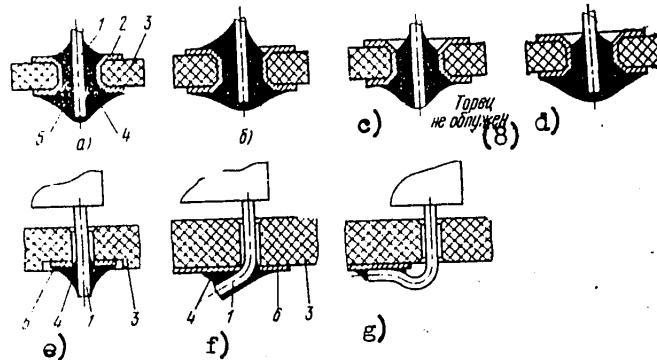in nonmetal-coated holes; 1 -- leadout; 2 -- metal-coated hole;
3 -- printed circuit board; 4 -- solder; 5 -- cavity in solder;
6 -- contact pad; 7 -- end not tinned.

When soldering IC leadouts to contact pads of printed circuit boards with holes
not coated with metal, the soldered connection must be made according to the sketch
(Fig. 5.12e-g). The spreading of the solder along the IC leadouts should not re-
duce the minimum distance from the housing to the soldering point, i.e., it should
be within the zone suitable for the wiring shown in the specification. There need
be no solder at the ends of the leadouts.

The equipment and fixtures used in soldering must provide the following; automatic
maintenance and control of the melted solder temperature with an accuracy of $\pm 5^{\circ}C$
when implementing the "soldering wave" operation; maintenance and periodic control
(every 1 to 2 hours) of the temperature of the soldering bit with an accuracy of
$\pm 5^{\circ}C$ in the individual method of soldering, control of the time the IC leadouts
are in contact with the soldering bit or with the molten solder in group soldering;
also control of the distance from the housing body to the boundary of the solder
along the length of the leadout. The soldering bit must be gounded (the ground re-
sistance should be no greater than 5 ohms). Table 5.10 shows the recommended modes
of IC soldering using single-bit and group methods.

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Table 5.10

Recommended IC soldering mode

Parameter	Soldering IC with planar leadouts		Soldering IC with plug-coupler leadouts	
	1-bit method	group method	1-bit method	group method
Max. temperature of soldering iron core, °C	265	-	280	-
Max. contact time of each leadout, seconds	3.0	-	3.0	-
Min. time interval between soldering of adjacent leadouts, seconds	3.0	-	3.0	-
Max. temperature of molten solder, °C	-	265	-	265
Max. contact time of each leadout with solder	-	2.0	-	3.0
Min. distance from housing to solder along leadout, mm	1.0	1.0	1.0	1.0
Min. time between two repeated solderings of same leadouts, min.	5.0	5.0	5.0	5.0

5.7. IC Assembly on Printed Circuit Boards

The following are the design features of IC housings: the presence of seal inlets and sealing seams, and a relatively "thin" housing base (0.1...0.2 thick), to which are fastened the substrates or the chip, determine a whole number of specific requirements which must be implemented in assembling IC on printed circuit boards. All precautionary measures, in this case, are reduced to protecting the IC housing from impermissible deformations.

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On one hand, the assembly method must provide mechanical strength that would guar-antee resistance to mechanical loads expected in operation but, on the other hand, "rigid" attachment of the housing is impermissible because the deformation of the printed circuit board (if its deflection is even several tenths of a millimeter) may result either in the cracking of the sealing joints of the housing, or in the deformation of the bottom and the rupture of the substrate or chip.

In most cases of IC application, mechanical stability is insured only by soldering all leadouts to contact pads. The necessity and methods for additional fastening of the IC to the board are determined by the rigidity of the operating conditions of the apparatus, as well as the weight and size of the IC housings.

The design of the apparatus must insure efficient removal of heat by air convection and heat-removing metal buses. The convection is provided by using housings with the maximum permissible gaps between the plane of the board and the bottom of the hous-ing. The housing arrangement on the printed circuit board must provide the possi-bility of coating it with moisture-protective varnish without having it fall into places that should not be coated, and have free access for dismantling any IC. Taking into account the necessity of preserving the integrity of the housing and to provide for heat removal, recommendations are given below for using various types of IC.
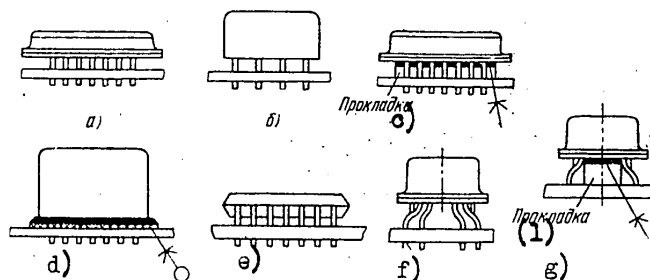

Fig. 5.13.   Variations of mounting various housings on the print circuit board with
metal-coated holes:
a,b -- housings with plug-coupler pins without additional fastening;
c,d -- housing with plug-coupler pins with additional gastening;
e -- plastic housing; f -- cylindrical housing without additional
fastening; g -- cylindrical housing with an electric insulation spacer

1. Spacer

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Fig. 5.13a,b shows variations of mounting housings with plug-coupler pin leadouts (housings 151.15-4 and 151.15-6). These housings are mounted in metal-coated holes. The IC do not have leadouts. The gap, equal to 1 - 0.5 mm, is chosen to insure IC stability in the entire range of mechanical loads and the preservation of the integrity of the housing (at smaller gaps, it is possible to damage the seal inlet of metal-glass housings due to the thermal effect of soldering).

IC in housings 151.15-2, 151.15-3 (Fig. 5.13c) and "Aktsiya" (Fig. 5.13d) require additional fastenings. IC in housings 151.15-2 and 151.15-3 are glued to insulation spacers, for example, made of DSV-2-R-2M (GOST 17478-72) or AG-4 (GOST 10087-62). The spacers must be fastened rigidly to the printed circuit board. In choosing the dimensions of the insulation spacers, it is necessary that they be as close as possible to the area of the IC housing base and that the integrity of the seal inlet be preserved. The IC in the "Aktsiya" housing (Fig. 5.13d) is mounted against an LN cement, placed along the perimeter. Cover should be provided with a two-sided arrangement of conductors in the board under the electric insulation of the IC housings.

IC in housings 201.14-1 are mounted on boards with a single-side or a two-sided arrangement of printed conductors into metal-coated holes with a gap insured by the design of the leadout (Fig. 5.13e). Fir. 5.13f,g shows variations of mounting IC with housings 301.8-1, 301.8-2 and 301.12-1 with formed leadouts. They are mounted with a gap of 3+0.5 mm (Fig. 5.13f). If the apparatus is subjected to higher mechanical forces in operation, rigid spacers of electrical insulation material must be used. The spacer should be glued to the board and the base (to the bottom) of the IC (Fig. 5.13g). The design of the spacer must also insure the integrity of the seal inlets of the microcircuit. IC with cylindrical housings without leadouts are mounted onto metal-coated holes with a 1+0.5 mm gap.

a)   b)   c)
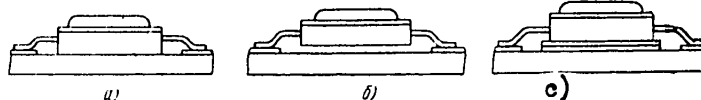
Fig. 5.14. Variations of mounting planar housings:
        a -- against the printed board; b -- with gap; c -- against a spacer

IC in housings 401.14-1 and 401.14-2 with shaped leadouts may be mounted on the boards with a single-side or a two-sided arrangement of printed conductors by the following methods: against the printed board or on a spacer (Fig. 15.14a,c) or with a gap of up to 0.3 mm (Fig.15.14b). In this case, the additional fastening is provided by coating with varnish. The gap may be increased to 0.7 mm, but then the IC housing must be fastened additionally to the board by glue.

Planar housings must be glued to the entire plane of the housing base. The thickness of the seam is determined by the chosen variation of forming the leadouts (the distance from the plane of the IC base to the board), but the gaps between the IC and the board must all be filled with glue. When IC are mounted on planar

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Fig. 5.15. Example of proper (a) and improper (b) mounting of a planar housing on a printed circuit

1. LN   2. UR-231

housings a shift of the free ends of the leadouts in the horizontal plane is permitted within ± 0.2 mm for matching with the contact pads. Free ends of leadouts may be shifted within ± 0.4 mm in the vertical plane from the leadout position after forming.

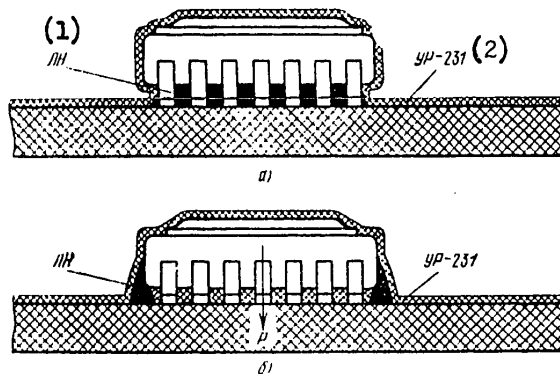The use of glues VK-9(ShchI0.026.400TU) or AK-20 (TU 6-10-1293-72), as well as cement LN (TU MKP. 3052-55) to glue IC to printed boards is recommended. The drying temperature of materials used for fastening IC to the board should not exceed the permissible temperature for operating IC. The recommended drying temperature is 65 ± 5°C. In gluing IC to the printed board, the squeezing force should not exceed 0.08 microPa. It is not permissible to glue IC with glue or cement applied at individual points on bases or at the ends of the housings.

Fig. 15b shows an impermissible variation of IC mounting which is glued to the end of the housing (this may be done for simplifying the dismantling of IC). In this method, the gap between the bottom of the IC and the board is partially filled with cement. In implementing the moisture protection operation, UR-231 varnish may get into the gap which, by polymerization, may be able to cause the deformation of the bottom of the housing (0.1...0.15 mm thick), the ungluing of the chip or breakage of the internal connections of the IC. In all cases of installation of IC on printed circuit boards, no force should be applied that leads to the deformation of the housing of the IC.

5.8. IC protection Against Electrical Effects

The degree of integration of the IC (i.e., the density of the grouping of elements on one wafer) is increasing with time because of the development of a technology that makes it possible to reduce the dimensions of the elements, as well as those areas by means of which the elements are electrically insulated from each other on the IC wafer. Such an increase in the density of the elements on the surface of the wafer makes it possible to improve the electrical and functional parameters of the IC, but is accompanied by a reduction in allowable electrical loads, and increases the sensitivity of the microcircuits to static electricity discharges. Table 5.11 shows comparative typical characteristics of transistors manufactured by different technological processes.

Table 5.11

Some parameters of various designs of transistors

Technical characteristics	Planar epitaxial technology	"Izoplanar-1" technology	"Izoplanar-II" technology
Dimensions of emitter area, micrometer	25x38	5x25	2.5x12.5
Breakdown voltage emitter-collector, volts	23	7	5
Breakdown voltage collector-base, volts	55	22	14

Actually, an analysis of IC that failed in the process of production indicates that the cause of failures of up to 40 to 50% of such IC is electrical overload.

In damaged IC there is detected a deterioration of the steepness of the volt-ampere slope or a complete breakdown of the p-n junction although there are no changes in the metal coating visible under a microscope. Emitter junctions are damaged more frequently than others. Externally the defect is manifested in that the value of the reverse current increases by several orders of magnitude, while the current amplification coefficient decreases essentially (by 70%). In this case, the electrical overloads cause irreversible changes in the p-n junction structures leading to the deterioration of the efficiency of the emitter. A typical volt-ampere characteristic of the junction for a reverse bias is shown in Fig. 5.16. The emitter current (curve 2) is almost linear which may be due ɪ the appearance of an ohmic shunt on the surface, or in the volume of the p-n junction.

A partial or complete burn-out of the metal coating and the formation of jumpers between adjacent tracks may occur, along with highly visible traces of p-n junctions breakdowns on the surface or under the passivating layer.

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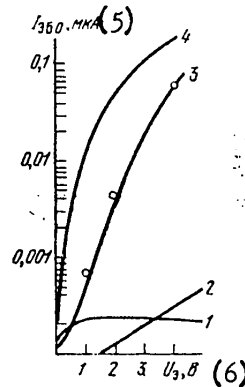
Fig. 5.16. Volt-ampere characteristics of emitter junctions of two transistors
without housings:
1,2 -- transistors in working order; 3,4 -- transistors after a 600-volt
discharge through the emitter junction in the reverse direction;
5 -- microamperes; 6 -- volts

IC that failed due to electrical overloads are characterized by the melting and
spattering of aluminum (when boiling) and the formation of short-circuited adjacent
sections of the metal coating. The burn-outs occur most frequently at the "weak-
est" points of the current-carrying tracks that have local thinning (at the "steps"
of the oxide).

One cause of IC failures of the above-indicated types may be the effect of dis-
charges of static electricity originating during various technological operations
due to the wide use, under production conditions, of strongly electrifiable syn-
thetic and other insulation materials. Moreover, due to poor grounding of device
housings and technological tools, considerable network noise inductions may occur.

The origination of static charges is due to several generating mechanisms and the
value of these charges depends on many factors. The values of static voltages
(U_{CT}) on the surface of the dielectric, independently of the mechanism of their
generation are always proportional to the specific surface resistance of the (ρ_s).
This can easily be seen by analyzing the experimental data on the value of static
voltages originating on the surface of several materials at a relative humidity of
50% (Table 5.12).

Fig. 5.17 shows the relationship between the static voltages and the relative air humidity of two types of material used widely for the special working clothes of production personnel -- Lavsan and cotton cloth. The relative humidity of the air is used as the parameter when measuring the voltages. In analyzing these relationships, it should be noted that static potentials at low relative humidity of the air (40 to 50%) reach 3 to 10 kilovolts. The static voltage on Lavsan is higher than on cotton cloth and depends strongly on the relative himidity of the air (at 65% humidity the voltage on cotton is zero, while on Lavsan, it exceeds 3 kilvolts).

In developing measures to protect IC from the effect of static electricity discharges, it is necessary to take into account also the ability of insulating materials to retain charges accumulated on their surfaces for a certain time. As the charge retention time is assumed the time (τ_y) during which the accumulated static voltage reduces to a half or a third.

τ_y may be measured as follows: the surface of the tested material is charged (for example, by rubbing) to a certain voltage and a flat metallic contact electrode is applied to the surface of the material. The electrode is connected to a type S-95 static voltmeter and then the time it takes for the voltage to drop to half or a third is recorded. The charge retention time is proportional to the specific surface resistance of the materials exactly the same as the values of the static voltages.

Table 5.12.

Static voltages and surface resistance of various materials

Material	U_{CT} Kvolts	ρ_s, ohms
Polyvinyl chloride	1.3 - 2.8	1×10^{14}
Wood	0.7	1.4×10^{13}
Glass	0.6 - 0.8	9.6×10^{12}
Getinaks	0.45	4.3×10^{12}

Table 5.13

Charge retention time on various surfaces

Material	τ_y, seconds	ρ_s, ohms
Paper	25	$(3.3 - 9.8) 10^{11}$
Varnished wood	1200	1.4×10^{13}
Polyvinyl chloride	7800	1.0×10^{14}
Glass	9000	2.2×10^{15}
Synthetic linoleum	12000	4.0×10^{14}

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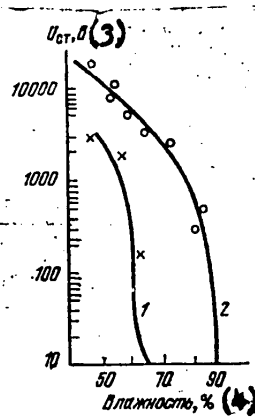
5.17. Relationship between the value of static
and relative humidity of air for cotton
cloth (1) and Lavsan cloth (2)
3. Volts   4. Humidity
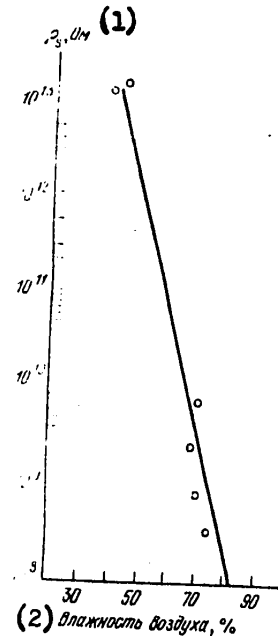
Fig. 5.18. Relationship between
specific surface re-
sistance (ρ_s) of poly-
vinyl chloride and the
level of the relative
humidity of the air,
1. Ohms   2. Air Hu-
                midity,
                %

Table 5.13 shows experimental data on charge retention time at the relative humidi-
ty of the air of 65%. The time retention time on the surface of synthetic linoleum
was measured at a lower humidity (60%).

It may be concluded from Fig. 5.18 that an increase in humidity from 40 to 83% re-
duces the specific surface resistance of polyvinyl chloride by five orders of mag-
nitude.

In organizing apparatus production using IC, it must be remembered that considerable
static voltages, from hundreds to several thousands of volts, are produced on the
hands of the workers when doing various technological operations. The value and
polarity of these voltages depend on many various factors, including the humidity

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of the air in the room, the material of the clothing worn, the materials used to cover the table and chairs, the technological and test equipment and the degree of insulation of the worker from the "ground" (materials of shoes and floor) Fig. 5.19).

An analysis of the data in Fig. 5.19 shows that with working shoes with rubber soles (curves 2), the static voltage on the hands of the workers is 2 to 2.5 times higher than when working in leather shoes (curves 1). This is due to the fact that the leakage resistance of shoes with rubber and leather soles differs by almost two orders of magnitude (leakage resistance of shoes with rubber soles is $1.8 \times 10^8 - 2.8 \times 10^9$ ohms, while on leather soles -- it is 5.6×10^6 to 1.9×10^7). It should also be noted that high values of static voltages on the workers' hands correspond to the case where dielectrics with high specific surface resistance are used at the working position.
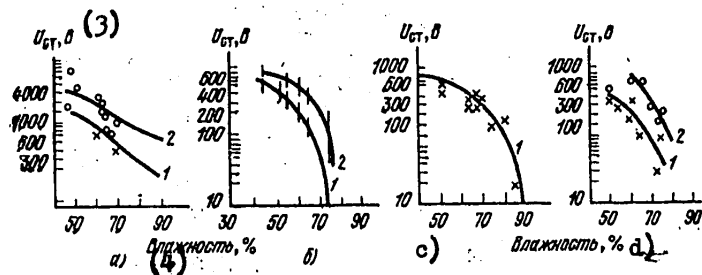
Fig. 5.19. Relationship between the static voltage originating on the workers' hands when rubbing different materials and the relative level of the humidity of the air for the table surface being of polyvinyl chloride (a); varnished wood (b), textolite (c), covered with glass (d). Workers' shoes with leather (1) and rubber soles (2).

3. Volts   4. Humidity, %

When the workers walk on a floor covered with synthetic linoleum, charges are also accumulated on them (Fig. 5.20). The prevention of static electricity charges in the production process should proceed in two directions: first reduction of the possibility of static electricity charge generation and, secondly, insurance of the removal of accumulated charges from the production and technological equipment and workers.

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In organizing apparatus production sections where IC are used the use of finishing materials with high specific surface resistance is not recommended. The use of finishing materials for production furniture, floors, testing and technological equipment materials with low -- not over (1 to 5)10^9 ohms, insures the necessary conditions for the rapid draining of the static electricity charges.
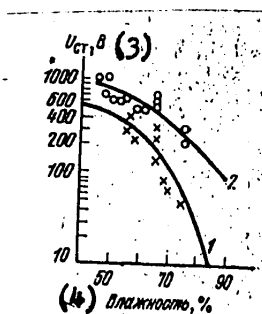
Fig. 5.20. Relationship between static voltage on the worker at various values
of the relative humidity and degree of insulation from the floor, if
the workers' shoes have leather (1) or rubber (2) soles.

3. Volts

4. Humidity, %

Table 5.14

Relative characteristics of two types of linoleum

Type of synthetic linoleum	ρ_s , ohms	ρ_v , ohm.cm	τ_y , seconds
Common	4×10^{14}	5.9×10^{17}	12000
Antistatic	5×10^9	2.4×10^9	0.5

A special antistatic linoleum is recommended to cover surfaces. The comparative electrical parameters -- specific surface (ρ_s) and volumetric (ρ_v) resistances and the time of charge retention (τ_y) of common and antistatic linoleums are shown in Table 5.14.

The use of antistatic linoleum eliminates the possibility of charge accumulation on the worker: a contact by the worker's hand with a surface covered by the anti-static linoleum before doing the next technological operation insures draining of the charge in 1 second. Synthetic cover P-2-E-S-5 has the best antistatic proper-ties: specific surface resistance of the material is 10^6 ohms. The use of such material insures the complete destruction of the static charges because the drain-ing time of a charge from a person is only 2x10^{-4} seconds.

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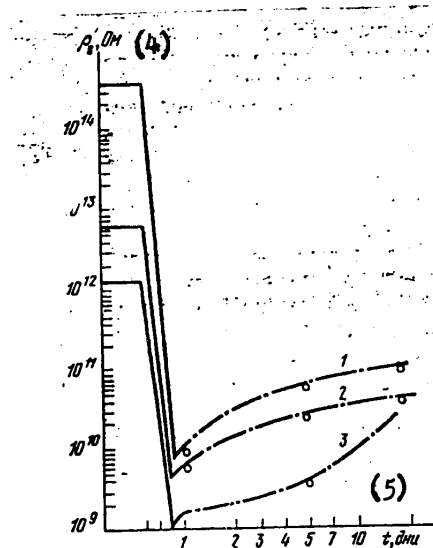
Fig. 5.21. Relationship between specif.c surface resistance (ρ_s) of various
materials and time before (————) and after (——— · ———) their
treatment by "Charodeyka" paste:

1. synthetic linoleum   3. cardboard
2. textolite   4. ohms
                                5. days

One of the methods recommended to reduce the specific surface resistance of covers
is to use surface-active substances (PAV), for example, "Charodeyka" paste
(TU-6-15-604-71), which is applied in a thin layer on the working dielectric sur-
faces of tables, test and technological equipment, packing for storing IC and
assembly units, and is used to mop floors and wash paper covers for production
furniture. The antistatic properties of the paste with respect to time are char-
acterized by experimental data (Fig. 5.21).

The increase in surface resistance with time of the processed surface is due to the
natural drying and aging of the paste and also to its being rubbed off in opera-
tion. The resistance increases by an order of magnitude in 10 to 15 days; there-
fore, the interval between applying the paste should be determined on the basis
of concrete productions. In the case of using antistatic linoleum, as well as

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in using PAV to drain charges, it is necessary to insure good electrical contact of one-two points of the processed surface (contact area not less than 1 cm^2) with the "ground."

To reduce the surface resistance of covers at working positions, it is recommended to insure the maximum relative humidity in the production areas (a satisfactory result may be achieved at 65 to 70% humidity).

Materials with surface resistances of 10^6 and 10^8 ohms are recommended for interoperation packing. The packing material may be coated with aluminum current-conducting paint. The paint layer does not prevent charge draining because it has a low ρ_s.

The continuous contact between the worker and the "ground" should be provided by a special antistatic bracelet, connected through a high-voltage resistor (for example, the KLV type 10 kilovolt resistor). However, it should be taken into account that the use of an antistatic bracelet is effective only when the working position, packing and fixtures are made of materials with low surface resistances that prevent the accumulation of static electricity charges. Otherwise the possibility of IC damage is high. Actually, charges of static electricity on a high resistance surface, for example, on interoperation packing, may produce a voltage of up to several thousand volts on the packing itself, as well as on the IC in it. At the moment of contact between the worker and the IC when there is a current circuit "IC-worker-ground" the pulse of the discharge current may cause the failure of the IC [2].

The workers' clothes should be made of cotton cloth, be laundered with antistatic "Charodeyka" paste or other surface-active substance. The workers should wear leather or semiconducting rubber soles.

5.9. Dismantling

In manufacturing apparatus, it frequently becomes necessary to dismantle IC. The following are recommended for this operation. If IC with planar leadouts are to be disassembled, it is necessary to, remove the varnish at points of leadout soldering (if needed); unsolder the IC leadouts using a mode that does not exceed the soldering mode specified in the IC certificate; lift the ends of the leadouts from where they were fixed in the seal inlet; remove the IC from the boards thermomechanically by means of a special device. (This device is heated to a temperature that prevents the IC housing from overheating above the temperature indicated in the certificate. The heating time should be sufficient to remove the IC and not permit cracks, chipping and damage to the housing).

When removing an IC with pin leadouts, it is necessary to, remove varnish at the points of soldering of the leadouts; unsolder the leadouts with a special soldering tool (the solder should be drawn off according to a mode not exceeding the soldering mode, specified in the IC certificate, until all IC leadouts are freed from connection with the metal-coated printed circuit board); remove IC from the board (not permitting cracks, chipping of glass or deforming of the housing and the leadouts). In this case also,if necessary, it is permitted (if the housing is fastened

to the board with varnish or glue) to use a thermomechanical method to remove the IC that prevents overheating of the housing, or chemical solvents that have no effect on the coating, labeling and material of the housing.

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SM-3 AND SM-4

SMALL COMPUTER HARDWARE FOR CREATION OF DEVELOPED COMPLEXES

[Text] The main purpose of the first step in realizing the program for development
of small computer hardware (and software) included development, testing and indus-
trial adoption of single-machine single-processor complexes of different designa-
tion. Further development of small computers along with improvement of single-
machine complexes envisions the development of hardware and software oriented
toward design of multiprocessor and multimachine complexes.

Development of the functional capabilities of single-processor small computer com-
plexes is primarily related to the need to remove the restrictions on the number of
devices connected to the complexes and on their configuration and to creation of
conditions that permit more complete utilization of available resources of central
processors and achieving the maximum functional return from the complexes. This
problem is partially solved by means of the interface expander (RIF SM).

No less important is the problem of maintaining a sufficiently high level of com-
plex productivity when using a large number of high-speed direct-access devices in
it. It can be solved by using an interface segmenter (SGI SM) in the complex whose
main function is relieving the "Common bus" (OSh) mainline of the most frequently
repeated direct-access exchange operations.

The possibility of parallel connection of interface expanders and interface seg-
menters to the common busses of SM-3 and SM-4 complexes permits development of
multiple, but highly productive small computer complexes and systems of different
designation.

A programming timer (TMRP SM) has been designed to relieve the central processor
of constant routine operations in real-time formation by programs. Its use is es-
pecially effective in SM-3 (SM-4) complexes that control complex facilities and
processes in real time.

- The productivity, reliability and other characteristics of single-machine single-processor UVK [Control computer complexes] or of computer systems do not always meet the requirements of ASU [Automated control systems]. In these cases an alternative solution of the problem may be the use of multimachine or multiprocessor complexes and systems. The small computer hardware that permits development of both concentrated and decentralized multiprocessor and multimachine complexes and systems of different designation is related to AMS SM [Intercomputer communications apparatus], PSh SM [expansion unknown], USVM [expansion unknown] devices and so on.

3.1. The Interface Expander

The desire to utilize more fully the configuration capabilities and productivity of central processors in developing efficient control computer complexes or systems leads to an increase of the number of devices connected to the communications mainline (MS) of the systems input-output interface (IVV). However, the number of devices in the system cannot be increased infinitely due to the limitation on the load capacity of the mainline amplifiers (components of signal sources).

Moreover, the problem of designing the complexes with at least a small number of devices but whose disposition requires an increase of the physical length of the interface communications mainline frequently arises to meet the requirement of optimum configuration. Rigid restrictions are placed on the length of the communications mainlines in any computer systems.

The restrictions of physical length and load capacity of interface mainlines actually existing in many complexes and computers can be eliminated by using additional devices. One of these devices is the interface expander (RIF).

All the peripheral devices in traditional computer systems with three-bus communications structure are distributed by their own buses and therefore requirements on load capacity are placed only on the communications program channel in which the number of devices (in complex systems) may exceed the capabilities of the mainline amplifiers. All the devices in complexes with single-bus structure (SM-3 and SM-4) are connected to a single interface communications mainline and therefore its capabilities are considerably limited in length and load.

The load capacity and physical length of communications mainlines are important systems parameters that largely determine the functional and technical capabilities of designing complex systems based on small computer complexes. Since the productivity of the central processors (TsP) of SM-3 and SM-4 complexes and the carrying capacity of communications mainlines are adequate to service a large number of peripheral devices, these characteristics of the complexes become important and largely determine the capability of developing complex, but effective systems based on small computer hardware.

The communications mainline in SM-3 and SM-4 complexes permits connection of up to 20 devices to it provided that each device loads it only with a single load unit with a total length of the mainline up to 15.0 meters (with regard to all possible branches). If each connected device loads the communications mainline with more than one load unit, the maximum possible number of devices in the complex is reduced sharply.

Uneconomical consumption of load capacity (some devices from the small computer hardware nomenclature load the communications mainline with more than one load unit) and the length of the mainline (nonoptimum laying of communications mainline wires in BKI [expansion unknown] type units and the need to leave more than one meter allowances of common bus cable to move complete units or BRS [expansion unknown] units from the bay) lead to the fact that these indicators are considerably limited in standard configurations of SM-3 and SM-4 complexes and the capabilities of the communications mainline may be insufficient for users developing ASU based on standard small computer complexes (TK) having a reserve length and reserve load capacity of the communications mainline. The geometric length of the communications mainline must be taken into account when selecting the configuration of any complex. It is obvious that a reserve length facilitates configuration of the devices in bays and in the area of the computer center or ASU and brings it close to the optimum. The resources of the complex usually remain unutilized in the use of load capacity or length.

The SM-4101 interface expander (RIF SM) permits elimination of all the noted restrictions.

The SM-4101 interface expander is designed for complexes and systems that utilize the "Common bus" interface as the systems interface.

The device is required to design multiple complexes with number of peripheral devices that exceeds the capability of the main segment of the interface mainline.

The interface expander has the following specifications and designation factors:

The interface for connection of the device at the input (central segment of the communications mainline) and at the output (the peripheral segment of the communications mainline) is the common bus of the small computer. The method of connection is series, parallel and combination (parallel-series and so on).

The load capacity through the output is 19 load units. The natural load on the input-output interface is 1/1 load units.

The geometric length of the interface mainlines after the expander is not more than 15.0 meters.

The additional delay of the exchange cycle upon access to the device, established after the expander, is not more than 0.35 microsecond when executing the READ operation and not more than 0.25 microsecond when executing the WRITE operation.

The component base is TTL-IS and SIS. The electronics capacity (in arbitrary housings of integrated circuits) is 80. The design version is the small computer plug-in unit and the number of printed-circuit cards (two-digit electronics unit) is 2 and the number of types of cards is 1. The mass of the device is no more than 3.0 kg.

The power supply voltage is +5 ± 0.25 V. The consumed power is no more than 9.0 W.

The operating conditions are group 3b according to GOST [State Standard] 20397-74. The version is ordinary according to GOST 21552-76.*

The efficiency checking devices are the ir..erface expander tester and the test programs for it and tests of the devices connected after the interface expander.

Identifiers of the device on the common bus are not required.

The interface expander increases the functional capabilities of small computer complexes by expanding the systems characteristics of the input-output interface with a slight reduction of productivity. It permits the mainline of the complex to be extended to 15 meters and permits control of an additional 19 load units. A further increase of the interface capabilities is provided by series or parallel connection of the expanders.

No software is required in the complexes to control the operation of the interface expander.
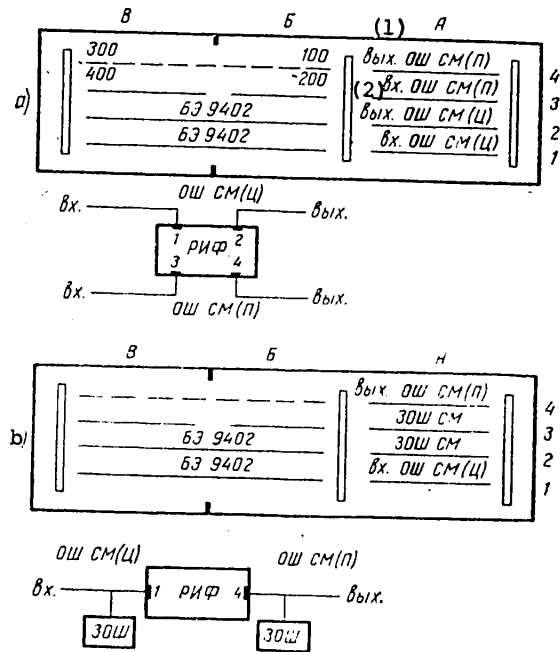
Figure 3.1. Configuration and Possible Layouts of Connecting the Interface Expander to the Common Bus

Key:
    1. Output   2. Input

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*The operating conditions and the version correspond to the indicated normative documents for a small computer hardware.

The interface expander is a structurally independent unit (plug-in package unit--BK) designed for installation in units of type AKB, BAM or BRS* of SM-3 and SM-4 complexes. The following devices: the interface expander tester TRIF SM (BE9401), the status designator of the small computer common bus ISOSh SM (BE284 is i· illed in place of the TRIF SM if necessary), common bus plugs (ZOSh SM) and common bus cables or jumpers (POSh).

Possible diagrams of the body configurations of interface expanders are shown in Figure 3.1.

The parallel method of using interface expanders also increases the number of directions of increase of the common bus mainline, which significantly simplifies the configuration of the complexes (Figure 3.2).

The interface expander tester and common bus status designator (included in the nomenclature of small computer devices used in complexes of automated designer job sites ARM (SM-3-M-400 ARM)) can be connected by the expander body both on the central and on the peripheral segments of the communications mainline.

Parallel, series and combination principles of increasing the peripheral devices (PU) in the complexes are possible when using interface expanders (see Figure 3.2).

The function not only of signal translation from one (central--Ts) segment of the common bus to another (peripheral--P), but also the function of restoring the time relationships between common bus signals is entrusted to the expander during operation in the complex, as a result of which series connection of an unlimited number of interface expanders and achievement of a mainline of infinite length is possible.

The function of restoration includes an additional delay in the exchange cycle between devices located on different common bus segments.

The delay introduced by the expanders is added with series use of them, which reduces the total rate of exchange with the devices located behind the expanders. The length of the exchange cycle between devices is calculated according to the formula

$$T_{tso} = T_0(1 + T_r \cdot n),$$

where T_{tso} is the time of the exchange cycle, nanoseconds, T_0 is the time of the exchange cycle between devices of the same bus segment, nanoseconds, T_r is the average delay introduced by the expander, nanoseconds, and n is the number of expanders used in the complex.

Thus, the parallel principle of connecting the expanders may be used in which there is no increase of the delay introduced by the expanders with an increase of their number in the complex. In this case the maximum delay introduced by the expanders is achieved upon participation of two different peripheral segments of the common

_____
*AKB--self-contained complete unit, BAM--self-contained installation unit and BRS--systems expansion unit.

bus in the exchange of the devices and comprises $2T_r + T_o$. If the devices are located on the central and peripheral segments, the exchange cycle T_{tso} will always be equal to $T_r + T_o$.

If the number of peripheral devices used in the system exceeds the capabilities of the expanders connected in parallel to the central segment or if devices separated by 30-50 meters from the bay must be connected by using the common bus mainline, the parallel-series principle of connecting the expanders may be used.
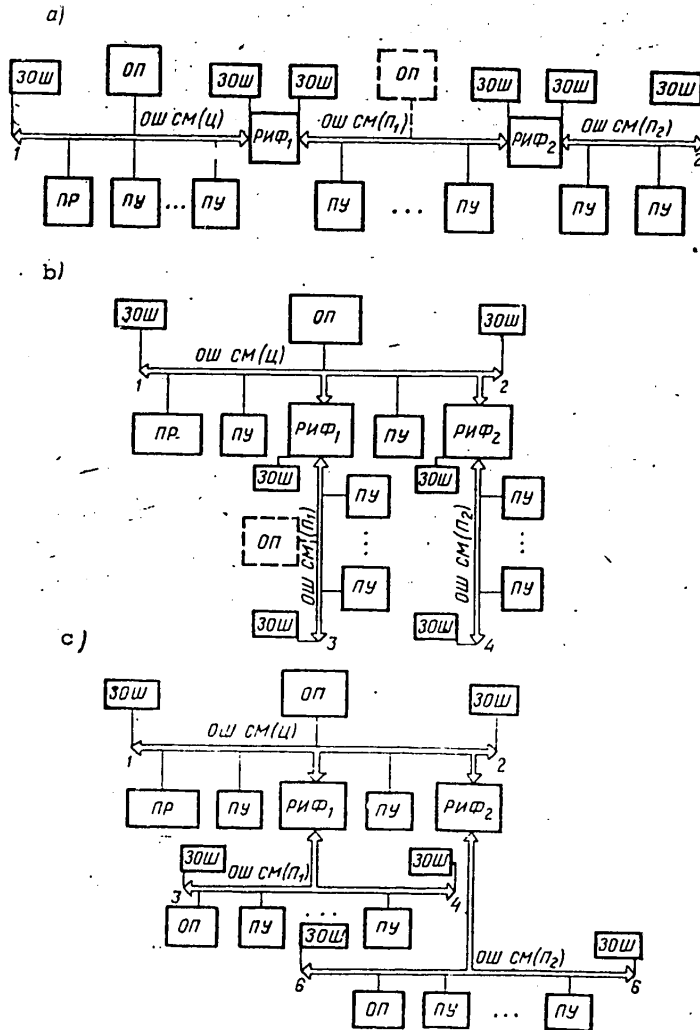

Figure 3.2. Principles of Build-Up of Common Bus Mainline Using an Interface Expander

An additional delay of the exchange cycle through the common bus, which occurs due to the use of the expander (for devices connected after the interface expander), plays no significant role since it is short ($\leq$ 350 nanoseconds). On the other hand, program-control devices which are very slow with respect to the processor and memory speeds, may be connected behind the expanders and the overall reduction of the productivity of the complex will be insignificant. High-speed devices having short (critical) service waiting time, such as NMD [Magnetic disk carrier], computer communications devices (USVM) and so on, should be connected before the expanders on the main common bus segment.

Inclusion of interface expanders in small computer complexes permits more complete utilization of the capabilities of the SM-3P and SM-4P central processors in servicing a large number of peripheral devices and makes it possible to develop complex, but economical control systems for different facilities and processes.

The Interface Expander Tester (TRIF SM)

The interface expander tester is used as the service equipment of SM-3 and SM-4 complexes and is designated for a complete check of the efficiency of the interface expander without using peripheral devices. A minimum of one device would have to be connected to each of the interrupt levels (ZPD, ZP7-ZP4) to check the interface expander by means of peripheral devices. The tester also permits one to check the common bus exchange with the central processor and the internal memory devices and to organize interrupt modes at all four program levels and the direct-access level and makes it possible to check the interaction of all common bus signals.

The specifications of the interface expander tester are as follows.

The interface connecting device is the small computer common bus. The natural load on the interface is one load unit.

The main modes of exchange of the devices with the tester are the executor, interrupt servicing and direct access.

The tester forms the following types of interruptions: program generation of requests at any of the ZP7-ZP4 levels and apparatus generation of requests at the direct-access level with period of approximately 1 microsecond.

The component base of the device is TTL-IS and SIS. The device is structurally made in the form of a two-plug unit of BE9401 components. The power supply voltage is +5+0.25 V. The consumed power is no more than 7.5 W.

The device is installed in the interface expander body or by means of an attenuator in the cable compartment of the common bus in the plug-in package unit of other devices. The mass of the device is no more than 0.6 kg.

The tester has a 16-digit storage consisting of 16 registers with access time of no more than 250 nanoseconds. The addresses of the registers are 767700-767736. With program use of the file of these registers, the tester can be serviced by the executor in communications sessions through the common bus controlled by any device of the system.

The level of interruption should be given to organize the interrupt mode. The four lowest orders of the interrupt request register (RZP), having address 767740, are used to store the number of the level of interruption. A "1" is entered by program or from the console in one of these RZP digits, corresponding to the selected level. The outputs of digits 3-0 form the ZP7-ZP4 signals on the common bus.

After the interrupt authorization signal (according to RP7-RP4) has been received from the central processor, the tester generates a sequence of signals through the common bus according to the algorithm for processing the interrupt procedure (see 2.6). The address of the interrupt vector issued by the tester on the common bus is first entered in the zero register of the tester storage device.

The type of operation (read or write) and the type of access from the tester (only to the memory cell or to the keyboard register), besides the direct-access request itself, are given (by program or from the console) to organize the direct-access mode. These data are stored in the three digits of the RZP: a "1" in digit 4 denotes "write" and a "0" denotes "read": a "1" in digit 5 denotes a series of ZPD signals; a "1" in digit 6 denotes access to the internal storage cell and a "0" denotes access to the internal storage cell and to the keyboard register (the address of the internal storage cell is 000214 and the address of the keyboard register is 777562).

A one recorded in digit 5 of the interrupt request register induces the tester to emit a series of ZPD signals. Having received authorization from the processor (RPD), the tester generates a series of exchange signals according to the direct-access algorithm (see 2.6).

When writing in the direct-access mode, the data are selected from register 6 (when writing in the internal storage cell) or from register 9 (when writing in the keyboard register) of the test register block.

The tester generates a sequence of executor signals (the executor mode) during the communications cycle through the common bus by the corresponding algorithm (see 2.6) with access to it through the address of any of the 16 registers of the tester (767700-767736) or the interrupt request register (767740). Thus, the necessary information can be entered in any register of the tester or the contents of the register can be read (only writing is possible during access to the interrupt request register).

Test programs are used to check the exchange through the common bus by means of the interface expander tester. Diagnosis of malfunctions when the tests are stopped is given in commentaries to the halt instructions.

3.2. The Interface Segmenter

The devices in complex with single-bus structure of the systems interface cannot carry out parallel exchange of information due to the need for time sharing of the single data transmission mainline.

Since all information flows travel over only one path, the time delays in this system may be longer than in other systems containing a larger number of information transmission mainlines. In a system with a common mainline when one source transmits data to a receiver, the third source (and the others) waits for clearing of the mainline. Although conflicts between devices for the right to utilize the common bus are automatically resolved and present no serious problem, they still occur and delay the overall operation of the complex. The productivity of the system is thus dependent on the speed of the communications mainline (on its exchange cycle). The use of a large number of devices in a complex with single-bus communications structure may lead to an impermissibly long waiting time for servicing of "remote" devices (from the central processor arbitrator) as the composition is expanded, especially with frequent exchange of data files (at the level of direct-access requests).

The interface segmenter permits a reduction of the effect of the single-bus structure on the overall productivity of SM-3 and SM-4 complexes.

Only two devices, one of which is a controller and the other of which is an executor, participate in each data exchange cycle through the common bus mainline in the SM-3 and SM-4 control computer complexes. Other devices which the mainline also requires for exchange wait for completion of the current exchange cycle. During exchange of information between the controller and executor, only that part of the mainline is required which connects these two devices (although the mainline connects all the devices of the complex in series). During this time the remaining parts of the mainline, except relay of electrical signals, carry no functional load of any kind.

The use of an interface segmenter device in SM-3 and SM-4 complexes permits one to increase their productivity by relieving the common bus mainline of the most frequently repeated direct-access exchange operations. Relief is accomplished by dividing the interface mainline by means of the segmenter into individual address sections (peripheral segments of the common bus) to which devices that perform a more intensive exchange with each other are connected. Independent operation of the devices within sections and parallel operation of sections with each other and with respect to the central segment of the common bus are possible.

The integrity of the system (and of the interface) is retained in this case, i.e., the interface segmenter device maintains the capability of information exchange between devices of different segments if the need for this volume occurs. Control of isolated devices by means of a processor and self-contained operation of devices on the peripheral segments of the common bus are provided by the corresponding adjustment of the segmenter address selectors to the address zones (segments). These address zones may be the register addresses of the devices or the address zones of the internal storage devices.

When the interface segmenter is used in the complex, besides its main function, it performs the functions of an interface expander that permits lengthening of the interface mainline by the same length and control of the same additional number of loads as in the main common bus mainline.

The interface segmenter is structurally completely identical to the interface expander device. The body configuration corresponds to Figure 3.1, except BE9403 instead of BE9402 components are used in place of the blocks. Therefore, the main installation on the body is different than in the interface expander. The capabilities of installing other devices in the interface segmenter body completely correspond to the list presented in the interface expander (these are the interface expander tester, the common bus status designator, the common bus plugs and so on).

The diagrams for connecting the segmenters to the common bus of small computer complexes are similar to those for connecting the expanders (see Figure 3.1). The length of the exchange cycle between devices on both sides of the interface segmenter is calculated by the same formula as for the interface expander.

The use of the interface segmenter in SM-3 or SM-4 control computer complexes may yield a significant effect. For example, there is one each graphical display of the EPG type in SM-3 or SM-4 automated job sites which interact intensively with the internal storage, regenerating information files (which may have capacity of 4-8K words) at frequency of 50 Hz, as a result of which they take "for themselves" almost 50 percent of the carrying capacity of the common bus interface of each complex. Taking into account that there are also other devices (processor, NMD [Magnetic disk carrier], NML [Magnetic tape carrier] and others) interacting intensively with the memory, it is practically impossible to realize an economic complex of an automated job site with a large number of EPG.

When using segmenters, the number of EPG SM displays connected to the complex through them may be rather large and will be determined by the internal storage capacity rather than by the carrying capacity of the common bus. The structure of the computer complex based on the SM-4 control computer complex with three EPG SM connected through segmenters and with self-contained internal storage units is shown in Figure 3.3.

The use of interface segmenters in combination with other devices permits one to develop original small computer complexes of increased productivity and provides expansion of the input-output interface functions by increasing the load capacity and physical length of the common bus mainline.

3.3. A Programmable Timer

A circuit that generates interrupt signals at network frequency (50 ± 1 Hz) is provided in the central processors to organize real-time service in SM-3 and SM-4 complexes. The processor, reading the interrupt signals from this network timer (TMR-S), measures the real time and if necessary the individual time intervals. The need for continuous execution of the time interval read programs and astonomical time after each interruption requires specific time expenditures of the central processor which could be used by it to perform more useful functions.

The use of a programmable timer TMR-P SM in SM-3 and SM-4 complexes makes it possible to do away with program accounting of time and to increase its useful return.

The programmable timer provides self-contained processing of programmable time intervals with shaping of the interrupt signals, recording of astronomical time and other operations. It can also be used to check the efficiency of the complex.

A further build-up of the interface capabilities (in load and length) is provided by series or parallel connection of the segmenters to the mainline of the complex or system. Parallel connection of the segmenters is preferable. The use of segmenters also significantly improves the configurations of the devices in the bays and outside them.

An interface segmenter may be used to design multiple complexes with a large number of high-speed devices with direct access to the memory that exceed the capabilities of a systems interface by its carrying capacity, load and (or) length.

No special software is required to control the operation of the device in the complex.

The interface segmenter has the following specifications and designation.

The interface is connected to the device by the small computer common bus at the input (the central segment of the communications mainline) and at the output (the peripheral segment of the communications mainline).

The method of connecting the device is series or parallel. The method of indicating the address zones on the peripheral sections of the common bus is rigidly programmed prior to the beginning of use (by means of electrically programmed PPZU of the K556RE4 type). The dimensions of the possible address and word zones are from 2 to 124 K (with spacing of two or more). The arrangement of the address zones is arbitrary.

The load capacity at the output comprises 19 load units. The natural load on the interface is one load unit through the input and output.

The geometric length of the interface mainlines after the segmenter is no more than 15.0 meters. The additional delay of the exchange cycle upon access to the device installed after the segmenter is no more than 0.5 microsecond.

The component base of the device is TTL-IS and SIS. The electronics capacity (in conditional integrated circuit bodies) is approximately 100.

The device is made structurally in the form of a small computer plug-in unit and the configuration of the cards is identical to the interface expander). The number of printed-circuit cards (two-plug) is two and the number of types of cards is one. The mass of the device is not more than 3.0 kg.

Power supply voltage is +5±0.25 V and consumed power is no more than 15.0 W.

The means of efficiency checking is the interface expander tester and the test programs for it.

Note. A special "Programmer" device for automatic broaching of this microcircuit by means of the SM-3 (SM-4) control computer complex can be set up together with the interface expander device to program the K556RE4 semipermanent memory unit.
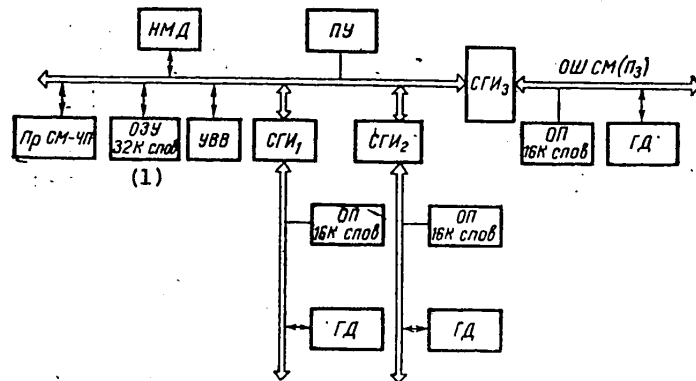
Figure 3.3. Structure of Computer Complex Based on SM-4 Control Computer Complex With Three EPG SM Connected Through Interface Segments

Key:
    1. Words

The use of a timer in the complexes that control facilities and processes in the real-time mode is especially effective.

The specifications of the programmable timer are as follows.

The interface connections of the device are the small computer common bus. The natural load on the interface comprises one load unit. The method of shaping the length of the time intervals and interruptions is apparatus.

The device operates in the single interrupt and repeated (cyclic) interrupt modes and the external signal counting mode with interruptions and the astronomical time counting mode without interruptions.

The rates of counting the time intervals with synchronization (for these modes) are 110 Hz from a crystal oscillator (with timing accuracy of not less than 0.01 percent) and 50 Hz from network frequency with deviation frequency of the external analog signal.

The component base is TTL-IS and SIS. The electronics capacity (in arbitrary integrated circuit housings) is 50. The device is made structurally in the form of a two-plug component unit. The mass of the device is not more than 0.6 kg. The power supply voltage is +5±0.25 V and consumed power is not more than 7.5 W.

The means of testing the efficiency is the programmable timer test. The identifiers of the device based on the "common bus" are ZP6 for the interrupt level and 104 for the interrupt vector.

The timer is included in the complex by installing its component unit on any free adjustable point in the BSI or BKI units which are in turn included in the BAM or

BRS units, respectively. An auxiliary unit of BE9514 components installed in the BSI or BKI cable compartment is used to connect the timer to the external signal sources or to signals with frequency of 50 Hz. This unit of components contains an optron isolator and matching resistors for reception of the external signal and a printed-card insert for connecting the external signal reception cables and the 50-Hz signal. The 50-Hz signal reception cable is included in the timer. The 50-Hz signal source is the connect-disconnect units (BVV) of the bay power supply of the complex.

The operation of the device is controlled by transmission of information (by means of the processor instructions) to its registers having the following addresses: 772540--instruction and state register (RKS), 772542--buffer register (RB) and 772544--counter register (RSCh).

The distribution of the RKS digits and the functions connected to them are presented in Table 3.1.

The buffer register (16-digit) is designed to store the counting intervals. It provides automatic reloading of the counter in the periodic interrupt mode. The buffer register is used only to write by the program and is reset by the PODG signal and also upon overflow or antioverflow in the single interrupt mode.

The counter register (16-digit) is a synchronous binary counter with the capability of counting in forward and reverse directions at one of four program-controlled rates. Information can be read during operation. In the direct counting mode, an interruption on the common bus is initiated with counter contents equal to 177777 (overflow). This mode is used to count external signals. An interrupt on the common bus is initiated in all digits (antioverflow) of the counter at zero in the reverse counting mode used when working with a previously set time interval.

3.4. Computer Integration Device

An ASU may include several multimachine control computer complexes as a function of the complexity, territorial disposition of the control facility, the importance of the problems being solved and other factors. The functions in multimachine complexes are always distributed among machines (subcomplexes). In this case one of the machines coordinates the actions of all other machines to solve a common pro problem.

Another type of organization of multimachine complexes is hierarchical construction of the system (the relationship between complexes is established by the seniority principle). For example, one or several parallel-operating lower level complexes (peripheral machines) gathers information from the controlled facility, first processes it and transmits it to an upper level subcomplex (a central machine-- TsM) for a production process control system. The central machine carries out secondary processing of the entered information and makes economic calculations and issues information to the lower level subcomplexes to change the operating mode of the facility.

Complexes with hierarchical structure may have two or more levels of hierarchy. Upper level subcomplexes usually perform more complex calculating functions and are constructed on processors of higher productivity than lower level subcomplexes.

Table 3.1. Functional Designation of RKS Digits of Programmable Timer

Digit	Name	Function
0	Operation	The counter register is triggered when set to "1." It is reset upon antioverflow and over-flow of the counter in the single mode and also by the PODG signal in all remaining cases
1.2	Assignment of counting rate	Provides selection of one of four possible counting rates:

Digits		Rate
"2"	"1"	
0	0	100 kHz
0	1	10 kHz
1	0	50 Hz
1	1	External signal

Both digits are set by the program and are re-set by the PODG signal

Digit	Name	Function
3	Operating mode	The operating mode is given with interruptions: periodic with "1" and single with "0." It is set by the program and reset by the PODG signal
4	Direct-reverse counting	The operating mode of the counter register is given: direct counting with "1" and reverse counting with "0." It is set by the program and reset by the PODG signal
5	Single step	A single time step of the counter is induced upon setting. Counting is under program control
6	Interrupt authorization	Setting of digit to "1" provides interrupt of processor program if the "Readiness" digit is also set to "1." Setting to "0" prohibits interruption. It is set by the program and re-set by the PODG signal
7	Readiness	It is set only upon overfilling and antiover-filling of the counter. It is reset by program or by the PODG signal
8-14	Not used	
15	Error	It is set (with periodic operating mode) when the last (second) overfilling or antioverfill-ing occurred prior to detection of the previous interrupt. It is reset either by program or by the PODG signal

Territorially concentrated complexes, in which the distance between central proces-sors of subcomplexes does not exceed 30-50 meters, do not require data transmission apparatus for organization of communications. Data transmission apparatus is re-quired in dispersed control computer complexes to organize communications between processors.

The small computer hardware contains devices that permit creation of hierarchical complexes of these two classes. Specifically, the USVM A71118 computer integration

device helps to solve the problem of designing concentrated hierarchical complexes and ASU based on them.

The USVM A71118 device is designed to organize multimachine hierarchical systems based on models of the M-4030 and M-4030-1 control computer complex (or any other computer of the YeS EVM series) as a central machine and one of the SM-3 or SM-4 complexes as the peripheral machine (PM).

The device is connected to the M-4030 (M-4030-1) model on one side and to the SM-3 (SM-4) control computer complex on the other side as a peripheral device.

The specifications of the device are as follows.

The interface is connected to a YeS EVM (with the possibility of connection to a multiplex MK or selector SK channels) on the side of the central machine and to the small computer common bus on the side of the peripheral machine. The algorithm of the YeS EVM is realized as schematic.

The possibility of organizing the beginning and end of an exchange session is accomplished at the initiative of any of the machines (peripheral or central machines).

The possible transmission modes on the side of computer integration device-central machine exchange when connected to the multiplex channel is monopole, multibyte (portions of eight bytes each) or multiplex (one byte each).* The possible modes of continuation of transmission on the side of the computer integration device-peripheral machine exchange is at the level of program control (upon interrogation of the readiness of the device), program interrupt or direct (extraprocessor) access to the internal storage.

The types of information exchange on the side of the peripheral machine are byte by byte in the program interrupt mode and word by word in the direct access mode.

Data are exchanged with the internal storage of the peripheral machine in the direct access mode under the control of only the program of the central machine and without any participation of the programs of the peripheral machine. The maximum data transmission speed in the program interrupt mode is 40,000 bytes/s and in the direct access mode is 400,000 words/s.

The device is program compatible with the A7119 computer integration device that provides communication of the M-4030 central machine with the M-400 control computer complex. The maximum distance between the integrated machines is up to 55 meters. The natural load on the common bus interface is two load units and the component base is TTL-IS.

The composition of the device is a control device (made in the form of a UTK cabinet of the modular computer equipment system), an interface unit (BI)(in the form of a complete small computer unit) is inserted in the bay of the SM-3 (SM-4) complex and a set of communications cable.

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*
During one communications cycle.

The overall dimensions are (B X L X H) are 600 X 650 X 880 mm for the cabinet and 482.6 X 767 X 146 mm for the interface block.

The power supply for the cabinet is from a three-phase AC network with neutral conductor at voltage of 380 V, 50 Hz and that for the interface units is from a single-phase AC network with voltage of 220 V, 50 Hz separated in the bay (cabinet) of the SM-3 (SM-4) complexes.

The mass of the cabinet is not more than 130 kg and that of the interface unit is not more than 20 kg.

The devices for checking efficiency are by means of testing the computer integration devices in the hierarchical system and by means of a built-in control console (in the cabinet) that simulates the operating mode of the central machine interface (M-4630) and so on in the self-contained mode with a peripheral machine.

The identifiers of the device on the common bus are ZPD and ZP5 for the interrupt level and the first vector 170 for the interrupt vectors; the second vector is 174.

The computer integration device is selected and responds to the instructions of the central machine and the peripheral machine exactly the same as any controller of a peripheral device. However, it utilizes these instructions to establish communications between the channels of the central and peripheral machines and to synchronize their operation rather than for working with the peripheral device.

The device consists of two parts: a cabinet (control device) and interface unit connected to each other by two cables. The distance between the cabinet and M-4030 device and between the cabinet and the interface unit is determined by the the lengths of the cables delivered with the device, which are equal to 16 and 5 meters, respectively.

The receivers and transmitters used in the device permit the cabinet to be separated up to 50 meters by means of an IKM-2 type cable. The design version of the device is shown in Figure 3.4. The structure of the hierarchical system based on the A71118 computer integration device is illustrated by Figure 3.5.
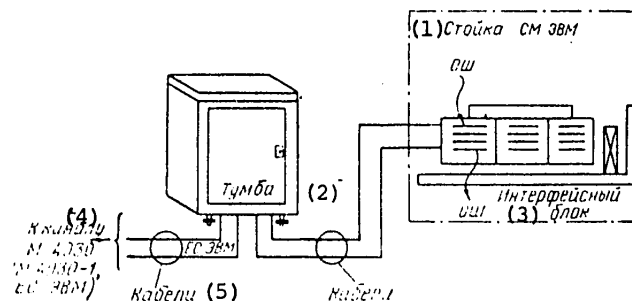

Figure 3.4. M-4030 (M-4030-1 and YeS EVM) and SM-3 (SM-4) Computer Integration Device
[Key on following page]

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[Key continued from preceding page]:

1. SM EVM bay
2. Cabinet
3. Interface unit

4. To M-4030 (M-4030-1 or YeS EVM) channel
5. Cables

Interaction of the device with the peripheral machine is organized by means of four program-accessible registers: a data register RD (address 777500), instruction and state register (address 777502), address register (address 777504) and length of file register (address 777506).

All the control information in the form of instructions and notations for communication of the computer integration device with the SM-3 (SM-4) is located in the instruction and state register. The functional designation of the digits of the instruction and state register is presented in Table 3.2. All the capabilities included in the instruction system of the SM-3 or SM-4 processors are used for working with these digits in the driver of the computer integration device from the direction of the peripheral machine. The algorithms for interaction of the computer integration device with the central machine after program initiation of the exchange mode are realized by the apparatus method.

The computer integration device is controlled by a special driver when working in the hierarchical control system (automated production control system and so on) from the direction of the peripheral machine and by means of a program that organizes the corresponding exchange modes when working from the direction of the central machine.

The program driver for working with the computer integration device includes DOS-ARM [Disk operating system of automated job sites] of the SM-3 and the small computer FOBOS [Basic real-time background-operating system].

3.5. The Common Bus Switch

As noted, the required high productivity of the complex can be achieved both by the use of highly productive components and by designing the complex in the form of a multimachine or multiprocessor system.

The reliability of the complexes is enhanced by using so-called "hot" redundancy of its individual components, which are automatically replaced by duplicate devices if they break down.

Such problems as access of each of the processors to each of the external devices common to them and to internal storage units, synchronization of the operation of processors with common data files and automatic reconfiguration of the complex if some of its components break down are solved when designing local multimachine complexes.

These problems help to solve intrasystems communications devices existing in the nomenclature of small computer hardware, specifically, the SM-4501 common bus switch (PSh SM).
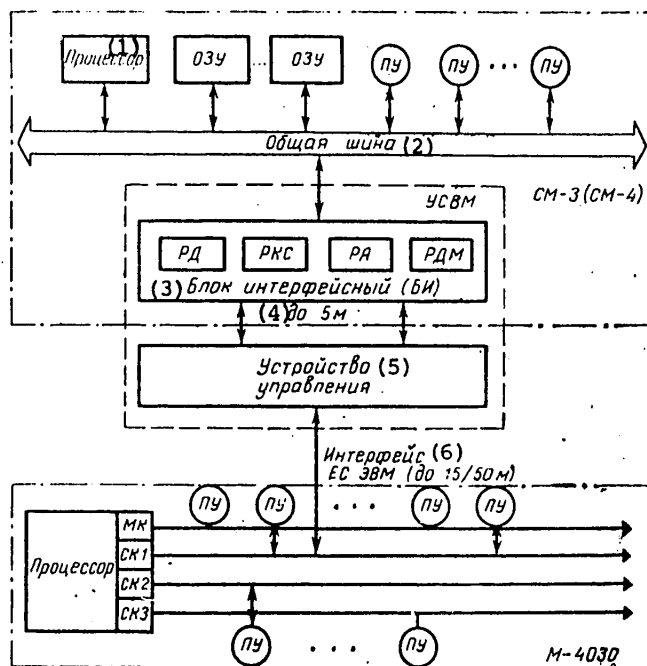
Figure 3.5. Version of Structure of Hierarchical System Using the A71118
Computer Integration Device (RD--data register; RKS--instruc-
tion and state register; RA--address register; RDM--length of
file register; PU--peripheral device)

Key:

1. Processor
2. Common bus
3. Interface unit

4. Up to 5 meters
5. Control device
6. YeS EVM interface (up to 15/50
   meters)

The common bus switch is designed to construct multimachine complexes of different
configurations on the basis of SM-3P and SM4P processors: two-machine complexes
with time-shared common devices, including the internal storage units, external
magnetic disk and magnetic tape storage devices, peripheral devices and systems
of enhanced reliability due to the use of one of the complexes (or part of it) in
"hot" reserve that is switched on automatically in place of one that is broken down.

The common bus switch is an electronic device that permits connection of an addi-
tional "Common bus" section to the common bus of one of two processors. Any de-
vices except the processor can be connected to the additional "common bus" section
(DSh) (Figure 3.6). The additional common bus section fully meets the requirements
of the Common Bus Interface Standard.

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Table 3.2. Functional Designation of Digits of Instruction and State Register of
           Computer Integration Device

Digits	Name	Function
0-2	Instruction or notation	Different instructions to the device from the direction of the peripheral machine program to continue or halt operation of data exchange
3	Byte arrangement notation	Indicates the order of byte arrangement of the central machine in the word issued to the memory (or received from the memory) of the peripheral machine at the extraprocessor level
4,5	Memory expansion	Permits the device to utilize all 18 digits of the common bus address
6	Interrupt authorization	Indicates whether the peripheral machine program authorizes work in the program interrupt mode Note. Digits 0-6 can be set only by the peripheral machine program
7	Data register request	Used only during operation of the device in the SM-3 mode to indicate readiness for the next data transmission cycle
8	Instruction and state register request	Used only during operation of the device in the SM-3 mode; informs of the readiness to transfer any information of state to the peripheral machine program Note. Digits 7 and 8 are set by apparatus and can only be read by the peripheral machine program for organization of work in the readiness interrogation mode
9	Execute	Used only in the SM-3 mode when organizing work on readiness interrogation to indicate to the device completion of the next data transmission cycle by the peripheral machine program
10	SM-3 mode	Indicates in which mode (SM-3 or M-400) the device is. Writing a one in the given digit converts the device to the SM-3 mode
11	M-400 mode	Writing a one in the given digit converts the device to the M-400 mode in which complete program compatibility with the A7119 computer integration device is provided Note. Digits 9 and 11 can be only written by the peripheral machine program and digit 10 can also be read.
12	Parity error	Indicates that information with incorrect parity was detected during data transmission from the central to the peripheral machines

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Table 3.2 [Continued from preceding page]:

Digits	Name	Function
13, 14	Halt or reset	Indicates the reason for completing the data exchange operation
15	Response delay (time out)	Indicates that the device turned to a nonexistent memory cell during data transmission at the extraprocessor level Note. Digits 12-15 are set by apparatus and can only be read by the peripheral machine program
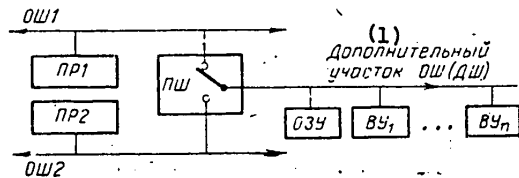
Figure 3.6. Diagram for Connecting Additional Devices Through the Common
Bus Switch: two processors (PR1 and PR2), internal storage
device and external devices (VU)

Key:
1. Additional common bus section

The common bus signals are relayed by the switch without distortion. Thus, if the common bus switch were connected to the additional common bus processor, the operation of the processor with devices connected to the additional common bus is provided as if these devices were connected directly to the common bus. Exchange can be carried on with them both through the program channel and through the direct-access channel. The delay of the signal transmission cycle through the common bus switch is no more than 500 nanoseconds.

The common bus switch consists of two identical structural and electrical sections, each of which is connected to the common bus of the corresponding processor (see Figure 3.6). There is also internal communication between sections in the form of common signals.

The load capacity of each section of the common bus switch is two load units at the input and 18 load units at the output. The control modes of the common bus switch are local manual, remote manual and program.

The component base is series K131, K155, K559 and K599 microcircuits. The common bus switch is structurally formulated in the form of a self-contained complete unit built into the standard small computer bay. The overall dimensions of the common bus switch are 667 X 482 X 266 mm and the mass is not more than 30 kg.

Power is supplied from a stabilized DC source of 5 volts. The consumed power is 0.5 kV·A.

Each of the common bus switch sections identical in structural and electrical version is connected to the common bus of the corresponding processor. Each section contains its own switch which performs the functions of an electronic key and a common bus expander that regenerates and relays signals.

The switch itself consists of an addressable monitoring and state register (RKS), address selector, interrupt signal shaping unit, signal shaping unit for communications between two switch sections and a timer.

The state of the switch is monitored and controlled by information reading and writing to the corresponding digits of the monitoring and state register. The address of the monitor and state register and the vector interrupt address are conferred on each section of the common bus switch. The address of the monitor and state register is 177420. The range of addresses 177420-177436 is reserved to connect several common bus switches to their monitor and state register.

The address of the interrupt vector is 540. If need be, the user can change the address of the interrupt vector to 544 by means of jumpers.

The processor, referring to its own common bus switch section, displays the address of the monitor and state register on the address buses and enters the necessary information in the specific digits of the monitor and state register or reads them. The designation of the digits of the monitor and state register is given in Table 3.3.

Each section of the common bus switch has its own timer that is started if the processor must be connected to the additional common bus section, which may be connected to the first or second processor or may be in a neutral position.

If the additional common bus section is in the neutral position, the following operating modes of the timer are possible:

if the additional common bus section is connected to the requesting processor for 10 milliseconds, the timer of the common bus switch section of this processor is reset;

if the additional common bus section is not connected to the requesting processor for 10 milliseconds, the timer is reset during this time and digit 15 of the monitor and state register is set.

If the additional common bus section is connected to one of the processors (A), digit 12 of the monitor and state register is set, the signal for interruption of processor A is shaped and the timer is started upon request to the additional common bus section of another processor (B) in the common bus switch section connected to processor A.

Processor A, having completed the interruption, may disconnect the additional common bus section by resetting digit 0 of the monitor and state register or may

Table 3.3. Functional Designation of Digits of Monitor and State Register

Digits	Name	Function
1	2	3
0	Request	Set by request of the processor to connect the additional common bus section. If the additional common bus section is free, connection occurs immediately (no later than within 1 microsecond). If the additional common bus section is occupied by another processor, digit 12 of the monitor and state register in the section of this processor working with the additional common bus section is automatically set and the timers of both sections are switched on. If the processor working with the additional common bus section does not release it and does not reset digit 12 of the monitor and state register of its own section of the common bus switch during the timer cycle, digit 0 of this monitor and state register is reset and emergency release of the additional common bus section occurs. If the processor releases the additional common bus section during the timer cycle of the section of the common bus switch of the requesting processor working with the additional common bus section, the additional common bus section is connected to the requesting processor
6	Interrupt authorization	Set by the processor to authorize interrupt of the common bus switch in the following cases: upon connection of the additional common bus section, if the additional common bus section is active and is requested by another processor and upon completion of the timer cycle. It is accessible to the processor for reading and writing
7	Connection	Set for reporting to the processor that the additional common bus section is connected to it and for authorization for signals to pass from the common bus to the additional common bus section. It induces interruption together with digit 0 if digit 6 is set. It is accessible for reading. It automatically sets digit 11 of the monitor and state register of an adjacent section of the common bus switch.
9	Initial setting	It is set to emit an initial setting pulse (RESET) to the additional common bus section if it is connected. It is automatically reset

[Table continued on following page]

Table 3.3 [Continued from preceding page]:

<u>Digits</u>

10	Interrupt authorization	It is set by the processor to authorize interruption of itself upon completion of the work of another processor with the additional common bus section
11	The additional common bus section is connected to another processor	It is set by the common bus switch by digit 7 of the adjacent section of the monitor and state register. The additional common bus section is occupied by another processor if bit 11 is set
12	Request from another processor	It is set so as to inform the connected processor of the request for the additional common bus section from another processor. It causes interruption jointly with digit 6. It switches on the timer. It is accessible to the processor for reading and reset
13	Activity	It is set to initiate occupation of the additional common bus section. It is accessible to the processor for reading
14	Main power supply emergency	It is set upon the appearance of the main power supply emergency signal on the additional common bus section. It is accessible to the processor for reading
15	Timer overflow	It is set if the additional common bus section was not connected by request during the timer cycle. It is accessible to the processor for reading

Note. The remaining digits of the monitor and state register are not used.

continue working with the additional common bus section, by resetting digit 12 of the monitor and state register.

If digit 12 of the monitor and state register is not reset by processor A and the additional common bus section will not be released by it, this situation will be regarded within 10 milliseconds as breakdown of processor A and the additional common bus section is automatically disconnected from it.

Let us consider as examples some possible configurations of multimachine complexes that utilize common bus switches.

The configuration of a two-machine complex with two time-shared processors PR1 and PR2 with external magnetic disk memory NMD3 and external magnetic tape memory NML3 is shown in Figure 3.7. The time-shared external memory units NMD3 and NML3 are connected to the common bus of processor PR1 and are accessible to it in the position of the common bus switch key (position "A"). During this time processor PR2 can perform operations that do not require exchange with NMD 3 and NML3. If processor PR2 needs to exchange information with these devices, several methods of

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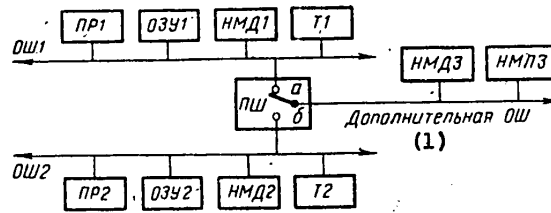
Figure 3.7. Configuration of Two-Machine Complex With Two Time-Shared
Processors PR1 and PR2 with External Storage on NML3 and
NMD3 (T1 and T2 are terminal devices)

Key:
    1. Additional common bus section

satisfying it can be organized by means of the control and informing digits of the
monitor and state register.

Method 1. Processor PR2 periodically sends requests to use the additional common
bus. Each such request causes an interruption in the processor working with the
additional common bus. But until the additional common bus is required by this
processor, it extinguishes digit 12 (no later than within 10 milliseconds) in the
monitor and state register of its own section set during each request of PR2 for
the additional common bus. When PR1 completes operations with the additional com-
mon bus, it releases it and PR2 gains access to the devices connected to the addi-
tional common bus.

This method has the advantage that the working order of PR1 is determined simul-
taneously with sharing the external devices connected to the common bus between two
processors. If PR2 does not extinguish digit 12 within 10 milliseconds from the
moment the request occurs on the additional common bus, this fact is identified as
a breakdown of it and the additional common bus is automatically disconnected from
it. The disadvantage of this method may be regarded as the additional time expen-
ditures to organize periodic requests of PR2 for the additional common bus and to
process interruptions from these requests in PR1.

Method 2. Processor PR2, if there is a need for common devices, sends a request to
the additional common bus. If the additional common bus is free, it is immediately
connected to PR2. If the additional common bus is occupied by PR1 (digit 11 of the
monitor and state register of the requesting processor is set to one), PR2 sets
digit 10 of the monitor and state register of its own section to one and changes
the tasks requested by the additional common bus to the interrupt wait mode until
the additional common bus is free. Two problems can be processed on the processor
in this case. PR1 releases the additional common bus after the exchange with the
shared (common) devices is completed. After the additional common bus is released,
there is an automatic interruption in PR2 which may connect the additional common
bus to itself and carry on exchange with common devices.

This method can be used only with distrib.tion of common devices between processors. Breakdown of a processor working with the additional common bus cannot be established by this method (if only the processor working with the additional common bus did not break down prior to the request of the other processor for the additional common bus). These two methods can be used in the system. For example, if one of the problems whose functions is following the efficiency of PR2 is being solved, method 1 is feasible when working with the common bus switch. Method 2 is used to solve the remaining problems which require an exchange with common devices.
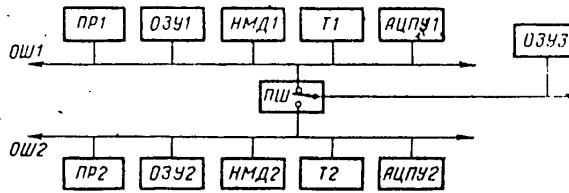
Figure 3.8. Configuration of Two-Machine Complex With Internal Storage Unit OZU3 Shared Between Processors PR1 and PR2

The configuration of a two-machine complex with internal memory unit OZU3 shared between processors PR1 and PR2 is shown in Figure 3.8. The logic of the processors working with shared internal memory unit OZU3 may be similar to that presented above. It is important for this scheme that the total capacity of the internal storage, including the common internal storage with which each of the processors will work, not exceed the maximum memory capacity of the processor being addressed. The maximum capacity of the internal storage unit being addressed comprises 28K words for the SM-3 processor and 124K words for the SM-4P processor.

Different examples of making the equipment redundant by using a common bus switch are illustrated by Figures 3.6, 3.9 and 3.10. The redundancy scheme that provides for maintenance of system efficiency upon failure of one of two processors is shown in Figure 3.8. However, devices connected to the additional common bus section are not redundant.
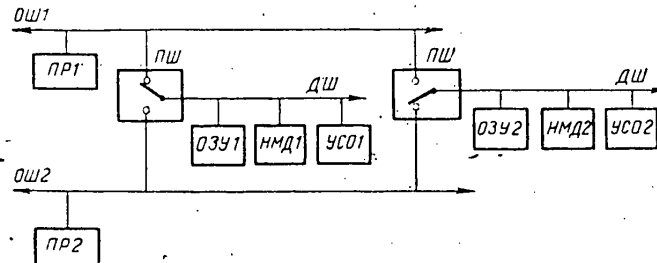
Figure 3.9. Example of Redundancy of Common Bus Switch (USO--control facility integration device)

Redundancy upon failure of any of the devices of the system, including the common bus switch itself, is presented in Figure 3.9. An example of redundancy with simultaneous failure of several devices is illustrated by Figure 3.10.
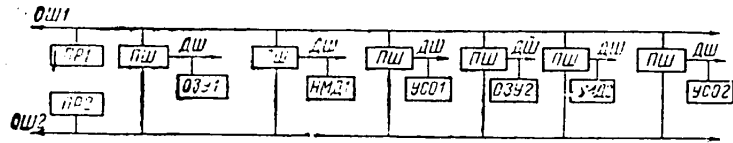
Figure 3.10. Redundancy Scheme of Several Devices

Systems having increased survivability can be designed by using a common bus switch in combination with an interprocessor communications adaptor (AMS) of the "window" type. An example of designing this system is given in Figure 3.11.
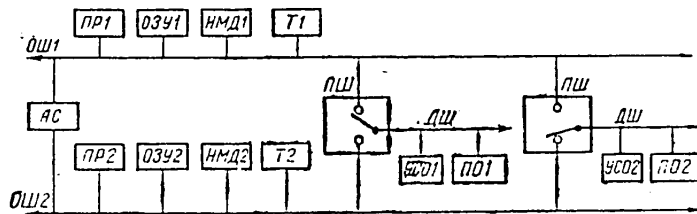
Figure 3.11. Diagram for Designing Systems of Increased Survivability Based on Common Bus Switch and Interprocessor Communications Adaptor (PO--operator's console)

3.6. Interprocessor and Remote Communications Adapters

Devices for communication (information exchange) between processors included in a multiple complex or between complexes that form a system and equipment switching devices for organization of redundancy (for example, bus switch devices) are required to organize interprocessor communications.

Communications devices may be of two types as a function of the structure of the complexes (frequently determined by the requirements of the control facility and the ASU). High-speed devices for communication between the interfaces of processors located in the same building and which form a unified complex are related to intrasystems communications, while devices for communication between individual complexes that form a system, but remote from each other (from hundreds of meters to kilometers or more) are related to remote communications. Intrasystems communications (which the systems interface of the small computer common bus is primarily related) permit a length of the cable communications mainlines of not more than 15.0 meters.

The data prepared by a single processor in complexes with sharing of functions between processors located near each other should be rapidly transferred to the other processor for subsequent processing.

An interprocessor communications adapter (AMS SM) that provides rapid access not only to the memory but to any of the peripheral devices from any of the processors (the common buses of which are connected through the adapter) meets the requirements of providing rapid intrasystems communications between complexes.

The Interprocessor Communications Adapter (AMS SM)

The interprocessor communications adapter is designed for communication of two computer complexes that utilize the small computer common bus interface (specifically, for communication of SM-3 and SM-4 complexes). The adapter can be used during joint operation, mutual redundancy of two complexes and for one complex to receive data from another and for other purposes.

The adapter permits access of each of the connected processors to the memory or peripheral device of the other system as if each of them belonged to its own system. Access from one complex to the device of another complex is carried out by ordinary processor instructions using a specially allocated address zone for this-- the so-called window. The window address is the source complex is interpreted by the adapter as the window address of another complex, called the target complex.

The specifications of the device are as follows.

The interface for connecting the device to each of two connected complexes is the small computer common bus. The method of connecting the device to each of the connected buses is parallel (usual for connection of peripheral devices to the common bus). The load on each of the interfaces of OSh-1 is one load unit.

The operating mode of the device is working by program in the source complex using the window addresses and in this case each access to the window is realized on the target bus as a direct-access transmission, working by interruption and referring to the registers of the device to prepare or monitor the communications through the adapter.

The size of the window is selected during design of the system and may comprise 512, 1K, 2K, 4K, 8K, 16K and 32K words. The location of the window on the target bus is assigned by program prior to the communications session through the adapter.

The additional delay introduced by the adapter during each transmission cycle to another bus is no more than 0.4 microseconds.

The component base is TTL-IS and SIS. The electronics capacity (in artibrary integrated circuit housings) is 250. The design version is the small computer plug-in unit: four printed-circuit cards (two-plug electronics units) and two card types.

The device is installed in the systems expansion unit (BRS) and in the bay of one of the connected complexes. The mass of the device is no more than 4.0 kg. The power supply voltage is $+5\pm0.25$ V and consumed power is no more than 25.0 watts.

The efficiency testing equipment is the interface expander tester (using a single complex); the test programs are the interprocessor communications adapters (with connection of two complexes).

The adapter identifiers on the common bus are the ZP7 for interrupt level; the vector address is selected from the floating vector zone (cell 300 and above) for the interrupt vector.

The interprocessor communications adapter is located in one of the connected complexes. Communications with the second complex is accomplished by its common bus cable. If the reserve length of the common bus cable of the second complex is exhausted and does not permit "extension" to the adapter, the interface expander is used to lengthen the common bus.

When used as the communications channel of two control computer complexes, the interprocessor communications adapter performs two functions: realizing the direct (extraprocessor) communications cycle during access through the window of one complex to the device of another and program interruption upon a signal from one complex or by an error in operation through the window.

Communicatios between complexes is accomplished by relay by the device of access to a specific range of addresses of the common bus, called a window, during requests for direct access to another bus.

The window may be located in any unutilized address zone and may have dimensions from 512 to 32K words. The zone on the source bus in which the window is located and its dimensions are determined during assembly of the complex and are permanent for it.

The range of addresses of the target bus to which the source bus may gain access is equal in value to the window and its location on the target bus is assigned by program during organization of the communications session through the window. Thus, it can gain access to any address of the target bus.

Access through the window can proceed from any device capable of being the controller on the bus by means of any instruction that contains an address selection. Thus, instruction access and data reading and writing can be carried out.

The device is functionally symmetrical: any of two buses connected by it may be a source or target in the communications cycle; any processor can gain access to another complex.

The common bus interface of one complex can be connected to those of other complexes by means of the corresponding number of interprocessor communications adapters. The connection of each pair of complexes is independent.

Each processor controls access to the devices of its own complex. It can prohibit access to them from another bus or can restrict it to reading, having prohibited writing; it designates the address file to which another complex can gain access through the window.

The processor itself also controls authorizations for interruption of its own program by requests from the interprocessor communications adapter. The authorized interruption may occur for two reasons:

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upon a signal that an adjacent processor has prepared data for the complex connected to it;

upon a signal that access to a related bus through the window was not successful since there was no authorization for access, there was no authorization for writing with the request to an adjacent bus for writing; no response was received from it upon referral to the adjacent bus (that is, a "time out" signal was generated if the second bus did not respond within 100 microseconds).

Table 3.4. Composition and Function of Registers of Interprocessor Communications Adapters

Register	Notation Part A	Part B	Program Operation	Address
1			4	5
Control and state	ARU	BRU	READ/WRITE	XXXX00
Output data buffer	ARD	BRD	READ/WRITE	XXXX02
Output data buffer	BRD	ARD	READ	XXXX04
Displacement address	ARS	BRS	READ	XXXX06
Transposition address	ARP	BRP	READ/WRITE	XXXX10
Effective address	ARA	BRA	READ	XXXX12
Vector address	ARB	BRB	READ	XXXX14

Notes.
1. The octal digit of the address given for each complex individually is denoted by the symbol X in the table.
2. The functions for the data buffer registers--output for complex A and input for complex B--are performed by the same register; access to it from complexes A and B occurs by different addresses as indicated in Table 3.4.
3. There is no separate displacement address register; the lowest orders of the effective address register are read upon access by address XXXX06. The number of of digits that comprise the displacement address are determined by the size of the window.

These reasons were disregarded if interruption was not authorized. If interruption was authorized, the occurrence of one of these situations causes generation of an interruption request through level ZP7 from the interprocessor communications adapter.

The program that services this interruption analyzes its reasons, using the state of the digits of the control and state register (RU) of the device. The other addressable registers contained in the adapter are presented in Table 3.4. The interprocessor communications adapter that connects two common buses is symmetrical with respect to these buses and has two identical parts (arbitrarily denoted by A and B; the same letters--A and B--are contained in the notation of the registers of each part of the device).

Table 3.5.   Functional Designation of Digits of Control and State Register of Interprocessor Communications Adapter

Number of Digit	Name	Method of Writing	Function
1	2	3	4
0	New data for another bus	Program	Indicates to another processor that data are ready for it
1	Write authorization from another bus	Program	Authorizes writing from another bus through the addresses of its own bus
2	Write authorization to another bus	Automatic, repeats digit 1 of adjacent control and state register	Authorizes writing through addresses of another bus
3	Data for another bus (digit 1)	Program	Is loaded for transmission to another bus
4	Data for another bus (digit 2)	Program	Is loaded for transmission to another bus
5	Data for another bus (digit 3)	Program	Is loaded for transmission to another bus
6	Interrupt authorization	Program	Authorizes interrupt request through level ZP7 upon error (digit 15) or readiness of data from adjacent processor (digit 12)
7	Authorization of access to another bus	Automatic, repeats digit 8 of adjacent control and state register	Indicates that access can be gained to another bus through the window. An attempt to gain access with reset digit 7 leads to setting of digit 15
8	Authorization of access from another bus	Program	Authorizes access to its own bus from another complex. Other data for interaction (digit 1, transposition address and so on) should be prepared prior to setting
9	Data from another bus (digit 1)	Automatic, repeats digit 3 of related control and state register	

[Table continued on following page]

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Table 3.5 [Continued from preceding page].

Number of Digit 1	Name 2	Method of Writing 3	Function 4
10	Data from another bus (digit 2)	Automatic, repeats digit 4 of adjacent control and state register	
11	Data from another bus (digit 3)	Automatic, repeats digit 5 of adjacent control and state register	
12	New data from another bus	Automatic, repeats setting of digit 0 of adjacent control and state register	Indicates that another processor prepared data for operation of the first processor. If the interrupt authorization digit (6) is set, interruption is initiated
13	Power supply failure	Automatic, upon power supply failure in target bus	
14	Time out	Automatic, if response from another bus is not received within 100 microseconds	Sets error digit (15)
15	Error	Automatic, if access to another bus is not gained	Prohibits access through window; causes interruption with set interrupt authorization digit (6)

Note. The control and state register is only partially accessible for writing by program: it can write only digits 0, 1, 3-6 and 8 by program.

All these registers should be programmed prior to a communications session.

The control and state register is used to store the notations which organize the operation of the device or serve to monitor it (Table 3.5).

Data for transmission to another bus are written in the 16-digit buffer data register (RD). The buffer data register is used in the following cases (the ARD is set for definiteness, and the same is true of the BRD):

with writing through the window is bus A (data are entered in the register from bus A and are stored there until transmission to bus B);

with reading through the window if the source is bus B (the read information is entered in the register from bus A);

if new data must be transmitted to bus B they are entered in the register by program from bus A and can be read on bus B by the program that services interruption (data can be transmitted in this manner only if there is prohibition of data transmission through the window--with reset digit 8 of the control and state register).

Information can be written in the buffer data register by program only from its own bus (from bus A in the ARD) through the address XXXX02 and can be read from both buses: through address XXXX02 from its own bus (A) and through address XXXX04 from an adjacent bus (B).

The real address of the target bus through which access through the window is gained is stored in the effective address register of bus A. This address is formed of two parts. Thus, the address whose lowest orders are selected from the window address displayed by the control device to address sub-bus A and whose highest orders are selected from transposition address register prepared beforehand by complex B during organization of communications through the window is located in effective address register A upon access from bus A to bus B through the window address. The contents of the buffer data register A are transmitted by the inter-processor communications adapter to address bus B and is perceived by complex B as the effective address.

The contents of effective address register A (the address of bus B to which complex A gains access) is read upon access through address XXXX12 in complex A and the contents of the lowest orders of the effective address register A are read through address XXXX10 (the address inside the window is the so-called displacement address).

The effective address register is 16-digit, the transposition address register is 8-digit and the displacement address register B does not exist separately: the displacement address is contained in the lowest orders of effective address register A. The digits of the effective address register A which are the address inside the window are sent to the bus when reading through address XXXX06 of displacement address register A.

Vector address register B (may be 9-digit) is the set of contacts soldered to voltage levels "0" or "1" as a function of the significance of the corresponding digits in the vector address. The outputs of vector address register B are connected to the corresponding data sub-bus of the common bus if there is an interruption by signal ZP7--interrupt request from the interprocessor communications adapter.

Execution of interaction operations through the window (including interruption through level 7) is considered in the corresponding technical description for the interprocessor communications adapter.

In a real complex, any unutilized address unit with capacity from 512 to 32K addresses of the common bus can be used as a window for connection of the interprocessor communications adapter. It is usually located behind the last module of the internal storage. Thus, for example, organization of a window having capacity of 4K words that occupies the range of addresses from 24K to 28K words is possible in a system with internal storage of 24K words.
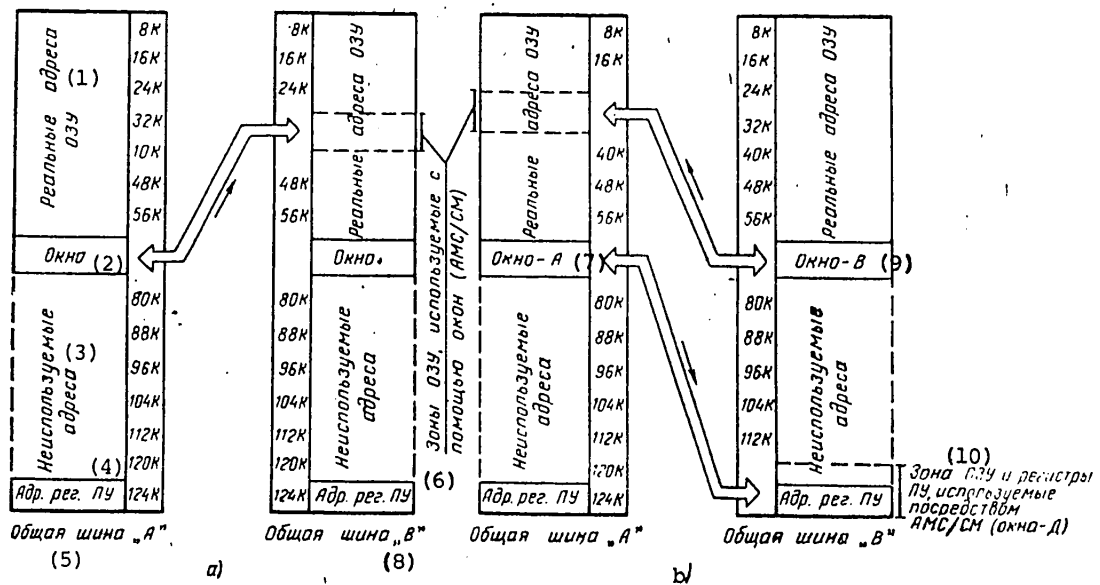

Figure 3.12. Example of Communications of Two Computer Complexes With Identical Processors Through the Interprocessor Communications Adapter By Means of a Single Window (a) and a Window That Realizes Two Independent Communications Channels (b)

Key:
1. Real addresses of internal storage device
2. Window
3. Unutilized addresses

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[Key continued from preceding page]:

4. Address register of peripheral device
5. Common bus A
6. Internal storage zones used by means of windows (interprocessor communications adapter)
7. Window A
8. Common bus B
9. Window B
10. Internal storage zone and external device registers used by means of interprocessor communications adapter (window D)

An example of communication of two complexes through the interprocessor communications adapter is shown in Figure 3.12. Let OShA be common bus A that initiates access and let OShB be common bus B to which access proceeds. A window with width of 8K addresses in common bus A is located beyond address 64K. The window on common bus B is arranged in similar fashion (the identity of the addresses is not compulsory). Reading is initiated through address X from the range of addresses 32-40K of common bus B. Complex A issues read instructions through address X located in the range of addresses 64-72K of the window of common bus A in the following sequence:

processor A issues a request for bus A through address X;

the interprocessor communications adapter (window) converts this address to that located in the range of 32-40K of common bus B and formulates the request to common bus B (with the highest priority at the extraprocessor level of interruptions) to gain access through this address;

the data from common bus B are transmitted to the interprocessor communications adapter;

the data from common bus B are transmitted to processor A during the final phase of the instruction issued through common bus A. Thus, information is transmitted from the internal storage of system B by a single instruction of the processor of system A.

An example of communications through the interprocessor communications adapter, where two independent communications channels between the common buses are realized by means of the windows, is shown in Figure 3.12b. Unlike the previous example, reading and writing through the interprocessor communications adapter is authorized for both systems. Access from system A through the interprocessor communications adapter to the NMD [magnetic disk carrier] registers of system B initiates transmission of the information file from the NMD of system B to the memory of system A.

Extraprocessor transmission of the information file from the NMD of common bus B to the range of addresses 68K-72K windows of common bus A is prepared by issuing instructions to the processor of system A to write through the corresponding addresses lying in the range of addresses 68K-72K windows of common bus A

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automatically converted by the interprocessor communications adapter to the addresses of the NMD registers of common bus B. The addresses of the window of common bus B are automatically converted in the adapter to the addresses of the previously selected memory zone of the common bus during transmission of the file. Thus, the interprocessor communications adapter permits system A to initiate transmission of the magnetic disk carrier of system B directly to its memory at the direct-access level.

The common bus of any system may have several windows (interprocessor communications adapters) for communicating with other systems.
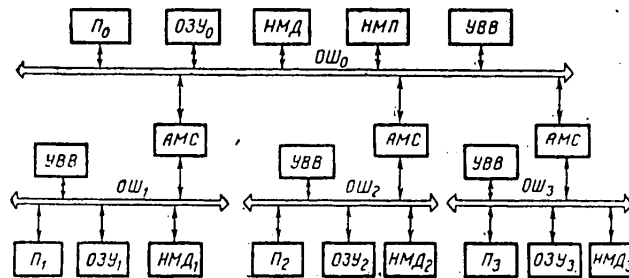
Figure 3.13. Hierarchy of Computer System Based on Four Single-Processor Computer Complexes With Communications Through Interprocessor Communications Adapters

Multiprocessor complexes can be constructed by combining single-processor complexes into a system by using interprocessor communications adapters (Figure 3.13). In this case the common operating system is stored in the internal storage of the central processor (this same system can be organized as a four-machine system if each of the processors in it has its own operating system). Another example of organizing a computer complex on the basis of an interprocessor communications adapter may be the system shown in Figure 3.14.

The working programs that utilize the interprocessor communications adapter contain special small computer software.
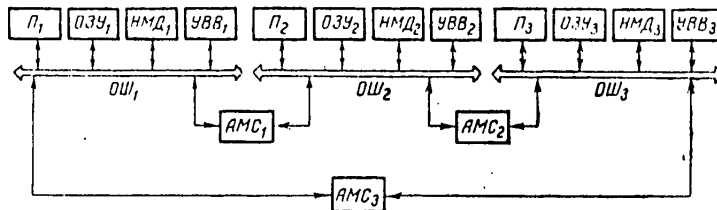

Figure 3.14. Multimachine Computer Complex With Circular Communication Through Interprocessor Communications Adapters

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Remote Communications Adapter (ADS SM)

The problem of communications of remote SM-3 and SM-4 complexes with each other and with remote terminals is partially solved by means of remote communications adapters (ADS-1 SM, ADS-2 SM and ADS-3 SM) in the small computer system. The use of adapters is feasible if the number of communications channels which must be connected to a single SM-3 or SM-4 complex is small (not more than 10-20). These adapters can be adjusted for operation over a wide range of data transmission speeds--from 50 to 9,600 bits/s.

The use of remote communications adapters in SM-3 and SM-4 control computer complexes permits essentially new capabilities of ASU design such as remote data processing in hierarchical (and other decentralized) systems that are essentially computer networks, data and program exchange between computers and consequently between network users, creation of distribution data banks accessible to many users and redistribution of computer and other capacities between different processing centers if necessary. Realization of the principles of remote data processing also permits one to come closer to solving the problem of more complete loading and more efficient use of still rather expensive computer equipment of ASU.

It is insufficient to design effective remote processing networks on the basis of existing small computer hardware of single adapters of the remote communications adapter type. Development of other computer integration devices with standard and special communications channels and lines: data transmission multiplexers, communications channel concentrators, other types of synchronous and asynchronous communications adapters (including high-speed) and so on, is being accomplished with regard to this circumstance within the framework of the program of small computer hardware development.

A number of remote communications adapters is designed for construction of single- and multimachine ASU (including multilevel hierarchical systems) and collective-use computer systems with remote data processing when they are used in SM-3 and SM-4 complexes. The adapters permit connection of such devices of the data transmission system as modems, signal conversion devices and terminal devices (VT-340 display and T-63 teletype) to the common bus systems interface of SM-3 and SM-4 complexes.

Information exchange between interacting SM-3 complexes, for example, with SM-4 complexes (or with computer complexes of the unified computer system) or between complexes and remote terminals (including communications with user stations of the unified computer system) through nonswitchboard and switchboard industrial, municipal and long-distance telephone communications channels and also over special communications lines can be organized when operating at long distances by means of modems (or signal conversion devices) connected to remote communications adapters at junction S2.

The characteristic feature of each of these adapters is its asynchronous operating mode that determines the need for all devices connected to the adapter also to operate in the asynchronous mode.

Table 3.6.   Characteristics of Communications Channels of Remote Communications
             Adapters

ADS-1 Communications Unit

Characteristic	Channel 1	Channel 2
Connected apparatus	Modem	Modem
Designation and interface of channels of remote communications adapter	Connected to telephone (TLF) channel through modem (MDM). Integration with modem with standard junction (interface) S2. Operation in duplex and semiduplex modes	Connected to telephone channel through modem. Integration with modem through junction S2. Operation in duplex and semiduplex modes
Format of data to be transmitted	1 "start" bit, 8 information bits, 1 check (evenness) bit and 2 "stop" bits	1 "start" bit, 8 information bits, 1 check (evenness) bit and 2 "stop" bits
Length of communications line (L) and data transmission speed (V)	Length of communications line is determined by modem used, V = 50-9,600 bits/s	Length of communications line is determined by modem used, V = 50-9,600 bits/s

ADS-2 Communications Unit

Characteristic	Channel 1	Channel 2
Connected apparatus	Modem	VT-340 display or analog device
Designation and interface of channels of remote communications adapter	The same as for ADS-1 communications unit	Connected to VT-340 display by special four-wire communications line. Data to be transmitted and received are represented by two-pole current bursts with nominal current of $\pm$ 20 mA
Format of data to be transmitted	The same as for ADS-1 communications unit	1 "start" bit, 7 information bits, 1 check (evenness) bit and two "stop" bits
Length of communications line (L) and data transmission speed (V)	The same as for ADS-1 communications unit	$L \leq 10$ km; V = 50-9,600 bits/s

ADS-3 Communications Unit

Characteristic	Channel 1	Channel 2
Connected apparatus	Modem	T-63 teletype
Designation and interface of channels of remote communications adapter	The same as for ADS-1 communications unit	Connected to T-63 teletype by special two-wire communications line. Single-pole current bursts with nominal line current of 40 mA are used to receive and transmit data

[Table continued on following page]

Table 3.6 [Continued from preceding page].

ADS-3 Communications Unit

Characteristic	Channel 1	Channel 2
Format of data to be transmitted	The same as for ADS-1 communications unit	1 "start" bit, 5 information bits, 1 "stop" bit (on reception) and two "stop" bits (on transmission)
Length of communications line (L) and data transmission speed (V)	The same as for ADS-1 communications unit	$L \leq 10$ km; $V = 50$ and 100 bits/s

The systems unit of remote communications adapters (BS ADS) is formed of two functionally independent remote communications adapters structurally configured in the same body. Thus, each systems unit of remote communications adapters (as a single device) provides output of data transmission on two independent channels when connected to the SM-3 or SM-4 complex. Three versions—the BS ADS-1, BS ADS-2 and BS ADS-3—are produced as a function of the types of data transmission channesl of the adapters installed in the body.

The characteristics of the channels of each type of systems block of remote communications adapters are presented in Table 3.6. The characteristics and indices of designation are common for all three types of systems units of remote communications adapters.

The interface is the small computer common bus for connection to unified computer system complexes and S2 for peripheral devices and terminals, there is a four-wire interface for the VT-340 and a current loop (40 mA) for the T-63. The number of data transmission channels is up to two. The communications lines are telephone, telegraph and physical lines.

The operating mode of the adapters is asynchronous (start-stop). The method of data transmission is sequential. Data are transmitted in the semiduplex and duplex modes at speeds of 50, 100, 200, 600, 1,200, 2,400, 4,800 and 9,600 bits/s.

The digit capacity of the information code to be transmitted is 5.7 or 8 (see Table 3.6 for the data format). The number of stop-digits is one or two. The information code is monitored by parity or without monitoring.

The natural load on the common bus is four load units (two each for each adapter).

The component base is TTL-IS, SIS and other microelectronics components.

The composition of the device and the design version is as follows: the systems block of the remote communications adapter consists of a six-row plug-in chassis and a set of single-plug component units and interface cables installed in the

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chassis; the number of component units and types of cards are 11/6 for the BS ADS-1, 11/8 for the BS ADS-2 and 11/8 for the BS ADS-3.

The overall dimensions are 271 X 456 X 97 mm and the mass of the device is not more than 5.0 kg.

The power supply voltage is +5 V $\pm$ 5 percent and 60 V at frequency of 20 kHz (a power supply source of type BP 113/SM is recommended). The consumed power (through the +5 V circuit) is not more than 18.0 watts. The efficiency testing equipment in the SM-3 (SM-4) complex is in testing the systems unit of the remote communications adapter.

The identifiers of the first systems unit of the remote communications adapter for the common bus are the ZP4 for the adapter interrupt level, 310 (for the receiving part) and 314 (for the transmitting part) for the neutral adapter and 320 (for the receiving part) and 324 (for the transmitting part) for the first adapter. The vectors for the other systems units of the remote communications adapter are selected in the zone of variable (floating) common bus vectors, continuing the vectors of the first remote communications adapters--330, 340 and so on.

Each of the remote communications adapters, regardless of whether it is connected to a modem, display or teletype, operates in the data receiving, data transmission and autonomous modes.

The operation of the adapters in these modes is controlled from the SM-3 or SM-4 complexes by a special service program through their program-address registers.

Integration of the remote communications adapter with data transmission apparatus (modems and signal conversion devices) is accomplished according to the requirements of the S2 junction (GOST 18145-72). The S2 junction (interface) is a 16-wire type. Any modem having an output to the S2 junction and which meets the requirements of speed can be used jointly with the remote communications adapter for working to the communications line. Examples of small computer system modems may be SM-8101 devices (modem-200, Hungarian Peoples Republic), SM-8102 (modem-1200, Hungarian Peoples Republic) or SM-8103 (modem-2400, Hungarian Peoples Republic).*

The remote communications adapter is integrated with the VT-340 display by means of a special four-wire interface containing two input and two output communications lines. The data to be transmitted and received are represented by two-pole current pulses with levels of -48 V, 20 mA for logic zero and +48 V, 20 mA for logic one.

The transmission range over a special line (TG-0.7 cable, R = 48 ohms/km and C = = 0.046 µF/km) is up to 10 km when working with a display.

The data can be transmitted on a line in the SEND and ONLINE modes controlled from the display keyboard. In the SEND mode, the contents of the screen (the buffer

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*A more complete list of the data transmission apparatus with output to the S2 interface and telegraph and telephone communications channels is given in [13].

memory of the display) are transmitted automatically to the line at the established data transmission rate and upon transmission to the ETX control character line for the last character of the screen, the display automatically converts to the ONLINE mode in which the data are simultaneously received from the keyboard and transmitted to the screen.

The remote communications adapter is integrated with the T-63 drum printer by two-wire physical lines. The type of transmitted and received signals is single-pole telegraph (TG) pulses; the parameters of the TG-line signals are: line voltage—+60 V $\pm$ 10 percent and nominal value of line current—40 mA. The data transmission rate is 50 and 100 bits/s. The transmission range over the physical line (type TG-0.7 cable, R = 48 ohms/km and C = 0.046 μF/km) is up to 10 km when working with a display.

The data transmitted over the line and received from the line are represented in MTK-2 code.

Each adapter contains four registers accessible to the service program from the common bus, by means of which the complex interacts with the data transmission apparatus and the communications lines:

the instruction and state register of the adapter part (receiver) $RKSp_M$ (address 77XXX0);

the data receiver register RDp_M (address 77XXX2);

the instruction and state register of the transmitting part of the adapter (transmitter) $RKSp_D$ (address 77XXX4);

the data transmitter register RDp_D (address 77XXX6). The symbols XXX are numbers from 561 to 617. The register addresses for the neutral remote communications adapter then begin at 775610, those for the first adapter begin at 775620 and so on and those for the 30th adapter begin at 776170.

The adapter control functions are mainly related to the instruction and state registers.

The structure of the instruction and state register of the receiving part of the adapter $RKSp_M$ and the functions of its individual digits are described in Table 3.7.

Similar information on the instruction and state register of the transmitting part of the adapter $RKSp_D$ is contained in Table 3.8.

The data receiver register consists of digits 0-7 and 12-15. Digits 8-11 are not used. Sequential information coming from an external device (modem and so on) is converted to a parallel code and written in the RDp_M. This information is retained in it until the next symbol is received from the communications line. The information bits are arranged in the eight bottom digits of the register (0-7).

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Table 3.7.

Digit	Name	Function
1	2	3
0	Read authorization	The punch tape is advanced in the teletype if this digit is present. It is set by program and is reset in the middle of the "start" bit upon entry of sequential data from an external device or a PODG signal. It is accessible only for writing
1	Connect data transmission apparatus (APD)	It is set by program when the data transmission apparatus must be connected to the communications lines (circuit 108.2 of S2 junction is excited). It is reset only by program. It is not reset by a PODG signal. It is accessible for reading and writing
2	Request for transmission	It is set by program when the data transmission apparatus must be converted to the transmission mode (circuit 105 of junction S2 is excited). It is reset by program or by a PODG signal. It is accessible for reading and writing
3	Secondary transmission	It is set by program as a notation that data must be transmitted a second time through the direct channel (a logic "1" is transmitted through circuit 118 of junction S2). It is reset by program or by a PODG signal. It is accessible for reading and writing
4	Not used	
5	Interrupt authorization from data transmission apparatus	Setting the digit to "1" authorizes interruption by digit 15 of the RKS_{PM}. It is reset by program and by the PODG signal. It is accessible for reading and writing
6	Receiver interrupt authorization	Setting of the digit to "1" authorizes interruption by digit 7 of the RKS_{PM}. It is reset by program and by a PODG signal. It is accessible for reading and writing
7	Data readiness	It is set if reception of the symbol is completed and can be transmitted to the common bus. It is reset during reading of the data receiver register RD_{PM} or by the PODG signal and also when digit 0 "Read authorization" is set to "1." It is accessible only for reading by program. If digit 7 of the RKS_{PM} is set, then an interruption occurs with the presence of digit 6 of the RKS_{PM}
8, 9	Not used	

[Table continued on following page]

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Table 3.7 [Continued from preceding page].

Digit	Name	Function
1		
10	Secondary reception	It is set if digit 3 of the RKS$_{PM}$ is set (circuit 119 of junction S2 is in the logic "1" state). It is reset by the PODG signal or upon resetting of circuit 109 of junction S2. It is accessible only for reading
11	Receiver is operating	It is set in the middle of the start bit of sequential data. It is reset with setting of digit 7 of the RKS$_{PM}$ or by the PODG signal. It can only be read
12	Detection of carrier frequency	It is set to "1" upon excitation of circuit 109 of junction S2. It is reset upon resetting of circuit 109. It can only be read by program. The digit is not flip-flop type
13	Data transmission apparatus is ready for transmission	It is set upon excitation of circuit 106 of junction S2. It is reset upon disappearance of circuit 106. It is read only by program. The digit is not flip-flop type
14	Call	It is set upon appearance of the signal in circuit 125 of junction S2. It is read only by program. The digit is not flip-flop type
15	Interruption from the data transmission apparatus	It is set in all cases if the digits of the RKS$_{PM}$ change its state (from "1" to "0" and from "0" to "1"): 10—"secondary reception," 12—"carrier frequency detection," 13—"data transmission apparatus is ready for transmission" and also upon conversion of digit 14—"call"—from "0" to "1." It is reset upon readout of the RKS$_{PM}$ or by a PODG signal. The presence of digit 15 causes an interruption if digit 5 of the RKS$_{PM}$ is set to "1." The given digit can only be read

Note. All digits of the RKS$_{PM}$ can be read simultaneously by program.

The four top digits of the register (12, 13, 14 and 15) are used for signalling about errors occurring during reception of messages:

digit 12—parity error. It is set if the received symbol has an incorrect control digit;

digit 13—format error. It is set if the received symbol did not have the required number of "Stop" bits;

digit 14—overflow error. It is set if the previously received symbol was not read before a new one was recieved, i.e., digit 7 of the RKS$_{PM}$ was not reset;

digit 15--error. It is set upon the appearance of one of the three errors given above.

Table 3.8.

Digit	Name	Function
0	Continuous blank	A low level (absence of information) is maintained at the sequential output of the transmitter with a set digit. It is reset by a PODG signal. It can be set and reset by program
1	Not used	
2	Autonomous mode	Setting of this digit means that the device is being converted to the preventive mode in which the sequential output of the transmitter is connected to the sequential input of the receiver and is disconnected from the output to the external device. It is reset by a PODG signal. The digit is accessible for reading and writing by program
3,4,5	Not used	
6	Transmitter interruption authorization	Setting the digit authorizes interruption from the transmitter with the presence of digit 7 of the RKS_{PD}. It is reset by a PODG signal. It is accessible for reading and writing by program
7	Transmitter readiness	It is set when a symbol can be written in the transmitter data register. It is read only by program. The PODG signal sets this digit to "1." It is reset when writing information in the transmitter data register
8-15	Not used	

The error digits written in the RD_{PM} are not reset by the PODG signal. The error digits are renewed only when the next symbol is received and the new state of the error digits is read upon access to the RD_{PM}.

The transmitter data register (RD_{PD}) is an eight-digit type (digits 0-7). If the symbol loaded into it for transmission to the line contains fewer than eight significant bits, it is shifted to the bottom digits of the register. The contents of the RD_{PD} register cannot be read by program.

Examples of designing small computer complexes using the systems unit of the remote communications adapter are presented in Figures 3.15 and 3.16.

Operation of the devices of the systems unit of the remote communications adapter in SM-3 and SM-4 complexes is supported by DIAMS (dialogue multiterminal system), OS RV [Real-time operating system] and STOD (remote data processing system).
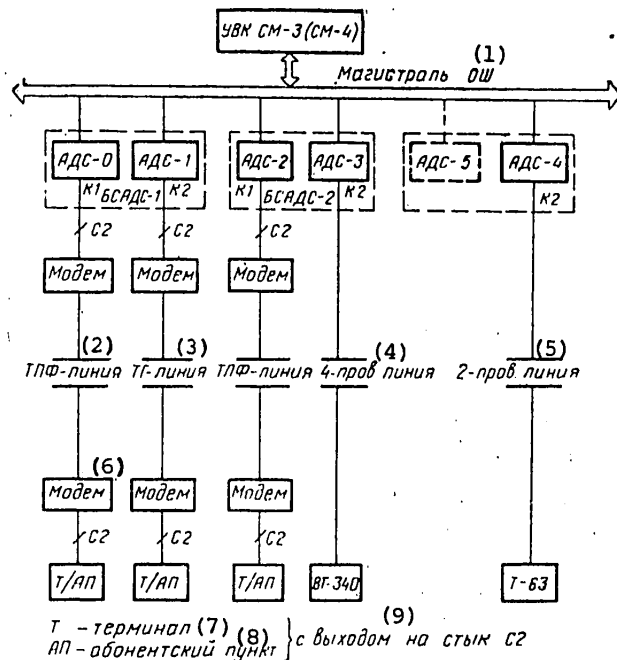
Figure 3.15. Example of Designing Small Computer Complex With Remote Terminals

Key:

1. Common bus mainline
2. Telephone line
3. Telegraph line
4. Four-wire line
5. Two-wire line

6. Modem
7. Terminal
8. AP-user terminal
9. With output to junction S2

3.7. The Arithmetic Expander

The arithmetic expander RA of the SM-3 is designed to increase the productivity of the SM-3 control computer complex; it can also be used in problem-oriented complexes and ASU, the basis of which are baseline or standard SM-3 complexes. The use of it in the SM-4 control computer complex is essentially possible, although there is no standard software for this application of it.

The SM-3 arithmetic expander provides apparatus realization of the number processing operations most frequently used in the programs, which include multiplication and division of numbers with fixed decimal and multiple arithmetic and logic shifts. Moreover, the SM-3 arithmetic expander can perform the normalization operation required in processing numbers with floating decimal and thus provides acceleration of the time of executing subroutines of processing numbers with floating decimal.

The arithmetic expander performs by apparatus (using the SM-3P processor) the enumerated operations more than an order faster than the processor by the program

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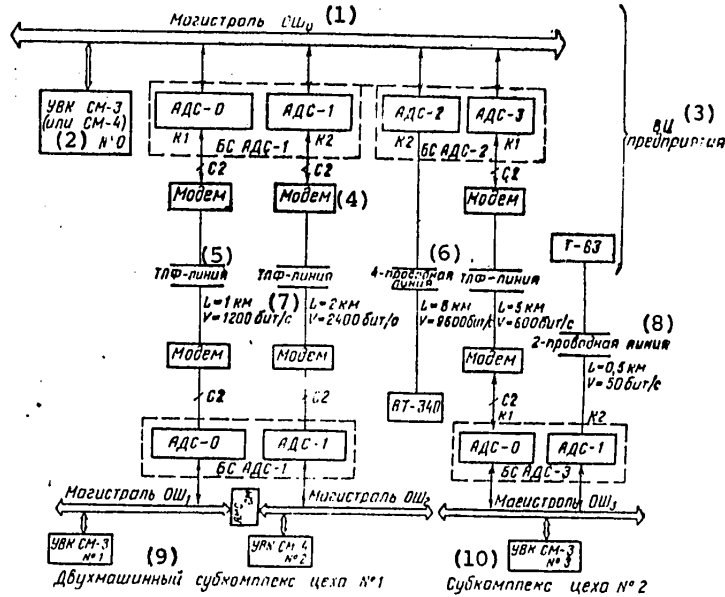
Figure 3.16. Example of Designing a Distributed Multimachine Complex With Remote Subcomplexes

1. Mainline	6. Four-wire line
2. SM-3 (or SM-4) control computer complex	7. Bit/s
3. Computer center of enterprise	8. Two-wire line
4. Modem	9. Two-machine subcomplex of shop No 1
5. Telephone line	10. Subcomplex of shop No 2

method. For example, the SM-3P processor expends only 400 microseconds to execute the multiplication operation by the subroutine, while this operation can be executed within no more than 25 microseconds when using the SM-3 arithmetic expander.

Performing the operation with access and decoding of the instruction address, which will be used for access of the result from this expander, can be integrated during programming of operations executed in the SM-3 arithmetic expander. This integration permits a reduction by a factor of almost 1.5 microseconds in the total time of executing the operation.

Provision of easy switching of the register address zone in the SM-3 arithmetic expander permits connection of up to two expanders simultaneously to a single SM-3 complex and even greater expansion of the functional capabilities of this complex.

The use of the SM-3 arithmetic expander in complexes and systems based on the SM-3 control computer complex permits solution of new, more complex problems. At the

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same time, some operating systems of the unified computer system cannot operate without the SM-3 arithmetic expander (for example, the DIAMS operating system).

The SM-3 arithmetic expander is connected directly to the common bus and is accordingly a peripheral device of the complex. Execution of the operation in the device is initiated upon transmission of operands (numbers) by fixed addresses of the storage registers and special operation registers by means of ordinary memory access instructions. The result of the operation is read from the registers by the same instructions; therefore, special operating codes are not required for the SM-3 arithmetic expander.

The central processor and the SM-3 arithmetic expander are interconnected through the common bus mainline. The following address zones are distinguished in the address file of the complex for possible connection of up to two devices: from 777300 through 777316 (the SM-3 version of the arithmetic expander) and from 777300 through 777316 and from 777320 through 777326 (the SM-3-1 version of the arithmetic expander).

The SM-3-1 arithmetic expander is two expanders installed in a unified structure and distinguished by the working zones of the addresses. Let us consider the addresses of the first arithmetic expander, since those of the second differ only by one in the fourth address digit. The SM-3 arithmetic expander is adjusted for the address zone 777320-777326 when a wire jumper is installed in the fourth digit of the address on a BE9456 circuit card. If this jumper is absent, the device is automatically adjusted to the main address zone 777300-777316.

The SM-3 arithmetic expander has the following specifications and indices of designation.

The interface for connecting the device is the small computer common bus. The natural load on the common bus is one load unit.

The digit capacity of the operands (whole numbers) to be processed is 8, 16, 24 and 32).

The implemented operations and the time of executing them (variation of values in the range of $\pm$ 10 percent is permitted) are 4.0 microseconds for multiplication (two 16-digit numbers with a 32-digit result), 4.5 microseconds for division (a 32-digit number by 16-digit number with a 16-digit quotient and a 16-digit remainder), up to 4.0 microseconds for an arithmetic or logic shift (a 32-digit number to the left or right by the number of digits given prior to the beginning of the operation) and up to 4.0 microseconds for normalization (a 32-digit operand with calculation of the number of shifts).

Note. The indicated values do not take into account the time for loading the operands into the device and for retrieving the result from it.

The type of control device is a rigidly commutated plus nanoprogram logic using electrically programmed semipermanent memory units of type K556RE4 (256 X 4 bits).

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The component base is TTL-IS and SIS of series K155, K131, K559 and other series compatible with them.

The electronics capacity (in arbitrary integrated circuit housings) is approximately 110.

The composition of the device is: SM-3 and SM-3-1 versions of the arithmetic expander have one plug-in chassis each, the SM-3 arithmetic expander has one each BE9456 and BE9457 component unit, while the SM-3-1 arithmetic expander has two of these units each. There are two types of printed-circuit cards each in both versions.

The design version is the small computer plug-in unit (four-digit with two-plug component units).

The overall dimensions of the device are 267 X 456 X 68 mm. The mass of the device is not more than 3.5 kg for the SM-3 arithmetic expander and not more than 4.7 kg for the SM-3-1 arithmetic expander.

The power supply voltage is +5 V $\pm$ 5 percent. The consumed power is not more than 20 watts for the SM-3 arithmetic expander and not more than 40 watts for the SM-3-1 arithmetic expander.

The efficiency checking device is the test of the SM-3 arithmetic expander on random numbers and the logic test of the SM-3 arithmetic expander.

The SM-3 arithmetic expander has no identifiers of the device based on the common bus since it can function only in the execution mode.

The arithmetic expander utilizes a standard pack of arithmetic operations which is contained in the following small computer operating systems: DOSS SM, DOS ARM, DIAMS, DOS RV, FOBOS and so on.

The device is constructed in the form of a standard plug-in unit (BK) whose structure is designed for installation in BAM [Autonomous installation unit] or BRS [Systems expansion unit] units. These units provide the device with power supply voltage and permit installation of it into the complex bay. Besides the SM-3 arithmetic expander, other devices can be installed (or are available) in the BAM (or BRS) unit; therefore, one should follow the excess output of the power supply source.

The SM-3 arithmetic expander contains three operand registers: storage (AK), multiplier-quotient register (MCh) and multiplier-divisor register (X). The AK and MCh registers are used in executing all operations in the device, while the X register is used only when performing multiplication and division. The device contains an eight-digit state register (RS) which contains information about the contents of the MCh and AK registers and about the course of executing the previous instruction, and a six-digit cycle counter (STs) used to count the operating cycles of the device. Writing to the RS and STs registers is performed only from the common bus mainline or from the output of the operating control unit of the device.

The AK and MCh registers have addresses on the common bus and can both be loaded and read from the mainline. During loading the AK and MCh registers are a single 32-digit register and the MCh register contains 16 bottom digits, while the AK register contains 16 top digits of the operand. Loading into this 32-digit register is possible both by words and by bytes. Loading a bottom word or byte causes the digits of the top word or higher bytes to be filled with an expanded symbol of information to be loaded. The third operand register X has no special address on the mainline and is loaded simultaneously with start of multiplication and division operations. Information cannot be read from this register from the common bus.

The cycle counter (STs) and the state register (RS) have the addresses of two adjacent bytes (bytes contained in a single word) and the cycle counter is the bottom byte of this word while the state register is the top byte. Writing of only the entire word is possible to these registers by their systems addresses, i.e., the cycle counter and state register simultaneously.

The common bus address is assigned to each operation performed by the device. Writing a word or bottom byte by this address forces the device to perform a given operation. The information transmitted during this writing is either used in performing the operation (this is one of the operands during multiplication or division and the number of shifts in the case of shifts) or is not used (during normalization).

The central processor loads the first operand in the MCh and AK registers. The following loading sequence is observed when unloading these registers: the bottom bytes are loaded first and the start of the operation is then begun.

A second multiplier is sent to the device by address 777306 to start the multiplication operation. In this case the first multiplier is in the MCh register. The contents of the AK register are disregarded. After the operation is executed, the result of multiplication is contained in the AK and MCh registers, while the bottom digits of the product are in the MCh register.

The division operation is started upon transfer of the divisor by address 777300. The contents of the AK and MCh (a 32-digit word) are divided by the divisor during the operation. The MCh register contains the quotient at the end of the operation and the AK register contains the remainder. The sign of the remainder always coincides with the sign of the dividend.

The arithmetic shift (logic shift) operation is started when the number of shifts is written by address 777316 (777314). In this case the sign of the number of shifts determines the direction of the shifts. When these operations are completed, the 32-digit contents of the AK and MCh registers are shifted by the corresponding number of digits.

The normalization operation is begun by transfer of any number by address 777312. During completion of this operation, the contents of the AK and MCh registers are shifted to the left until they become normalized. At the same time, the shift cycles are counted to the left in the cycle counter.

Table 3.9. Response of SM-3 Arithmetic Expander to Access by Register and
Operation Addresses

Operation Register	Common Bus Address	Common Bus Operations			
		Reading of Word	Writing of Word	Writing of Lowest Byte	Writing of Highest Byte
DIVISION	777300	Reading of zeroes	Writing and X, beginning of divisions	Writing and X, expansion of sign, beginning of division	No
Accumulator Register (AK)	777302	Reading of AK	Writing to AK	Writing to AK, expansion of sign	Writing to AK
Multiplier-quotient Register (MCh)	777304	Reading of MCh	Writing to MCh, expansion of sign in AK	Writing to MCh, expansion of sign in highest byte of MCh and AK	Writing to MCh, expansion of sign in AK
MULTIPLI-CATION	777306	Reading of zeroes	Writing to X, beginning of multiplication	Writing to X, expansion of sign, beginning of multiplication	No
Cycle counter (STs), register of state (RS)	777310	Reading of STs and RS	Writing of STs and digits 0, 6 and 7 of RS	No	No
NORMAL-IZATION	777312	Reading of STs	Beginning of normalization	Beginning of normalization	No
LOGIC SHIFT	777314	Reading of zeroes	Writing to STs, beginning of logic shift	Writing to STs, beginning of logic shift	No
ARITHMETIC SHIFT	777316	Reading of zeroes	Writing to STs, beginning of arithmetic shift	Writing to STs, beginning of arithmetic shift	No

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The response of the SM-3 arithmetic expander to access from the common bus by the register and operation address is illustrated by Table 3.9.

The device blocks communications with the common bus mainline and does not respond to requests from other devices, including those from the processor, after any operation has been started. After the operation has been completed, the SM-3 arithmetic expander restores communications with the complex and again responds to requests from the processor. Because of this, reading of the intermediate result of the operation is blocked and the information read is always the final result of the last operation.

Table 3.10. Conditions for Formation of State Register Digits of SM-3 Arithmetic Expander

Digit of Register	Significance of Digit
0	During shifts the digit contains the last bit coming from the AK and MCh registers
1	The digit is equal to "1" if each digit of the AK register is equal to the highest order of the MCh register, i.e., the numbers in the AK and MCh registers have the accuracy (length) to one word
2	The digit is equal to "1" if the AK and MCh registers contain all zeros
3	The digit is equal to "1" if the contents of the MCh register is equal to zero
4	The digit is equal to "1" if the contents of the AK register are equal to zero
5	The digit is equal to "1" if the contents of the AK register are ones in all its digits
6	During division and in the absence of overflow, the digit is set at "1" if the quotient is negative. If there is overflow, the digit is equal to "1" if the dividend is negative. When performing other operations, digit 6 is equal to the highest order of the AK register.
7	The digit together with digit 6 is used to indicate overflow conditions: if the values of these digits coincide, there is no overflow, and if the values of the digits are different, there is overflow.

When operations are being performed in the SM-3 arithmetic expander, the register of state (RS) is loaded with information about the operands to be processed and the result obtained. This information is subsequently used by the central processor to control calculations. The conditions for filling individual digits of the register of state when executing operations are presented in Table 3.10.

The structure of the SM-3 complex using arithmetic expanders is shown in Figure 3.17.

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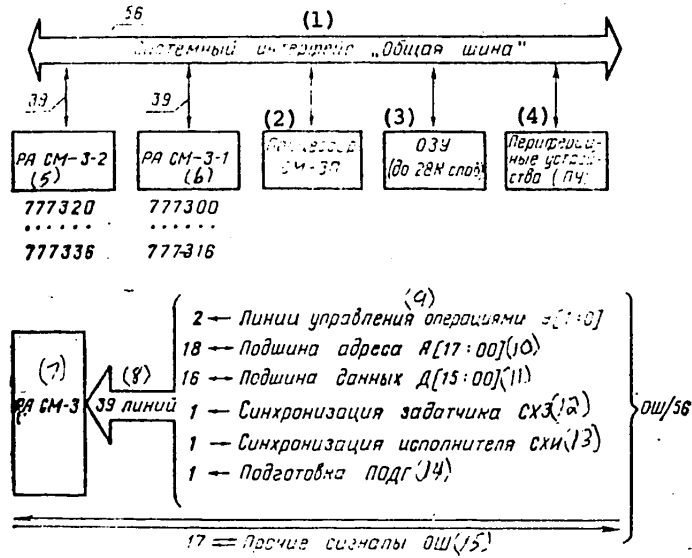
Figure 3.17. Structure of SM-3 Complex With Use of Arithmetic Expanders

Key:
1. Common bus systems interface
2. SM-3P processor
3. Internal storage device (up to 28K words)
4. Peripheral devices (PU)
5. SM-3-2 arithmetic expander
6. SM-3-1 arithmetic expander
7. SM-3 arithmetic expander
8. 39 lines
9. Operation control lines [1:10]
10. Address sub-bus A [17:00]
11. Data sub-bus D [15:00]
12. Controller synchronization SKhZ
13. Executor synchronization SKhI
14. PODG preparation
15. Miscellaneous signals of common bus

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SOFTWARE OF THE INTERNATIONAL SMALL COMPUTER SYSTEM

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[Text] 4.1. The Composition of Software

The variety of areas of application, mass production and wide range of peripheral equipment (storage and terminal devices and devices for communicating with the facility) predetermine the main requirement on software--problems orientation.

The software of the international small computer system is constructed as the aggregate of operating systems and applied program packs different in their functional capabilities.

Nine operating systems, 10 applied program packs and also a test-monitor system that provides different modes of testing computer complexes during production and operation have been developed for the international small computer system.

The specific orientation of computer complexes is determined to a significant degree in each individual case by the applied program facilities of the user, but this orientation is considerably simplified due to the wide nomenclature of basic software for the international small computer system.

The operating systems of the SM-3 and SM-4 control computer complexes comprise three classes by their designation: general-purpose operating systems, real-time operating systems and time-sharing operating systems.

General-purpose operating systems include the general-purpose papertape operating system (PLOS SM), the dialogue programming system (DS SM) and the disk operating system (DOS SM). They provide execution of the basic functions related to organization and control of the calculating process and preparation, debugging and fulfillment of user programs and control of data input-output and program procedures.

Real-time operating systems are the most representative. They include the real-time papertape operating system (PLOS RV), the basic real-time background-operating system (FOBOS), the multiprogramming real-time disk operating system (DOS RV) and the real-time operating system (OS RV).

The operating systems of this class include monitor devices that ensure simultaneous completion of many real-time problems. Real-time systems make it possible to establish the time the problems are in the system and to interrupt some programs by others depending on the ratio of the their priorities.

Time-sharing operating systems are represented by the multiterminal time-sharing dialogue operating system (DIAMS) and the time-sharing disk operating system (DOS RVR). These systems provide sharing of the resources of the complex for many users (including remote users).

The following are typical for systems of this class:

sharing of devices (the capability for many users to gain access to the same devices of the complex--processor, storage devices and input-output devices;

sharing of files (the possibility of remote access of the user to the files located in the complex where each user can create several files belonging to him). Moreover, the system may contained collective-use files;

access authorization (making available devices to the user to protect the data and programs belonging to him against unauthorized access and password access to the system);

dialogue programming languages;

expanded composition of remote data processing software compared to the operating systems of other classes.

4.2. The Structure and Main Characteristics of Operating Systems

With all the variety of the properties and capabilities of the operating systems of the SM-3 and SM-4 control computer complexes, they are joined by a single very important property--the modular principle of design.

Let us consider the programming modules that are the main components of the operating systems.

The "Monitor" module is the nucleus of the operating systems. Its main functions are access to systems and user files, data transmission during input-output operations and loading, starting and restarting of user programs.

The monitor stores, processes and issues upon request such information as the date and time of day and the status of the system.

Communications with the monitor can be gained both by program requests and requests assembled on the keyboard of the operator's console.

The affiliation of an operating system to one or another class is primarily reflected in the composition of the monitor functions. Thus, the set of monitor functions in general-purpose operating systems is limited and is relatively complete only in disk operating systems. The monitor functions in the general-purpose papertape operating system reduced to control of input-output operations.

The monitor in real-time operating systems also performs the functions of dispatcher that provides starting and simultaneous completion of several real-time problems, accounting for the time that they are in the system and interrupting them by other programs as a function of established (or dynamically redistributed as in real-time operating systems) priorities.

The input-output supervisor module is typical for time-sharing systems in which the monitor is released from realization of input-output procedures. In these systems physical realization of input-output procedures is accomplished by input-output supervisor programming devices that offer access to the user with requirements to execute these procedures at the logic level. These modules are used in time-sharing systems (DIAMS and DOS RVR).

The problem control module is used in time-sharing systems. The functions of this module include distribution of resources for problems arising during collective access of remote users to the resources of the control computer complex. The module programs monitor the time the problem is in the system and ensure removal of problems whose time given during generation has expired.

The time parameters for each of the problems monitored and controlled by the system are given upon generation.

The problem planner module is used only in resource time-sharing systems (DOS RVR) and provides distribution of resources among independently existing and serviced problems in a collective-use system.

The file control program module provides organization and access to files for the user's programs. The functions of this module permit users:

to gain direct and subsequent access (depending on the operating system) to files distributed in different memory and data input-output devices;

to shift files between devices of the control computer complex (to enter files from data input devices, to issue files to data output devices, to rewrite data from one type of carrier to another and so on);

to duplicate files;

to monitor the format of files.

The functions of this module in the real-time operating system are supplemented by (direct and inverse) conversion of the file formats of the DOS SM and FOBOS for use in the system and vice versa.

The file control module in the DIAMS system is supplemented by devices that provide data conversion to the formats used in the operating systems of the unified computer system and reverse conversion. This makes it possible to connect systems operating under the control of the DIAMS to different models of the unified computer system at the machine carrier (magnetic tape) level.

The data base supervisor module is typical for the multiterminal dialogue system DIAMS that provides devices for creation, management and search in data bases with hierarchical structure for many users. The software of this module provides access to data bases at the logic level (i.e., connection of the physical data bases to the user programs at the logic access level--symbolic names). The programs of this module provide access to data at the physical level, including control of disk and tape storage devices, freeing the user of the need to distribute data on external carriers.

The generation equipment module makes it possible to adjust the operating systems in all the systems of teh SM-3 and SM-4 control computer complexes during generation to a specific composition of the hardware maintained and the functions performed. During generation, the programs of this module provide inclusion of the required programs from the library of systems program in the system nucleus, which makes it possible to create a version of an operating system oriented toward control of a specific hardware configuration of the computer complex that performs the functions given during generation.

The text editor module provides the user with the capability of creating and correcting the initial files (created in the initial language) with subsequent output of the edited files to an external carrier (for example, to a punch tape).

The composition module transforms the facility modules obtained as a result of relay and also the modules removed from the systems program library to a unified connected module.

The composer provides conversion of relative addresses to absolute physical addresses of the memory using global symbols indicated in the programs to be figured. Thus, the composition program transforms a facility module to a loading module ready for loading into the memory and execution.

The librarian module provides creation, management and printing of the contents of the library that contains one or more facility modules. The presence of a librarian program provides the user with the following advantages: it eliminates individual entries for each facility module in the user's catalogue, it accelerates the process of searching for the necessary modules and configuration by using the composition program and it provides standard construction and the capability of correction of frequently used programs.

The debugger module permits the user to debug the composed programs and to perform the following operations: starting of all or part of the program with indication of a stop at the required point of the program, inspection and changing of the contents of any memory cell, searching in the program text for the given binary combinations and calculation of the shift for binary addresses.

Table 4.1. Main Characteristics of Operating Systems of SM-3 and SM-4 Control Computer Complex

Characteristics of Operating System	DS SM	PLOS SM	DOS SM	PLOS RV	FOBOS	DOS RV	OC RV	DIAMS	DOS RVR
1	2	3	4	5	6	7	8	9	10
Type of control computer complex	SM-3 SM-4	SM-3, SM-4							
System carrier	paper-tape	paper-tape	magnetic disk	paper-tape	magnetic disk	magnetic disk	magnetic disk	magnetic disk	magnetic disk
Minimum capacity of internal storage, K words	8	8	16	12	16	16	16	16	40
Maximum capacity of internal storage, K words	28	28	28	28	28	28	124	124	124
Servicing capability	one-user	one-user	multi-user	one-user	one-user	multi-user	multi-user	multi-user	multi-user
Presence of multi-program operation	No	No	No	Yes	Yes	Yes	Yes	Yes	Yes
Number of programs executed simultaneously	--	--	--	127+1 background	1 operational + +1 background ground	127+1 background	250 priority levels	40	24
Presence of remote processing devices	No	No	No	Yes	No	Yes	Yes	Yes	Yes
Number of connected terminals	--	--	--	8	--	8	32	64	24
Programming language	Dialogue DS	Assembler	Macro-Assembler	Assembler	Macro-Assembler, FOR-TRAN-4	Assembler	Macro-Assembler, FOR-TRAN-4	Dialogue, DIAMS	Basic-Plus

*Only with the presence of an arithmetic expander in the SM-3.

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The essential components of the operating systems of the SM-3 and SM-4 control computer complex are the program automation devices that include devices for interpretation and (or) translation from the input languages. The characteristic feature of the SM-3 and SM-4 software is the extensive use of dialogue languages (DS SM, DIAMS and BASIC-PLUS), which predetermines the presence of interpreting type translators (interpreters) from these languages in the corresponding operating systems. In this case, like the DS SM, the interpreter for these systems is essentially the monitor system that ensures starting and fulfillment of the programs prepared in the initial language.

The advantage of interpreters is immediate execution of each instruction after its entry from the operator's console (which does not exclude preparation of the program for subsequent execution in the pack processing mode).

The most widespread programming languages in SM-3 and SM-4 operating systems are Assembler, Macroassembler and FORTRAN-4.

Translators provide translation of programs written in these languages to programs in machine codes (facility modules), syntax monitoring of the translated programs and printing (issue of a listing) of the program in the initial language with indication of detected errors (flags that characterize the type of detected error). If necessary the translator provides transfer of the facility module to papertape for subsequent loading of it while the translated program listing provides transfer to the printer.

The main characteristics of the operating systems of SM-3 and SM-4 control computer complexes are presented in Table 4.1. Practically all the operating systems can be used in computer complexes designed on the basis of both the SM-3 and SM-4 processor. An exception are the DIAMS operating systems, whose use in the SM-3 control computer complex requires the compulsory presence of an arithmetic expander and a DOS RVR that functions only in the SM-4 control computer complex.

One should bear in mind in this case that all the remaining operating systems (except the real-time operating system), being installed in the SM-4 control computer complex, cannot utilize the addressable memory expansion hardware. The real-time operating system can be generated in a version that does not use a memory dispatcher and can operate at the minimum configuration of the SM-3 and SM-4 control computer complexes.

The indicator of the servicing capability (see Table 4.1) determines the independent use of the operating system installed in the SM-3 or SM-4 control computer complex by many users (starting of programs belonging to different users and creation of user data files).

Multiuser systems in this sense are DOS RV, OS RV, DIAMS and DOS RVR. It should be noted that the DOS SM provides creation and management of program and data libraries for many users.

The presence of remote data processing devices determines the capability of the remote user's access to resources and to the capabilities of the operating system.

At the same time, despite the absence of remote processing devices in the DOS SM, it does contain software that provides connection of additional terminals. It should also be noted that the DIAMS system provides not only connection of remote users but also creation of a homogeneous computer system with up to 15 terminals, offering the capability of access to each of the users of the terminal of the network to the data and devices distributed in this network.

4.3. Designation and Areas of Application of Operating Systems

The dialogue programming system (DS SM) is a dialogue language and interpreter program from this language intended for preparation, debugging and execution of user programs written in the input dialogue language and for executing the user's direct directives.

The areas of application of the dialogue programming system are automation of scientific experiment, scientific-technical and economic calculations and the sphere of teaching.

The DS SM permits the user to work in dialogue and program modes and provides execution of arithmetic operations on numbers represented in formats with fixed and floating decimal and execution of standard functions, offers service devices for program preparation and debugging and accomplishes input-output of numerical files and programs.

The minimum capacity of internal storage required for working with the DS SM is 8K words. The capacity of the memory occupied by the program interpreter itself fluctuates from 2 to 8K words. The remaining memory is at the user's disposal.

The dialogue programming system performs the following functions:

preparation of user programs in DS SM input language;

debugging of user programs, which includes editing of the initial text, output of all or part of the edited program to the input-output device and automatic removal of user error codes;

routing--control of program text printout;

loading user programs from the punchtape into the internal storage;

output of user programs completely or in parts onto punchtape or printing of text.

The dialogue programming system is delivered on a papertape carrier. The following devices are required for functioning of the dialogue programming device: an SM-3P or SM-4P processor, internal storage device with capacity of not less than 8K words, papertape input-output device and alphanumeric video terminal based on the Videoton-340 device.

The dialogue programming system provides connection of additional devices: a printer with keyboard and an alphanumeric sequential printer. The dialogue programming system offers the user devices for using other devices from the international small computer nomenclature, including devices for communicating with the facility (USO).

The general-purpose papertape operating system (PLOS SM) is a complex of programs designed for preparation, debugging and execution of user programs in Assembler language in the single-program mode and also for preparation of debugging user programs for the real-time papertape operating system (PLOS RV). The area of application of the PLOS are scientific and technical calculations, simple control systems and automation of scientific experiment.

All the programs in the PLOS system are on punchtape. Program and data input-output are executed through an input-output device from punchtape; the user maintains a dialogue with the system programs by means of instructions entered from the terminal keyboard.

A minimum hardware complex, which includes an SM-3P (SM-4P) processor, internal storage device with capacity of 8K words and an input-output papertape device, are required for the system to operate.

The PLOS system can operate with a type SM-6302 alphanumeric printer.

The disk operating system (DOS SM) is a general-purpose system designed to develop, debug and execute programs in the pack and dialogue modes.

The DOS provides the following capabilities in dialogue and pack modes: arrangement of system and user files on disks using multilevel catalogues, duplication, printout and file security, translation, composition and debugging of programs written in FORTRAN-4 or Macroassembler language, editing of symbol files and creationof libraries of facility and loading modules.

The DOS contains a set of control programs and is designed on the modular principle and has a set of processing programs for file transfer from device to device and for library management.

The minimum configuration of hardware for the DOS SM is an SM-3P or SM-4P processor, internal storage device with capacity of 16K words, a magnetic disk store, papertape input-output device, alphanumeric printer and alphanumeric video terminal.

An internal storage device with capacity up to 28K words, a timer, magnetic tape stores, magnetic disk stores with fixed heads or plug-in type, a punch card input device, additional terminals and a hardware loader may also be connected.

The real-time papertape operating system (PLOS RV) is designed to solve a wide range of problems arising in systems for automation of scientific experiments and in systems for control of industrial facilities.

The PLOS RV provides a multiprogram mode on a priority basis using the time-planning mechanism of problem solving, provides operator communications with the

control system and other important functions required for operation of the control computer complex in the real-time multiprogram mode. The PLOS RV is an operating system resident in the internal storage that occupies the region of internal storage with capacity of 8K words. The PLOS RV system includes devices that carry out input-output operations which provide independence of the problem from external devices and which offers them the capability of redundancy and of joint use of external devices and also of being connected to alternative devices.

The PLOS RV is provided with devices for development of software and utilizes systems programs: a text editor, a movable assembler and composer which are formulated as background problems (these background problems require an additional internal storage capacity of 4-8K words). The loading modules obtained as a result of operation of the composer systems program are loaded by the systems loader through the papertape input-output device.

The operator has at his disposal a wide range of systems instructions transmitted through the console. These instructions are intended for operational communication of the user with the system and problems. The PLOS RV may maintain up to eight additional terminals.

The PLOS RV system offers the following problem-planning capabilities:

one-time execution of real-time problems, the total number of which does not exceed 127;

execution of a single background problem (this problem may be both a user and systems type);

execution of problems on four priority program levels;

initiation of problems at the operator's request, program request and by interruption at the request from the timer;

the length of problem execution at each priority level is controlled by the tracking timer, which reduces the priority of problem execution if the time of execution does not exceed the time interval given for this level. The duration of the problem is unlimited at the lowest level.

Real-time problems can be written in Assembler language.

The minimum configuration of hardware supported by the PLOS RV system includes an SM-3P or SM-4P processor, internal storage device with capacity of 16K words, a timer, papertape input-output device and alphanumeric video terminal.

An alphanumeric printer, additional internal storage units with capacity up to 28K words, analog-digital signal input-output devices, eight terminals and a magnetic disk store (without working with files) may also be used. The basic real-time background-operating system (FOBOS) is designed to create specific versions of the operating systems of problem-oriented computer complexes based on the SM-3P or SM-4P processor. The areas of application of the system are automation of laboratory experiments, control of tests and solution of scientific-technical and other problems of a calculating nature.

The FOBOS operating system is a real-time system and is characterized by minimum response time to external action compared to other real-time disk operating systems. The resonant part of the FOBOS supervisor occupies a minimum memory (4K words), offering the remaining part of the internal storage for operation of the real-time operating program in combination with execution of another program or a program pack in the background mode.

The supervisor and set of driver programs service a wide range of external devices of the international small computer system.

A memory with capacity of 16-28K words is required for operation of the FOBOS and it offers the user a flexible real-time input-output queueing system. The system provides three modifications of input-output operations:

synchronous input-output in which control is not returned to the requesting program upon completion of the input-output operation;

asynchronous input-output in which the request for input-output is established in turn for servicing and control is returned immediately to the requesting program;

input-output with the event in which the request for input-output is established in turn for servicing and control is returned to the requesting program. The main program is interrupted upon completion of the input-output operation and control is transferred to the completion program upon output from which control is returned to the requesting program.

The FOBOS offers the capability of working simultaneously with a large number of external devices (up to 256).

The system permits users to prepare programs in Macroassembler, FORTRAN-4 and DIASP languages.

If nonstandard external devices are connected to the international small computer system, there is the capability of expanding the set of drivers for servicing these devices.

Such functions as diagnosis of error situations, management of program operation, processing of interruptions, organization of input-output and maintaining a dialogue with the operator's console are managed by the FOBOS monitor.

Working with user and systems programs is usually accomplished in the interactive mode from the console terminal.

A special pack monitor that permits one to combine several programs subject to execution in the international small computer system into a single packet and to process the packet automatically is included in the FOBOS for more effective use of computer resources when working in the background mode.

Users have access to the monitor through special call-ups from the console or program requests from the user programs.

The auxiliary programs of the FOBOS perform the following functions:

comparison of texts (sequential character comparison of two initial texts and removal of all differences between them to the output device);

file conversion (the capability of exchanging files for different operating systems;

code variation (making slight changes in the memory copy files);

changing the facility modules (capability of correction and restoration of facility modules);

printout (printout of a file or parts of it on a printer in one of the following formats: in octal code, word by word, byte by byte and in internal machine code).

The minimum configuration of the hardware is an SM-3P or SM-4P processor, alphanumeric video terminal, internal storage with capacity of not less than 16K words, a timer, magnetic disk stores and papertape input-output device.

An internal storage device with capacity up to 28K words, an alphanumeric printer, a punchcard reader, additional magnetic disk stores (including floppy disk stores) and magnetic tape stores may also be connected.

The real-time disk operating system (DOS RV) is a multiprogram system with fixed number of priority levels designed on the modular principle.

It is designed for creation of systems for automation of scientific research and planning-design work on the basis of the SM-3 and SM-4 control computer complexes.

The DOS RV provides the multiprogram mode of real-time problem execution on a priority basis using the time-planning mechanism of problem solving, communication of the operator with the system and other functions required for operational work of the SM-3 and SM-4 control computer complexes in the multiprogram real-time mode.

The DOS RV is an operating system resident in the internal storage; the residence of the system occupies an area of the internal memory with capacity of 8K words.

The programs carried out under the control of the DOS RV can be written in FORTRAN-4 language expanded by real-time operating devices. Problems written in FORTRAN-4 language are carried out in the DOS RV with preliminary translation and debugging in the DOS SM.

The real-time disk operating system is compatible with the disk operating system at the level of input-output program requests, formats of loading and facility modules and disk file structure.

Devices for achieving versions of the system corresponding to a specific configuration of the SM-3 and SM-4 control computer complexes are provided in the DOS RV and there are also instructions for development of driver programs for additionally connected devices.

The real-time disk operating system has such devices as a text editor, assembler and composer formulated as background problems for program development. The loading modules achieved as a result of operation of the Composer systems program are loaded by the systems loader through the papertape input-output device. If the loading module is prepared in the general-purpose disk operating system, it can be loaded into the memory from the disk by the systems loader of the real-time disk operating system.

The real-time disk operating system has a set of systems instructions transmitted through the console of the console terminal for operator communication with the system and problems.

The real-time disk operating system provides independence of external devices for problems and offers the capability of redundancy and joint use of external devices and also permits switching to alternative devices.

The real-time disk operating system provides the following capabilities:

concurrent real-time execution of a set of problems on a priority basis;

execution of a single background problem (translation from the assembler, editing and composition of programs;

execution of problems at four-program priority levels.

The problems can be initiated by the operator's instructions, by program request and interruption and by request from the timer.

The length of problem solving at each priority level is determined during generation of the system.

If the problem-solving time exceeds a given time interval for this priority level, the problem-solving priority is lowered. The problem-solving time is unlimited at the lowest level.

The main features of the real-time disk operating system are:

multiprogramming;

priority dispatching and combining it with time-quantification dispatching;

providing capabilities of working with files created under control of the the disk operating system;

the possibility of loading problems from disk and from punchtape;

restoration after power failure;

the possibility of including problems in the system during generation of the system;

the possibility of organizing work with additional external devices;

independence of input-output devices;

alternative devices.

The use of the real-time disk operating system envisions the compulsory presence of a general-purpose disk operating system in the control computer complex as a production system. This is determined by the fact that the control system of the real-time disk operating system permits the user to work with continuous files from a single catalogue previously arranged on the carrier by the general-purpose disk operating system. The user's problems under control of the real-time disk operating system can be summoned from the disk into the internal storage by means of operator instructions.

All the servicing programs of the real-time disk operating system are loaded from punchtape and are recorded on punchtape.

The devices of the real-time disk operating system provide configuration and execution of programs written in FORTRAN-4 language, but they should be previously translated by means of the translator of the general-purpose disk operating system.

The minimum configuration of the equipment is an SM-3P or SM-4P processor, internal storage device with capacity of not less than 16K words, a timer, console terminal, disk storage device, papertape input-output device and initial loader.

The auxiliary devices are an internal storage with capacity up to 28K words, an alphanumeric printer, magnetic disk store with fixed heads and eight terminals.

Any user terminal can be designated during generation of the real-time disk operating system as a console type and can be used for entering operator instructions.

The real-time disk operating system offers the capability of the system working in a configuration with additional standard and nonstandard external devices by connecting the drivers of these devices to the real-time disk operating system during generation.

The real-time operating system (OS RV) is a disk system that provides solution of a wide range of control problems in real-time.

The real-time operating system is designed to work with different equipment. Versions of the system are generated as a function of the application of the system: from small systems for laboratory investigations to large multiuser processing and control systems.

The real-time operating system is oriented toward disks and utilizes them both to maintain the system and system files and as the main data carrier. Creation of a general file system, temporary unloading of problems from the internal storage, rapid initiation of problems and working with duplications are possible due to this use of the disk.

The real-time operating system provides a multiprogram real-time mode and sharing of system resources on the basis of priorities.

Parallel execution of many problems in the real-time mode is provided due to priority dispatching, division of the memory into sections, temporary unloading of problems to a disk and operational interference of users from their own terminals during execution of problems.

Loading of problems into the memory and temporary unloading of problems onto a disk during execution are carried out during a single access to the disk, which considerably increases the speed of the system.

The real-time operating system provides servicing of many terminals and any user terminal can be used as an instruction terminal and start and stop instructions, changes of the problem and instructions to set certain system parameters can be entered from it.

The real-time operating system provides execution of both real-time and background problems. Problems are programmed for the real-time operating system in Macroassembler and FORTRAN-4 languages.

The main components of the real-time operating system provide:

multiprogramming;

priority dispatching and combination of it with time-quantification dispatching;

temporary unloading of problems onto a disk;

outlets from synchronous and asynchronous interruptions;

restoration upon power failure;

dynamic memory distribution;

division of the memory into sections controlled by the system or the user;

automatic sealing of the memory;

broad capabilities of working with the file system of the real-time operating system on disks of various types and on magnetic tapes;

conversion of files in DOS and FOBOS formats to the file structure format of the real-time operating system and vice versa;

working with resident shared libraries of modules and generaly data fields;

broad interaction of problems;

high reactivity of problem startup;

dynamic reconfiguration of external devices;

independence of input-output from external devices;

multiterminal operation;

dynamic loading and unloading of problems on disks;

a programming system based on translators from real-time Macroassembler and FORTRAN-4 languages;

working with libraries of macrodefinitions and facility modules;

dialogue and packet editing;

broad variable set of operator instructions.

The real-time operating system requires the presence of the following equipment: a central processor (SM-3P or SM-4P), alphanumeric video terminal, initial equipment loader, internal storage device (with capacity of 16K or 24K words as a function of the type of processor), a plug-in type magnetic disk and a timer.

An arithmetic expander, floating arithmetic equipment and memory dispatcher may also be installed.

The memory dispatcher equipment (DP) permits expansion of the program addressing of internal storage from 28K to 124K words and also provides equipment security of the memory. An internal storage with capacity of 24K words is required for versions of the real-time operating system that utilize memory dispatcher equipment (OS RV with DP). A real-time operating system with memory dispatcher equipment supports the work of many users in configurations of the SM-4 control computer complex with internal storage capacity up to 124K words. Versions of the real-time operating system that do not utilize the capabilities of a memory dispatcher permit configuration of the equipment of the complex with the SM-3P or SM-4P processor with internal storage capacity from 16K to 28K words.

The real-time operating system permits one to expand the configuration of the computer system with auxiliary devices connected to a common bus (floppy disks, disks with fixed heads, remote communications adapters, papertape input-output device, symbolic information input and display devices and terminals) and also by other devices from the nomenclature of international small computer system connected to a common bus.

The multiterminal disk dialogue system for solving information problems (DIAMS) is oriented toward control of data bases and toward solution of information-logic problems on disk configurations of the control computer complex based on SM-3P and SM-4P processors.

The DIAMS is used in automated operational control systems, scientific experiment control systems, economic data processing systems and in other systems where data

gathering, storage and processing are required in the mode of collective access to the data bases of many users with different terminals, including remote terminals.

The DIAMS offers users a wide range of capabilities, including:

multiprogram mode of problem solving;

working in the dialogue and program modes;

creation and management of data bases of tree-like hierarchical structure on disks;

simple access to a wide range of external devices included in the nomenclature of hardware of the international small computer system;

development, debugging and execution of programs in a high-level dialogue language;

processing of line data;

simultaneous access to the data base of many users with different terminals, including remote terminals;

authorization of access to user programs and data;

interrelation between user problems;

generation of versions of the system as a specific configuration of hardware and given functions;

operational modification of system configuration;

diagnostic monitoring of errors during operation of both system and user programs.

The DIAMS system is located completely in the internal storage and occupies a variable capacity (from 22K to 48K bytes) depending on the functions selected during generation and depending on the hardware configuration.

The DIAMS offers the user a high-level dialogue programming language oriented toward processing line data of variable length, numerical information and logic variables. The language contains a set of operations and functions: operations on lines (comparison, concatenation, checking by specimen, checking of inclusion and tracking, line conversion and so on), arithmetic operations on numbers with fixed and floating decimal, Boolean digit operations and also a set of input-output, control, editing and debugging instructions.

The DIAMS is designed on the modular principle and consists of an internal storage and applied program pack.

The operating system consists of a system dispatcher, input-output monitor and data base interpreter and supervisor.

The system dispatcher organizes the time-sharing mode and provides multiprogram operation of user problems. Time is shared by utilizing the principles of time intervals and priority dispatching. The input-output monitor controls the peripheral devices and creates terminal-independent conditions in which the applied program can be executed with any terminal. The interpreter interprets the input language, authorizes access to the program and data and programs from the terminals in dialogue language. The data base supervisor provides logic display of the data base to a physical storage medium and carries out physical and logic control of disk stores and symbolic access to data. The data base has a tree-like hierarchical structure. Any element within the tree may contain data in the form of a number, line value and/or indicator to a lower level. The data can be stored at any level. In this case the physical memory is not allocated in the structure for specific missing data. No restrictions of any kind are placed on the number of hierarchical levels. The total maximum capacity of the data bases is 200 Mbytes.

Besides data, systems and user programs are stored on disks.

Along with tree-like structures, the system can maintain sequential files on given areas of the disks. The user may superimpose any of his own file structure onto these areas.

The applied program pack contains systems programs that perform the functions required for the system administrator and library programs accessible to all users. All the pack programs are written in input language.

The applied program pack performs a number of service functions such as sending messages to given terminals, gathering and printout of statistics on errors in the system, establishing the date in the system and reporting the date to the input-output devices, restoration and maintenance of files, following the structure of data bases, starting and disconnecting the system, generation and initiation of the system, testing the system and reporting the status and functioning of the system.

The following minimum set of hardware is required to support the functioning of the DIAMS: an SM-4P processor (or SM-3P processor with arithmetic expander, internal storage with capacity of 16K words (simultaneous work of two users is provided in this case), a magnetic disk store with fixed heads or plug-in type, a magnetic tape store, timer, papertape input-output device, alphanumeric video terminal and alphanumeric printer.

The internal storage can be expanded to 124K words for the SM-4P (work of up to 40 users and connection of up to 641 terminals are provided in this case) and up to 28K words for the SM-3P (up to 16 users).

The system supports the operation of up to eight interchangeable disks or disks with fixed heads, up to four magnetic tape or floppy disk stores, up to four alphanumeric printers and up to 64 alphanumeric terminals.

Data transmission equipment (up to four remote communications adapters) is used to connect remote terminals.

The resource time-sharing disk operating system (DOS RVR) is used to prepare, debug and execute user programs.

The areas of application of the system are automated scientific experiment control systems, operational control systems, teaching systems and systems for solving scientific and engineering problems.

The programming language in the DOS RVR is Basic-plus language, which is a high-level dialogue language. The language has a wide range of standard functions for working with line data. A powerful facility of the language is the presence of matrix operations (elementary matrix operations and matrix functions). The language has a set of service instructions that control the system resources. A wide range of problems can be solved by using the Basic-plus language.

The DOS RVR permits simultaneous execution of the problems of a large number of users (up to 24). Sequential and direct access to the magnetic disk files is permitted with simultaneous work of users.

The user can designate the devices, including terminals, in operational mode for information input-output. The system carries out multiproblem work in the dialogue mode with time-sharing and ensures data security and also supports work with remote terminals by telephone or telegraph communications lines.

The minimum hardware configuration for operation of the DOS RVR system is an SM-4P processor, internal storage (with capacity of 40K words), console terminal and plug-in type magnetic disk store.

The auxiliary devices are an internal storage with capacity up to 124K words, paper-tape input-output device, console terminals (up to 24), data transmission equipment, plug-in tape magnetic disk stores (up to 8), industrial magnetic tape store, magnetic disk stores with fixed heads (up to 4) and floppy disk stores.

The test-monitor operating system (TMOS) is designed to combine all SM-3 and SM-4 test equipment into a unified system. The system permits one to automate the process of checking the computer complex and to operationally change texts during adjustment of devices to recycle error situations. The TMOS offers a wide range of devices to the adjuster to facilitate the process of adjusting the equipment.

The system is used in the SM-3 and SM-4 control computer complexes to work jointly with equipment tests of the computer complex.

The TMOS program is delivered on papertape carriers.

The TMOS SM includes the following program components: monitors (zero and one), correcting programs (1 and 2) and a text editor.

The main designation of the monitors (0 and 1) is automatic execution of test programs in the chain mode. The main designation of the correcting programs (1 and

2) is modification of the test programs in the internal storage, duplication of carriers and generation of the test-monitor system.

The text editor is designed to create text documents and to edit the symbol text of the programs.

The test programs used in the TMOS are also created in other operating systems and should be presented on a papertape carrier in absolute binary format for inclusion in the TMOS SM. The standard point of entry into the text program should have an absolute address of $200_{(8)}$. The test programs should not change the contents of the memory cells with absolute addresses of $40_{(8)}$ and $42_{(8)}$. A minimum configuration of hardware--an SM-3P or SM-4P processor, an internal storage with capacity of 8K words, papertape input-output device and alphanumeric terminal--is required for operation of the system.

The expanded composition of the peripheral equipment includes an internal storage with capacity up to 28K words, an alphanumeric printer and a magnetic disk carrier.

4.4. Applied Program Packs

The software of the SM-3 and SM-4 control computer complexes includes procedure-oriented and problem-oriented applied program packs (PPP).

The procedure-oriented packs include:

a) production-oriented program packs (packs that implement individual data processing functions);

a remote data processing system (STOD);

a data base control pack (SUPD) in the DIAMS system;

an applied program pack for management of data banks on SM-3, SM-4 and M-4020 multimachine hierarchical complexes (IRIS).

b) method-oriented program packs (packs that implement logic-mathematical methods of data processing):

numerical analysis program packs (ChAP);

program packs for data processing by mathematical statistics methods (PAST);

program packs for optimization methods (OPTIMUM);

program packs for network planning methods (PASEP).

Problem-oriented packs include:

program packs for simulation modelling of analog and digital processes (SIMFOR);

program packs oriented toward economic applications (PEKO);

program packs for data processing in laboratory experiment automation systems (PALEKS);

program packs for scientific and engineering calculations (NTR).

Production and method-oriented program packs contain the most widespread data processing procedures and are used under the control of disk operating systems.

The relationship of operating systems and applied program packs is shown in Table 4.2.

Table 4.2. Relationship of Operating Systems and Applied Program Packs

Applied Program Pack	Operating System			
	DOS	DOS RV	FOBOS	OS RV
STOD	+			
ChAP	+	+	+	+
PAST	+	+	+	+
OPTIMUM	+	+	+	+
PASEP	+	+	+	+
SIMFOR			+	
PEKO	+			
PALEKS			+	
NTR	+	+	+	+
IRIS			+	

The composition and parameters of hardware for the SM-3 and SM-4 control computer complexes required for functioning of applied program packs are determined by the requirements on the hardware of those disk operating systems under whose control the pack is executed.

The remote data processing system (STOD) is designed to control the data transmission processes over communications lines and to service remote data processing systems and message concentrators and switches based on the SM-3 or SM-4 control computer complex.

The STOD system has a wide range of areas of application--from industrial research and scientific developments to control systems. A remote pack processing system and a system that requires data exchange between remote terminals and computers and between different computers can be developed on the basis of the STOD.

The STOD program pack is designed on the modular principle and consists of the following main modules:

a monitor for remote data processing;

terminal servicing subprograms, the arrangement of which is determined by the operating characteristics of a specific terminal to be serviced;

input-output servicing subprograms related to control of the modem and data transmission.

Executing the functions most difficult for encoding and debugging, the STOD offers the following capabilities to the user: initiation of data transmission lines, message reception and transmission over communications lines, message buffering synchronization during message transmission and communication of systems subprograms with the user program.

The STOD is delivered in two versions: for self-contained operation and for operation under control of a disk operating system.

When using the autonomous version, the program modules of the pack and also the user programs should be located in the internal storage.

The disk version of the pack combines the capabilities of the autonomous version of the STOD and the disk operating system under whose control it operates.

The distributed hierarchical information system for management of the data bank on multimachine complexes of the international small computer system--the M-4030 (IRIS)--is designed to manage centralized data banks (TsBD) on the M-4030 (or M-4030-1) control computer complex and to provide operation with them on multimachine complexes of the international small computer system and M-4030.

The IRIS system is used in information retrieval systems, statistical data processing systems, financial and personnel systems, operational accounting and planning systems, reserve control systems, ASU TP [Automated production process control systems] and experiment and test data gathering and processing systems.

Access to data banks created under the control of IRIS is gained both in the pack and in the dialogue mode. The use of the effective FOBOS real-time operating system at the lower level (SM-3 and SM-4) provides the capability of organizing real-time interaction with the TsBD via the international small computer system.

The IRIS system provides for communication with the user in a special language close to natural, which is very simple to implement and which does not require special knowledge for studying it. Moreover, user programs compiled in Assembler languages of the M-4030, Macroassembler language of the international small computer system, FORTRAN and COBOL can be connected to the IRIS system.

The IRIS system is a further development of the integrated data processing system (SIOD), which is completely compatible with it.

If the user has no standard hardware for remote data processing of the M-4030 (M-4030-1), their functions can be successfully entrusted to the international small computer system. The use of the international small computer system to control remote processing is very efficient since it relieves the resources of the M-4030 (M-4030-1) control computer complex.

The use of the IRIS system is based on the following characteristics:

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the capability of storing a large volume of data of arbitrary structure that occupy tens of volumes of disk memory;

the capability of rapid access to the required data via local or remote terminals of tens of users by means of programs that work with the international small computer system or in the M-4030 (M-4030-1);

the capability of receiving data from the TsBD according to one or several given features that are in complex logic relationship;

to use both Assembler level languages and high-level languages to write user programs;

the presence of special devices that ensure the functional reliability of the system (security copies of the TsBD, control points and repeat starting):

a variety of data formats.

The use of the IRIS system completely frees users from solving problems of data organization, data security, from programming input-output procedures, data retrieval and remote processing control. The presence of special devices to generate reports, to issue tabular information and information on given patterns renders significant assistance to the user.

The use of the IRIS system to protect information against unauthorized access acquires special significance.

A block diagram of the IRIS system can be represented in the form of three interrelated components (Figure 4.1):
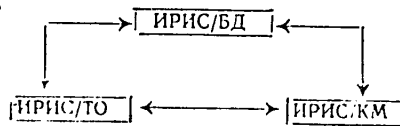
Figure 4.1.

The IRIS/BD (data bank) is the nucleus of the system and provides internal management of the data bank on the M-4030 (M-4030-1). The IRIS/BD subsystem functions under the control of the ASVT-2 disk operating system in the M-4030 (M-4030-1) and can be used both for independent application and for joint operation with the IRIS/TO (remote processing) and IRIS/KM (complex).

The functions of the IRIS/BD include data control, operational work with data banks and service assistance to users.

IRIS/TO provides telecommunications access to the TsBD both via terminals connected to the M-4030 and via terminals of the international small computer system. The IRIS/TO subsystem is delivered to the user jointly with the IRIS/BD in three versions:

for working in the M-4030 (M-4030-1) control computer complex equipped with a data transmission control device (UUPD) and VT-1 video terminals;

for   on the M-4030 (M-4030-1) control computer complex equipped with UUPD to which the SM-3 (SM-4) computer with its own video terminals is connectéd through one communications line. The international small computer system performs the functions of data transmission concentrator;

for working on the M-4030 (M-4030-1)--SM EVM multimachine complex connected via a computer communications device (USVM). The IRIS/TO functions jointly with the IRIS/KM and the international small computer system is used as a telecommunications processor.

The IRIS/KM is a set of program interfaces that support the work of users with TsBD on M-4030 (M-4030-1)--SM EVM multimachine complexes.

The user is offered the following capabilities by the international small computer complex when using the IRIS/KM:

real-time access to the TsBD;

maintaining a dialogue with the TsBD on the M-4030 (M-4030-1) control computer complex in simple language from several terminals (up to eight);

transmission of pack assignments for execution of them on the M-4030 (M-4030-1) control computer complex and receipt of the results of execution on the international small computer system;

access from applied programs on the international small computer system and TsBD to the M-4030 (M-4030-1) control computer complex.

The IRIS/KM subsystem provides the capability of connecting several control computer complexes of the international small computer system to the M-4030 control computer complex. The IRIS/KM software from the direction of the international small computer system functions under the control of a real-time basic background-operating system (FOBOS) expanded to work with many terminals (including remote terminals).

The software of the IRIS system is delivered to the user on magnetic carriers.

The program pack for numerical analysis methods (ChAP) is designed to expand the areas of application of disk operating systems of the SM-3 and SM-4 control computer complex, specifically, to solve numerical analysis problems.

The program pack can be used during automation of production processes and scientific experiments, to carry out scientific and engineering calculations and to construct mathematical models of analog and digital processes.

The pack is a library of program modules in FORTRAN-4 that permits the user to create the pack configuration required to solve specific problems.

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The combination of pack modules permits one to perform the following functions:

solution of ordinary differential equations;

numerical integration of functions;

operations with polynomials and finding the roots of polynomials;

calculation of special functions;

Fourier transformation;

approximation and interpolation of functions.

The modules for solving ordinary equations solve first-order ordinary differential equations and systems of first-order ordinary differential equations. The modules for numerical integrations of functions calculate a specific integral of functions given in tabular form or expressed by nonelementary functions.

The modules of operations with polynomials and finding the roots of polynomials perform operations with polynomials, calculate the values of the first derivative and the integral of the polynomial and the real and complex roots of a real polynomial.

The modules for calculating special functions calculate the values of the following special functions: the gamma-function, the Kelvin function, hyperbolic functions, integral sine and cosine of elliptical integrals and Bessel and Neyman functions.

The modules for approximation and interpolation of functions perform quadratic interpolation of functions and interpolation of functions by means of the Eytkin process and approximation of functions by the least squares method.

All modules of the pack are written in algorithmic FORTRAN-4 language and are formulated as subroutines according to the requirements of this language.

The pack modules do not contain data input-output operations. These operations are executed by the user programs compiled in FORTRAN-4 language and which contain data input operations from external devices, access to pack modules required to solve a specific problem and the message output operation about the course of solving the problem and the results of calculations.

The pack is an open system and can be expanded by the users as necessary.

The program pack for data processing by mathematical statistics methods (PAST). The pack is designed to expand the areas of application of the disk operating systems of the SM-3 and SM-4 control computer complex, specifically to process data of arbitrary nature by mathematical statistics methods. The area of application of the pack is a wide range of scientific-engineering and economic problems (experimental data processing, queueing systems and automated systems of various designation).

The pack is a library of program modules in FORTRAN-4 that permits the user to create the pack configuration required to solve specific problems.

The complex of pack modules can be arbitrarily divided into the following functional parts:

calculation of the sequence of random numbers;

calculation of elementary statistical characteristics;

correlation and regression analysis;

dispersion analysis;

factor analysis;

analysis of time series;

generation of random numbers;

calculation of distribution functions;

calculation of nonparametric statistics;

preliminary processing of input data.

The pack also contains a number of service modules.

The modules for correlation and regression analysis process data by multiple line, polynomial, step regression and canonical correlation methods for the dependent variable and a number of independent variables.

The characteristics for analysis of a multifactor experiment and for analysis of observations of factors are calculated by means of modules for dispersion (planned) and factor analyses.

The modules for analysis of time series determine the autocovariation and mutual covariation of time series of observations and calculate their smoothed values. Modules for generation of random numbers calculate uniformly and normally distributed random numbers.

The module of distribution functions calculates the sequence of random numbers with given distribution law. The modules of nonparametric statistics make checks and compare one or two sequences of selected observations by measuring the divergence between the empirical and theoretical distribution functions.

The modules for preliminary data processing are used to calculate the elementary statistical characteristics of a series of observations and for racking and classification of input data.

Auxiliary modules are used to carry out operations on vectors and matrices, to print information in the form of graphs and so on.

All modules of the pack are written in problem-oriented FORTRAN-4 language and are formulated as subroutines according to the requirements of this language. The modules of the pack are free of input-output operations which should be in the basic program compiled by the user in FORTRAN-4 and which includes data input-output operations, access to pack modules and nonstandard data processing (not provided by means of the pack).

The pack is an open system and can be expanded by the user as needed.

The program pack of optimization methods (OPTIMUM) is designed to expand the capabilities of the disk operating systems of teh SM-3 and SM-4 control computer complexes in the area of solving optimization problems by linear and dynamic programming methods. The pack is used to solve scientific and economic problems that require the use of optimization methods. It provides a significant saving of labor expenditures in engineering design, scientific experiments, current and future planning and control of production and technological processes.

The pack is a library of program modules written in FORTRAN-4. The pack modules provide solution of the common linear programming problem, the transport problem, the whole-number programming problem and the one-dimensional dynamic programming problem with additive criterion of quality.

The modules for solving the common linear programming problem provide for solution of the common linear programming problem by the simplex method and by the modified simplex method. The modules for solving the transport problem achieve the solution by the Hungarian of the sampling problem, the closed model of the transport problem and the transport problem with limited communications capacity.

The modules for solving the whole-number programming problems achieves solution of a mixed whole-number linear programming problem by the branch and boundary method. The modules for solving the dynamic programming problem provide for solution of the one-dimensional dynamic programming problem with additive criterion of quality.

All modules of the pack are formulated as subroutines according to the requirements of this language. The pack modules do not contain data input and output operations. These operations should be provided by the user programs compiled in FORTRAN-4 language and containing data input operations from external devices, access to pack modules required to solve a specific problem and the operation of issuing messages about the course of solving the problem and the results of calculations.

The pack is an open system and can be expanded by the user as necessary. The pack is delivered on punchtapes.

The applied program pack of network planning methods (PASEP) provides for expansion of the areas of application of the SM-3 and SM-4 control computer complexes for solving the problems that require the use of mathematical network planning apparatus.

The applied program pack is used during automation of planning and control of developments on the basis of network methods. The use of the pack permits one to increase the effectiveness of controlling developments with a limited number of events. The program pack can be used when automating the solution of both local planning and control problems and of problems contained in automated systems of different designation.

The PASEP SM contains a set of programs for network processing and is designed on the modular principle, which permits the user to create the software configuration required for specific applications.

The pack modules are designed to perform the following functions:

input and preliminary processing of information on the operations of a network schedule;

selecting the work of a planning period;

calculating the parameters of a network schedule;

issuing information in documented form.

The modules for entry and preliminary processing of information about the work of a network schedule are designed for entry, editing and ordering of the list of operations and to determine the contours in the final oriented schedule. Work performed completely or partially during a given planning period is selected by the modules for selection of work of the planning period.

Modules for calculating the parameters of a network schedule are used to calculate the critical path, to determine early and late periods of the beginning and end of operations, to calculate total and free operating reserves, to convert relative dates to calendar dates and vice versa and to determine the values of deviation of actual fulfillment of operations from planned operations.

The modules for issuing information in documented form are designed to formulate the results of calculation in the form of output documents and to issue output forms of documentation on an alphanumeric printer.

All modules of the pack are written in FORTRAN-4 and are formulated as subroutines in this language according to the system standards.

All modules of the pack are independent of input-output operations, which are written by the user in the basic program that solves a specific problem.

The pack is delivered on papertape carriers (on magnetic disks or tapes in the expanded version).

The program pack for simulation modelling of analog, analog-digital and digital processes (SIMFOR).* The area of application of the pack is essentially unlimited

*SIMFOR--Simulation Modelling System in FORTRAN.

since any system and any process can be reduced to one of three of the named groups without special violations of the requirement of the adequacy of the phenomenon and model (data processing and transmission systems, transport equipment flows, communications systems, the wide range of problems represented by queueing models, continuous production process control systems, aircraft and spacecraft, automatic control systems, physical experiment control systems, ecological systems and so on). The advantage of the pack is the capability of modelling analog-digital phenomena and working with analog and digital models of phenomena without changing the programming system.

The pack is a set of program modules written in FORTRAN-4 language with its own control program, which permits the user to write the phenomena to be modelled in subroutines standard in their format. The pack and control programs are adjusted to the user's needs during generation of the pack in the dialogue mode.

The pack contains programs with the following functional designation:

the initiation program sets the initial state of the model and the pack;

the control programs of the pack provide the necessary sequence of operation of individual modules of the system;

the programs for communicating with the system permit the user to interfere in the modelling process at any step to review and modify the variables contained in the description of the model;

the error processing programs provide diagnosis of errors occurring during modelling;

the statistics gathering program permits accumulation of information related to specific parameters of the model and subsequent processing of it by statistical analysis programs;

the differential equation-solving program is used to simulate analog processes described by differential equations in SIMFOR language;

the event servicing program determines whether any event, digital or related to analog changes in the system occurs at a given moment in the model and if it does occur, whether it induces a corresponding event processing program which is written by the user and which is a part of the description of the system being modelled;

programs for laying out the modelling process permit one to obtain not only the final result of modelling but also the intermediate results during modelling of the system.

the model time processing program is engaged in management of accounting for the model time;

the input-output programs provide control of input-output operations and solution of the entire range of related problems;

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graphical information display programs construct histograms and graphs on the basis of the infromation gathered during modelling for the system parameters indicated by the user;

random number sensors permit one to find several independent flows of random numbers with the required distribution parameters;

the user programs include the programs for processing the events occurring in the system and describe digital and analog events occurring in the model;

the servicing programs provide service functions and performance of additional auxiliary functions of the pack.

The pack also contains a generation program which provides adjustment of the pack to specific user requirements to optimize the use of systems resources of the control computer complex.

User modules that describe the model are written in FORTRAN-4. Inclusion of programs written in Macroassembler language is also permitted.

SIMFOR is an open modular system, i.e., the user has the capability of expanding the pack functions by his own programs, for example, for processing input-output operations, nonstandard error and data processing, management of new random number sensors and so on.

SIMFOR operates under the control of the FOBOS operating system and requires 28K words of internal storage.

A program pack oriented toward economic applications (PEKO) is designed to process small volumes of economic data at enterprises and in organizations where the use of large computers is unfeasible. The area of applicationof the pack is design and introduction of economic information processing systems that perform planning and control functions.

The pack equipment together with the technical capabilities of the SM-3 and SM-4 control computer complexes provide the use of the SM-3 and SM-4 UVK in th ASU for organizational management of small enterprises and organizations as a lower level technical base of hierarchical systems for automation of solving individual problems of business production, accounting and planning and so on.

Program packs for solving control problems for specific groups of enterprises (standard solutions) can be created on the basis of the pack modules.

The pack is designed on the modular principle and contains two groups of modules that provide both data file processing and file-recording operations.

The pack modules are designed to perform the following functions:

input and primary monitoring of data with recording on magnetic disk or magnetic tape and with monitoring of the entered information;

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sorting and merging of data files;

data processing;

data retrieval to external UVK devices, including to alphanumeric printers in a form convenient for the user.

The pack modules are written in FORTRAN-4 and Macroassembler.

The user organizes access to the pack modules from the main program containing the parameters required for adjustment of modules to solve a specific problem.

The PEKO pack is executed under the control of a disk operating system DOS having translators from Macroassembler and FORTRAN-4 languages.

The data processing program pack in systems for automation of laboratory experiments (PALEKS) is designed to expand the capabilities of the disk operating systems of SM-3 and SM-4 UVK in the area of analysis and processing of experimental data. The area of application of the pack is a wide range of problems of logic-mathematical data processing at all stages of investigations in laboratory systems of different nature.

The pack is a library of program modules that permits the user to create the pack configuration required for a specific application.

The complex of pack modules permits one to realize the following functions:

analysis of planned experimental data;

calculation of main and nonparametric statistics;

analysis of eigen-values;

forecasting and analysis of time series;

generation of random numbers;

solution of linear algebraic equations;

calculation of special functions;

multidimensional analysis;

operations on matrices.

The pack also contains service modules.

The modules for analyzing planned experimental data permit dispersion analysis for different plans of cross and hierarchical classification of experimental data. The modules for calculation of main and nonparametric statistics calculate the main statistical characteristics of an aggregate of observations and check statistical hypotheses using distribution-free methods.

Eigen-values and eigen-vectors of real asymmetrical and symmetrical matrices are determined by means of modules for analysis of eigen-values and the structure is analyzed, the parameters of models of time series are estimated and time series are analyzed by means of modules for forecasting and analysis of time series.

Modules for generation of random numbers generate uniformly and normally distributed random numbers with given characteristics. The modules for solving linear algebraic equations permit one to solve linear algebraic equations for various types of system matrices.

The modules for calculating special functions calculate special statistical and mathematical functions. The modules for multidimensional analysis permit one to represent the structure of experimental data by using models of regression analysis and the method of the main components of correlation analysis.

Modules for operations on matrices execute arithmetic operations on matrices, transposition, inversion of matrices and conversion of methods of storing them.

The auxiliary modules provide reading of matrices, printing of matrices and vectors and printing of messages about errors detected in the call-up module.

All pack modules are written in FORTRAN-4 and are formulated as subroutines according to the requirements of this language.

The pack modules contain no data input and output operations. These operations should be provided by user programs compiled in FORTRAN-4 and which contain data input operations from external devices, access to the pack modules required for solving a specific problem and operation of message retrieval about the course of problem-solving and the results of calculations.

The pack is an open system and can be expanded by the user as needed. The pack is delivered on papertapes.

The program pack for scientific and engineering calculations (NTR) is designed to expand the capabilities of the disk operating systems of SM-3 and SM-4 control computer complexes in automation of engineering calculations in different areas of science and technology. The area of application of the pack is a wide range of problems of computer mathematics that utilize linear and matrix algebra.

The pack is a library of program modules that permits the user to create the pack configuration required for a specific application.

The complex of pack modules permits one to perform the following functions:

matrix storage;

matrix conversion;

matrix arithmetic operations;

operations on the lines and columns of matrices;

solution of systems of linear equations;

analysis of eigen-values.

The pack also contains service modules.

The matrix storage modules provide writing of both the entire matrix and of its individual lines and columns in the form of a vector, calculation of the index in a tightly stored matrix and variation of the method of matrix storage.

Matrix conversion modules perform matrix inversion, matrix transposition and products of matrices and matrix conversion by means of user functions.

Matrix arithmetic modules perform operations of addition, subtraction and multiplication of matrices and scalar multiplication and division of matrices.

Tabulation, sorting, rearrangement, addition and other operations on the lines and columns of matrices are provided by means of modules for operations on the lines and columns of matrices.

Modules for solving systems of linear equations provide solution of systems of joint linear equations by the Gauss method and by other numerical methods.

Modules for analysis of eigen-values calculate the eigen-values and eigen-vectors of real symmetrical and special asymmetrical matrices.

The auxiliary modules perform service functions: reading of control writing and of data elements and matrices from the input device by papertape and printing of files of any dimensions on the alphanumeric printer.

All pack modules are written in FORTRAN-4 and are formulated as subroutines according to the requirements of this language. The pack modules contain no data input-output operations. These operations should be provided by the user programs compiled in FORTRAN-4 and which contain data input operations from external devices, access to the pack modules required to solve a specific problem and operations to retrieve messages about the course of problem-solving and the results of calculations.

The pack is an open system and can be expanded by the user as needed. The pack is delivered on papertapes.

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DESIGN OF CONTROL COMPUTER COMPLEXES

[Excerpts] 5.2. Principles of Configuring User Complexes of the International
Small Computer System

User complexes are configured from baseline, specified, standard specified or
problem-oriented complexes and unit modules of the international small computer
system. The configuration procedure, as a result of which the hardware and soft-
ware composition of the complex is determined, is an iterative sequence of logic,
structural and electrical configuration steps and software configuration.

Logic configuration includes interrelated selection of the basic software compon-
ents (of the operating system, applied program pack and other types), the baseline,
standard or problem-oriented complex and auxiliary external devices and modules
which most fully meet the requirements of solving the user's problems in the
system.

Problems of arrangement functional modules and devices in standard design compon-
ents are solved at the structural configuration stage.

Electrical configuration includes selection of the set of cables, conductors and
power supply sources for structurally configured devices and modules.

The composition of the modules of the operating system (drivers of auxiliary de-
vices, monitors and so on), methods of including applied program packs in the sys-
tem and the characteristics of generating the software system for a specific user
complex are refined at the software configuration stage.

Logic Configuration

Let us consider some common principles of logic configuration and the character-
istics of designing complexes based on the SM-3 and SM-4.

The main task of logic configuration can be defined as selection of the minimum composition of devices, units and modules from the nomenclature of the international small computer system (or in some cases from the nomenclature of other families of computer equipment) that provide sufficiently effective execution of functional problems faced by the system and also complexing of these individual devices, units and modules, i.e., combining them into a unified computer system that operates under given conditions under the control of a common operating system. Several alternative schemes of logic configuration can be used in practice which are characterized by the characteristics of the system being designed, the experience accumulated by developers, available data and so on.

The requirements of complexing devices into a unified system may be taken into account to the maximum degree when selecting the devices to simplify the logic configuration. Therefore, logic configuration can begin with selection of the operating system and then the standard or baseline complex is selected and problems of connecting the auxiliary devices to the selected standard specified or baseline complex are solved at the last stage of logic configuration.

The input data for selecting the type of operating system are the operating mode, internal storage capacity, the required hardware which should be maintained by a given operating system, the number of users, the type of systems carrier, programming languages, problem-execution mode, program processing and debugging mode, availability of remote processing, restrictions on the operating conditions of the complex, the need to compile applied program packs and so on.

The type of operating system is selected for these input data with regard to the data of Table 4.1. However, the selection may not always be identical at this stage.

For example, a complex operating in real-time mode (a systems carrier--plug-in magnetic disk type) with dialogue debugging of programs and so on must be configured.

Let us assume that a real-time disk operating system and real-time operating system meet all the given requirements according to Table 4.1. These operating systems have the following advantages. The real-time disk operating system provides higher responsiveness of the system and simplicity of operation. The real-time operating system provides the capability of building up the memory (to 64-124K for SM-4 complexes) and management of remote processing modes.

Thus, selection of a specific operating system may be rather cumbersome and may require deeper study of the technical documentation or may require one to conduct additional investigations (responsiveness, reliability, functional completeness of the software system and so on).

The standard specified complex on the basis of which the required complex of the international small computer system will be configured is selected after preliminary selection of the type of operating system. Besides the noted data, the following additional input data are required: the parameters of the input and output information (capacities, carriers, speed and level of reliability), the capacities of the stored information, methods of file organization, data bases, methods of

access to files and methods of file correction, the required productivity of the complex in typical information processing modes, the capacity of system carriers, the selected method of redundancy and support of the operating reliability of the complex and the distance at which the input devices of the sensor signals, the information output devices and terminals are located from the complex.

These input data are determined at the stage of examining the facilities and during compilation of the technical assignment (TZ) for the complex by methods developed for typical areas of application of computer equipment. Some aspects of the methods of determining the indicated input data are presented in [7, 8, 14, 15].

The standard specified complex which can initially work with the selected operating system and which can completely meet the requirements of the input data (types of modules, units and systems modules) must be determined from these initial data from the list of standard specified complexes (for example, according to the data of Table 5.1). If the second requirement is not met, a standard specified complex is selected for which connection of auxiliary modules, units and devices is provided with the least refinements (and permissible from the viewpoint of the configuration of complexes of the international small computer system). It should be taken into account that not all types of devices may be in explicit format and clearly determined from the materials of examining the facility and the technical assignment for development of the complex. Therefore, the complexes which include sets of devices and modules that most fully meet the postulated requirements must be selected from the alternative versions of standard specified complexes (with different types of devices) at the given stage of configuration of the complexes from the results of comparing the input data to additional characteristics of the modules.

For example, when selecting a standard specified complex for a facility control complex using a USO, if there is no need to locate the USO modules at a distance of more than 500 meters and operation with high-speed analog signal input devices is not required, SM-3-1, SM-3-2, SM-3-3/1 and SM-4-1 standard specified complexes can be used with connection of the USO modules to the common bus interface (UVA [Analog signal input device] and UVD [Digital signal input-output device]). The principles of configuration of UVA and UVD modules are considered in Section 5.3.

SM-3-4/1, SM-3-5 and SM-4-3 standard specified complexes can be selected if necessary to provide high-speed analog input, to work with remote USO modules or to use other devices from the nomenclature with a 2K interface. If the sets of USO modules with 2K interface connected to SM-3-5 and SM-4-3/2--SM-4-3/10 complexes (some characteristics of the USO of these complexes are presented in Table 5.2) do not correspond to the postulated requirements, then SM-3-4/1 and SM-4-3/1 complexes are selected. The required USO modules are connected to the 2K interface selected from the common nomenclature of the international small computer system are connected to the interface matching devices (OSh/2K USS) contained in these complexes at the next stage of configuration.

In the general case the required level of productivity, internal storage capacity, the need for memory security and so on must be taken into account to refine the

type of processor (SM-3 or SM-4). The type of processor is refined and the specific standard specified complex is selected (for example, an SM-3-1 or SM-4-1 or SM-3-4/1 or SM-4-3/1 from the examples considered above) according to the configuration differences (see Chapter 1) and the required input data.

The logic configuration step is completed by connection of auxiliary peripheral devices to the selected standard specified complex. The following versions are possible in this case:

the total number of peripheral devices of the type under consideration (for example, NMD, NML and so on) does not exceed the maximum number of devices connected to a single controller which is included in the standard specified complex. In this case the auxiliary devices are connected to a given controller. For example, the total number of connected plug-in disks may be equal to four for an NMD controller;

auxiliary controllers from the SM-3 and SM-4 nomenclature must be connected; the restriction on the number of controllers in the selected operating system and the capacity of the channel in the selected mode are checked when configuring the complexes;

nonstandard devices or devices from the SM-3 or SM-4 nomenclature in nonstandard operating modes must be connected. To do this, interface matching devices (for example, the OSh/2K USS, CAMAC controller, ASET controller or a device of the programmable controller type) are used or new drivers of devices are developed with regard to the instructional requirements of specific operating systems.

The intersystems communications modules (bus switches and interstation communications adapters) described in Chapter 3 may be used to configure complexes of increased survivability. Versions of configuring two-processor complexes using these modules are presented in Figures 3.8 and 3.12.

Structural Configuration

The main structural components of the system are the component unit, plug-in unit, self-contained complete unit and bay.

The component unit (BE) is based on a printed-circuit card with integrated circuits and components.

The plug-in unit (BK) is designed for disposition and structural joining of the component unit and is based on a chassis with windows for installation of plug and socket units and guides for installation of the component unit. A 94-contact plug and socket unit is used as the main plug and socket unit. The chassis of the plug-in unit is divided into three sections (A, B and C) along the horizontal and into 3-12 levels along the vertical (depending on the version). The levels are numbered from bottom to top and the spacing of the levels is 15 mm.

The self-contained complete unit (AKB) is designed to install a plug-in unit, power supply and ventilation systems in it. When the unit is removed from the bay, access to the main installation of the plug-in unit is provided by rotating the power supply sources by 180°.

The bay (ST) is designed for installation, electrical connection and damage pro-
tection of the devices built into it. Structurally, the bays of the international
small computer system (ST1 bays) contain a built-in forced ventilation system,
main power supply and grounding. Distributing frame units, a power supply unit
of the measuring and signal circuits and a distributing frame panel are also in-
stalled in bays designed for communicating with the facility (ST2).

Bays for independent installation outside the bays of the control complex (ST1/1
and ST2/1 bays) are produced with lateral sheathing; the middle part of the later-
al sheathing is absent in ST1/2, ST2/2 and ST2/3 bays. The sheathing of the adja-
cent bay of the plug-in unit is used when they are joined to the complex.

The front panel of the bay is formed by the front panels of the installed units and
blank panels. The blank panels are ranged at points of the front part of the bay
free of devices.

The devices are installed in the bay on guides and are attached to the frame of the
bay by screws behind the front panel. The guides can be installed at any of the
levels (with the exception of 34, 35 and 36).

The bay is arbitrarily divided by height into 36 levels designed for installation
of devices. Each level is equal to a buildup module with height U = 44.45 mm.
The levels are numbered from top to bottom.

The specifications of the bays are as follows:

Specifications of Bays	ST1/1	ST1/2	ST2/1	ST2/2	ST2/3
Nominal height of window for installa-tion of units (U = 44.45 mm)	30U	30U	12U	12U	18U
Overall dimensions, mm		1,800 X 600 X 850			
Mass, kg (not more than)		100			
Consumed power (internal) kV·A (not more than)	0.3	0.3	0.75	0.75	0.75
Permissible heat release of installed units, kW (not more than)	1.5	1.5	1.2	1.2	1.2
Temperature transfer with respect to surroundings, t°C (not more than)		10			
Number of distributing frame units (at eight adjusting points for 36-contact distributing frame recepta-cles and normalization units)	--	--	6	6	4

The bay has no doors in front and the external appearance is arranged by face panels of the built-in devices. Free areas are covered with easily removable blind panels. The concept of standard location is defined to simplify the configuration process. The number of standard locations is determined by the number of levels of the bay. Thus, if the self-contained complete unit has a height of 6U, then this unit will occupy six standard locations of the bay.

A horizontal row (sections A, B and C) of plug and socket units of the plug-in unit installed in the AKB is taken as the unit of standard location in the AKB. Thus, if two six-row plug-in units are installed in the AKB, there are 12 standard locations for installation of the component unit.

Devices of the following types are configured in the bay of the complex:

devices of the international small computer system having final structural version (AKB). These devices are installed on the free locations of the bays or in an additional bay and are connected to the common bus by common bus cable of the required length;

devices whose controller is realized in the form of two component units developed for inclusion in the systems interface unit (BSI) of the processor or the system expansion unit (BRS);

devices that utilize more than two component units (for example, ADS) having individual installation and not having a final structural version used to communicate with the common bus interface. Similar devices can be assembled in BSI and installed in BRS.

A BRS is used if more than four of these devices must be connected to the SM-3 or more than three must be connected to the SM-4. A BRS is installed in a standard bay of the international small computer system.and permits connection of the devices and controllers of external devices (VU) in the form of two component units (a selector and driver) and which meet the requirements for connection to SM-3P and SM-4P processors and devices and controllers of external devices in the form of a plug-in unit and which meet the requirements of the common bus interface to complexes of the international small computer system.

Each systems interface unit permits connection of up to six VU controllers. The VU controller usually consists of two component units: a selector that determines the address of the connected external device and that performs interrupt and control functions of the controller mode (it is installed in the plug and socket unit of zone C) and a driver that performs specific logic control functions of the VU mechanism (it is installed in the plug and socket unit of zone B) and also cables for connection of the external device (installed in the plug and socket unit of zone A).

The BSI has regular installation. The signals of the common bus interface enter the BSI through the common bus cable to the upper plug and socket unit of zone A (A6) and emerge from the BSI through the lower plug and socket unit of zone A (A1).

If there are two BSI in the BRS, they are connected to each other by a cable installed between plug and socket unit A6 of the lower BSI and unit A1 of the upper BSI.

If there are no other devices in the complex connected to the common bus interface in series after the BRS, a common bus blind panel from the makeup of the complex should be installed in plug and socket unit A1.

The power supply unit permits connection of a load up to 20 A (but not less than 1 A) to the 5-volt bus.

The configuration of the system for communicating with the facility (USO) occupies a special place in the structural configuration. This is determined by the complexity of design of similar systems and by the variety of possible configurations of complete USO.

BKI-AV and BKI-DV units are arranged in the system expansion unit (BRS) installed in the processor bay.

The systems for communicating with the facility can be configured from USO modules (see section 5.2) connected via the USS-OSh/2K integration matching device. The USS-OSh/2K consists of a control unit (USS BU) and an interface unit (USS BI). Each of the units occupies 6U.

The process of structural configuration consists of two steps: determination of the composition of structural components that permit arrangement of the selected composition of devices and the configuration of the complex.

During the first step:

the baseline complex of the international small computer system and the composition of auxiliary external devices from the nomenclature of the international small computer system are selected;

the number of free standard locations in the bays of the baseline computer complex is determined and the capability of arranging auxiliary devices in them (in the AKB) is checked. If there are insufficient free locations, an additionally ordered bay is used. Configuration data of devices of the international small computer system are presented in Table 5.2;

the number of free standard locations in the BSI of processors and BRS is determined and is compared to the number of auxiliary external devices (of second type) required for arrangement of the controllers. Missing BRS are ordered additionally;

the possibility of installing a device consisting of the available BRS in the plug-in unit is checked if these devices exist among the auxiliary devices. If there is no BRS or if it is filled, an additional BRS is ordered.

The diagram for configuration of the bays of the computer complex is developed during the second step on the basis of ergonomic and aesthetic requirements.

Electrical Configuration

The first step of electrical configuration includes finishing the structural-logic circuit for connecting the devices of the computer complex, i.e., connection of the interface units and controllers to the common bus and connection of devices to the controllers, expanders and so on according to the principles which are considered below.

Examples of structural-logic diagrams for the two baseline complexes are presented in Figures 5.4 and 5.5.
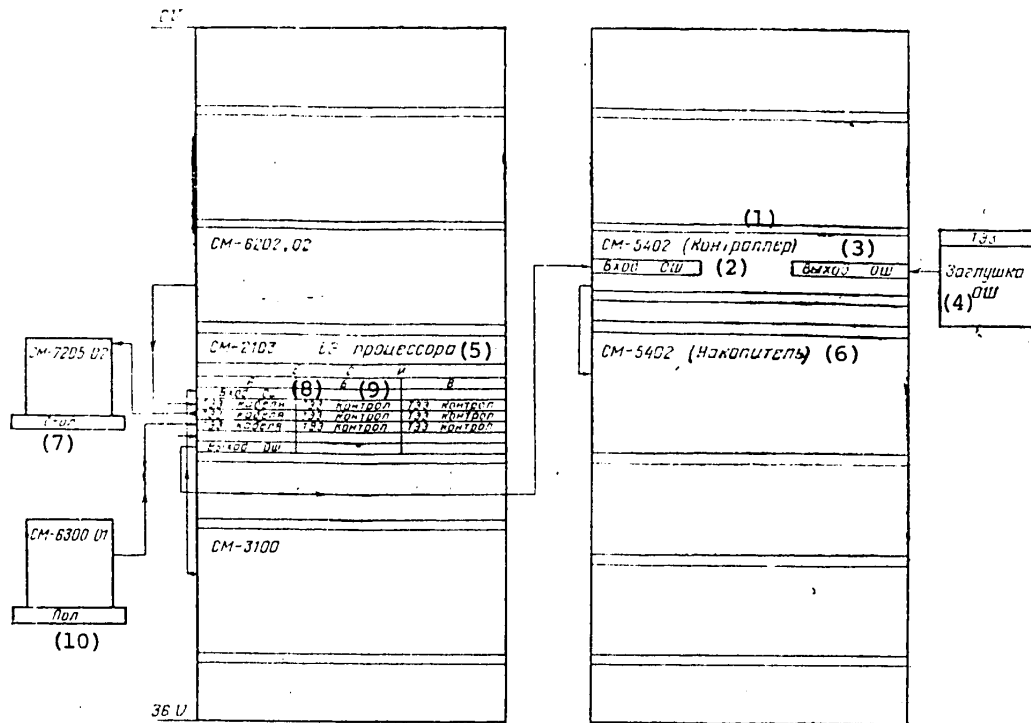

Figure 5.4.   Structural-Logic Diagram of SM-1301.03 Complex

Key:
1.	Controller	6.	Storage device
2.	Common bus input	7.	Desk
3.	Common bus output	8.	Cable
4.	Common bus blind panel	9.	Controller
5.	Component unit of processor	10.	Floor

The following configuration characteristics of the SM-3 and SM-4 should be taken into account when interface units and controllers are connected:

the common bus is physically realized in the form of main installation plug and socket units on a plug-in unit (section A) of individual devices of the

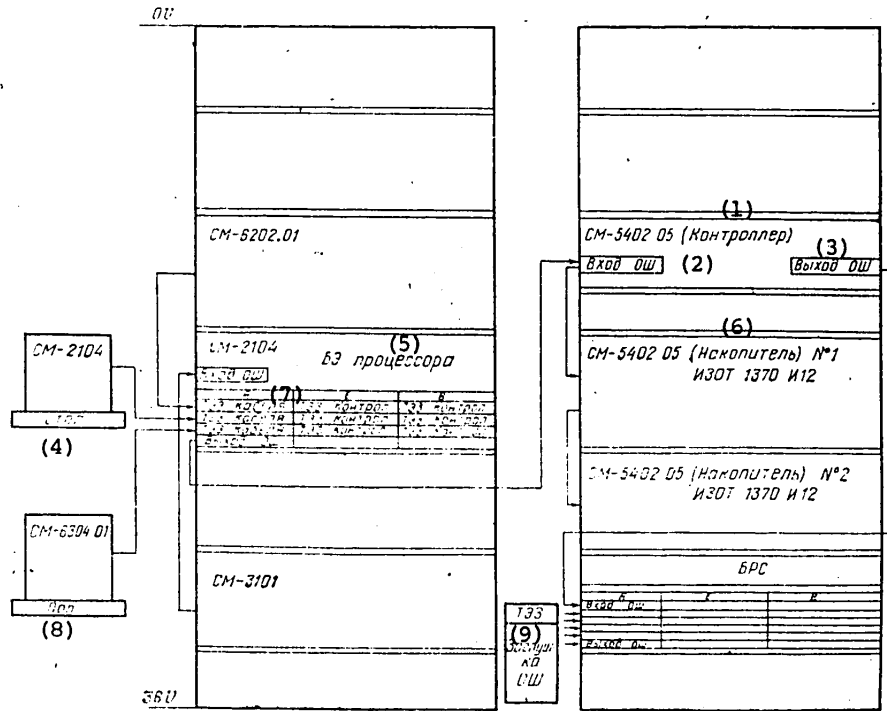Figure 5.5.   Structural-Logic Diagram of SM-1401.03 Complex

Key:
1. Controller	6. Storage device
2. Common bus input	7. Cable
3. Common bus output	8. Floor
4. Desk	9. Common bus blind panel
5. Component unit of processor	

computer complex (the processor, IZOT 1370 storage controller, BRS and so on) and the common bus cable that connects these devices. The common bus of the devices has a beginning (common bus input) and end (common bus output). If several devices are connected through the common bus, the common bus input of the second device (for example, the storage controller) is connected by means of the common bus cable to the common bus output of the previous device (for example, the processor) and so on. The internal storage (OZU) is connected to the common bus input of the processor, to the common bus output plug and socket unit of the last device connected to the common bus and a common bus blind panel is installed;

the length of the common bus should be no more than 15 meters;

the load on the common bus of the complex should not be more than 20 load units;

if the enumerated conditions are not fulfilled, an auxiliary device--interface expander OSh (RIF) in the form of a plug-in unit and installed in the BRS--must be used. The RIF permits additional connection of 18 loads;

an integration matching device (USS OSh/2K) must be ordered for use in the modules of external devices with 2K interface (from the M-6000, M-7000, SM-1 and SM-2 nomenclature). Structurally, the device is made in the form of 2 AKB--a control unit (6U) and interface unit (6U) which are installed in the SM-3 and SM-4 bays and are connected to each other by two cables. The interface unit permits connection of up to 16 external devices to the 2K interface or up to 8 expanders of 15 external devices each.

Physically, the USS OSh/2K does not exceed two load units.

The set of conductors required for electrical connection of the complexes is selected during the second step for the configured devices.

The third step includes checking the conformity of the output of the established power supply source consumed by the devices and selection of additional power sources if necessary (see Table 5.2).

The power supply of SM-3 and SM-4 complexes includes that of the bays and the power supply units of the AKB designed to supply power to the devices in these AKB.

The total consumption of the auxiliary component units or devices in the plug-in unit is determined during this step and the balance with the power supply sources available in a given AKB is established. If the plug-in units are installed in a separately ordered AKB, the power supply source conforming to the power consumed by the component unit must be selected.

5.3. Devices for Communicating With the Facility

Functional Capabilities and Composition of the Devices

The devices for communicating with the facility (USO) provide:

normalization of signals from resistance thermometers of all standard gradations;

temperature compensation of cold thermocouple junctions;

entry and conversion of low- and medium-level analog signals to binary codes;

noise suppression of common and normal types in the measuring channel of analog signal input;

digital signal input;

i.itiating signal input;

number-pulsed signal input-output;

digital signal output;

analog signal output;

autonomous retrieval of the initiating channel address;

information exchange with SM-3 and SM-4 processors through the common bus interface.

The devices for communicating with the facility contain a portable normalization unit (BNV), an analog signal input device (UVA) and a digital signal input-output device (UVD).

The portable normalization unit (BNV) is designed for:

normalization of resistance thermometer signals (gradations according to GOST 6651-78 and measurement range according to GOST 7164-71);

automatic compensation of the thermoelectromotive force of the free ends of thermoelectric thermometers;

positive bias of the entire range of output signals of thermoelectric thermometers;

transfer from individual cables that carry signals from the thermoelectric thermometers and resistance thermometers to the common (group) cable.

The BNV is designed for joint operation with the analog signal input device UVA in the SM-3 and SM-4 control computer complex.

The unit functions under operating conditions provided by GOST 20397-74 for articles of group 3a: ambient air temperature of 5-ᴸᴸ°C, relative humidity up to 90° at 30°C and atmospheric pressure of 630-800 mm Hg.

With respect to stability to mechanical effects, the BNV tolerates vibration at frequency up to 25 Hz with amplitude of no more than 0.1 mm.

The maximum number of sensors connected to one BNV is equal to 16.

The communication line of the BNV to resistance thermometers is three-wire. The maximum cross-section of the strands led in by the cables is 2.5 mm^2. The communication line of the BNV with the thermoelectirc thermometers is two-wire. The range of the normalized output signal of the resistance thermometers is from 0 to 35 mV.

Power is supplied to the BNV from an AC system with voltage of 220 V and frequency of 50 Hz. The consumed power is not more than 50 V·A and the overall dimensions are 456 X 465 X 220 mm.

The unit functions in the following manner. Signals from the thermoelectric thermometers are fed to the BNV, where the thermoelectromotive force of their free ends

is compensated for (and the band is shifted if necessary). The compensating voltage is shaped by a bridge, to one of whose arms a temperature-inedepent resistor is connected. This resistor and the free ends of the thermoelectric thermometer are in a space insulated from the surrounding air--a so-called passive thermostat. The remaining components of the bridge are located outside the thermometer in BE 361. The number of bridge components depends on the gradation of the thermoelectric thermometer. The number of BE 361 used in the BNV depends on the version.

Signals from the resistance thermometers are fed to the unit and are connected to the bridge circuit by a three-wire scheme. In this case a matching resistor is placed in each conductor of the communication line with the resistance thermometer and the total resistor of the conductor and of the matching resistor should be equal to that indicated on the resistor label.

The signals of the resistance thermometers are normalized by the bridge circuit. All bridge components are arranged in the BE 362. The number of bridge components is determined by the gradation and measurement range of the resistance thermomenter. The number of BE 362 used in a single BNV depends on the version of the BNV.

The total number of BE 361 and BE 361 in the BNV is equal to 16 in any combination.

The power supply to the bridge circuits is individual. Sixteen insulated circuits of a single-stage parametric DC stabilizer arranged in groups of four each on individual printed-circuit cards (BE 389) is provided for this in the BP 121 power supply unit.

The unit is made in the form of a special structure designed for suspended installation and is enclosed in a housing in whose side walls are openings for the input and output cables. The openings in the rear wall of the housing are intended for suspended installation.

The individual compensation wires from the thermoelectric thermometers are led into the BNV from below through the central opening in the housing. Type KPK5-11 receptacles are provided for attaching them.

The analog signal input device (UVA) is designed for input and conversion of DC voltages to a parallel 12-digit binary code from the facility sensors and also to receive control signals from the common bus interface and to transmit the results of conversion to the common bus.

Depending on the use of the apparatus for tying to the common bus (the presence of BKI-AV) and of controlling the UVA measuring channel (the presence of BKU-AV) and also the use of contact (BKK1) or contactless (BKK2) commutator, there is a number of versions of the analog signal input device of the international small computer system (Table 5.3).

A block diagram of the device is presented in Figure 5.6. Signals are fed from the sensors in the form of DC voltages to the inputs of the distributing frame panels based on two cards with metal-coated openings. Wires from the sensors and

Table 5.3.

No. of Item		Versions					
		UVA-0	UVA-1	UVA-2	UVA-3	UVA-4	UVA-5
1	Plug-in interface unit (BKI-AV)	1	1	-	-	-	-
2	Plug-in control unit (BKU-AV)	1	1	1	1	-	-
3	Plug-in expansion unit (BKR)	1	1	1	1	1	1
4	Plug-in relay switching unit (BKK-1)	2	-	2	-	2	-
5	Plug-in contactless switching unit (BKK-2)	-	2	-	2	-	2

The number of input channels in each of the UVA versions is 64.

normalizing resistors of type S5-5 (1 watt, 1 kohm, $\pm$ 0.05 percent) that convert current signals (in the range of -5-0 to +5 mA) to voltage signals (in the range of -5-0 to +5 V) are soldered to the cards.

The distributing frame panel provides connection of 64 two-wire analog signal sources.

Signals from the output of the distributing frame panel are fed to the inputs of two-plug switching units (BKK1 or BKK2). The input signals are filtered to the BKK by a symmetrical RC filters and two-wire two-stage switching of them is accomplished on RES43 relays (BKK1) or contactless switches of series K190 (BKK2).

The signal is fed from the BKK output to the input of the scaling amplifier made in the form of a plug-in expansion unit (BKR). The scaling amplifier amplifies the input analog signals and provides a standard signal at its output (in the range of -5-0 to +5 V) regardless of the range of input signals since its amplification factor is controlled by the program method by signals coming from the BKU-AV unit.

Besides emission of control signals, the BKU-AV unit receives the format of the control word from the BKI-AV, it decodes the numbers of the channel, group, unit and amplification factor of the amplifier and carries out analog-digital conversion of the DC voltages in the range of 0-5 V.

The exchange of control signals, addresses and data with the processor through the common bus is carried out by the plug-in interface unit (BKI-AV). At the same time (see Figure 5.6), one BKI-AV unit provides the capability of working with sets of analog signal input devices in four directions, thus permitting operation of a processor with 1,024 analog input channels.
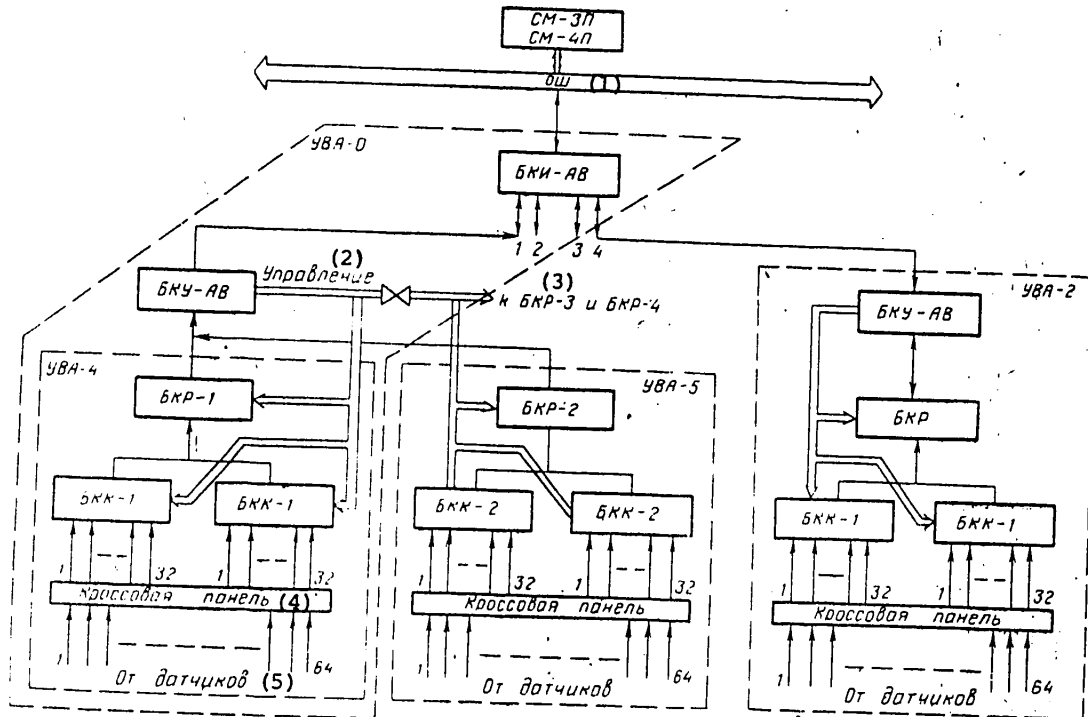
Figure 5.6. Block Diagram of Analog Signal Input Device: =>--control circuits

Key:
1. Common bus
2. Control
3. To BKR-3 and BKR-4
4. Distributing frame panel
5. From sensors

The characteristic feature of the UVA-1 compared to UVA-0 is the use of contactless switches BKK2 instead of contact switches BKK1. Components to protect the MOP-keys based on stabilitrons are introduced into the contactless switch.

The main structure of the analog signal input device is a self-contained complete unit having two modifications in height as a function of the equipment composition: 8U and 6U (U = 44.45 cm). Thus, the UVA-0, UVA-1, UVA-2 and UVA-3 have dimensions of 8U and the UVA-4 and UVA-5 have dimensions of 6U. These complete units have everything necessary for self-contained operation of the device, including power supply sources, blowers and distributing frame panel for connecting the wires from the sensors. Each self-contained complete unit contains (depending on the number of the modification) a set of plug-in units, each of which is a complete functional assembly.

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The analog signal input device has its own power supply system. The primary power supply is a single-phase AC system (220 V and 50 ± 1.0 Hz with deviations from the nominal voltage by +10 percent and -15 percent). The power supply system of the analog signal input device contains two power supply units: a standardized power supply unit BP113 and power supply unit BP123.

The power consumed from the system by each analog signal input device is no more than 150 V·A, including power to the plug-in interface block BKI-AV located in one of the processor bays.

The digital signal input-output device (UVD) is intended to receive signals from the digital sensors and to send digital and analog control actions to different mechanisms and the terminal devices.

The UVD has 12 modifications (Table 5.4).

The digital input-output function and also the analog output functions are realized by a set of functional modules: a digital signal input module (MVD), an initiating signal input module (MVI), a pulse signal input-output module (MVVI), a digital output module (MVD) and an analog output module (MAV).

Each of these modules, when installed in the plug-in control unit (BKU), has an output to the intraunit interface of the UVD which provides the efficiency of the modules in an arbitrary set in each BKU.

Table 5.4.

(1) Модификация УВД	Наименование и количество функциональных блоков (2)								(6) КР	(7) БКМ
(8)	(3) БКИ-ДВ	(4) БКР-ДВ	(5) БКУ-ДВ-0	БКУ-ДВ-1	БКУ-ДВ-2	БКУ-ДВ-3	БКУ-ДВ-4	БКУ-ДВ-5		
УВД-0	1	1	4	—	—	—	—	—	1	1
УВД-1	1	1	—	4	—	—	—	—	1	1
УВД-2	1	1	—	—	4	—	—	—	1	1
УВД-3	1	1	—	—	—	4	—	—	1	1
УВД-4	1	1	—	—	—	—	4	—	1	1
УВД-5	1	1	1	1	—	1	—	1	1	1
УВД-6	—	1	4	—	—	—	—	—	1	1
УВД-7	—	1	—	4	—	—	—	—	1	1
УВД-8	—	1	—	—	4	—	—	—	1	1
УВД-9	—	1	—	—	—	4	—	—	1	1
УВД-10	—	1	—	—	—	—	4	—	1	1
УВД-11	—	1	1	1	—	1	—	1	1	1

Key:
1. UVD modification
2. Name and number of functional units
3. BK-DV
4. BKR-DV
5. BKU-DV
6. KR
7. BKM
8. UVD

The UVD has the following specifications.

Through the digital signal input channels (MVD):

the maximum number of digital input channels in one self-contained complete unit is 256;

the input signal is a two-position type of positive or negative polarity;

there is optron galvanic isolation through each channel;

the input signal levels (logic "0"/logic "1") are, V: from 0 to $1.2/6 \pm 1.2$, from 0 to $2.4/12 \pm 2.4$, from 0 to $4.8/24 \pm 4.8$ and from 0 to $9.6/48 \pm 9.6$;

the maximum noise of general type is 100 V.

Through the initiating signal input channels (MVI):

the maximum number of initiating signal input channels in one self-contained complete unit is 128;

the type of input signal is a two-position initiating of positive or negative polarity (an interrupt signal is emitted with the sensor in a state from "0" to "1" or from "1" to "0");

the search of the module address that caused interruption is autonomous;

the maximum search time is 20 microseconds;

there is galvanic optron isolation through each channel;

the input signal levels are the same as through the digital signal input channels;

the maximum noise of general type is 100 V.

Through the number-pulse signal input-output channels (MVVI):

the maximum number of input-output channels in one self-contained complete unit is 16;

the maximum frequency of the input pulses is 15 kHz;

the length of the input pulses is not less than 10 microseconds;

the length of the output pulses is regulated in the range from 50 microseconds to 1 second with one-off time ratio of 2;

the maximum output voltage is 48 V;

the maximum load current is 0.2 A;

the capacitance of the counter is 16 digits (15 digits plus the sign);

the input-output operating modes are controlled by special jumpers.

Through the digital signal output channels (MDV):

the maximum number of digital output channels in one self-contained complete unit is 256;

the maximum output voltage is 48 V;

the maximum load current is 0.2 A.

Through the analog signal output channels (MAV):

the maximum number of analog signal output channels in one self-contained complete unit is 16;

the range of the output signal is 0-5 V and 0-5 mA;

the time required to establish an output signal with error of 0.1 percent is not more than 1 millisecond;

the nonlinearity error is not more than 0.2 percent.

There is a number of BKU modifications with different composition of functional modules:

BKU-DV-0--four functional digital signal input modules. It provides input of 64 parameters;

BKU-DV-1--four functional initiating signal input modules. The total number of input channels is 32;

BDK-DV-2--four functional pulse signal input-output modules. The total number of input-output channels is four;

BKU-DV-3--four functional digital signal output modules. The total number of output channels is 64;

BKU-DV-4p-four functional analog signal output modules. The total number of output channels is four;

BKU-DV-5--two functional analog signal output modules and two functional pulse signal input-output modules.

The UVD also contains two plug-in units: BKI-DV and BKR-DV. The BKI-DV provides information exchange between the UVD and the processor through the common bus and also automatic search of the initiating channel address (the channel that requires servicing); the BKR-DV realizes the capability of building up the digital input-output channels in the system.

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Communications plug and socket units are installed in the BKR which can be used to connect the expanding modification of the UVD (UVD-6--UVD-11) by means of a flat 1.5 meter communications cable located in the set of installation accessories of the UVD. The input-output system is further expanded by connection to the second third of the UVD device (in version UVD-6 and UVD-11) by a similar flat cable through the same communications plug and socket units.

Besides two plug and socket units, there are four BKR-BKU communications plug and socket units for external communications in the BKR by means of which the UVD bus is isolated to the BKU units.

The external cables of the user are connected by soldering to the functional input-output modules through a distributing frame device contained in the UVD. Each circuit should be completed by means of a wound pair of wires connected to the corresponding distributing frame contacts. The distributing frame consists of four distributing-frame cards with the capability of connecting 64 input-output channels to each one. The cards have continuous marking of channels.

Power is supplied to the device from a single-phase AC system with voltage of 220 V and frequency of 50 Hz. Two BP113 and BP123 power supply units are used in the device. Current consumption at the level of 5 V by all plug-in units of the device does not exceed 15 A for all versions of the device.

The main structure of the UVD is a self-contained complete unit (height of 9U) and a distributing frame panel (height of 1U).

The self-contained complete unit includes BP113 and BP123 power supply sources, blower units, a bus pack and network filter.

The distributing frame panels are connected by flat cables to the BKU-DV units (each card has one BKU unit).

A block diagram of the input-output system based on the UVD is presented in Figure 5.7.

Software of the Device for Communicating With the Facility (USO)

The software of the device for communicating with the facility (PO USO) is a set of programs to solve information gathering and processing problems from analog sensors and digital input-output signals, to check the efficiency and metrological characteristics of the analog signal input device (UVA), to check the efficiency of the digital signal input-output devices (UVD) and to localize malfunctions of USO hardware in automated production process and scientific experiment control systems operating in the control computer complex.

The programs for the PO USO are written in Assembler and operate under the control of the PLOS-RV operating system (except for the tests contained in the PO USO, which operate without an operating system).

The software contains:

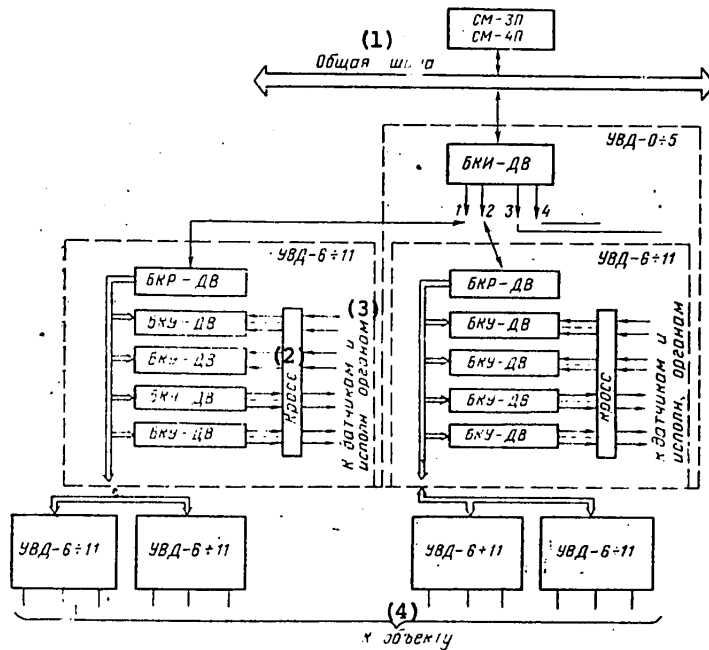Figure 5.7. Block Diagram of Input-Output System Based on Digital Signal
Input-Output Device

Key:

1. Common bus
2. Distributing frame
3. To sensors and actuating members
4. To facility

the program "Metrology of the UVA of the international small computer system;"

the program "Test VK1"--a test of the UVD controller;

test of the UVD modules;

user program LNMAS (linearization of nonlinear characteristics of sensors);

user program USRED (averaging of parameters);

user program USTAV (comparison of parameters to settings);

auxiliary programs;

UVA driver;

control problem of UVA driver;

UVD driver;

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control problem of UVD driver;

standard user problem.

The program "Metrology of UVA of international small computer system" is designed to check the analog signal input devices for functioning after they are installed at the manufacturing plant, to check the efficiency and metrological characteristics, to localize malfunctions of the analog signal input systems during acceptance-turnover and periodic trials and also for preventive checks during operation of the system. The program consists of four basic subroutines independent of each other which provide:

input and storage of input data in the memory to execute the program;

determination of the reliability of the measurement results with issue of the results of evaluation;

determination of the main error of the UVA measuring channel--(γ_0) with issue of the results of analysis;

determination of changes of the UVA readings with variation of external factors (γ) and temperature (γ_t) with issue of the results of analysis.

The program "Test VK1" checks the efficiency of the UVD controller for all functions performed by it.

The test of the UVD modules checks the efficiency of all varieties of functional modules of the UVD.

The set of software for the UVA and UVD is delivered to the user together with the equipment.

Configuration of Devices for Communicating With the Facility

The maximum possible composition of the apparatus of devices for communicating with the facility, serviced by a single digital input-output plug-in interface unit (BKI-DV) and a single plug-in analog input interface unit (BKI-AV), is shown in Figure 5.8.

The BKI-AV and BKI-DV units are located in the standard complete installation unit having its own power supply source of +5 V--BP113 and blowers and are installed in the processor bay or in the bay designed to include the interface units of the peripheral devices contained in the system.

Each of the BKI is designed to service up to four directions (four bays) (see Figure 5.8).

Since the UVD-0--UVD-5 modifications include a BKI-DV unit, only one of these modifications of the UVD is required for the entire digital signal input-output system. In similar fashion, the UVA-0 and UVA-1 contain a BKI-DV and therefore only one unit of these modifications is required in the analog signal input system.
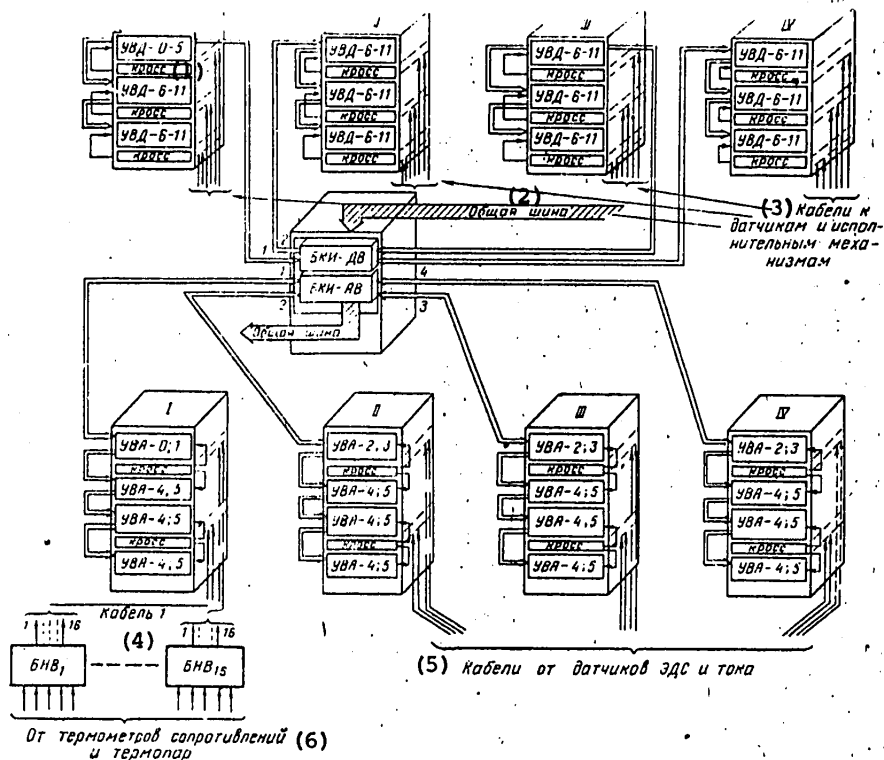
Figure 5.8. Design and Configuration of Devices for Communicating With
Facility of SM-3 and SM-4 Control Computer Complex: ⇒ --
logic communications; + --analog or digital input signals

Key:
1. Distributing frame
2. Common bus
3. Cables to sensors and acutating mechanisms
4. Cable 1
5. Cables from EMF and current sensors
6. From resistance thermometers and thermocouples

Each additional analog input bay of the UVA should contain either a UVA-2 or UVA-3 modification since these modules contain the analog-digital converter that services UVA-4 and UVA-5 modifications (containing only commutators and an amplifier).

The cables from the sensors approach from the pedestal and are attached along the lateral wall of the bays. The cable wires are then soldered to the distributing-frame cards.

Normalizing resistors for the current signals, additional filter capacitors (for example, for additional smoothing of rattles of the contacts from the digital sensors), fuses for the analog and digital output and so on may be located on the distributing frame cards.

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Since each UVA and UVD modification is structurally and electrically independent, they can be joined to each other in different combinations and can also be located in a single bay with any other peripheral devices. However, one should strive to arrange the units that perform analog signal input functions and also digital signal input-output functions close to each other.

The signal normalization units of the resistance thermometers and thermoelectric thermometers should be located at points of concentration of sensors, but not further than 300 meters from the UVA. Each BNV unit is designed to normalize signals from 16 sensors and consequently a maximum of four BNV may be connected to each UVA unit.

It should be noted that the bay does not contain any UVA and UVD modifications; therefore, any number of USO units is supplied in independent bays in specified SM-3 or SM-4 control computer complexes.

USO Configuration Based on Devices Having Output to Junction 2K

The presence of a common bus interface matching device and 2K-USS OSh/2K interface in the SM-3 and SM-4 nomenclature permits the use of the entire nomenclature of ASVT-M (M-400, M-6000 and M-7000) and SM-1 and SM-2 devices and modules having output to the 2K interface as devices for communicating with the facility.

The nomenclature contains:

low- and medium-level analog signal input devices (noise-protected UVAS-2 and high-speed UVAS-1);

digital signal input-output device (UVVDS);

relay output device (UVR);

high-speed analog signal input device (UVB-100);

a set of modules from the SM-1 and SM-2 nomenclature.

The set of modules for the SM-1 and SM-2 includes analog-digital converter modules, commutators, sampling and storage circuit modules, normalization modules, filtration and galvanic isolation modules, initiating and number-pulse signal input modules and digital and pulse-signal output modules.

Systems for communicating with the facility, different by the number and type of channels, can be configured from the USO modules connected through the USS-OSh/2K junction matching device.

The interface unit (USS BI) provides installation in it of up to 16 USO modules and interface cards of external devices. Each location on the 2K junction in the USS-BI is equivalent to independent connection of the module to the common bus of the complex with servicing through the program channel and through the direct access channels to the memory of the complex.

The number of locations on the 2K junction can be increased by connecting inter-face expanders USS-OSh/2K-1 (USS RI).

The USS-OSh/2K device permits connection of up to eight expanders. Connection of each expander occupies two locations of the 2K junction in the USS BI, offering 16 locations for installation of the USO modules.

A block diagram of organizing communications with the facility is presented in Figure 5.9.
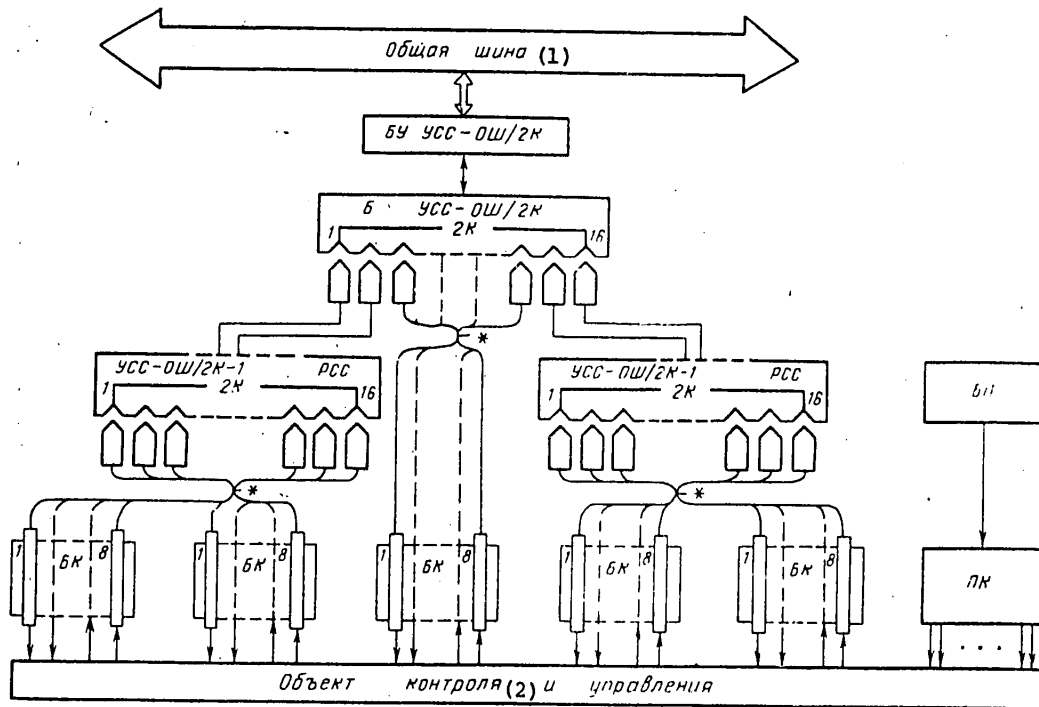

Figure 5.9. Block Diagram of Organizing Communications With Facility
(*--strand; Δ --USO interface module, junction 2K; ▢ --USO normalization module, distributing frame receptacle; RSS--USS OSh/2K expander--BP--distributing frame power supply unit; PK--distributing frame panel; BK--distributing frame unit)

Key:
1. Common bus
2. Monitoring and control facility

The minimum systems for communicating with the facility by equipment composition can be formed from the USS-OSh/2K device installed on the free locations of the bays of the SM-3 and SM-4 control computer complexes and the required number of USO modules.

We recall that the USS-OSh/2K device consists of two units--a control unit (USS BU) and interface unit (USS BI), each of which occupies 6U (U = 44.45 mm) along the height of the bay.

Direct, independent connection of 2K modules to the common bus of the complex means that each module (location of 2K) is represented directly by the instruction and state register (RKS) and data register (RD) address in the program.

Multiple use of USO modules is feasible with structural disposition of USS-OSh/2K and USS-OSh/2K-1 in a separate bay or group of bays equipped with distributing head units and power supply system for external circuits--the ST2 bay (ST2/1-ST2/3).

To reduce the number of individual converters and communications lines at territorially dispersed facilities, portable group commutators and converters, for example, group measuring converters (A614-1 and A614-2), current and voltage signal commutators (A612-115), digital signal commutators (A622-10) and an output commutator (A641-15), may be used.

The portable group converters and commutators and information input are controlled by program through the USO modules.

Portable USO (from the nomenclature of the SM-1 and SM-2 control computer complex) may be used if the control computer complexes are remote from the facility (up to 3 kilometers). Multiplex interface splitters A714-5/1 (RIM-1) and A714-5/2 (RIM-2) are used for this purpose.

The RIM-1 splitter can be connected to SM-3 and SM-4 control computer complexes through USS-OSh/2K. The RIM-2 splitter is an RIM-1 splitter. Sixteen each interface units can be installed in the RIM-1 and RIM-2 splitters.

The RIM-1 splitter permits one to connect the 2K junction to two leads and the devices of the SM-3 and SM-4 control computer complex to two common bus mainlines (through the bus switch). This capability provides creation of redundant control computer systems and also multimachine complexes with common peripheral equipment.

5.4. Operating Conditions of the Complex

Complexes configured from hardware of the international small computer system should be operated under conditions corresponding to GOST 20397-74 for articles of group 3b having direct contact with the external medium.

The limiting operating conditions of the complex are as follows:

Climatic Factors	Maximum Variation of Factors	
	Lower	Upper
Temperature, °C	+10	+35
Relative humidity at +30°C, percent	--	90
Atmospheric pressure, mm Hg	735	785

An industrial single-phase AC system (220 V and 50 $\pm$ 1 Hz) is used as the main primary power supply source. Smooth and intermittent variations of voltage of +10 $\pm$ $\pm$ 15 percent from the nominal are permitted.

The complexes should be installed in dry heated buildings. The height of the ceilings in the building is not less than 3 meters. The ceiling and walls should be covered with sound-absorbing materials of light tones. Coating with whitewash is not permitted.

Louvers or drapes should be provided in the window sashes.

The use of combustible and flammable materials is not permitted during construction and finishing of buildings. Automatic fire signalling should be provided.

Lighting is fluorescent or incandescent bulbs with diffusion device. The lighting is not less than 150 luxes at a height of 0.8 meter from the floor. The lighting of operator's positions and keyboards is 350-400 luxes. Emergency lighting from a separate power source must be provided.

An area of not less than 15 m^2 is required for arrangement of the SM-3 and SM-4 complexes and an area of not less than 10 m^2 is required for the auxiliary equipment.

An insulated production floor that prevents the accumulation of static electricity should be provided if possible. The degree of electric charge build up of the coating should provide a charge leakage time of not more than 30 seconds.

The production floor is calculated for a load of not less than 300 kg per slab. The recommended slab dimensions (nonmetallic or metallic) is 650 X 650 mm. The space between the production floor and the floor is not less than 208-250 mm in height. If a production floor cannot be installed, cable channels protected from above by wooden panels must be provided.

The composition of the service personnel depends on the organization (for example, centralized maintenance) and shift schedule of maintenance.

With three-shift uncentralized maintenance, the approximate composition of the maintenance personnel is as follows:

Position	Specialty	Number According to Position
Chief	Engineer and specialist in computer equipment	1
Duty officer	The same	2
Technician	Technician in computer equipment	1
	Technician in precision mechanics	1
Programmer	Engineer-programmer	*
Operator	Technician	2-3

*The number of programmers is determined by the nature and number of problems to be solved.

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With one-shift centralized maintenance, the user may not have his own personnel. The duties of the personnel are as follows:

Position	Main Functions
Chief of complex	Provides operation of complex. Manages the maintenance personnel of the complex
Duty engineer (shift chief)	The shift chief performs the same functions as the computer chief, only with respect to a single shift of a production cycle; he participates in management of preventive maintenance work and finding and correcting malfunctions in the complex
Technician	Participates in maintenance work and finding and correction of malfunctions in the complex, he checks and repairs power supply sources and logic and special units and ensures operation and repair of electromechanical devices
Programmer	Makes corrections to working programs, prepares new problems for solution and participates in debugging of new problems and preventive checks of the system
Operator	Switches the devices of the machine on and off. Participates directly in information processing on the machine according to the "Instructions of the system operator" and performs all activities required in solution and debugging of problems

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PROBLEM-ORIENTED COMPLEXES BASED ON THE INTERNATIONAL SMALL COMPUTER SYSTEM .

Moscow MALYYE EVM I IKH PRIMENENIYE in Russian 1980 (signed to press 14 Aug 80) pp 215-229

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[Text] 6.1. Computer-Measuring Complexes

Modern scientific investigations and bench test using complex equipment usually cannot be carried out without the corresponding automation systems based on com-puter equipment. Practice shows that small and microcomputers which can be con-nected to highly productive computers as terminal stations if the computer capacity must be increased may be used for the laboratory experiment and test automation system.

Depending on the type of test and experiment automation systems, the following functions may be entrusted to small computers:

recording of experimental information in real time and subsequent processing of it;

control of the experimental installation at the step of adjusting it for a given mode;

control of the experimental process from the results of information process-ing according to the decision-making algorithms;

transmission of experimental information for complex processing in an upper level computer and reception of the results of processing;

supporting the work of the experimenter with symbolic and graphical informa-tion in dialogue mode with the computer;

performing the role of a controller or concentrator in multimachine hierarci-cal systems for automation of scientific research and tests.

Experiment and bench test automation systems have a number of characteristics compared to automated systems of other classes, for example, ASU TP. They usually have significantly fewer measuring and control channels than ASU TP, but the range of signals to be measured is higher frequency and the requirements on the speed, accuracy and digit capacity of the converters of the signals to be measured are higher. Complex experimental installations (wind tunnels, plasma, nuclear and other installations) on which experiments of different layout are conducted require the presence of flexible, adjustable devices for integration of the experimental equipment with the computer and a set of analog, pulse, code and other signal input-output modules with different characteristics.

Integration of the computer with the experimental apparatus can be achieved on the basis of hardware made in different standards. However, the CAMAC system* has become widespread in worldwide practice, including in institutes of the USSR Academy of Sciences. As is known, CAMAC has an aggregate of standards for logic, electrical and structural realization of the integration device and information exchange between the measuring equipment and the digital controller. The controller can be made in the form of a self-contained functioning device or in the form of an interface between the CAMAC system and the computer. Thus, the CAMAC system is not oriented toward any specific type of computer, but may operate with different types of computers in the presence of the corresponding controllers.

CAMAC has a modular structure that permits rapid composition of different configurations of the integration device for experimental equipment. Structurally, the system is made in the form of a self-contained unit (crate) that is a chassis with power supply source and 25 setting positions for the modules having 86-contact plug and socket units. The dimensions of the front panel of the module that occupies one setting position is 221 X 17.2 mm. The first 23 positions are intended for connection of the CAMAC functional modules and the 24th and 25th positions are allocated for the CAMAC crate controller. The crate controller, which communicates with the computer, permits control of the functional modules of the computer. The functional modules are arranged in arbitrary setting positions of the crate. Complex modules may occupy two or more positions.

Computer-Measuring Complexes Based on Devices of the International Small Computer System and CAMAC

An extensive program of operations provides for development and circulation of standard computer-measuring and control complexes oriented toward automation of scientific experiments on the basis of devices of the international small computer system and CAMAC devices.

Let us consider the main characteristics and designation of computer measuring complexes of the first unit.

IVK-1 and IVK-2 complexes are the hardware and software base for design of systems for automation of various experiments of general physical profile. The control

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*
CAMAC--computer application for measurement and control.

computer part of the IVK-1 and IVK-2 is constructed on the basis of SM-3P and SM-4P processors, respectively.

The basic composition of the IVK-1 computer equipment includes an SM-3P processor, internal storage with capacity of 28K words, combination papertape input-output device, external magnetic disk storage with movable heads having capacity of 2.4M words on the basis of the IZOT 1370 storage device, an alphanumeric operator terminal on the basis of the VT-340 or VTA-2000 display and a wide-printing character-synthesizing device (DARO-1154 or DZM-180).

The basic composition of the IVK-2 computer equipment is distinguished by a larger SM-4P processor, increased capacity of the internal storage (up to 64K words) and external magnetic disk storage (up to 4.8M words), IZOT 5003 external magnetic tape storage and SM-6315 small high-speed wide-print device.

Two crates each with crate controllers whose configuration permits up to four parallel-connected crates in the complex are used as CAMAC devices in the IVK-1 and IVK-2. The set of modules of each crate includes the following functional modules:

a 9-digit analog-digital converter with maximum conversion time of 12 microseconds that permits measurement of both pulses of less than 1 macrosecond and variable voltage with maximum quantification frequency of 50 kHz;

analog signal commutator for 32 inputs;

four 24-digit input registers;

initiating signal input register for 24 inputs;

four 24-digit output registers;

10-digit digital-analog converter for two outputs with maximum conversion time of 10 microseconds;

a 16-digit pulse counter for four inputs that permits pulse counting at maximum frequency of 15 MHz with minimum width of 40 nanoseconds;

pulse generator with frequency from 1 Hz to 1 MHz, also capable of performing the role of decade frequency divider;

teletype communication module.

The crate also includes a set of service and mock-up modules.

Structurally, the IVK-1 is formulated in the form of two and the IVK-2 is formulated in the form of three standard bays of the international small computer system with two CAMAC crates built into one of the bays and a separately located operator terminal and wide-print device.

The IVK-3 complex is problem-oriented toward automation of experiments conducted by using optical spectral devices in different fields of science (physics,

chemistry, biology, medicine, metallurgy and so on). The composition of the IVK-3 computer equipment compared to the IVK-1 computer equipment is supplemented by a two-coordinate graph plotting board with working field dimensions of 200 X 300 mm. A crate that includes a controller and the following set of functional modules is used as the CAMAC devices:

a 14-digit analog-digital converter with conversion time of 2 milliseconds;

a 9-digit analog-digital converter with conversion time of 12 microseconds;

a relay commentator for 32 analog channels;

two 2-channel 10-digit digital-analog converters with conversion time of 10 microseconds;

two step motor control modules;

two 24-digit pulse counters with maximum counting frequency of 20 MHz;

four 24-digit input registers;

four 24-digit output registers;

a 24-digit initiating signal input register;

a timer-synchronizer;

a digital ampere-voltmeter control module.

Moreover, there is a set of CAMAC service and mockup modules.

The IVK-3 also includes a digital ampere-voltmeter with switching of the measuring range having conversion frequency of 5 Hz and display scale of measured values (six decimal digits).

The IVK-3 complex is structurally formulated in the form of two standard bays of the international small computer system with built-in CAMAC crate and self-contained printers, alphanumeric display, graph plotter and digital ampere-voltmeter.

The IVK-4 complex is designed for automation of complex laboratory experiments. The basic composition of the computer equipment contained in the IVK-4, compared to the IVK-2, also includes a graphical display (EPG SM), drum-plotting board graph plotter and common bus switch (SM-4501). The bus switch is an intersystem communication device that permits construction of multimachine complexes with two common, time-sharing processors, any external devices (including external storage devices) or hot redundancy of devices (including the processor) in multimachine complexes.

The CAMAC devices included in the IVK-4 include three crates, two of which contain a set of modules the same as in the IVK-2 and IVK-3, while the third is supplied with a crate controller and mockup cards that offer the user the capability of developing his own specific CAMAC modules not produced by industry.

The IVK-4 includes and F7046 voltage calibrator and Shch1516 digital voltmeter to calibrate and check the measuring modules.

All the IVK undergo metrological testing according to the methods confirmed by the State Standard and are metrologically certified.

The basic software of the IVK includes a number of standard SM-3 and SM-4 operating systems and applied program packs oriented toward various scientific calculations. The operating and servicing program systems of the IVK include:

a general-purpose disk operating system DOS SM designed for a single user and that permits creation, debugging and execution of programs written in Assembler and FORTRAN-4 languages in the pack mode;

a real-time multipurpose operating system DOS RV with fixed number of priority levels;

a real-time multipurpose operating system OS RV SM that provides a real-time multiproblem mode and also servicing of background problems in the multiterminal pack and (or) dialogue mode;

a basic background-operating system (FOBOS) that is a high-response compact system oriented toward laboratory experiments and that permits real-time execution of one problem and execution of another problem in the background accounting or debugging mode;

hardware for real-time operation with CAMAC apparatus using FORTRAN-4 language;

a test program pack to check the efficiency of the IVK and of its individual components.

IVK Based on the International Small Computer System and ASET

Soviet industry produces IVK in which the measuring and conversion devices that link the experimental equipment to the computer are executed in standard unit electrical measuring equipment (ASET) (IVK-7 and IVK-8).

The IVK-7 and IVK-8 are designed for switching, amplification, measurement and recording of DC voltage signals, programmed gathering, storage and processing of information and delivery of control actions and can be used as a basis for designing experiment1 automation systems in different fields of science and technology.

The complexes provide the following functional capabilities:

preliminary processing of measurement results;

obtaining the results of indirect, aggregate and joint measurements, including those in real time;

functional control of individual units during an experiment, including or-
ganization of requests and lines and establishing priorities and a dialogue mode
with the operator;

monitoring the efficiency of the units and channels of the complexes, includ-
ing its metrological characteristics;

service processing of received information (presentation of the results in
the form of tables, graphs and so on);

storage of the received information and creation of data files;

generation of control actions on the object under investigation (in the form
of analog and/or digital signals).

The functional capabilities are realized by software and algorithmic support de-
livered with the complexes.

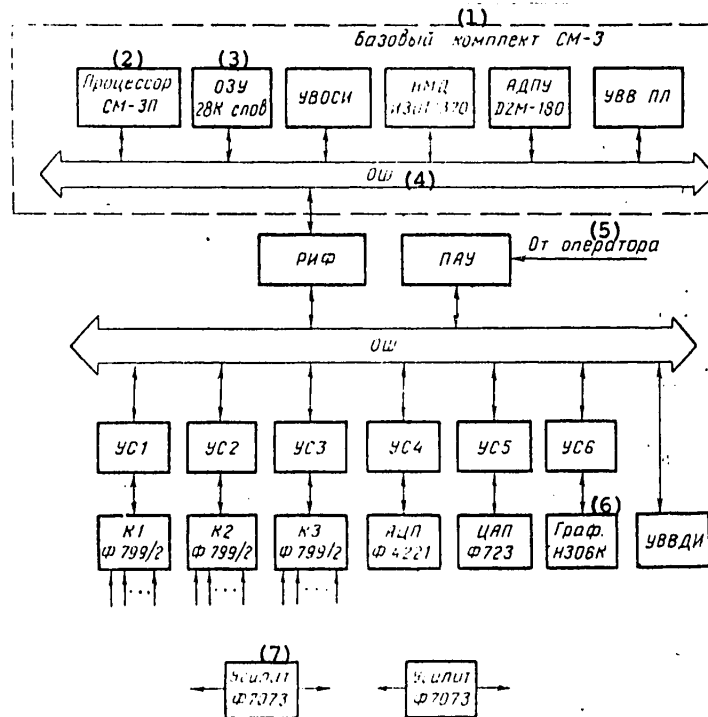Block diagrams of the IVK-7 and IVK-8 are presented in Figures 6.1 and 6.2.

Figure 6.1. Block Diagram and Composition of IVK-7

[Key on following page]

[Key continued from preceding page]:

1. Basic set of SM-3
2. SM-3P processor
3. Internal storage with capacity of 28K words

4. Common bus
5. From operator
6. N306K graph plotter
7. F7073 amplifier

The IVK-7 and IVK-8 complexes are constructed on the basis of the SM-3 control computer complex, which includes an SM-3P processor, internal storage with capacity of 28K words, a cathode-ray tube symbolic information input-display device (UVOSI), sequential type alphanumeric printer (ATsPU) on the basis of the DZM-180 mechanism and magnetic disk external storage based on the IZOT 1370 store with capacity of 4.8 Mbytes.

All the measuring and peripheral devices of the ASET included in the IVK are combined by a single signal system and unified high-frequency high-speed mainline communications channel—standard "common bus" (OSh) interface.

Let us consider how the peripheral (PU) and measuring devices in the standard ASET (subsequently the PU) are connected to the SM-3 control computer complex.
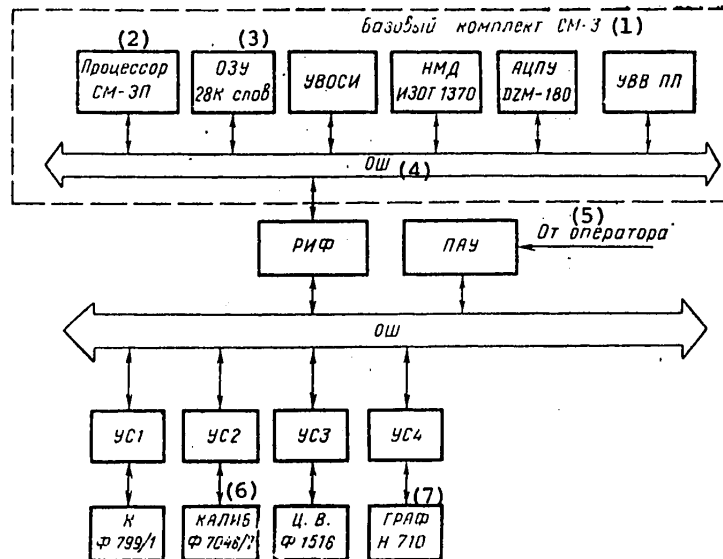

Figure 6.2. Block Diagram and Composition of IVK-8. The notations in Figures 6.1 and 6.2 are: (PAU—autonomous control panel; US—integration device; K1, K2 and K3—analog signal commutators, ATsP—analog-digital converter; TsAP—digital-analog converter; UVVDI—digital information input-output device; graf—graph plotting board; USILIT.—voltage amplifier; TsV—digital voltmeter; KALIB.—calibrator)

[Key on following page]

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[Key continued from preceding page]:

1. Basic set of SM-3	4. Common bus
2. SM-3P processor	5. From operator
3. Internal storage with capacity of 28K words	6. F7046/7 calibrator
	7. N710 graph plotter

The peripheral devices are integrated with the central processor of the SM-3 complex by means of integration devices (US). Structurally, the integration devices are grouped into a single unit--the systems interface unit (BSI). Each integration device consists of a selector (identical for all peripheral devices contained in the complex) and driver (different for each peripheral device) cards. Control signals, the addresses of the device and a synchronous signal for decoding the control information, which is used in the driver card to generate control signals by the registers and peripheral device, are fed to the selector card from the common bus mainline.

A common bus expander (ROSh), which relays signals without inversion over single- and two-directional lines with a delay not exceeding 350 nanoseconds, is used for communication of the BSI with the common bus mainline. The common bus expander divides the interface mainline into independent segments with identical capabilities, being the load on each mainline per standard load unit and increasing the load capacity of the mainline by 19 load units and the cable length by 15 meters. The principle of using the common bus expander permits a configurational increase of the number of peripheral devices of the complex without limit. The complex has an autonomous control panel (PAU) designed to check the functioning of the selector and driver cards in the static mode (without connection of the SM-3).

The following measuring channels (structural connections of the units) can be realized in the IVK-7: amplifier-commutator--analog-digital converter, commutator-amplifier-commutator--analog-digital converter, commutator-commutator--analog-digital converter, commutator--analog-digital converter, analog-digital converter and digital-analog converter (by output analog signals).

There is a method of determining the individual metrological characteristics which permits the user at the acceptance-turnover trials and also prior to conducting a crucial experiment to determine the true metrological characteristics of the realized measuring channels.

The number of commutated channels of the complex is 298, of which 100 channels have an input signal range of $\pm$ 100 mV, one channel has an input signal range of $\pm$ 10 mV and 197 channels have an input signal range of $\pm$ 10 V.

The speed of the measuring channels of the IVK-7 may reach 5 kHz with appropriate organization of the software (peripheral device control programs) and the apparatus speed of the complex (without regard to software) comprises approximately 8,000 measurements per second.

The characteristics of the analog output signals are output DC voltage range of +10 V and time required to establish output voltage of not more than 100

The output signals of the digital information input-output device provide control of eight relay devices and four step motor channels at TTL signal levels.

Power is supplied to the complex from an AC system with voltage of 220 V ± 10 percent and consumed power is no more than 4 kW. The area required for location of each complex is no more than 25 m^2.

Structurally, the complex consists of bays of the basic set of the SM-3 and measuring bays based on standardized designs (UTK) of type KZSSZ-8UZ. All the functionally complete units and peripheral devices of the IVK-7 are located in two bays of the UTK by levels. Two F7073 amplifiers, an F4221 analog-digital converter, an F723 digital-analog converter and systems interface unit are located in the first bay and three F799/2 commutators and an N306K graph plotter control device are located in the second bay and the plotting board of the N306K graph plotter itself is located lower on an extensible desk at a height of 700 mm from the floor level.

The IVK-8 complex provides programmed commutation of DC electric signals, digital measurement of DC electrical signals, data recording, plotting of graphs and functions, emission of DC electric signals and gathering, storage and processing of measurement results.

The number of commutated channels of the complex is 100. The number of simultaneously connected lines in the channel is three or six. The range of commutated voltages is ± 10 V. The time of a single measurement for the commutator-digital voltmeter structure is not more than 50 ms ± 2 percent or 410 ms ± 2 percent without a filter (4 seconds with a filter).

The maximum permissible permissible main reduced error for commutator-digital voltmeter structure with sensor resistor equal to zero and input signal level of ± 10 V is not more than 0.1 percent.

The characteristics of the input signals are output DC voltage range of ± 9.99999 V, output voltage subrange of ± 0.1, ± 1.0 and ± 10 V, number of discrete values in each subrange of -10^6 and time required to set output voltage of not more than 10 ms.

The operating conditions of the complex, the power supply and reliability characteristics are the same as for the IVK-7.

The IVK-8 consists of an SM-3 control computer complex, measuring bay of KZSSZ-8UZ standard design and N710 graph plotter with control bay.

The measuring bay includes an F7046/7 commutator, systems interface unit, power supply source of +5 V, autonomous control panel and set of connecting cables.

The systems software of the complexes is realized on the basis of the revised expanded version of the dialogue system (DS SM) with input language of Focal type. The input language of the dialogue system is supplemented by control operators of the effective area of variables and procedures, which permits the user to create large programs on the unit-modular principle. Moreover, control functions and exchange of measuring and peripheral devices with the central processor of the SM-3 are introduced. There are programs to determine the individual metrological

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characteristics of any channel for each of the realized structures for connecting the units. The software delivered with the IVK also includes an assembler, debugger and editor. The software of the complexes is delivered on papertape.

6.2. Automated Operator's Positions

Two types of computer complexes intended for design automation are produced serially: an automated electronics equipment designer's position (ARM-R) and an automated machinebuilding designer's position (ARM-M). These complexes are designed on the basis of small computers of type SM-3 (SM-4) and include a wide range of external devices that provide effective processing of text and graphical information.

The ARM-R complex includes the following devices:

processor (SM-3);

internal storage with capacity of 28K 16-digit words;

complex expansion device (URK);

FS-1501 papertape input device;

PL-150 papertape output device;

AP-6100 punch card input device;

IZOT 1370 (SM-5400) magnetic disk store;

AP-5080 magnetic tape store;

Videoton-340 (SM-7206) alphanumeric display;

EPG-SM graphical display;

AP-7252 drum graph plotter;

EM-709 graph information coder;

DZM-180 (SM-6302) alphanumeric printer;

device for communicating with the unified computer system (M-4030) USVM.

The ARM-M complex, besides the EPG-SP graph display, includes the UPGI graph display, an AP-7251 board graph plotter instead of a drum graph plotter and a PKGIO coder instead of an EM-709 coder.

Basic software, which is common for the ARM-R and ARM-M and which contains DOS-400 and DOS-ARM operating systems, TESARM test system, graph program system and data preparation system for machine tools with numerical program control, is delivered together with the complexes.

The basic software of the ARM offers the user a wide range of capabilities required when solving various design problems. The user may:

solve up to four different problems simultaneously;

enter drawings into the machine and review drawings that have been entered;

consider any fragments of drawings in magnified scale;

correct drawings;

create archives of drawing descriptions on disk and gain access to these drawings by name;

enter and edit textual materials;

obtain the final results of design in the form of drawings and text printouts;

prepare punchtapes for control of machine tools with ChPU [Numerical program control];

develop new user programs.

Thus, the basic software is the basis for creation of problem-oriented applied program packs by head institutes in different sectors of industry that permit solution of the specific problems of each sector.

Development of these packs should be accompanied by development of new organizational methods and new design techniques oriented toward the use of means of automation.

The process of man-machine interaction is accomplished on the basis of graphical images for the problems of many classes, especially design problems and those for developing manufacturing techniques. The designer presents his ideas by drawings or sketches and the final results of the design are also represented to a significant degree in the form of drawings. Therefore, this graphical "conversation" with the machine is more laconic and effective. The capabilities of this interaction are offered to the user due to the presence of a graphical display, graph plotter and drawing input device (graphical information coder).

The graphical display is supplied with alphanumeric keyboard for the set of instructions or texts, a functional keyboard, pressing of each key of which induces the specific response of the system, and a light pen that provides the greatest convenience for maintaining an interactive mode.

Part of the image (an individual component at the same level of structural hierarchy, for example, the image of a building facade, window or air vent) can be identified by means of the light pen, an operation can be selected from the set of given operations (for example, construction of a point, segment, broken arc, circle and so on) for acting on the selected object (light buttons), an object from a

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set of given objects can be selected (a set of standard graphical images) and a new object can be obtained by moving the light pen (drawing lines by hand on the display screen).

The automated operator's positions are used to solve the following classes of problems:

problems that require comparatively simple calculations (on the order of 30 minutes in length), especially problems, the result of which are graphical images;

problems of the type of arranging standard components on a plane (arrangement of equipment in a shop, configuration of a printed-circuit card, compilation of a block diagram or network schedule, pattern layout and so on). The descriptions of images of standard components are previously recorded in a special library. The disposition is illustrated by the image on the graphical display screen;

problems, solution of which are iterative in nature, and the criterion of quality is not exactly determined. In this case the operator, who enters corrections in the program parameters and awaits the results of the next iteration, finally evaluates the quality of solution. Problems of routing a printed-circuit card and different optimization problems can be constructed by this type;

problems related to periodic introduction of slight changes into complex drawings. The changes can be entered both by program and manually by means of a graphical display or by the graphical information coder;

problems related to periodic introduction of changes in textual materials;

data preparation for machine tools with numerical program control;

development and debugging of applied programs.

Further development of ARM will be carried out to improve theoperating characteristics such as the cost of calculating a single operator's position, expanding the set of functions carried out, increasing reliability, convenience and speed of work and providing the capability to install portable consoles directly at the designers' positions. Development of group ARM consisting of a central complex based on the SM-4 control computer complex with internal storage of 128K words and large-capacity magnetic disks and also a set of devices for retrieving the results of design and a number of terminal stations connected to the central complex by allocated telephone lines, is being carried out for this purpose. The terminal stations include interactive devices and simplified drawing and printing devices and are controlled by mini- or microcomputers of the SM EVM series. The software of group ARM should provide the multiprogram mode of the complex with the capability of autonomous operation of the terminal stations.

Among the POK oriented with the problem of designing complex objects, complexes that provide multiconsole dialogue and high coefficients of filling drawings of comparatively large area are promising.

These complexes can be used during design in cons⁺ruction, machinebuilding, electrical engineering and electronics.

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The POK contain the following hardware:

an SM-4 complex with internal storage up to 128K bytes;

from one to four wide-format graph designer screen consoles with screen dimensions of 350 X 350 mm and with specialized display processor that performs a number of editing operations independently of the computer;

from one to four semi-automatic plotting board devices for entry of graphical information into the computer on the basis of a specialized processor that performs the functions of preliminary monitoring and conversion of encoded information;

a graphical information output device.

The software contains:

a real-time operating system and methods of access (program drivers) that accomplish logic connection of the devices to the operating system;

programming devices that control the operation of terminals and that exchange data between the devices and the main files of the system.

The software permits servicing of initiating devices, maintenance of multiconsole dialogue, formation and processing of archive data and conversion of graphical information (for editing and processing of graphs in the dialogue mode).

As universality is reduced, the software can be divided into three levels:

1) driver-programs that accomplish logic connection of nonstandard devices to the real-time operating system OSRV;

2) equipment programs that control the operation of terminals and that exchange data between devices and the main files of the system. They support execution of the following main functions:

servicing the requests of graphical terminals, distribution of them between corresponding dispatchers and transmission to the required program sections for execution;

organization of a data base (systems archive) with high speed of search, reading and writing of the required information;

formation and processing of library data that include description of text and graphs;

maintaining information contact between graphical devices and the main system files;

conversion of graphical information for editing and processing of graphs in the dialogue mode.

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Thus, the second-level software permits entry of a description of different graphical objects into the system archive by means of one or several encoding devices, offering parallel with this the capability of editing by means of displays previously formed objects (including those designed automatically). The operator maintains a dialogue with the system in the directive language, by means of which a "window" can be summoned to the screen (part of the image in magnified scale), image quality can be improved, the library element can be summoned and so on and he can also gain access to the applied program;

3) applied program packs oriented toward a specific type of design objects and class of problems to be solved. The number of packs should be expanded as the sphere of use of the system is expanded.

The composition of hardware of standard PK based on POK may be as follows:

Name	Cipher	PK1	Number in Complex		
			PK2	PK3	PK4
SM-4P processor	SM-2104	1	1	1	1
Internal storage (UOP-16)	SM-3102	4	4	4	4
Analog-digital converter	SM-6315	1	1	1	1
Symbolic information input and display device	SM-7204 (SM-7205)	1	1	1	1
Papertape input-output device	SM-6202	1	1	1	1
External storage based on IZOT 1370-I12	SM-5301	1	1	1	1
Wide-format graph screen designer console		1	2	3	4
Semi-automatic plotting board for conversion of graphical information to digital code		1	2	3	4

Standard requests and editing time of the PK are:

requests for input and output of graphical information to graph devices and for conversion of graphical information;

requests related to access to the data archive and library;

requests related to execution of applied programs oriented toward classes of design objects.

Requests are divided by response time into three groups:

a) operations of conversion (editing) of graphical information executed on the display without access to the computer--response time of less than 50 ms;

b) short directives--response time of 2-10 seconds;

c) long directives (execution of which is interrupted upon the occurrence of short directives)--response time of 10 seconds to several minutes.

Analyzing the promising directions for developing the problem orientation of the international small computer system, it should be noted that the effectiveness of wide application of POK of the international small computer system is determined:

by improving hardware and software of the international small computer system;

by developing a rather wide range of methods of developing both the POK themselves and of user complexes based on POK in the main classes of applications of the international small computer system;

realization of an extensive program for developing a sufficiently complete set of POK for expanded areas of application of the international small computer system.

With regard to development of the hardware of the international small computer system, the feasibility of expanding the classes of processors, development of the nomenclature of peripheral devices, increasing the types of intrasystem and intersystem communications adapters, including adapters for communicating with the unified computer system, Elektronika-60 computer and so on, should be emphasized. The nomenclature of SM EVM processors can be expanded up to four classes, including microprocessors and microcomputers (for individual applications in small units as components of local automatons, intellectual devices for communicating with the facility and intellectual terminals, peripheral processors, computer cells of distributed systems and so on), small computers with improved technical and economic characteristics (expansion of the internal storage capacity to 2-4 Mwords, increasing the effective speed of executing the most widespread algorithms or systems subroutines), mega- and minicomputers (for upper levels of hierarchical control systems and dispatcher and information systems) and special processors (for realization of standard algorithms or classes of algorithms), can be expanded to solve the entire variety of problems of mass computer application.

Combining these classes of processors into a unified family should be achieved on the basis of principles of sufficiently extensive compatibility that provides operation of them in unified multiprocessor and multimachine complexes, including network structures and structures with remote access and distributed computer capacity.

The nomenclature of peripheral devices of the international small computer system may be developed both in the area of expanding the classes of devices (graph plotters, raster displays, operator consoles, external high-response stores and with volume of not less than 100-200 Mbytes and so on) that provide an increase of effective solution of user problems and by additional systems devices for interprocessor and intermachine communications. Because of this, the scales of work to develop problem-oriented complexes can be significantly expanded for such applications as preparation of production, automation of programming, design automation, multiple control of machine-processing sections, multiple shop systems, warehouse control systems and systems for nonindustrial applications.

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