LogiCore® Orion System Logic Chipset

Standard Features

- ❑ Support IDT's R4400, R4600 and R4700 RISControllers
- ❑ Capable of running processors at 100 MHz, 133MHz, and 150MHz
- ❑ Supports up to 256MB of main system memory
- ❑ Supports scalable secondary cache (0-2Megabytes)
- ❑ Supports ISA, EISA, VESA and PCI peripherals
- ❑ Compatible with existing desktop, mini-tower and full-size chassis
- ❑ Design kits include:
  - — Complete schematics, gerbers, PAL equations, BOM, AVL and design guides
  - — Complete BIOS binaries
  - — HAL modifications

CPUs Supported

R4400, R4600 (Orion), R4700

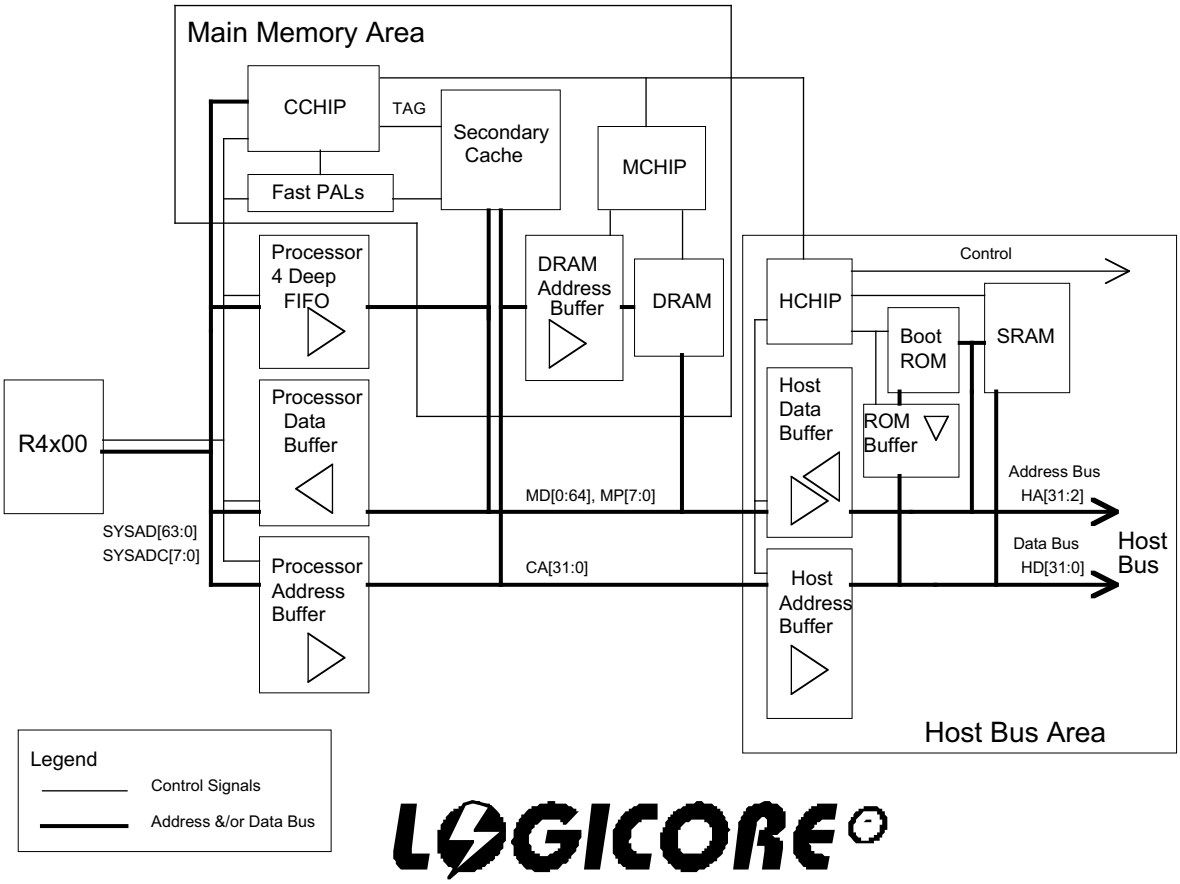
Host Platforms

Now Intel-based PC and embedded system manufacturers have the opportunity to enter the emerging high-performance RISC market with little R & D investment. DeskStation Technology, Inc. provides advanced system technology to enable and enhance high-performance RISC-based systems. A system built upon DeskStation's LogiCore chip set will support 64-bit MIPS processing power running at clock speeds of up to 200 MHz while maintaining compatibility with industry-standard PC components.

The LogiCore architecture features true scalability and flexibility for system designers. The chip set includes a cache-controller chip, a memory-controller chip and a bus-interface chip tied together through a high-bandwidth custom bus. The chip set will support the R4400, R4600 and R4700 IDT RISControllers running with internal clock rates of up to 200 MHz. The bus interface chip produces a 486 processor bus that can be connected to local-bus devices or, through standard PC bridges, to ISA, EISA or PCI peripherals.

DeskStation's LogiCore architecture supports up to 2 megabytes of secondary cache and 256 megabytes of system memory. The 128-bit cache controller allows for the use of the much lower-priced R4x00 PC (Primary Cache) CPUs while delivering the same secondary cache performance as that achieved by the more expensive R4x00SC (Secondary Cache) based systems.

DeskStation's LogiCore architecture has a scalable secondary cache that can be configured at the time of assembly with as little as 0kilobytes or as much as 2 megabytes using 25nS 128K x 8 static RAMS. The main memory can be configured with a single 16 megabyte, 70nS SIMM (organized as 4M x 36). The motherboard is compatible with existing desktop, mini-tower and full-size chassis.



LOGICORE®

Overview

The LogiCore chip set is designed for use in a workstation product that uses a R4600 or R4400 processor. The chip set provides the signals necessary for interfacing to DRAM, boot ROM, a VESA local bus and industry standard peripherals, and an optional secondary cache.

The chip set consists of three chips named CCHIP, MCHIP and HCHIP. CCHIP controls the secondary cache, processor address and data buffers, and sends signals to MCHIP and HCHIP for address decoding and other purposes. MCHIP activates the correct control signals to the DRAM including refresh cycles. HCHIP creates a VESA Local or ¡486 host bus with the signals necessary to interface to Intel compatible peripheral chips.

The external buses of the system may run up to 33MHz. Both the VESA Local bus bus and R4x00 processor bus operate at the same frequency. This speed provides optimal performance for host bus transfers while allowing simple synchronization of the host and processor buses. The R4x00 bus is 64 bits wide, the VESA Local bus is 32 bits wide.

The LogiCore chip set supports parity except on the host bus and is designed for little-endian cache, memory and VESA Local bus transactions.

The block diagram above illustrates the basic interconnections of the LogiCore Chip Set to other components in the system.

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