ADC Architectures I: The Flash Converter

by Walt Kester

INTRODUCTION

Commercial flash converters appeared in instruments and modules of the 1960s and 1970s and quickly migrated to integrated circuits during the 1980s. The monolithic 8-bit flash ADC became an industry standard in digital video applications of the 1980s. Today, the flash converter is primarily used as a building block within subranging "pipeline" ADCs. The lower power, lower cost pipeline architecture is capable of 8- to 10-bits of resolution at sampling rates of several hundred MHz. Therefore, higher power stand-alone flash converters are primarily used in 6- or 8-bit ADCs requiring sampling rates greater than 1 GHz. These converters are usually designed on Gallium Arsenide processes.

Because of their importance as building blocks in high resolution pipeline ADCs, it is important to understand the fundamentals of the basic flash converter. This tutorial begins with a brief discussion of the comparator which is the basic building block for flash converters.

THE COMPARATOR: A 1-BIT ADC

As a changeover switch is a 1-bit DAC, so a comparator is a 1-bit ADC (see Figure 1). If the input is above a threshold, the output has one logic value, below it has another. Moreover, there is no ADC architecture which does not use at least one comparator of some sort.

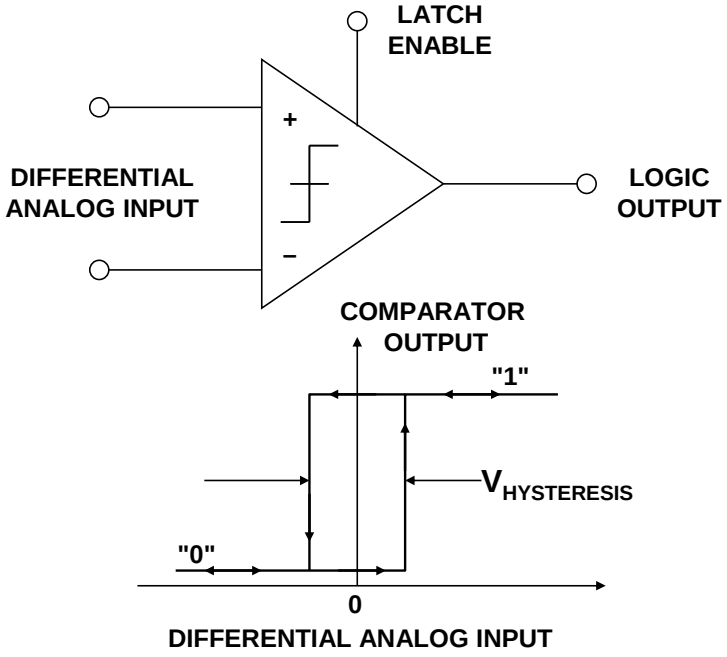


Figure 1: The Comparator: A 1-Bit ADC

The most common comparator has some resemblance to an operational amplifier in that it uses a differential pair of transistors or FETs as its input stage, but unlike an op amp, it does not use external negative feedback, and its output is a logic level indicating which of the two inputs is at the higher potential. Op amps are not designed for use as comparators—they may saturate if overdriven and recover slowly.

Many op amps have input stages which behave in unexpected ways when used with large differential voltages, and their outputs are rarely compatible with standard logic levels. There are cases, however, when it may be desirable to use an op amp as a comparator, and an excellent treatment of this subject can be found in Reference 1.

Comparators used as building blocks in ADCs need good resolution which implies high gain. This can lead to uncontrolled oscillation when the differential input approaches zero. In order to prevent this, "hysteresis" is often added to comparators using a small amount of positive feedback.

Figure 1 shows the effects of hysteresis on the overall transfer function. Many comparators have a millivolt or two of hysteresis to encourage "snap" action and to prevent local feedback from causing instability in the transition region. Note that the resolution of the comparator can be no less than the hysteresis, so large values of hysteresis are generally not useful.

Early comparators were designed with vacuum tubes and were often used in radio receivers—where they were called "discriminators," not comparators. Most modern comparators used in ADCs include a built-in latch which makes them sampling devices suitable for data converters. A typical structure is shown in Figure 2 for the AM685 ECL (emitter-coupled-logic) latched comparator introduced in 1972 by Advanced Micro Devices, Inc. (see Reference 2).

The input stage preamplifier drives a cross-coupled latch. The latch locks the output in the logic state it was in at the instant when the latch was enabled. The latch thus performs a track-and-hold function, allowing short input signals to be detected and held for further processing. Because the latch operates directly on the input stage, the signal suffers no additional delays—signals only a few nanoseconds wide can be acquired and held. The latched comparator is also less sensitive to instability caused by local feedback than an unlatched one.

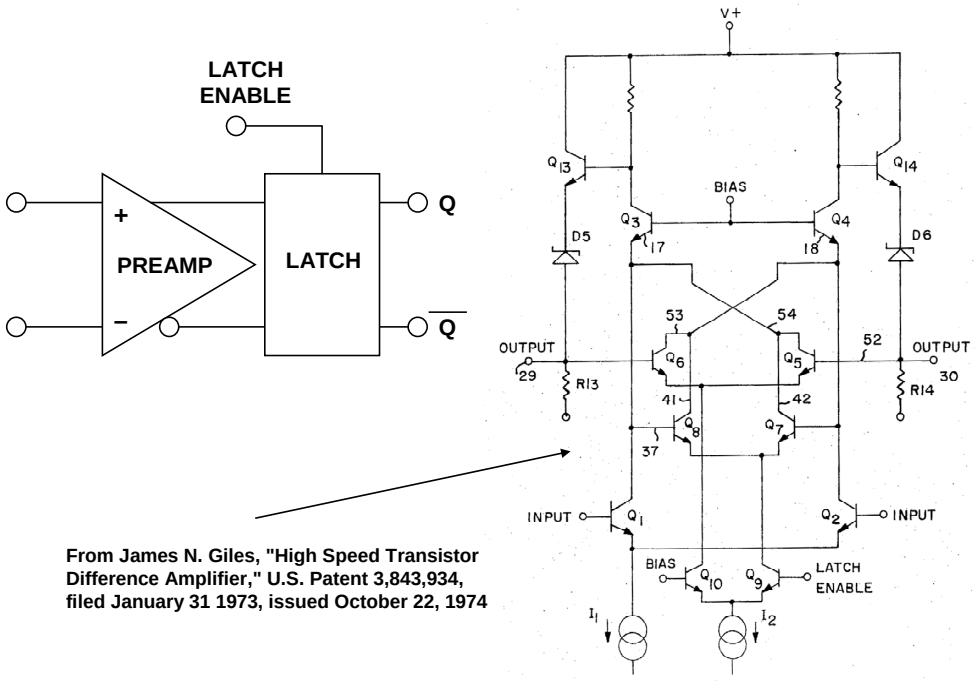


Figure 2: The AM685 ECL Comparator (1972)

Where comparators are incorporated into IC ADCs, their design must consider resolution, speed, overload recovery, power dissipation, offset voltage, bias current, and the chip area occupied by the architecture which is chosen. There is another subtle but troublesome characteristic of comparators which can cause large errors in ADCs if not understood and dealt with effectively. This error mechanism is the occasional inability of a comparator to resolve a small differential input into a valid output logic level. This phenomenon is known as "metastability"—the ability of a comparator to balance right at its threshold for a short period of time.

The metastable state problem is illustrated in Figure 3. Three conditions of differential input voltage are illustrated: (1) large differential input voltage, (2) small differential input voltage, and (3) zero differential input voltage. The approximate equation which describes the output voltage, $V_O(t)$ is given by:

$$V_O(t) = \Delta V_{IN} A e^{t/\tau}, \qquad \text{Eq. 1}$$

Where ΔV_{IN} = the differential input voltage at the time of latching, A = the gain of the preamp at the time of latching, τ = regeneration time constant of the latch, and t = the time that has elapsed after the comparator output is latched (see References 3 and 4).

For small differential input voltages, the output takes longer to reach a valid logic level. If the output data is read when it lies between the "valid logic 1" and the "valid logic 0" region, the data can be in error. If the differential input voltage is exactly zero, and the comparator is perfectly balanced at the time of latching, the time required to reach a valid logic level can be quite long (theoretically infinite). However, hysteresis and noise on the input makes this

condition highly unlikely. The effects of invalid logic levels out of the comparator are different depending upon how the comparator is used in the actual ADC.

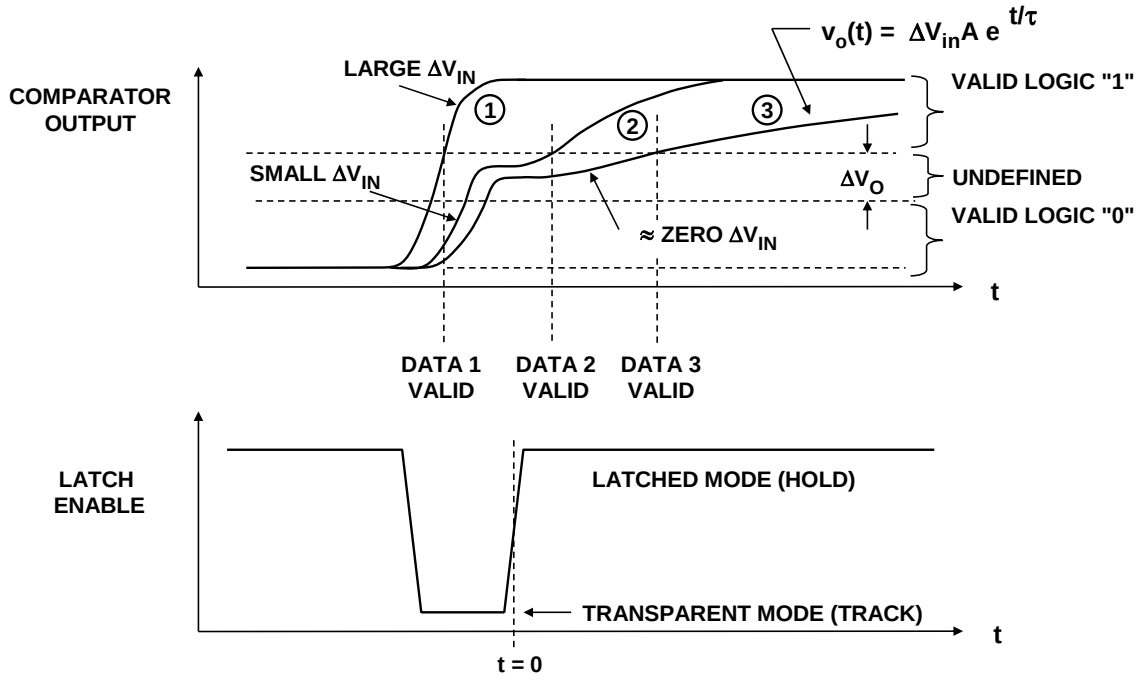


Figure 3: Comparator Metastable State Errors

From a design standpoint, comparator metastability can be minimized by making the gain, A, high, minimizing the regeneration time constant, τ, by increasing the gain-bandwidth of the latch, and allowing sufficient time, t, for the output of the comparator to settle to a valid logic level. It is not the purpose of this discussion to analyze the complex tradeoffs between speed, power, and circuit complexity when optimizing comparator designs, but an excellent treatment of the subject can be found in References 3 and 4.

From a user standpoint, the effect of comparator metastability (if it affects the ADC performance at all) is in the "bit error rate" (BER)—which is not usually specified on most ADC data sheets. The resulting errors are often referred to as "sparkle codes", "rabbits", or "flyers."

Bit error rate should not be a problem in a properly designed ADC in most applications, however the system designer should be aware that the phenomenon exists. An application example where it can be a problem is when the ADC is used in a digital oscilloscope to detect small-amplitude single-shot randomly occurring events. The ADC can give false indications if its BER is not sufficiently small. More discussion of sparkle codes can be found in Tutorial MT-011.

FLASH CONVERTERS

Flash ADCs (sometimes called "parallel" ADCs) are the fastest type of ADC and use large numbers of comparators. An N-bit flash ADC consists of 2^N resistors and $2^N - 1$ comparators arranged as in Figure 4. Each comparator has a reference voltage from the resistor string which is 1 LSB higher than that of the one below it in the chain. For a given input voltage, all the comparators below a certain point will have their input voltage larger than their reference voltage and a "1" logic output, and all the comparators above that point will have a reference voltage larger than the input voltage and a "0" logic output. The $2^N - 1$ comparator outputs therefore behave in a way analogous to a mercury thermometer, and the output code at this point is sometimes called a "thermometer" code. Since $2^N - 1$ data outputs are not really practical, they are processed by a decoder to generate an N-bit binary output.

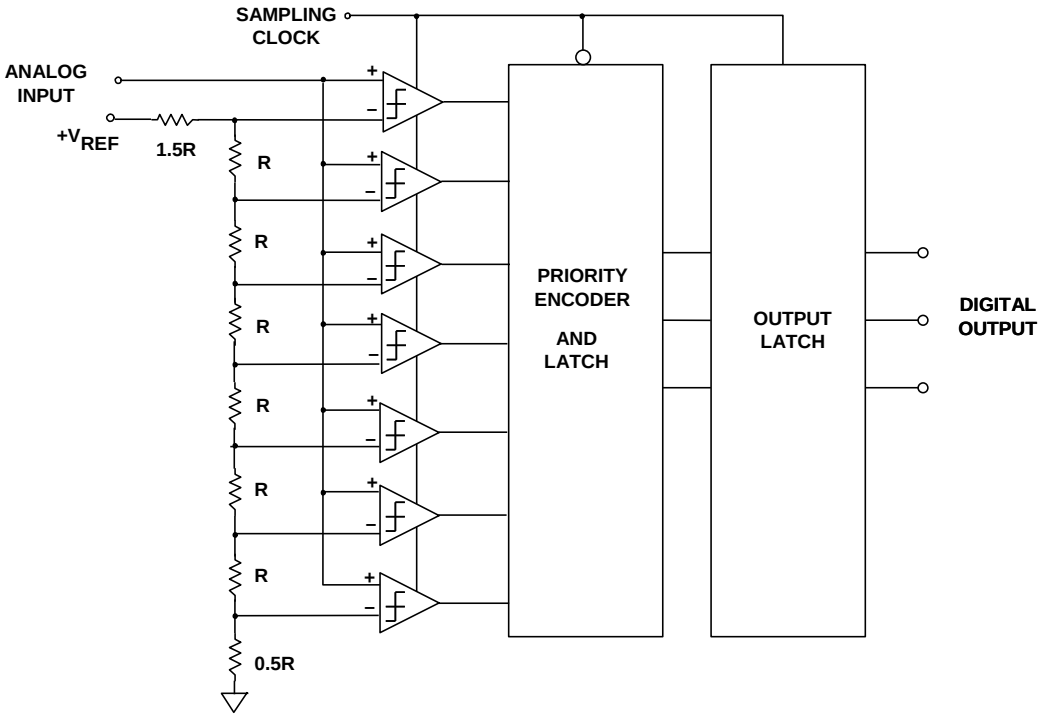


Figure 4: 3-bit All-Parallel (Flash) Converter

The input signal is applied to all the comparators at once, so the thermometer output is delayed by only one comparator delay from the input, and the encoder N-bit output by only a few gate delays on top of that, so the process is very fast. In addition, the individual comparators provide an inherent "sample-and-hold" function, so theoretically a flash converter does not need a separate SHA, provided the comparators are perfectly dynamically matched. In practice, however, the addition of a proper external sample-and-hold usually enhances the dynamic performance of most flash converters because of the inevitable slight timing mismatches which occur between comparators.

Because the flash converter uses large numbers of resistors and comparators and is limited to low resolutions, and if it is to be fast, each comparator must run at relatively high power levels. Hence, the problems of flash ADCs include limited resolution, high power dissipation because of the large number of high speed comparators (especially at sampling rates greater than 50 MSPS), and relatively large (and therefore expensive) chip sizes. In addition, the resistance of the reference resistor chain must be kept low to supply adequate bias current to the fast comparators, so the voltage reference has to source quite large currents (typically > 10 mA).

TYPICAL FLASH CONVERTER TIMING

Simplified timing for an early commercial flash converter (AD9048 8-bit, 35 MSPS) is shown in Figure 5. The input comparators are in the "track" or "transparent" mode when the sampling clock is low. The rising edge of the sampling clock places the comparators in the "hold" or "latched" mode. During the "hold" time, the decoding logic makes its decision based on the comparator outputs. The falling edge of the sampling clock latches the decoded data into an intermediate latch. The next rising edge of the sampling clock transfers the decoded data into an output latch. Note that this results in one cycle of "pipeline delay" in the output data with respect to the corresponding sampling clock edge. The intermediate latch allows for more sophisticated two-stage decoding methods. For instance, the comparator output data might first be decoded as a Gray code, latched on the falling edge of the sampling clock, and converted to binary during the "track" interval. The two-stage decoding is often used to minimized "sparkle codes" which are due to incorrectly interpreting a comparator output. (See Tutorial MT-011 for a complete discussion of sparkle codes and metastable state errors). Some flash converters use even more sophisticated decoding and therefore have more than one clock cycle of pipeline delay.

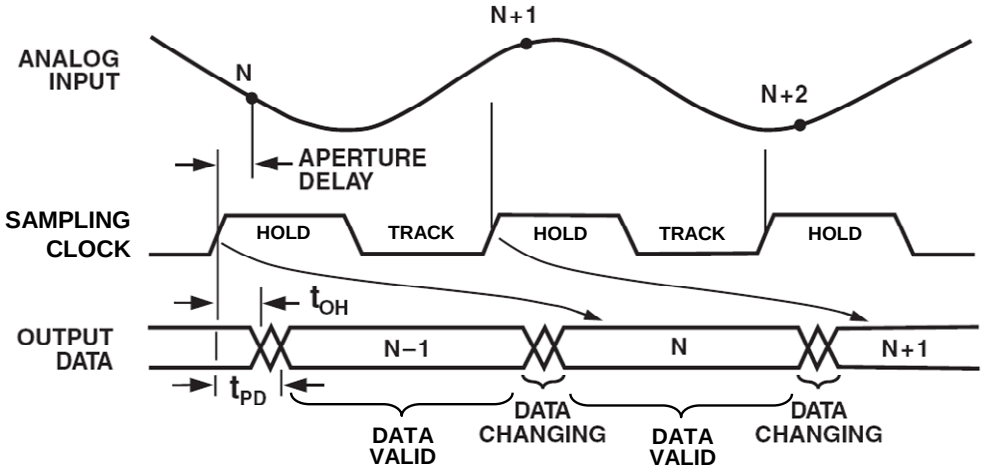


Figure 5: Data Timing for Typical Flash Converter (AD9048 8-bit, 35 MSPS)

If simple priority decoding is used, it would be possible to eliminate both the output latch and the intermediate latch and take the binary data directly from the output of the decoding logic. If this were the case, however, the output data is constantly changing during the "track" interval, thereby limiting the "DATA VALID" interval to one-half of the sampling clock period. It is therefore customary to use at least one latch so that the output data stays constant during the

entire sampling period, with the exception of the small amount of "DATA CHANGING" time shown in Figure 5.

FLASH CONVERTER HISTORICAL PERSPECTIVE

The first documented flash converter was part of Paul M. Rainey's electro-mechanical PCM facsimile system described in a relatively ignored patent filed in 1921 (Reference 5). In the ADC, a current proportional to the intensity of light drives a galvanometer which in turn moves another beam of light which activates one of 32 individual photocells, depending upon the amount of galvanometer deflection. Each individual photocell output activates part of a relay network which generates the 5-bit binary code as shown in Figure 6.

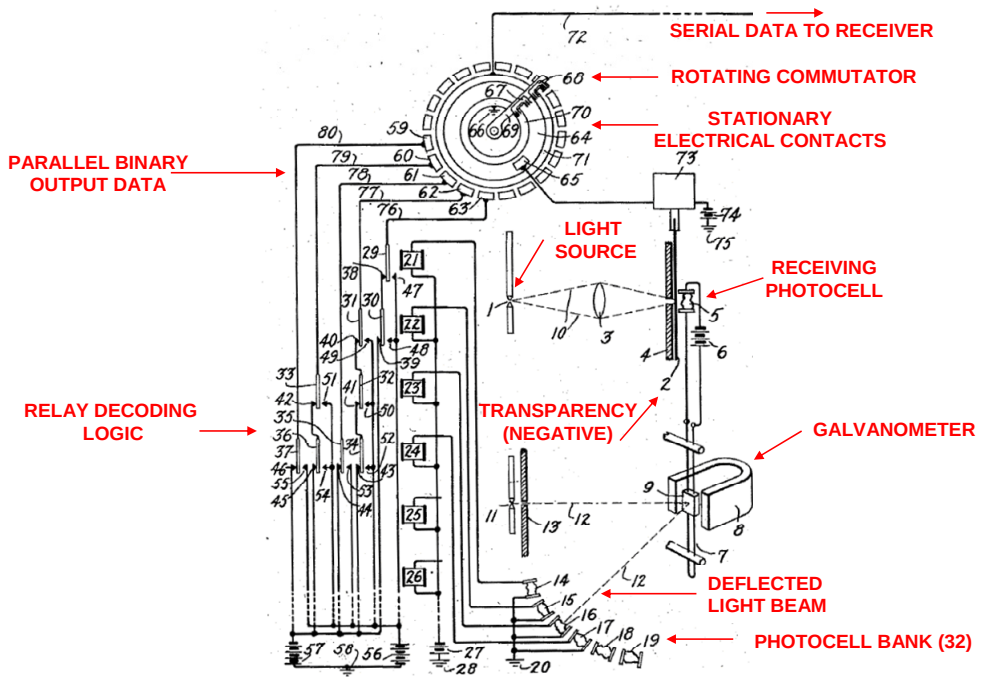


Figure 6: A 5-Bit Flash ADC Proposed by Paul Rainey
Adapted from Paul M. Rainey, "Facsimile Telegraph System," U.S. Patent 1,608,527, Filed July 20, 1921, Issued November 30, 1926

A significant development in high speed ADC technology during the 1940s was the electron beam coding tube developed at Bell Labs and shown in Figure 7. The tube described by R. W. Sears in Reference 6 was capable of sampling at 96 kSPS with 7-bit resolution. The basic electron beam coder concepts are shown in Figure 6 for a 4-bit device. The tube used a fan-shaped beam creating a "flash" converter delivering a parallel output word.

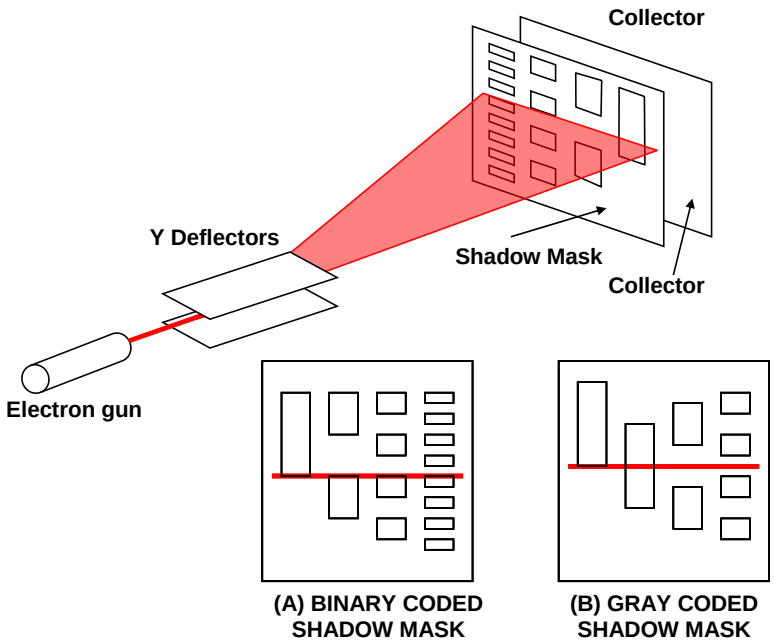


Figure 7: The Electron Beam Coder from Bell Labs (1948)

Early electron tube coders used a binary-coded shadow mask (Figure 7A), and large errors can occur if the beam straddles two adjacent codes and illuminates both of them. The errors associated with binary shadow masks were later eliminated by using a Gray code shadow mask as shown in Figure 7B. This code was originally called the "reflected binary" code, and was invented by Elisha Gray in 1878, and later re-invented by Frank Gray in 1949 (see Reference 7). The Gray code has the property that adjacent levels differ by only one digit in the corresponding Gray-coded word. Therefore, if there is an error in a bit decision for a particular level, the corresponding error after conversion to binary code is only one least significant bit (LSB). In the case of midscale, note that only the MSB changes. It is interesting to note that this same phenomenon can occur in modern comparator-based flash converters due to comparator metastability. With small overdrive, there is a finite probability that the output of a comparator will generate the wrong decision in its latched output, producing the same effect if straight binary decoding techniques are used. In many cases, Gray code, or "pseudo-Gray" codes are used to decode the comparator bank output before finally converting to a binary code output.

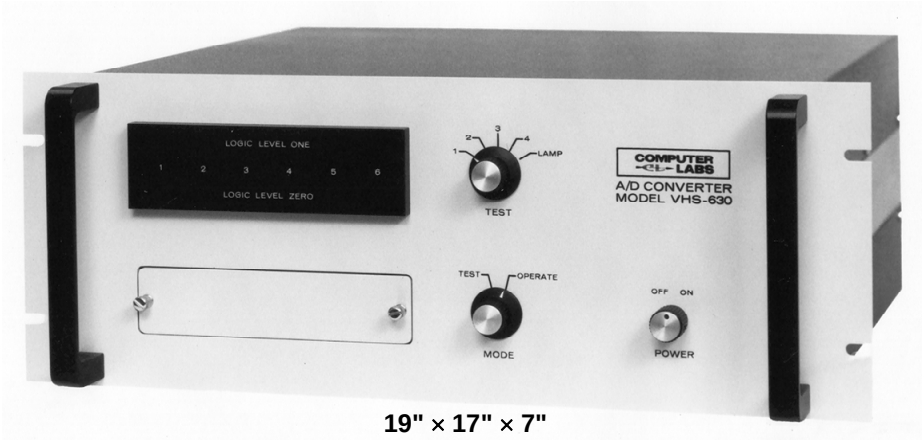
In spite of the many mechanical and electrical problems relating to beam alignment, electron tube coding technology reached its peak in the mid-l960s with an experimental 9-bit coder capable of 12-MSPS sampling rates (Reference 8). Shortly thereafter, however, advances in all solid-state ADC techniques made the electron tube technology obsolete.

It was soon recognized that the flash converter offered the fastest sampling rates compared to other architectures, but the problem with this approach is that the comparator circuit itself is quite bulky using discrete transistor circuits and very cumbersome using vacuum tubes.

Constructing a single latched comparator cell using either technology is quite a task, and extending it to even 4-bits of resolution (15 comparators required) makes it somewhat unreasonable. Nevertheless, work was done in the mid 1950s and early 1960s as shown in Robert Staffin and Robert D. Lohman's patent which describes a subranging architecture using both tube and transistor technology (Reference 9). The patent discusses the problem of the all-parallel approach and points out the savings by dividing the conversion process into a coarse conversion followed by a fine conversion.

Tunnel (Esaki) diodes were used as comparators in several experimental early flash converters in the 1960s as an alternative to a latched comparator based solely on tubes or transistors (see References 10-13).

In 1964 Fairchild introduced the first IC comparators, the µA711/712, designed by Bob Widlar. The same year, Fairchild also introduced the first IC op amp, the µA709—another Widlar design. Other IC comparators soon followed including the Signetics 521, National LM361, Motorola MC1650 (1968), AM685/687 (1972/1975). With the introduction of these building block comparators and the availability of TTL and ECL logic ICs, 6-bit rack-mounted discrete flash converters were introduced by Computer Labs, Inc., including the VHS-630 (6-bit, 30 MSPS in 1970) and the VHS-675 (6-bit, 75 MSPS in 1975). The VHS-675 shown in Figure 8 used 63 AM685 ECL comparators preceded by a high-speed track-and-hold, ECL decoding logic, contained a built-in linear power supply (ac line powered), and dissipated a total of 130 W (sale price was about $10,000 in 1975). Instruments such as these found application in early high speed data acquisition applications including military radar receivers.



19" × 17" × 7"

VHS-630
- **6-Bits, 30 MSPS**
- **32 dual MC1650 MECL III Comparators**
- **100 watts (linear power supplies included)**

VHS-675
- **6-Bits, 75 MSPS**
- **64 AM685 Comparators**
- **130 watts (linear power supplies included)**

Figure 8: VHS-Series ADCs from Computer Labs, Inc.VHS-630 (1970), VHS-675 (1975)

The AM685 comparator was also used as a building block in the 4-bit 100-MSPS board-level flash ADC, the MOD-4100, introduced in 1975 and shown in Figure 9.

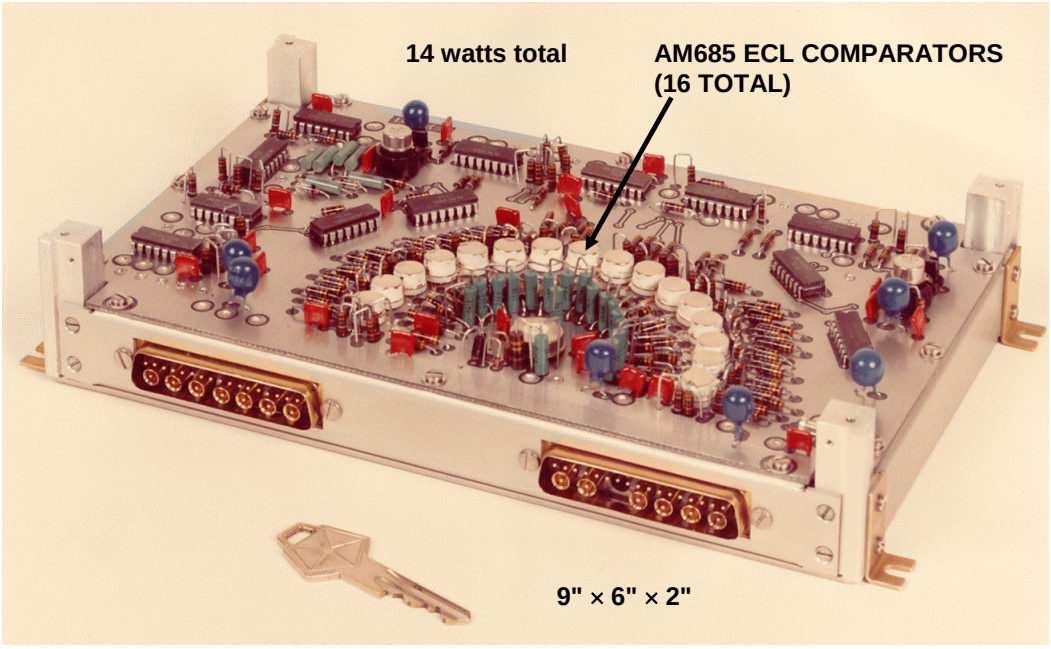


Figure 9: MOD-4100 4-Bit, 100-MSPS Flash Converter, Computer Labs, 1975

The first integrated circuit 8-bit video-speed 30-MSPS flash converter, the TDC1007J, was introduced by TRW LSI division in 1979 (References 14 and 15). A 6-bit version of the same design, the TDC1014J followed shortly. Also in 1979, Advanced Micro Devices, Inc. introduced the AM6688, a 4-bit 100-MSPS IC flash converter.

Monolithic flash converters became very popular in the 1980s for high speed 8-bit video applications as well as building blocks for higher resolution subranging card-level, modular, and hybrid ADCs. Examples from Analog Devices included the popular AD9048 (8-bit, 35 MSPS) and the AD9002 (8-bit, 150 MSPS). Many flash converters were fabricated on CMOS processes for lower power dissipation. Recently, however, the subranging pipeline architecture has become popular for 8-bit ADCs up to about 250 MSPS. For instance, the AD9480 8-bit 250-MSPS ADC is fabricated on a high speed BiCMOS process and dissipates less than 400mW compared to the several watts required for a full flash implementation on a similar process.

In practice, IC flash converters are currently available up to 10-bits, but more commonly they have 6- or 8-bits of resolution. Their maximum sampling rate can be as high as 1 GHz (these are generally made on Gallium Arsenide processes with several watts of power dissipation), with input full-power bandwidths in excess of 300 MHz.

But as mentioned earlier, full-power bandwidths are not necessarily full-resolution bandwidths. Ideally, the comparators in a flash converter are well matched both for dc and ac characteristics.

Because the sampling clock is applied to all the comparators simultaneously, the flash converter is inherently a sampling converter. In practice, there are delay variations between the comparators and other ac mismatches which cause a degradation in the effective number of bits (ENOBs) at high input frequencies. This is because the inputs are slewing at a rate comparable to the comparator conversion time. For this reason, track-and-holds are often required ahead of flash converters to achieve high SFDR on high frequency input signals.

The input to a flash ADC is applied in parallel to a large number of comparators. Each has a voltage-variable junction capacitance, and this signal-dependent capacitance results in most flash ADCs having reduced ENOB and higher distortion at high input frequencies. For this reason, most flash converters must be driven with a wideband op amp which is tolerant to the capacitive load presented by the converter as well as high speed transients developed on the input.

Comparator metastability in a flash converter can severely impact the bit error rate (BER). Figure 10 shows a simple flash converter with one stage of binary decoding logic. The two-input AND gates convert the thermometer code output of the parallel comparators into a "one-hot out of 7" code. The decoding logic is simply a "wired-or" array, a technique popular with emitter-coupled logic (ECL). Assume that the comparator labeled "X" has metastable outputs labeled "X". The desired output code should be either 011 or 100, but note that the 000 code (both gate outputs high) and the 111 code (both gate outputs low) are also possible due to the metastable states, representing a ½ FS error.

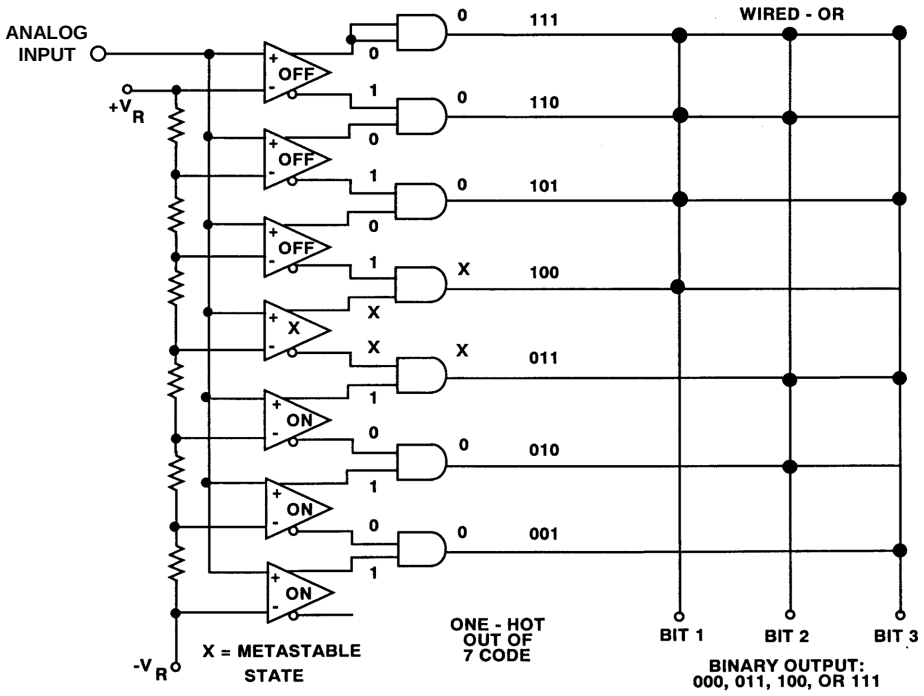


Figure 10: Metastable Comparator Output States May Cause Error Codes in Data Converters

Metastable state errors in flash converters can be reduced by several techniques, one of which involves decoding the comparator outputs in Gray code followed by a Gray-to-binary conversion as in the Bell Labs electron beam encoder previously described. The advantage of Gray code decoding is that a metastable state in any of the comparators can produce only a 1-LSB error in the Gray code output. The Gray code is latched and then converted into a binary code which, in turn, will only have a maximum of 1-LSB error as shown in Figure 11.

The same principles have been applied to several modern IC flash converters to minimize the effects of metastable state errors as described in References 3, 16, 17, for example.

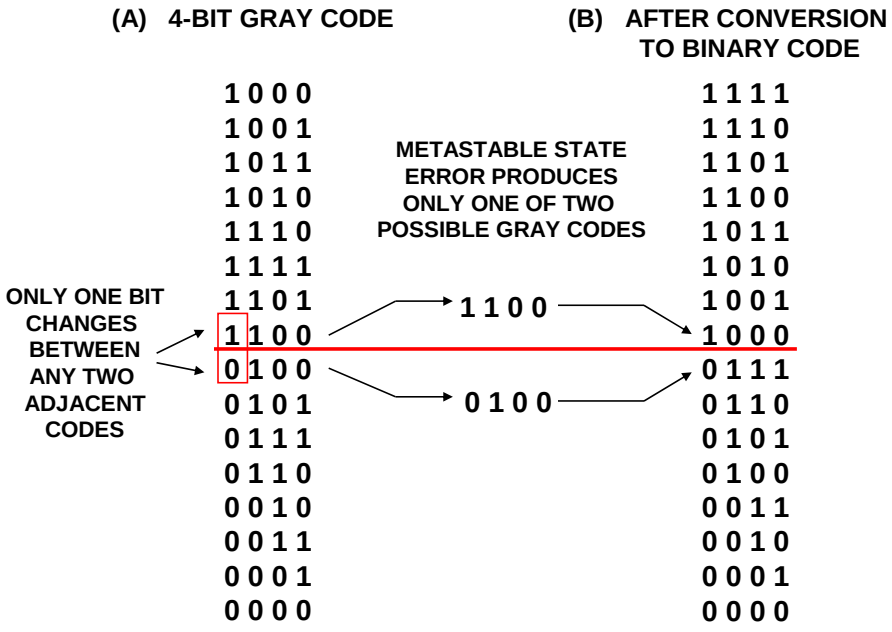


Figure 11: Gray Code Decoding Reduces Amplitude of Metastable State Errors

Power dissipation is always a big consideration in flash converters, especially at resolutions above 8 bits. A clever technique was used in the AD9410 10-bit, 210-MSPS ADC called "interpolation" to minimize the number of preamplifiers in the flash converter comparators and also reduce the power. The method is shown in Figure 12 (see Reference 18).

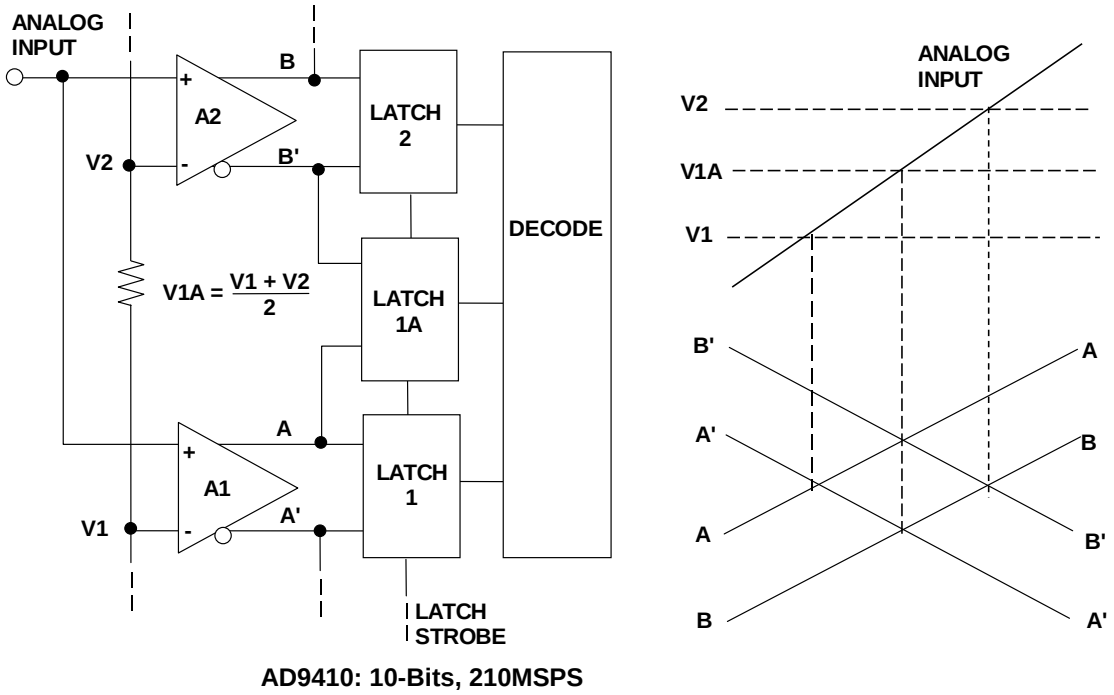


Figure 12: "Interpolating" Flash Reduces the Number of Preamplifiers by Factor of Two

The preamplifiers (labeled "A1", "A2", etc.) are low-gain g_m stages whose bandwidth is proportional to the tail currents of the differential pairs. Consider the case for a positive-going ramp input which is initially below the reference to AMP A1, V1. As the input signal approaches V1, the differential output of A1 approaches zero (i.e., A = A'), and the decision point is reached. The output of A1 drives the differential input of LATCH 1. As the input signals continues to go positive, A continues to go positive, and B' begins to go negative. The interpolated decision point is determined when A = B'. As the input continues positive, the third decision point is reached when B = B'. This novel architecture reduces the ADC input capacitance and thereby minimizes its change with signal level and the associated distortion. The AD9410 also uses an input sample-and-hold circuit for improved ac linearity.

SUMMARY

The flash converter still maintains its position as the fastest possible ADC architecture for a given IC process. However, power and real estate considerations generally limit the resolution to 6 or 8 bits. Commercial Gallium Arsenide flash converters are available with sampling rates over 1 GHz, however cost and power dissipation limit their popularity. Higher resolution, lower power, lower cost ADCs can be implemented at lower sampling rates (up to a few hundred MSPS) using the "pipeline" architecture. This technique makes use of low resolution flash converters as building blocks and is discussed in Tutorial MT-023.

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