

1 congatec Errata Sheet

Affected Products	conga-IA5, conga-MA5, conga-PA5, conga-QA5, conga-TCA5, conga-SA5
Subject	Errata sheet for congatec designs based on Intel Apollo Lake D.0 stepping or older
Confidential/Public	Confidential
Date (yyyy-mm-dd)	2017-07-26
Author	AEM

2 Affected Article Numbers

Product Data

Affected Part Number(s)	Product
Several	conga-IA5, conga-MA5, conga-PA5, conga-QA5, conga-TCA5, conga-SA5

3 General Information

This Errata Sheet provides information about limitations on congatec designs that are based on Intel Apollo Lake D.0 stepping or older.

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Intended Audience

This Errata Sheet is intended for technically qualified personnel. It is not intended for general audiences.

4 Errata Description

The congatec products listed in section 2 "Affected Article Numbers" feature Intel Apollo Lake SoCs with D.0 stepping or older.

During the lifetime simulation of these SoCs, Intel observed that under certain use cases, the LPC, USB (low speed and full speed), SD card and eMMC may stop functioning after several years.

For more information, see the following Intel Errata document at:

<https://www.intel.com/content/dam/www/public/us/en/documents/specification-updates/pentium-celeron-n-series-j-series-datasheet-spec-update.pdf?cache=no>

(Errata Number APL46)

4.1 LPC

LPC bus operating at 3.3V may degrade and stop functioning after several years if the use case is high. The product may not boot when this use case is reached.

4.1.1 Workaround

The LPC bus on congatec products operates at 3.3V. To reduce the utilization of the LPC interface, the LPC_CLKRUN# feature in the congatec BIOS setup menu must be enabled. This feature decreases the degradation of the LPC interface.

In order to enable the LPC_CLKRUN# feature, the following conditions must be met:

- use BIOS version Rx17 or later
- use Board Controller firmware CBGCP429 or later
- in the BIOS Setup Menu under Chipset->Platform Controller Hub (PCH) submenu set Serial IRQ Mode to 'Quiet'
- in the BIOS Setup Menu under Chipset->Platform Controller Hub (PCH) submenu, set PCI CLOCK RUN or CLKRUN Logic feature (see note below) to 'Enabled'



Note

LPC devices on the carrier board will no longer function properly if this workaround is implemented.

The Platform Controller Hub (PCH) submenu setup node displays either PCI CLOCK RUN or CLKRUN Logic Feature depending on the BIOS version being used.

4.2 USB

Low speed and full speed USB devices may stop functioning after several years if the use case is high.



Note

This limitation does not apply to High-Speed (USB 2.0) or SuperSpeed (USB 3.0 / USB 3.1) devices.

4.2.1 Workaround

To prevent this issue:

- do not use low speed or full speed devices that operate at 3.3V signaling
 - if you use 3.3V signaling on the SoC's native USB port, keep the active time of the device below 12% (max. 60 TB transmit traffic over lifetime per port)



Note

USB 1.1 devices connected to the conga-xA5 through a USB 2.0 or USB 3.0 hub are not affected.

4.3 SD Card

SD Card may stop functioning after several years if the use case is high.

4.3.1 Workaround

- do not use SD-card as a boot device
- remove the SD-card from the system when not in use
- use UHS-I cards and operate them at 1.8V I/O voltage only.

4.4 eMMC

The eMMC may not function properly if active for more than 33 percent of the time.

4.4.1 Workaround

- keep the eMMC active for less than 33 percent of the time for embedded use case
- ensure the operating system sets the eMMC interface to RTD3 or D3 whenever the interface is not in use.

4.5 HDMI/DP Hot Plug Detect

On conga-SA5 and conga-MA5, the HPD (Hot Plug Detect) signal of the HDMI and DP interface may degrade after several years. This degradation may affect correct detection of the unplug events.

4.5.1 Workaround

No workaround is currently available.

Note

This limitation does not affect systems with permanently fixed DP/HDMI screen.

5 Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
1.0	2017-07-26	AEM	Initial release
1.1	2017-08-02	AME	Updated Workaround settings in section 4.1.1 bullets 3 and 4 and updated Note text
1.2	2017-08-09	AEM	Corrected BIOS revision in section 4.1.1 bullet 1