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COMPACT GRAPHENE FIELD EFFECT TRANSISTOR MODELING WITH QUANTUM CAPACITANCE EFFECTS

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ABSTRACT

A scaled down graphene field effect transistor (GFET) has been modeled by incorporating the quantum capacitance effects. The proposed GFET model scaled down to 90nm has been developed using compact model equations. Metal oxide gated compact GFET models have been modeled without considering variation of top gate capacitance with quantum capacitance effects. But the effects of deviation of quantum capacitance become more with scaling down and cannot be neglected. In this paper the compact drain current equation has been derived by incorporating the dependence of quantum capacitance on the channel voltage and on intrinsic parameters of the device has been considered. The parameters of interest for circuit design have been determined from current characteristics, transfer characteristics, trans-conductance, and transit frequency. As the measure of performance of the model library in a circuit is often defined as unit gate delay, we propose to determine the rise time and fall time of a single GFET inverter and present the results.

Keywords: graphene field effect transistor, quantum capacitance, small signal model, large signal model.

INTRODUCTION

The scaling of silicon has reached its physical limit and hence non silicon based devices are the key. Carrier mobility of graphene is much higher than silicon which makes it a promising material for field effect transistors (FETs).

During last few years, graphene field effect transistors (GFETs) are successfully modeled and they exhibit outstanding I-V characteristics suitable for RF applications. Many compact models using ballistic and drift diffusion approach exist today [1]–[3],[5]-[8].Electrolytic gated GFET model in [2] incorporates effects of quantum capacitance and the graphene-electrolyte interface of graphene. But the drain current equations of metal oxide gated GFETs [1], [3] have been derived without considering the variation in top gate capacitance due to quantum capacitance effects. But these effects become prominent in short channel transistors [4]. This model is a drift diffusion based model developed in 90nm technology where variation in top gate capacitance due to quantum capacitance effects has been taken into account.

The focus here is on the development of a compact model using closed form expression for individual graphene transistors at 90nm scale based on drift diffusion approach to determine drain current, trans-conductance and transit frequency. Compact model of 100 nm using drift diffusion is available [3]. The 90nm model incorporates quantum capacitance effects with a compatibility of being used in future circuit applications within a design environment and an analog mixed signal library of it has been developed by verifying the model in HSPICE.

This paper is organized as follows: Section II discusses the quantum capacitance and how to incorporate this into the model. Section III presents the formulation of the compact model for GFETs and Section IV presents the results and section V gives the conclusion.

QUANTUM CAPACITANCE

Quantum capacitance is the measure of energy needed to drive carriers into the conducting channel [9]. It varies with the density of carriers induced into the channel by electric field. Thus the derivative of total channel charge to the channel surface potential gives quantum capacitance. It plays an important role in the carrier transport characteristics.

Scaling down to nano-scale region makes the top gate capacitance comparable with quantum capacitance. A minimum quantum capacitance has been reported in [10] due to the presence of charge density in the locality of minimum conduction point. Total quantum capacitance is the sum of minimum (Cqmin) and variable quantum capacitance (Cqv) and is given by,

$$C_q = C_{q\min} + C_{qv} \tag{1}$$

The reduced expression for measurement of quantum capacitance with respect to channel voltage has been given in [4] and is as follows:

$$C_q = \frac{2e^2 \left| n_g + n^* \right|^{1/2}}{(\hbar v_f)\sqrt{\pi}} \tag{2}$$

$$n_g = \left(\frac{eV_{ch}}{\hbar v_f \sqrt{\pi}} \right)^2 \tag{3}$$

where n^* is the charged impurity concentration, v_f is the velocity at Fermi level , $\hbar$ is reduced Planck's constant ,n_g is the carrier concentration induced by the gate voltage, V_{ch} is the channel voltage which depends on V_{ds} and V_{gs}, and e is the electronic charge. C_c, the capacitance between top gate and channel comes in series with the quantum capacitance and is,

$$C_c = \frac{C_{g0}\varepsilon_0\varepsilon_r}{t_{ox}} \quad (4)$$

where C_{g0} is the parameter for reduction in gate capacitance due to impurities and ε_0, ε_r are the permittivity of free space and dielectric respectively. Quantum capacitance in series with C_c gives the top gate capacitance and is,

$$C_{top} = \frac{2C_c e^2 \left|n_g + n^*\right|^{1/2}}{2e^2\left|n_g + n^*\right|^{1/2} + C_c(\hbar v_f)\sqrt{\pi}} \quad (5)$$

Figure-1 shows the GFET layout with quantum capacitance.

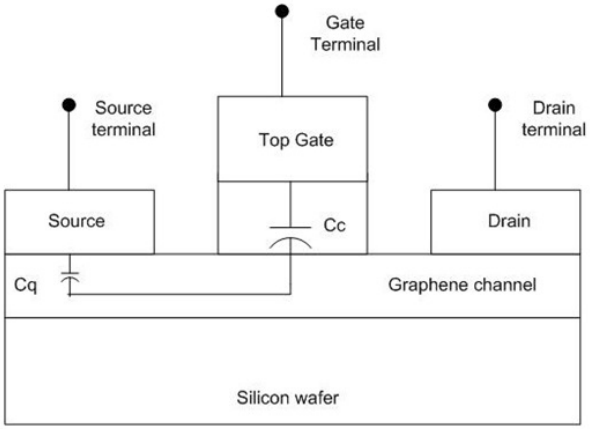

Figure-1. Layout of GFET.

GFET SHORT CHANNEL COMPACT MODEL

Large Signal Model

The drain current equation of [1] has been modified by using Equation.1 to Equation.5. Here the top gate capacitance is not a constant and depends on gate to source voltage unlike [1]. The regular parameters namely μ, ω, W, L and tox are used to determine the drain, trans-conductance and transit frequency characteristics as given in Equations 6 to 9. The drain current at any given voltage is,

$$I_D = \frac{\mu W k_1 V_{gs} V_{eff}}{\sqrt{k_2 V_{gs} + k_3}\left(\frac{L}{V_{ds}} + \frac{\mu}{\omega}\sqrt{\pi k_1 V_{gs}}\right)\sqrt{V_{eff}}} \quad (6)$$

where k_1, k_2 and k_3 are given as

$$k_1 = 2e^2\varepsilon_0\varepsilon_r, k_2 = 2e^3 t_{ox} \text{ and } k_3 = \varepsilon_0\varepsilon_r(\hbar v_f)^2\pi.$$

$$V_{tot} = V_{gs} + \frac{en_f}{C_c} \quad (7)$$

where nf is the net acceptor/donor doping.

The effective voltage is given as Veff = Vtot − (Vdsi/2) which is simplified with the assumption that the Vtot> Vdsi/2. The above model can be used to obtain the triode and saturation regions where the assumption Vtot> Vdsi/2 holds true.

Table-1. Parameter values.

Parameter	Value
μ	7000 cm² /Vs
ω	8.5*10⁻¹³Hz
ε_r	4
n*	10¹²/cm²
C_{g0}	1
v_f	1*10⁶ m/s
t_{ox}	5*10⁻⁹ m

Small Signal Model

Small signal modeling is to obtain the significant parameters like trans-conductance, transit frequency and gate capacitance. Transit frequency and trans-conductance plays a crucial role in amplifier circuits. Hence the analysis of these parameters is essential in modeling a transistor circuit.

- **Trans-Conductance**

Trans-conductance of a device is the derivative of the output current with the gate voltage. It is the main performance metric for two port devices, especially for amplifiers. The equation for trans-conductance can be derived from Equation. 6 and is given by,

$$g_m = I_d \times \left(\frac{1}{\sqrt{\frac{L}{V_{ds}} + \frac{\sqrt{I\mu\pi K_1}}{\omega}}}\left(\frac{1}{V_{gs}} + \frac{\mu V_{gs}}{I}\right) + \frac{K_2}{2WK_1 I\left[V_{gs}K_2 + K_3\right]}\right) \quad (8)$$

The equation has been derived with the binomial approximation $L/V_{ds} >>> \sqrt{I\mu\pi K_1/\omega}$ where I is, $\mu V_{gs}\sqrt{V_{tot} - V_{ds}/2}$

- **Transit Frequency**

Transit frequency is an important parameter in RF circuit design as it determines the speed of the device. The improvement in transit frequency enables us to develop analog devices of high performance. Transit frequency equation can be derived from Equation. 6, and given is,

RESULTS AND ANALYSIS

The derived expressions have been implemented in Matlab and VerilogA. Parameter values for quantum capacitance measurement [4] and of electrical compact model [1] have been taken for simulations. The GFETs under consideration are built utilizing hexagonal boron

nitride (h-BN) as gate dielectric with relative permittivity of 4 [11].

Results of MATLAB Implementation

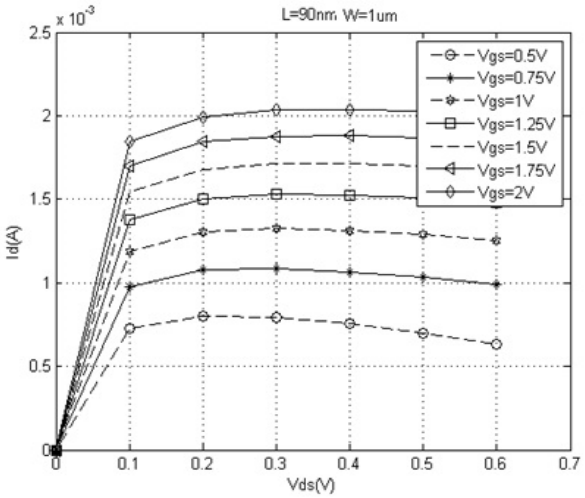

Figure-2. Id v/s Vds characteristics of the 90nm GFET model with tox=5nm, μ=7000 cm2 /Vs, ω=8.5*10-13Hz and relative permittivity=4.

Table-2. Drain current at L=440NM,L=100NM and L=90NM with VGS.

Parameter/Length	440nm [1]	100nm [3]	90nm
Drain current (mA)	1.21	1.41	2

Table-2 is the comparison of drain characteristics of the modified 90nm model with 440 nm and 100 nm models. Figure-2 has been plotted by sweeping the Vds value from 0 to 0.6 V. The simulation step size is 0.1 for Vds and 0.5 V for Vgs. Table-2 and Figure-2 shows that the drain current at maximum voltage is higher than that of model implemented at 440 nm and 100 nm. A saturation region has been achieved and hence this model can be used for voltage controlled current sources.

Figure-3 Shows the transfer characteristics of GFET v/s Vgs with L=90nm, tox=5nm, μ=7000 cm2 /Vs, ω=8.5*10-13Hz and relative permittivity=4.

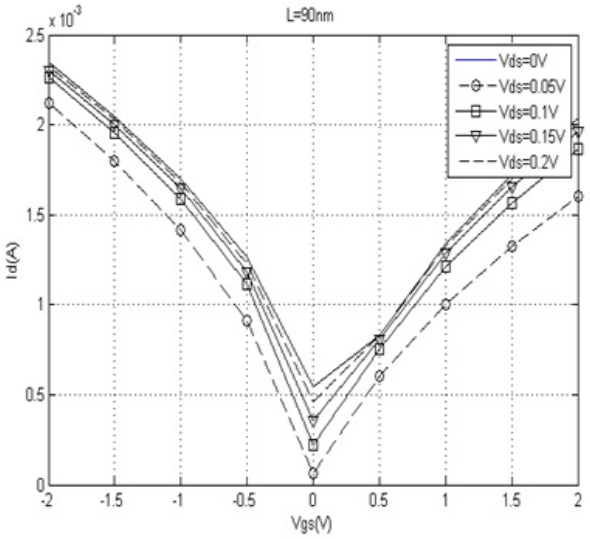

Figure-3. Represents the transfer characteristics of the model. The dirac point stability of the proposed model is for Vds<0.35V.

Figure-4 Shows the trans-conductance of GFET v/s Vgs with L=90nm, tox=5nm, μ=7000 cm2 /Vs, ω=8.5*10-13Hz and relative permittivity=4.

Table-3. Transconductance at L=440NM,L=100NM AND L=90NM.

Parameter/Length	440nm [1]	100nm [3]	90nm
Trans-conductance (mS)	0.91	1.12	1.25

Table-3 shows that the trans-conductance at maximum voltage is found to be improved than in [1] and [3].

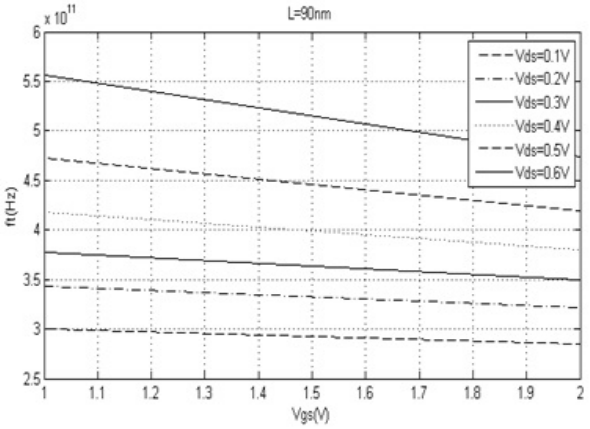

Figure 5. Shows the variation of transit frequency versus Vgs with L=90nm, tox=5nm, μ=7000 cm2 /Vs, ω=8.5*10-13Hz and relative permittivity=4.

Table-4. Transit frequency at L=440NM,L=100NM and L=90NM.

Parameter/Length	440nm [1]	100nm [3]	90nm
Transit frequency(GHz)	90	520	550

Table-4 shows that the transit frequency at maximum voltage has increased than in [1] and [3]. The graphs shown in Figure-4 and Figure-5 are the trans-conductance characteristics and transit frequency characteristics of the model. Trans-conductance and transit frequency decreases with increase in voltage. But, this reduction in values doesn't have an impact in scaled down GFET devices due to voltage scaling. Transit frequency of the model is in RF range and hence suitable for RF applications.

Hspice Implementation

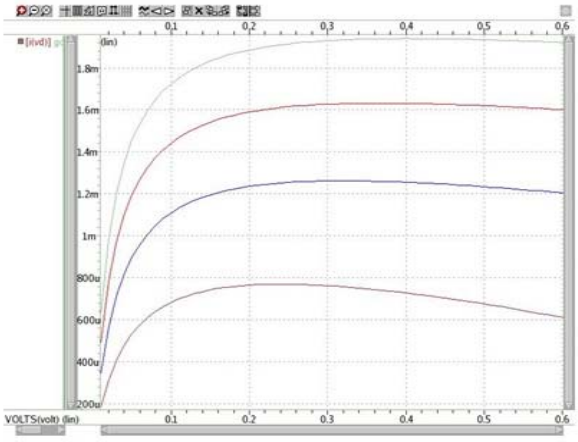

Figure-6. Shows the Id vs Vds characteristics of the Verilog-A model in HSPICE.

GFET Inverter

The GFET 90 nm verilogA model is used as a library to implement the circuit simulation in HSPICE with VDD = 5 V, Vss =-1.5 V and circuit parameters values from [12].

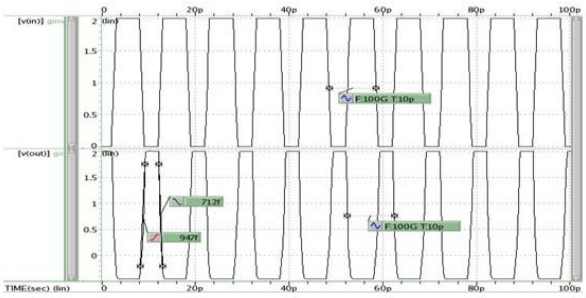

Figure-7. Shows the characteristics of the inverter using proposed model at 90nm.

Table-5. Comparison of GFET and CMOS based inverters.

Parameter	GFET	CMOS(Level 54)
Rise time	0.947	42.5
Fall time	0.712	16.8

The input-output characteristics of inverter graph in the Figure.7 shows that the GFET inverter shows better performance than CMOS inverter and 100nm GFET inverter. The switching speed of the inverter is high due to reduced rise time and fall time.

CONCLUSIONS

The significant contribution of our work is the scaling of the model to 90nm, incorporating the quantum capacitance effects in the drift diffusion model. The capacitance effect is more pronounced at 90nm which has been considered here using quantum capacitance leading to the determination of the carrier concentration more accurately and shows improved drain characteristics as reflected by the current values reported herein when compared with 440nm [1] and 100nm [3]. Analog –mixed signal model in HSPICE and its results back up the implementation results obtained from MATLAB. Significant improvement of the transit frequency and trans-conductance also has been noted for 90nm. The transit frequency has been improved by an amount of 30 GHz than the model at 100nm. The switching characteristic without considering load is 100GHz for the first level GFET inverter model. Contact resistances effects can be included for future modifications and determine the output resistance and its effect on switching frequency.

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