PF56/63

Sub-Assemblies Bulletin

MANOR ROYAL, CRAWLEY, SUSSEX, ENGLAND

MULLARD EQUIPMENT LIMITED

No.9 November, 1962

Guide to Circuit Blocks (Combi.Elements.)and their use in Digital Systems and Equipment - Part IV.

LOADING TABLE

The new loading table differs in some details from that previously issued, and generally gives slightly more flexibility. The main changes are as a result of an uprating of the maximum base input current of the transistors used from 5mA to 10mA. This means that, with the usual 1KΩ collector loads in the driving stage, the current into a direct base connection will be less than the new limit, though it was outside the old.

Where there are reductions in the figures these have generally been made as a result of a re-examination of worst case tolerances, particularly at the maximum temperature ratings.

The loading table is intended as a quick guide to safe loading factors under all circumstances, but often increased loading can be obtained by careful reference to the input and output data given in the individual data sheets.

For driving a given block there are one or more of 3 primary input requirements.

(a) Steady current* into the block (towards OV or +6V)
(b) Steady current out of the block
(c) Surge current out of the block

Category (a) includes IA's, EF's, PS's, FF direct inputs and OR - gates
(b) AND - gates
(c) includes a.c. inputs of FF's, OS's, PL's.

The G_S and G_R inputs of FF2's and PL's can best be considered as a type 'a' input for '1' signals and a type 'c' input for '0' signals.

* In these notes the electron current convention is used; with PNP transistor logic circuits, this generally means that current flow is in the same direction as information flow.

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Preceding Units		Driving Unit		MAXIMUM NUMBER OF DRIVEN UNITS											
			Output Terminal	FF1		FF2			And Gate	EF1	EF2	IA1	IA2	PS1	OS1
		Type		S_D R_D	S R	S_D R_D	P	G_S G_R	W	W	W	W	W	W	S
		FF1	Q, $\bar{Q}$	1[a]	4[c]	1[a]	4[c]	2	4	1	2	1	X	3[b]	4[c]
		FF2	Q, $\bar{Q}$	1[a]	4[c]	1[a]	4[c]	2	4	1	2	1	X	1[b]	4[c]
		And Gate	Q	X	X	X	X	X	X	X	1	X	1[d]	·1	X
	FF1			X	4[e]	X	4[e]	X	X	X	1	X	1[d]	1	4[e]
	FF2			X	4[ce]	X	4[ce]	X	X	X	1	X	1[d]	1	4[ce]
	OS1[f]			X	4[e]	X	4[e]	X	X	X	1	X	1[d]	1	4[e]
	PS1			X	2[e]	X	2[e]	X	X	X	1	X	1[d]	1	2[e]
FF1	IA1			X	4[e]	X	4[e]	X	X	X	1	X	1[d]	1	4[e]
FF2	IA1														
PS1	IA1														
PS1	IA2														
		EF1	Q	8[ar]	X	8[ar]	X	X	4	X	X	4	X	18[b]	X
			T	1[g]	X	1[g]	X	X	X	X	X	X	1	X	X
		IA1	Q	2[a]	4[h]	2[a]	4[h]	3	7 / 16[i]	2	5	3[j]	1	8[b]	4[h]
		And Gate	Q	X	X	X	X	X	X	X	X	X	1[l]	X	X
		EF2	D	1	X	1	X	X	X	X	X	X	X	X	X
			via Amp[k]	2[a]	4[h]	2[a]	4[h]	3	50[m]	2	5	2	1	8[b]	4[h]
	IA1	IA2	Q^n	2[a]	4[h]	2[a]	4[h]	3	60	2	5	3[j]	1	8[b]	4[h]
	IA2	And[d]		2[a]	X	2[a]	X	3[q]	X	2	5	3[j]	1	8[b]	X
		And[d]	Q^o	X	X	X	X	1	6	1	1	1	1	2[b]	X
		And[d]	Q^p	X	X	X	X	X	9	X	X	X	X	X	X
		PS1	Q	X	2	X	2	2	2	1	2	1	1	3[b]	2
		OS1	Q	1[a]	X	1[a]	X	X	X	1	2	1	X	3[b]	X
			$\bar{Q}$	2[a]	4	2[a]	4	3	3	2	5	2	X	8[b]	4

NOTES FOR CIRCUIT BLOCK LOADING TABLE

Or gate Unless specified otherwise an Or gate may be interposed between two units without influencing the number of units which can be driven. The a.c. inputs of FF1's, FF2's or OS1's, cannot be driven from it.

The 2 PL1 is normally used in conjunction with FF1 or FF2 circuit blocks. The input data are equivalent to those of the similar FF2 inputs. The output terminals are connected directly to the d.c. terminals of the FF1 or FF2.

(a) Each via a 4.7 KΩ resistor in series with a diode OA200, anode to driven unit.

(b) Each via a 18 KΩ resistor by-passed with a 330 pf capacitor.

(c) If any G_S and G_R terminals are also being driven the number is reduced to 1.

(d) Via an Or gate (with the bias resistor to the positive supply not connected), or via a diode OA200.

(e) The operating point is the back edge of the negative pulse through the And gate. This pulse must be at least 15 μs long.

(f) Using a $\bar{Q}$ terminal.

(g) Via a diode OA85 anode to driven unit.

(h) The chain must be driven by an FF1, FF2 or PS1.

(i) With the collector load not connected to the negative supply.

(j) This applies when driving only IA1's. When driving IA1's and any other units the equivalent figure is 2.

(k) A grounded emitter amplifier using an OC41 or 42, or the OC47 (as contained in the 2 EF1 block), with a 1 KΩ collector load.

(l) Only if the EF2 is driven directly by an And gate not by an And Or combination.

(m) This number is reduced to 27 if the EF2 is driven by And Or combination.

(n) With all collector loads used.

(o) With only terminals N1 or N2 connected to a negative supply.

(p) With all negative terminals disconnected.

(q) The maximum speed of operation is 30 Kc/s.

(r) Can be increased to 18 at a maximum ambient temperature of 49°C.

The input impedance of the blocks must be considered as well as their current requirements. The IA1's EF's and the G_S and G_R inputs of FF2's and PL's have a high impedance input and consequently must be fed from a voltage source which does not fall far from -6V when supplying the required current. The And-gates also have a high input impedance to '1' signals. On the other hand the IA2's, the PS1's and the direct input terminals of the FF's have low impedance inputs and consequently pull the output voltage of the driving unit up to almost 0V. It is therefore important to ensure that high input impedance circuits and low input impedance circuits are never fed from the same source. If such a mixture cannot be avoided it is possible to increase the input impedance by introducing a resistor (6K8 for the IA2 and FF direct inputs, 15KΩ for the PS1).

A low impedance input must not be driven directly by an FF or OS1, since these blocks have internal feedback connections and their operation will be prevented if any of their output terminals is held down.

And-gates pass current from the -6V line into the driving unit and are effectively in parallel with the collector load; consequently the collector load can be disconnected in IA1's and IA2's when these are driving And-gates, and hence the current normally fed through the collector load is available for driving additional And-gates. When the collector load is not used the output terminal of the driving unit may not go towards -6V even though the transistor is cut off, consequently this method of driving extra And-gates should not be used with FF's and OS's.

The loading table figures for units driving And-gates are given on the assumption that the driving unit provides all the current required by the And-gates. This is in fact seldom the case, and more usually the driving unit shares the And-gate load with other units. For maximum loading, therefore, all possible states of the And-gates should be considered and the current required from the driving source calculated for each state. This is not generally such a tedious operation as it appears at first sight, since a pattern can usually be found and only a few calculations need be made. For instance if 7 And-gates are to be driven by a single block, possibly gates A and B are held at 0V solely by the driving unit under consideration, giving a current requirement of 2 x (0.48 + 0.06n)mA - 'n' being the number of other inputs to the gate which are at -6V (here assumed to be 2 in each); possibly gates C and D are held at 0V by two driving blocks, giving a current requirement of $2 \times \frac{(0.48 + n.0.06)}{2}$mA; possibly gates E, F and G are held up by 4 driving blocks, giving a current requirement of $3 \times \frac{(0.48 + n.0.06)}{4}$mA. Thus the total current required for the state considered is under 2.5mA and consequently the load is within the capabilities of an FF1 or FF2.

It should be noted that the EF's and OR-gates do not produce positive edges suitable for driving the A.C. terminals of OS's and FF's.

OR-gates are virtually transparent, i.e. the driving source looks straight through them to what comes after. Hence, it is not possible to use OR-gates to increase fan-out. For example an And-gate will only drive a single IA2, and hence cannot drive two or more OR-gates with IA2's after them.

And-gates feeding A.C. input terminals require both surge current and steady current out of the block, and hence it is not permissible for an FF1 for instance to drive And-gates which in turn drive more than 4 A.C. input terminals.

2610/C95/B6/7½M/11/62

RANGE OF UNITS IN THE COMBI-ELEMENTS SERIES

The range of units available is being continually increased as the development of new types is completed, but the present range is as follows:

Circuit Block Description	Provisional Type No.	Final Type No.	Abbreviation
Pulse shaper	B1 649 01	B8 950 00	PS1
Flip-Flop	B1 649 02	B8 920 00	FF1
Twin 3 input AND gate	B1 649 03	B8 930 00	2.3A1
Twin 2 input AND gate	B1 649 04	B8 930 01	2.2A1
Emitter follower/ inverter amplifier	B1 649 07	B8 940 00	EF1/1A1
One shot multi-vibrator	B1 649 08	B8 950 01	OS1
Twin emitter follower	B1 649 09	B8 940 01	2EF1
Twin inverter amplifier	B1 649 10	B8 940 02	2IA1
Flip-Flop	2P 727 07	-	FF2
Pulse logic	2P 727 26	-	PL1
Twin emitter follower	2P 727 27	-	2EF2
Twin inverter amplifier	2P 727 28	-	2IA2
Twin 3 input OR gate	2P 727 29	-	2.3O1
Twin 2 input OR gate	2P 727 30	-	2.2O1

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CIRCUIT BLOCKS FOR DIGITAL EQUIPMENT
(Combi - Elements)

RF Jabon 6/63

ADVANTAGES OF USING CIRCUIT BLOCKS

Circuit design, drawing and system proving can be reduced considerably by adopting standard circuit blocks, made in large quantities and tested as functional elements. The M.E.L. range of circuit blocks includes flip-flops, amplifiers, pulse shapers, gates etc. and a block schematic diagram can be translated into working equipment in a remarkably short space of time.

Unless circuit blocks are used, it is advisable to start with a breadboard layout in order to prove that one circuit works satisfactorily with another. Where the equipment is to be made in quantity or where reliability is important it is necessary to check the effect of component variations, power line variations and temperature. This can be a very lengthy and expensive business. With circuit blocks the satisfactory operation of one circuit with another is guaranteed. Each circuit block is tested under marginal conditions and is guaranteed to work satisfactorily under these conditions. The block is guaranteed to drive a stated number of other circuits and to operate at well-defined input levels.

These circuit blocks are the outcome of considerable development. Special components have been developed, where necessary, before being incorporated into the circuit blocks. Some of the transistors used were developed specially for this application when it was found that ordinary commercial types did not meet the exceptionally high standard of reliability required. Exhaustive tests were carried out on the potting compounds used for these blocks, to ensure their reliability under all climatic conditions and any exceptional circumstances in which they were likely to be used. Fundamental research and statistical analysis on millions of joints were carried out to ensure that the soldering was of the highest possible standard.

This high standard of reliability is maintained in production by constant quality checks as the blocks are made.

PRINCIPLE

This range of transistorised circuits has been built up on the principle of D.C. gating; in general the signal transfer from one element to another is by D.C. levels. The flip-flops and other multi-vibrators can be triggered either by a D.C. signal or a voltage step (A.C. signal).

Depending on the applications the units can be used for non-synchronous or synchronous logic, the latter using block pulses. The data sheets on each circuit block give full details of rise times, speed of operation etc. and the limits of these are clearly specified.

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The inputs and outputs of different units can be interconnected directly and full information on the maximum load and input requirements is given in the loading table.

Since these specific data on the performance of the units can be considered as design data for the equipment there is no need to add a further safety factor. The limits are clearly specified and guaranteed.

CIRCUIT PERFORMANCE

Though the units function reliably with any combination of given tolerances in supply voltage and ambient temperature, the maximum operational safety margin and maximum life can be expected by using the units under conditions as close as possible to the values originally specified: plus 6 volts and minus 6 volts for the supply voltages, and 25°C (77°F) for the ambient temperature.

GENERAL TECHNICAL DATA ON CIRCUIT BLOCKS

SYMBOLS AND DEFINITIONS USED IN THE DATA SHEETS

When considering any equipment which uses circuit blocks, most engineers use some form of block diagram; the number of ways of drawing block diagrams is immense. We have adopted a simple convention in block diagrams used in these data sheets and these are described below. Using these conventions and writing in the boxes the abbreviated type number of the circuit block, a wireman can assemble a complete system in a very short space of time, with the minimum of drawing and instruction from the design engineer.

SIGNAL FLOW

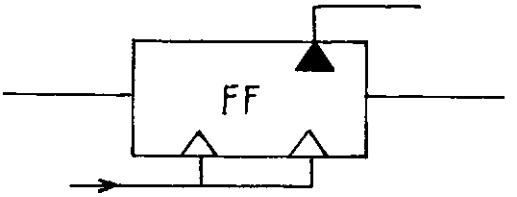
The direction of flow of information can be indicated with the aid of an arrow in the line connecting two blocks. Discrimination must be made between D.C. signals, where information is given by a D.C. voltage level, and A.C. signals, where the information is given by a voltage step derived from a pulse of short duration or from a fast variation of the D.C. level. The D.C. signal flow in a line is indicated by a solid black arrow, and the A.C. signal flow by an open arrow.

D.C.

A.C.

INPUT AND OUTPUT TERMINALS

These are indicated as shown below, again using the solid arrow for D.C. connections and the open arrow for A.C. connections. Where a unit has several input and output connections these can be marked with the appropriate letter as shown in the individual data sheets.



CURRENT DIRECTION

The direction of drive and load currents is called positive when running towards the unit i.e. when the terminal of the unit referred to is more positive than the other end of the line to which it is connected.

POWER LINES ETC.

These have no special indication except that, where appropriate, the supply or bias voltage is indicated on the diagram.

SET AND RESET

The starting position is that reached when the units have been reset; where appropriate this is marked by a black dot against the reset line or the terminal of the unit.

In the flip-flops the reset or start position is termed the "O" and the set condition is called "1" position.

BINARY LEVELS

The two binary levels, 0 and 1, have the following limits. Binary 0 is between +0.6 volts and -1.2 volts and binary 1 is between -3.6 and -6 volts. These voltages assume a negative supply line of -6 volts and a positive supply line of +6 volts. Symmetrical variation of the power lines will produce proportional changes in the limits of binary 0 and binary 1.

MECHANICAL INFORMATION

The dimensions of the circuit blocks are as follows: height 10 mm depth 24 mm width 54 mm. The weight is approximately 20 grammes (0.7 ozs).

The unit is hermetically sealed, and 10 terminals are brought out in the form of tinned wires 0.8 mm in diameter, all from one side of the unit. The ten terminals are numbered 1 to 10 from left to right looking at the pins with the type number on top.

COMBI-ELEMENTS FOR DIGITAL SYSTEMS

LOADING TABLE
Supply Voltage +6V and -6V ±10%

Chain of driving units									Maximum number of driven units													
First			Second			Third			FF1		FF2		OS1	IA1	IA2		FF1	FF2	PS1	AND	OR	Type
in	type	out	in	type	out	in	type	out	S,R or Parallel	S_dR_d	P	S_dR_d	S	W	W	W'	W	W	W	W	W	In
						S,R	FF1	Q	4	$1^{1)}$	4	$1^{1)}$	4	1			1	3	$4^{6)}$	$4^{7)}$	$\phi^{12)}$	
								$\bar{Q}$	4	$1^{1)}$	4	$1^{1)}$	4	1			1	3	$4^{6)}$	$4^{7)}$		
						W	FF2	Q	4	$1^{1)}$	4	$1^{1)}$	4	1			1	3	$4^{6)}$	$4^{7)}$	$\phi^{12)}$	
								$\bar{Q}$	4	$1^{1)}$	4	$1^{1)}$	4	1			1	3	$4^{6)}$	$4^{7)}$		
						S	OS1	Q	4	$1^{1)}$	4	$1^{1)}$	4	1			1	3	$4^{6)}$	$4^{7)}$	$\phi^{12)}$	
								$\bar{Q}$		$2^{1)}$		$2^{1)}$		2			2	6	$8^{6)}$	$4^{7)}$		
						W	IA1	Q	$4^{2)}$	$2^{1)}$	$4^{2)}$	$2^{1)}$	$4^{2)}$	2			2	6	$8^{6)}$	$8^{7)}$	$\phi^{12)}$	
			W	AND	Q	W'	IA2	Q		$2^{1)}$		$2^{1)}$		2			2	6	$8^{6)}$	$4^{7)}$	$\phi^{12)}$	
W	AND	Q	W	OR	Q																	
								Q	$4^{2)}$	$2^{1)}$	$4^{2)}$	$2^{1)}$	$4^{2)}$	2			2	6	$8^{6)}$	$60^{7)}$		
W	AND	Q	W	EF2	Q	W	IA2	$Q^{9)}$	$20^{2)}$	$8^{1)}$	$20^{2)}$	$8^{1)}$	$20^{2)}$	6			6	20	$25^{6)}$	$30^{7)}$		
								$Q^{10)}$	$30^{2)}$	$18^{1)}$	$30^{2)}$	$18^{1)}$	$30^{2)}$	12			12	40	$50^{6)}$			
						W	EF1	Q	$4^{2)3)}$	$8^{1)}$	$4^{2)3)}$	$8^{1)}$	$4^{2)3)}$	6					$25^{6)}$	$4^{7)}$	$\phi^{12)}$	
				IA1,2	Q	W	EF1	Q	$4^{2)3)}$	$18^{1)}$	$4^{2)3)}$	$18^{1)}$	$4^{2)3)}$	12					$50^{6)}$	$4^{7)}$		
				OS1	$\bar{Q}$	W	EF1	Q		$18^{1)}$		$18^{1)}$		12					$50^{6)}$	$4^{7)}$		
			W	AND	Q	W	EF2	Q		$1^{4)}$		$1^{4)}$				$1^{13)}$						
W	AND	Q	W	OR	Q	W	FF2	Q		1		1									$\phi^{12)}$	
						W	PS1	Q	2	$1^{1)}$	2	$1^{1)}$	2	1			1	1	$4^{6)}$	$2^{7)}$	$\phi^{12)}$	
						W	AND	Q	$4^{5)}$		$4^{5)}$		$4^{5)}$			1		1	1		1	
						W	OR	Q		$1^{8)}$		$1^{8)}$		$\phi^{11)}$		$\phi^{11)}$	$\phi^{11)}$	$\phi^{11)}$				

NOT PERMITTED

NOT RECOMMENDED

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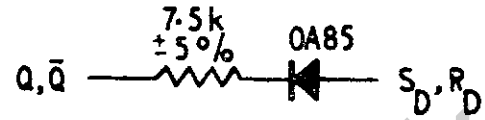
LOADING TABLE NOTES

1) Each via the following circuit:



2) Applies only if the chain of driving units is driven by an FF1-2, PS1 or OS1 (Q output).

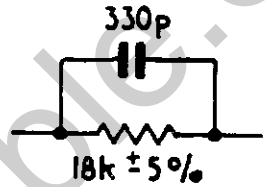
3) With diode OA 47 connected between W and Q of the EF1, cathode to Q.

4) In this instance the flip-flop is controlled directly by the emitter follower. The state of the flip-flop depends on the EF2 input level.

5) Applies only if the AND gate is driven by an FF1-2, PS1, OS1 (Q output) or a suitably driven IA1-2 (see under 2). The maximum speed is

$$\frac{30 \text{ kc/s}}{\text{number of driven units}}$$

6) Each via the following circuit:



7) Inputs of a single gate driven by the same unit count as one input.

8) Via a 7·5 kΩ ± 5% resistor.

9) With a 470Ω ± 5% resistor between Q and the negative supply.

10) With a 180Ω ± 5% resistor between Q and the negative supply.

11) The number of units that an OR gate can drive is equal to the number that the unit driving the OR gate can drive directly under the circumstances given in the Loading Table.

12) One OR gate may be applied between the last driving unit output and the DC input of an FF1, FF2, EF1, EF2, IA1 or IA2 (W' input) in all combinations given in the Loading Table.

13) Connection A of the EF2 must be connected to Q of the IA2.

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Circuit Blocks (Combi Elements)

Price List and Numbering Sheet

Type No.	Item Description	Circuit Code	Price £ s. d.
B8 800 15	Empty Combi Element Case	—	5 0
B8 920 00	Flip Flop	FF1	2 10 0
B8 920 01	Shift Register Flip Flop	FF2	2 10 0
B8 930 00	Twin 3 input AND gate	2.3A1	1 5 0
B8 930 01	Twin 2 input AND gate	2.2A1	1 0 0
B8 930 02	Twin 3 input OR gate	2.301	2 0 0
B8 930 03	Twin 2 input OR gate	2.201	1 10 0
B8 940 01	Twin Emitter Follower	2EF1	2 0 0
B8 940 02	Twin Inverter Amplifier	2IA1	2 0 0
B8 940 03	Twin Emitter Follower	2EF2	2 10 0
B8 940 05	Twin Inverter Amplifier	2IA2	2 10 0
B8 940 00	Emitter Follower/Inverter Amplifier	EF1/IA1	2 0 0
B8 950 00	Pulse Shaper	PS1	3 0 0
B8 950 01	One Shot Multivibrator	OS1	2 10 0
B8 850 00	Complete (4FF1) Decade Counter	DC1	12 10 0
P8 905 59	Printed Wiring Board for Decade Counter	—	10 0
P8 900 89	Experimenters Printed Wiring Board (Large—Undrilled)	—	3 0 0
P8 900 91/2	Experimenters Printed Wiring Board (Small—Drilled)	—	1 0 0
B8 930 04	Pulse Logic	2PL1	1 10 0
B8 960 00	Twin Selector Switch for Core Memories	2SS1	5 0 0
*2P 727 32	Pulse Generator for Core Memories	PG1	3 10 0
B8 930 05	Selection Gate for Core Memories	SG1	1 15 0
*2P 727 31	Read Amplifier for Core Memories	RA1	4 5 0

* Available late 1962.

NOTE 1. **QUANTITY DISCOUNTS ARE AVAILABLE.**

NOTE 2. NATO Stock Numbers available on request.

MULLARD EQUIPMENT LIMITED
Manor Royal,
Crawley, Sussex. Telephone: Crawley 28787

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MOUNTING AIDS FOR SUB-ASSEMBLIES

DATA SHEET

This chassis has been designed for the mounting of circuit blocks and is intended for use in a standard 19 in (48 cm) rack. Figure 1 shows that the chassis can contain a maximum of 24 standard printed-wiring boards, together with their mating connectors type F 042 CC/025. Details of the printed-wiring boards are given in separate data sheets.

TP262

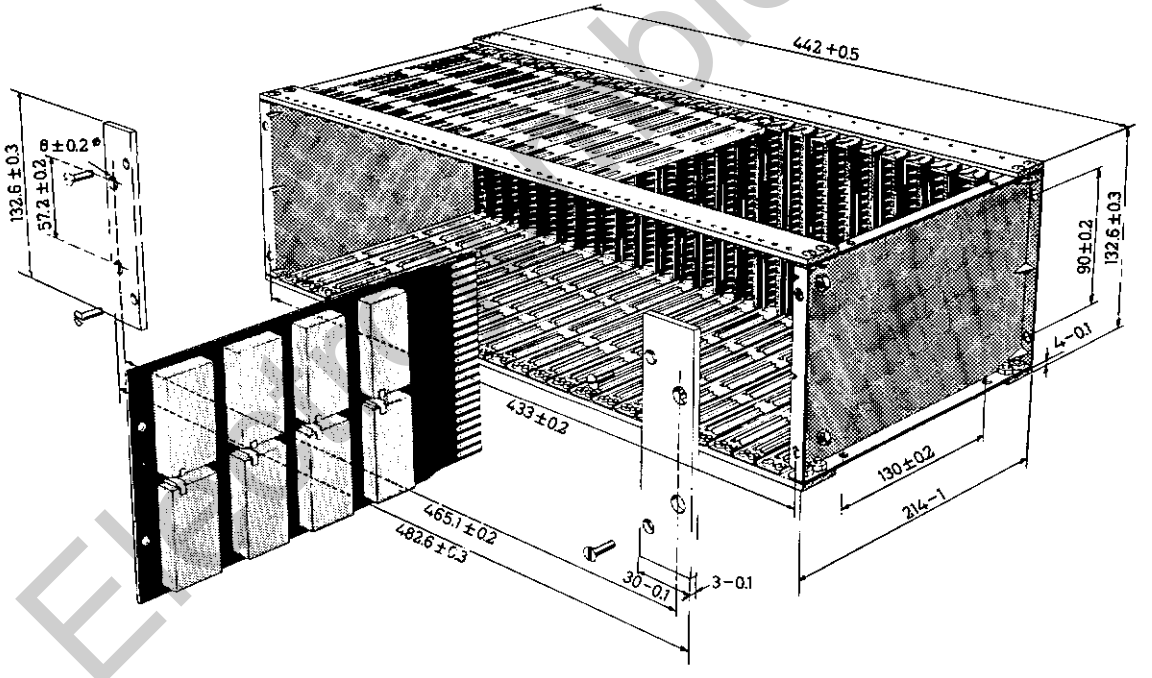

Fig. 1. Mounting Chassis Type B8 716 10

UNIVERSAL PRINTED-WIRING BOARD
(WITH PLATED-THROUGH HOLES) TYPE P8 906 15

DATA SHEET

Universal Printed-Wiring board type P8 906 15, one of three boards (all with similar outside dimensions) suitable for use with Mounting Chassis type B8 716 10 is illustrated in fig. 1. The thickness of the board is 1.6mm ($^1/_{16}$ in) and is provided with 23 single-sided, gold plated contacts. The layout complies with the I.E.C. standard grid, 2.54mm (.1 in).

TP263

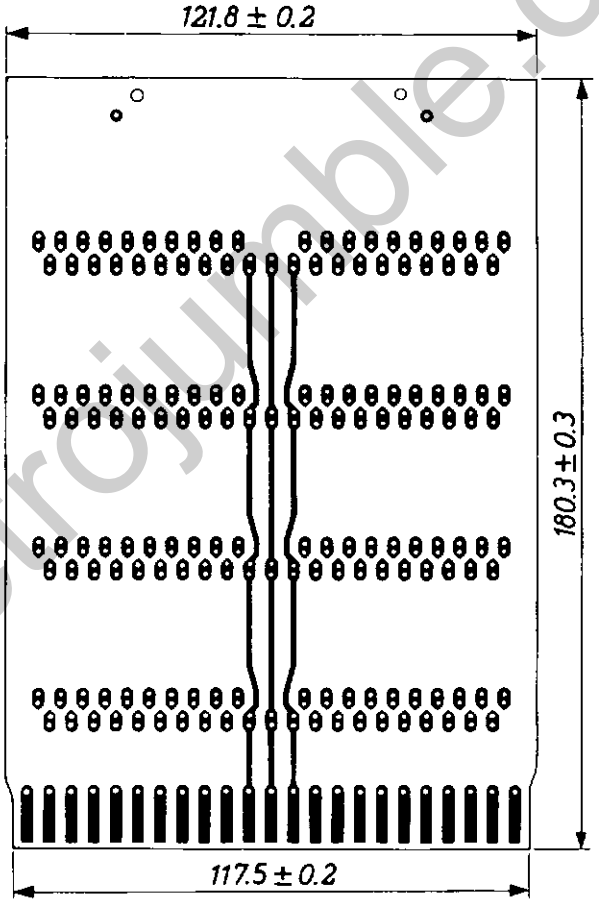

Fig. 1 Universal Printed-Wiring Board Type P8 906 15

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EXPERIMENTER'S PRINTED-WIRING BOARD (WITH PUNCHED HOLES) TYPE P8 906 11

DATA SHEET

Experimenter's Printed-Wiring Board type P8 906 11, one of three boards (all with similar outside dimensions) suitable for use with Mounting Chassis type B8 716 10, is illustrated in fig.1. The thickness of the board is 1.6mm ($^1/_{16}$ in) and is provided with 23 single-sided, gold-plated contacts. The layout complies with the I.E.C. standard grid, 2.54mm (.1 in).

TP261

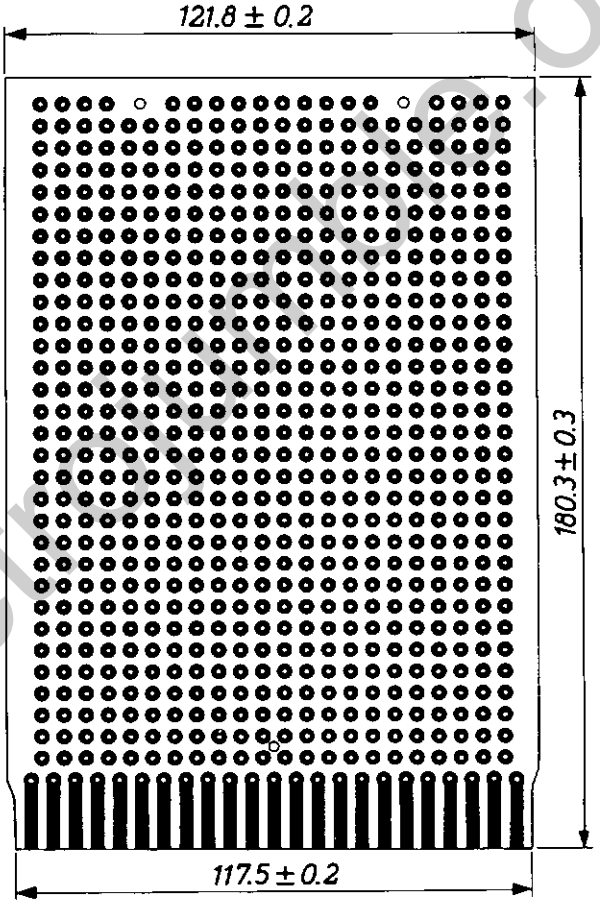

Fig.1. Printed-Wiring Board, Type P8 906 11

UNIVERSAL PRINTED-WIRING BOARD TYPE P8 901 46.2
(WITH PUNCHED HOLES)

DATA SHEET

Universal Printed-Wiring board type P8 901 46.2, one of three boards (all with similar outside dimensions) suitable for use with Mounting Chassis type B8 716 10, is illustrated in fig.1. The thickness of the board is 1.6mm ($\frac{1}{16}$ in) and is provided with 23 single-sided, gold-plated contacts. The layout complies with the I.E.C. standard grid, 2.54mm (.1 in).

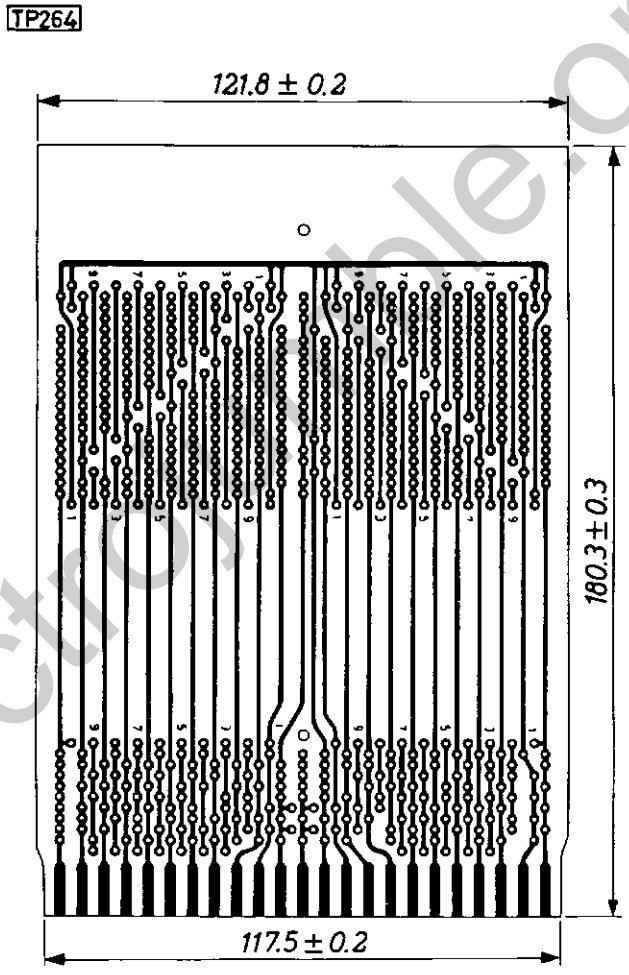

Fig.1 Universal Printed-Wiring Board Type P8 901 46.2

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MOUNTING CHASSIS TYPE B8 716 09

MOUNTING AIDS FOR SUB-ASSEMBLIES

DATA SHEET

This chassis has been designed for the mounting of circuit blocks and is intended for use in a standard 19 in (48 cm) rack. Figure 1 shows that the chassis can accommodate a maximum of 19 circuit blocks, mounted side by side. A number of these chassis can be mounted in a metal frame; six of them can be mounted side by side in a standard 19 in rack.

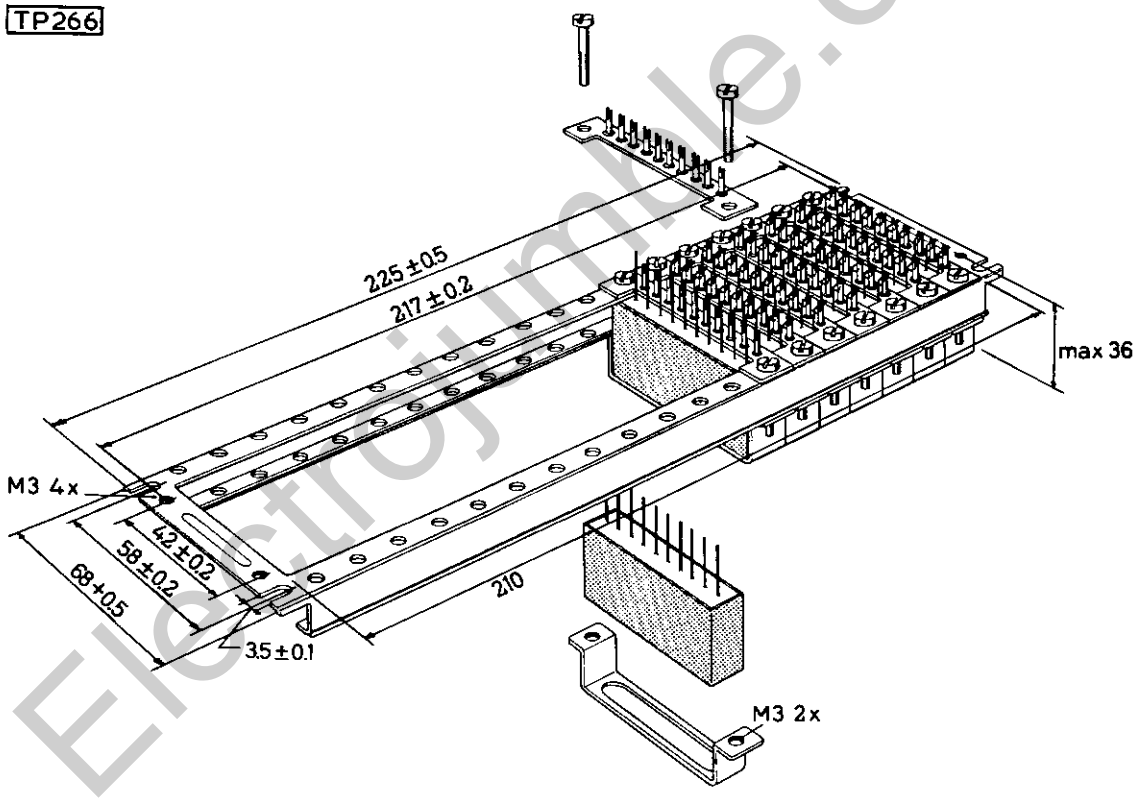

Fig. 1. Mounting Chassis Type B8 716 09

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TRANSISTOR COUNTER (DC1) B8 850 00

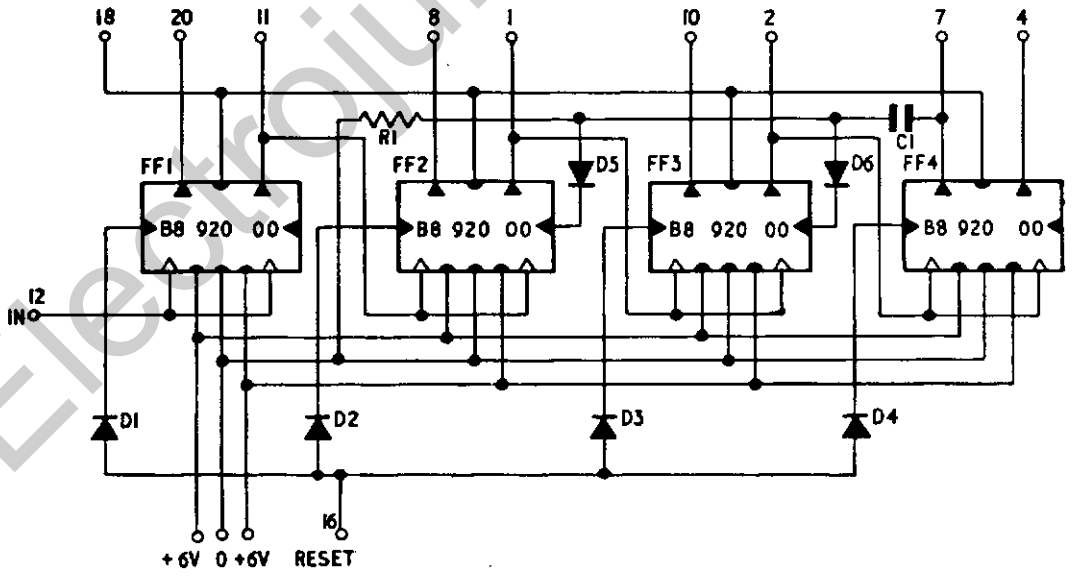
TERMINAL INDICATION

1 = Q_2 = Direct output of FF 2
2 = Q_3 = Direct output of FF 3
4 = Q_4 = Direct output of FF 4
7 = Q_4 = Inverted output of FF 4
8 = Q_2 = Inverted output of FF 2
10 = Q_3 = Inverted output of FF 3
11 = Q_1 = Direct output of FF 1
12 = IN = Input
14 = Ep_2 = To be connected to positive supply
15 = Eo = To be connected to common 0 V supply line
16 = RESET = Reset input
17 = Ep_1 = To be connected to positive supply
18 = Em = To be connected to negative supply
20 = $\overline{Q}$ = Inverted output of FF 1

CONSTRUCTION

The counter consists of four standard flip-flops type B8 920 00, mounted on a standard printed wiring board type P8 905 59, with plated-through holes and gold-plated plug-in contacts.

The mating printed wiring connector is not normally supplied with the counter and must be ordered separately under code number F 042ZZ/03.



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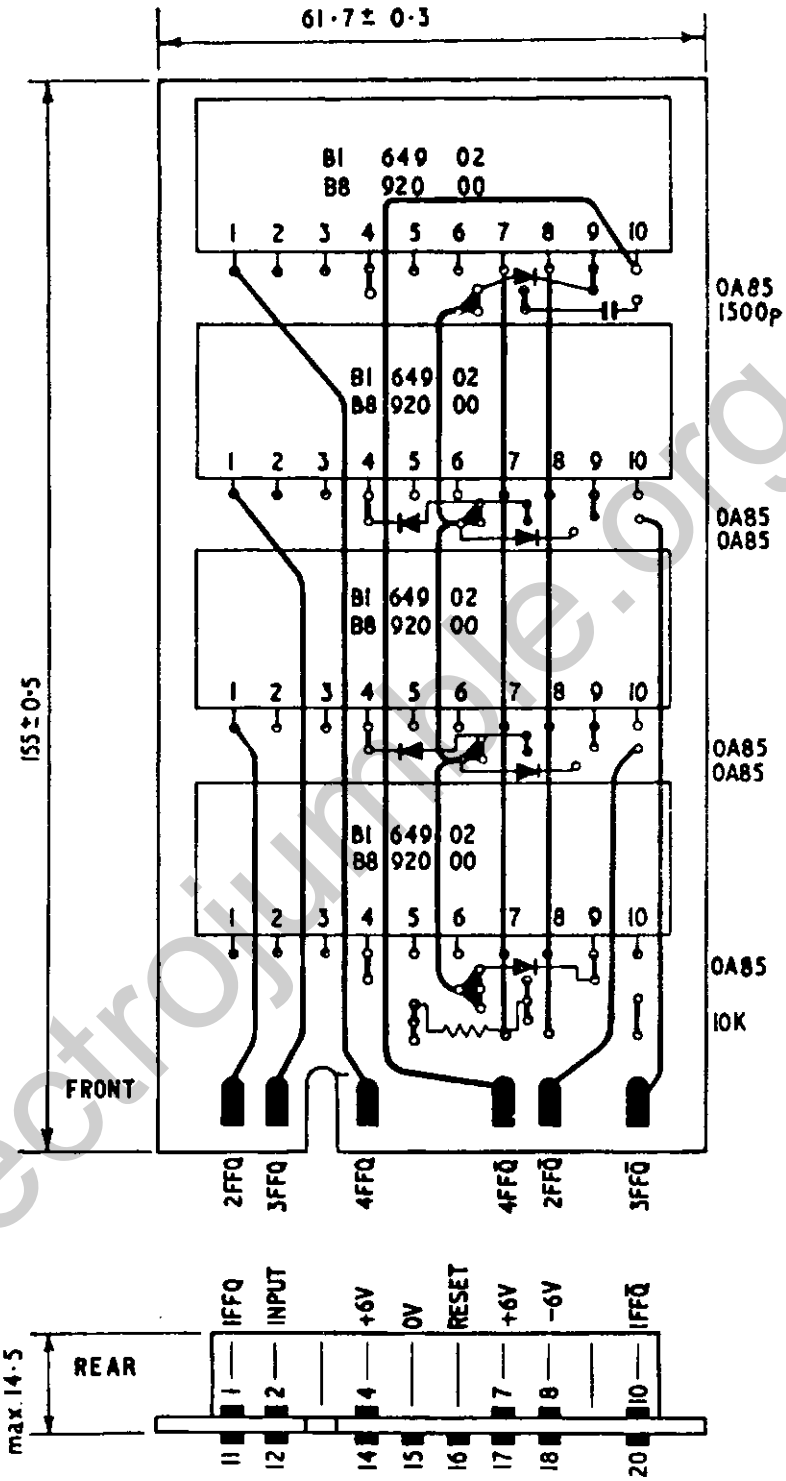


Circuit Block Decade Unit
B1 649 11

Transistor Counter 2of2

DC1

GENERAL PERFORMANCE

The counter is designed to operate at any pulse repetition frequency between 0 and 100,000 pulses per second.

Temperature range: - 20 to + 60° C
Supply voltages: - 6 V and + 6 V ± 10%.

The unit counts positive-going voltage steps applied to terminal 12 and may be reset by a positive voltage on terminal 16.

The counter operates in the binary/decimal code. The transition of FF 4 from the RESET to the SET position at the count position 8 is used to set FF 2 and FF3 by means of a built-in pulse feedback network. In this way 6 of the 16 possible count positions are skipped.

The RESET diodes D_1, D_2, D_3 and D4 and the feedback network D_5, D_6, R_1 and C_1 are mounted directly on the printed wiring board.

OUTPUT SIGNALS

The levels appearing on the output terminals during the count cycle can be taken from the following table.

Count	1		2		3		4		Flip-Flop No.
	11	20	1	8	2	10	4	7	Terminal
0	0	1	0	1	0	1	0	1	Binary "0" repre-
1	1	0	0	1	0	1	0	1	sents a voltage
2	0	1	1	0	0	1	0	1	level between
3	1	0	1	0	0	1	0	1	-0·1 Em V and 0·2
4	0	1	0	1	1	0	0	1	Em V
5	1	0	0	1	1	0	0	1	
6	0	1	1	0	1	0	0	1	
7	1	0	1	0	1	0	0	1	Binary "1" repre-
8	0	1	1	0	1	0	1	0	sents a voltage
9	1	0	1	0	1	0	1	0	level between
0	0	1	0	1	0	1	0	1	0·7 Em V and Em V

OUTPUT LOADING

Available output currents

binary "0" +0·5 mA
binary "1" -2·5 mA
(positive direction towards the unit)

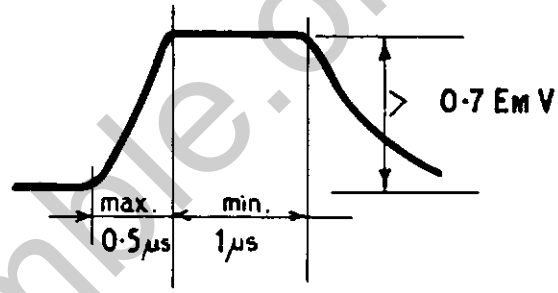
These loads may be applied to all outputs simultaneously.

Maximum capacitive loading for high speed operation:

1500 pF on terminal 7
2000 pF on all other output terminals

DRIVE SIGNALS

Input signal: in accordance with the following requirements:
The counter responds only to a positive-going voltage step. Em is the value of the negative supply voltage.



Reset signal (during RESET)
voltage, terminal 16: minimum +1V, maximum +10V.
current: 1 mA at +1V
2·8 mA at +10V

During counting, terminal 16 should be left floating or returned to a negative voltage source between -0·2 and -6V.

POWER SUPPLY

Two power supplies are needed, namely Em = -6V ± 10% 24 mA
Ep = +6V ± 10% 1·2 mA

The common return line is designated Eo.